STCF RICH PIDB progress

Speaker: Jiaming Li
On behalf of STCF RICH PIDB Group

University of Science and Technology of China
University of Chinese Academy of Sciences
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Outline

1、Physical requirements for STCF PIDB

2、RICH PIDB detector design

3、RICH PIDB readout electronics design

4、Conclusion

Outline

1、**Physical requirements for STCF PIDB**

2、RICH PIDB detector design

3、RICH PIDB readout electronics design

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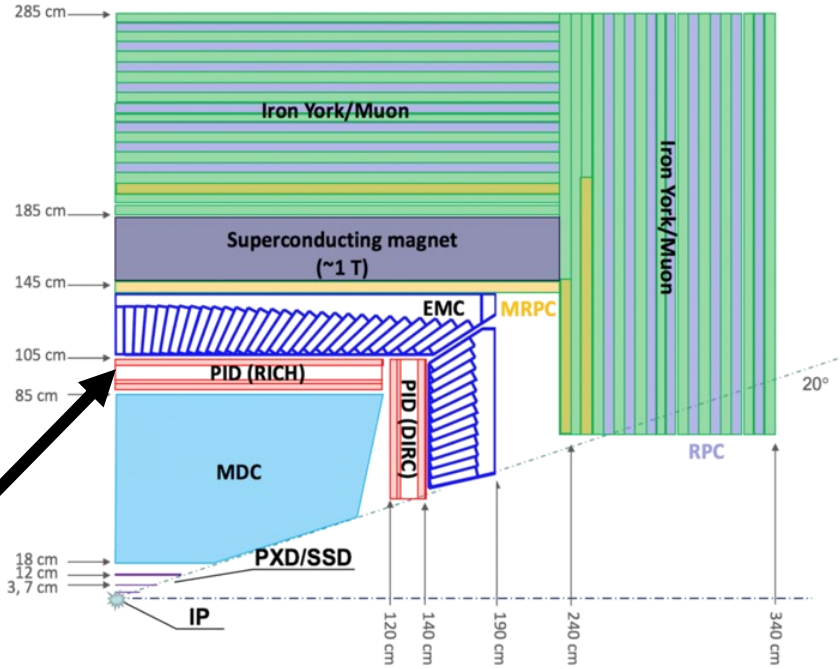
PIDB RICH Detector

- Expansion plan after the BESIII facility
- Center-of-mass energy extend to 2~7 GeV, luminosity up to 100 times ($0.5\sim1\times10^{35}$ cm^{-2} s^{-1})
- High event, background rate & large dynamic range vs high PID ratio



PID detector on barrel:
Ring Imaging Cherenkov Detector (RICH) with C_6F_{14} radiator,
reflective CsI photocathode,
hybrid amplification of THGEM-MicroMegas.

Technical Specification

- Covered area: 13 m²
- Thickness < 200 mm
- Material budget < 0.3 X_0
- Accumulated charge < 2 μC/cm² @ 10 year
- $K/\pi > 3\sigma$ @ 2.0 GeV/c
- MPGD: High gain(~10^5), low IBF(~10^{-3})
- Pixel size: 5×5 mm²
- Single Photon angular resolution: < 2.5 mrad

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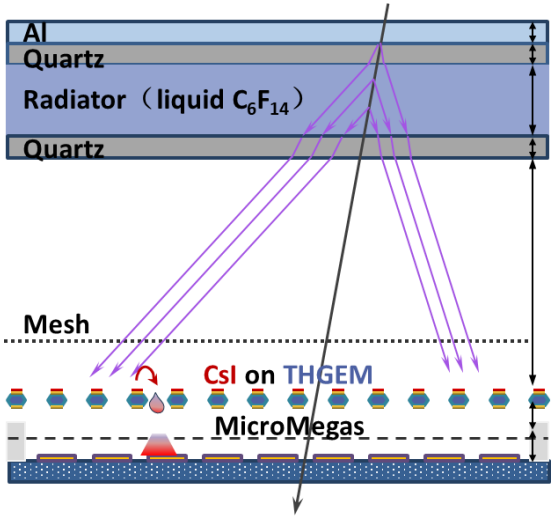
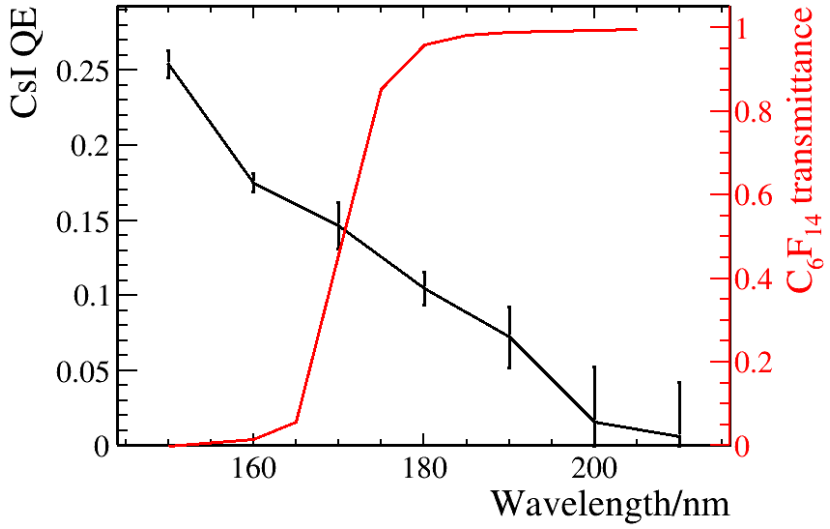
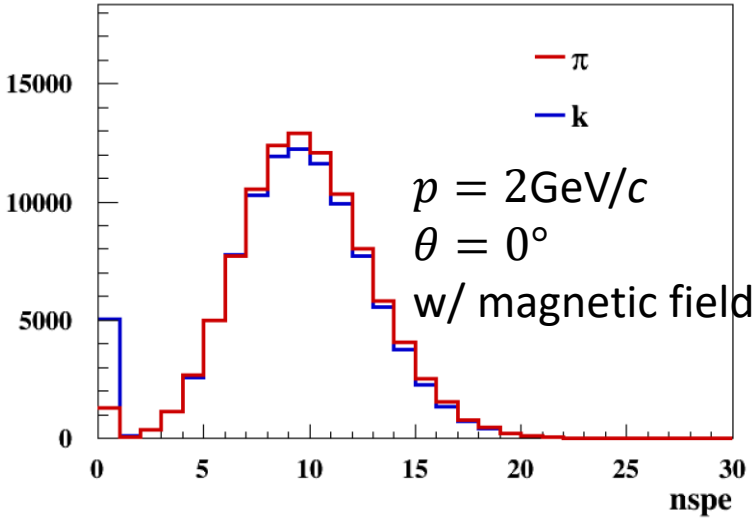
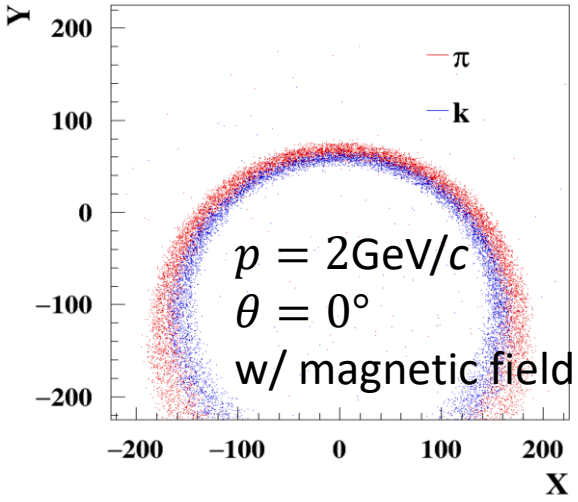
Performance of RICH

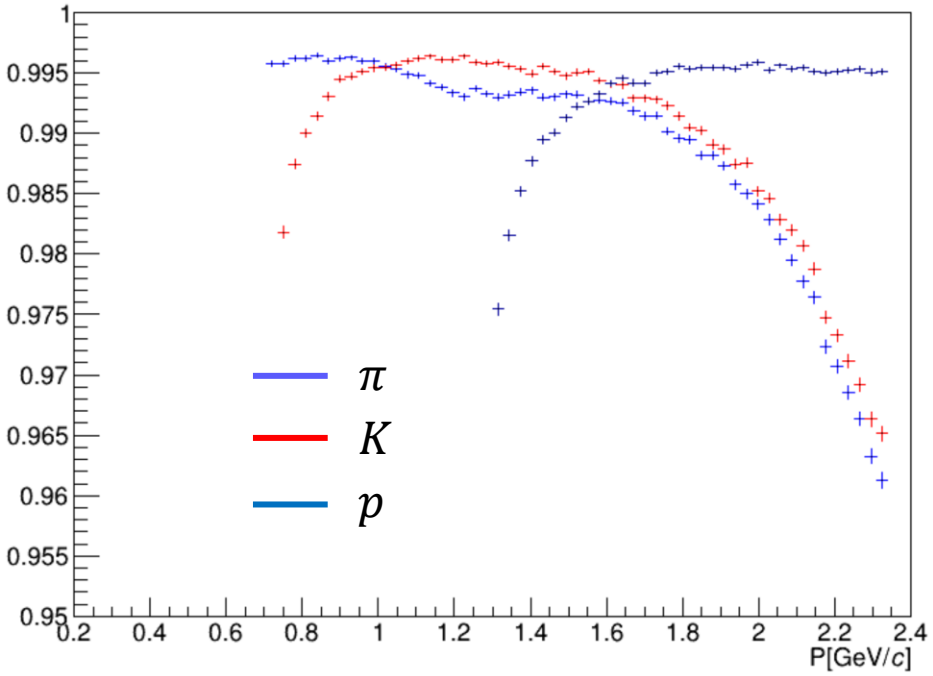








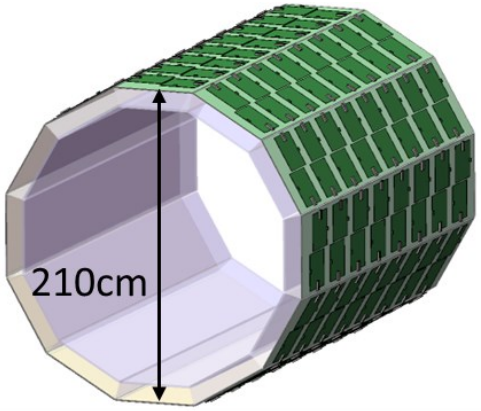
RICH performance in simulation



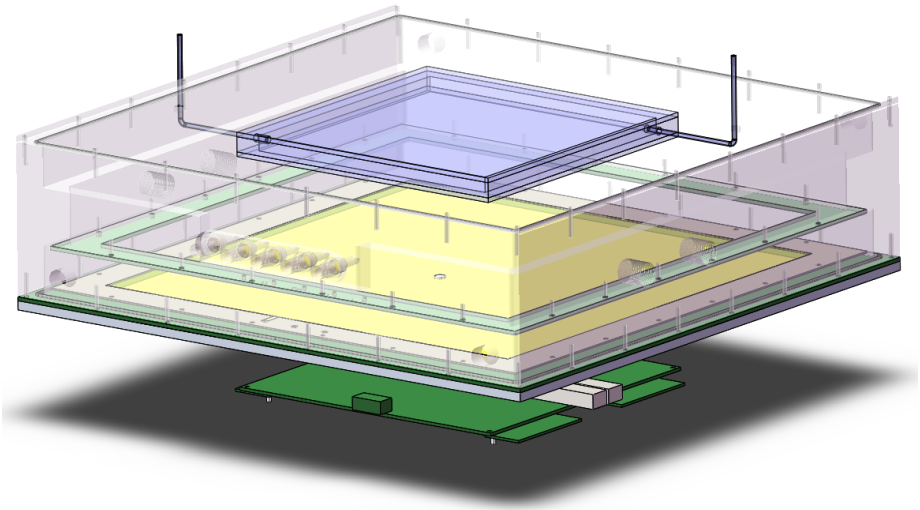
- Background level:
  10^{-3} hit / (pixel × time window)
- PID ratio for π, K, p > 98% in momentum ∈ [0.7, 2.0] GeV/c
- More detail in RICH software report

- Will validate parameters used in simulation & validate the PID performance in prototype beam test

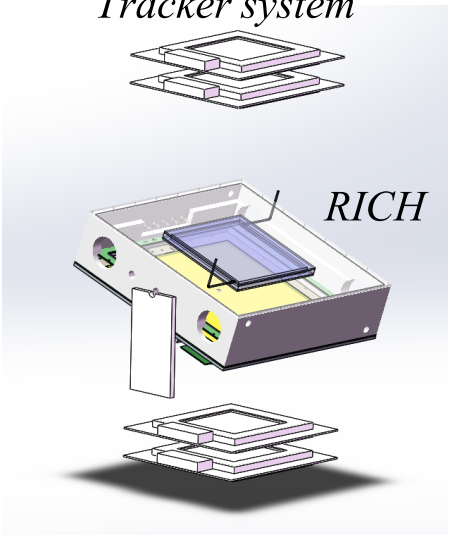
Structure of RICH Detector

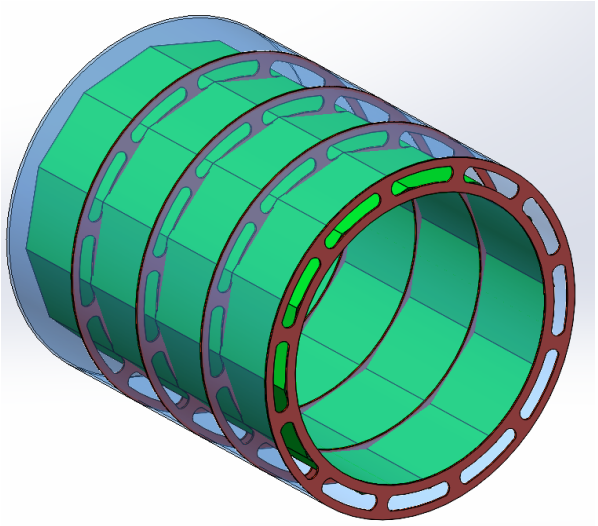


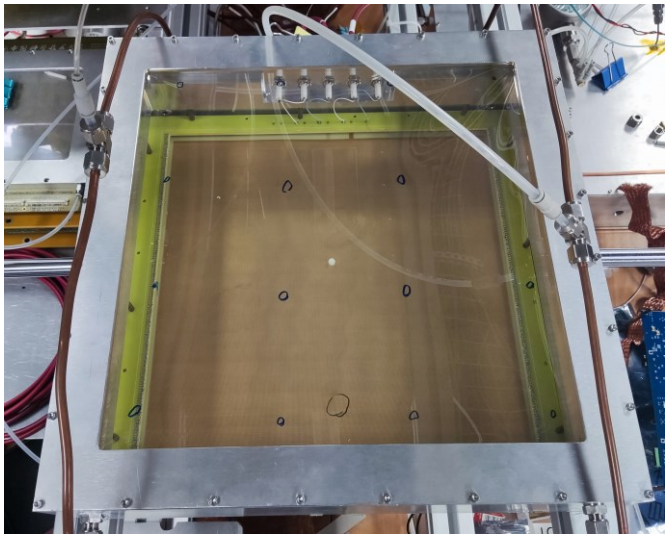
RICH: 12 modules

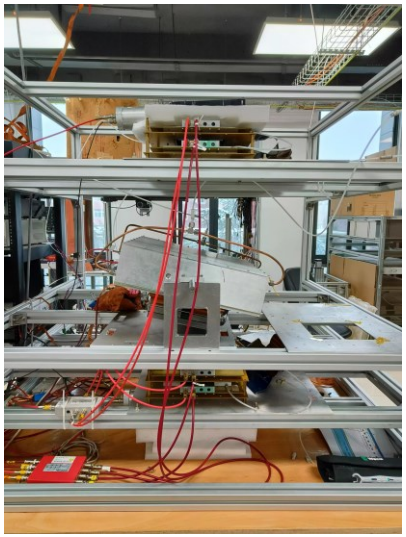


Engineering prototype







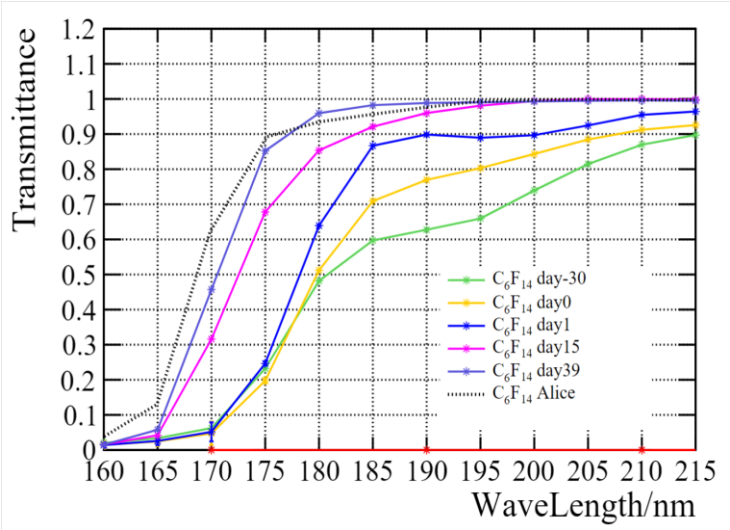


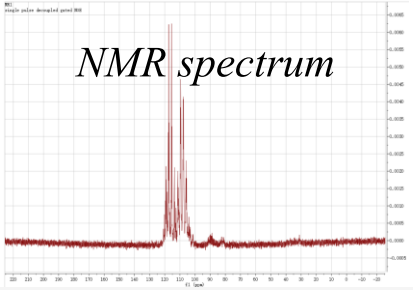
Build the Prototype

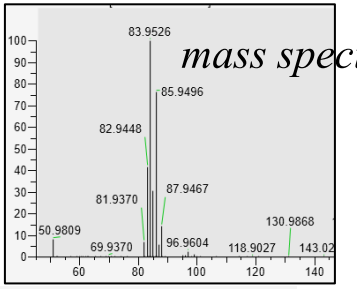
- Radiator purification
- Coating CsI photocathode on THGEM on large area, QE test
- THGEM-MicroMegas: gain and uniformity
- AGET-based readout electronics
- Custom ASIC-based readout electronics
- On going: Test of encoding anode
- On going: Cosmic ray test system
- Preparing the beam test

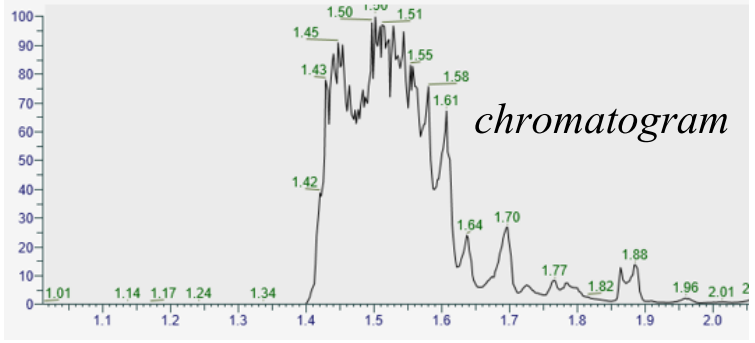
Radiator Purification

- Remove water and oxygen
  - The C_6F_{14} is absorbent to water and oxygen ← less transparent to VUV
  - Developed using metal catalyst purification, faster and smaller loss
- Hunting for C_6F_{14} with stable quality
  - Tried various samples from various suppliers, optical properties not stable
  - Multiple chemical analyses conducted. Cooperating with suppliers to figure out the relations between optical properties and chemical properties.
  - SiO_2 used as radiator prototype now



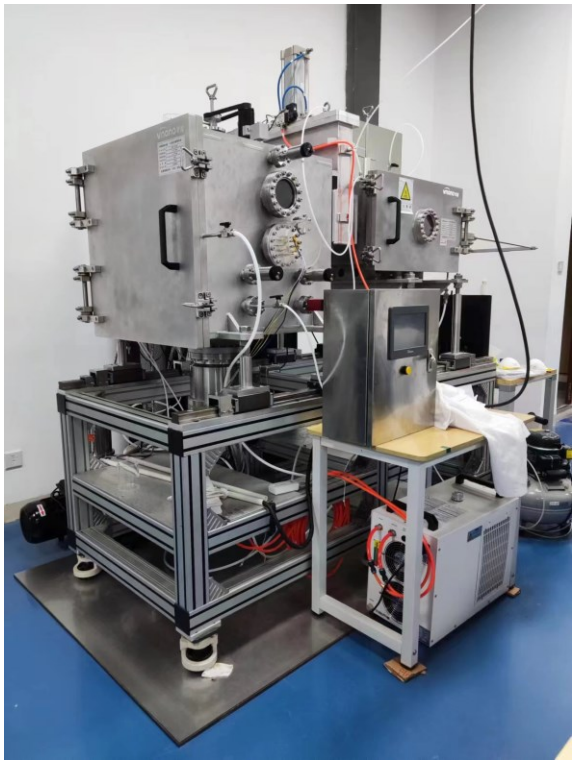


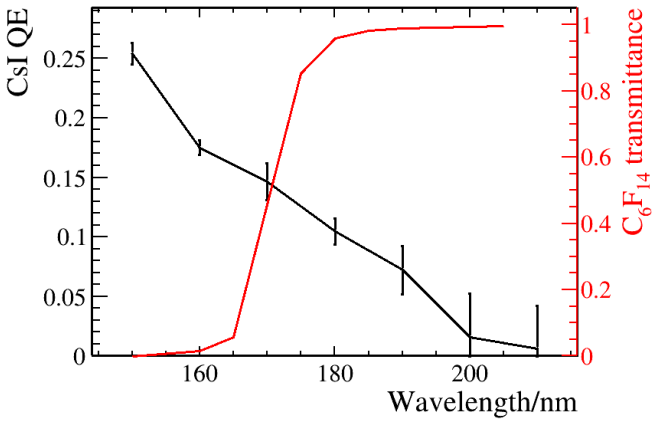


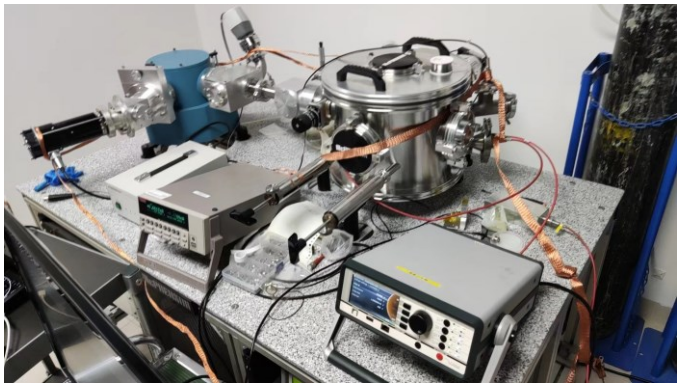


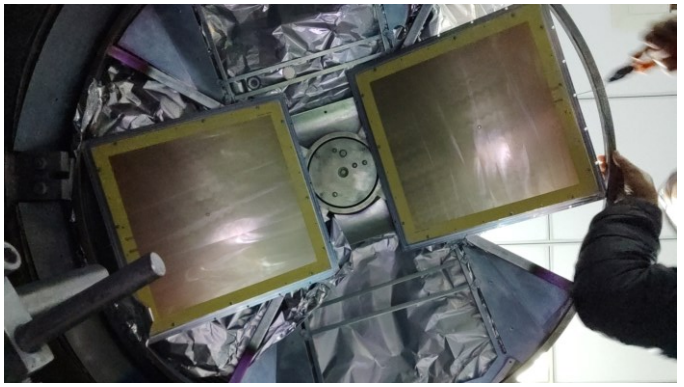
Coating CsI Photocathode on THGEM

- Build the large area coating system & cooperate with Anhui Institute of Optics and Fine Mechanics, Chinese Academy of Sciences.
- Build the QE & radiator transmittance measurement system.



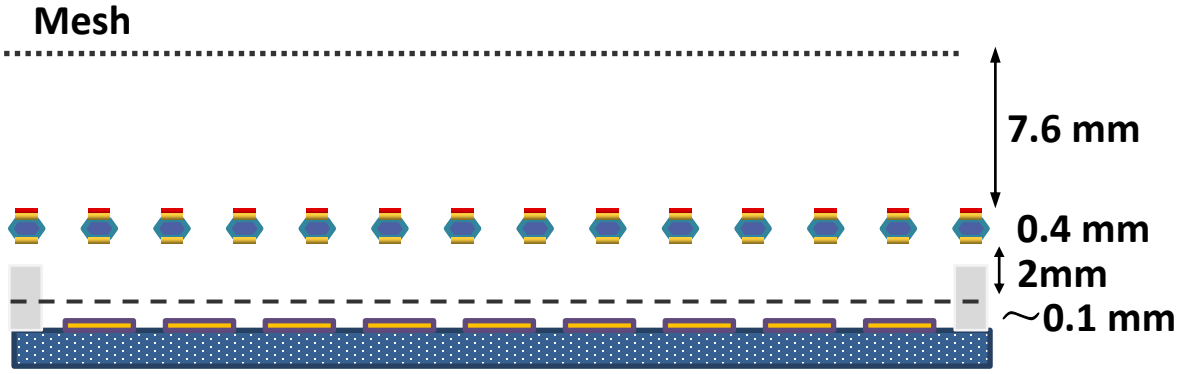




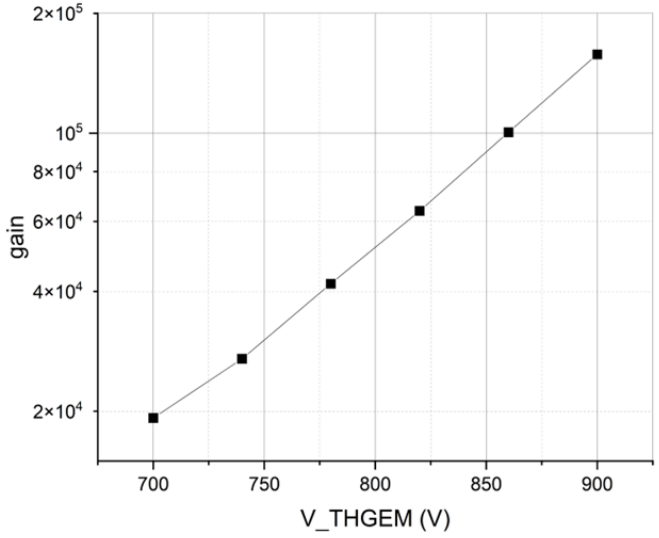


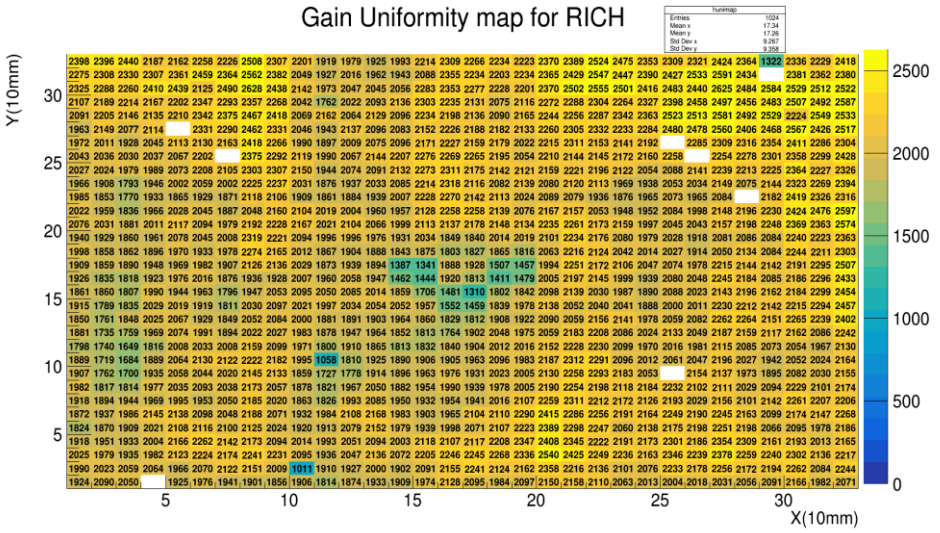
Gain & Uniformity

- Test with THGEM-MicroMegas and AGET-based readout electronics.



Gain

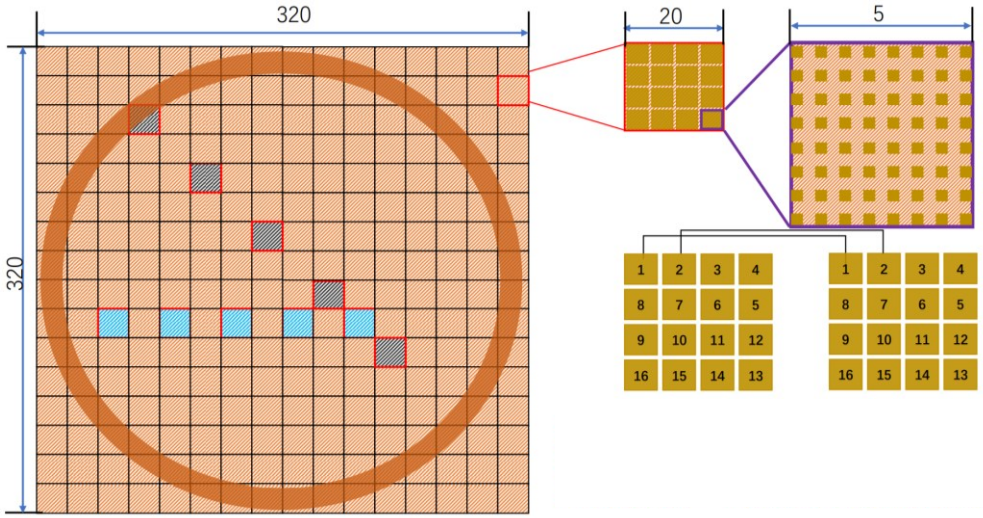


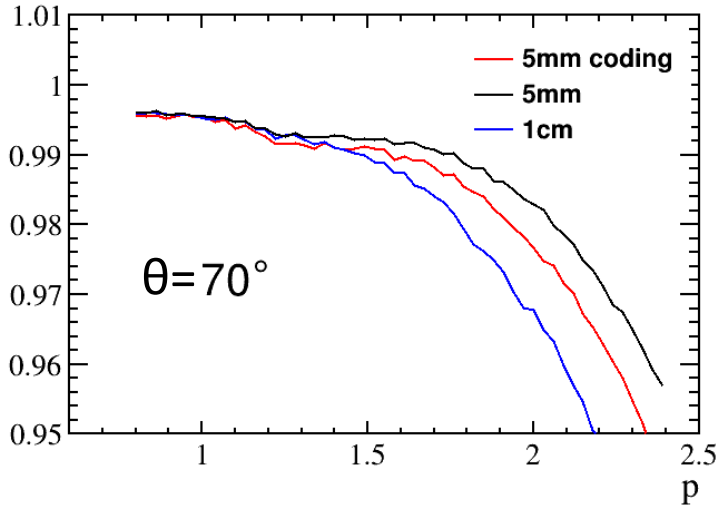


Uniformity 8% @ gain~1.6×10^4

Encoding anode

- The encoding anode method is proposed to reduce the number of readout channels to 1/5.
- Connect and read out the anode by a special geometric rule (encoding) and determine the hit position by the firing mode (decoding).
- Dual-layer readout for the resistive anode, with a large top pixel corresponding to 16 small bottom pixels (5 mm × 5 mm), and the small pixels are encoded.





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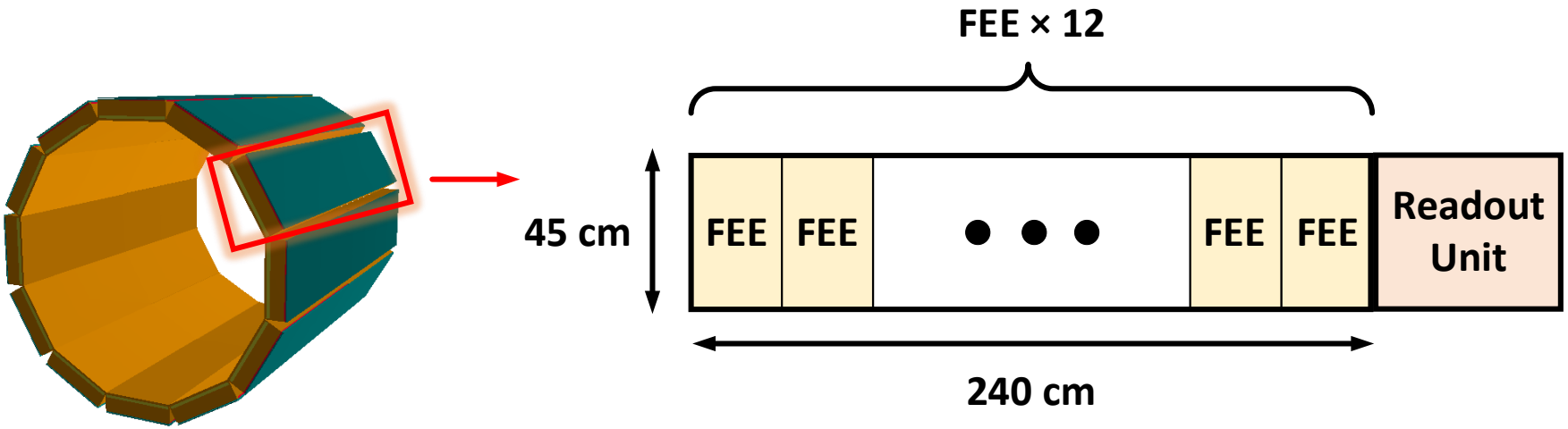
PIDB Readout Electronics

- The RICH PIDB detector consists of 12 identical block modules, each with 43,200 readout channels when using the 5 × 5 mm^2 readout pads.
- The readout electronics are located directly behind the detector to avoid a large number of long readout cables.
- Each block module is divided into 12 FEEs along the beam direction, each with 3600 channels of integration.



Conceptual design of the RICH PIDB readout electronics

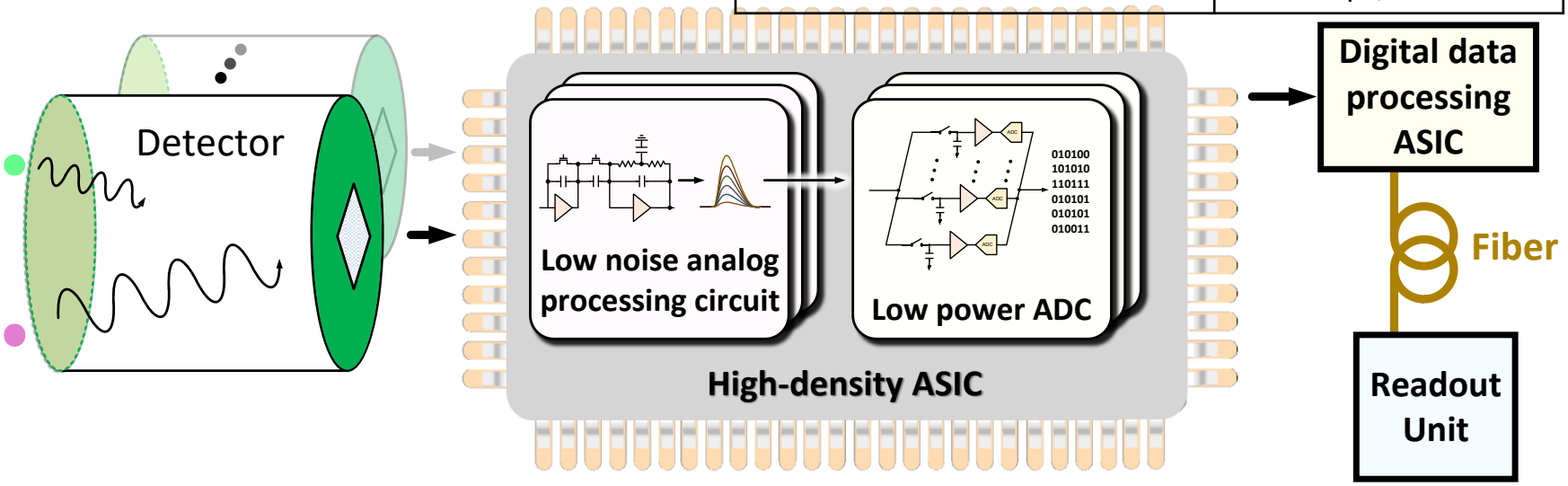
PIDB Readout Electronics

Challenges posed to readout electronics:

- High density
- Large number of channels
- High resolution
- Short dead time

Requirements for the readout electronics

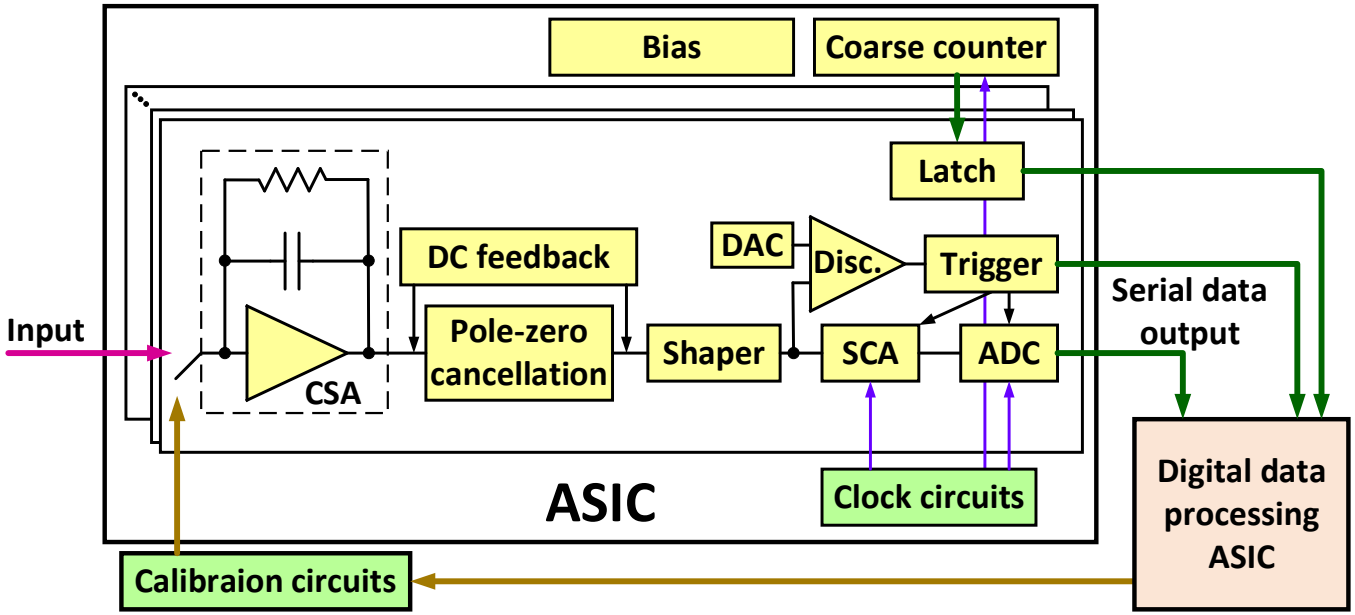
	Requirement
Charge measurement range	48 fC
Equivalent noise charge (ENC)	0.5 fC @ 20 pF C_{in}
Time resolution	≤ 1 ns @ 16 fC @ 20 pF C_{in}
Total redout channels	~ 518,400 (can be reduced with encoding anode)
Dead time	< 66 μs/channel



Signal processing chain of the readout electronics

PIDB Front-end ASIC Prototype

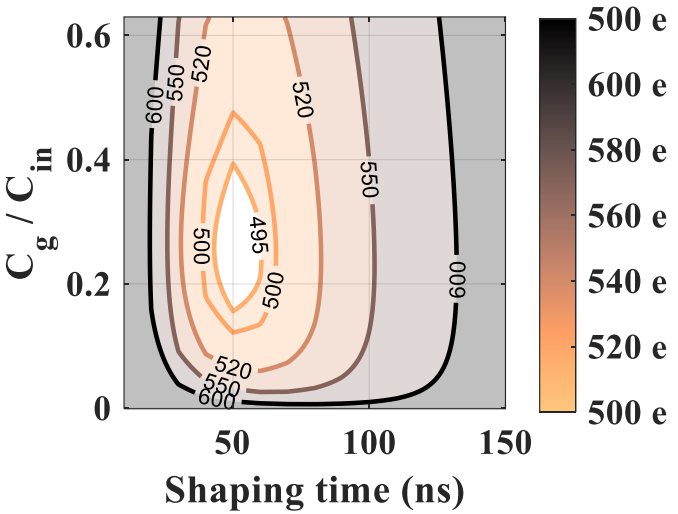
- The prototype ASIC integrates 32 channels, including analog processing circuits and analog-to-digital conversion (ADC) circuits.
- Compatible with both external trigger mode and triggerless mode.
- All outputs are digital, can be directly connected to the digital data processing ASIC.



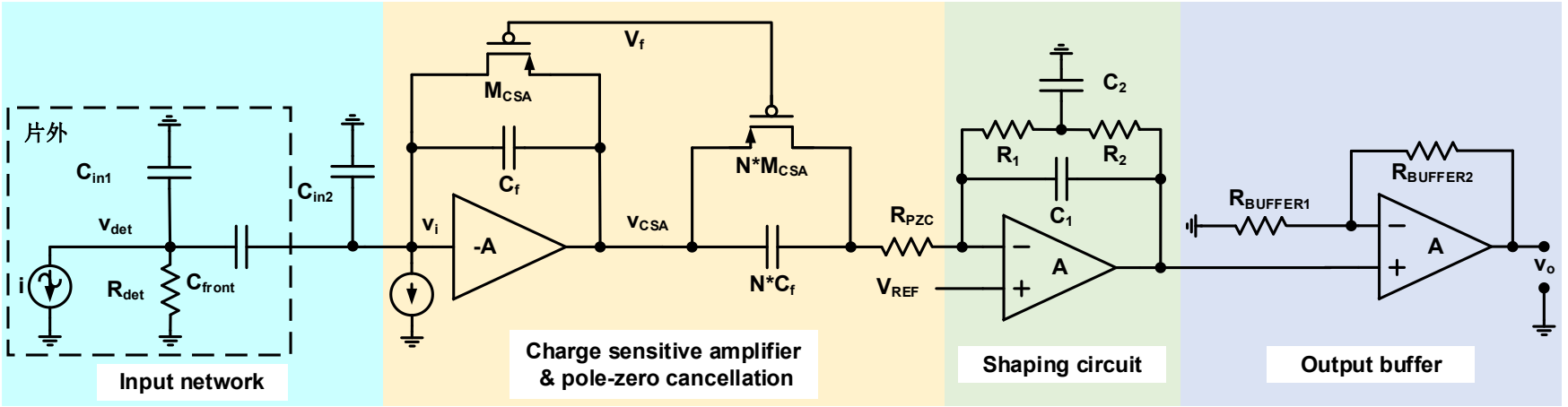
Block diagram of the prototype ASIC

PIDB Front-end ASIC Prototype

- Since the digital waveform data can be further processed by digital filters, a CR-$(RC)^2$ semi-Gaussian shaper is selected.
- A characteristics table based on the BSIM3v3 model is created to optimize the transfer function and ENC better.



ENC optimization



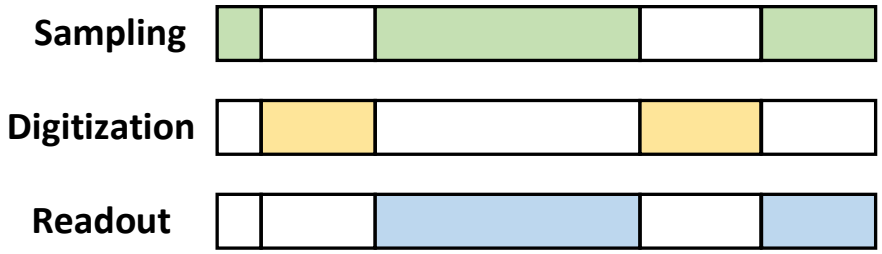
Schematic of the analog processing circuit

PIDB Front-end ASIC Prototype

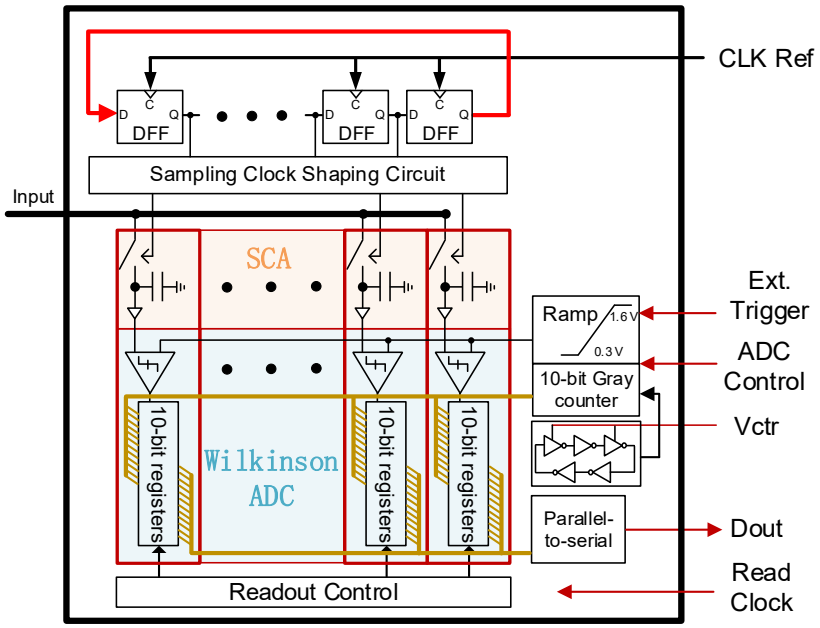
- Higher sampling rate to extract more information from the waveform.
- Lower power consumption for high density and low cooling requirements.
- Effective signal duration only accounts for about 1% of the total time.

Switched Capacitor Array (SCA) + ADC

(ADC in suspend mode without valid signal)



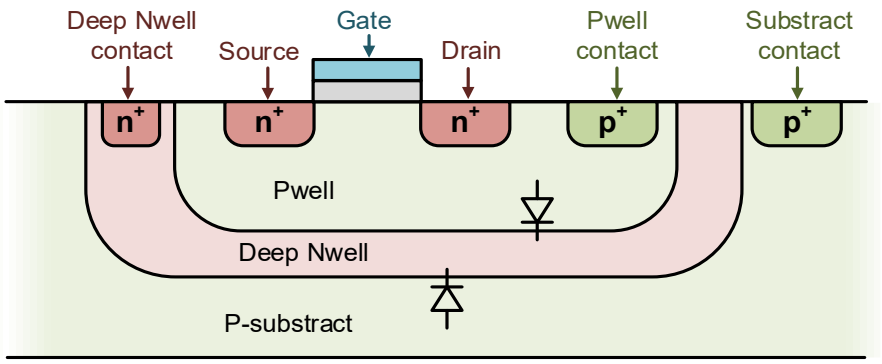
Working sequence of the digitization circuit



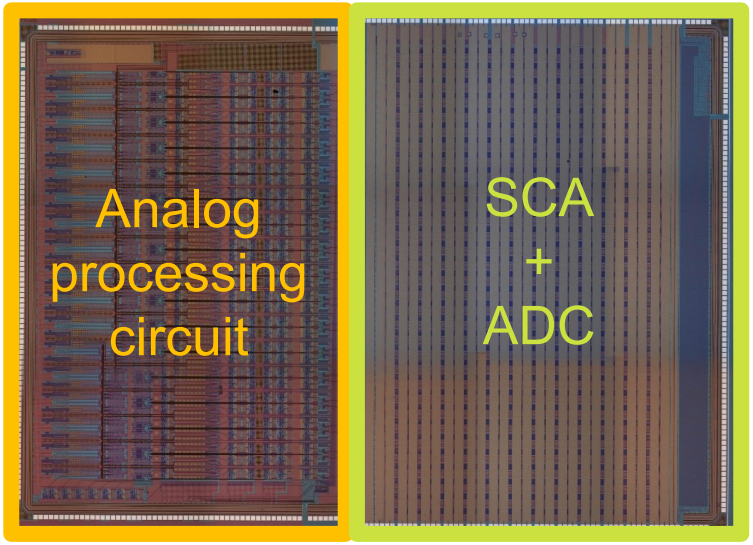
Block diagram of the digitizing circuit

PIDB Front-end ASIC Prototype

- This 32-channel mixed-signal ASIC is fabricated in the 180 nm CMOS process with a die size of 10,005 μm × 6,168 μm.
- Approaches to reducing crosstalk between sensitive front-end and digital circuits:
  - Place the noisy digital circuits in the deep Nwell.
  - Use Dcap cell as filler during digital implementation to reduce the power ripple.
  - Isolate the ESD loop between digital IO and analog IO.



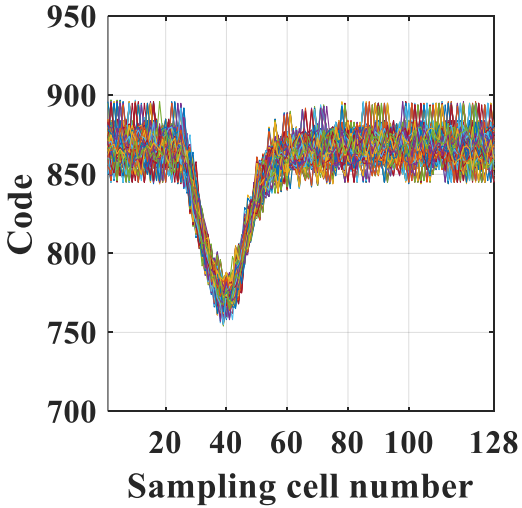
Cross-sectional view of the deep Nwell



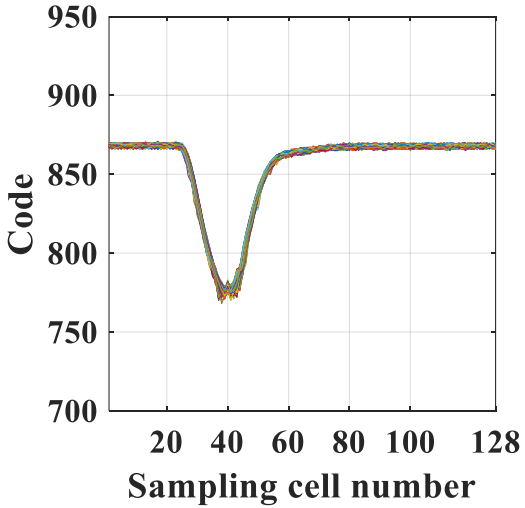
Photograph of the fabricated chip

PIDB Front-end ASIC Prototype

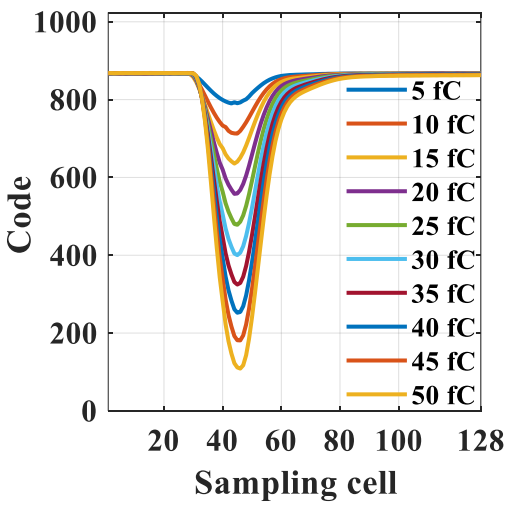
- Output waveforms are sampled and digitized by 128 independent cells, the mismatch between cells results in different codes for the same input.
- This mismatch is a form of fixed pattern noise that can be corrected by sampling the baseline waveforms and generating the DC correction data.
- Output waveform is similar under different input charges, with a gain of 15.2 code/fC and an INL of 0.92%.



Pre DC calibration waveforms of 6 fC charge signals



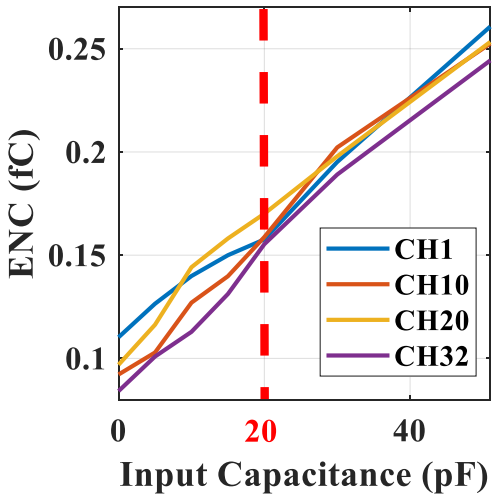
Post DC calibration waveforms of 6 fC charge signals



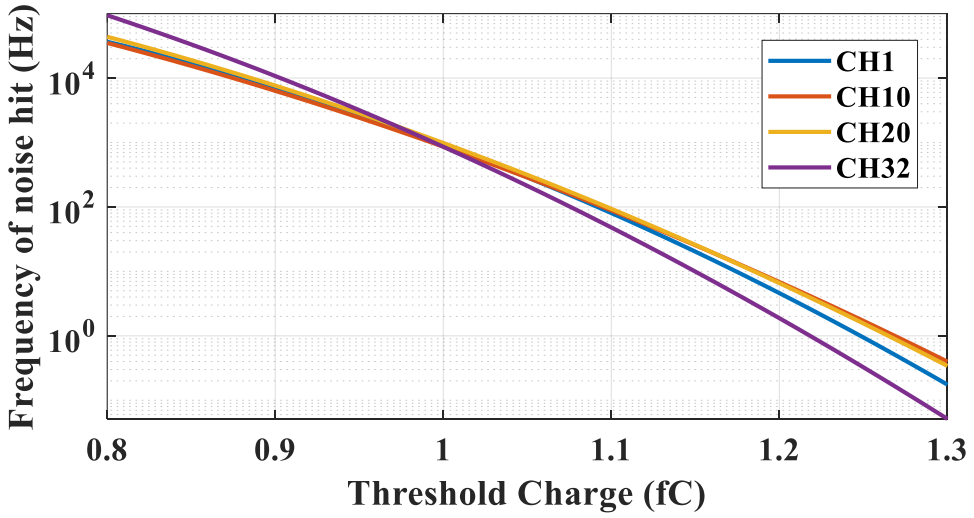
Output waveforms versus input charge

PIDB Front-end ASIC Prototype

- ENC at the discriminator input affects the lower limit of the threshold setting and then the detection efficiency in triggerless mode.
- Measured ENC ≈ 627 e + 18.8 e/pF
- With a threshold greater than 1.2 fC, the noise hit frequency for a single channel is a few Hz.



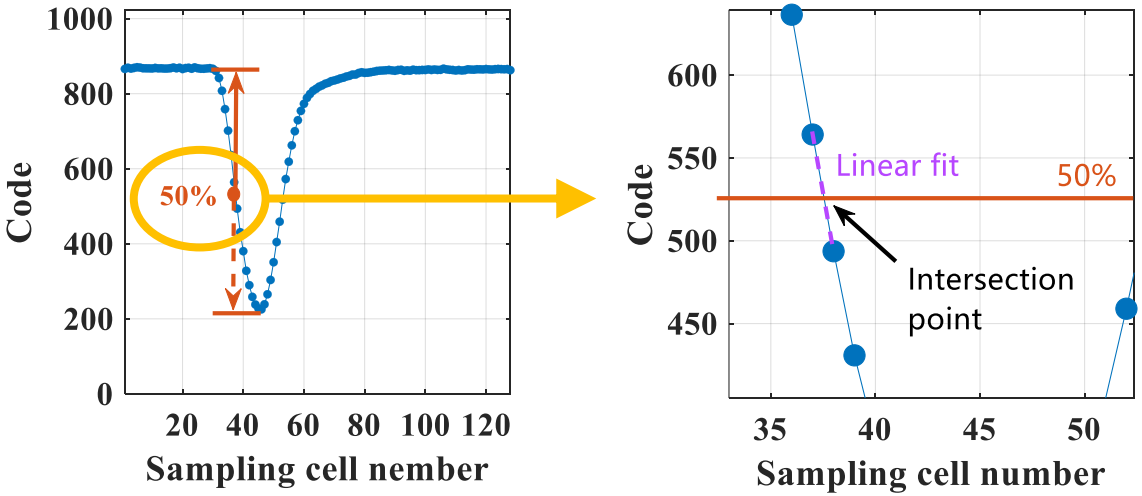
ENC at discriminator input versus input capacitance



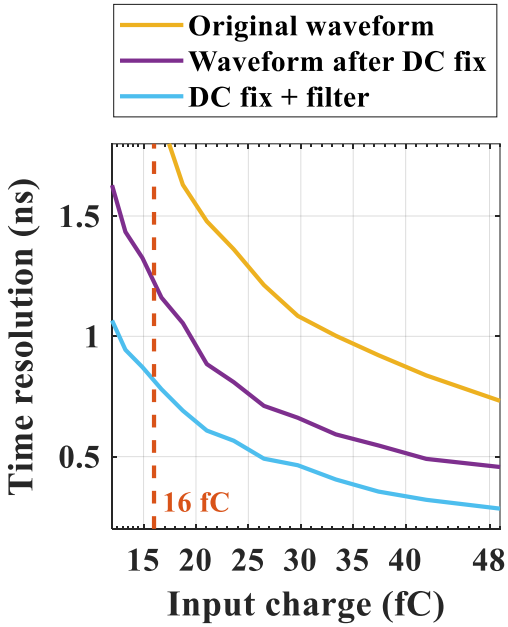
Frequency of noise hit versus threshold

PIDB Front-end ASIC Prototype

- Time resolution is tested for various input charges at 20-pF input capacitance.
- Constant Fraction Discriminators (CFD) and 2-point linear fit are used for time calculation.
- Digital filter and waveform fitting methods will be further investigated to improve the time resolution.



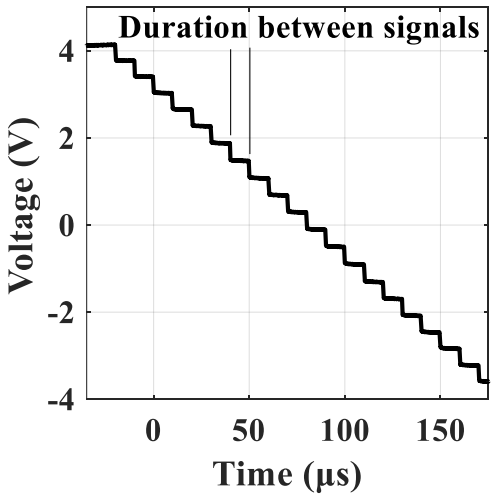
Timing extraction algorithm used for the digital waveform



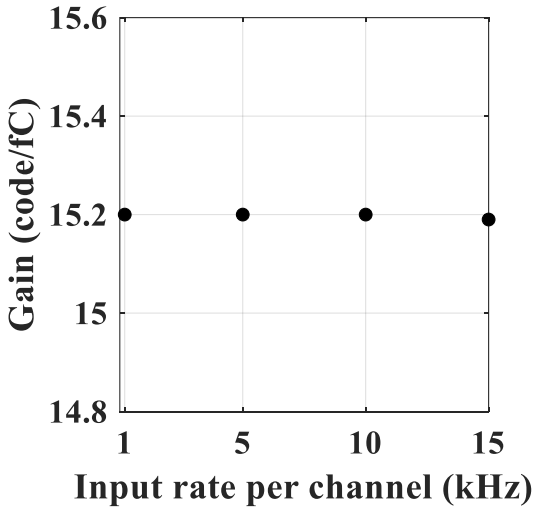
Time resolution versus input charge

PIDB Front-end ASIC Prototype

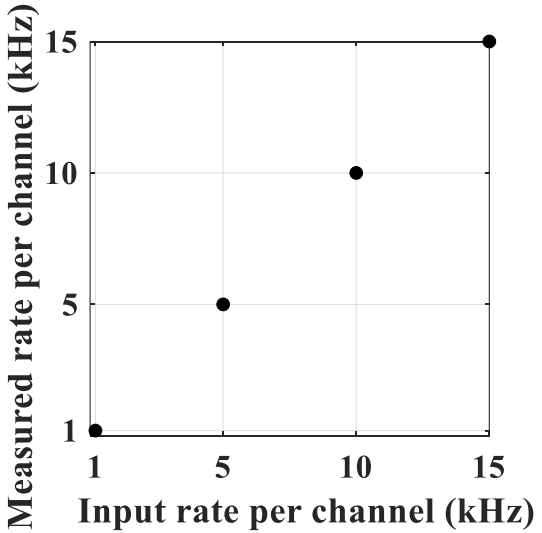
- The step voltage waveform is used as the input signal to test the counting rate capability.
- The gain remains almost the same and the readout efficiency maintains 100% up to 15 kHz repetition rate for a single channel, meeting the requirement.



Step voltage waveform used for the dead time test



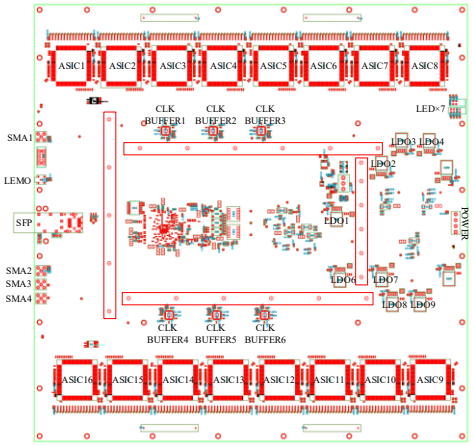
Gain variation with input rate

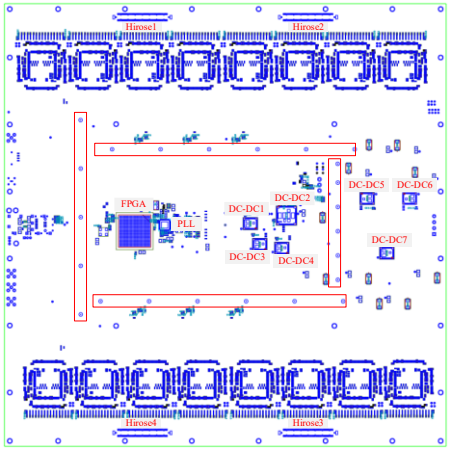


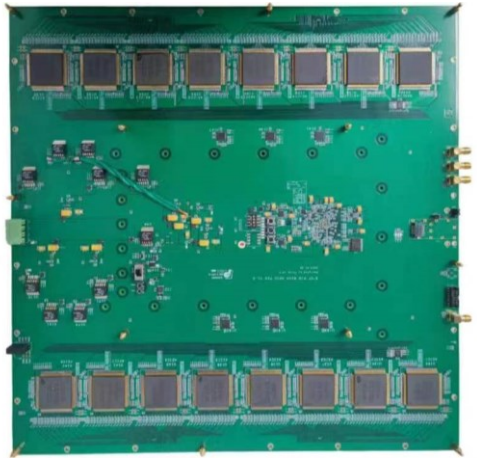
Measured output rate versus input rate for a single channel

PIDB FEE Functional Verification

- Based on the 32-channel prototype ASIC, a 512-channel FEE prototype was designed.



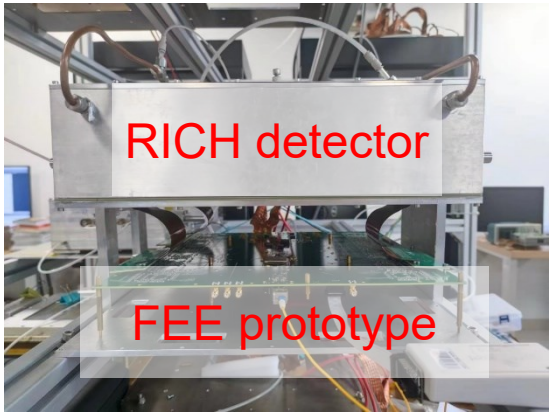


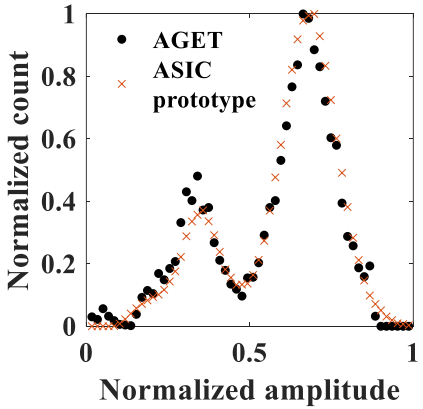


Layout of the 512-channel FEE prototype

Photograph of the FEE prototype

- Functional verification and energy spectrum test with ^{55}Fe are completed.





Experimental setup for energy spectrum testing

^{55}Fe spectrum

Outline

1、Physical requirements for STCF PIDB

2、RICH PIDB detector design

3、RICH PIDB readout electronics design

4、Conclusion

Conclusion

- Use THGEM-MicroMegas based RICH as barrel PID detector.
- Estimated PID ratio for π, K, p > 98% in momentum $\in$ [0.7, 2.0] GeV/c.
- Developed the AGET-based readout electronics and custom ASIC-based prototype readout electronics.
- Engineering prototype setup, running the cosmic ray test.

Ongoing:

- Hunting for C_6F_{14} with stable quality.
- Optimize the process to improve the QE of CsI.
- Preparing for the beam test.
- Develop the 64-channel custom ASIC.

Thanks!