R&D of a MAPS based Inner Tracker for the STCF

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USTC

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Detector considerations

- Physics requirements

Required tracking performance for the STCF

Process	Physics Interest	Optimized Sub-detector	Requirements
$\tau \to K_s \pi \nu_\tau$,	CPV in τ sector,		acceptance: 93% of 4π; trk. effi.:
$J/\psi \to \Lambda\bar{\Lambda}$,	CPV in hyperon sector,	Tracker	$> 99\%$ at $p_T > 0.3$ GeV/c; $> 90\%$ at $p_T = 0.1$ GeV/c
$D_{(s)}$ tag	Charm physics		$\sigma_p/p = 0.5\%$, $\sigma_{\gamma\phi} = 130\,\mu$m at 1 GeV/c

BESIII tracking performance

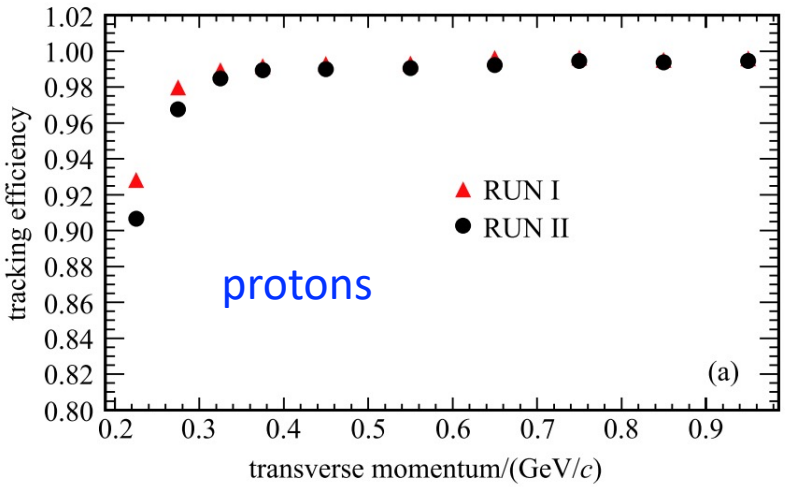
	Sub-system	BESIII
MDC	Single wire $\sigma_{r\phi}$ (μm)	130
	σ_p/p (1 GeV/c)	0.5%
	σ (dE/dx)	6 %

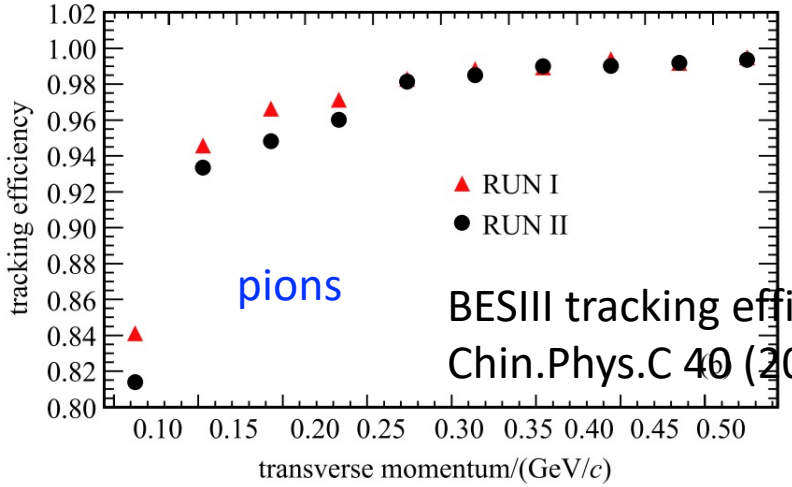
Vertex resolution: σ_{d0} ~0.2 mm; σ_{z0} ~ 1.mm

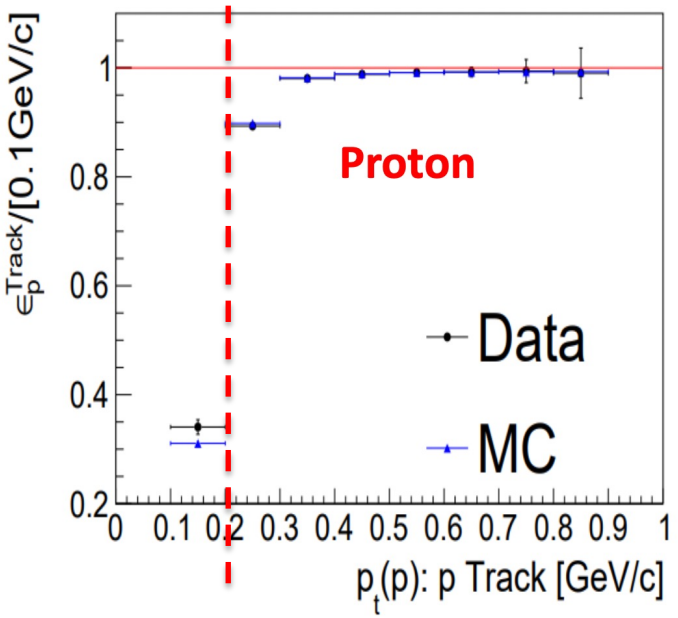
- ❖ No stringent requirements on vertexing
- ❖ The main challenge is the tracking at the low momentum region (p_T < 100 MeV)

Detector considerations

- The challenge at the low p_T region
  - For BESIII, the tracking efficiency drops sharply below 100MeV
- There is strong physics motivation to go to low p_T region

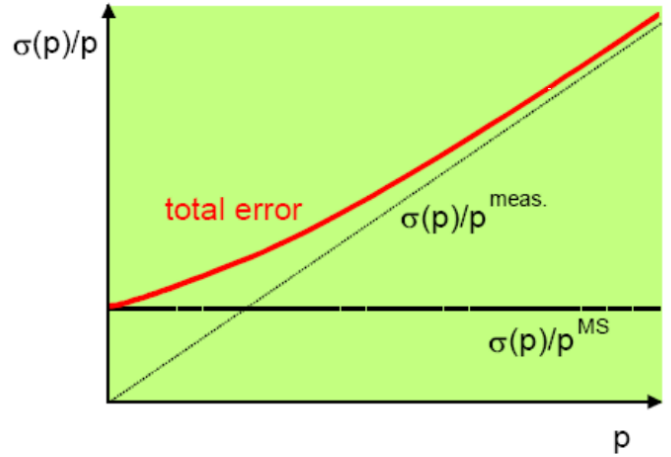






BESIII tracking efficiency,
Chin.Phys.C 40 (2016) 2, 026201

- Tracking challenges at low p_T
  - Momentum resolution: Multiple Coulomb scattering
  - Track reconstruction efficiency

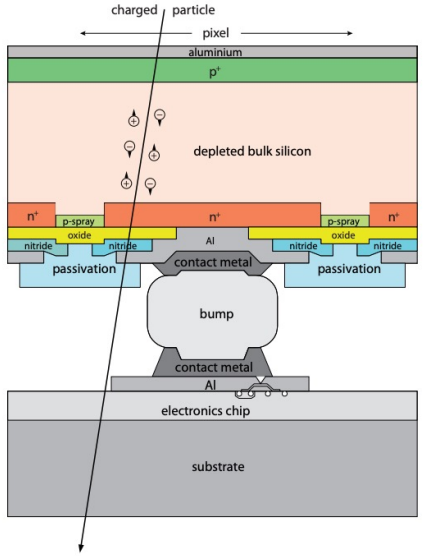


- Low material budget is essential to satisfy the physics requirements

CMOS pixel sensors

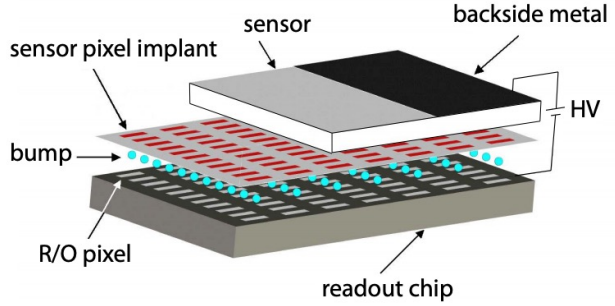
- Hybrid pixels:
  - Large area, radiation hard
  - Widely used in ATLAS/CMS
  - Disadvantages：
    - relatively large material budget
    - Hybridization: complex, expensive

- CMOS active sensors
  - Traditional MAPS：diffusion, slow
    - Low rate, low radiation
  - Fully depleted CMOS: DMAPS
    - Drift
    - HR/HV-CMOS

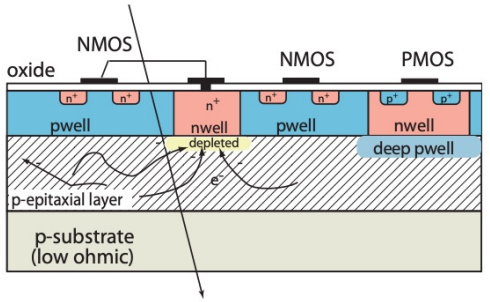


(a) Hybrid pixel

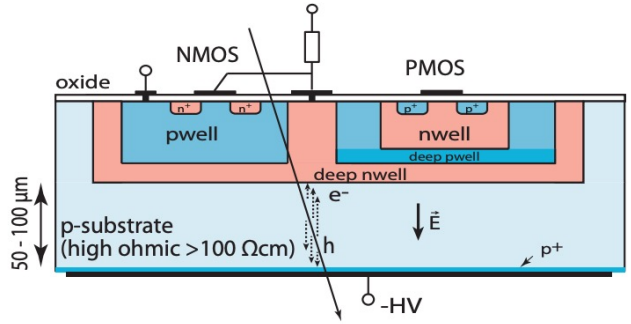
arXiv:1705.10150v3



(b) Pixel matrix



(a) MAPS

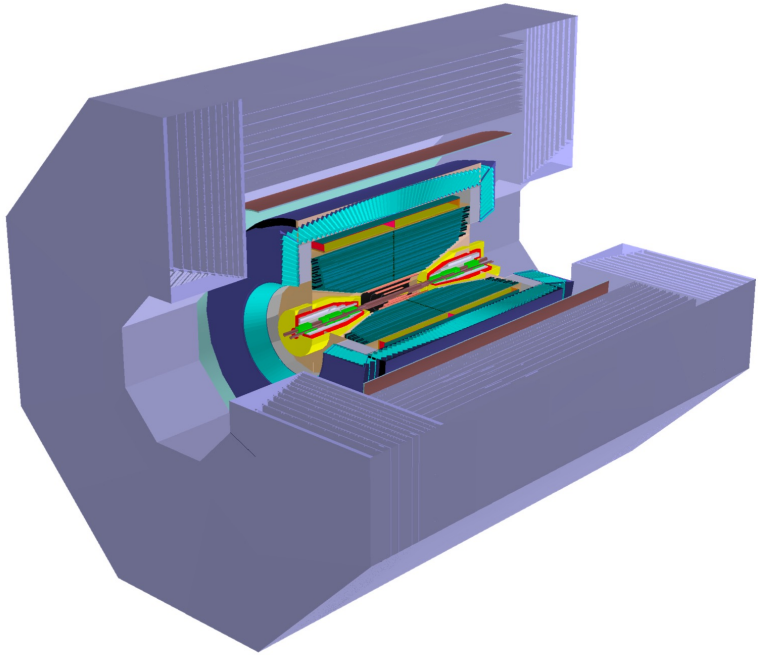


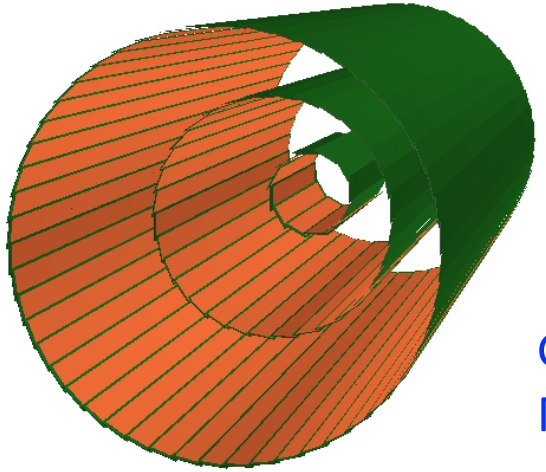
(b) DMAPS

$$d \sim \sqrt{\rho V}$$

Conceptual design

- A preliminary design of the MAPS based Inner Tracker (ITKM)
  - An alternative option to the MPGD based Inner Tracker (ITKW)
- Three layers of silicon pixel detectors, with radii of 36mm,98mm,160mm
  - Beam pipe radium: 30mm
- Acceptance: polar angle of 20°~160°
- Total area: 1.3m^2





Layer	Radius (mm)	Length (cm)	Area (cm^2)
1	36	19.78	447.46
2	98	53.85	3315.87
3	160	87.92	8838.63

Geometry/layout still being optimized
Might extend to 4 or more layers

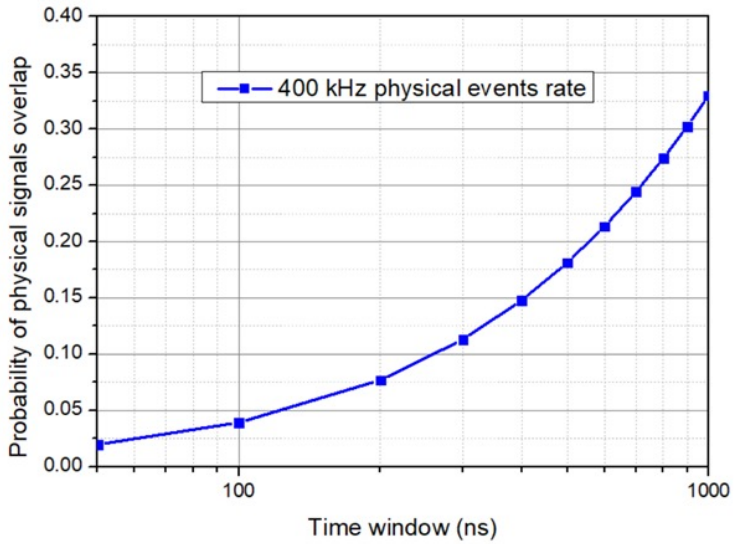
Design targets

- Requirements on the MAPS based Inner Tracker
  - Spatial resolution： $\leq 100\mu m$
  - Power consumption： $\leq 100mW/cm^2$
  - Material budget per layer： $\leq 0.35\%\ X_0$
  - Time resolution： $\leq 50\text{ns}$ (to deal with the pileup issue at high luminosity)
  - Time-over-threshold (TOT) measurement:
    - Time-walk correction
    - Correction of multi-coulomb scattering in track finding

High event rate at STCF

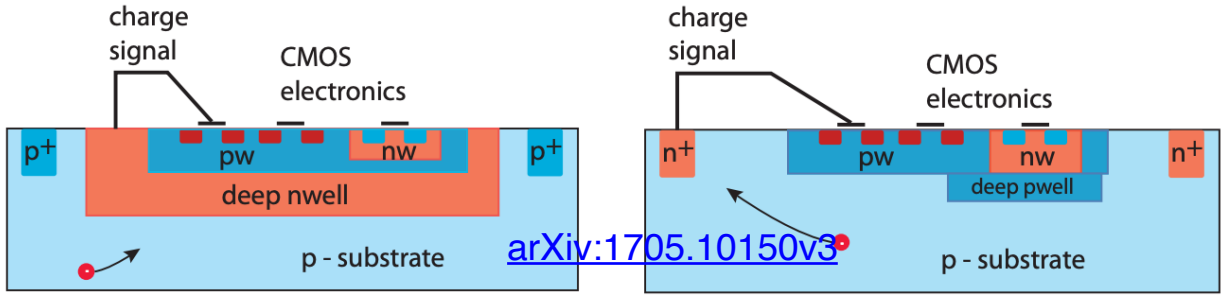
Physics Process	Cross-section (nb)	Rate (Hz)
$\sqrt{s} = 3.097$ GeV, $\mathcal{L} = 0.75 \times 10^{35}$ cm^{-2}s^{-1}, $\Delta E = 0.848$ MeV		
J/ψ	4500	337500
$\rightarrow e^+e^-$	270	20000
$\rightarrow \mu^+\mu^-$	270	20000
Bhabha ($\theta \in (20°, 160°)$)	734	55000
$\gamma\gamma$ ($\theta \in (20°, 160°)$)	36	2700
$\mu^+\mu^-$	11.4	900
Hadronic from continuum	25.6	2000
2γ process ($\theta \in (20°, 160°)$, $E > 0.1$ GeV	~23.3	1740
Total	~5300	~400000

Pileup probability



Small fill-factor

- To reduce the power consumption, a small fill-factor design is preferred



(a) Large fill-factor (b) Small fill-factor

arXiv:1705.10150v3

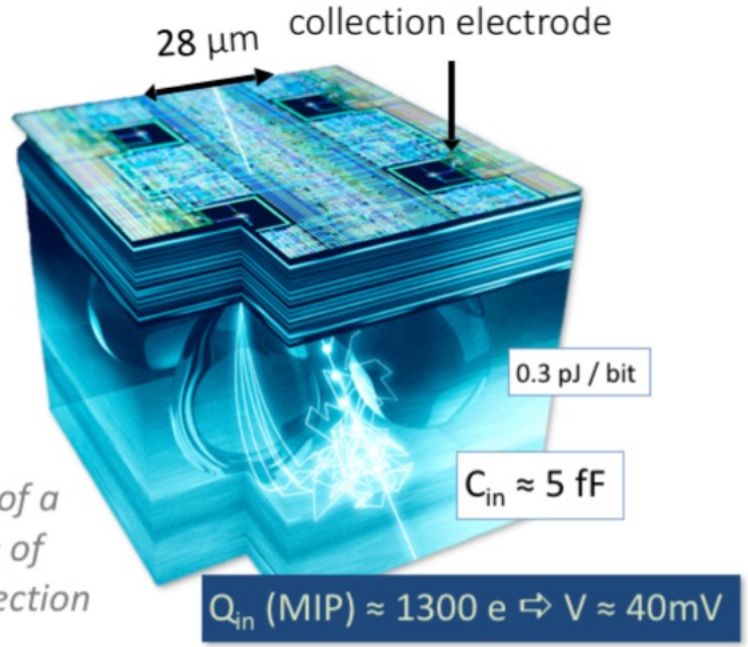
Large fill-factor: HV-CMOS

- Pros: timing, radiation hardness
- Cons: capacitance, power consumption

Small fill-factor: HR-CMOS

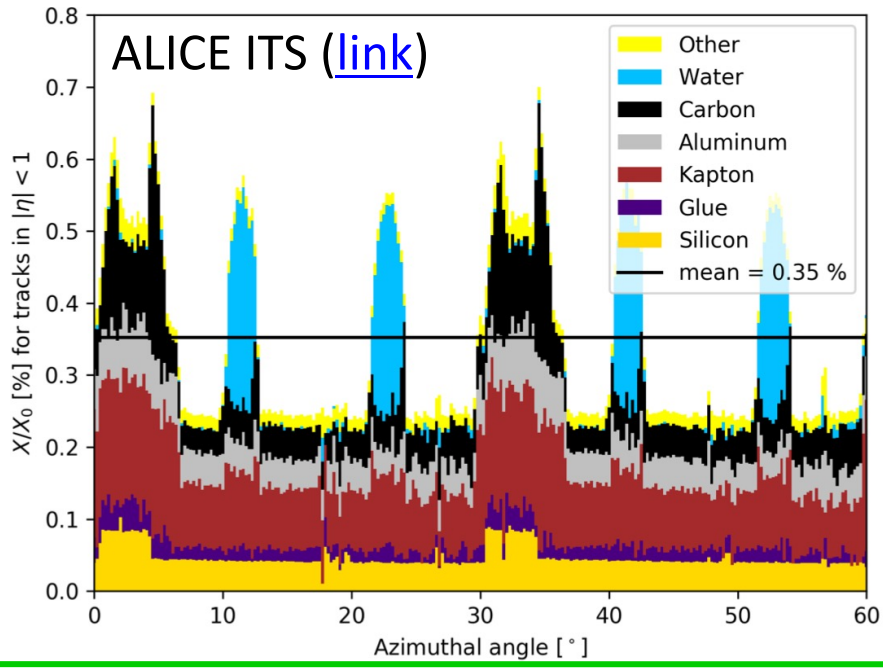
- Pros: spatial resolution, capacitance, power consumption
- Cons: timing, radiation hardness

ALPIDE(link)



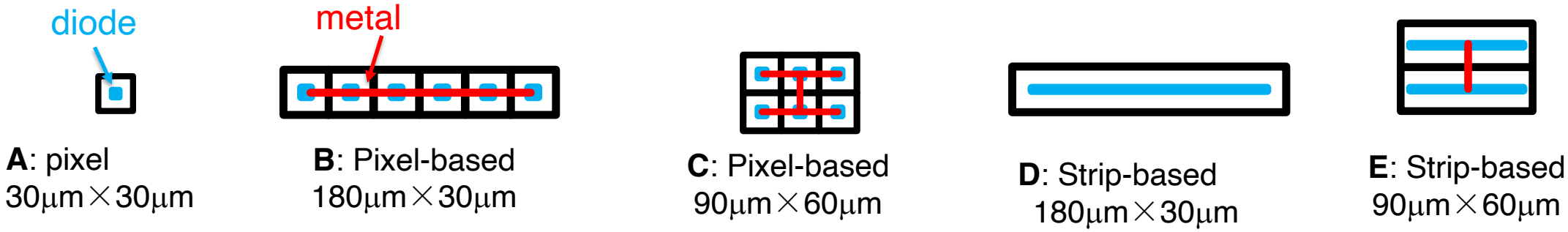
Artistic view of a SEM picture of ALPIDE cross section

Not to scale



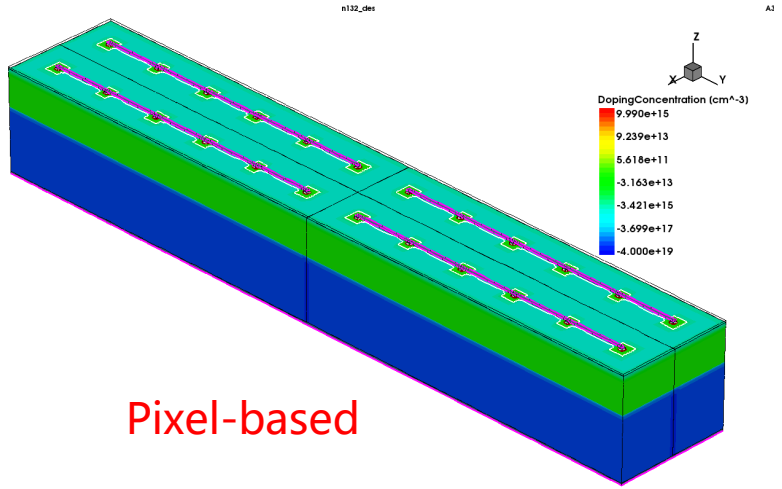
Sensor design

- Pixel size considerations
  - Higher priority on the power consumption than the spatial resolution → larger pixel size to reduce the power consumption density
  - The ALPIDE sensor is already optimized and proven experimentally → keep the sensor geometry as close to ALPIDE as possible
    - Pixel-based: analog connected small pixels ($1\times6 \rightarrow 1, 2\times3 \rightarrow 1$) using metal lines
    - Strip-based: extended diode size in one direction
    - A 3rd option also under design: digital connected small pixels

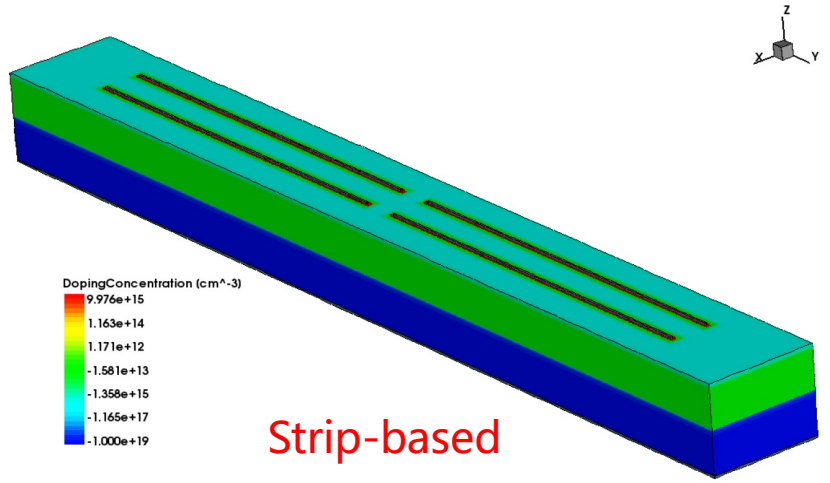


TCAD simulation

- Strip Sensor
  - Rectangular: 30μm×180μm
  - Diode : 2μm×150μm
  - Spacing: 2μm
  - -6V bias
  - Depletion depth: 12μm
- Sensor capacitance
  - Single pixel: 2 fF
  - Pixel-based pixel: 12 fF
  - Strip-based pixel: 30 fF

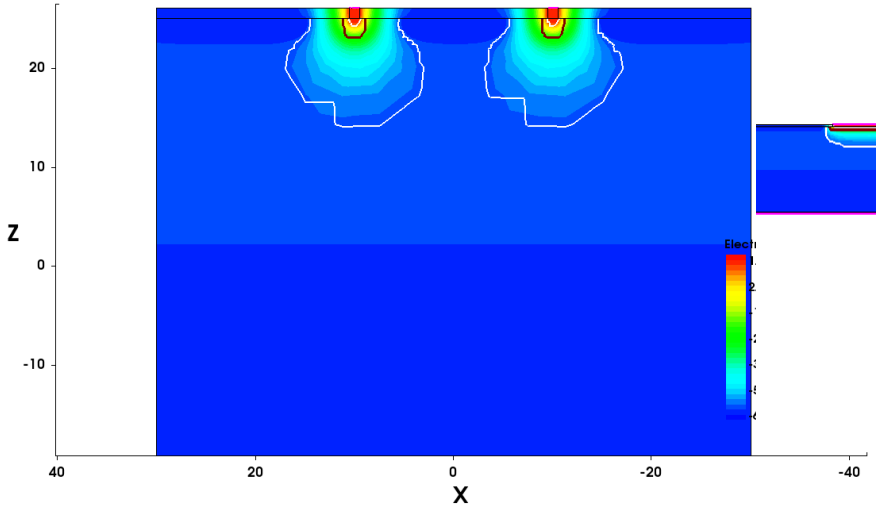


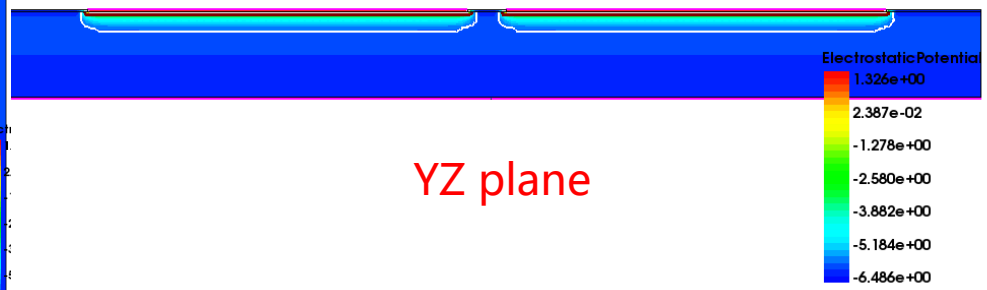
Pixel-based



Strip-based

XZ plane





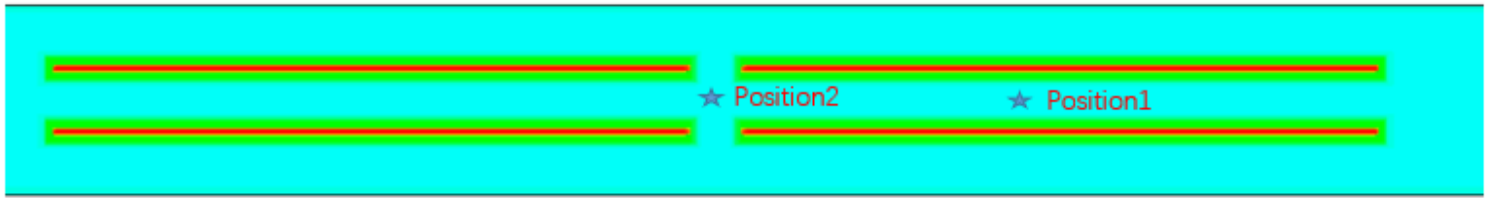
YZ plane

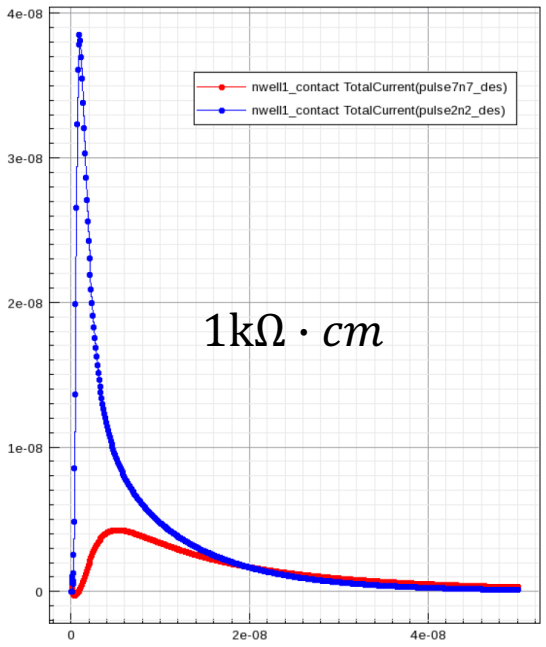
Alternative CMOS technologies

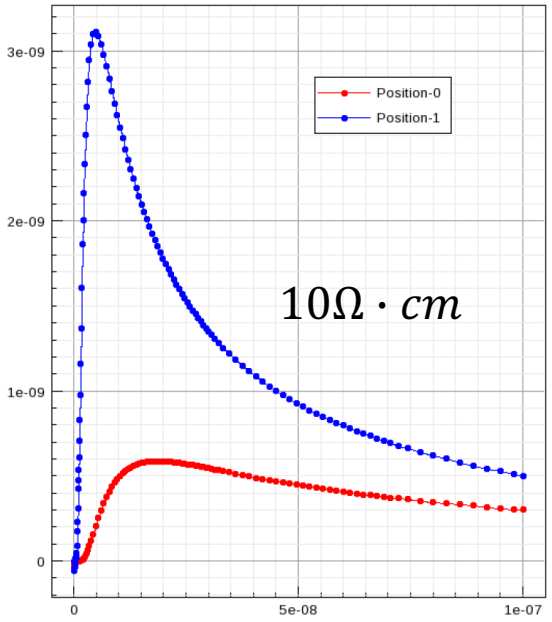
- Usually MAPS is based on high-resistivity epitaxial wafers
  - Resistivity: $\gtrsim 1\mathrm{k}\Omega \cdot cm$; epi thickness: ~20 μm
- Other options are also being considered, based on available technologies in domestic foundries
  - Low resistivity epi wafers:
    - Resistivity: $\gtrsim 10\Omega \cdot cm$; epi thickness: 10~20 μm
  - High resistivity substrates:
    - Resistivity: $\gtrsim 1\mathrm{k}\Omega \cdot cm$, no epi layers

Low-resistivity epi

- Charge collection for strip-based pixels: impact of resistivity







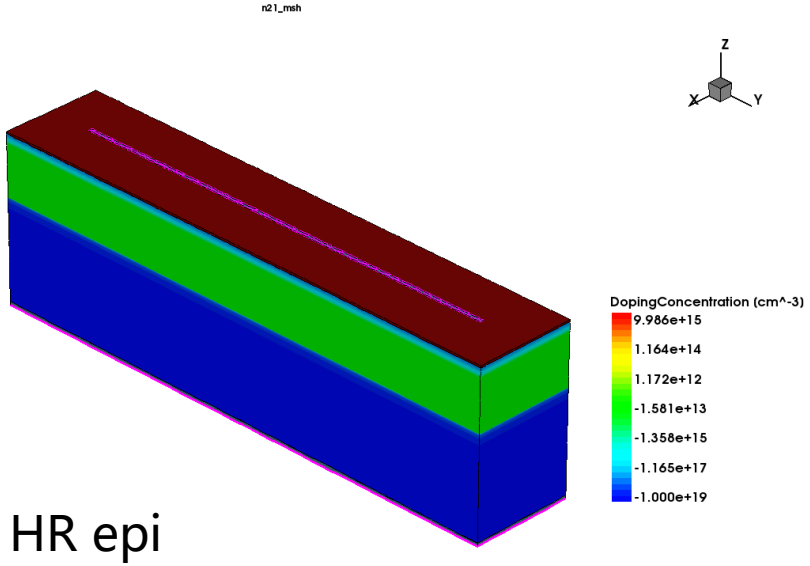
$1k\Omega \cdot cm$	Charge collected(e)	Total charge(e)	Collection time(ns)
P1	1100	2100	25
P2	570	2000	37

$10\Omega \cdot cm$	Charge collected(e)	Total charge(e)	Collection time(ns)
P1	730	1500	79
P2	260	1000	86

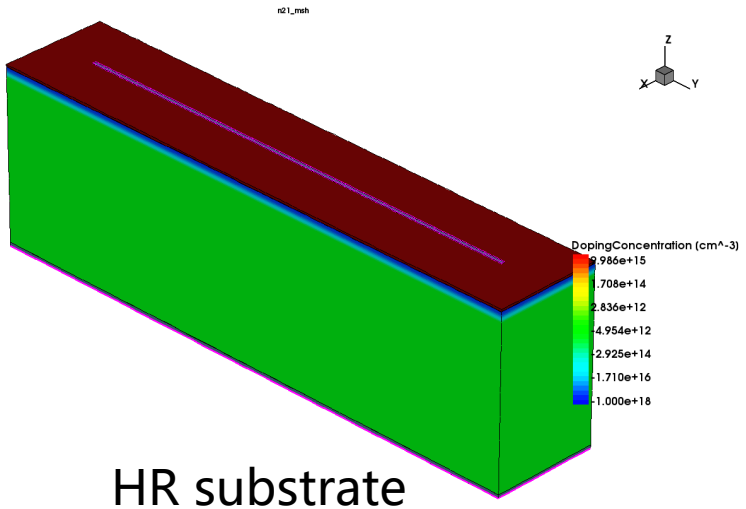
Apparently low-resistivity MAPS gives much lower collected charge and much slower signal response

High-resistivity substrate

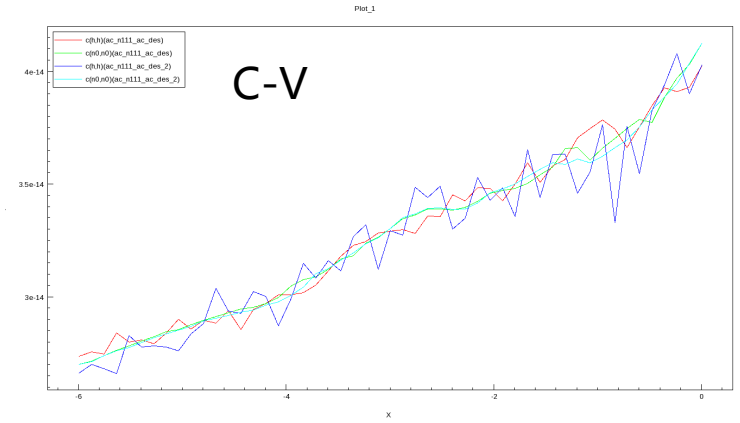
- Charge collection for strip-based pixels:
  - HR epi: HR epi 20μm, LR substrate 30μm
  - HR substrate: 50μm

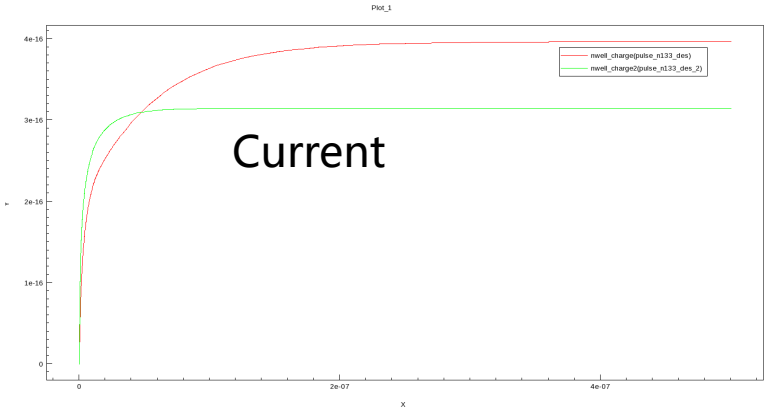


HR epi



HR substrate



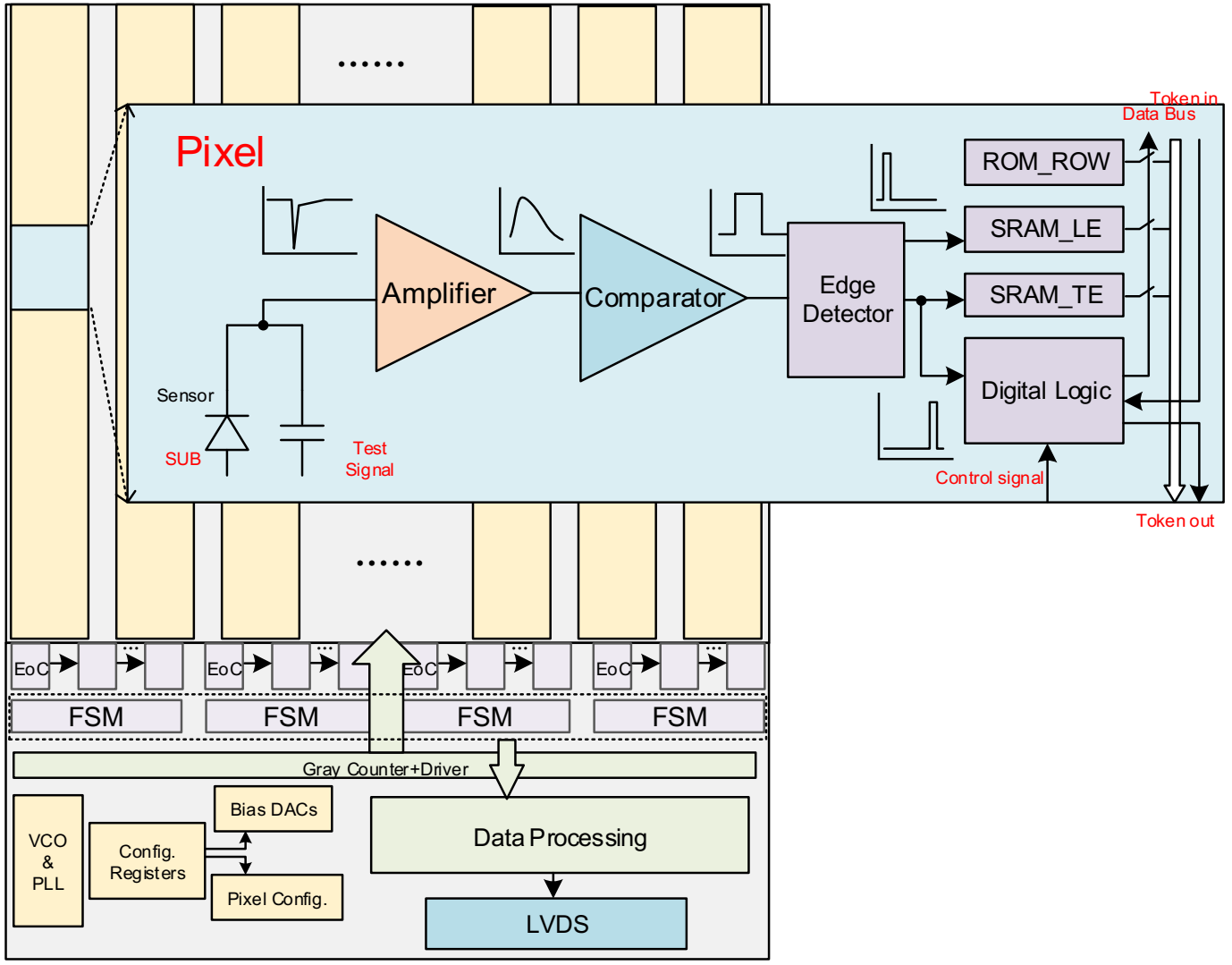


	Collected charge(e)	Collection time(ns)
HR epi	2000	17
HR substrate	2500	90

- Capacitance very similar
- Slower signal response, higher collected charge

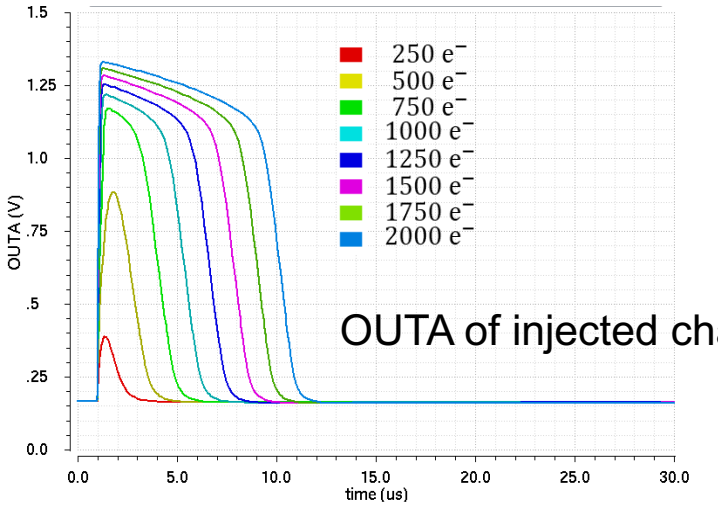
Readout architecture

- In-pixel circuits
  - Analog amplifier, comparator
  - Priority readout
  - SRAM, ROM
  - Charge injection
- Digital readout
  - End-of-column driver
  - Column level priority logic
  - Data processing module
  - Serializer
  - PLL, LVDS
- Analog configuration
  - VDAC×2, IDAC
  - Bandgap, EoC current mirror
  - I2C
- Test points

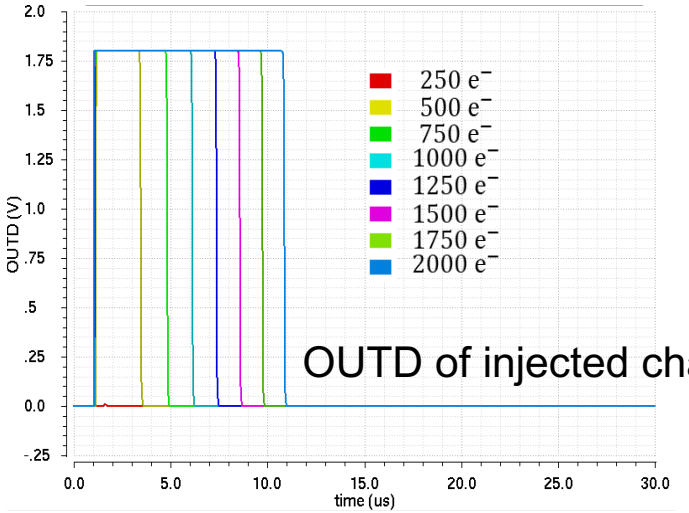


In-pixel front-end: analog

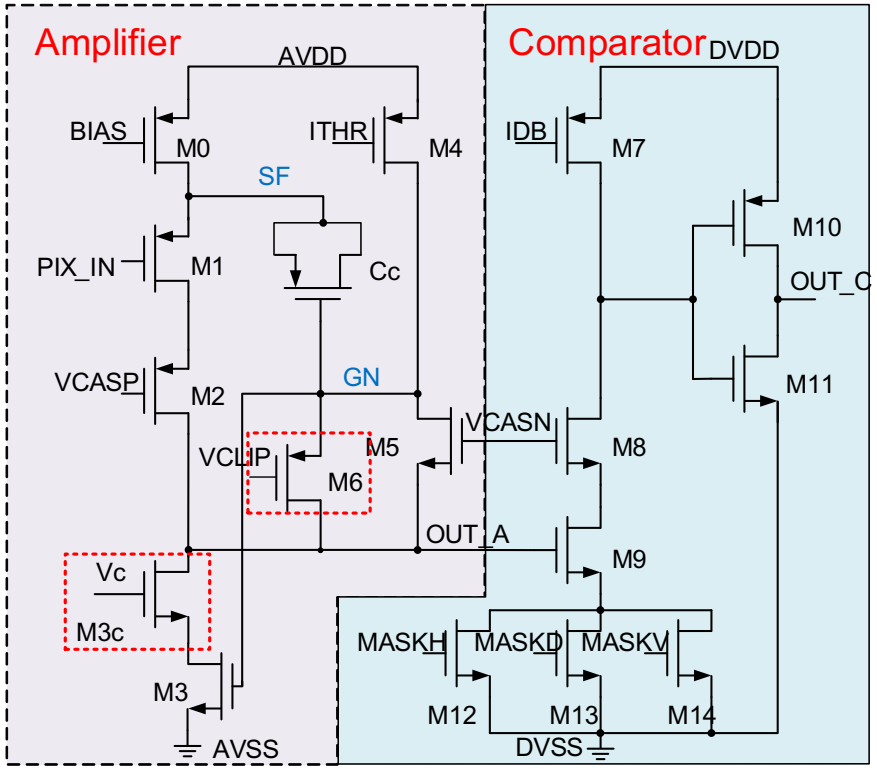
- Post layout simulation of the analog amplifier and comparator
- Simulated performance (180μm×30μm,strip-based sensor)
  - In the timing measurement mode: Threshold=309.0 e^-, ENC=11.4 e-, MISMATCH=5.7 e^-
  - Power consumption: ~800 nA/pix, ~26 mW/cm^2
  - ΔToT/ ΔQ_{inj}=4.8 μs/ke^-



OUTA of injected charge

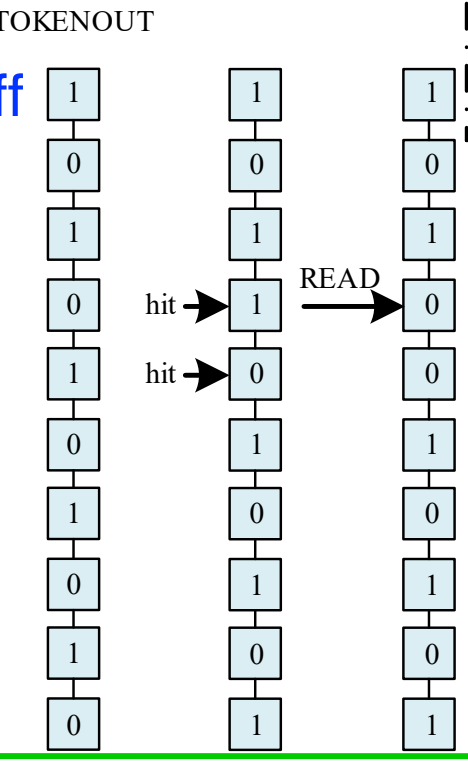


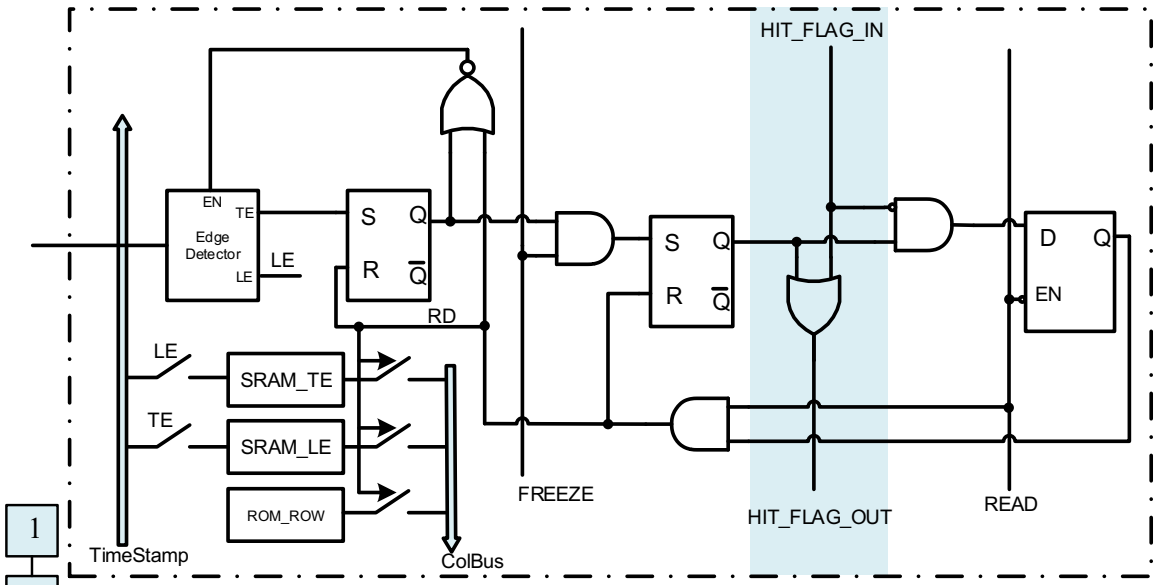
OUTD of injected charged

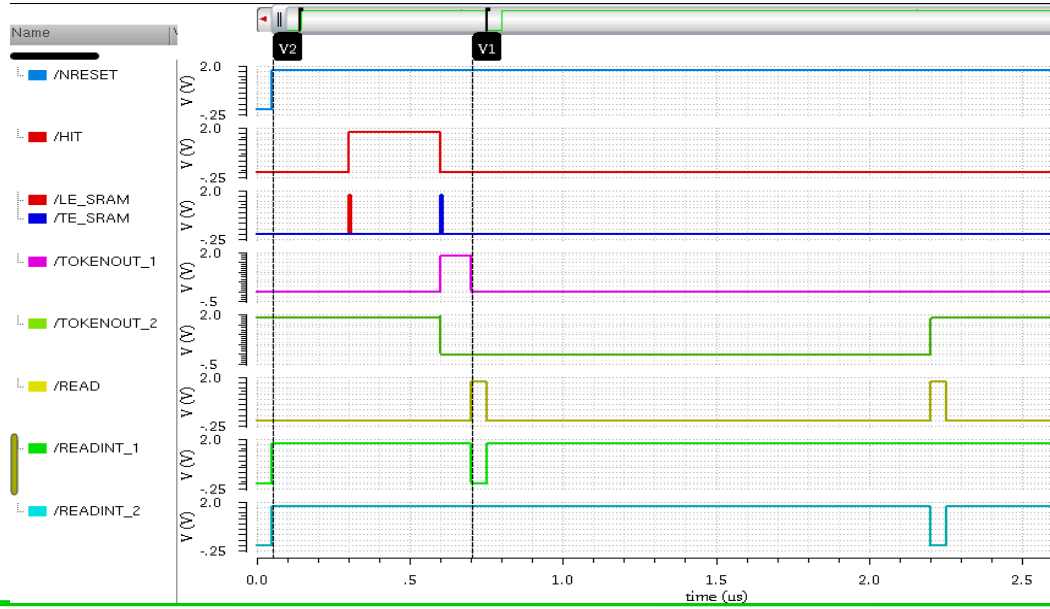


In-pixel front-end: digital

- In-pixel digital circuits
  - Priority readout based on TOKEN
  - Readout scheme similar to ATLAS FE-I3
  - Timestamp clock: 20MHz
  - 8-bit leading-/falling-edge
    - Can be optionally turned off
  - Readout clock: 10MHz

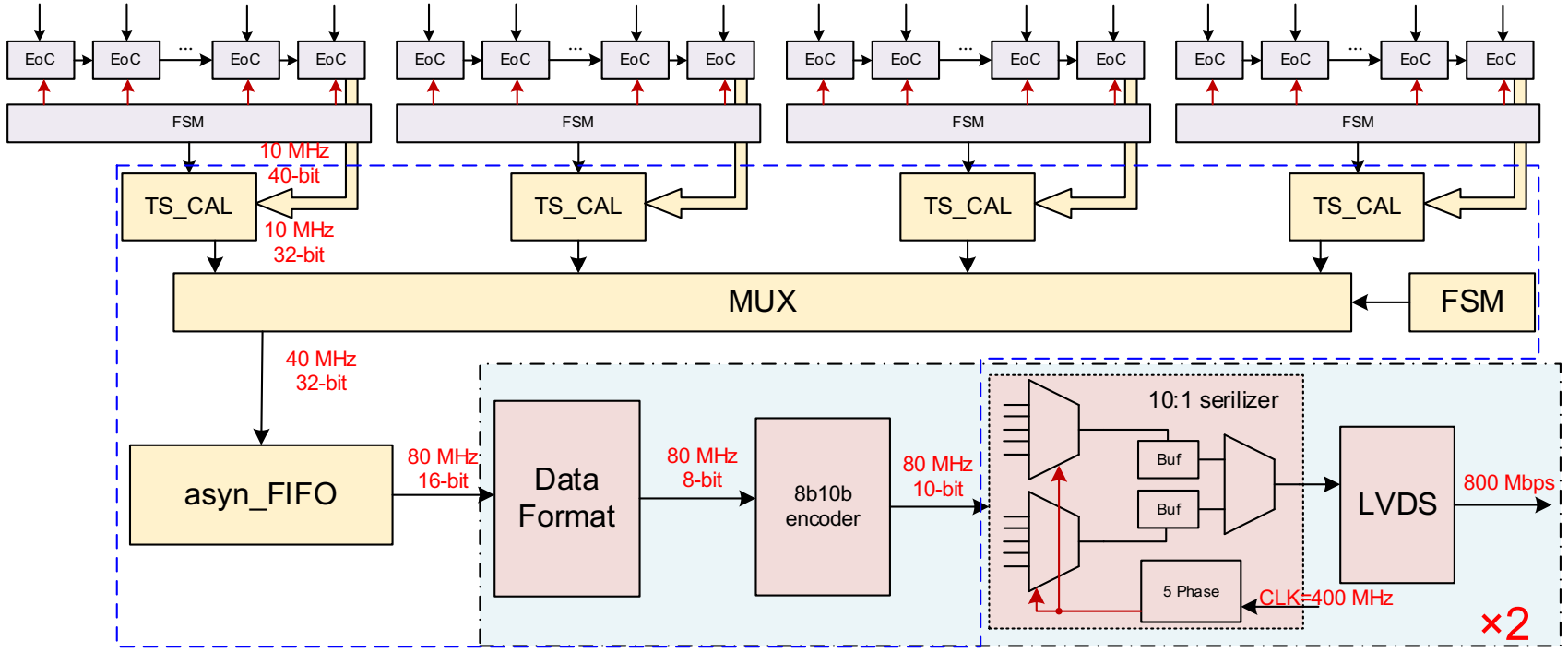






Peripheral readout

- EoC data readout circuit
  - Grouped columns with each group readout in parallel to reduce waiting time
  - Readout rate >29.6 MHz/Chip，40-bit/Hit(55-bit/Hit after frame encoding)
  - Bandwidth: 800Mbps×2



- Data processing unit
  - Timestamp calibration
  - Column group MUX
  - Async FIFO
  - Frame builder
  - 8b10b encoder
  - Serializer

Prototype chips

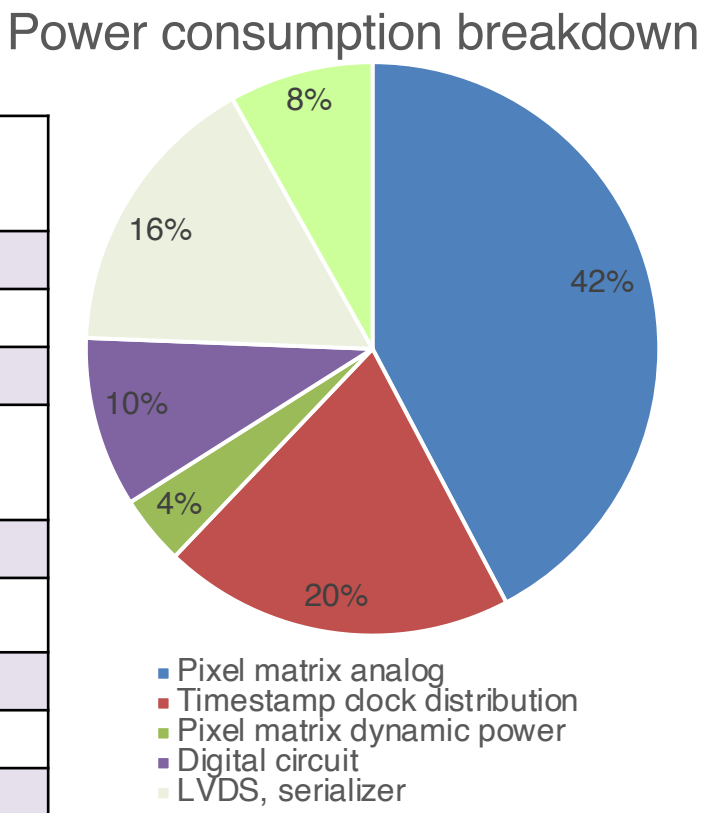
- Designed 4 prototype chips based on the TJ 180nm technology
  - Chip 1: ALPIDE-like small pixels，0/1 digital readout
  - Chip 2: large pixels ($96\mu m \times 60\mu m$, Strip-based + Pixel-based) with TOA+TOT readout
  - Chip 3: large pixels ($170\mu m \times 31\mu m$, Strip-based + Pixel-based) with TOA+TOT readout
  - Chip 4: 3T analog readout (5 types of sensors)

	Chip1	**Chip2**		**Chip3**		**Chip4**
Pixel size（μm×μm）	28.1x30.1	96.4x59.6		170.0x31.0		Mixed
Sensor	ALPIDE-like	Strip-based	Pixel-based	Strip-based	Pixel-based	Mixed
Pixel array	16x30	8x12	8x12	60x8	60x7	Mixed
Readout	Token	Token		Token		Analog readout
ToA & ToT	X	√		√		X
Chip area（mm^2）	1.5x1.4	2.5x1.6		2.8x3.1		1.2x1.4

Power density estimation

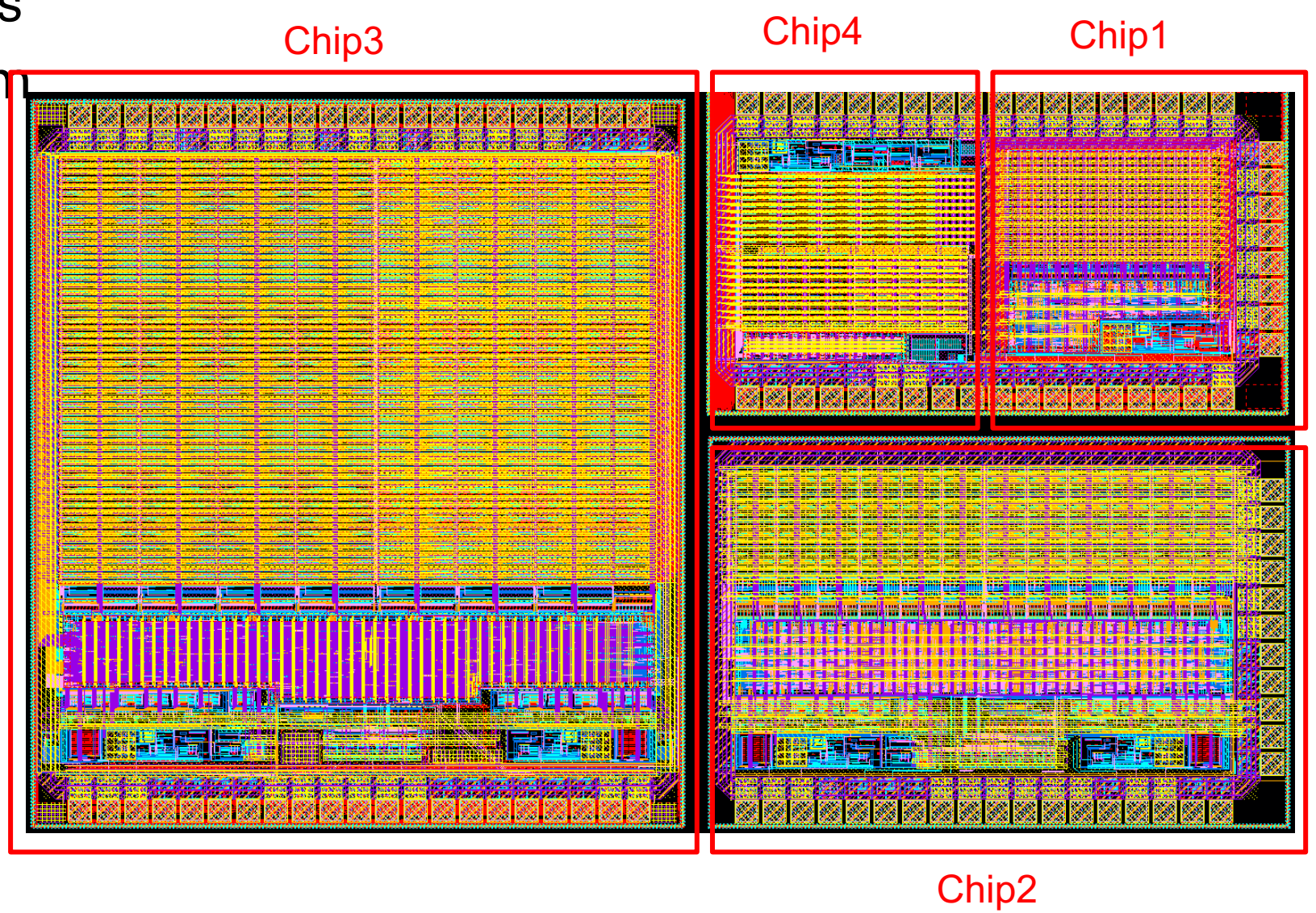
- Estimated power consumption extended to the full scale chip (~2 cm×2 cm)
  - Strip-based: 55.7 mW/cm^2
  - Pixel-based: 46.2 mW/cm^2
- Expected to reach the target of ~50 mW/cm^2
  - With the potential to use air cooling

Items	Power consumption	Notes
Analog in pixel matrix	~26 mW/cm^2	Strip-based
	~15 mW/cm^2	Pixel-based
Timestamp clock distribution	12.2 mW/cm^2	
Dynamic power consumption of the pixel matrix	2.4 mW/cm^2	with a data rate of 8.7 MHz/cm^2
Periphery	23.5 mW	32MHz event rate
PLL, serializer, LVDS	39 mW	x 2 data/clock output
Analog configuration	20 mW	
Total	222.6 mW	Strip-based
	184.6 mW	Pixel-based



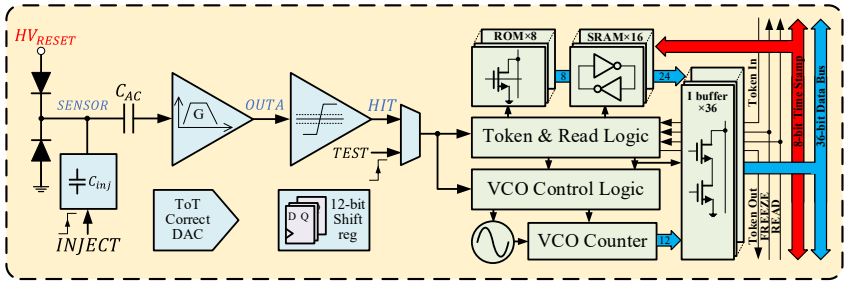
Prototype chips

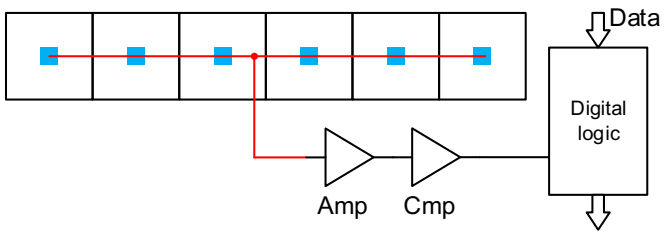
- Layout of the 4 prototype chips
- Total area: 5.4 mm× 3.15 mm
- To be submitted in 2024 Q1

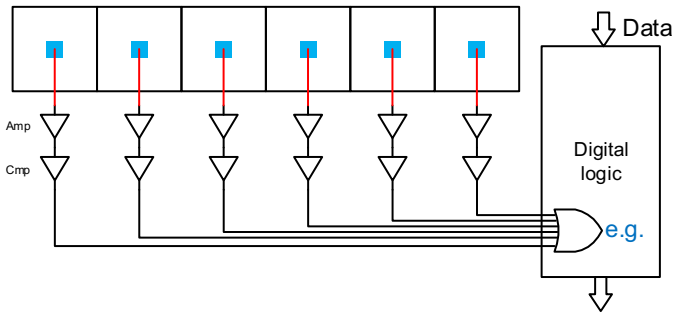


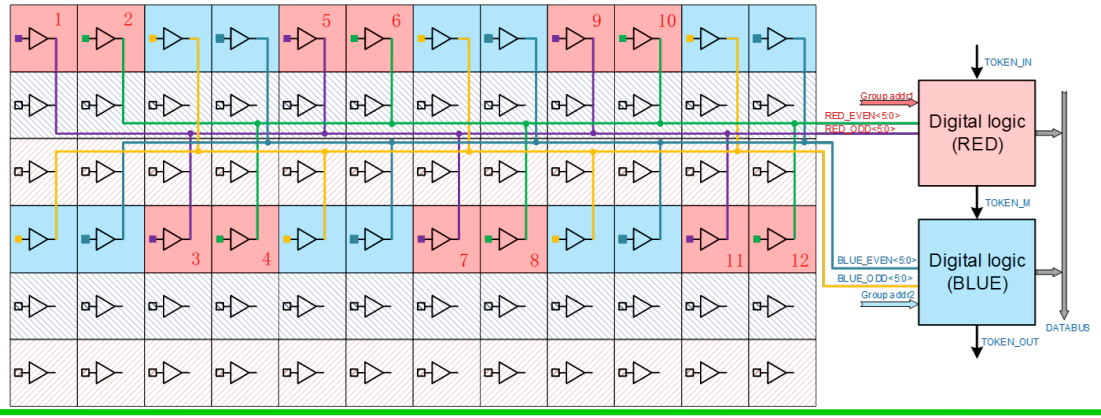
Alternative designs

- Also exploring alternative technologies based on domestic CMOS foundries
  - Nexchip at Hefei: 90nm CIS, 12 inch wafers
    - Only support low resistivity epi
    - Only 4 metal layers and no deep p-well currently → with the potential to increase to 6 metal layers and support deep p-well
    - Prototype chips design finished, with VCO counter to reduce TDC bin size
  - Shanghai HHGrace GSMC 130nm CIS
    - Only support high resistivity substrate
    - 6 metal layers and support deep p-well
    - Chip design ongoing with improved readout









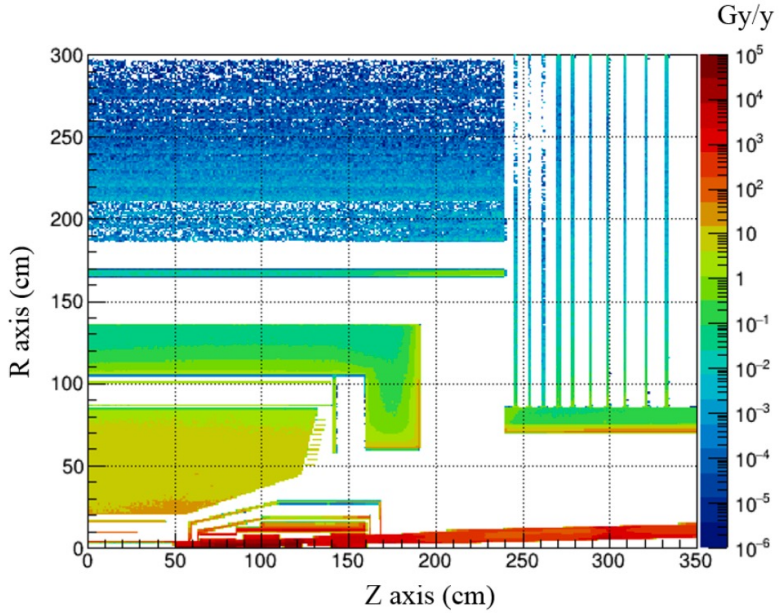
Summary

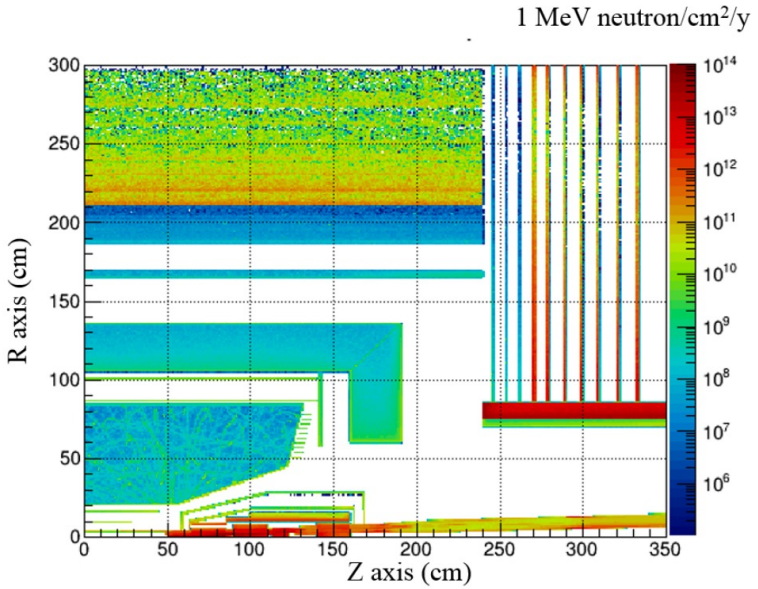
- MAPS-based inner tracker is a promising option for the STCF
  - Spatial resolution: $\leq 100\mu m$
  - Power consumption: $\leq 100mW/cm^2$
  - Low material budget per layer: $\leq 0.35\%\ X_0$
  - Time resolution: $\leq 50\mathrm{ns}$
- Prototype chips design finished and to be submitted to the foundry in 2024.3
  - Based on the TJ 180nm HR epi technology
- Also exploring alternative CIS technologies
  - 90nm CIS with LR epi
  - 130nm CIS with HR substrate

Backup

Radiation level

- Simulated radiation level





Detector	Highest TID value per pixel (Gy/y)	Highest NIEL damage per pixel (1 MeV neutron/cm^2/y)	Highest count rate per channel (Hz/channel)
Silicon-inner-1	3490	1.75×10^{11}	2.61×10^{2}
Silicon-inner-2	320	3.72×10^{10}	2.74×10^{1}
Silicon-inner-3	150	2.68×10^{10}	8.51×10^{0}

NIEL: ~ 10^{11} n_{eq}/cm^2/y
TID: ~0.35MRad/year