

课题3: 基于MAPS的高位置分辨低物质质量 径迹探测器研发 -- 研发进展汇报

王亚平（华中师大）

课题单位：华中师范大学

中国科学院近代物理研究所

超子-核子谱仪物理研讨会，南开大学，2026年

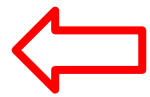


- 背景介绍
- 课题目标及考核指标
- 课题年度计划
- 课题研究进展
 - MAPS芯片研发进展
 - MAPS探测器研发进展
- 总结与展望

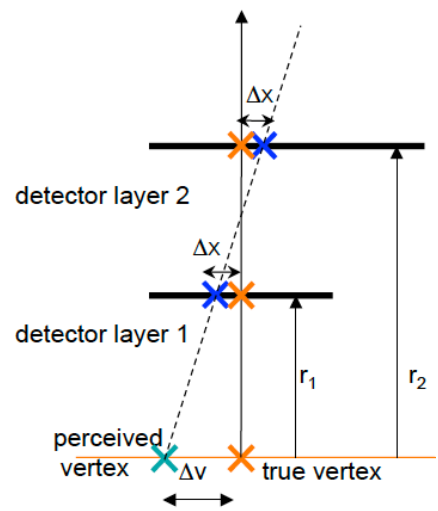
背景介绍 – Why We Need Pixel Tracker in HIC

径迹探测器的性能参数：

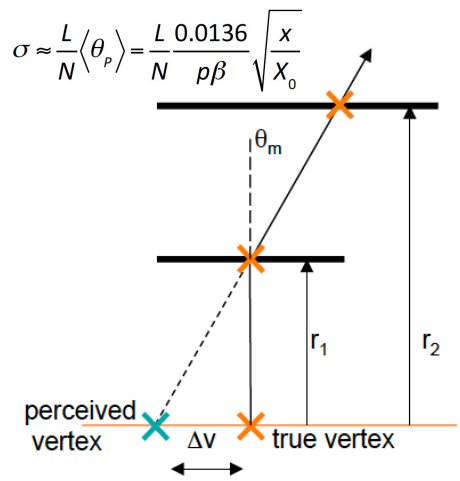
1. 碰撞参数分辨率
2. 动量分辨率
3. 寻迹效率



- 物质质量
- 固有位分辨率
- 到碰撞点的距离

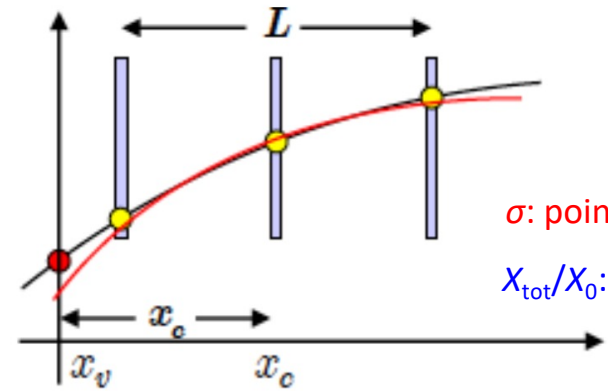


$$\Delta v = \Delta x \cdot \sqrt{\frac{r_2^2 + r_1^2}{(r_2 - r_1)^2}}$$



$$\Delta v = \theta_m \cdot r_1$$

Ref.: Luciano Musa@HP2023



σ : pointing resolution/plane
 X_{tot}/X_0 : total material budget

Ref.: R.L. Gluckstern, NIMA 24 (1963), 381-389

$$\frac{\Delta p_t}{p_t} = \frac{\sigma[m] p[\text{GeV}/c]}{0.3 B[T] L^2[m^2]} \sqrt{\frac{720 (N-1)^3}{(N-2) N (N+1) (N+2)}}$$

$$\approx \frac{\sigma[m] p[\text{GeV}/c]}{0.3 B[T] L^2[m^2]} \sqrt{\frac{720}{N+4}}$$

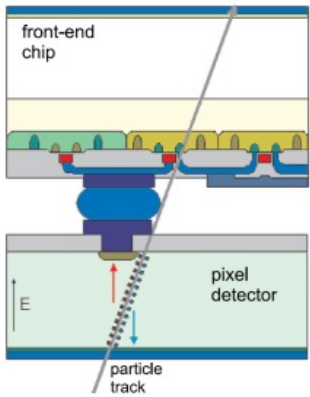
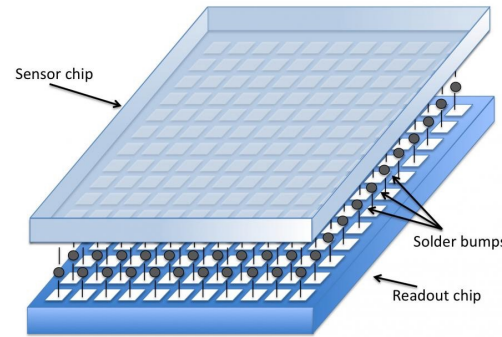
$$\frac{\Delta p_t}{p_t} = \frac{0.0136}{0.3 \beta B[T] L[m]} \sqrt{\frac{X_{tot}}{X_0}} \sqrt{\frac{10}{7} \frac{12 + (N-1)N^2(N+1)}{(N-2)N(N+1)(N+2)}}$$

$$\approx \frac{0.0136}{0.3 \beta B[T] L[m]} \sqrt{\frac{X_{tot}}{X_0}} \sqrt{\frac{10}{7}}$$

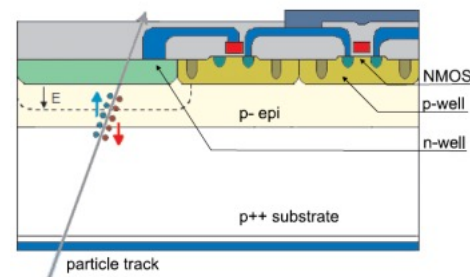
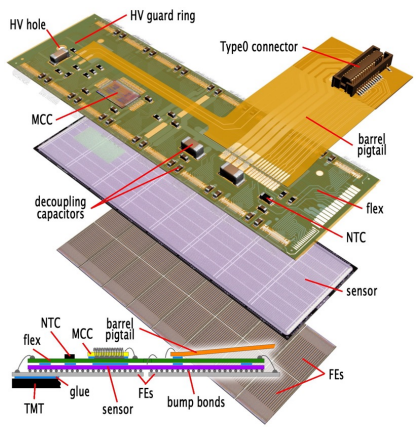
$$\approx \frac{0.0542}{\beta B[T] L[m]} \sqrt{\frac{X_{tot}}{X_0}}$$

背景介绍 – Pixel Tracker in HIC

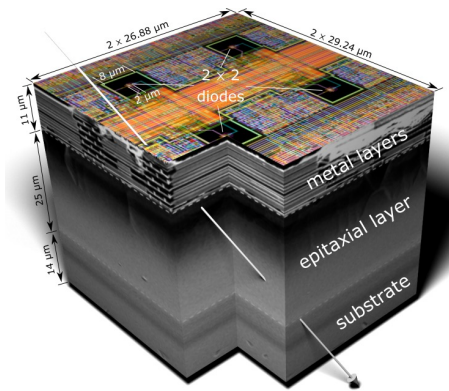
- “The silicon micropattern detector: a dream?”
E.H.M Heijine, P. Jarron, A. Olsen and N. Redaelli, *Nucl. Instrum. Meth. A* 273 (1988) 615
- “Development of silicon micropattern detectors”
CERN RD19 collaboration, *Nucl. Instrum. Meth. A* 348 (1994) 399
- 1995 – First Hybrid Pixel detector installed in WA97 (CERN, Omega facility)
- 1996/97 – First Collider Hybrid Pixel Detector installed in DELPHI (CERN, LEP)
- Silicon pixel detectors were installed at the heart of LHC experiments since 2005



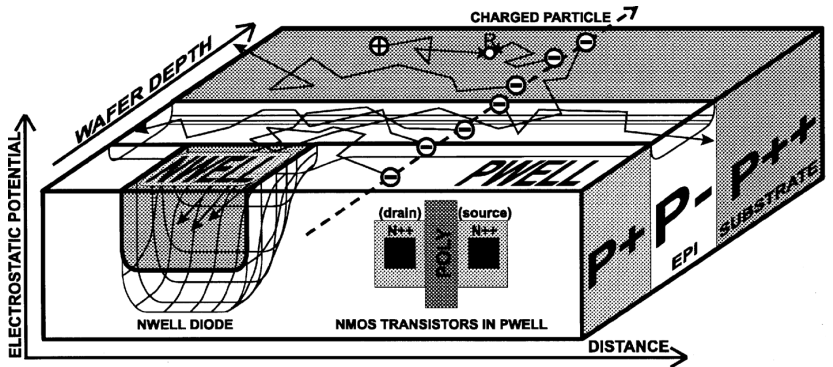
混合式像素传感器 (Hybrid)



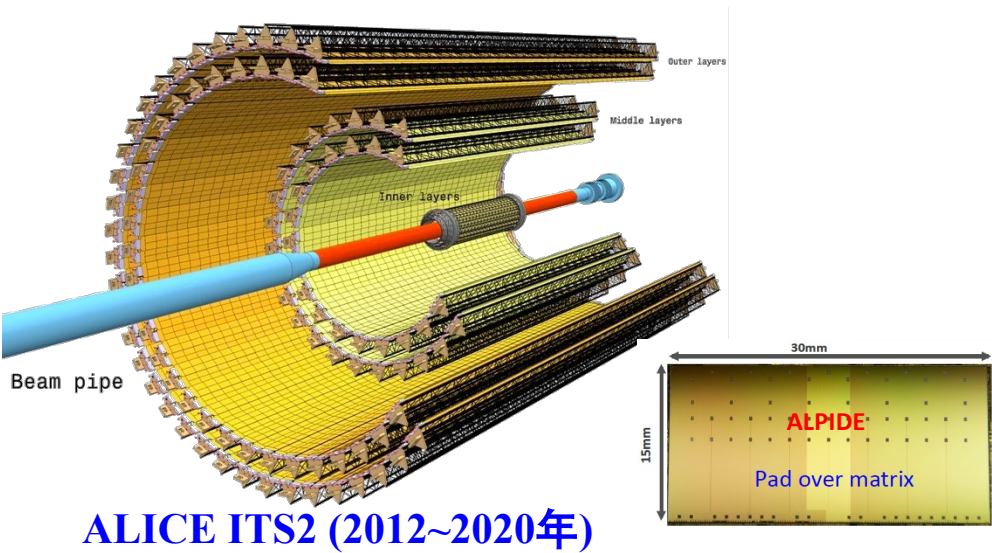
单片有源式像素传感器 (Monolithic Active Pixel Sensor, MAPS)



背景介绍 – MAPS Tracker in HIC

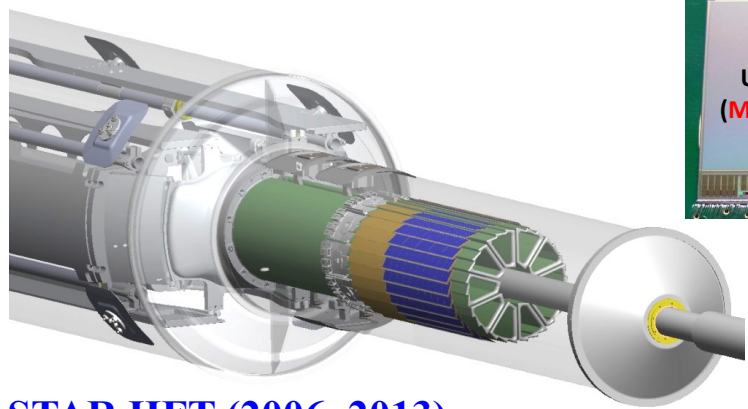


MAPS (2001): doi:10.1016/S0168-9002(00)00893-7



ALICE ITS2 (2012~2020年)

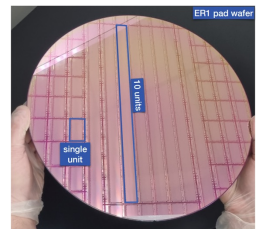
2026年8月16日



STAR HFT (2006~2013)

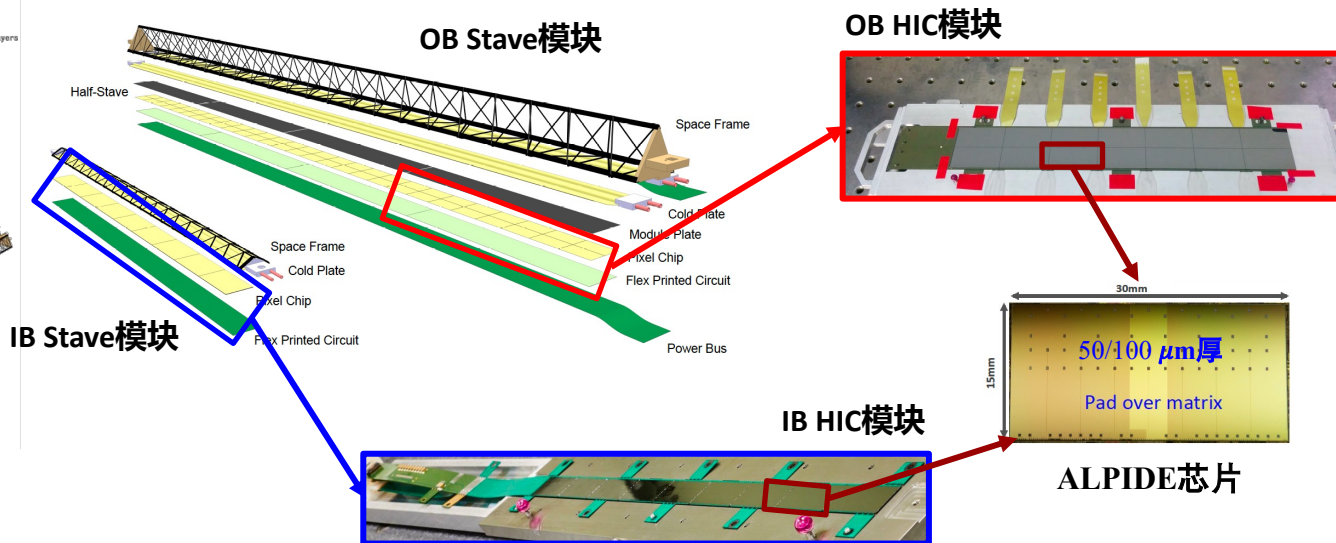
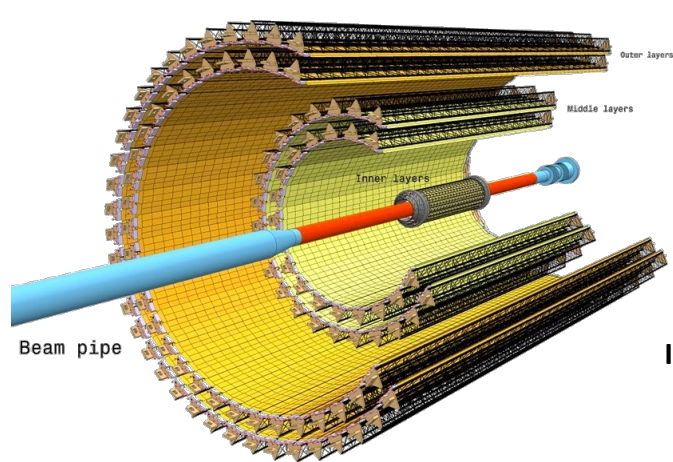


ALICE ITS3 (2019~2027)



背景介绍 – ALICE ITS2 Upgrade (recap)

✓ ALICE/ITS2探测器模块的结构设计

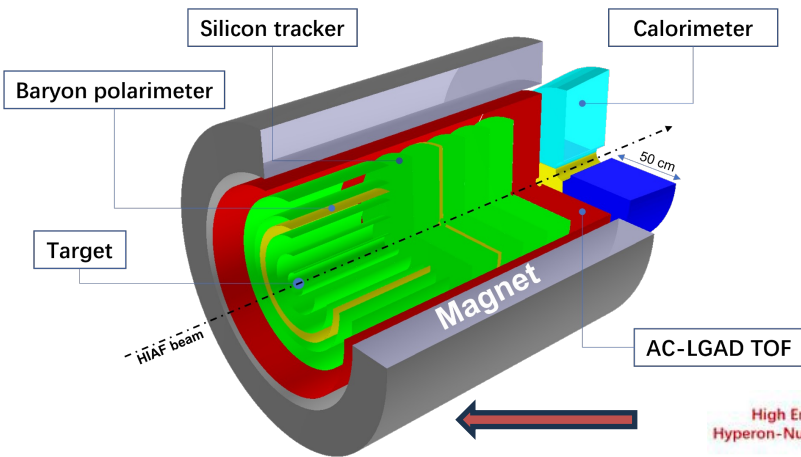


Inner Tracking System 2

7 layers of MAPS, 12.5G pixels

- Monolithic Active Pixel Sensor (MAPS)
- 5 μm impact parameter resolution
- 7 cylinders covering $\sim 10 \text{ m}^2$ area
- Innermost radius: 23 mm

- Inner Barrel (IB): $\sim 0.35\% X_0$
 - ✓ 3 Inner Layers (48 x 9-chip Staves)
- Outer Barrel (OB): $\sim 0.85\% X_0$
 - ✓ 2 Outer Layers (90 x 14-HIC Staves)
 - ✓ 2 Middle Layers (54 x 8-HIC Staves)



Hyperon-Nucleon Spectrometer (H-NS)

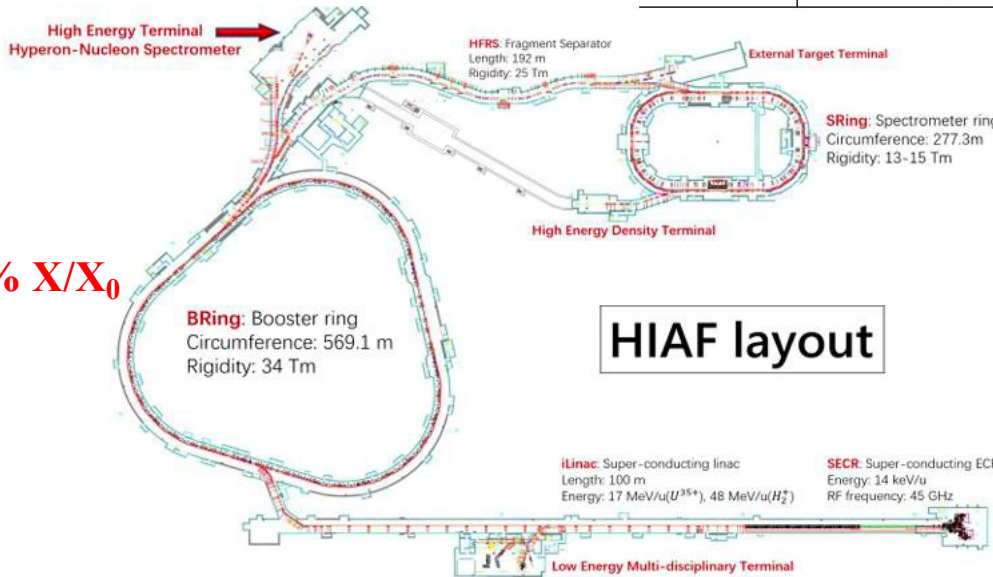
$$p+p \rightarrow p + K^+ + \Lambda$$

$$U+U \rightarrow {}^3_{\Lambda}H + \dots$$

Ion species	Kinetic Energy (GeV/u)	Beam intensity (ppp)
p	9.3	6.0×10^{12}
$^{16}\text{O}^{8+}$	4.25	6.0×10^{11}
$^{18}\text{O}^{6+}$	2.6	6.0×10^{11}
$^{78}\text{Kr}^{19+}$	1.7	3.0×10^{11}
$^{209}\text{Bi}^{31+}$	0.85	1.2×10^{11}
$^{238}\text{U}^{35+}$	0.835	1.0×10^{11}
$^{238}\text{U}^{78+}$	2.6	1.0×10^{10}

H-NS major requirements:

- Mag. Field: 1.5 Tesla
- Tracker: MIC6, $30 \times 30 \mu\text{m}^2$, $<0.8\% X/X_0$
- LGAD: $\sigma_t \sim 30 \text{ ps}$, $300 \times 300 \mu\text{m}^2$
- Calorimeter: $\sigma_E \sim 3\% @ 1\text{GeV}$
- Polarimeter: nucleon and photon polarization



近期规划: 利用 HIAF 束流开展高能核物理研究

长期规划: HIAF $\rightarrow$ HIAF-U $\rightarrow$ EicC

超子-核子谱仪 – MAPS径迹探测器关键技术

- To achieve momentum resolution ($\sim 2\% @ 1 \text{ GeV}/c$) and high SNR in Λ reconstruction, **material budget below 0.8% X/X_0 per layer** is required

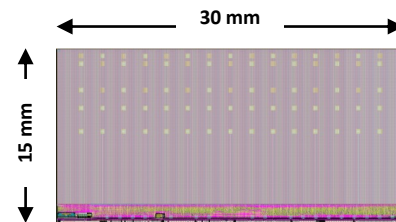
✓ **MAPS-based MIC6 pixel chip:** MIC6-v4 (CCNU), **spatial resolution $\sim 10 \mu\text{m}$** with pixel size $30 \mu\text{m}$, developed and manufactured with the domestic process

✓ **Mechanics:** carbon fiber mechanics, water cooling, low mass flexible PCB (FPC)

✓ **Detector assembly and integration:**

- Barrel tracker: Stave module design
- Forward tracker: Ladder module aligned to disk super-module

✓ **Readout electronics and DAQ** (see *Lei Zhao & Kai Chen's talks*)



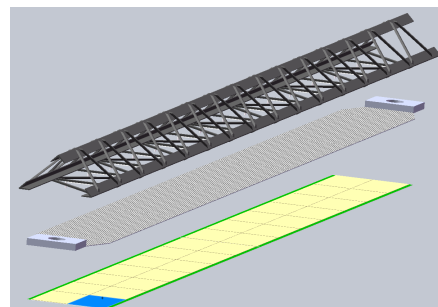
MIC6-v4

Identical geometry to ALPIDE

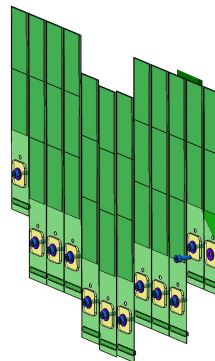
chip module (chip + FPC)



Ref. ITS2



stave module (chip module + carbon mechanics)

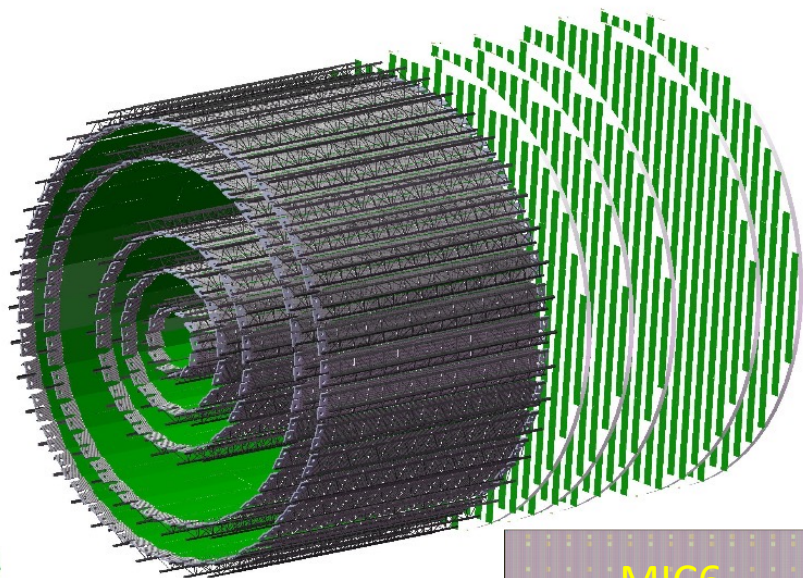


Forward disk module

Ref. MFT

超子-核子谱仪 – MAPS径迹探测器概念设计

✓ H-NS/MAPS径迹探测器几何布局 (见H-NS白皮书 [arXiv:2606.06553v1](https://arxiv.org/abs/2606.06553v1))

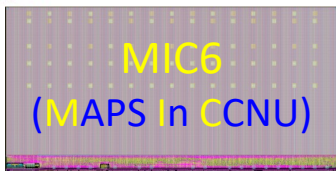


桶部:

R (cm)	Length (cm)	Pitch Size (μm)	Material Budget (X/X_0)	Tech.
5.0	42	30	< 0.8%	MIC6
11.0	42	30	< 0.8%	MIC6
17.0	42	30	< 0.8%	MIC6
29.0	42	30	< 0.8%	MIC6
35.0	42	30	< 0.8%	MIC6

端盖:

In R (cm)	Out R (cm)	Z (cm)	Pitch Size (μm)	Material Budget (X/X_0 %)	Tech.
2.0	38	30	30	< 0.8%	MIC6
2.0	38	39	30	< 0.8%	MIC6
2.0	38	48	30	< 0.8%	MIC6
2.0	38	66	30	< 0.8%	MIC6
2.0	38	75	30	< 0.8%	MIC6



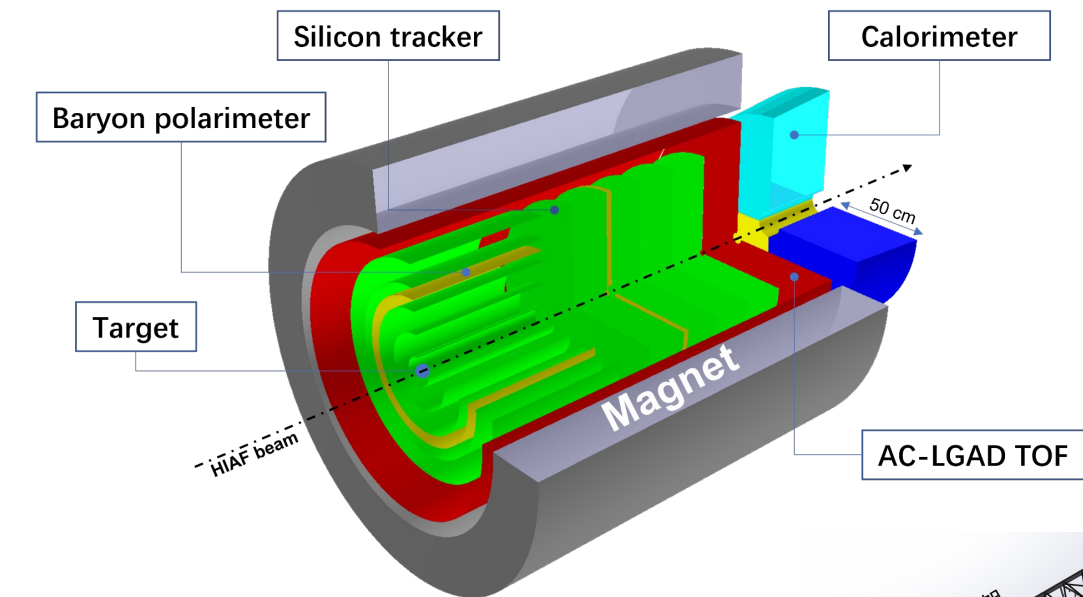
周江鹏 (CCNU) 提供

• **5.2 m² MAPS in total**

✓ Barrel: 5 stave layers, ~2.9 m²

✓ Endcap: 5 disk layers, ~2.3 m²

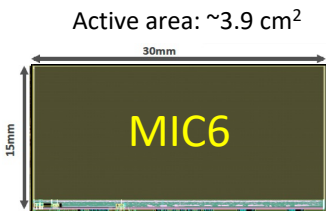
课题目标



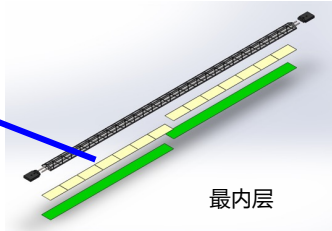
- 重离子碰撞实验：高事例率，高径迹数，强辐照
- 探测器挑战：高精度，快速响应及抗辐照能力

课题目标:

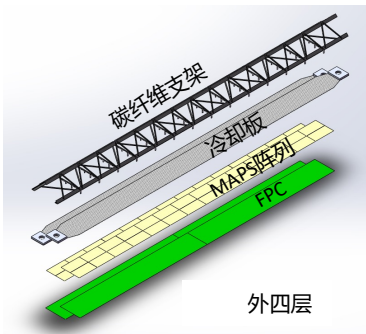
1. 重点发展基于MAPS的径迹探测器核心技术，MAPS像素探测器芯片集成精度优于5微米，单层物质质量小于 $0.35\% X/X_0$
2. 利用stave模块样机组装可测试系统，探索多层筒形结构探测器原型机的技术方案



MAPS像素芯片



混合集成电路(HIC)模块：1×7或2×7枚MAPS芯片组装在柔性印制电路板(FPC)上并电学连接



Stave模块：1个或多个HIC模块沿束流方向拼接组装在碳纤维支撑材料上

❖ 采用国产化工艺，为超子-核子谱仪(H-NS)实验开展MAPS径迹探测器的关键技术攻关！

考核指标

❖ 课题研究内容



❖ 课题考核指标

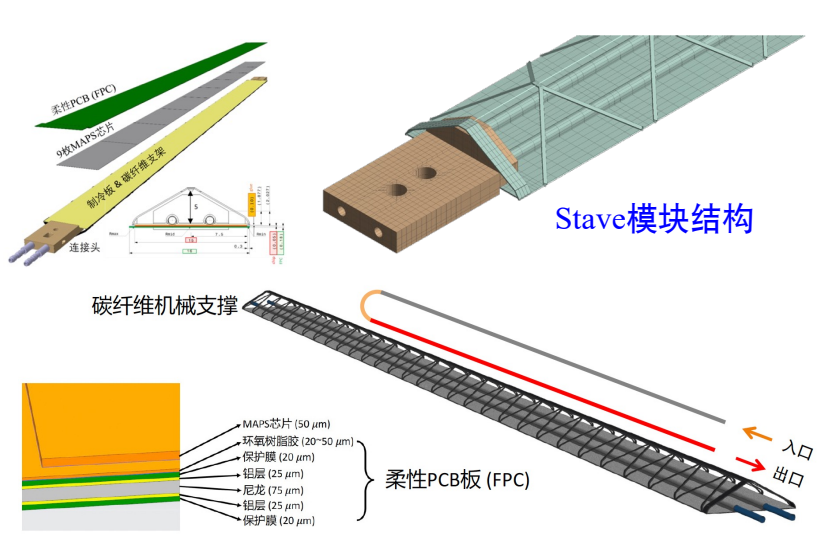
考核指标 ²			
指标名称	立项时已有指标值/状态	中期指标值/状态 ³	完成时指标值/状态
指标 1.1 芯片集成精度（关键核心指标）	芯片集成精度优于 20 μm	芯片集成精度优于 10 μm	芯片集成精度优于 5 μm
指标 1.2 单层物质量（关键核心指标）	单层物质量小于 1.0% X_0	单层物质量小于 0.85% X_0	单层物质量小于 0.35% X_0

预期成果：基于MAPS的stave模块样机
考核方式：制定测试方案，邀请同行专家进行测试方式，并出具测试报告

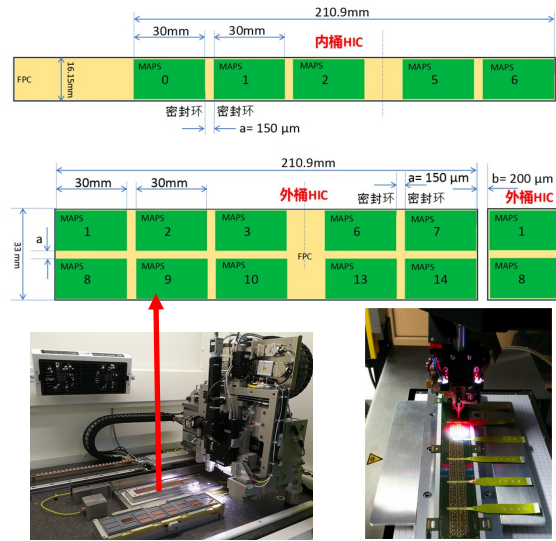
课题实施方案

- 通过Geant和物理模拟，开展探测器结构设计和几何参数优化
- 通过有限元分析方法（FEA）开展模块结构的静力分析与热分析，优化机械结构设计并验证性能
- 通过模型仿真与样品试制来定型柔性PCB、机械结构与制冷等，制定模块组装和测试工艺
- 完成高精度芯片拼接完成HIC模块制作，进而实现stave模块样机的制作与测试

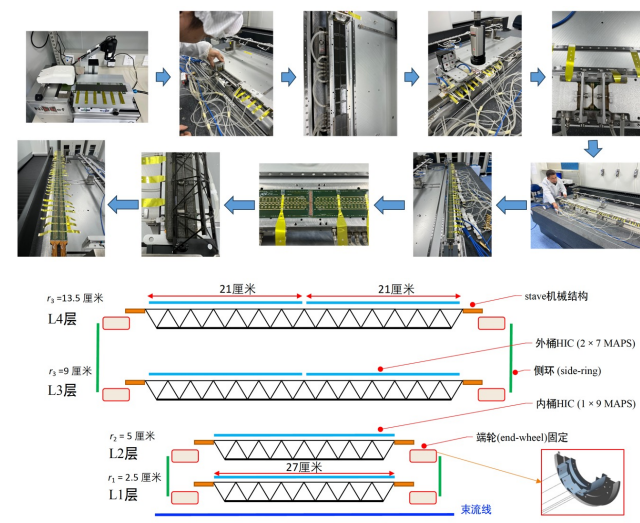
1. Stave模块结构与仿真及其制作 2. 高精度MAPS芯片集成与模块制作 3. Stave模块样机及多层集成



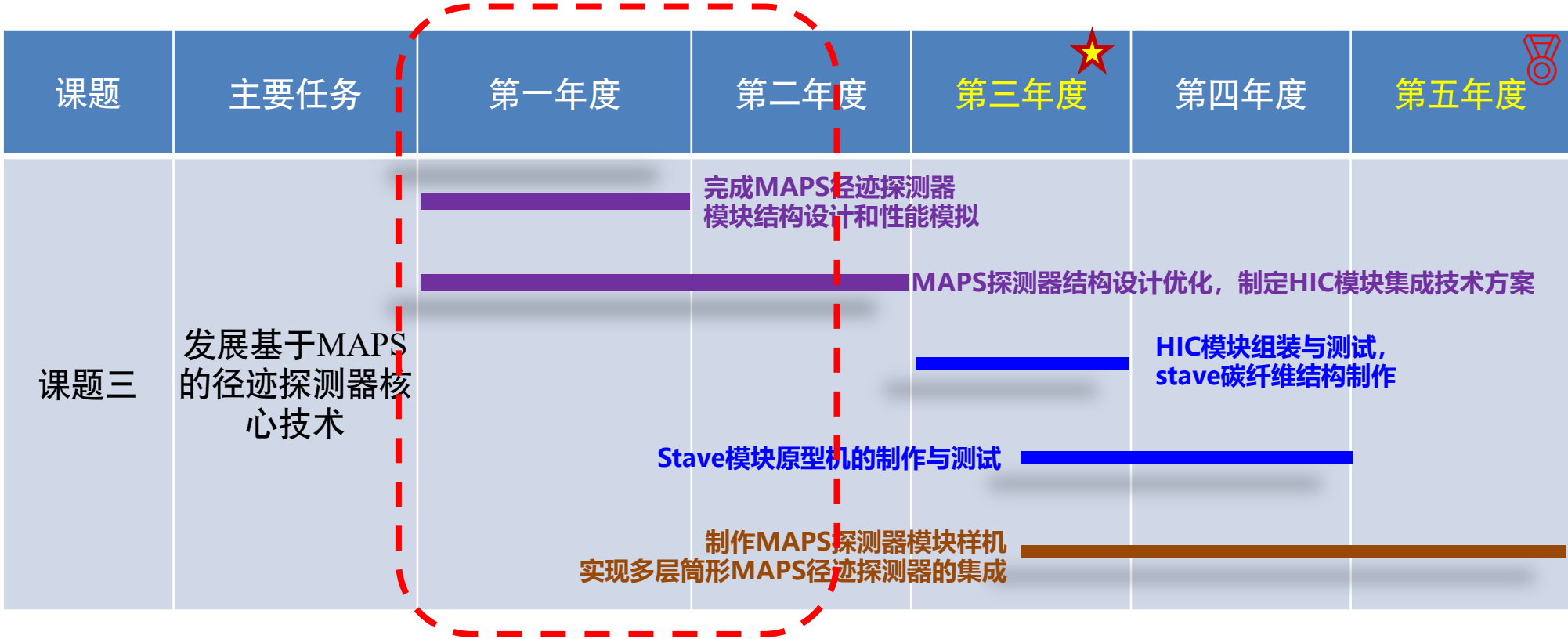
低物质量： 柔性PCB + 碳纤维机械支撑



**高精度芯片集成 + 高良率：
自动化芯片拼接 + 焊线**



**MAPS径迹探测器stave模块及
多层筒形扇区原型机集成**



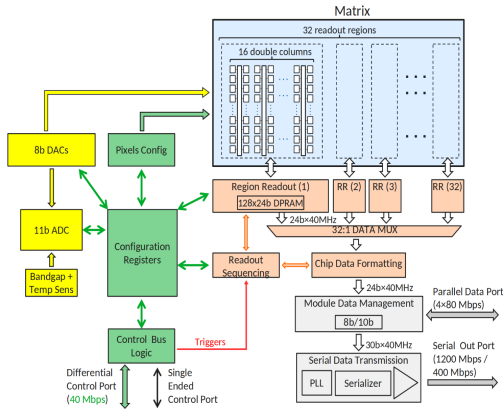
★ 项目中期

🏆 项目结题

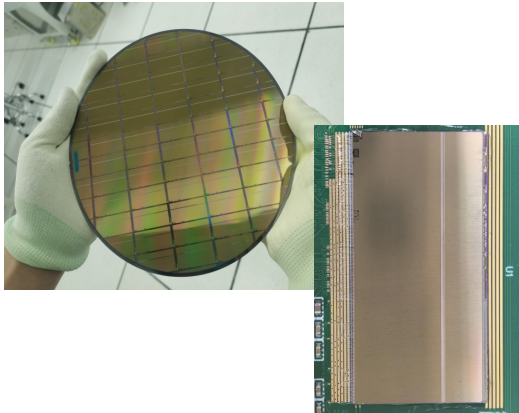
✓ MIC6_V3 chip developed with domestic modified process

Features	ALPIDE	MIC6_V3
Process Technology	180nm	130nm
Core Voltage	1.8V	1.2V
Chip Size	30 mm×15 mm	30 mm×15 mm
Pixel Array	1024×512	980×512
Pixel Size	29.24 um×26.88 um	30.53 um×26.8 um
Zero Suppression Readout	AERD	AERD
High-Speed Serial Output	1.2Gbps	1.1Gbps
Power Consumption	40 mW/cm ²	32 mW/cm ²

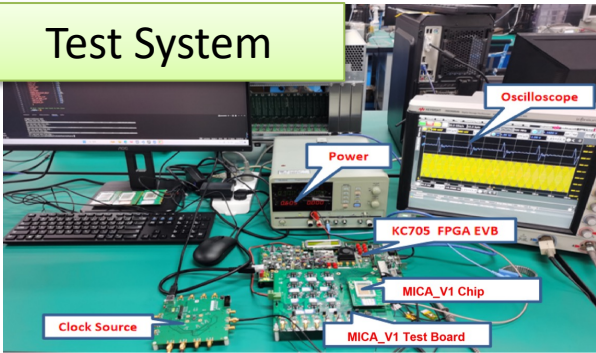
MIC6_V3 Architecture



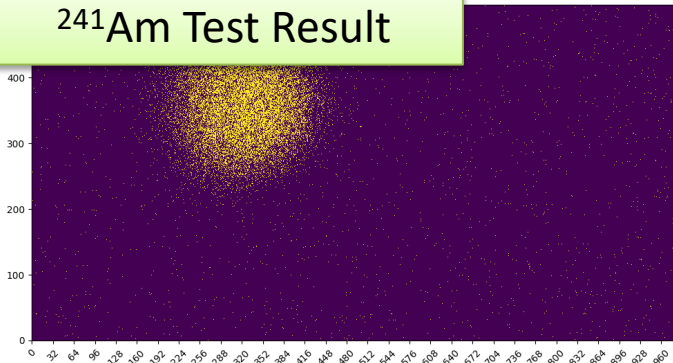
MIC6_V3 Chip



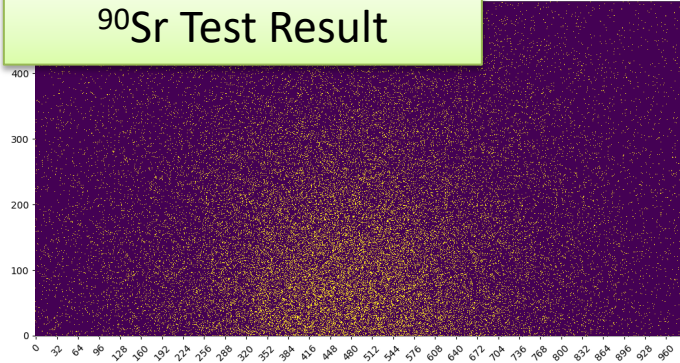
Test System



²⁴¹Am Test Result

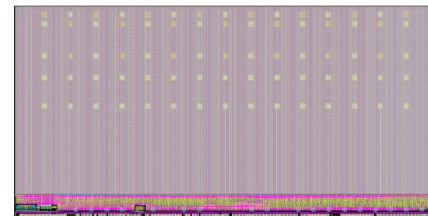


⁹⁰Sr Test Result

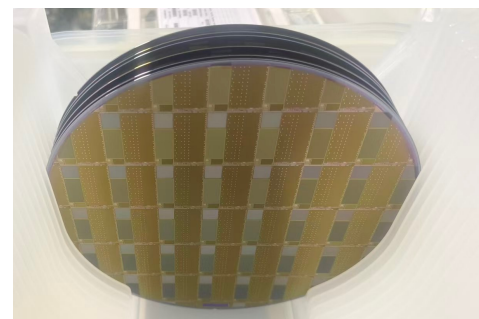
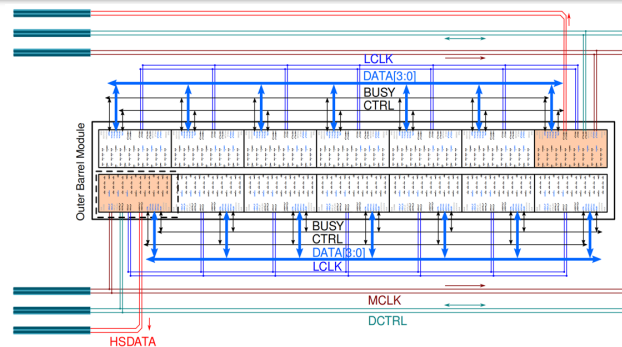


- ## MIC6 V4 Architecture

MIC6_V4 Layout



MIC6_V4 Chip

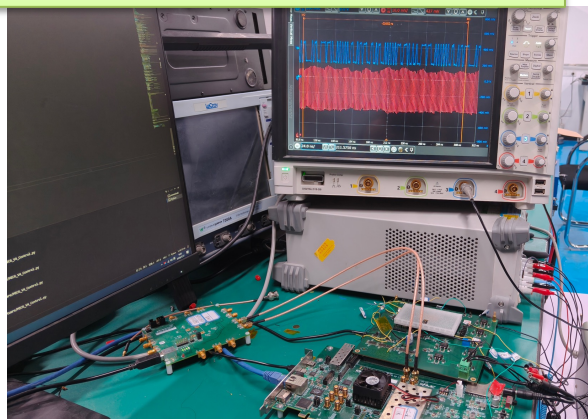


**Received the MIC6_V4
at the end of June, and
testing launched!**

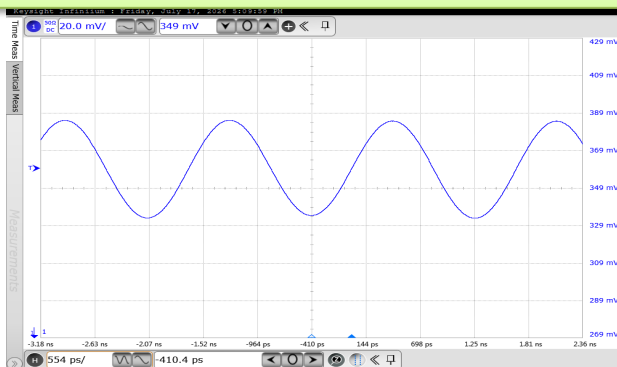
- ## MAPS探测器研制进展 -- YPW

✓ Preliminary test of MIC6_V4 chip at CCNU

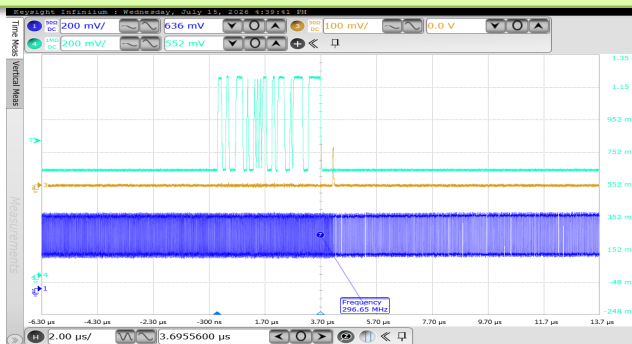
MIC6_V4 Test System



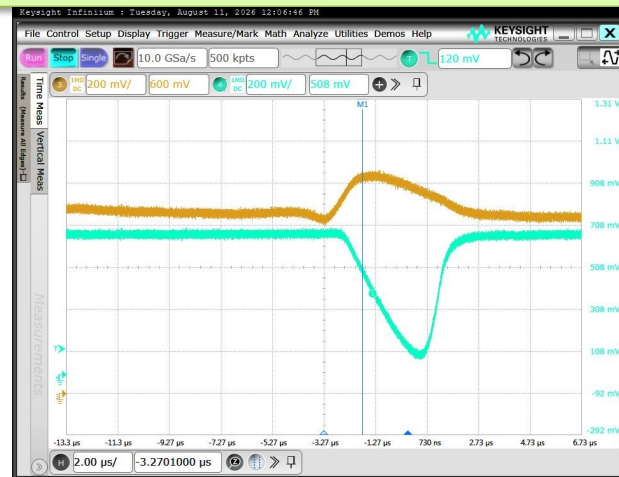
PLL Output 600MHz Clock



CMU Configure PLL Clock



Pixel Out_A & Out_D

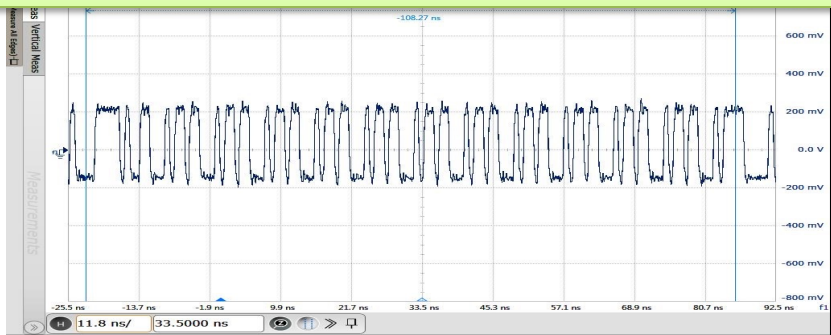


Positive results:

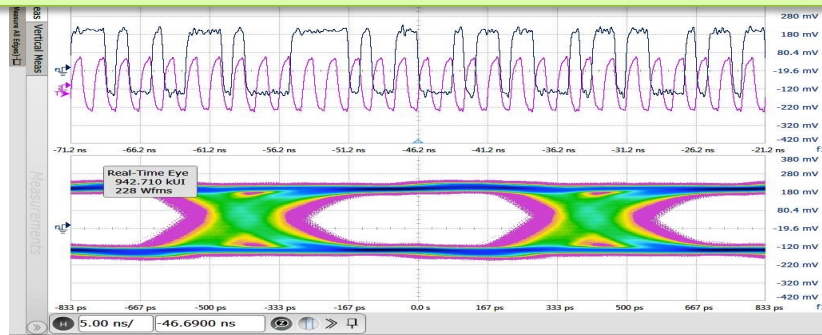
- MLVDS Module ✓
- PLL Module ✓
- Control Management Unit ✓
- DAC ✓
- Pixel Front-end ✓

✓ Preliminary test of MIC6_V4 chip at CCNU

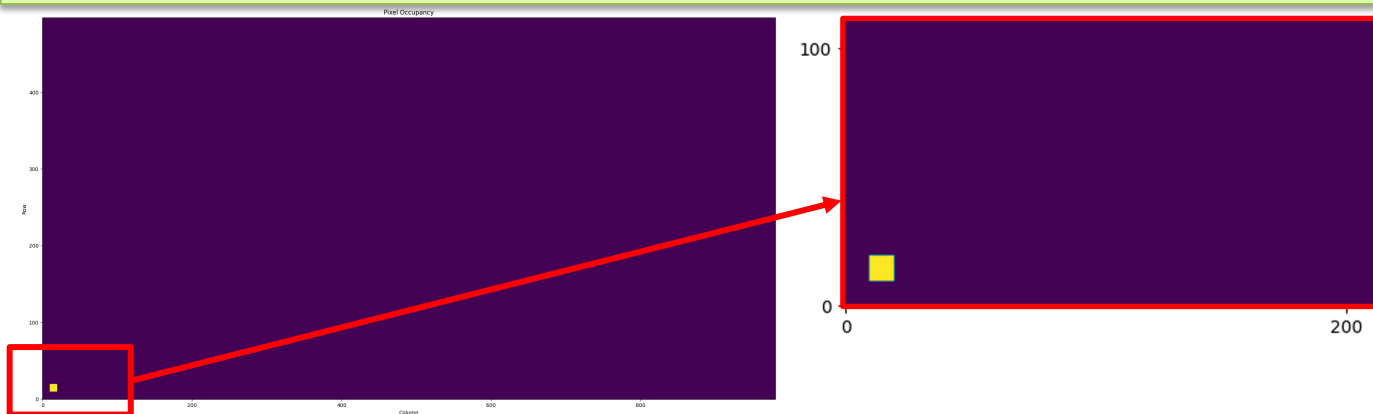
Serial Data Output Frame @ 1.2Gbps



Serial Data Eye Diagram @ 1.2Gbps



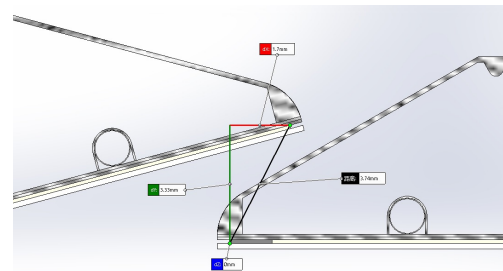
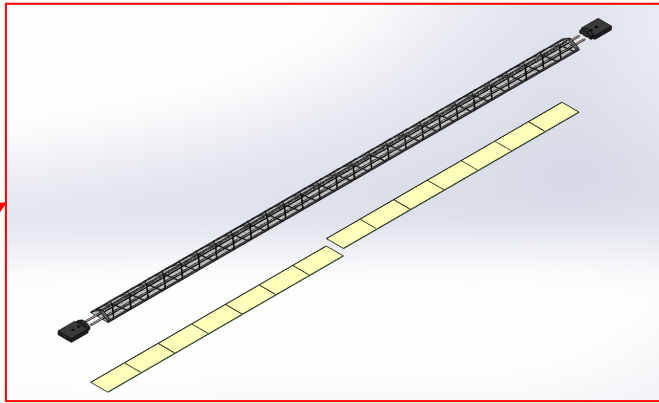
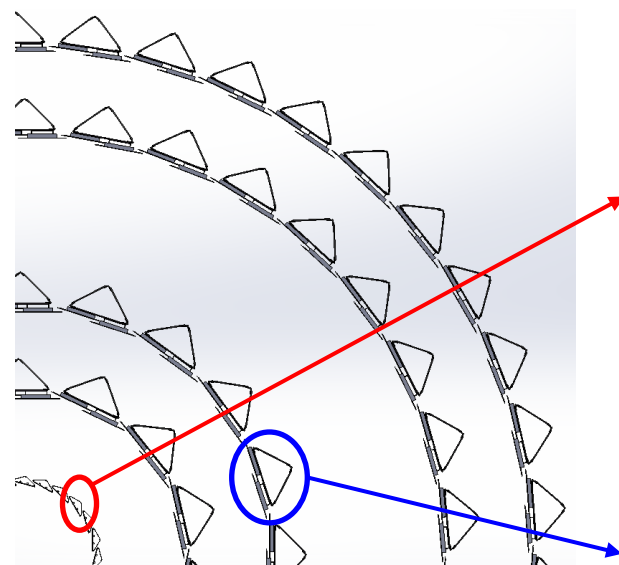
Array readout test using Dpulse excitation of 10×10 pixels.



Positive results:

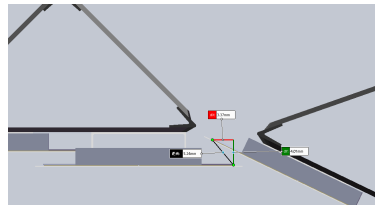
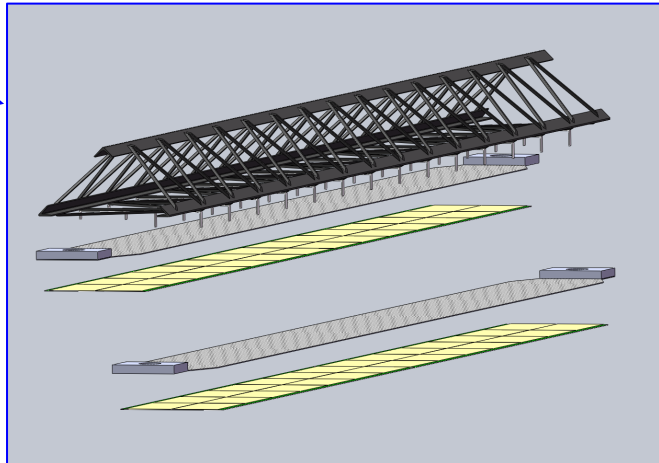
- Serializer ✓
- Frame Builder and 8b10B Encoder ✓
- Pixel Configuration Module ✓
- AERD for Pixel Array Readout ✓

✓ 桶部stave模块结构设计:



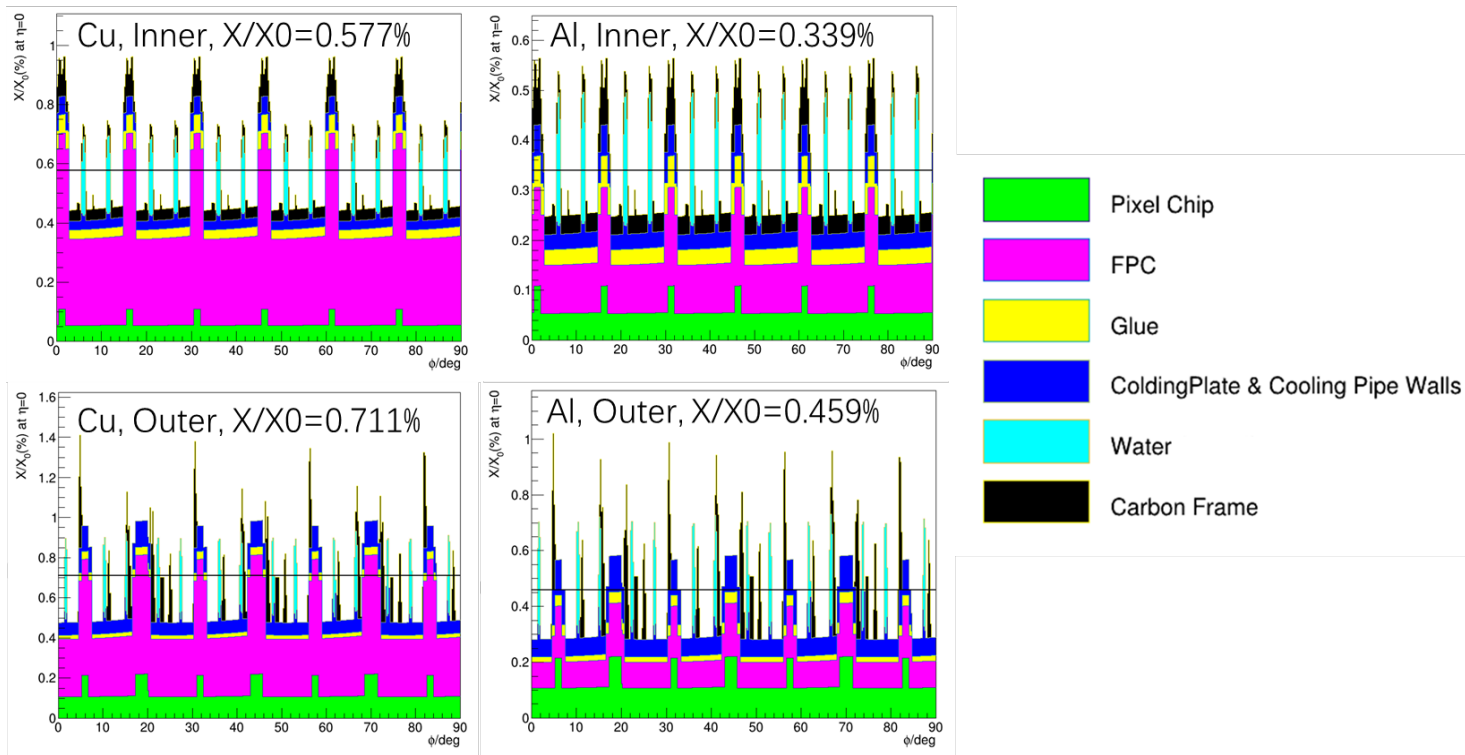
最内层stave模块: 每个stave由2个芯片级模块(HIC)拼接而成。每个HIC由1×7枚MIC6芯片与FPC拼接而成，HIC上的**所有芯片均工作在主模式**

Layer No.	R (cm)	Nr. Of Staves
L0	5.0	24
L1	11.0	14
L2	17.0	20
L3	29.0	34
L4	35.0	42



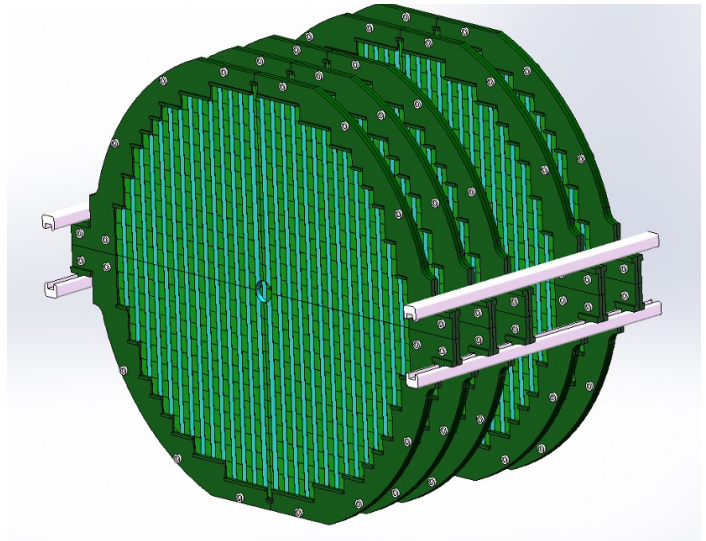
外四层stave模块:每个stave由2个 half-stave组成，每个half-stave由2个芯片级模块(HIC)拼接而成。每个HIC由2×7枚MIC6芯片与FPC拼接而成，HIC上2枚芯片工作在主模式，其余在从模式

- ✓ 基于Geant4 + DD4Hep模拟了两种不同选材（铜质与铝质）的FPC的物质质量分布
- ✓ 最内层和外四层FPC分别铝质和铜质方案。
采用铝质FPC可降低质量
- ✓ 当前设计采用水冷方案。下一步将基于MIC6实际功耗水平，继续优化stave机械结构设计，
探究进一步减小质量方案

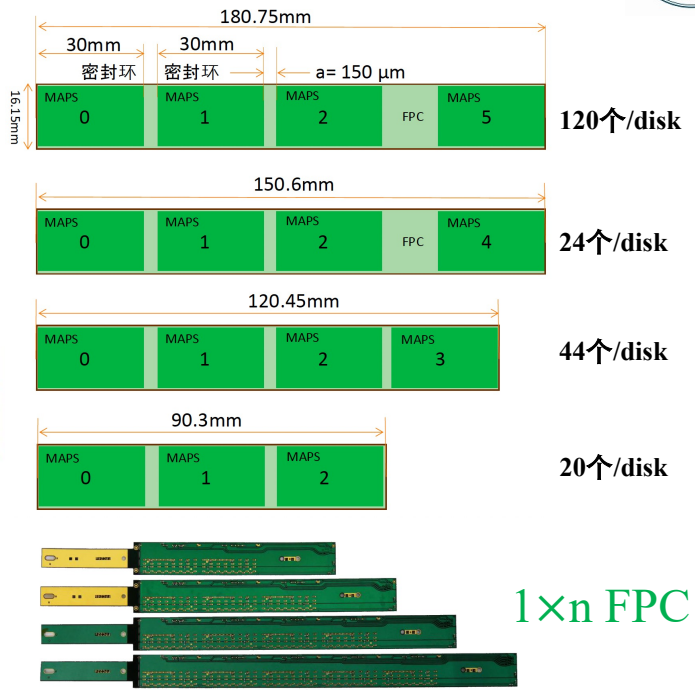
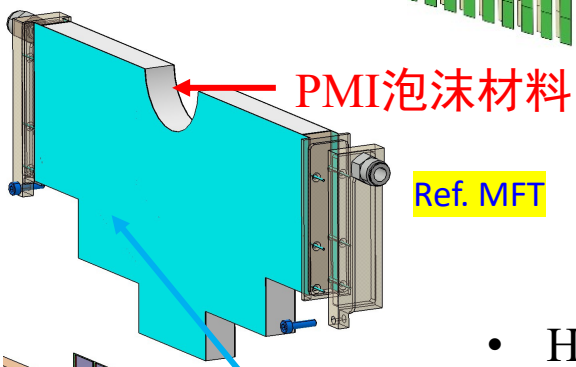
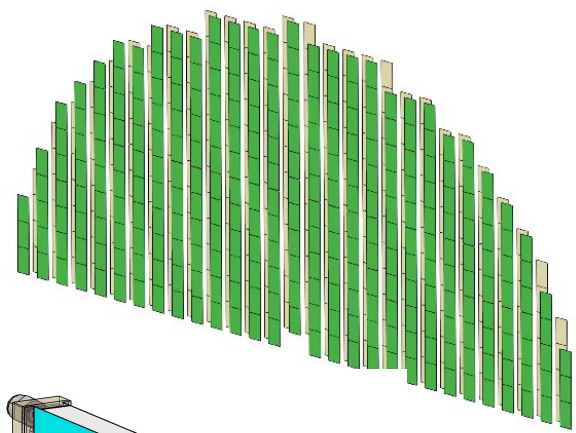


Al/Cu两种FPC选材下，内层和外层的单层物质质量沿 Φ 方向分布（ $\eta=0$ ）

✓ 端部disk模块结构设计:

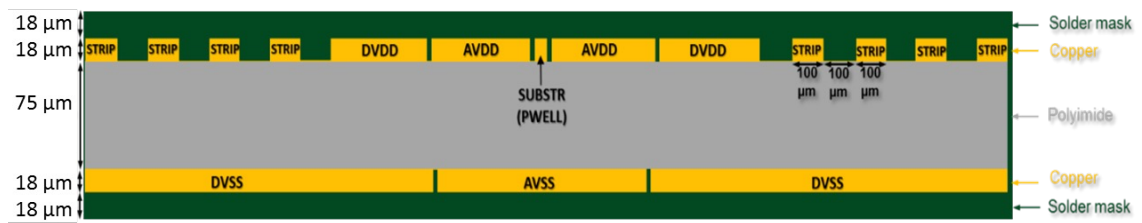
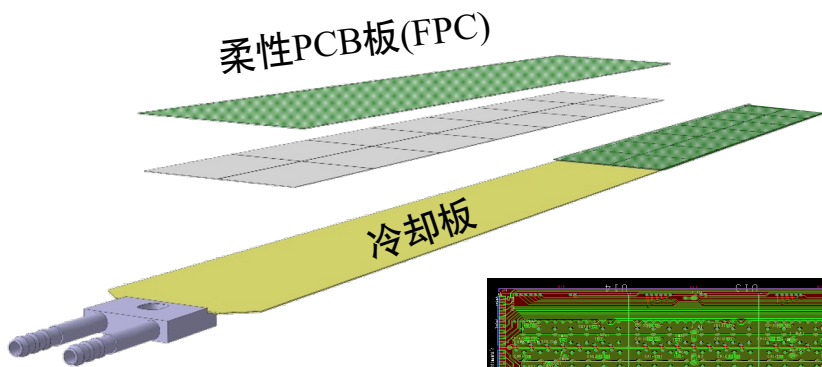


Layer No.	Nr. of ladders	ladder overlap (mm)
D0	114	2.0
D1	114	2.0
D2	114	2.0
D3	114	2.0
D4	114	2.0

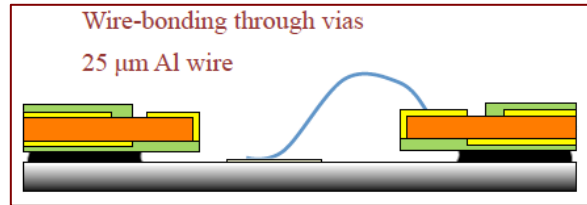
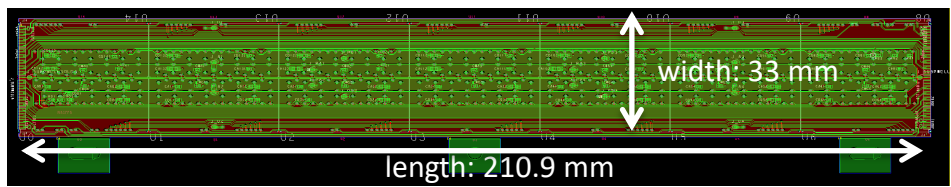


- Heat exchanger material, $\sim 0.26\%$ X/X₀
- Ladder material (50 μ m chip + Al/Cu-FPC): $\sim 0.17\%$ ($\sim 0.41\%$) X/X₀
- 半圆盘边缘转接板实现disk模块的信号传输和与机械支撑固结

课题研究进展 – FPC设计与样机试制



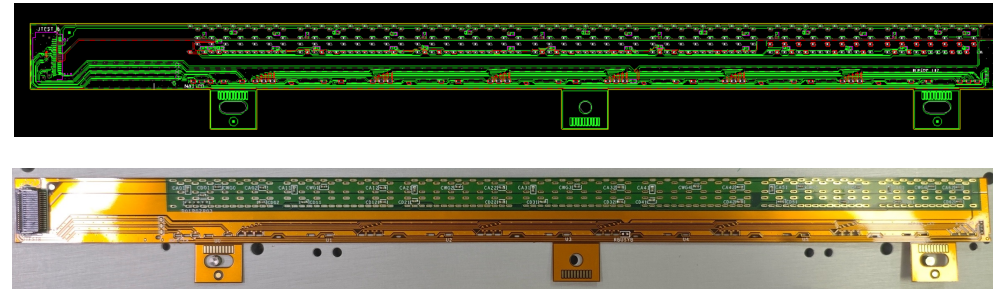
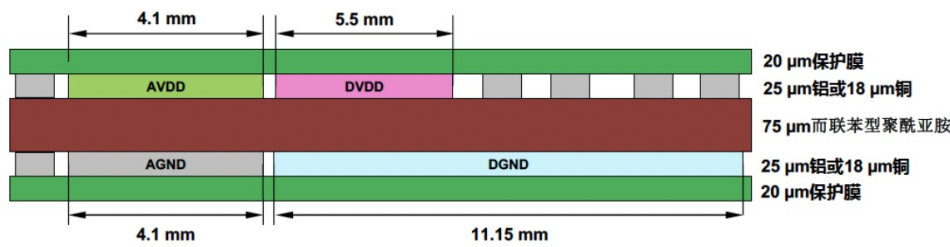
外四层模块的FPC设计



- **低物质量** (铜基FPC可在国内制备; 铝基FPC需找国内厂商联合攻关, 或与CERN联合研制)
 - ✓ Standard Cu or Al can be accepted. A thickness of 75 μm has been adopted for the polyimide layer
- **低压降和高品质信号传输** (需基于MIC6-V4芯片的实际性能优化设计)
 - ✓ The thickness of each Cu layer is 18 μm or Al layer of 25 μm, a value which allows both minimising the voltage drop, and ensuring a differential impedance of 100 Ω in the signal lines
- **工艺精度**
 - ✓ Position tolerance of $\pm 40 \mu\text{m}$ is required to align vias on interconnection pads by overlapping the FPC on the pixel chips

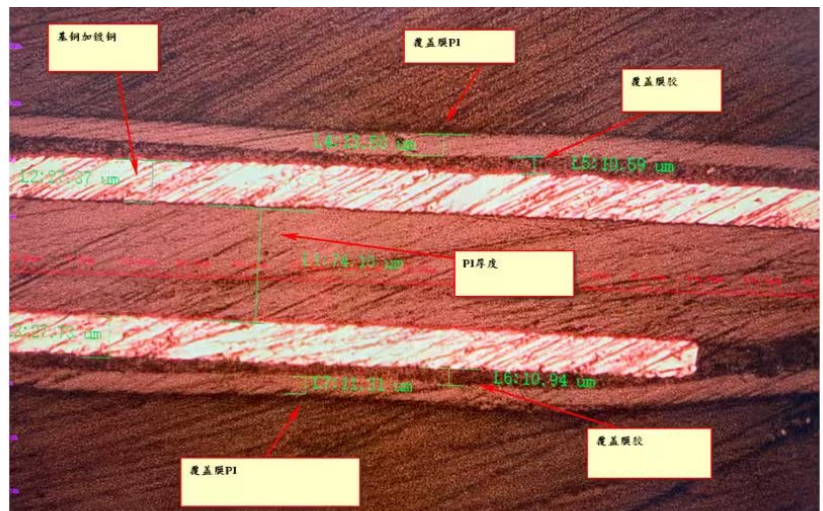
课题研究进展 – FPC设计与样机试制

- ✓ 完成了柔性PCB板（FPC）的设计，在国内完成铜质FPC研制（聚酰亚胺膜75微米厚，双铜层18微米/层，双覆盖膜层18微米/层）



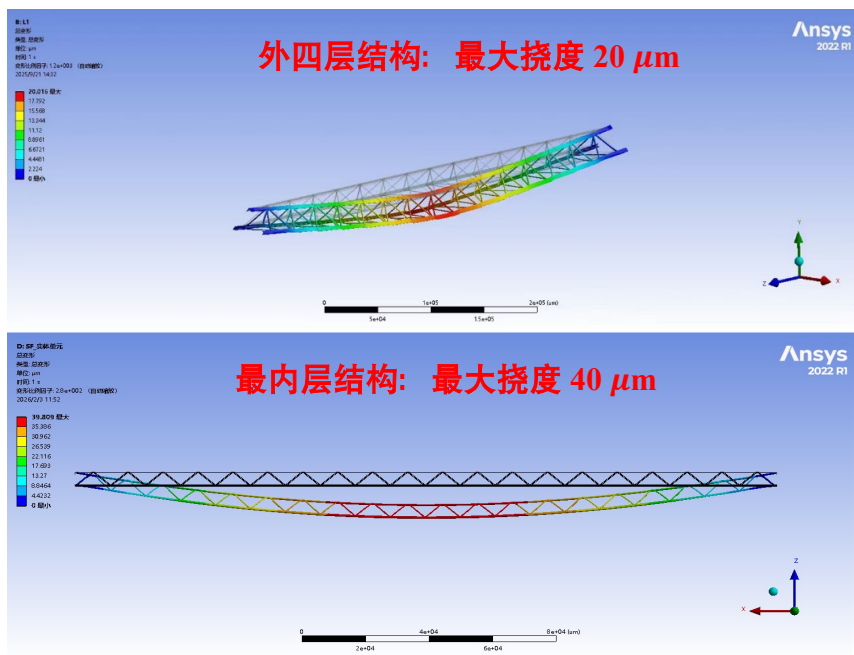
最内层模块的FPC设计

叠层设计					
层	材料名称	FPC	FPC	FPC	单位
	Coverlay PI	12.5	12.5	12.5	μm
	Coverlay AD	15	15	15	μm
Top	Base copper+plating	22	22	22	μm
	Polyimide	75	75	75	μm
Bot	Base copper+plating	22	22	22	μm
	Coverlay AD	15	15	15	μm
	Coverlay PI	12.5	12.5	12.5	μm
	设计厚度	174	174	174	μm
FPC厚度要求mm		0.17	厚度公差mm	±0.05	

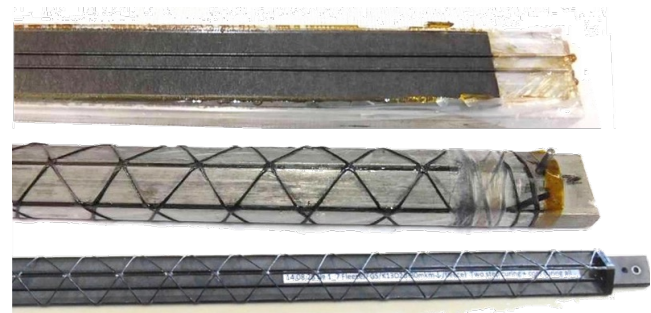
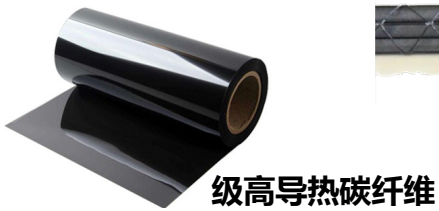
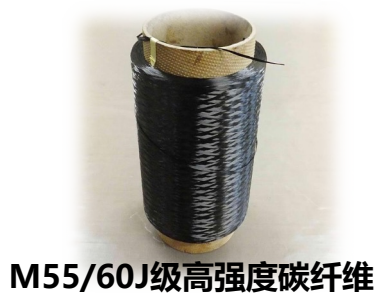
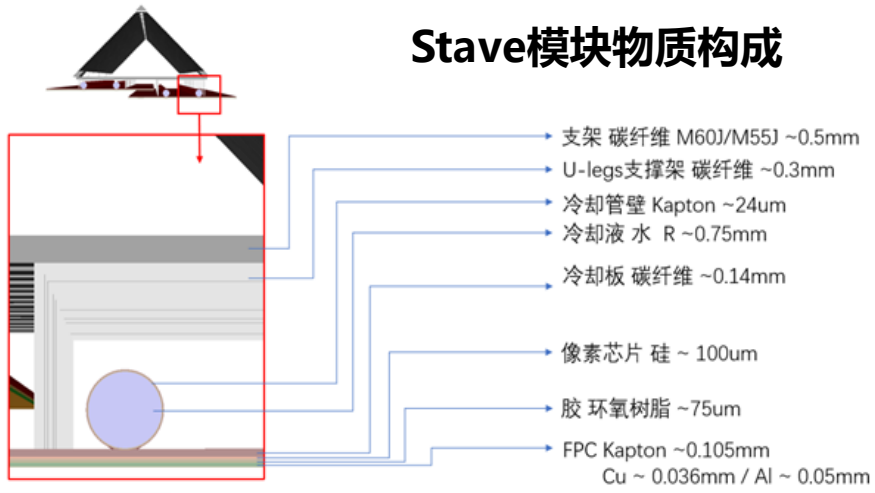


课题研究进展 – 碳纤维机械结构设计与样机研制

- ✓ 完成机械性能模拟和物理仿真模拟
- ✓ 基于选材和结构进行了FEA仿真，验证了当前设计的机械性能
- ✓ 针对stave需要的碳纤维材料与工艺进行了调研，与国内科研单位开展联合研制

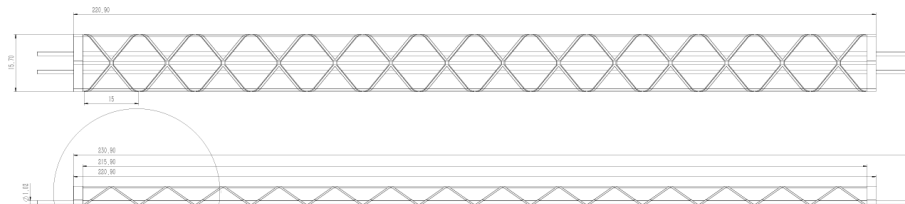
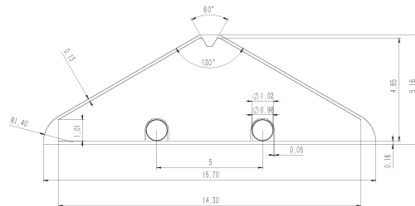
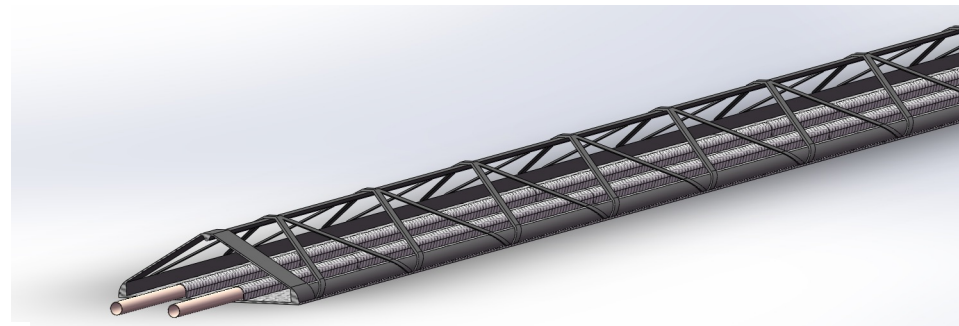
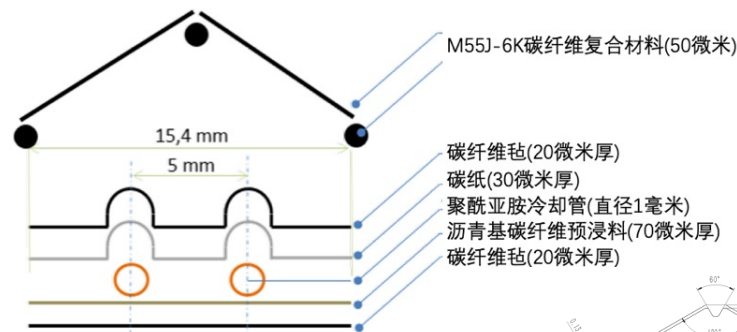


Stave模块物质构成

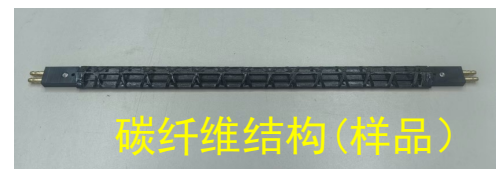
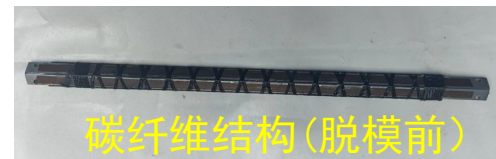
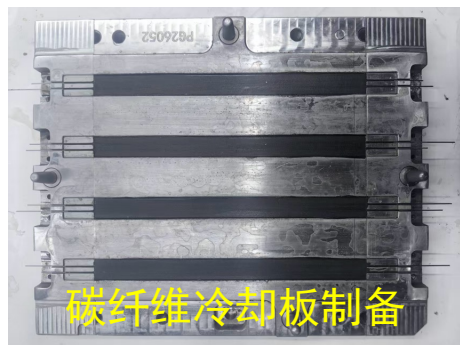


碳纤维预浸料缠绕固化工序示意图

- ✓ 完成了stave模块的碳纤维机械结构（支架和冷却板）的设计与优化，目前在国内完成了样机制作

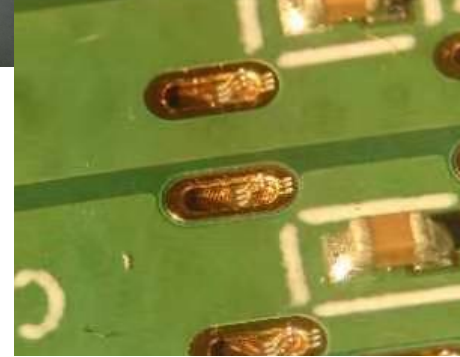
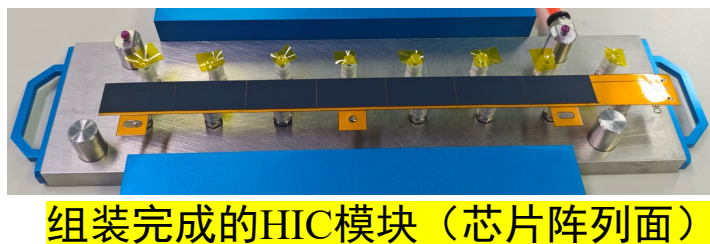
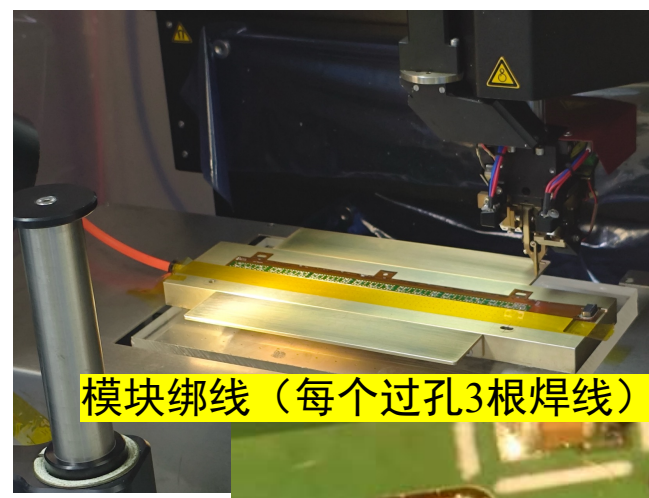
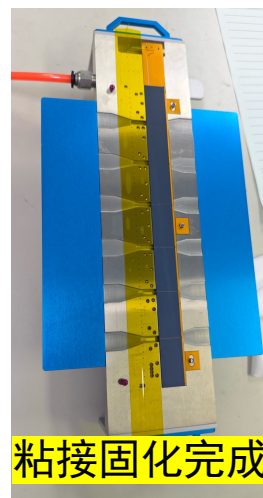
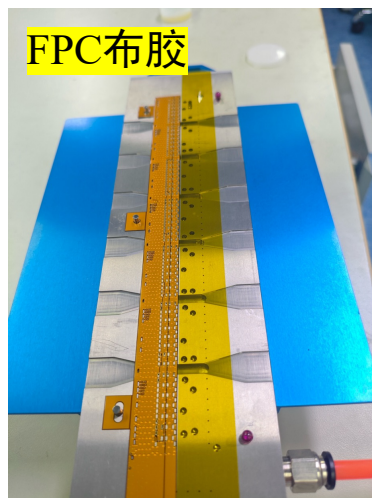
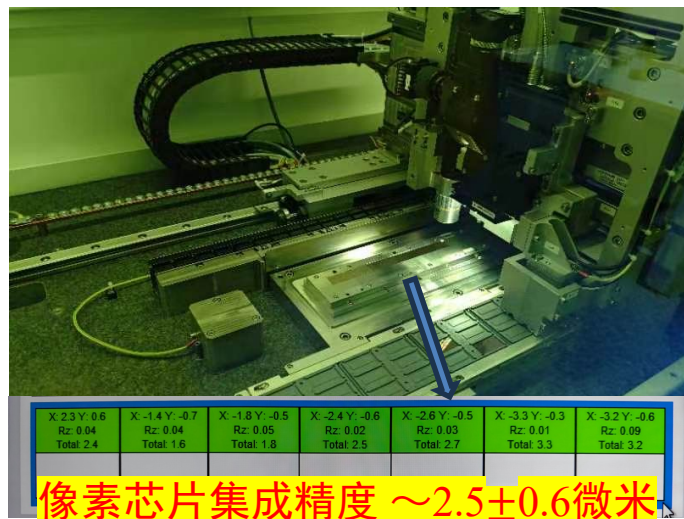


碳纤维结构工程设计图

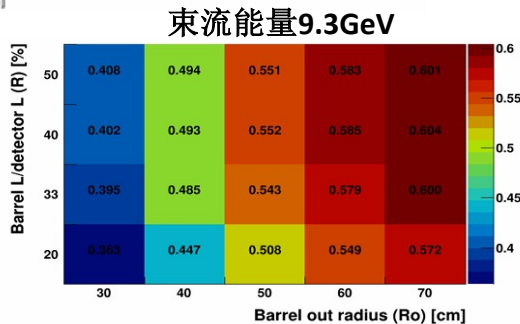
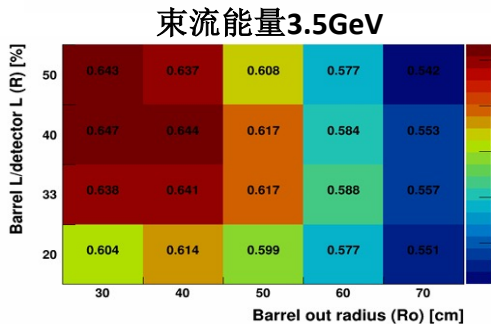
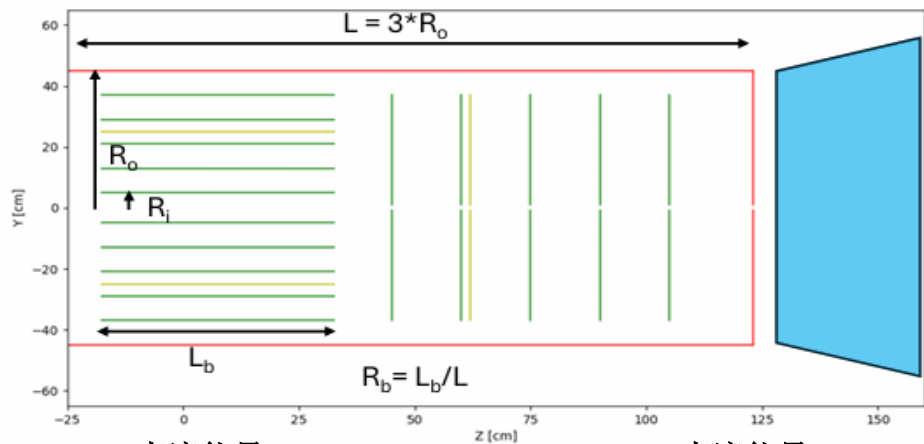


课题研究进展 – HIC模块集成方案

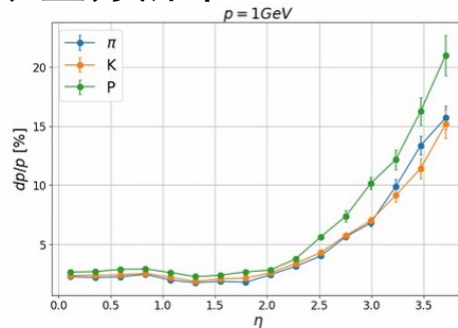
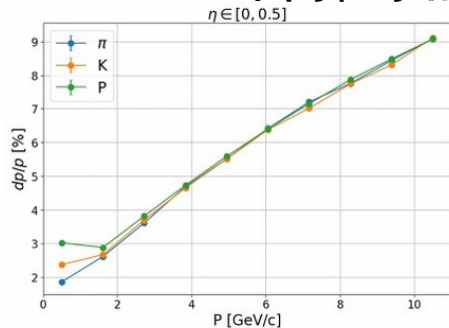
- ✓ 制定了HIC模块组装与测试的技术方案，用于HIC模块组装与测试平台已就位
- ✓ 利用MAPS样片成功组装了HIC 模块样机，**芯片集成精度好于5微米**



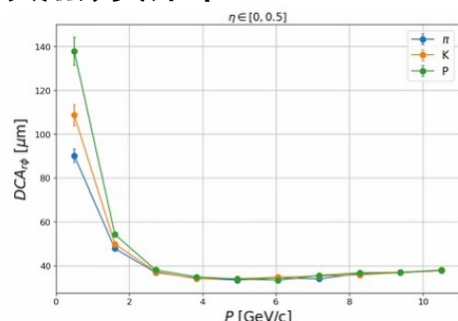
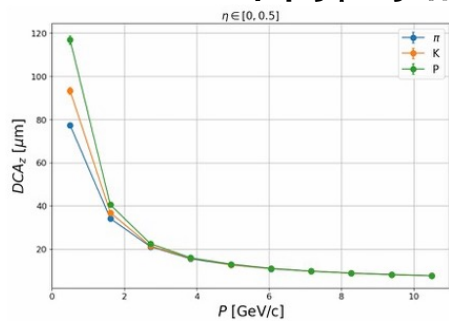
- ✓ 模拟了MAPS像素探测器系统在不同几何参数下的表现以优化关键性能参数
- ✓ 考虑两个参数：桶外半径 R_0 ，Z方向桶部占比 $R_b = L_b/L$
- ✓ 模拟了3.5和9.3 GeV能量下质子碰撞中 Λ 超子的探测效率： $R_0=50\text{ cm}$, $R_b=0.33$



不同粒子的动量分辨率

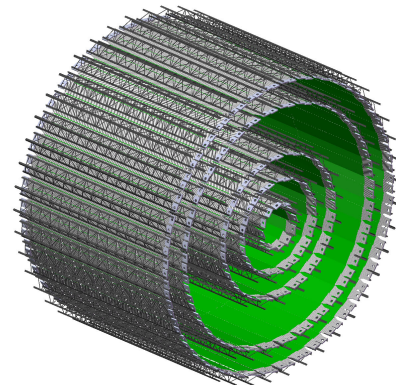
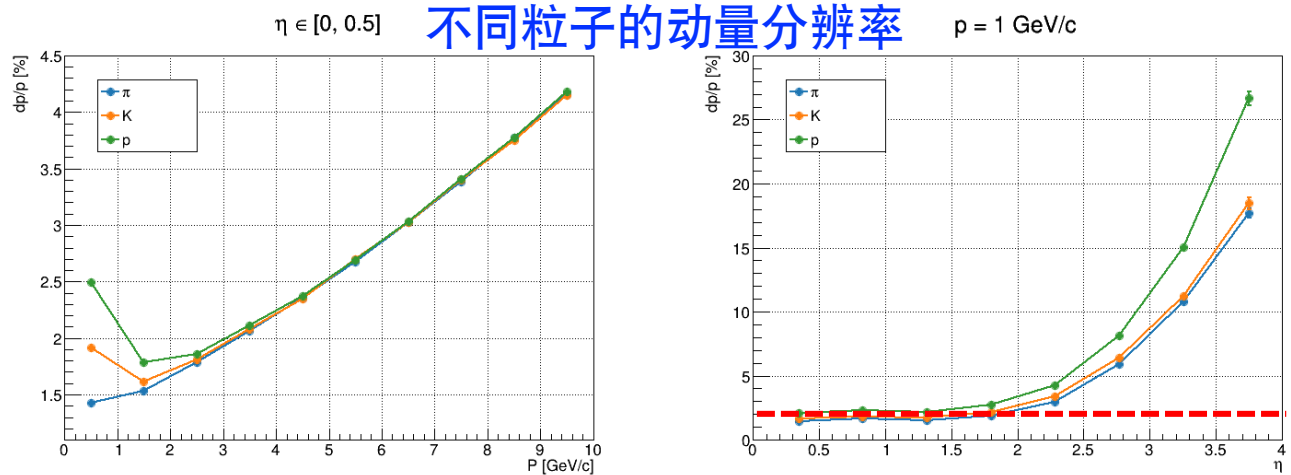


不同粒子的顶点分辨率



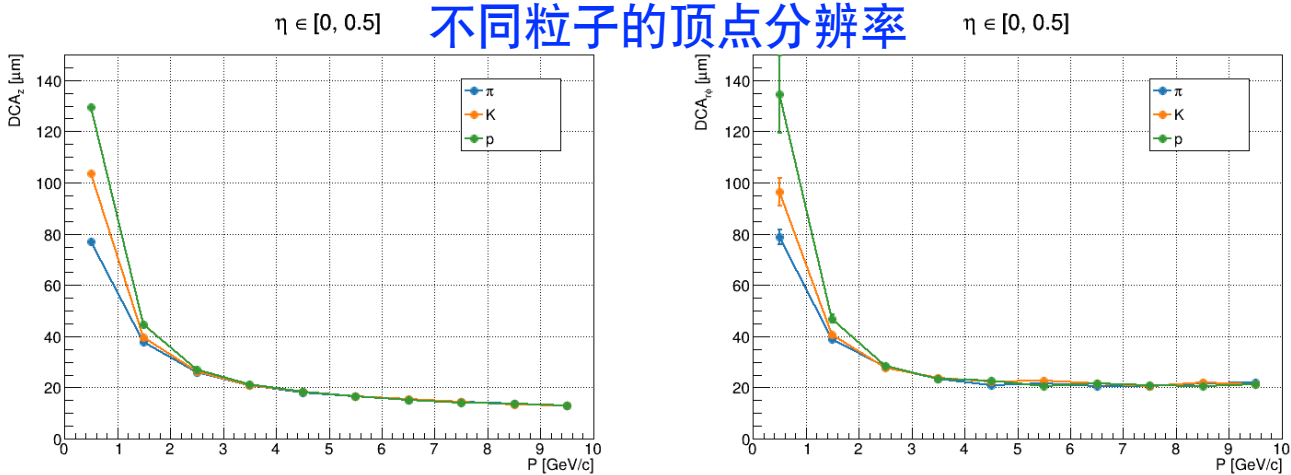


不同粒子的动量分辨率

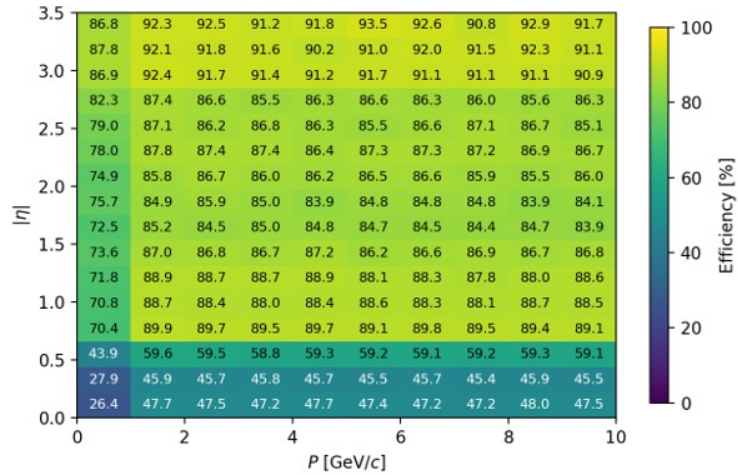


考虑桶部stave模
块真实的几何结
构和质量

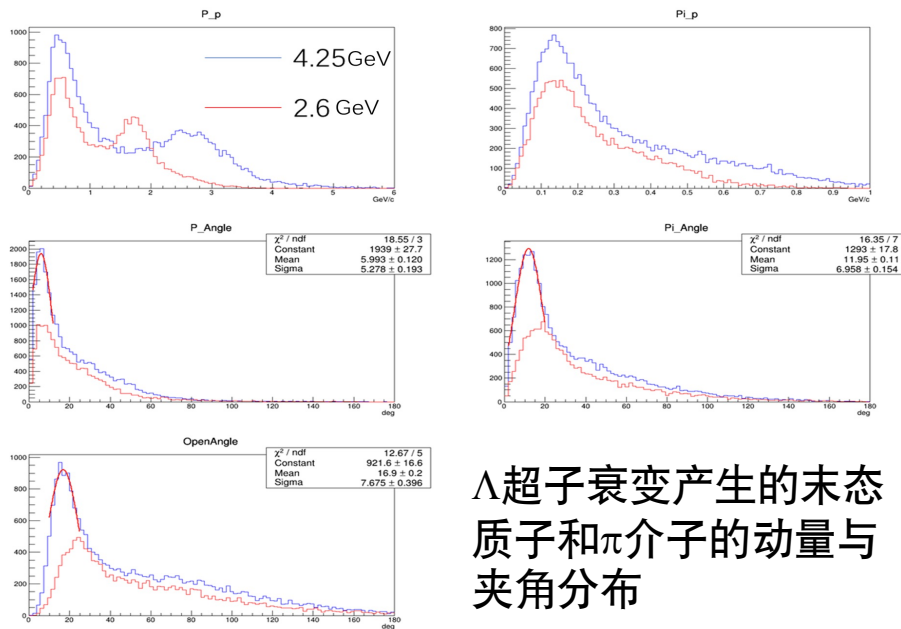
不同粒子的顶点分辨率



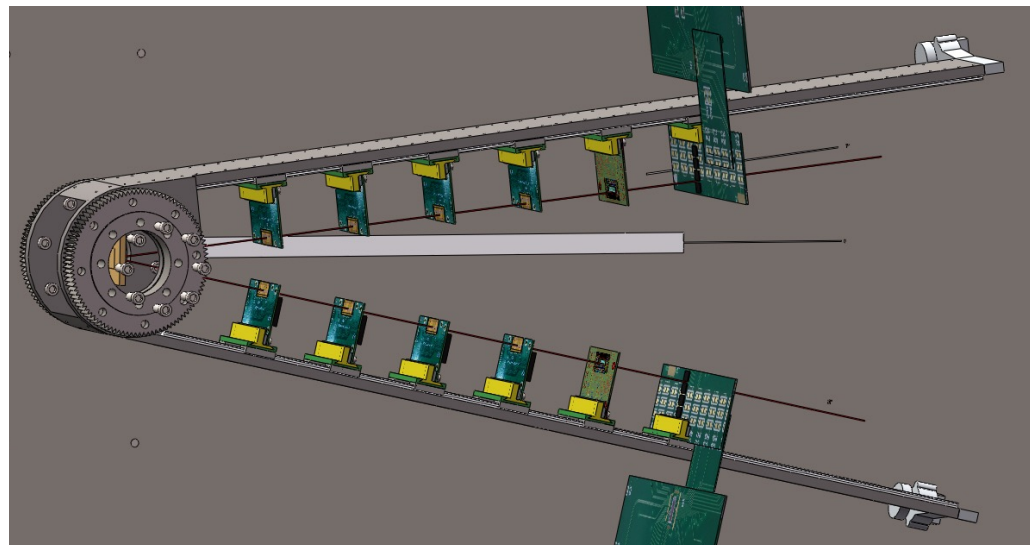
探测效率(GenFit in HnsRoot)



- ✓ 为了验证包含MAPS径迹探测器在内的H-NS径迹探测系统的各个关键探测器技术可行性, 设计了其原理样机H-NS0
- ✓ H-NS0将在HIAF上使用束流能量2.6 GeV氧束+碳靶进行实验, 验证MAPS系统和LGAD系统正常运行并尝试重建 Λ 超子
- ✓ H-NS0成两臂结构, 每支臂上安装5层MAPS芯片和一层LGAD芯片。每层MAPS探测器仅包含一枚芯片, 而每层LGAD探测器则由12枚芯片构成

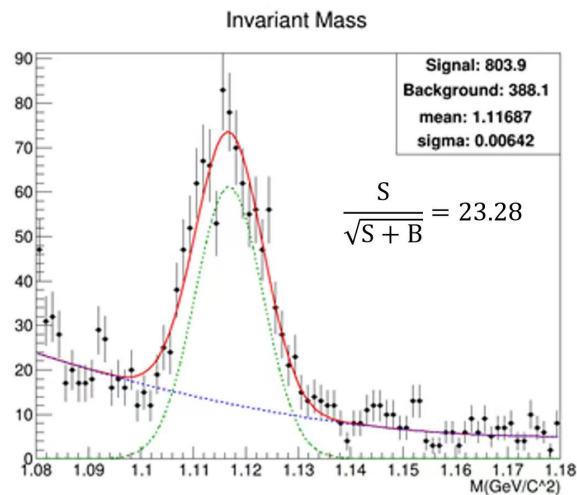


Λ 超子衰变产生的末态
质子和 π 介子的动量与
夹角分布

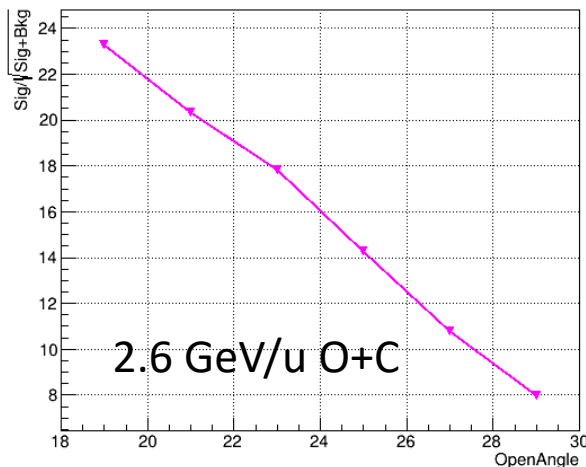


H-NS0结构设计图, 两臂张角为 $(7^\circ+12^\circ)$

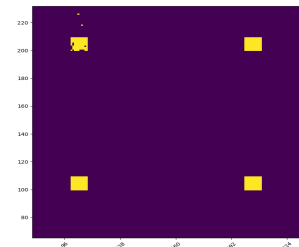
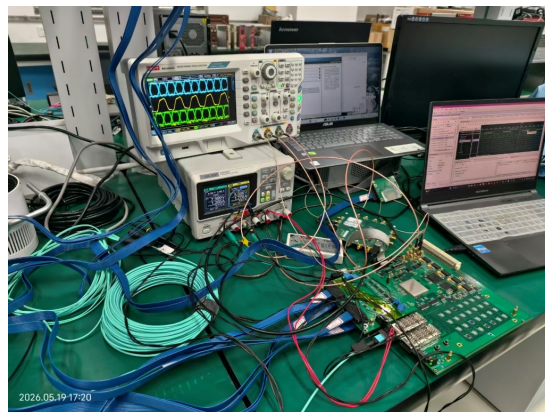
- ✓ 准备了11套MIC6-V3载板（镂空窗设计），其中9套在电学和alpha放射源测试中工作正常
- ✓ 利用DAQ系统完成H-NS0一条支臂上四套MIC6载板的读出测试，读出链路工作正常
- ✓ 基于H-NS0原型机真实几何，开展支臂张角优化和重建性能分析
- ✓ 根据模拟估计，H-NS0重建出10000个 Λ 超子信号，2.6 GeV/u下需要三周末流时间，4.25 GeV/u下需要两周束流时间（未考虑上游T0和触发探测器造成的背景）



19°张角下重建的 Λ 不变质量谱



不同双臂张角下 Λ 信号显著度



总结与展望

- 按课题任务书的年度计划，已完成：
 1. H-NS/MAPS像素探测器单模块的结构设计，FEA仿真与物质质量模拟结果达到初步要求。
 2. MAPS探测器整系统的几何结构初步设计，确定了合适的几何参数，并通过模拟检测了其各个物理性能参数。
 3. MIC6-V4芯片流片，已开始芯片表征测试，各功能模块工作正常。
 4. 根据设计试制了FPC测试样机和碳纤维机械结构样机，组装了HIC模块样机
 5. H-NS0原理样机的设计和模拟，制作了11套MIC6-V3芯片载板，具备开展束流实验条件

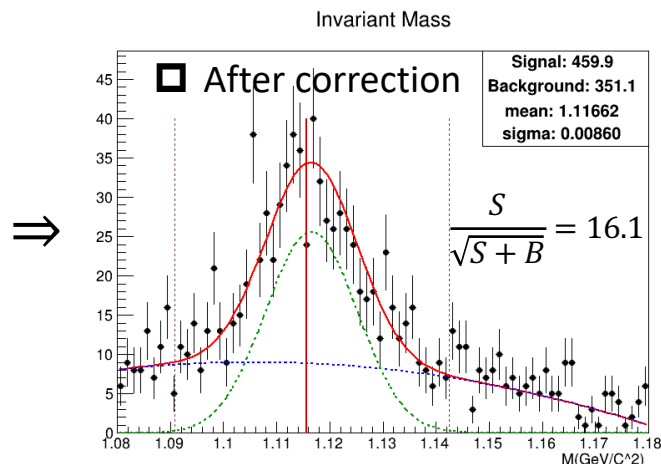
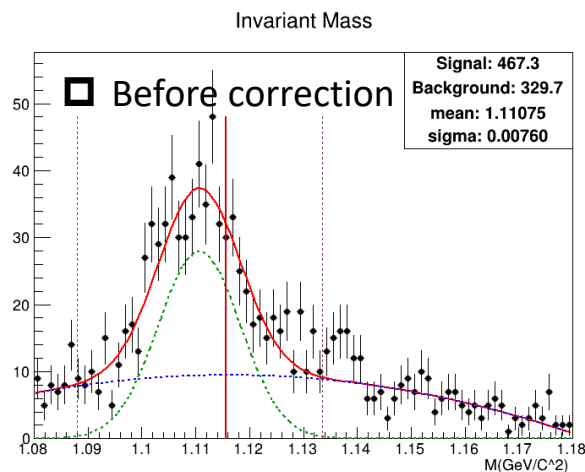
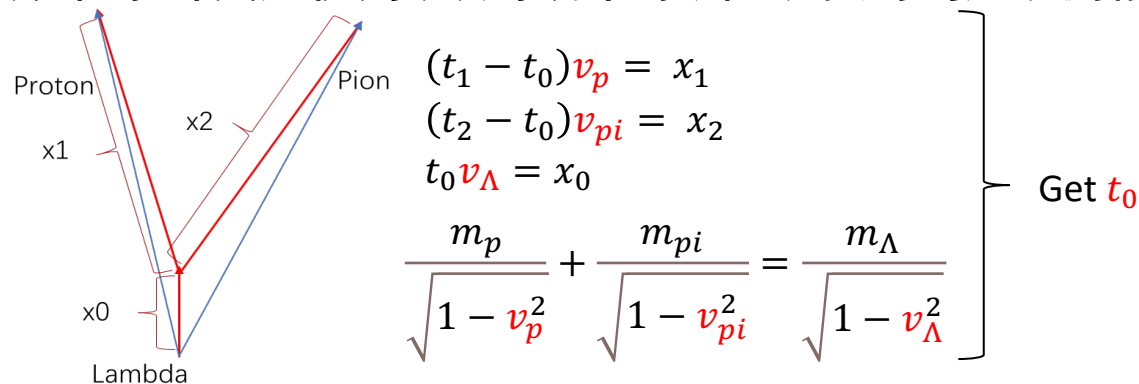
下一步，按课题任务书的年度计划执行。本年度将开展：

1. 将根据实验要求进一步完善模块结构设计，优化物质量。
2. 开展MIC6-V4芯片的放射源测试和束流测试。
3. 利用MIC6-V4样片、FPC样机和碳纤维机械结构样机，完善HIC模块组装技术方案，制作HIC模块样机；开展后端MicroTCA模块。
4. 完成H-NS0样机的MIC6探测模块的集成，参与2026年末流测试。

谢谢大家！

课题研究进展 – H-NS原理样机(H-NS0)

- ✓ 基于次级顶点拟合+数值求解有效修正了重建过程中 Λ 不变质量谱峰偏小的问题。
- ✓ 假设粒子种类, 使用动力学方程求解 Λ 衰变时间, 从而修正p-pi重建动量。



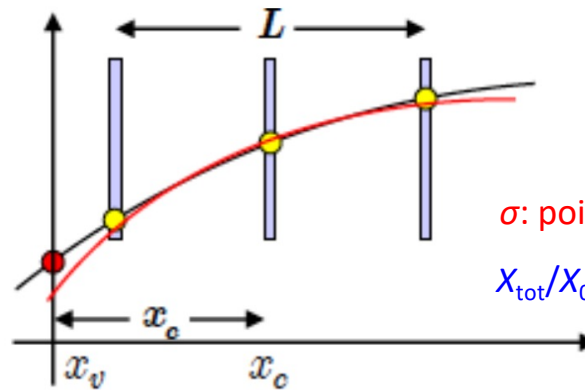
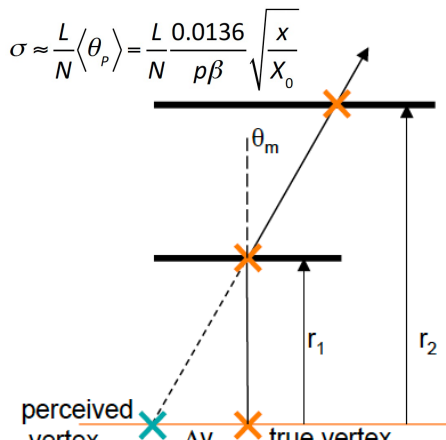
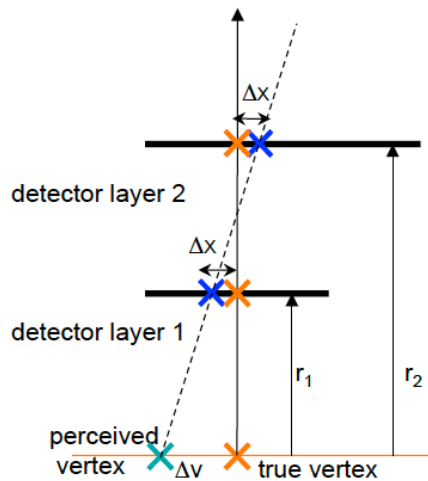
背景介绍 – Why We Need Pixel Tracker in HIC

像素探测器的性能参数：

1. 碰撞参数分辨率
2. 动量分辨率
3. 寻迹效率



- 物质质量
- 固有位置分辨率
- 到碰撞点的距离



σ : pointing resolution/plane

X_{tot}/X_0 : total material budget

Ref.: R.L. Gluckstern, NIMA 24 (1963), 381-389

$$\frac{\Delta p_t}{p_t} = \frac{\sigma[m] p[\text{GeV}/c]}{0.3 B[T] L^2[m^2]} \sqrt{\frac{720 (N-1)^3}{(N-2) N (N+1) (N+2)}}$$

$$\approx \frac{\sigma[m] p[\text{GeV}/c]}{0.3 B[T] L^2[m^2]} \sqrt{\frac{720}{N+4}}$$

$$\frac{\Delta p_t}{p_t} = \frac{0.0136}{0.3 \beta R[T] L[m]} \sqrt{\frac{X_{tot}}{X_0}} \sqrt{\frac{10}{7} \frac{12 + (N-1)N^2(N+1)}{(N-2)N(N+1)(N+2)}}$$

基于CMOS像素传感器技术的径迹探测器具备**高分辨率、低物质**
量、抗辐照、集成度高等优势！