粒子物理实验像素型探测器读出到H-NS电子学

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MODERN PHYSICS DEPARTMENT

Content

- Background
- Front end ASICs for pixelated detectors
- Readout system for pixelated detectors
- Our work on readout electronics
- Our work on DAQ and control system
- Conclusion

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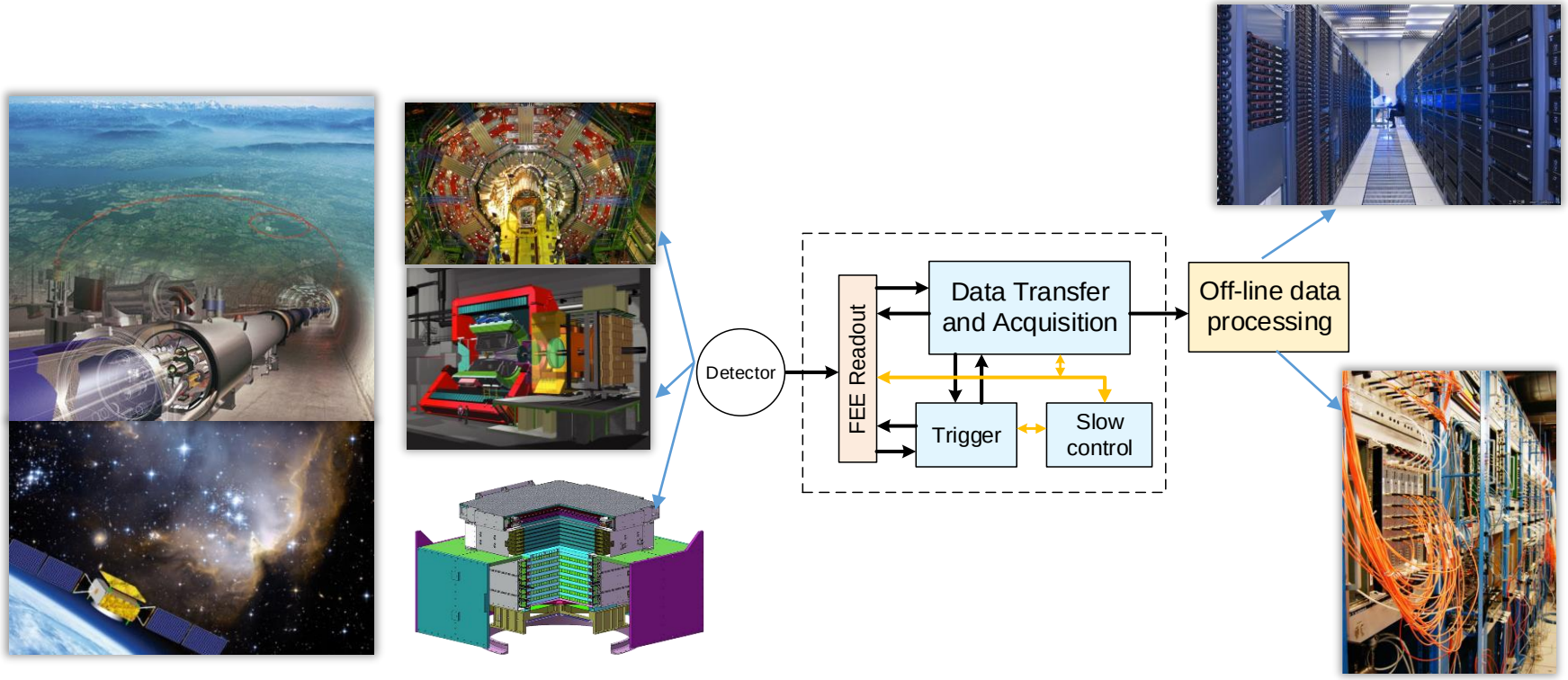
Readout electronics in particle physics experiments

- In large-scale particle physics experiment facilities, electronics are key parts.



- The information obtained from the detectors (sensors) has to be manipulated, processed, and transferred by the electronics before being used by the computer farms.

Tasks of readout electronics

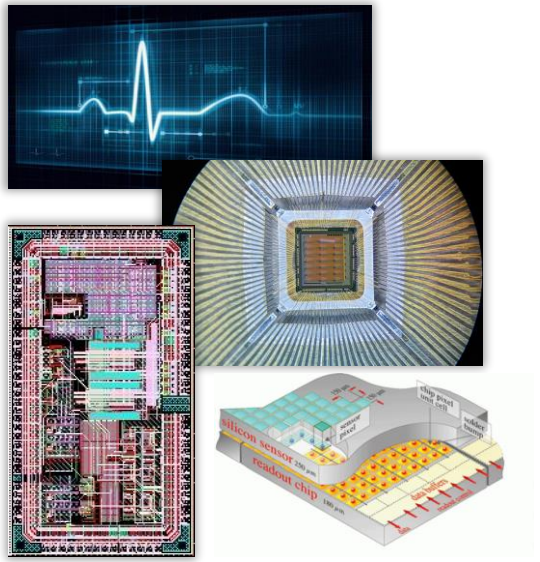
❖ New challenges appear for electronics with the development of particle physics experiments:

- ◇ Faster signal processing
  - ◇ ns → sub-ns
- ◇ Higher measurement accuracy
  - ◇ ps Time、sub-fC Charge
- ◇ Larger number of channels
  - ◇ Tens of thousands -> millions or more channels
- ◇ High-speed real-time data processing and transmission

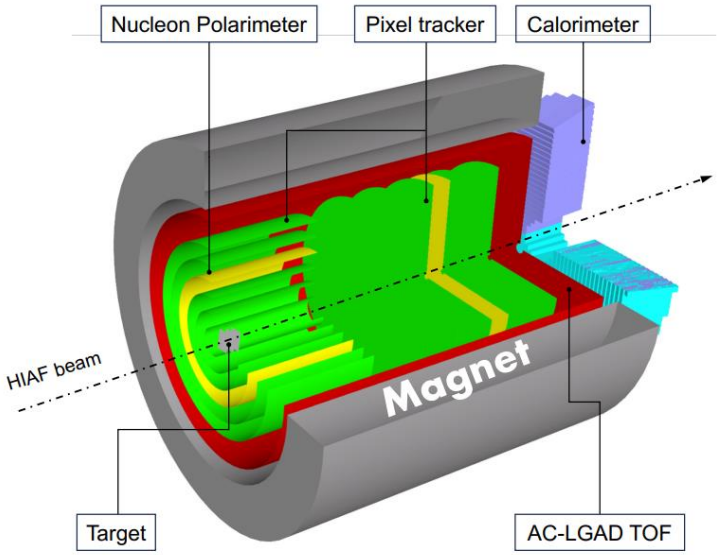
■ Electronics from other fields can not meet the requirements

■ Necessary to study key techniques

- ◇ Higher Speed
- ◇ Higher Accuracy
- ◇ Higher Integration
- ◇ Low Power
- ◇ Radiation Tolerance



H-NS Structure



系统组成：

- **Pixel tracker**
- **LGAD TOF**
- Target
- Nucleon Polarimeter
- Calorimeter
- **Electronics**
- Magnet
- Beamline
- Mechanics + Engineering

1) Λ (p) polarization, hadron spectra, spin structure, …;
2) High μ_B properties, QCD critical point, …

❖ **Pixelated silicon detectors are key parts in H-NS:**

1) Low material, high spatial resolution tracker -- MAPS (Monolithic Active Pixel Sensor)
2) Large area, high time resolution TOF system -- LGAD (Low-Gain Avalanche Detector)

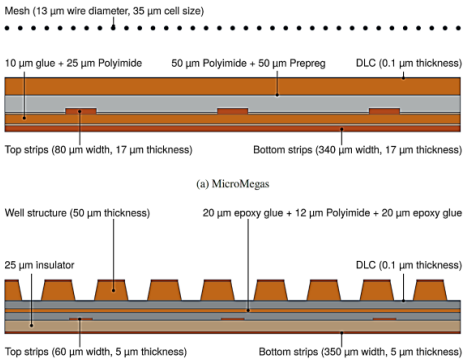
Development of high-granularity detectors

Tracking

Vertex, tracker rebuilding

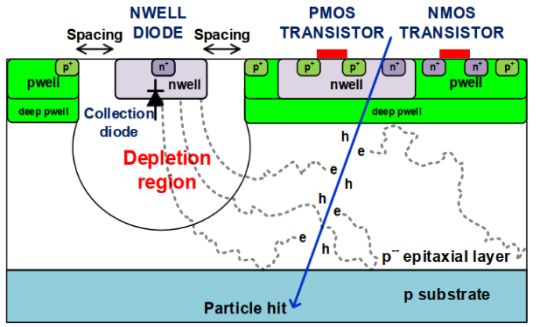
High-precision position measurement

MPGD



Spatial precision: tens of μm

Silicon Pixel Detector



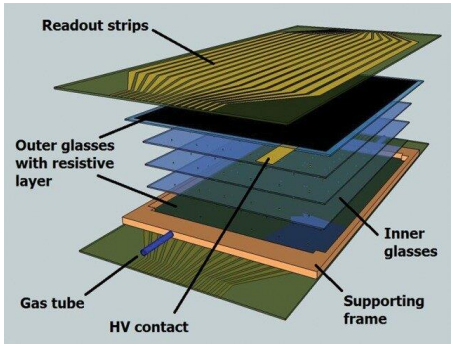
Spatial precision: < 5 μm

Time-of-Flight

Particle Identification

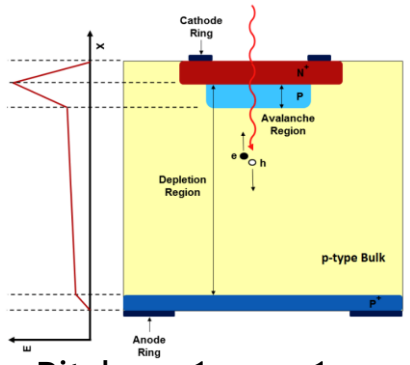
High-precision time measurement

MRPC



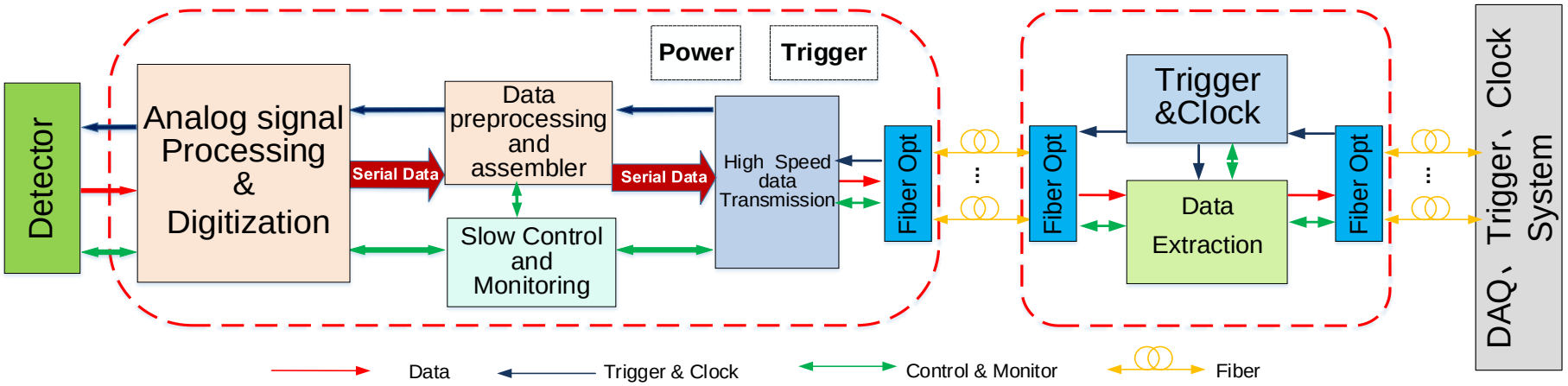
- High time precision

LGAD



- Pitch: ~1mm×1mm
- Position information & high precision time

Readout electronics system



- Data Link: Analog → Digital →Preprocessing → Reformat →Extraction
- Time stamp Link: Clock System → Synchronized Clock → Clock Distribution
- Trigger Link: Multi-Level Trigger →Trigger Information Dec & Check

  →Trigger Signal Distribution
- Control Link: Control Information Dec & Check → Control Signal Distribution

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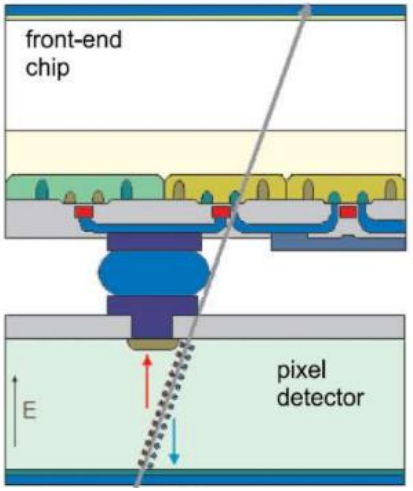
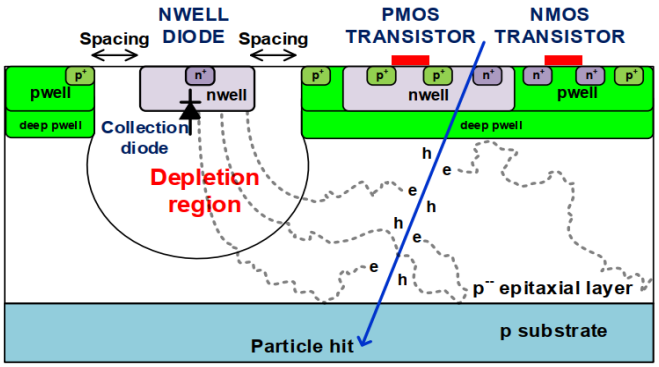
Pixel Detectors

- **Hybrid pixels**
  - Advantages:
    - Sensor and readout circuit can be optimized separately
    - Excellent radiation hardness
    - Fast timing and high rate capability
  - Disadvantages：
    - Relatively large material budget
    - Hybridization: complex, expensive



- **Monolithic active pixel sensors (MAPS)**
  - Advantages:
    - Easier integration, lower cost
    - Potential of low material budget
    - Higher spatial resolution
  - Disadvantages:
    - Smaller signal and longer collection time
    - Radiation tolerance limitation

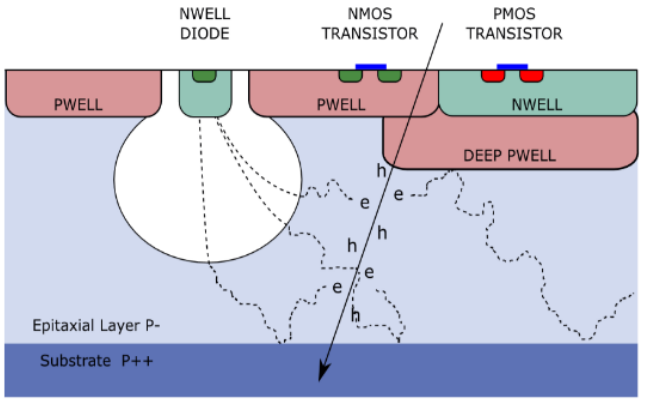


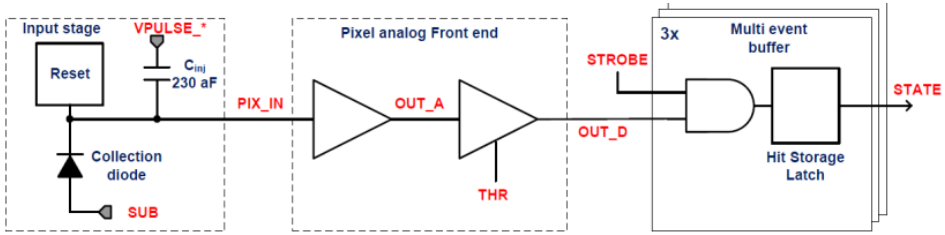
Pixel chips

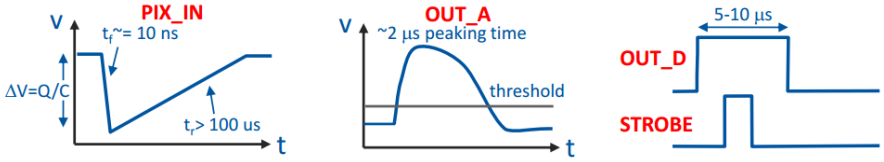
Chip	Process	Array size	Pixel size	Experiment	Type
FEI3	250 nm	18×160	50 ×400 μm^2	ATLAS pixel detector	hybrid
FE-I4	130 nm	80×336	50 ×250 μm^2	ATLAS pixel detector	hybrid
Timepix3	130 nm	256×256	55 ×55 μm^2	GEM-TPCs	hybrid
HEPS-BPIX4	130 nm	20×32	55 ×55 μm^2	HEPS	hybrid
EMPIX	180 nm	32×8	150 ×150 μm^2	/	hybrid
ULTIMATE	350 nm	928×960	20.7 ×20.7 μm^2	RHIC STAR	monolithic
ALPIDE	180 nm	512×1024	28 ×28 μm^2	ALICE ITS	monolithic
ATLASPix3	180 nm	132×372	150 ×50 μm^2	ATLAS pixel detector	monolithic
Mupix10	180 nm	250×256	80 ×80 μm^2	Mu3e	monolithic
TJ-Monopix2	180 nm	512×512	33 ×33 μm^2	ATLAS pixel detector	monolithic
CLICTD	180 nm	16×128	300 ×30 μm^2	CLIC	monolithic
JadePix3	**180 nm**	**512×192**	**16×23.1 μm^2**	**CEPC**	**monolithic**
TaiChuPix-2	**180 nm**	**192×64**	**25×25 μm^2**	**CEPC**	**monolithic**
MIC	**180 nm**	**356×398**	**20×30 μm^2**	**CEPC**	**monolithic**
Topmetal-M2	**130 nm**	**400×512**	**45×45 μm^2**	**/**	**Topmetal+MAPS**
Topmetal-S2/CEE	**130 nm**	**/**	**/**	**0νββ/CEE**	**Topmetal**

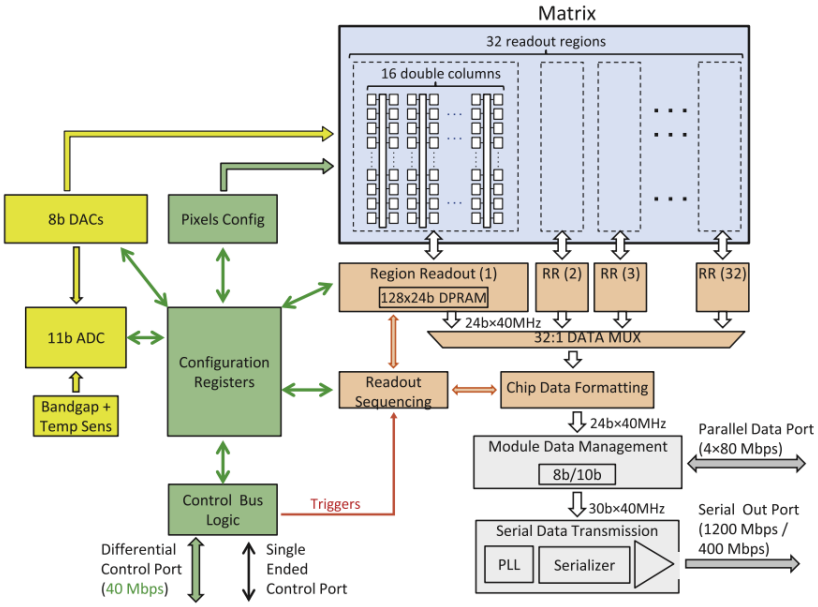
ALPIDE

- MAPS for the ALICE ITS upgrade
  - Process: TJ 180 nm (High resistivity p-type epitaxial layer on a p-type substrate)
  - Array size: 512 × 1024
  - Pixel size: 28 μm × 28 μm
  - Chip size: 15 mm × 30 mm
  - Power: < 40 mW/cm^2

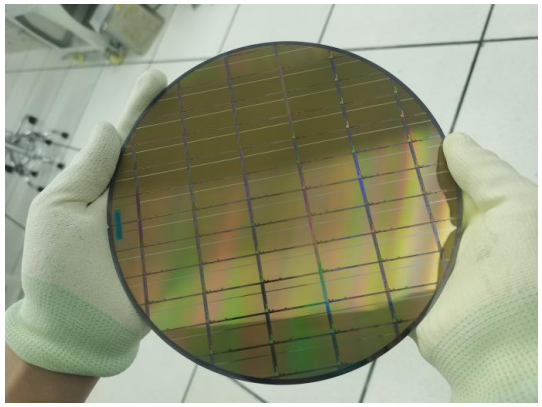




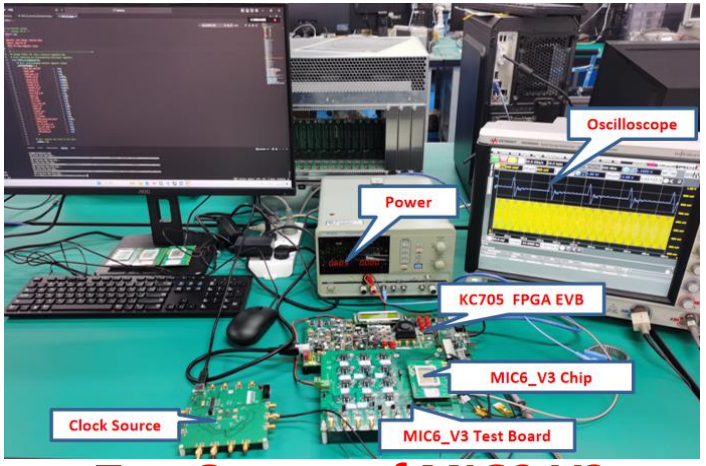




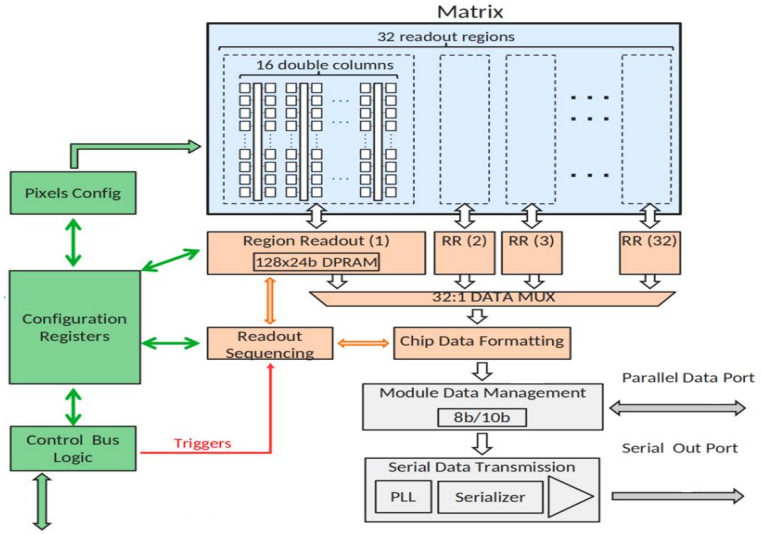
MIC6_V3



MIC6_V3 wafer



Test System of MIC6_V3

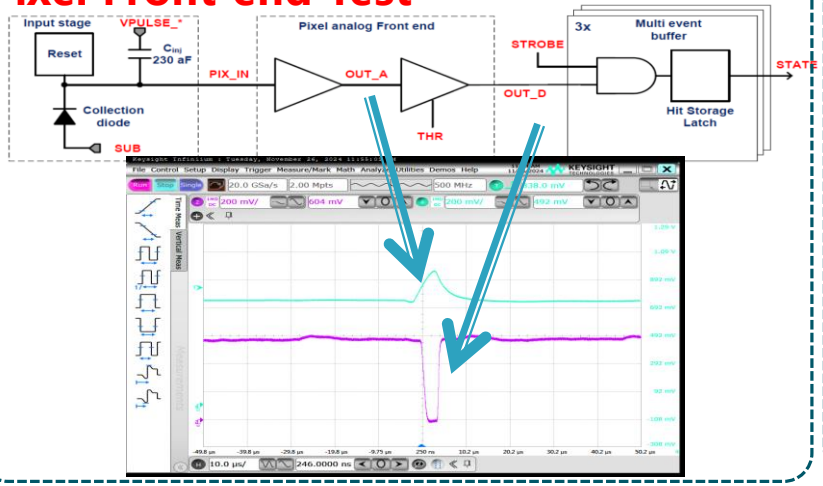


MIC6_V3 block diagram

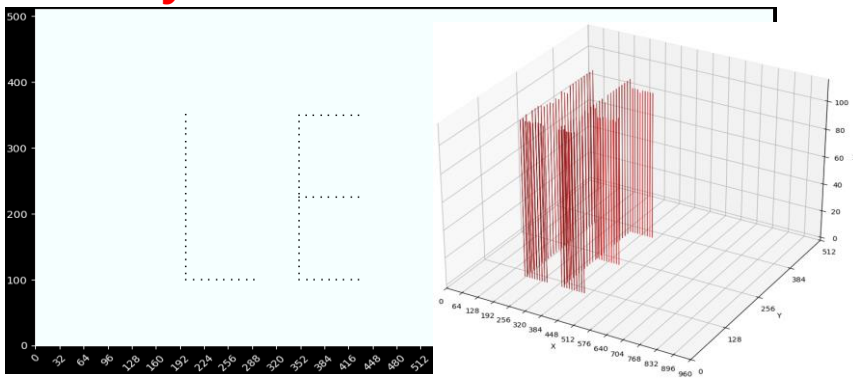
Features	MIC6_V3
Process Technology	GSMC-130 nm
Core Voltage	1.2V
Chip Size	30 mm×15 mm
Pixel Array	980×512
Pixel Size	30.53 um×26.8 um
Zero Suppression Readout	AERD
High-Speed Serial Output	1.1Gbps
Power Consumption	32 mW/cm²

MIC6_V3

Pixel Front-end Test

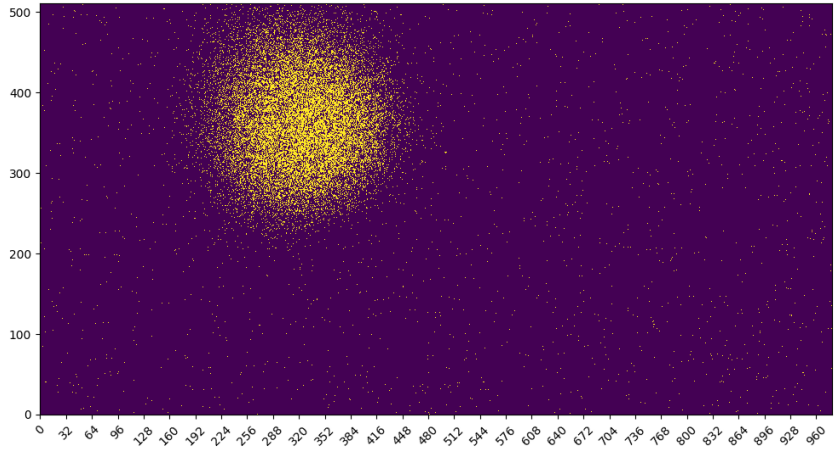


Pixel Array Readout Test

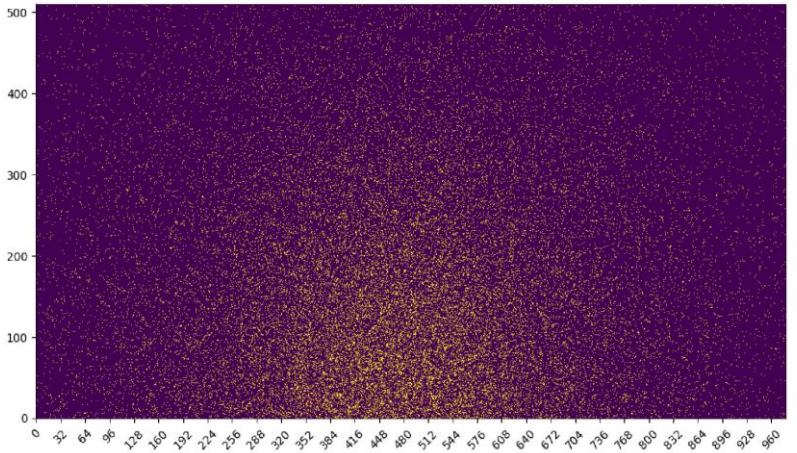


Readout function test with pixel MASK and Apulse/Dpulse

^{241}Am Test using MIC6_V3



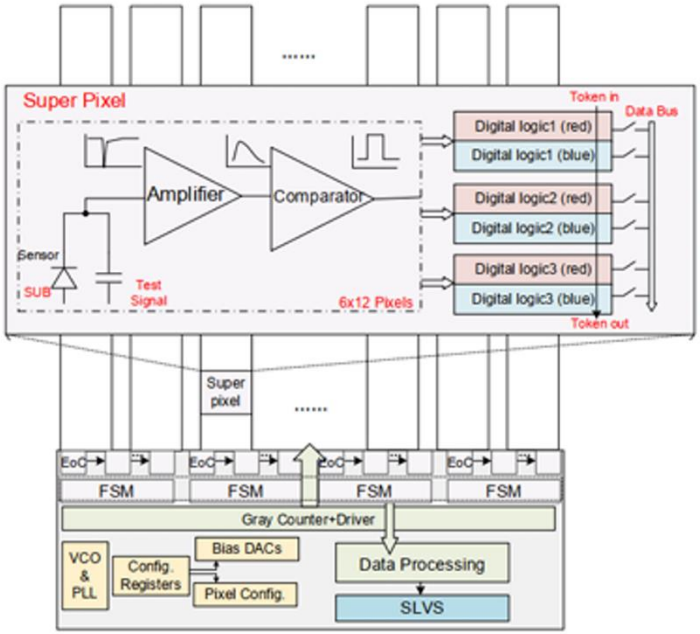
^{90}Sr Test using MIC6_V3

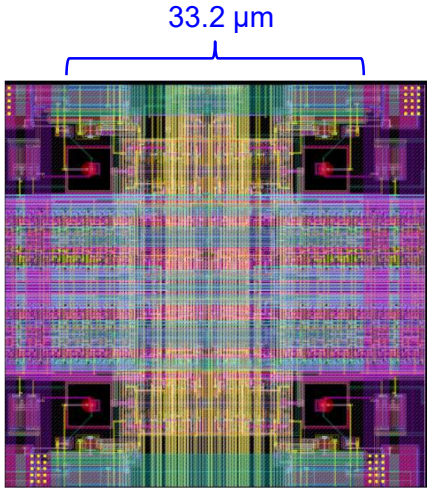


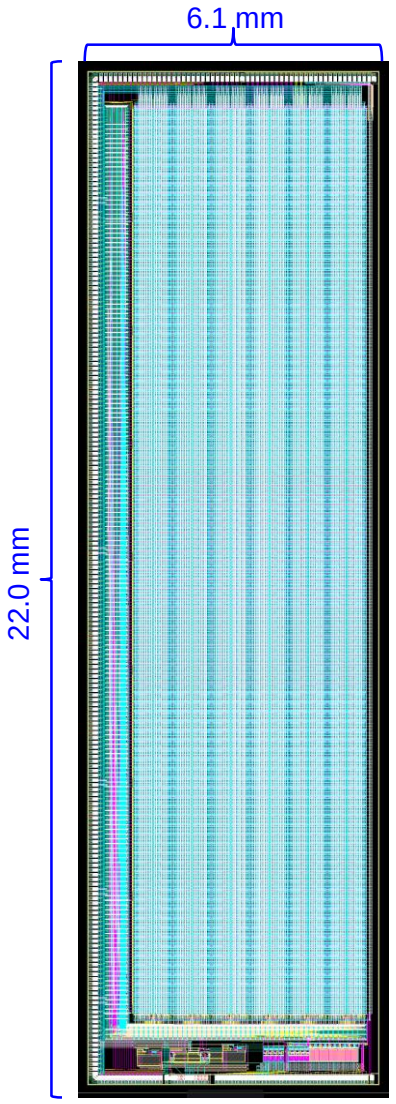
CharTPix

- Designed for Super Tau-Charm Facility Inner Tracker
- Position, Time and Charge measurement with low power consumption (Low material budget)

- Pixel Pitch: 33 μm×33 μm
- Pixel Array: 576 rows × 144 columns (prototype chip)



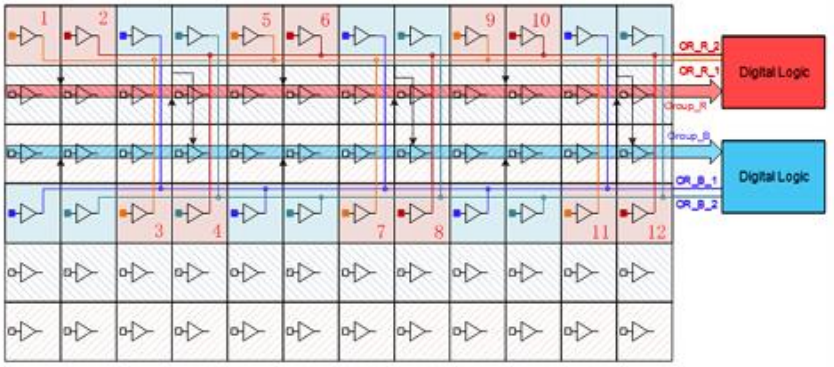


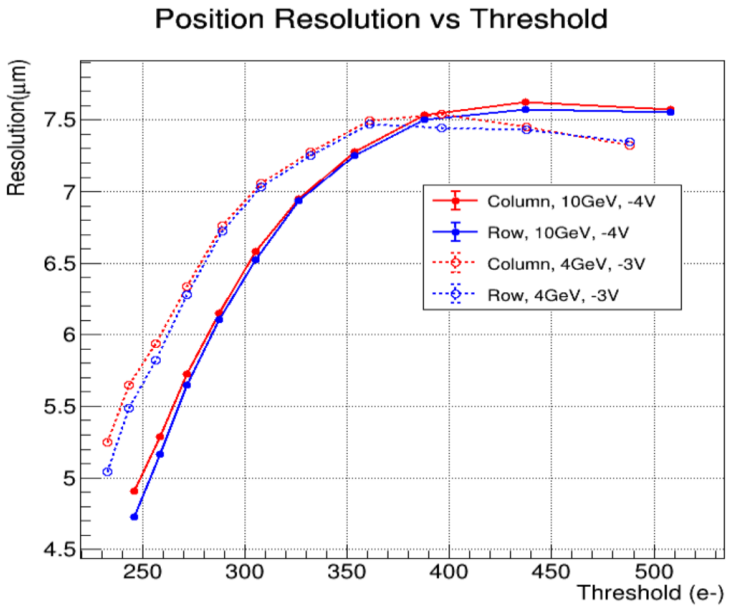


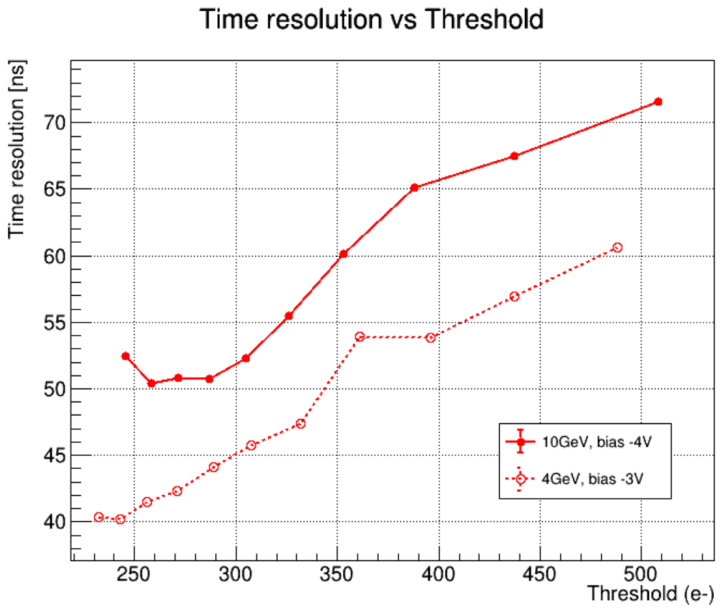
layout

CharTPix

- A novel super-pixel readout scheme is proposed
- Prototype performance
  - Threshold: 225 e-, ENC: 6.6 e-
  - Position resolution: up to 5 μm
  - Time resolution: up to 50 ns







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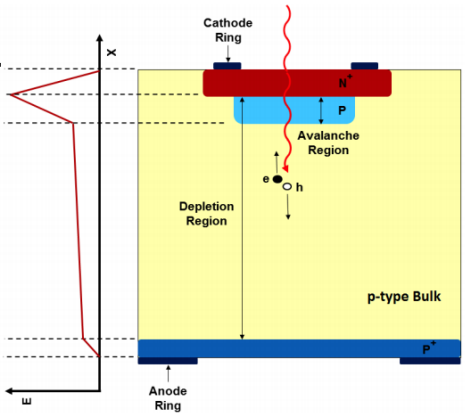
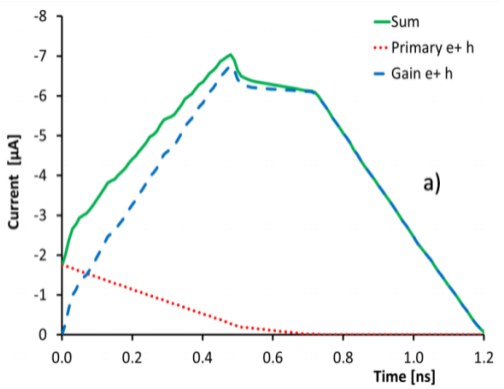
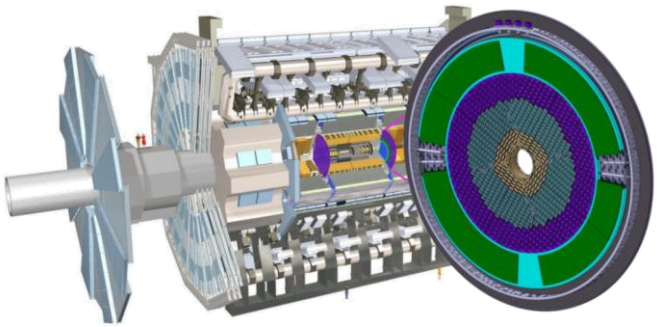
LGAD

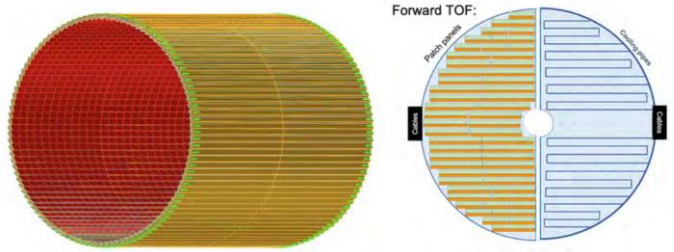
- LGAD : Low Gain Avalanche Detector
  - Pitch: ~1 mm → ~100 μm (AC-LGAD)
- Advantages:
  - High time resolution (~30 ps)
  - High spatial resolution (AC-LGAD)
- Fast and weak signals:
  - Rise time ~500ps; bottom width ~1ns; charge quantity ~10fC
- Readout challenge:
  - Low-jitter amplification discrimination
  - High-precision time measurement
  - Low-power readout (for low material quantity application)







ATLAS LGAD

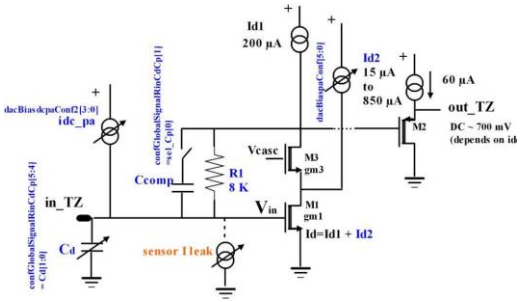


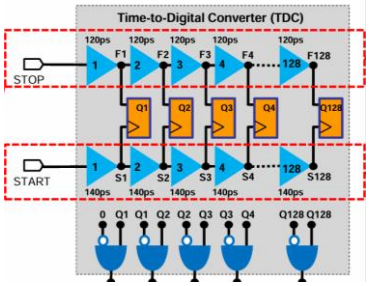
EIC AC-LGAD

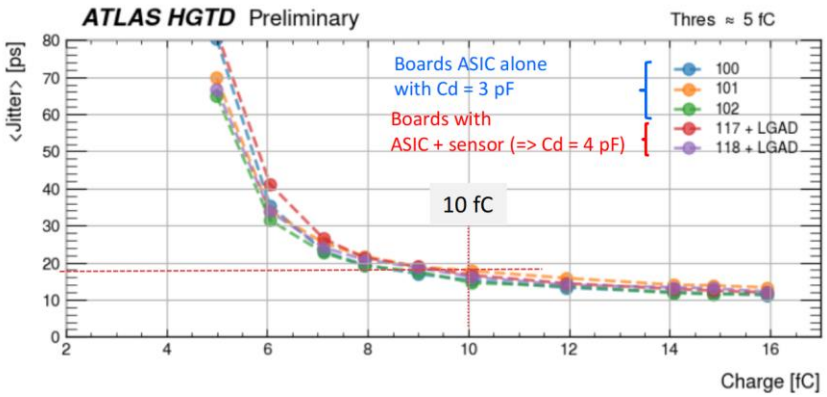
Readout ASIC: ALTIROC, ETROC, EICROC, LATIC…

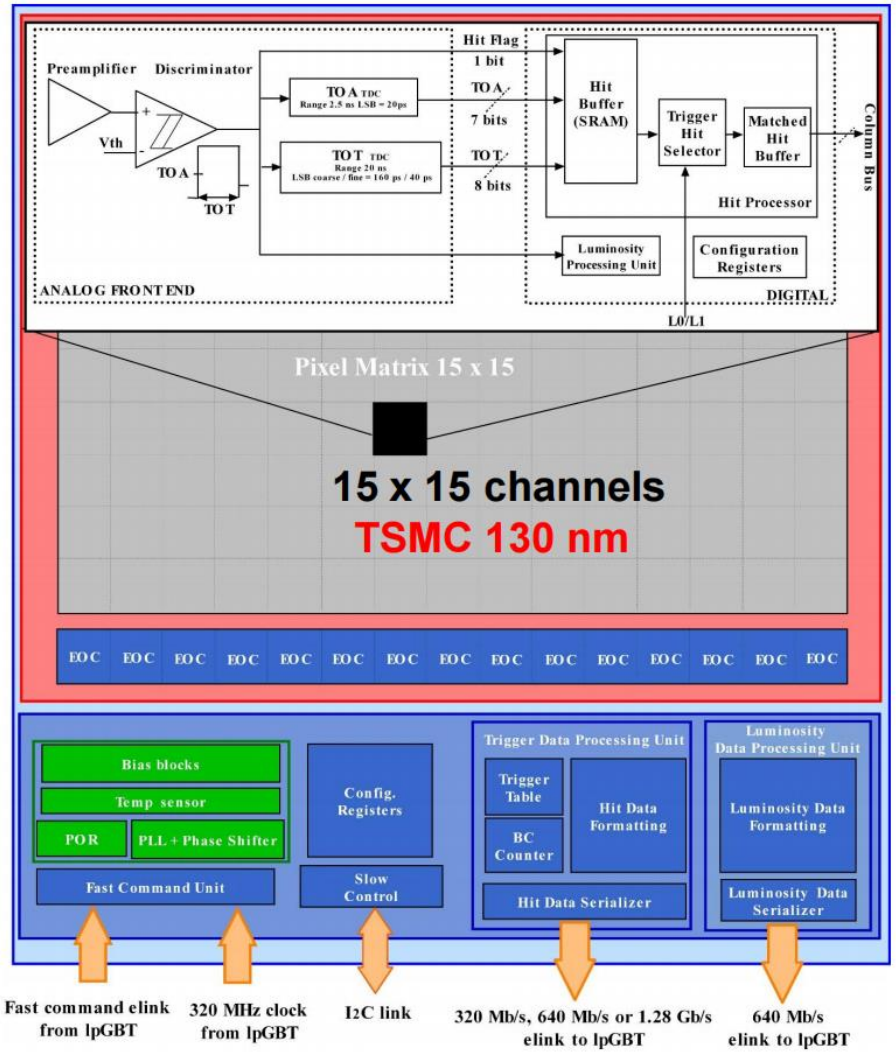
ALTIROC (for ATLAS)

- ATLAS LGAD Timing Integrated Read-Out Chip
  - Process: TSMC 130 nm
  - Architecture: Pre-Amplifier + Discriminator + TDC
  - PA：Cascode + Source Follower
  - TDC：Vernier TDC (20 ps LSB，2.56 ns range)
  - Jitter：~20 ps @ 10 fC
  - Power consumption per channel: 4mW ~ 5 mW



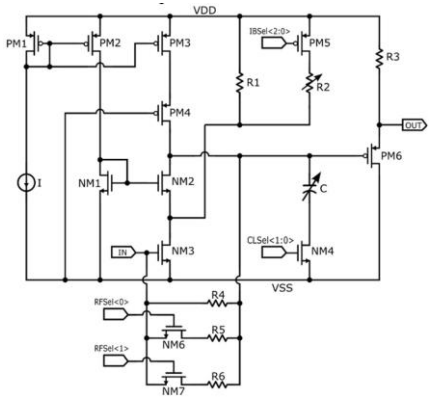


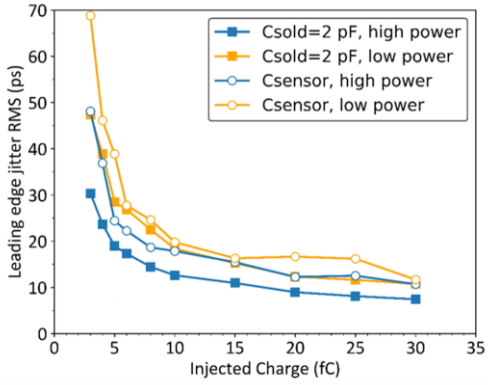


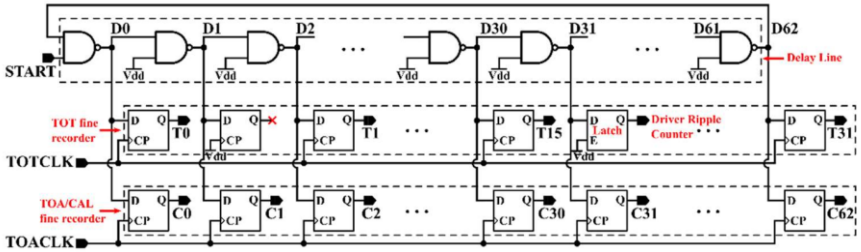


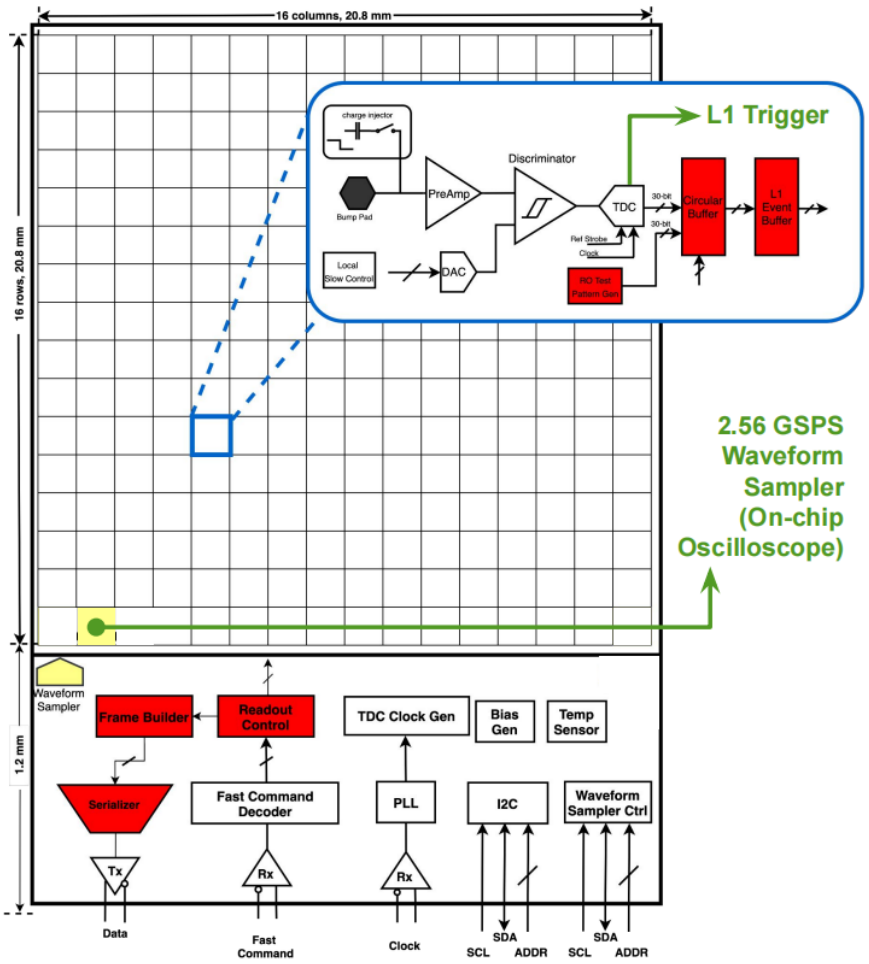
ETROC (for CMS)

- ETROC (Endcap Timing Readout Chip)
  - Process: TSMC 65 nm
  - Architecture: Pre-Amplifier + Discriminator + TDC
  - PA：Cascode + Source Follower
  - TDC：Delay chain TDC(15 ps LSB)
  - Jitter：~20 ps @ 10 fC
  - Power consumption per channel: 2.9 mW



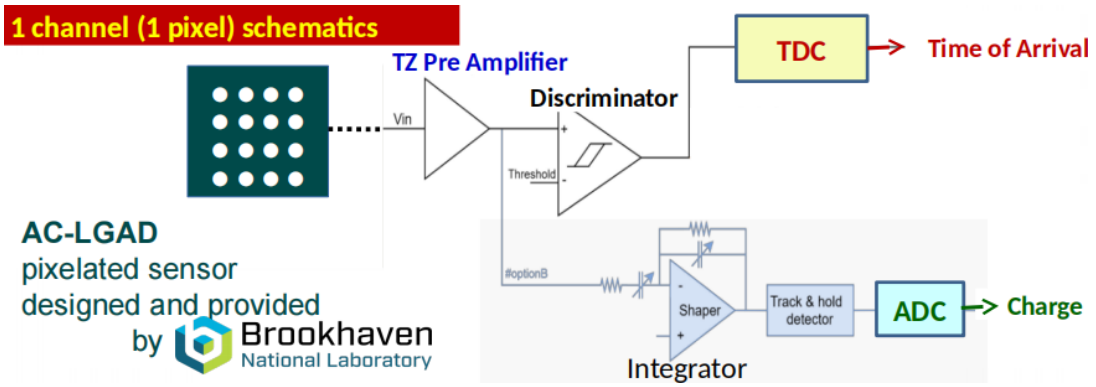






EICROC (for EIC)

- EICROC（Electron-Ion Collider Read-Out Chip）
  - Process: 130 nm
  - Architecture:
    - Pre-Amplifier + Discriminator + TDC (time measurement)
      - Adopts the time measurement circuit of ALTIROC
    - Amplifier + Shaping + ADC (charge measurement)
  - Design Goals:
    - Pixel size: 0.5 × 0.5 mm²
    - Power consumption: 2 mW/channel
    - Minimum detectable charge: 2 fC
    - Time resolution: 30 ps
    - Charge measurement function



  - Preliminary test results: jitter ~ 30 ps
    - Time jitter estimated from noise/slope of preamp output waveform

Injected charge value	ASIC without sensor	ASIC with sensor
10 fC	27.5 ps	33 ps
20 fC	16.5 ps	20 ps

Development of Pixelated Detectors

- **Larger scale & high density:**
  - a total area of m^2 to 100 m^2
  - small pitch size: hundreds of μm for LGAD and tens of μm for pixel detector
  - Smaller pixels to improve position resolution and to cope with higher hit density

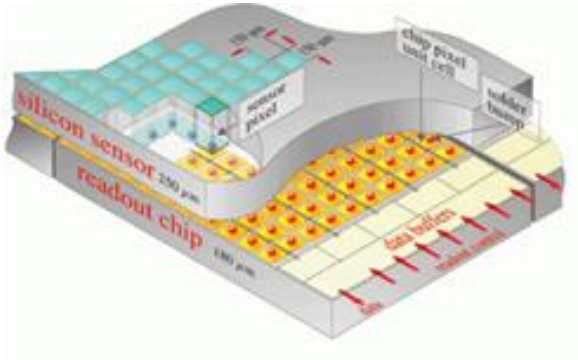
- **Pixel detector**
  - High-precision position
  - → improving timing precision
  - + charge measurement

- **LGAD**
  - High-precision timing
  - → improving spatial precision
  - + charge measurement

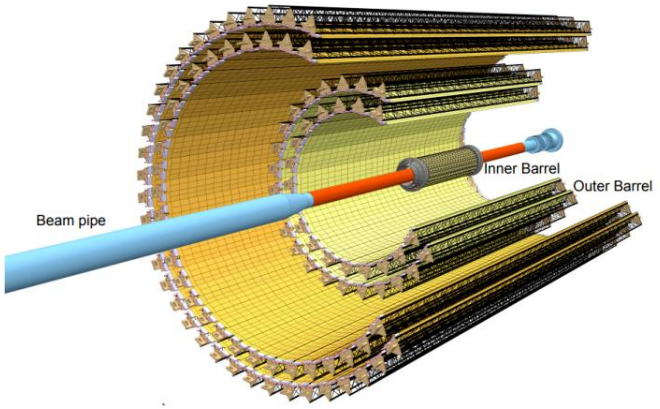
Multi-dimensional information measurement

Challenges for Pixelated Detector Readout

- **Larger number of chips**
  - e.g. ALICE ITS2 ~24000 ALPIDE chips
  - Multi-layer data concentrator is needed



- **Large amount of data to collect, process, and transfer in real-time**
  - High speed data receiving and transferring
  - Trigger match
  - Data compression



- **Control/Clock distribution**
  - Command decoding and distribution
  - Clock recovery and distribution

Content

- Background
- Front end ASICs for pixelated detectors
- Readout system for pixelated detectors
- Our work on readout electronics
- Our work on DAQ and control system
- Conclusion

RHIC-STAR

❖ Heavy Flavor Tracker, HFT

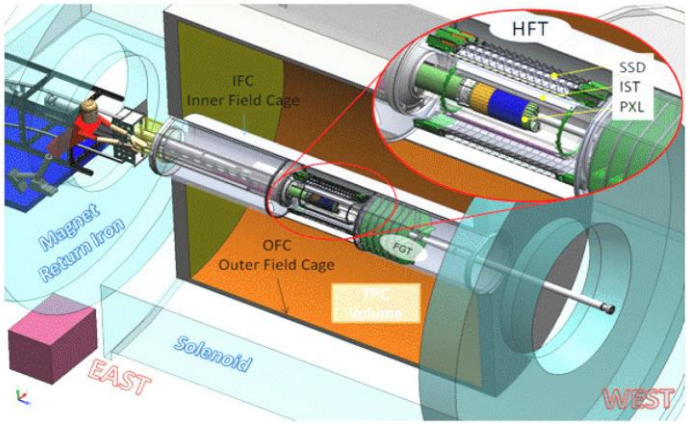
➢ Readout required

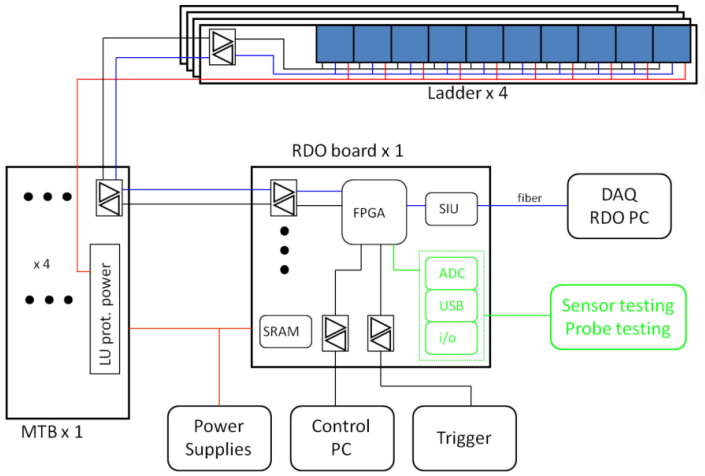
- 400 MAPS chips
- Trigger based hit selection
- Format event package
- Configuration /Trigger/Clock

➢ Readout System

- Mass Termination Board
  - Drive the detector data
  - Config & monitoring
  - 160 Mbps
- Via a 13 m twisted-pair cable to RDO
- ReaD Out Board (FPGA)
  - Zero compression and data formatting
  - Configuration processing
  - Optical fiber transmission

MAPS Detector





RHIC-sPHENIX

❖ Time-Projection Chamber, TPC

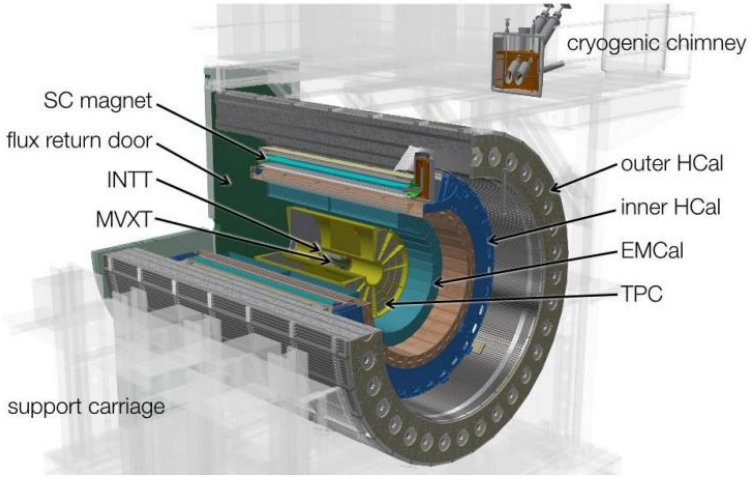
➢ Readout required

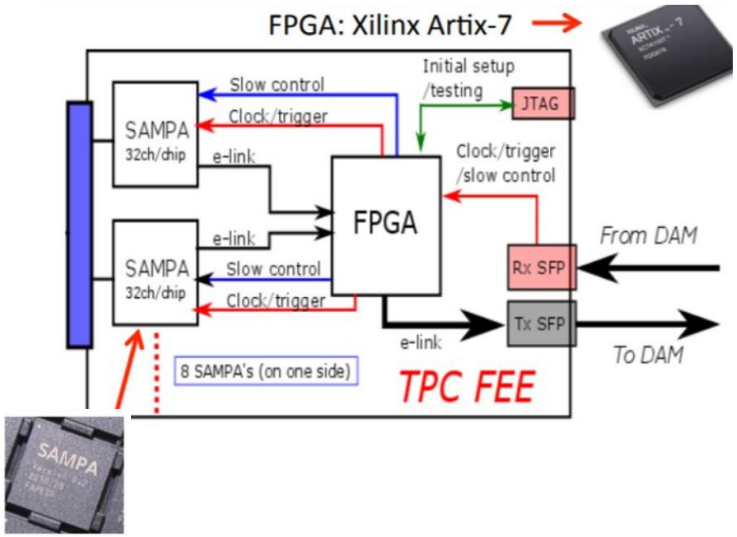
- ~1.6×10^5 chl / 624 FEE
- 960 bidirectional fibers links
- Average continuous: 1.1-1.8 Tbps total

➢ Readout System

- SAMPA ASIC
  - 32ch/chip & 320 Mbps
  - Fast timing /ADC/DSP
- FPGA
  - Data formatting
  - Clock/Trigger/Slow control
  - 5 Gbps fiber link

MPGD Detector

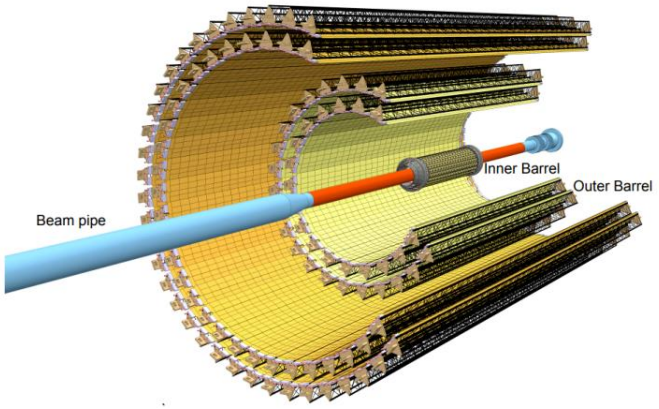




LHC-ALICE

❖ Inner Tracker System，ITS

MAPS Detector

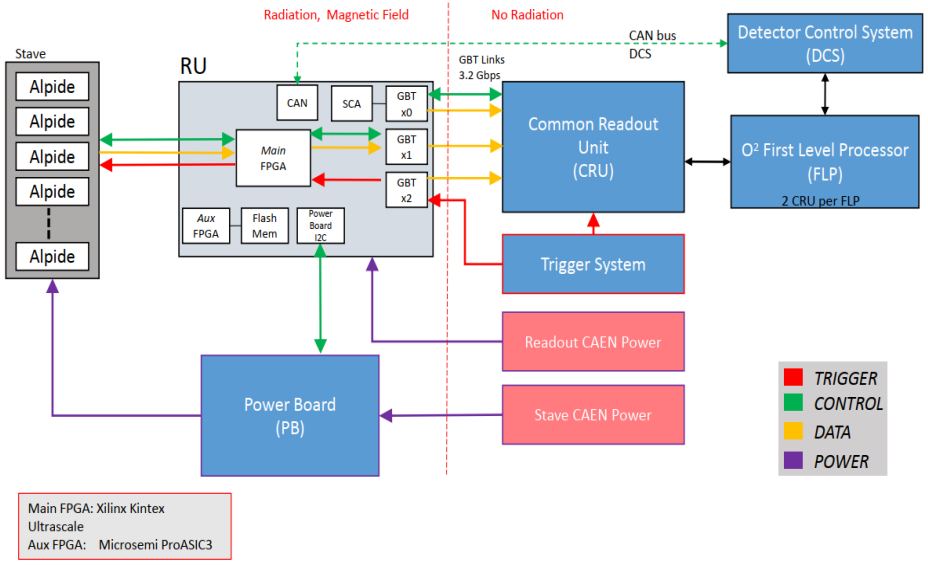


➢ Readout required

- 2 barrels (IB,OB)
- 7 cylinder layers
- Data Reformat & Uplink
- Control /Trigger/Time Signal

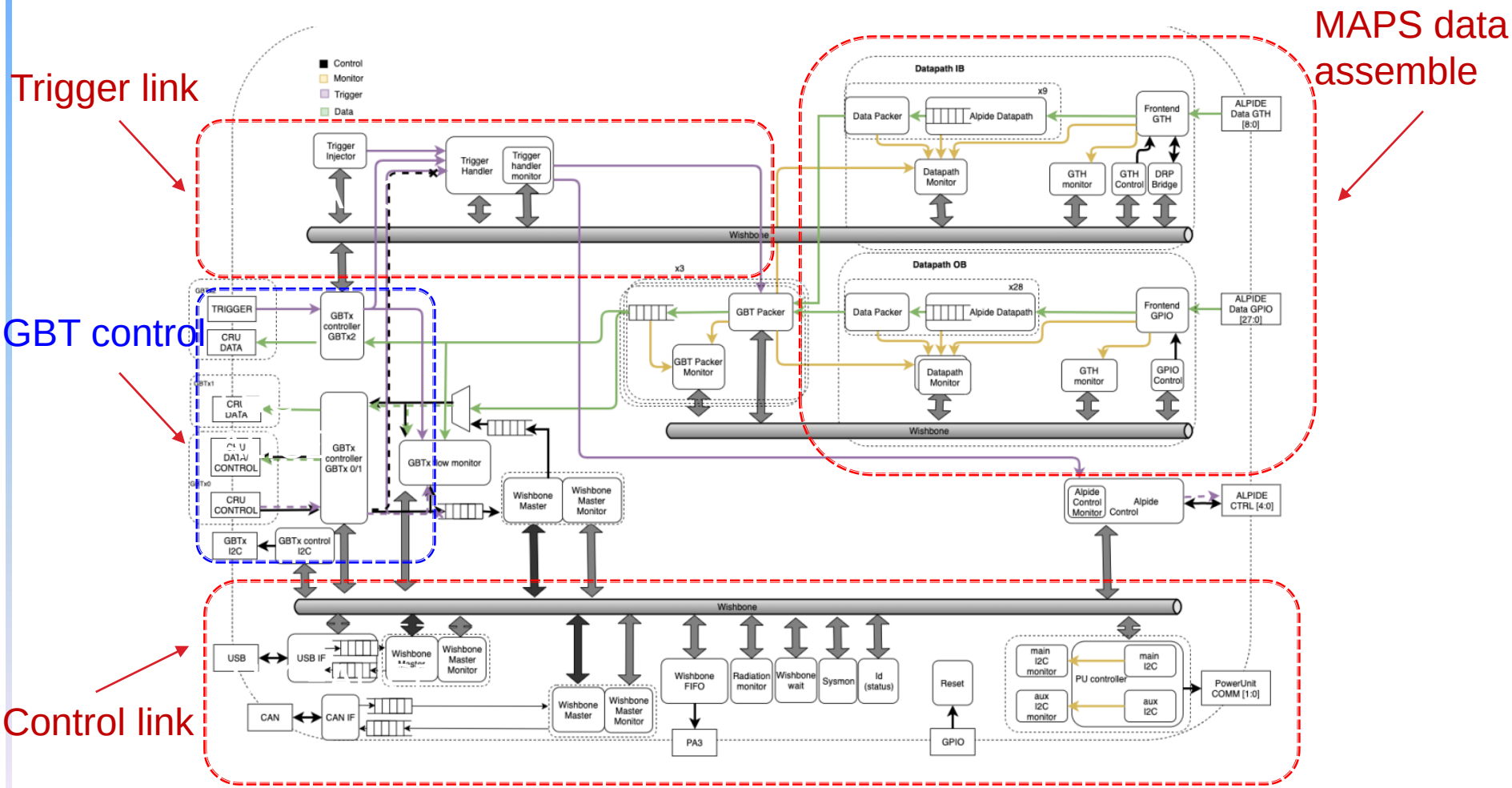
➢ Readout System

- SRAM-FPGA
  - Control and read out the data from stave
  - Deliver packed data to CRU
- Flash-FPGA
  - monitor and protect the SRAM-FPGA from SEU
- SCA ASIC
  - Control and monitor
- GBT ASIC
  - High-speed data transfer(4.8 Gbps)



LHC-ALICE

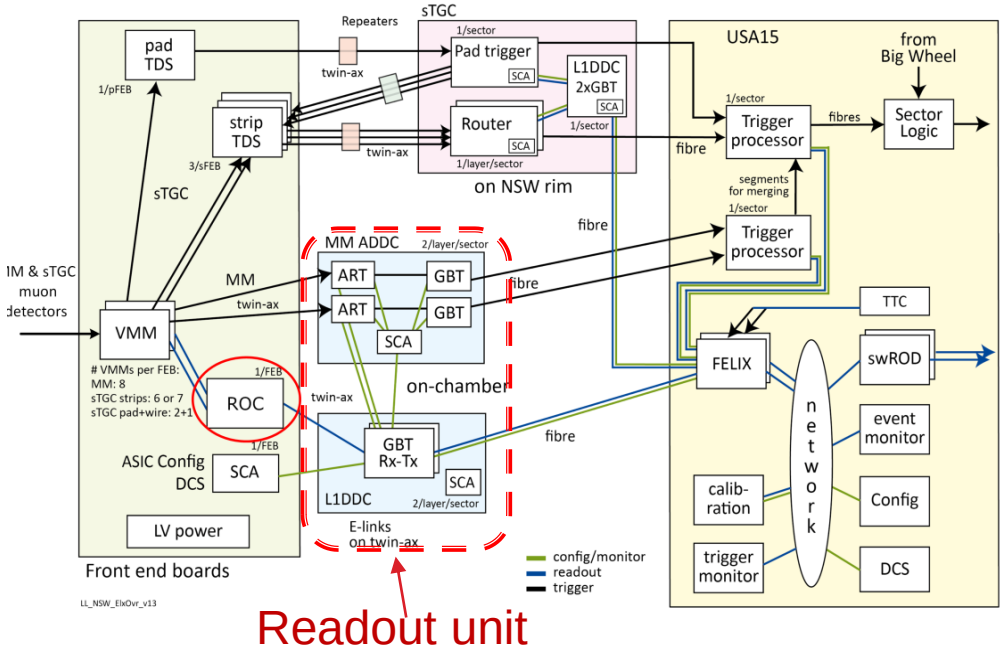
- Block Diagram of ITS-RU data processing logic



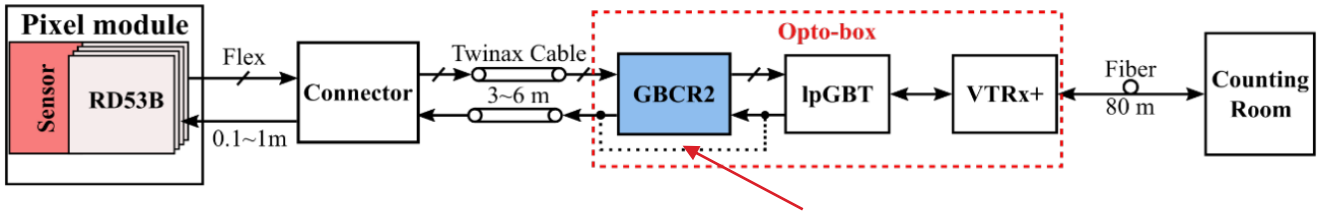
LHC-ATLAS

❖ New Small Wheel，NSW

- VMM ASIC
  - Merges data from 64 front-end channels
  - Output: 2 lines @ 640 Mbps
- ROC ASIC
  - Handling, Preprocessing and formatting the data
  - E-LINK
  - 320 Mbps/link
- SCA ASIC &GBT ASIC (4.8 Gbps)

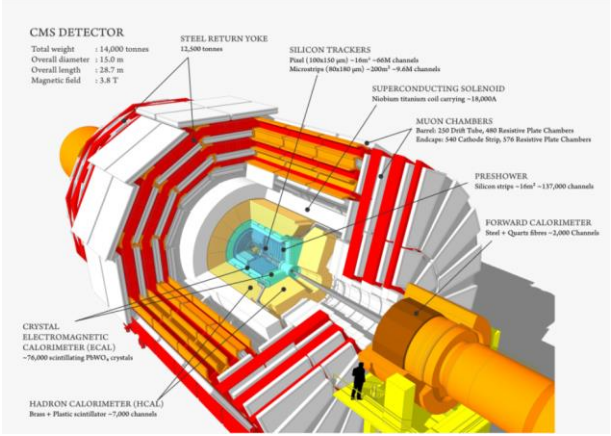


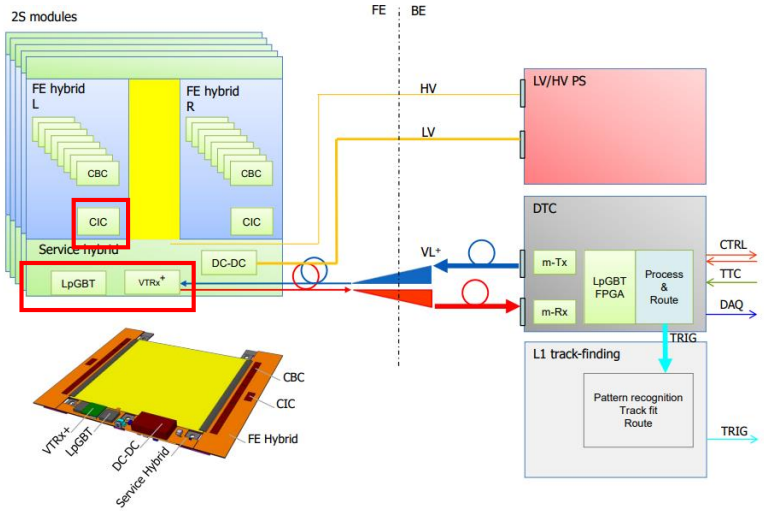
❖ Inner Tracker (ITK)



LHC-CMS

- **Tracker system**
  - Providing tracking information to the L1 trigger
  - Outer Tracker & Inner Tracker
- Trigger rate: 100 kHz to 750 kHz
- Latency: 12.5 μs
- **Readout System**
  - CIC ASIC
    - ✓ Collect and format the front-end chips data
    - ✓ Distribute clock, trigger, and control signals
  - lpGBT ASIC & VTR+ ASIC
    - ✓ Transmission of the data and the distribution of clock and control signals





Data chain options

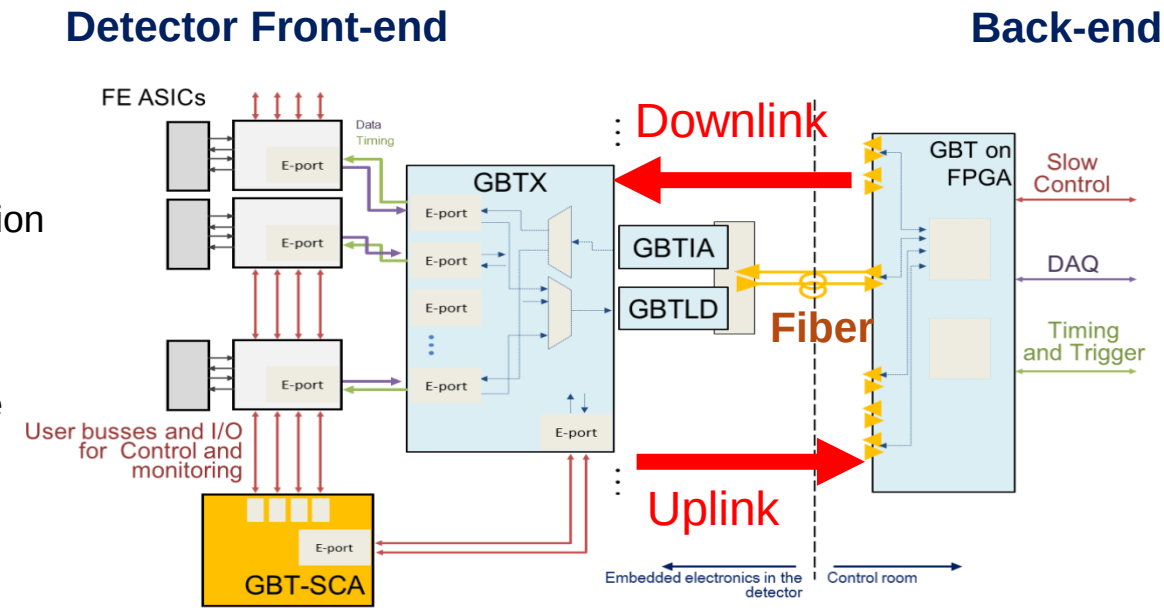
- FPGA
  - Programmable device
  - Flexible
  - Abundant resource
  - High speed data interface
  - High cost
  - High system complexity
  - System radiation hard design

- ASIC
  - Specifically designed chip
  - Much effort in chip design & testing
  - High speed data interface
  - Low cost in massive production
  - Low system complexity
  - Chip level radiation hard design

- ASIC-based technique is very important for large scale application.
- Categorization in functionality and systematic R&D is necessary.

High-speed Data Transmission System in HEP

- **FE/ROC ASIC**:
  data collector & processing
- **SCA ASIC**:
  slow control, cmd & config distribution
- **GBTx**:
  bi-directional data interface ASIC
- **VTRx**: Customized optical module
  - **GBLD**:
    high-speed laser driver ASIC
  - **GBTIA**:
    high-speed low noise
    transimpedance amplifier ASIC

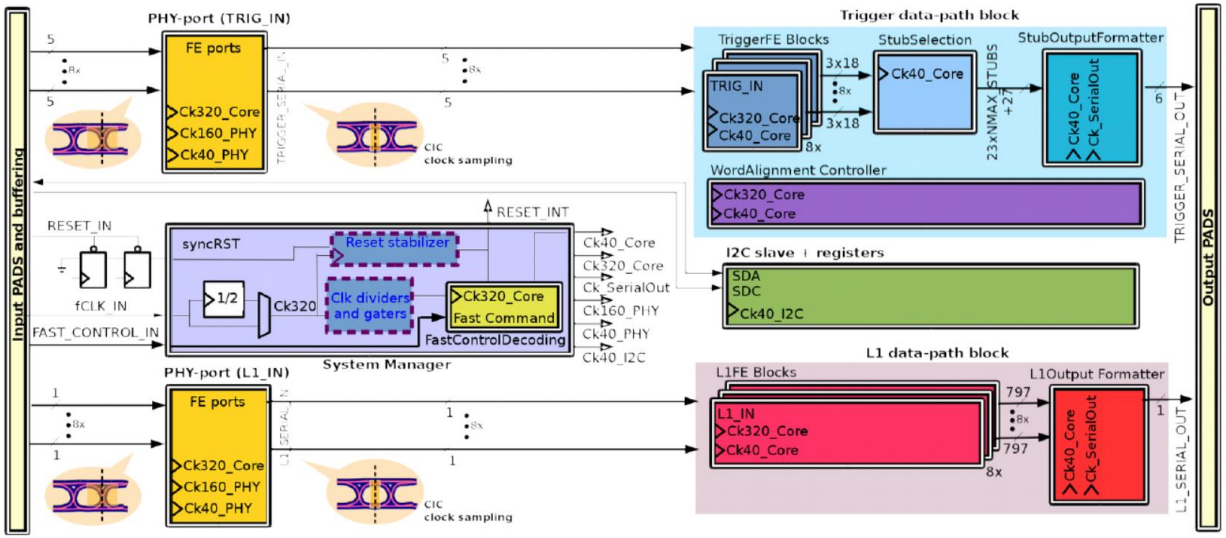


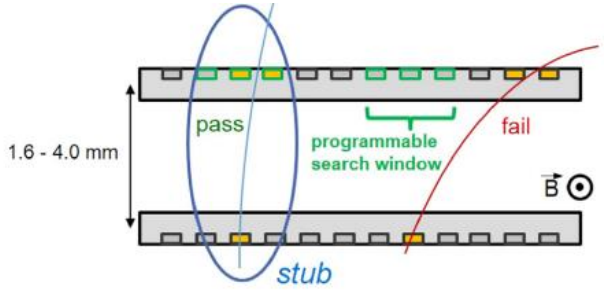
Bi-directional Optical data transmission scheme developed by CERN

- Optical data transmission between the front-end and back-end is widely used in particle physics experiments.
- Versatile Link Project: A typical system developed by CERN.
  - Aims to build a high-speed, radiation-tolerant, bi-directional optical data transmission system for the particle physics experiments applications.

CIC ASIC

- The Concentrator Integrated Circuit (CIC) ASIC is a front-end chip for both Pixel-Strip and Strip-Strip modules of the Phase-II CMS Outer Tracker upgrade at HL-LHC.



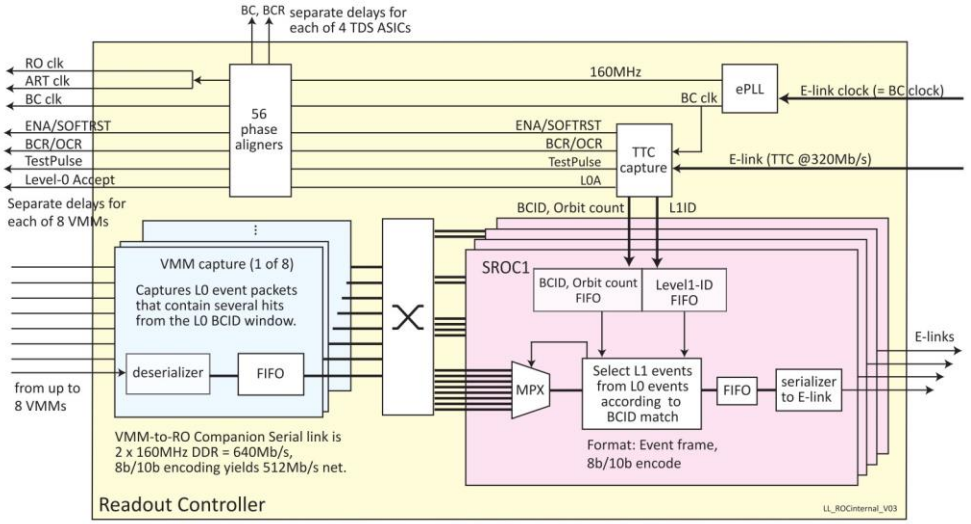


- Input: 48 lines @ 320 MHz, connected to 8 FE chips
  - Each FE chip, 5-bit trigger data and 1-bit L1 data
- Output： 7 lines @320/640MHz
  - 6 lines for trigger data and 1 line for L1 data
- Data compression

VMM ROC ASIC

- VMM ROC is used for handling , filtering and real-time packet processing of ATLAS muon detector data

  - Input
    - 8 channel / Data rate: 640 Mbps
  - Output
    - 4 channel / Data rate: 640/320/160/80Mpbs (DDR)
  - TTC rate: 320 Mbps (DDR)
  - Configurable X Bars
  - Multi-channel data aggregation
  - Output clk 80/160/320MHz clock signal to VMM, TDS, ART
  - Send soft reset /BC reset/Test Pulse

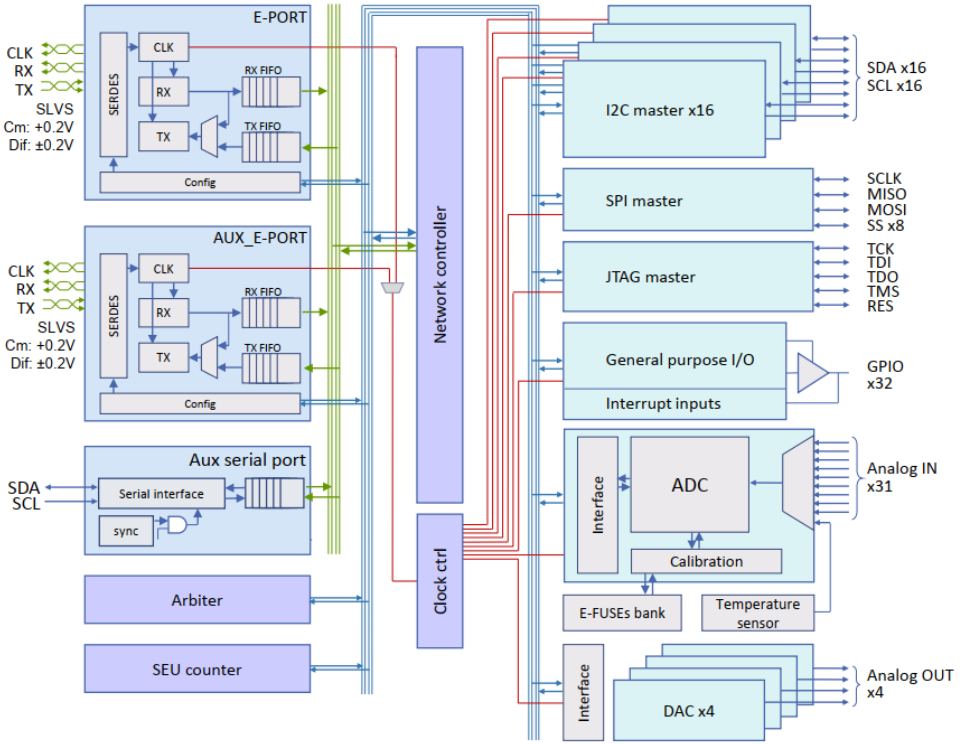


Slow Control ASIC

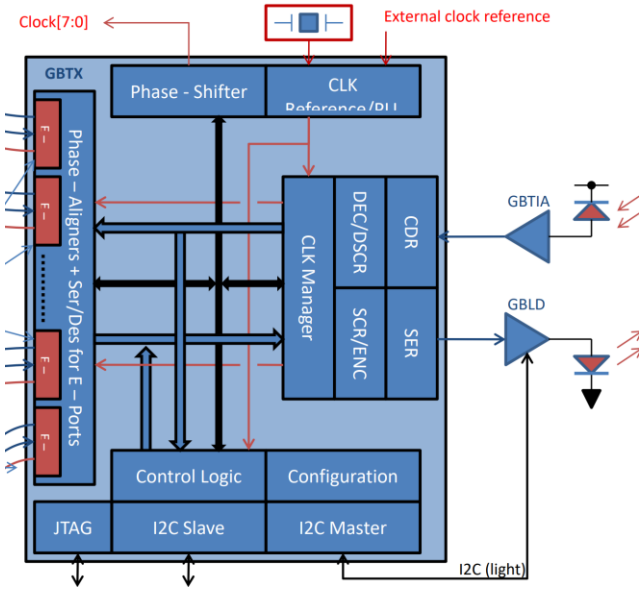
- GBT-SCA ASIC provides slow control signals for configuring and monitoring FE and detectors.

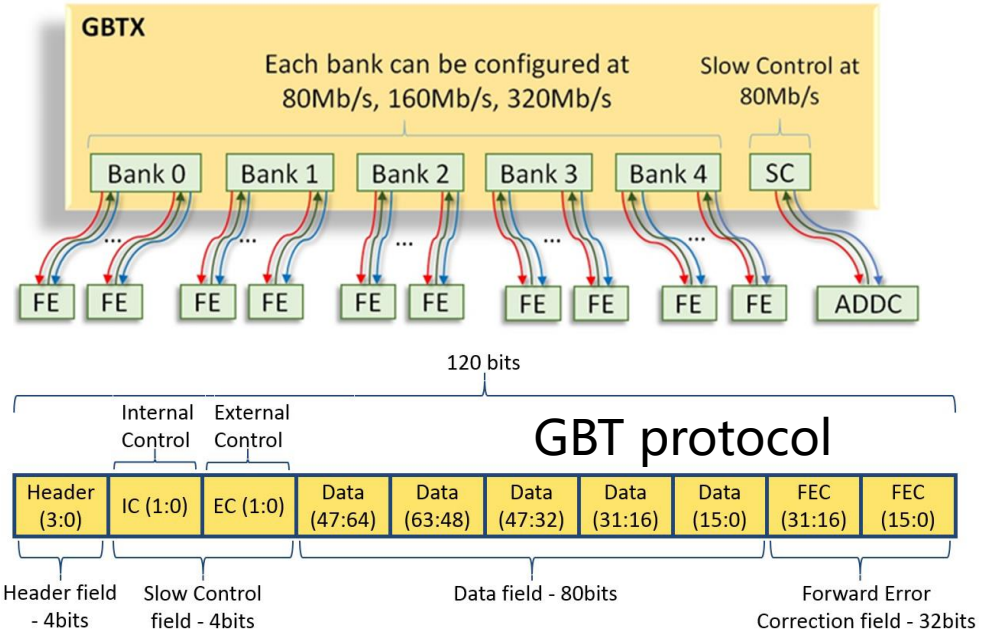
- Variety of protocol buses and functions
  - 32 bit Parallel Interface Adapter (GPIO)
  - 16 independent I^2C master serial bus channels

    SPI master，8 individual slave
  - JTAG serial bus master channel
  - 12-bit ADC（31 bit analog inputs）
  - 4 DAC channels，8 bit resolution
  - Temperature monitoring module



GBTx & LpGBT ASIC

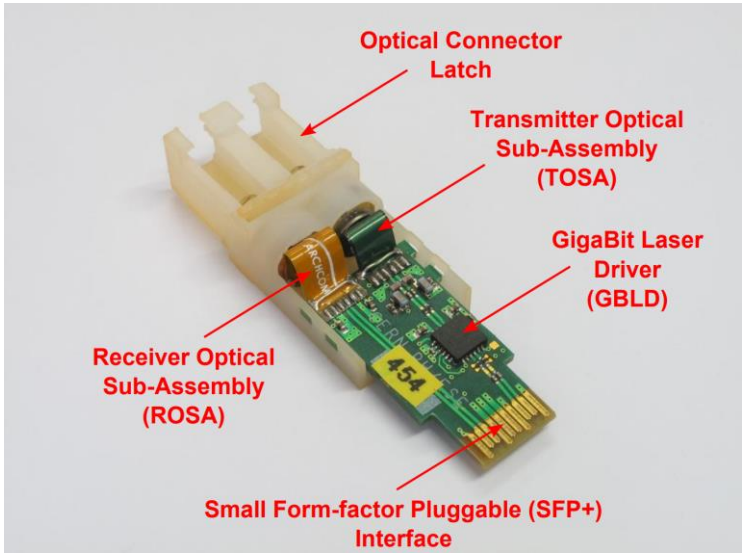




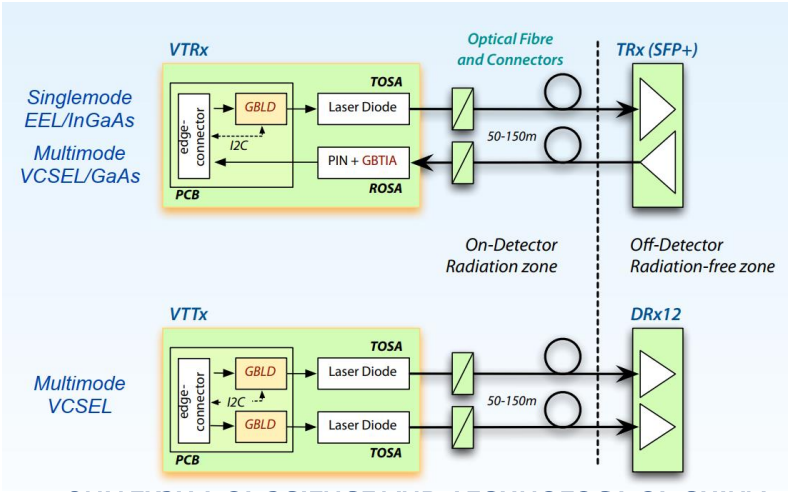
- GBTx ASIC
  - Input:
    - -40 channels @ 80Mbps
    - -20 channels @ 160Mbps
    - -10 channels @ 320Mbps
  - Output： 4.8 Gbps
  - Power： 2.2 W / 1.5V
  - BGA 400 pin
  - 130 nm CMOS

- LpGBT ASIC is the upgraded of the GBTx
  - Input：
    - Input channel: 28/14/7
    - Data rate: 160/320/640 Mbps @ output 5.12 Gbps
    - Data rate: 320/640/1280 Mbps @ output 5.12 Gbps
  - Output: 5.12 Gbps /10.24 Gbps
  - Power： 1.2V
  - BGA 289 pin
  - 65 nm CMOS

Optical Fiber Transceiver ASIC



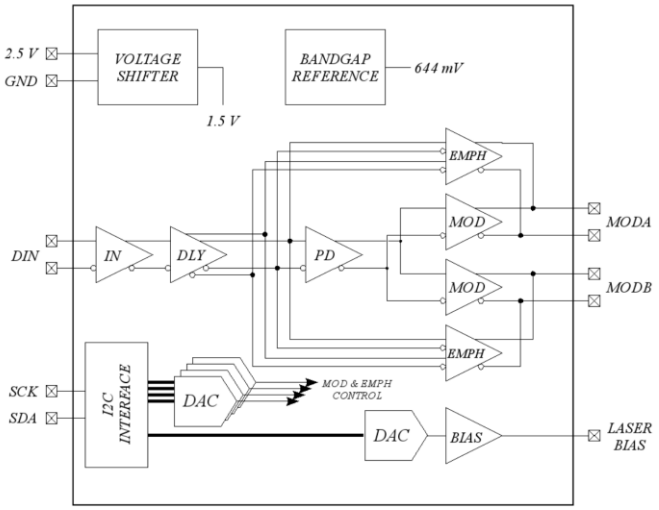
VTRx Optical Module Developed by CERN

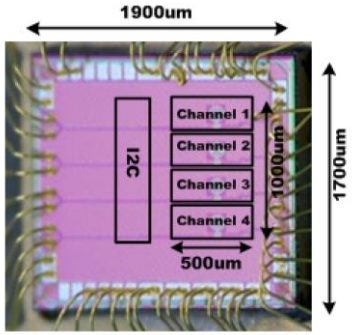


- VTRx (Versatile Link Transceiver) is a customized optical module developed by CERN. It is a pluggable module that integrates the laser, PIN-diode, GBLD, GBTIA and related optical components and mechanics.

- This module was first developed using TOSA and ROSA components as the single-channel form (1Tx + 1Rx), and updated to **VTRx+** using the laser array and array driver to achieve the parallel-channel form (4Tx + 1Rx, configurable).

GBLD & GBTIA ASIC

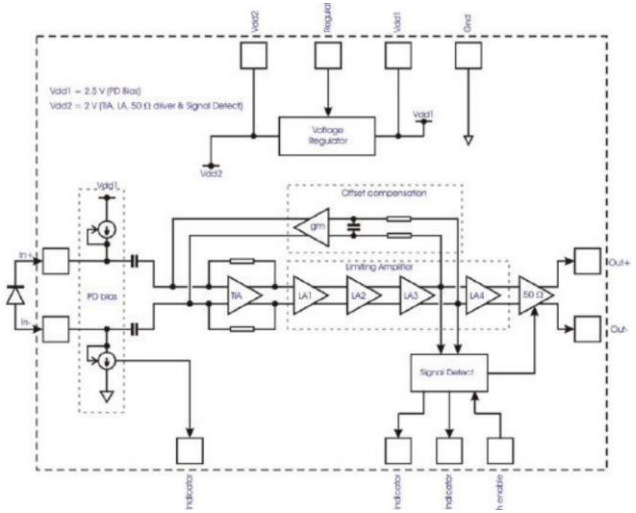


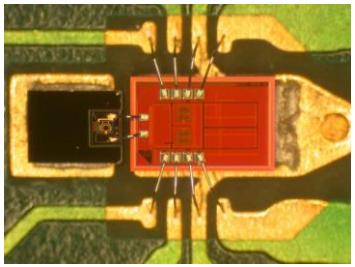


LDQ10 ASIC（GBLD ASIC in 65nm）

- Upgrade to 65nm CMOS
- 4 x 10 Gbps/ch
- Four-channel laser array driver

- GBLD is a laser driver ASIC. It amplifies the high-speed serial data from GBTx ASIC, and drives the VCSEL laser to emit light.
- This lase driver ASIC was first developed under 130nm CMOS technology (GBLD, 5 Gbps/ch), and updated to the four-channel array form (4 x 10 Gbps/ch) in 65nm CMOS technology.





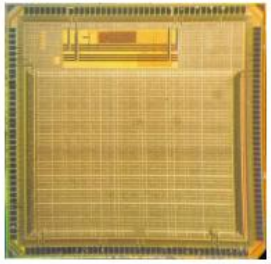
GBTIA ASIC

- 130 nm CMOS
- 2.56 Gbps/ch
- Downlink

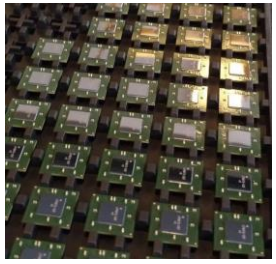
- GBTIA is a transimpedance amplifier ASIC. It amplifies the high-speed current signal from PIN-Diode as part of the downlink optical-to-electrical conversion.
- This ASIC was first developed under 130nm CMOS technology (GBTIA), and updated to the lpGBTIA using 65nm CMOS technology.

Summary of GBT & VTRx

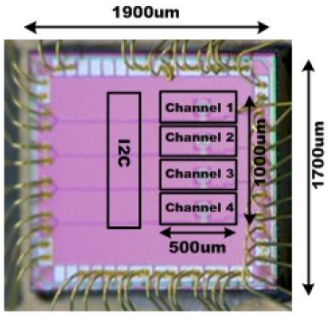
- The first generation of the GBT ASICs is based on 130 nm CMOS technology (around 2011). 2.56 Gbps Downlink + 5 Gbps uplink.
- The second generation of the GBT ASICs is based on 65 nm CMOS technology (around 2019). 2.56 Gbps Downlink and 10 Gbps uplink.
- In future, more advanced process (28nm, …), higher data rate, lower power…



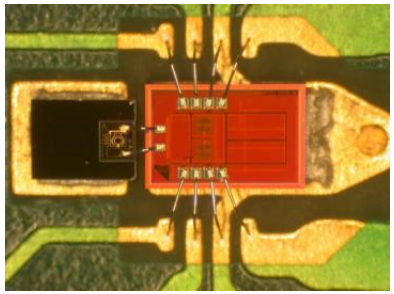
GBT_SCA
130nm CMOS



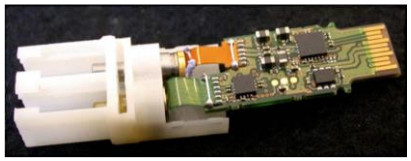
lpGBTx
65nm CMOS



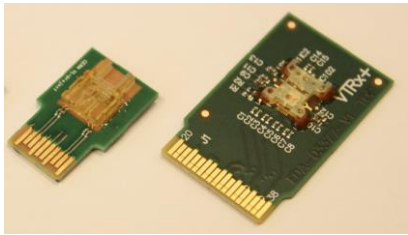
GBLD (LDQ10)
65nm CMOS



GBTIA
130 nm CMOS



1Tx
1Rx



4Tx
1Rx

VTRx+ optical module

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  - Readout chain
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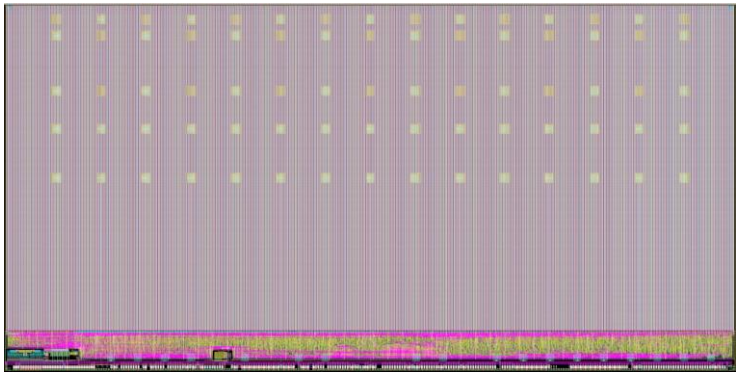
MIC6_V4

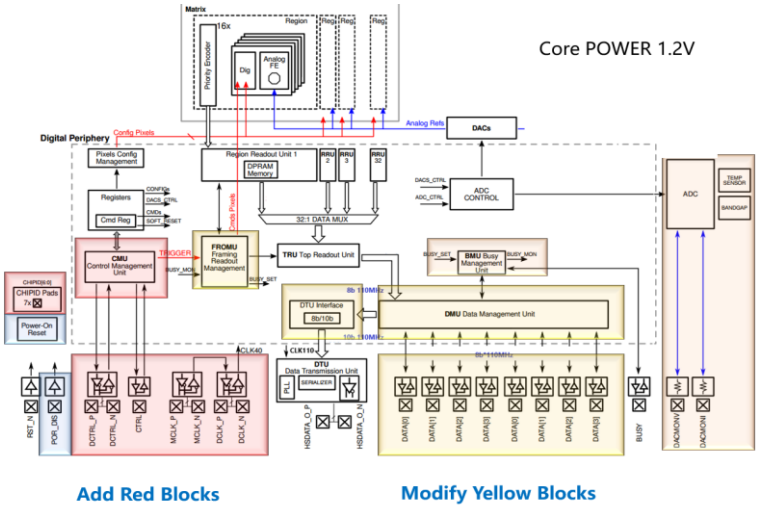
MIC6_V4 has been designed and fabricated.

Modifications based on MIC6_V3

- Add clock interconnection between chips
- Add control management unit to replace SPI
- Add master-slave transmission mode
- Differential signals are used for clock and control signals
- Increase output data rate to 1.2Gbps
- Add on-chip LDO



Layout of MIC6_V4



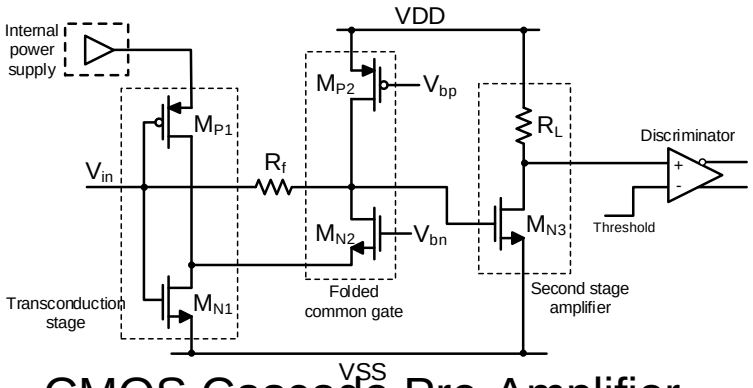
MIC6_V4 block diagram

Test board of MIC6_V4

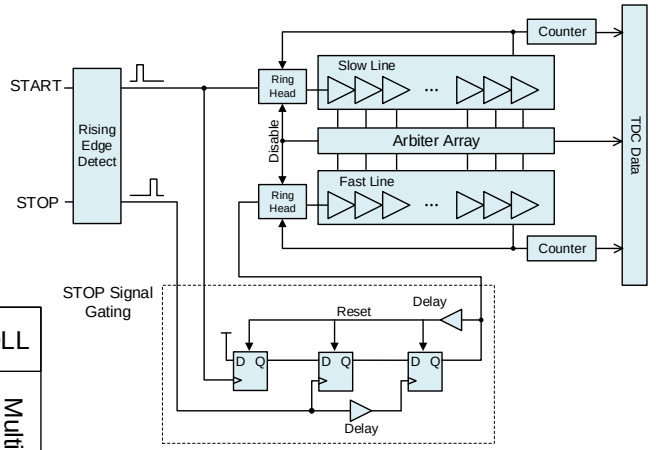
Chip performance	
Process	GSMC-130 nm
Core Voltage	1.2V
Chip Size	30 mm×15 mm
Pixel Array	980×497
Pixel Size	30.53 um×26.8 um
Readout Mode	AERD
Output data rate	1.2Gbps
Encoding	8B10B
Slow Control	MLVDS Control Bus
Cascade Readout	master-slave data aggregation and transmission

LGAD front-end readout ASIC

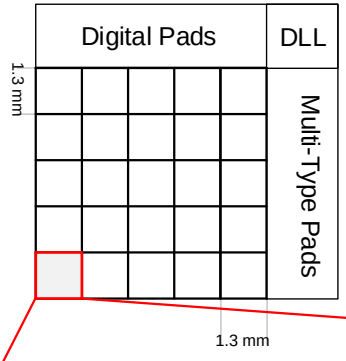
- LATIC: LGAD Amplification and Timing IC
- High precision time measurement array for weak and fast signal
  - 10 fC charge，~500 ps rising time
  - < 20 ps electrical time measurement precision

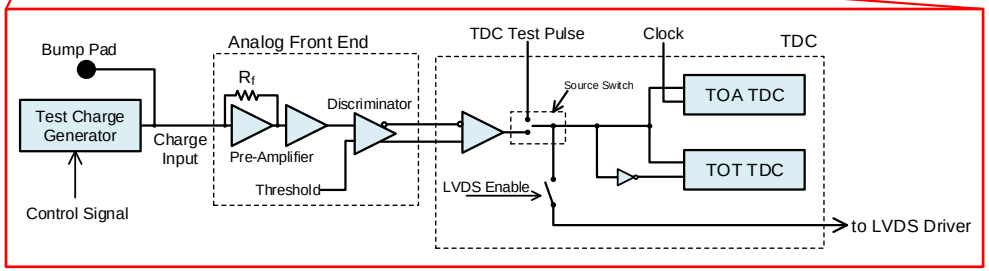


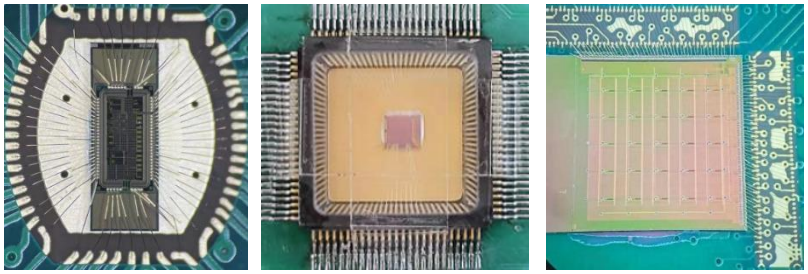
CMOS Cascode Pre-Amplifier



Dual-ring Vernier TDC

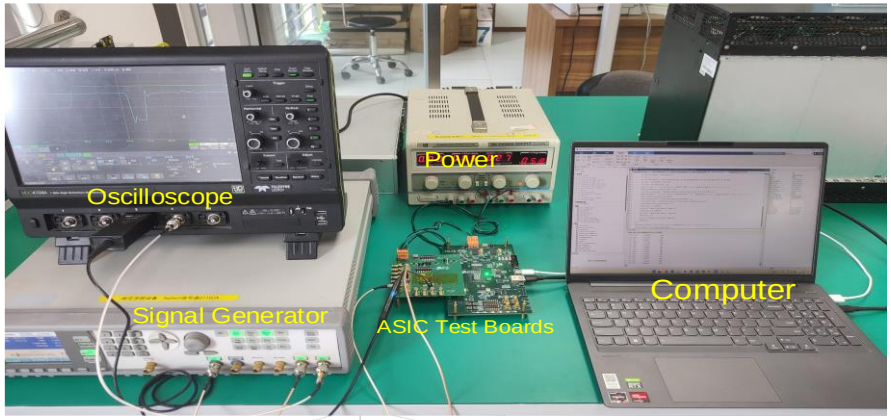


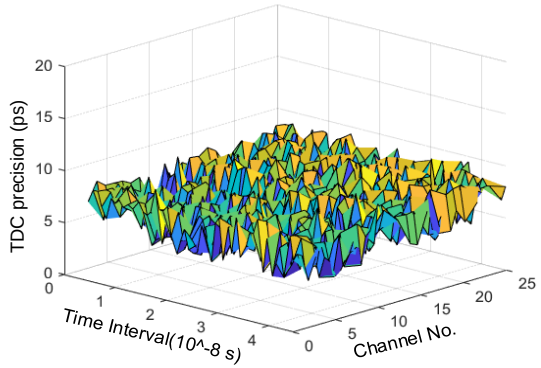


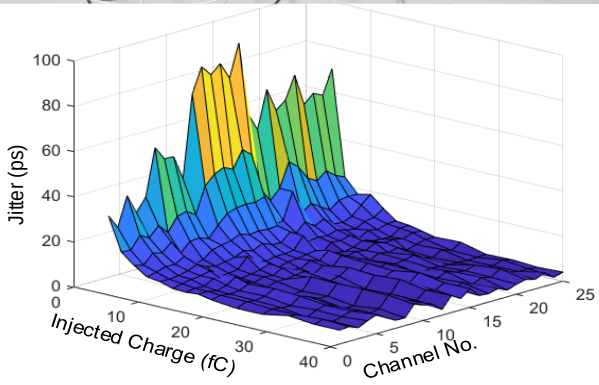


LGAD front-end readout ASIC

- TDC performance:
  - Dual-ring Vernier TDC
  - ~5 ps precision
- Full-chip performance:
  - < 20 ps @10 fC, 4pF
  - < 10 ps @large signal (>15 fC)
- Power consumption: 3 mW/chn





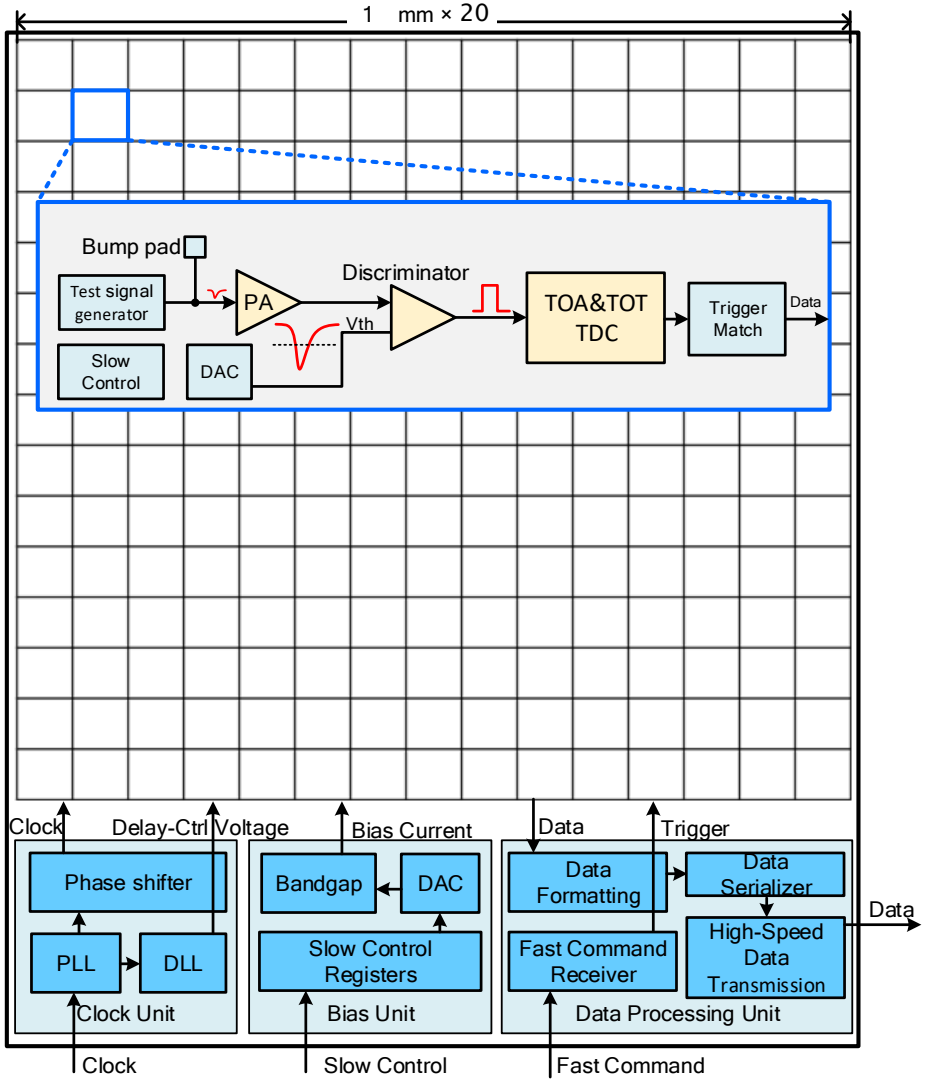


key design parameters of LGAD readout ASICs.

ASIC	ALTIROC0	ALTIROC1	ETROC0	ETROC1	LATIC0	LATIC1
Technology	130 nm	130 nm	65 nm	65 nm	180 nm	130 nm
LGAD pad size	1.3×1.3 mm^2	1.3×1.3 mm^2	1.3×1.3 mm^2	1.3×1.3 mm^2	1.3×1.3 mm^2	1.3×1.3 mm^2
Channel number	8	5×5	1	5×5 (4×4 with full chain)	8 / 5×5	5×5
Integrated TDC	no	yes	no	yes	no	yes
σ_{TOA} @	27 ps	<25 ps	<16 ps	~42 ps beam test with sensor	<20 ps	<20 ps
Charge	10 fC	10 fC	15 fC sensor cap.		10 fC	10 fC
Capacitance	3.3 pF	4 pF			6 pF	4 pF

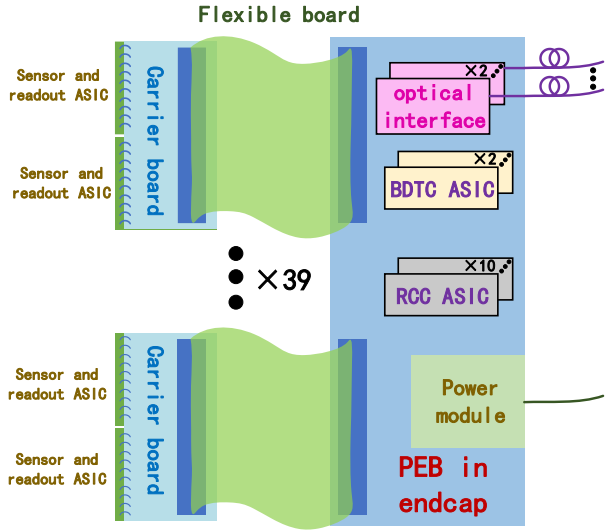
LGAD readout ASIC for H-NS

- Further power consumption optimization for the in-pixel circuit
- Develop LGAD readout ASIC with 20×20 array size
- Global Bias and monitoring
- Global Slow Control
- On-chip clock management
- On-chip data buffering and aggregation

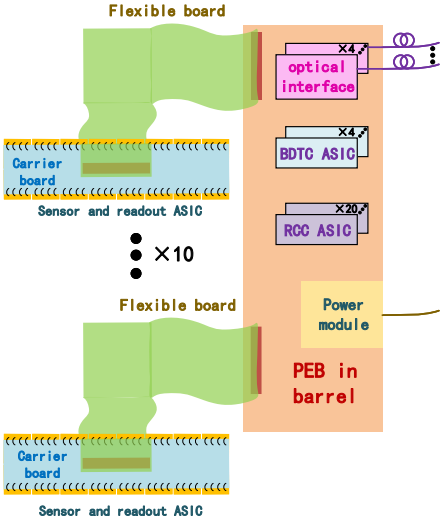


Scheme of readout electronics for LGAD

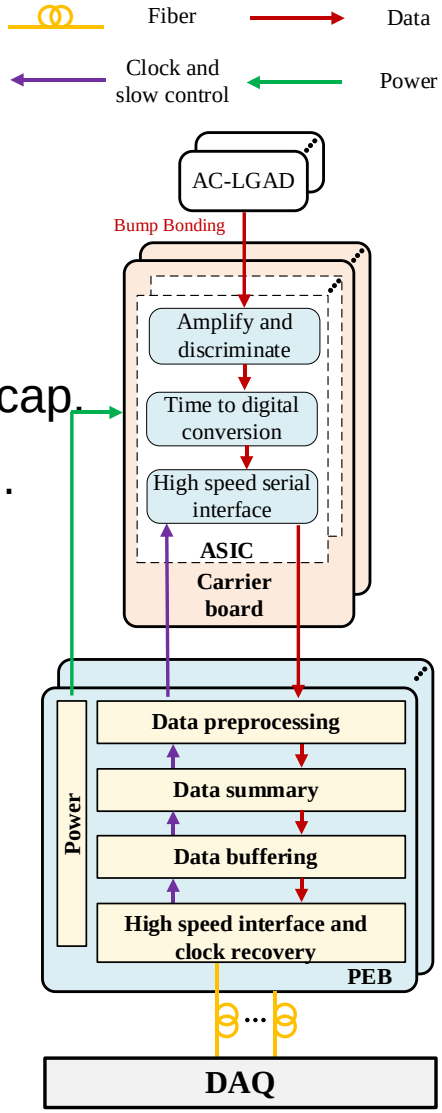
- H-NS LGAD includes one barrel and one endcap.
- The front-end electronics include carrier board and peripheral electronics board (PEB).
  - The carrier boards are installed in the sensitive area.
  - The PEBs of endcap are installed on the outer of the endcap.
  - The PEBs of barrel are installed along the beam direction.



Scheme of electronics in endcap



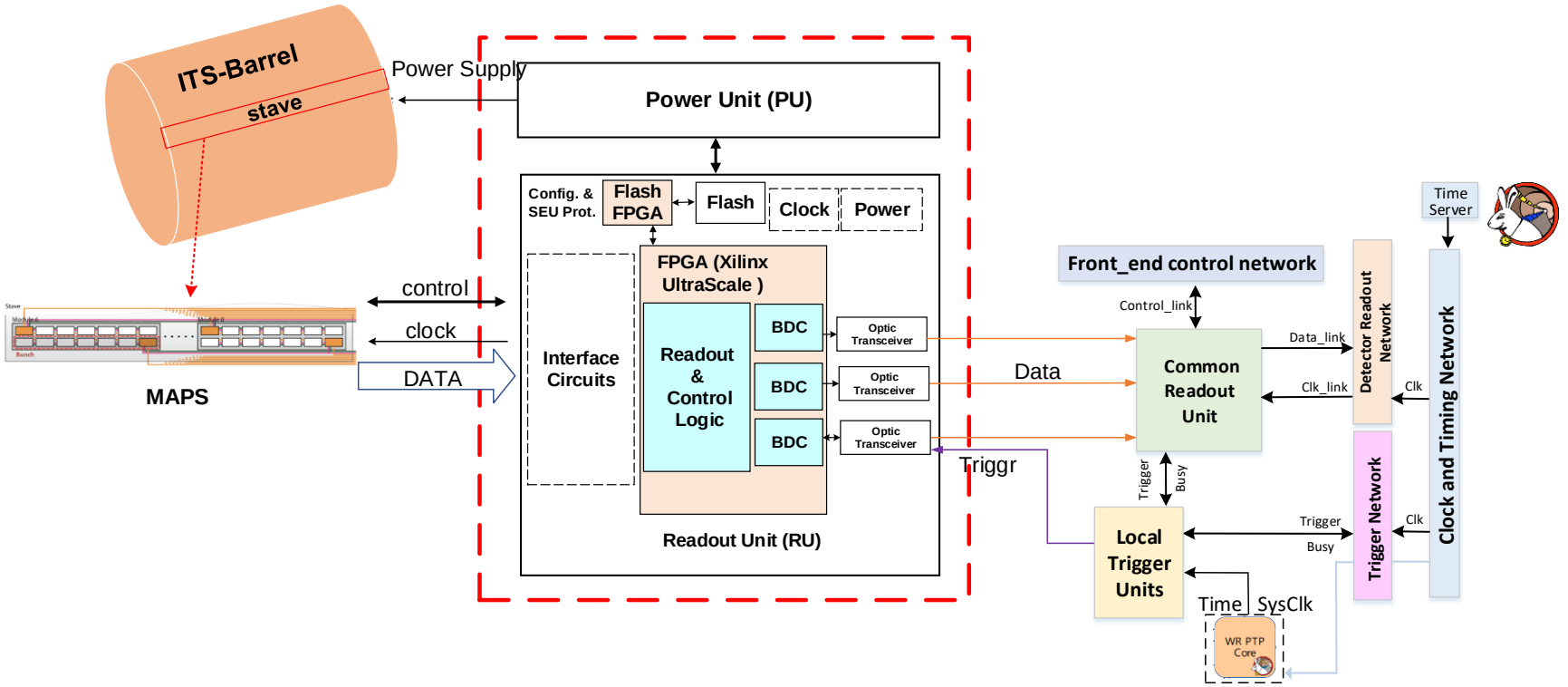
Scheme of electronics in barrel



Content

- Background
- Front end ASICs for pixelated detectors
- Readout system for pixelated detectors
- Our work on readout electronics
  - Front end
  - Readout chain
- Our work on DAQ and control system
- Conclusion

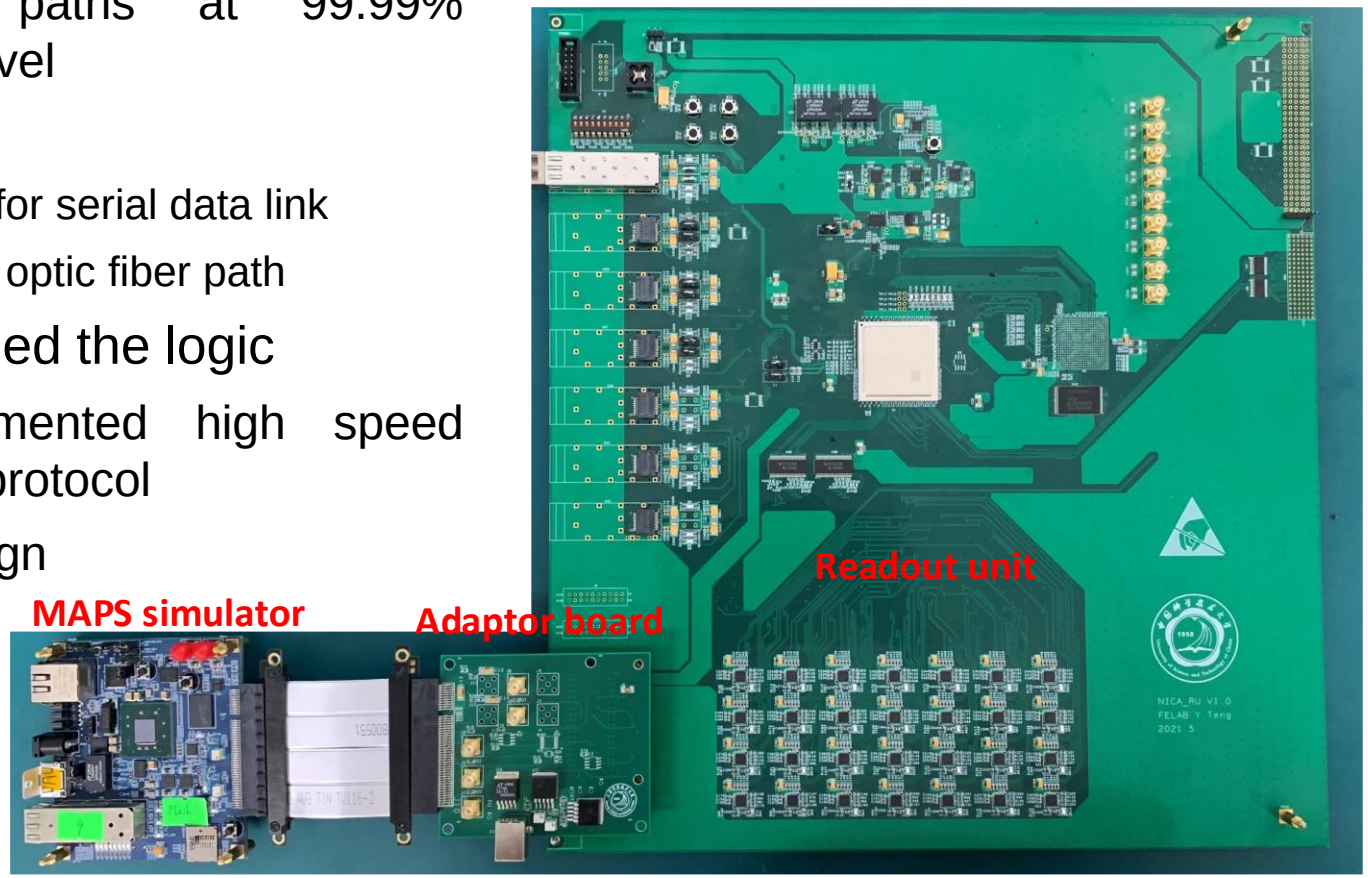
FPGA based Readout Unit



- Control and read out the data from MAPS stave
- SRAM-FPGA receives control/trigger signals and delivers packed data to CRU
- BDTC function integrated into the SRAM-FPGA
- A Flash-FPGA to monitor and protect the SRAM-FPGA from SEU based on scrubbing

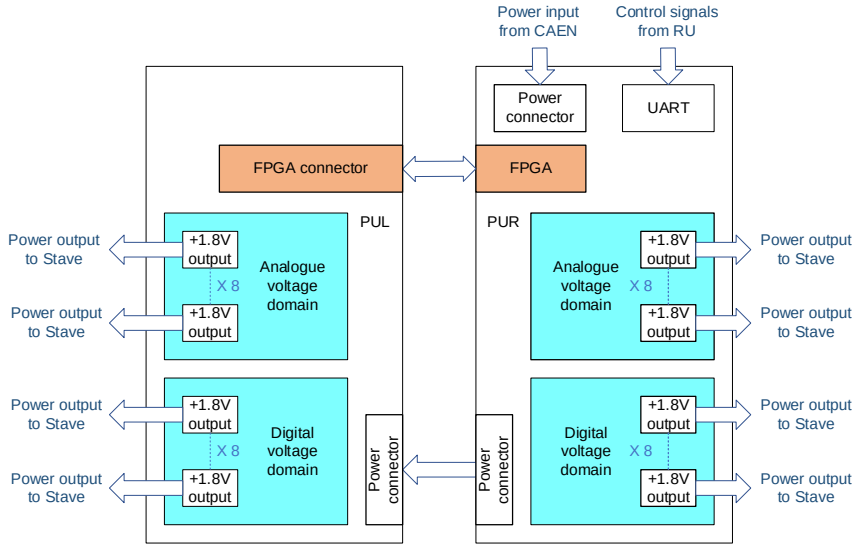
ITS-FPGA based Readout Unit

- Tested and verified the circuits
  - BER < 10^{-12} for serial data links and optic fiber paths at 99.99% condidence level
  - Data rates:
    - 400 Mbps for serial data link
    - 5 Gbps for optic fiber path
- Tested and verified the logic
  - FPGA implemented high speed data transfer protocol
  - Scrubber design

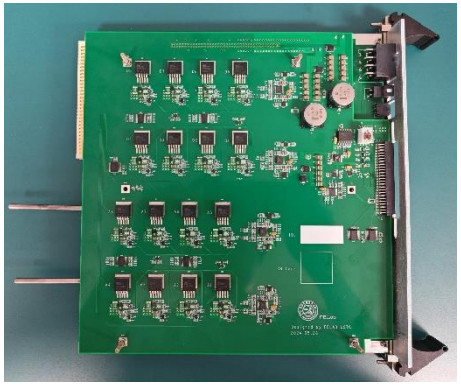


ITS-Power Board

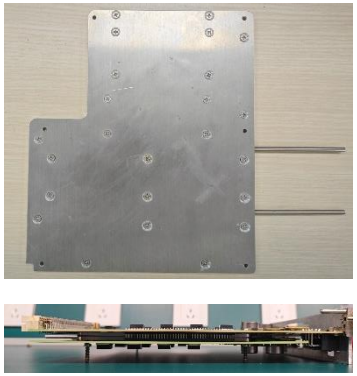
- One PB is composed by two independent PU (PUR and PUL)
- Each PU contains 8 channels of analogue output (1.8V/250mA) and 8 channels of digital output (1.8V/1.5A)
- A flash FPGA on PUR controls both PUR and PUL and is responsible for communication with RU



PUR



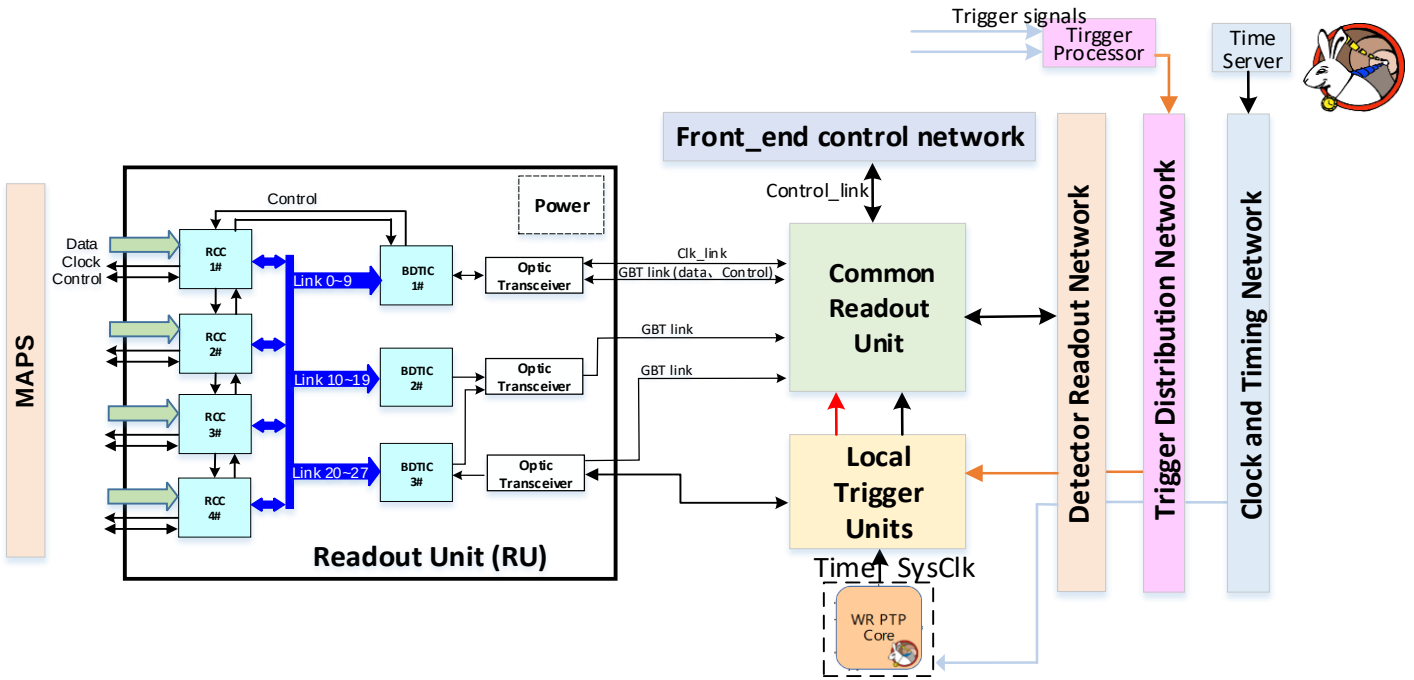
PUL



Cooling plate

Front Panel

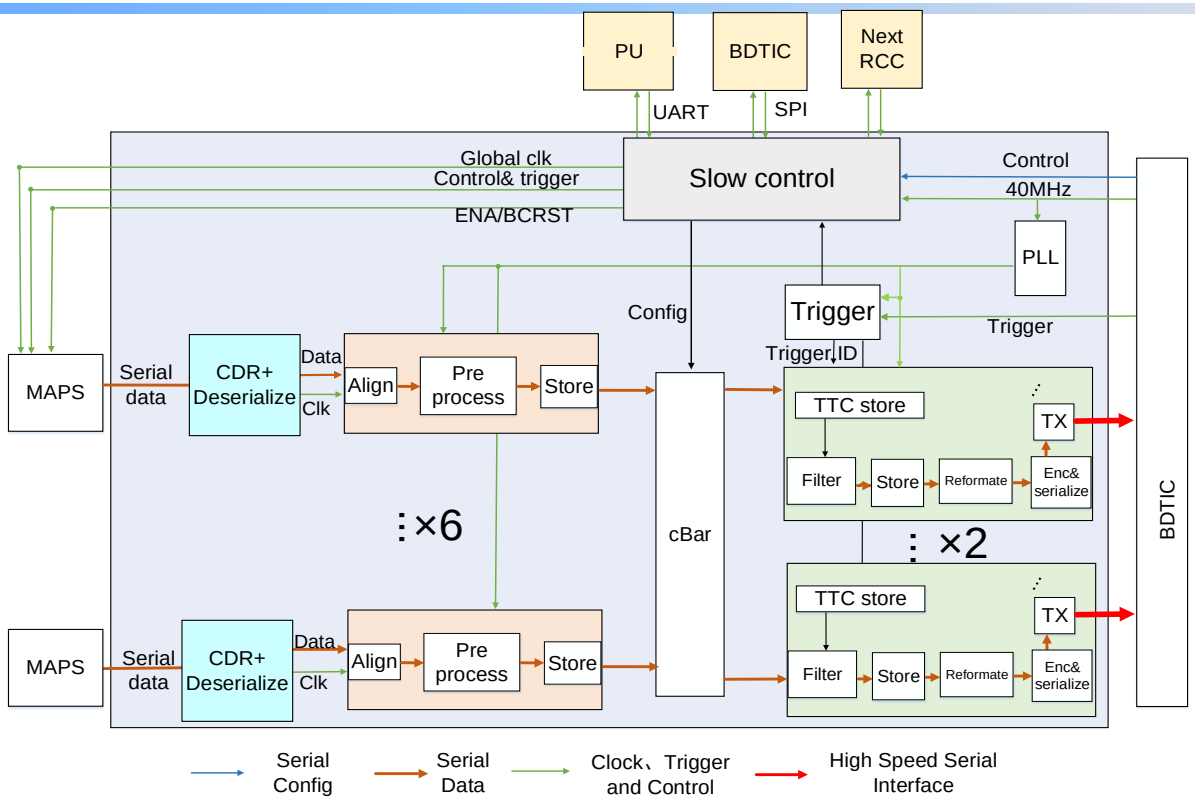
ITS- ASIC based RU



- ASIC group replace the function of FPGA, form the complete data and control link;
- **RCC: Readout and Control Chip**
  - ✓ MAPS data receive and processing, Slow control, Clock and Trigger
- **BDTC: Bi-directional Data-transceiver Chip**
  - ✓ high speed bidirectional data transfer
- Optical Transceiver : Laser-driver/receiver ASIC to modulate serial data on a laser

RCC ASIC

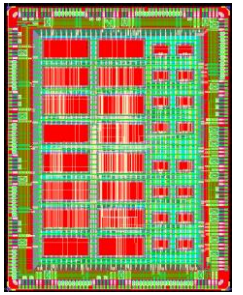
RCC: Readout and Control Chip

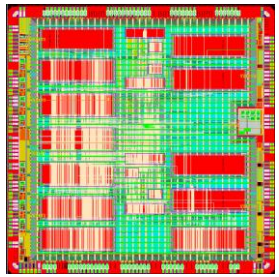


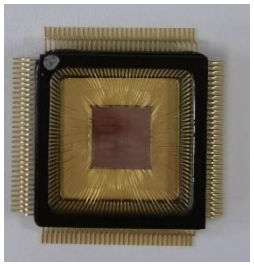
- RCC integrates the functionalities of Assembler, Buffer, Aggregator, and Data Packet processing for the MAPS detectors.
- Adjust and distribute control, trigger and clock information for MAPS/GBT/PU.
- RCC also optimizes the bandwidth utilization and reduces the number of required data links.

RCC ASIC

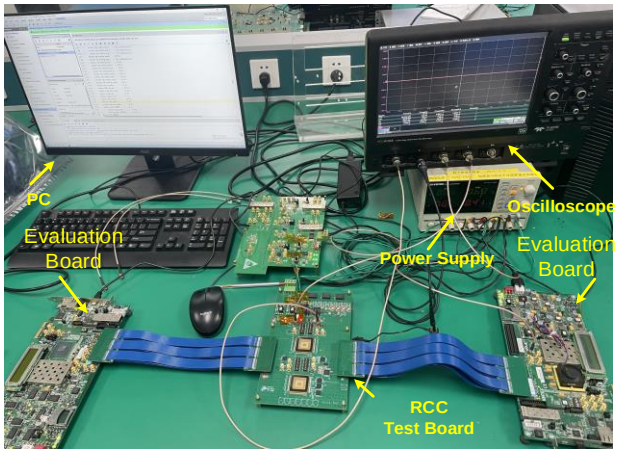
- MAPS Link:
  - ✓ Data link: 400 Mbps / 8 channels → 1.2 Gbps
  - ✓ Cfg link: 40 Mbps / Bi-directional
- Link to BDTC:
  - ✓ Data link: 160/320/640/1280 Mbps (configurable)
  - ✓ 1/2/4 channels
  - ✓ Cfg link: 80 Mbps
  - ✓ Trigger link :320 Mbps
  - ✓ Clock : 40 MHz
- Provides Control, Trigger and Clock information for the detector Realize the function of data reorganization
- Trigger / Trigger-less
- Integrated CDR & PLL
- SPI for BDTIC / UART for PU cfg & monitor
- SRAM ECC & Critical logic TMR protection





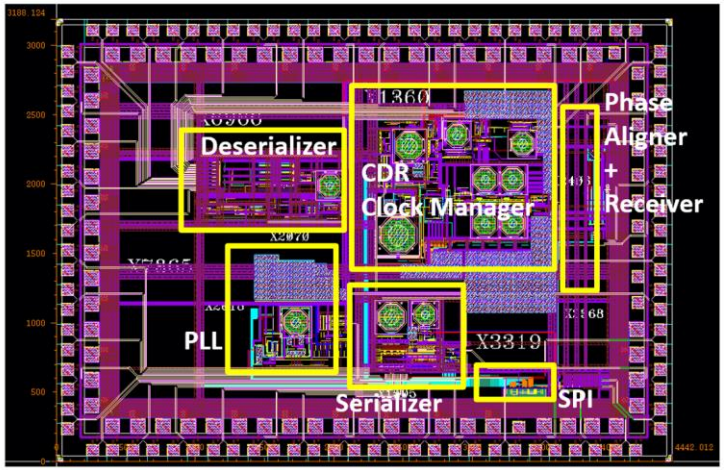


V0 V1

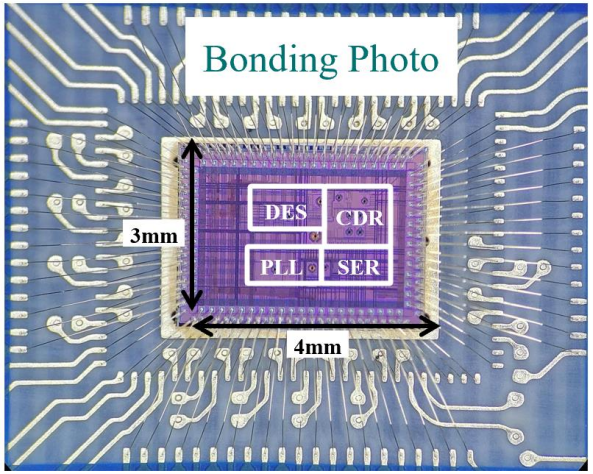


BDTC ASIC

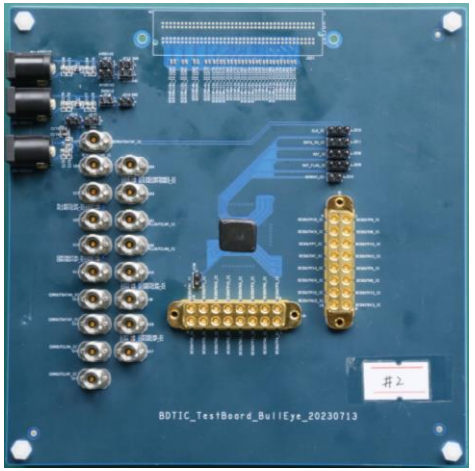
BDC: Bi-directional Data-transceiver Chip



Data Interface ASIC Layout



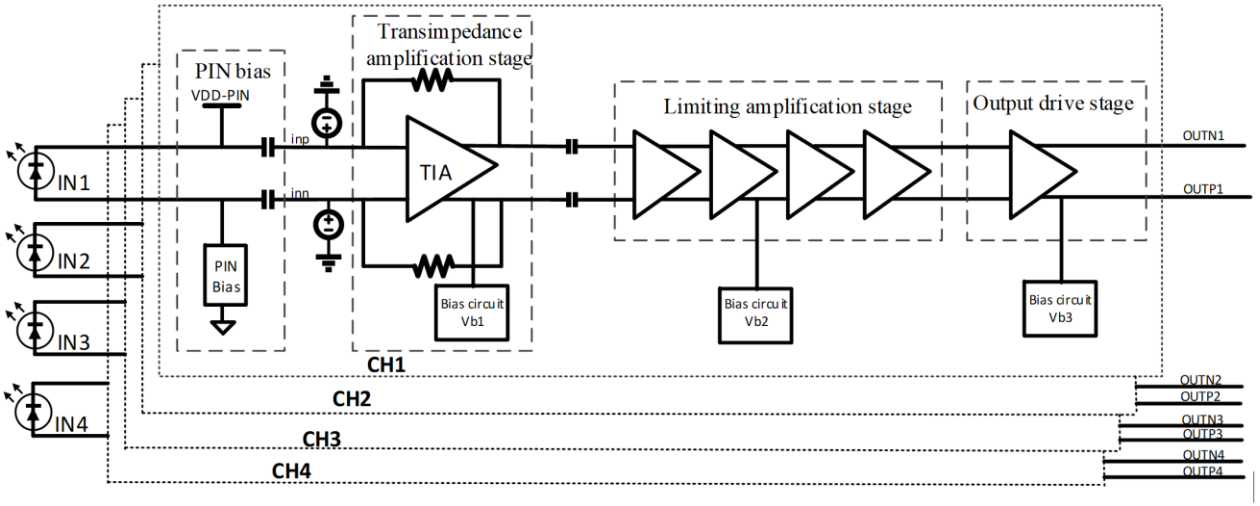
ASIC Bonding Diagram



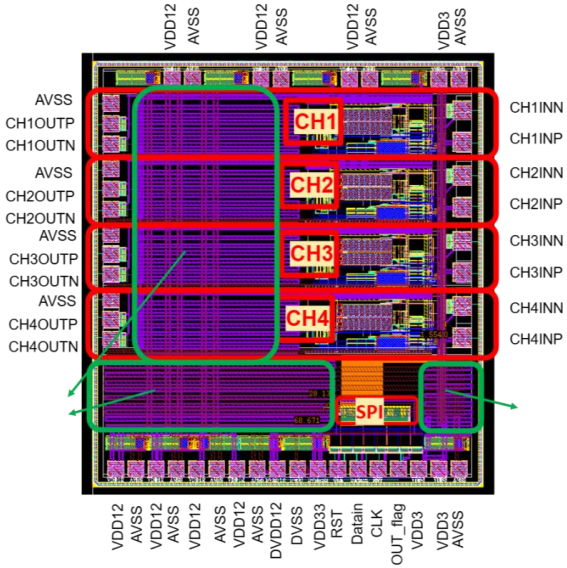
ASIC Test Board

- The first prototype of the data interface ASIC has been designed and verified, including the following analog cores.
  - 5.12 GHz PLL
  - 2.56 GHz Clock and Data Recovery (CDR)
  - 10.24 Gbps 16:1 Serializer
  - 2.56 Gbps 1:16 Deserialzier
- Based on 55nm CMOS Technology
- Die size: 3 mm x 4 mm 166 Pins

Optical Transceiver- Laser Receiver ASIC



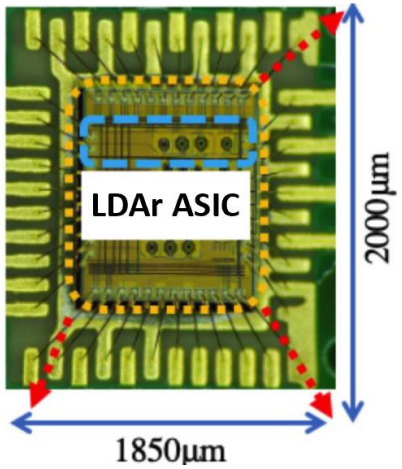
Block diagram of 4 channel x 2.56 Gbps TIA ASIC

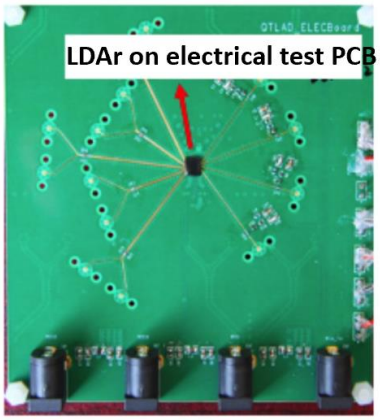


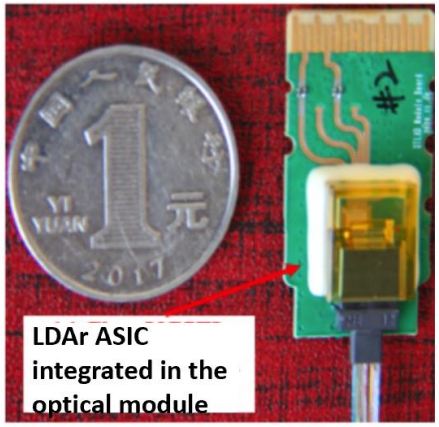
Layout of the TIA ASIC

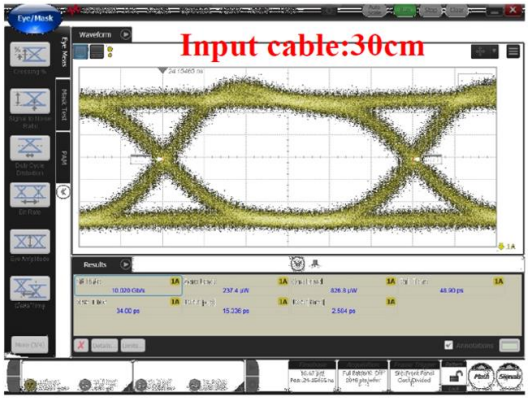
- The prototype of 4 channel x 2.56 Gbps TIA (Trans-Impedance Amplifier) ASIC has been designed.
- It is based on domestic 55 nm CMOS technology, with a die size of 1750 um x 1900 um.

Optical Transceiver- Laser Driver ASIC









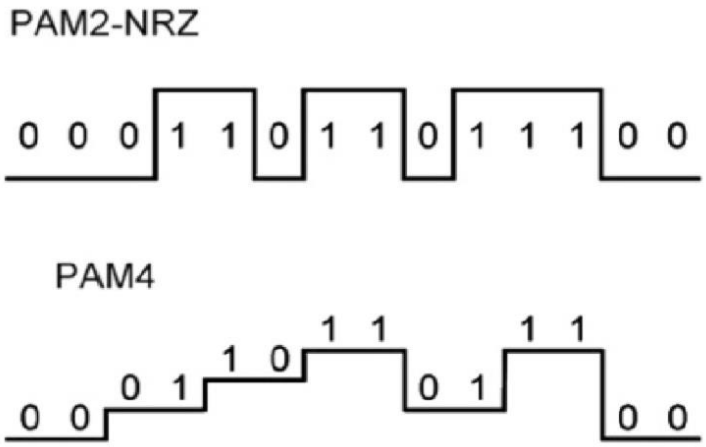
10 Gbps optical eye

LDAr ASIC Layout

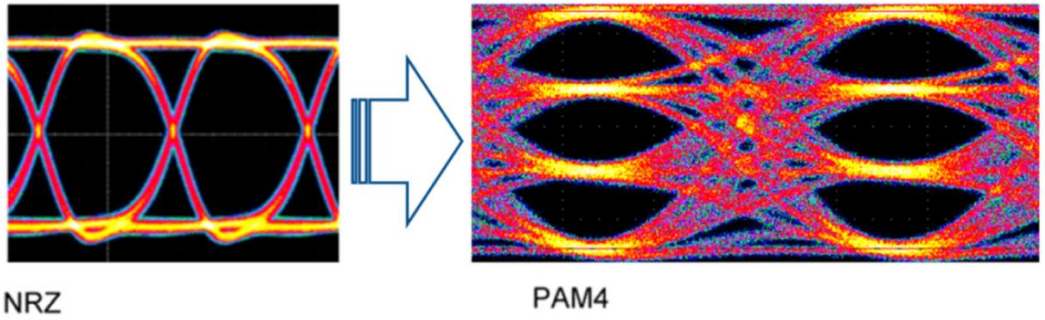
LDAr ASIC integrated in the customized array optical module (4Tx) for test

- Prototype of 10 Gbps high speed laser array driver ASIC (LDAr) has been designed and tested based on domestic 55 nm CMOS technology.
- 10 Gbps wide-open Tx optical eye has been captured and verified.
- Further optimization is going on.

Optical Transceiver- Higher Speed Research



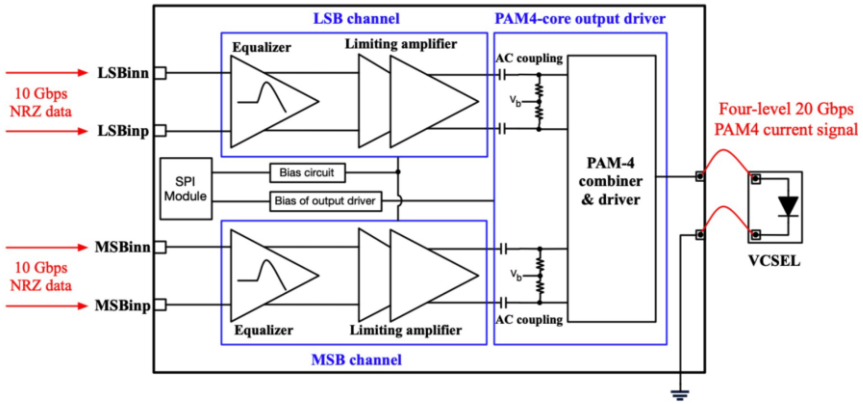
NRZ signal and PAM4 signal



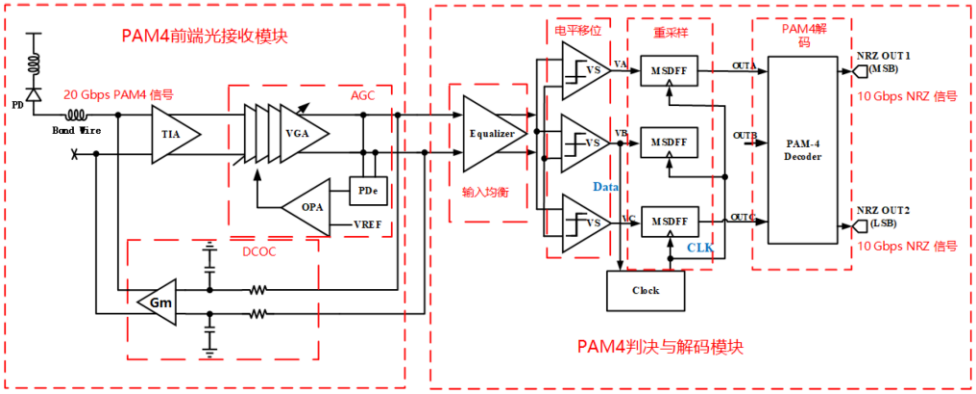
NRZ and PAM4 eyediagrams

- For higher speed optical data transmission development (two ways):
  - Use more peaking techniques in ASIC circuit design, and use more advanced process in ASIC manufacture for higher intrinsic analog bandwidth.
  - Use different signal modulation format, e.g. Pulse Amplitude Modulation 4-level (PAM4).

Optical Transceiver- Higher Speed Research



20Gbps/ch+ PAM4 VCSEL Driver ASIC Block Diagram



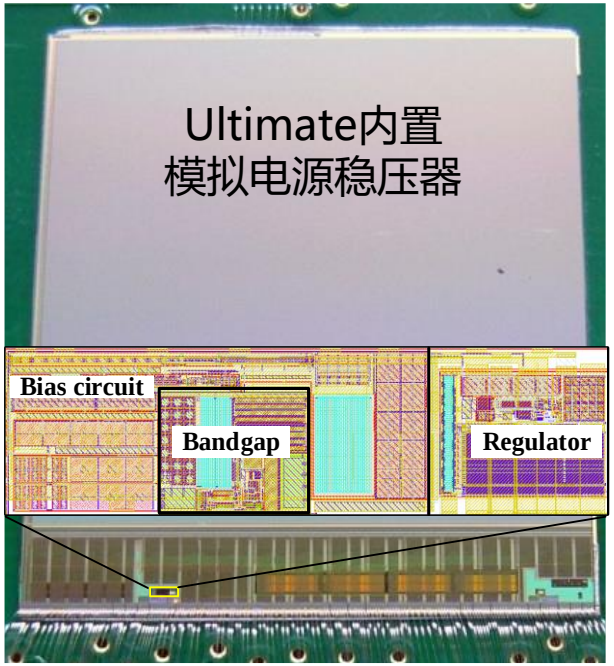
20Gbps/ch+ PAM4 Receiver ASIC Block Diagram

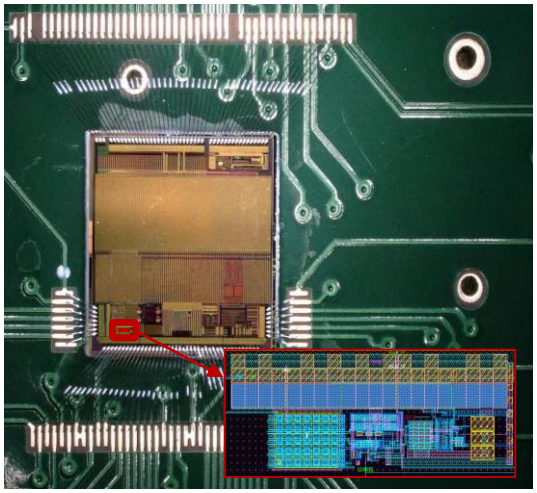
- PAM4 VCSEL Driver ASIC is under design. The core issue for this ASIC:
  - To combine and transform two regular NRZ signals into a 4 voltage level signal with enough amplitude and linearity.

- PAM4 Receiver ASIC is under design. The core issue for this ASIC:
  - To amplify the signal, and recover two NRZ signals from the PAM4 signal with enough bandwidth.

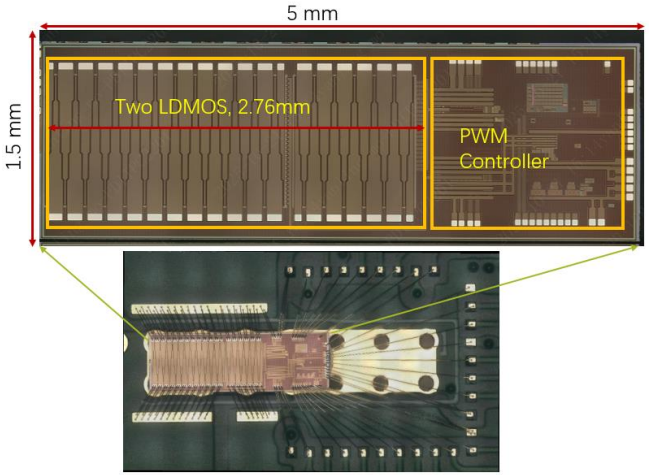
Radiation hard DC/DC & LDO

- Radiation hard DC/DC & LDO are important parts of readout electronics in particle physics experiments.

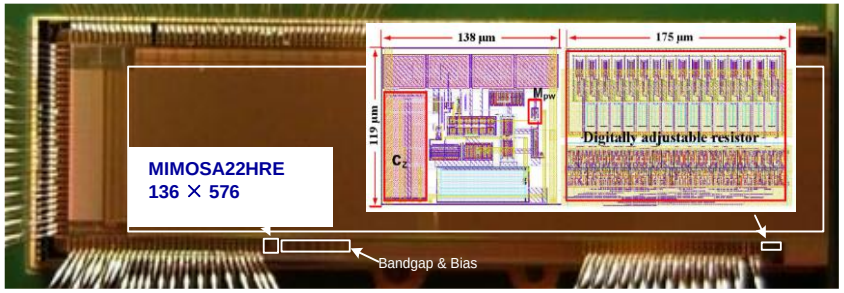




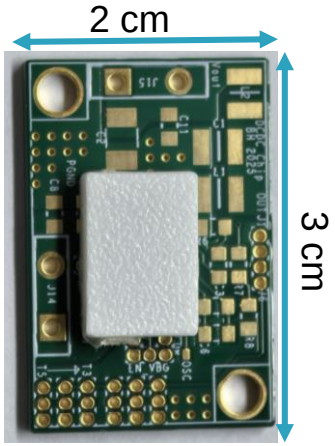
Taichupix内置电源稳压器



MIMOSA22HRE内置
钳位电压稳压器



- ❖ 抗辐照DC/DC转换器
  - 180nm高中低压混合BCD 国产工艺



Content

- Background
- Front end ASICs for pixelated detectors
- Readout system for pixelated detectors
- Our work on readout electronics
- Our work on DAQ and control system
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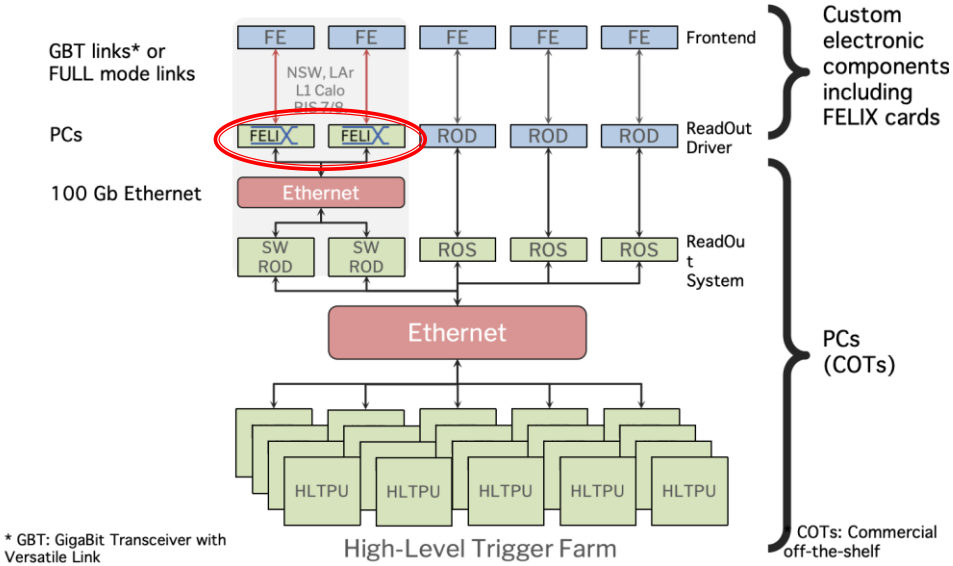
DAQ

- DAQ plays an important role in the whole electronics systems.
- Participated in LHC FELIX R&D, and in charge of the FELIX project of ATLAS upgrade supported by the DOE of U.S.A.

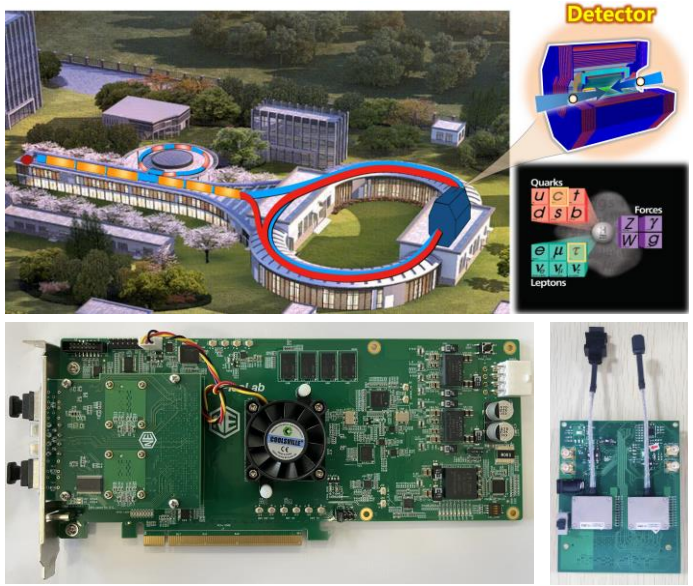


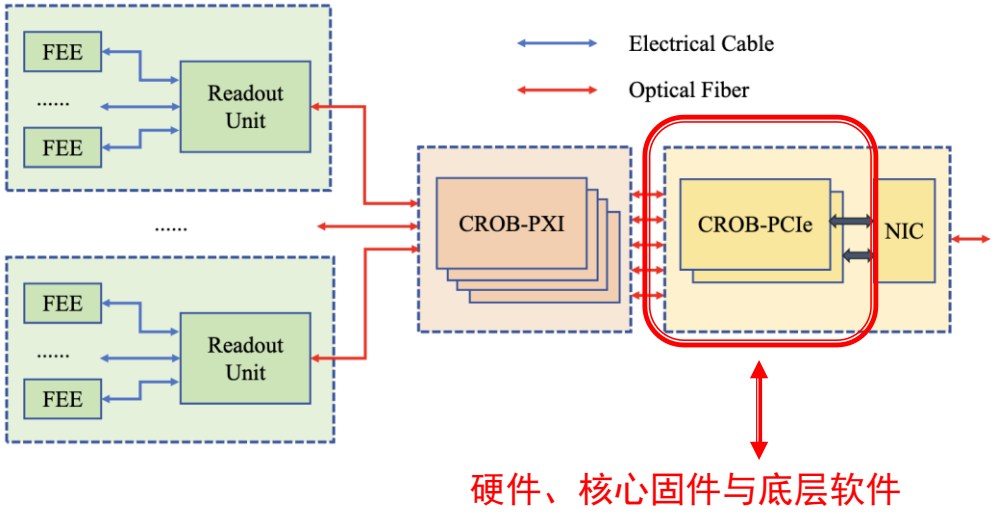
承担硬件研制，高速数据传输固件研发，及与多个子探测器的集成

应用于ATLAS，sPHENIX，CBM，NA62，ProtoDUNE-SP

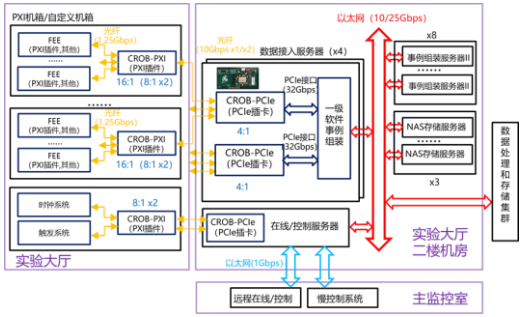
DAQ

- R&D of high density high speed data aggregation module (24 channel/module) has been finished.
- Fabrication of the first bunch (10 modules) are finished, and are used in the R&D project of STCF.

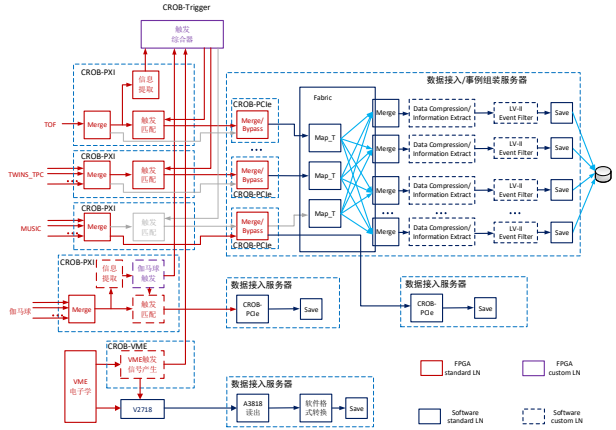




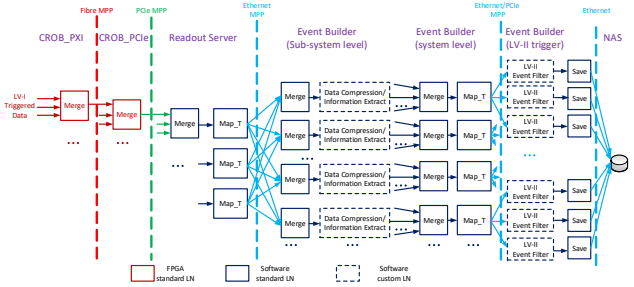
DAQ



CEE-DAQ



HIRIBL-DAQ

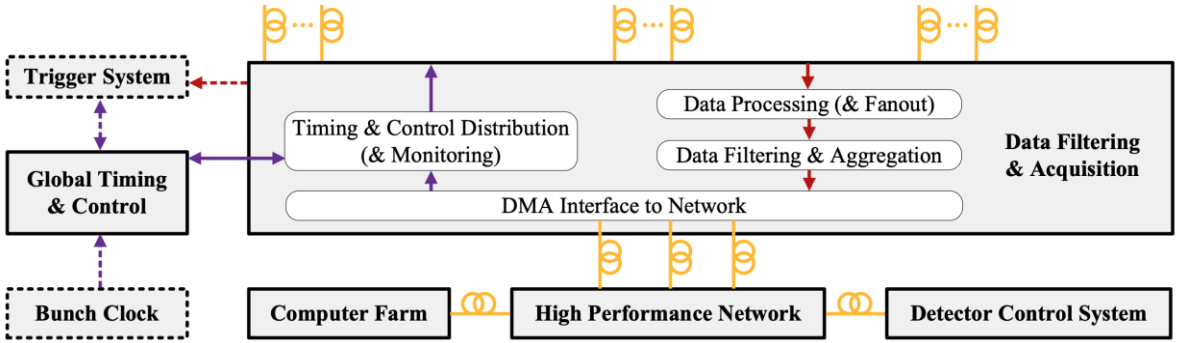


STCF-DAQ

- Undertook design tasks:
  - Cooling Storage Ring External-target Experiment (CEE) data acquisition system
  - High Intensity Accelerator Facility – High Intensity Radioactive Ion Beam Line (HIAF-HIRIBL) data acquisition system
  - Super Tau-Charm Facility (STCF) detector spectrometer data acquisition system

- Full-stack development capabilities across hardware, software, and FPGA firmware
- Architecture：D-Matrix，an independently developed general streaming data acquisition architecture
- DAQ System Features:
  - Work mode: trigger / trigger-less
  - Data rate：~30GB/s
  - Event rate：10kHz ~ 7MHz

Structure of the H-NS DAQ



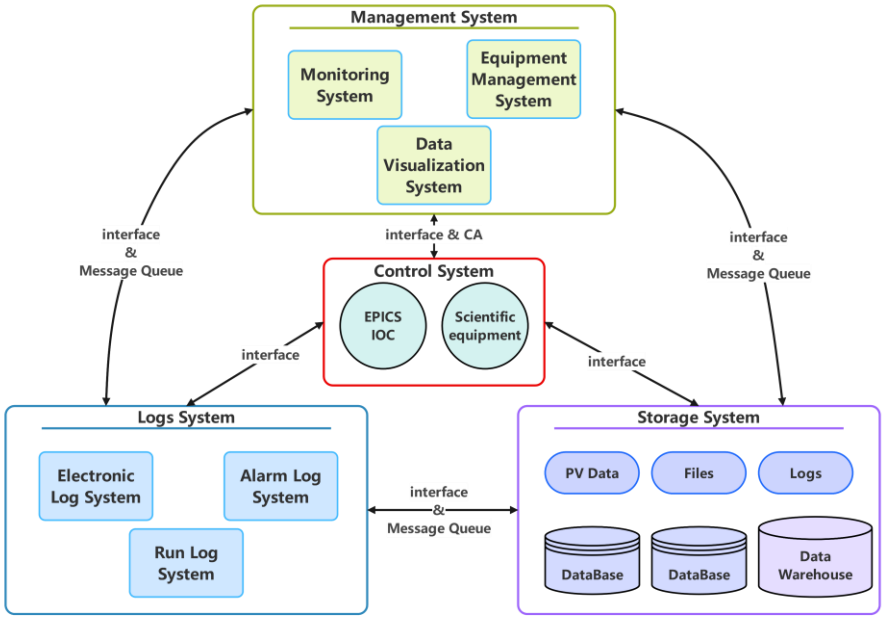
Baseline方案
基于PCIe的无触发读出架构
200Gbps/板卡

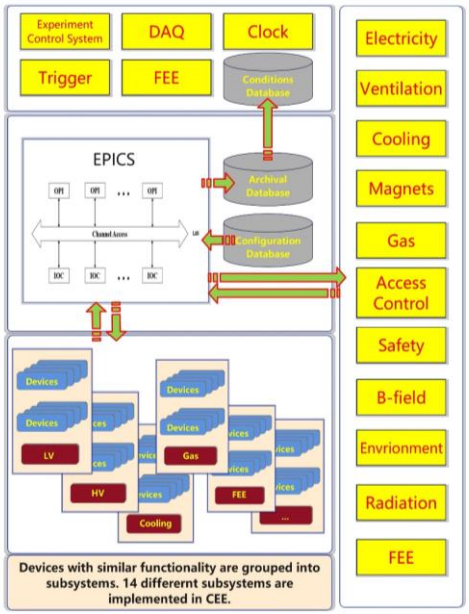
同步研究MicroTCA+RDMA的无触发读出架构（具备切换至MicroTCA+PCIe的硬件触发的灵活性）

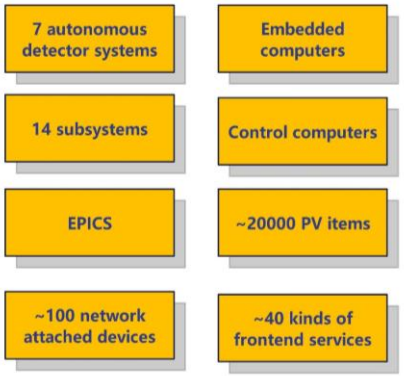
- Feature:
  - R&D based on domestic chips/components
  - High density (≥24ch/module), supporting10/25 Gbps/ch
  - Unified DAQ architecture, compatible with application using PCIe/RDMA
  - Computer farms for event building based on Heterogeneous Computing: CPU+GPU / CPU+FPGA

Architecture for Detector Control System

- Ensure the safe and stable operation of all sub-systems.
- Achieve distributed real-time control with high modularity and scalability.
- Provide efficient data management and intelligent alarming functionalities.
- Support flexible experiment configuration and rapid parameter archiving.
- Integrate intelligent data analysis and visualization tools into the user interface(GUIs/HIMIs).

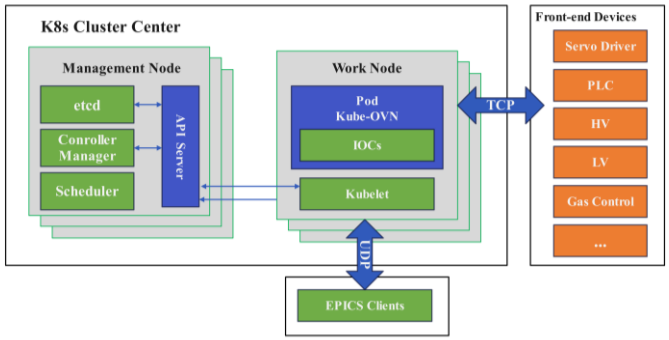




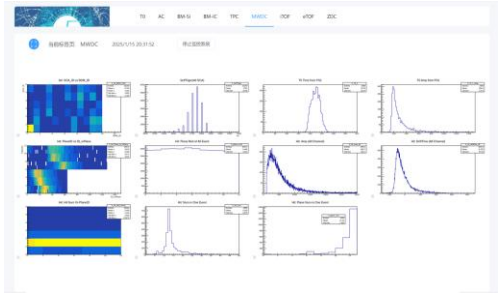


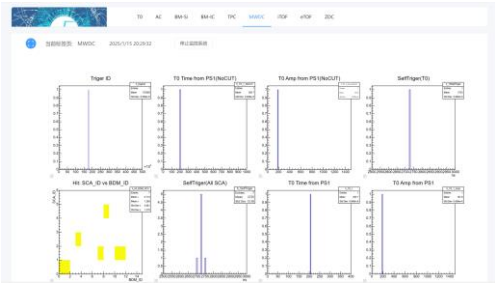
Key Techniques applied for DCS

- The control system adopts EPICS architecture, achieves containerized deployment, enabling flexible scalability and simplified management
- Hybrid database is designed for multiple data sources, enabling efficient storage and archiving
- Introducing CI/CD and DevOps into nuclear detector control systems enables automated deployment and continuous delivery, ensuring high reliability
- Web-based QA(Online) provides cross-platform, accessible collaborative environment

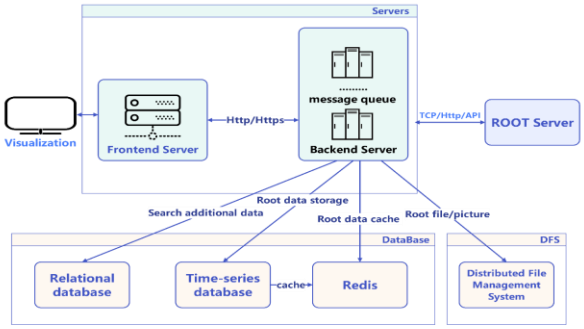


Containerization deployment for high stability

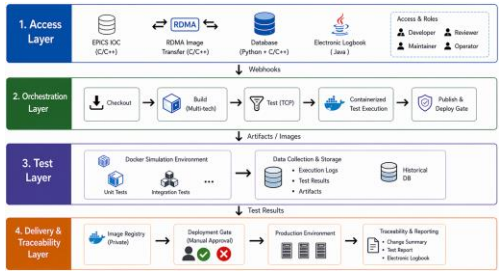


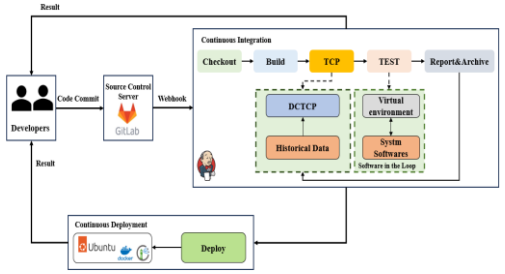


DAQ Online/offline monitoring and operation



Hybrid database architecture





Conclusion

- Pixelated silicon detectors are key parts in H-NS.
- MAPS has been applied in high-energy particle physics experiments, and is one key solution for ITS in future domestic experiments of this domain.
- LGAD is under fast development, and several readout ASICs have achieved good performance, such as ALTIROC, ETROC, EICROC. We have also finished the prototype ASIC -- LATIC, which is expected to be used.
- Data transfer is one of the key techniques of readout electronics for pixelated detectors and other high-granularity detectors.
- FPGA devices were widely used in this domain, while ASIC-based transmission from the front end is an important direction.
- High precision front-end and high speed interface will be built based on ASICs, combined with DAQ and detector control system, forming a full chain with our own intellectual proproteins.

Thanks