ATLAS High Granularity Timing Detector Upgrade

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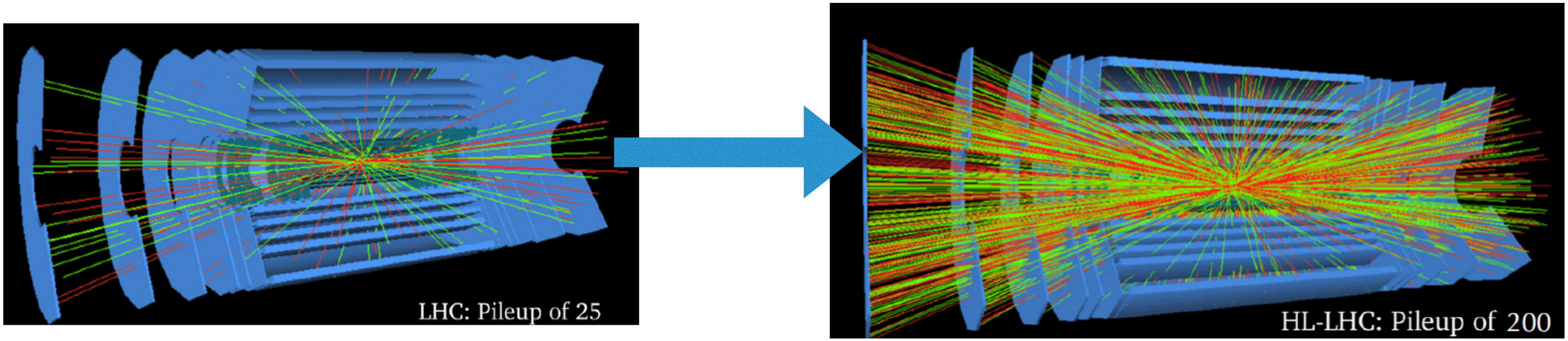
ATLAS EXPERIMENT

The High-Luminosity-LHC Challenges to Detectors

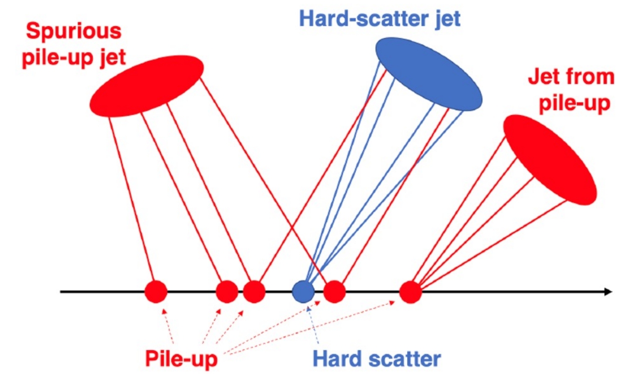
- High Luminosity LHC upgrade will happen in ~5 years
- One order of magnitude increase in instant luminosity compared to now



Current detectors cannot cope with such large rates, need:
Larger granularity
Faster trigger rates
New technologies (fast timing)

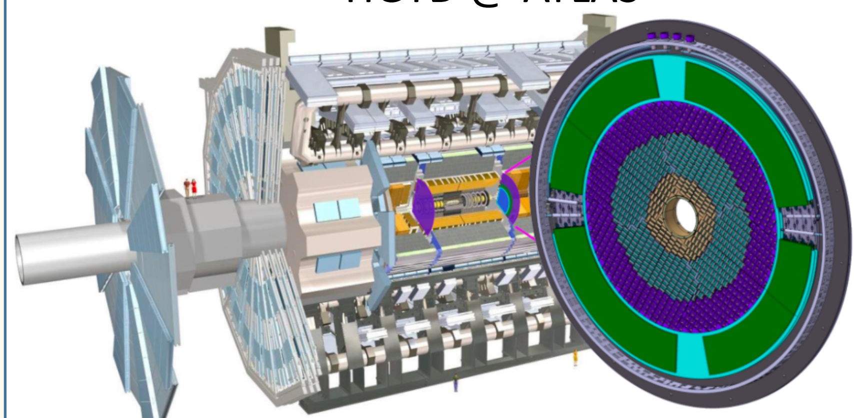
High Granularity Timing Detector (HGTD)

- **HGTD aim to reduce pileup contribution at HL-LHC**
  - **Timing resolution is required to be better than 30 ps (start) - 50 ps (end) ps per track**
- **6.4 m^2 area silicon detector and ~ 3.6 $\times$ 10^6 channels**
- **High Granularity: Pixel pad size: 1.3 mm $\times$ 1.3 mm**
- **Radiation hardness : 2.5×10^{15} N_{eq} $/cm^2$ and 2 Mgy**



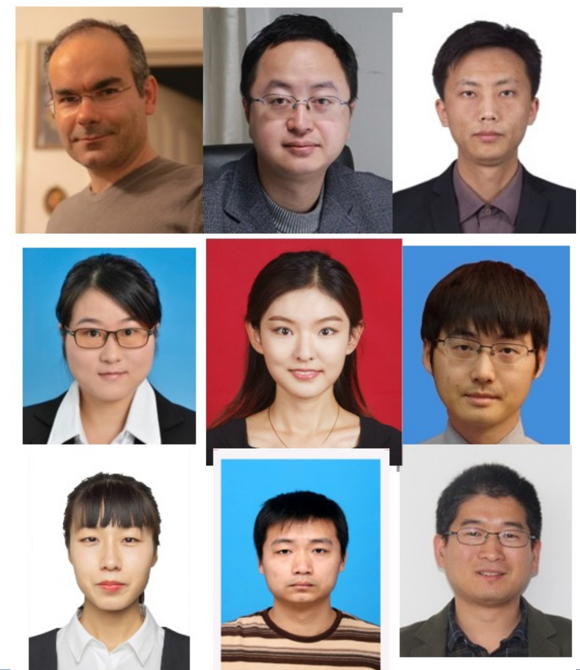
- **China team is making key contributions to HGTD**
  - **100% LGAD sensor (90% IHEP + 10% USTC)**
  - **44% detector assembly (34% IHEP + 10% USTC)**
  - **100% front-end electronics board (IHEP +NJU)**
  - **~33% flex tail (SDU)**
  - **50% ASIC testing (IHEP)**
  - **>16% high-voltage electronic systems (IHEP+ SDU)**
  - **Software and performance (USTC, IHEP)**

HGTD @ ATLAS



ATLAS HGTD project： China team's leadership

- China team is playing an leading role in HGTD detector project
  - I am severing as deputy project leader (2025-2027)
  - 2021-2025, Joao was HGTD project leader.
  - 5 person served as Level-2 convener
  - 3 person served as Level-3 convener

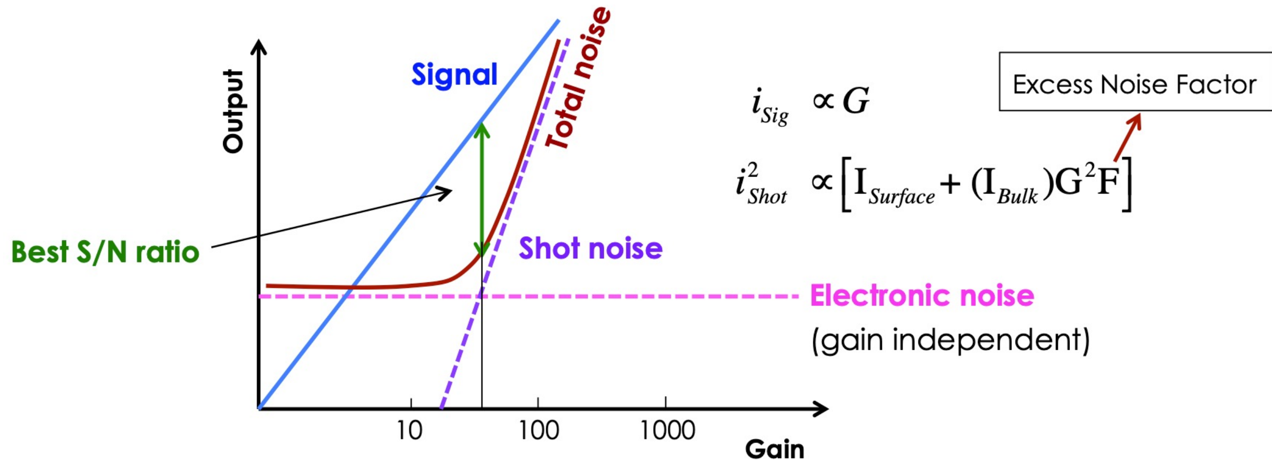


Low Gain Avalanche Detectors (LGAD)

- Compared to APD and SiPM, LGAD has modest gain (10-50)
- High drift velocity, thin active layer (fast timing)
- High S/B, no self-triggering

$$\sigma^2_{jitter} = \left(\frac{t_{rise}}{S/N}\right)^2$$

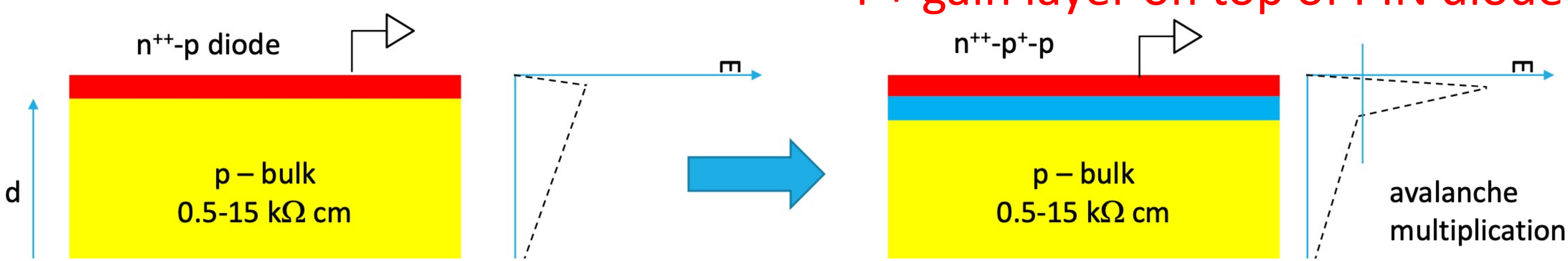
- **Modest gain to increase S/N**
- **Thin detector to reduce t_{rise}**



Conventional PiN diode

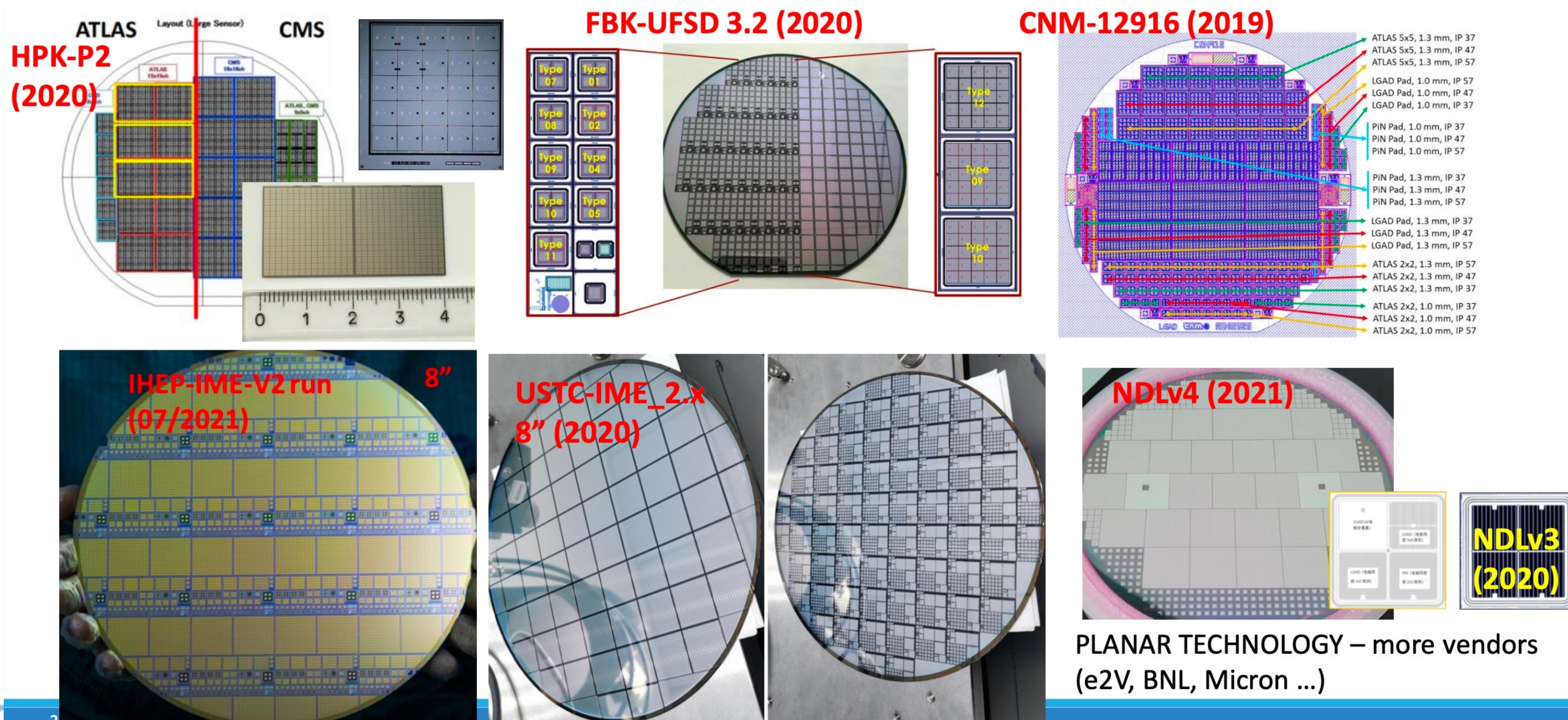
LGAD

P+ gain layer on top of PIN diode



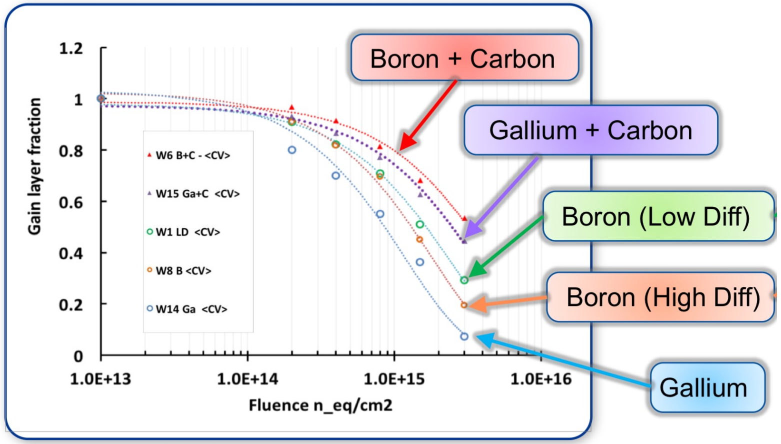
Latest prototypes produced by different vendors

- Lots of prototypes R & D in LGAD in last few years, active vendors includes:
  - IHEP-IME (China), USTC-IME (China), IHEP-NDL(China), FBK (Italy), CNM (Spain), HPK (Japan) …

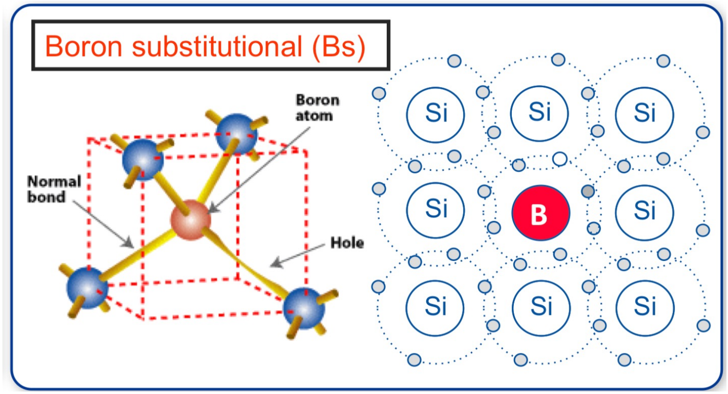


Challenge : LGAD sensor radiation hardness

- 2021, RD50, CMS and ATLAS confirmed Single Event Burnout (SEB) effect in testbeam
  - The key to avoid SEB is reduce the acceptor removal, reduce the operation voltage

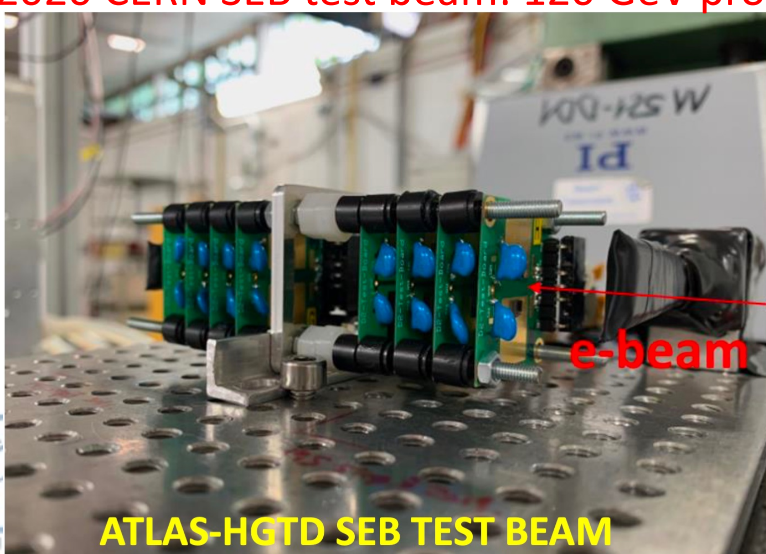


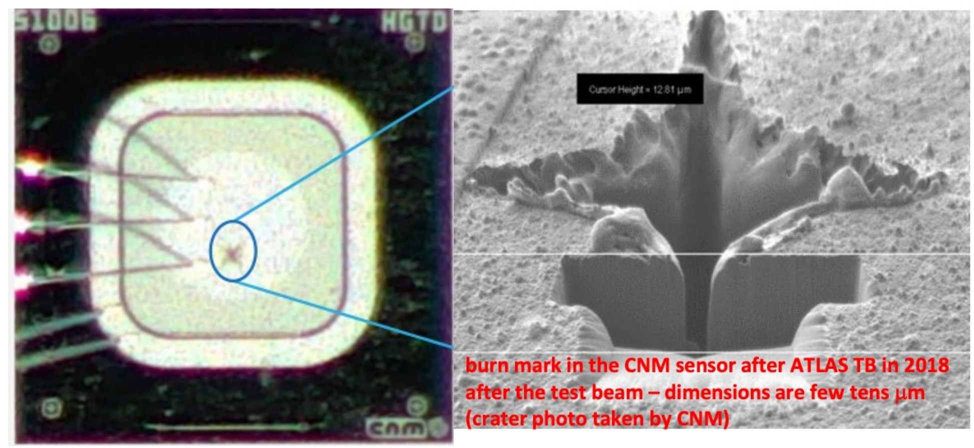
[G.Paternoster, FBK, Trento, Feb.2019]



Single Event Burnout (SEB) effect

2020 CERN SEB test beam: 120 GeV proton

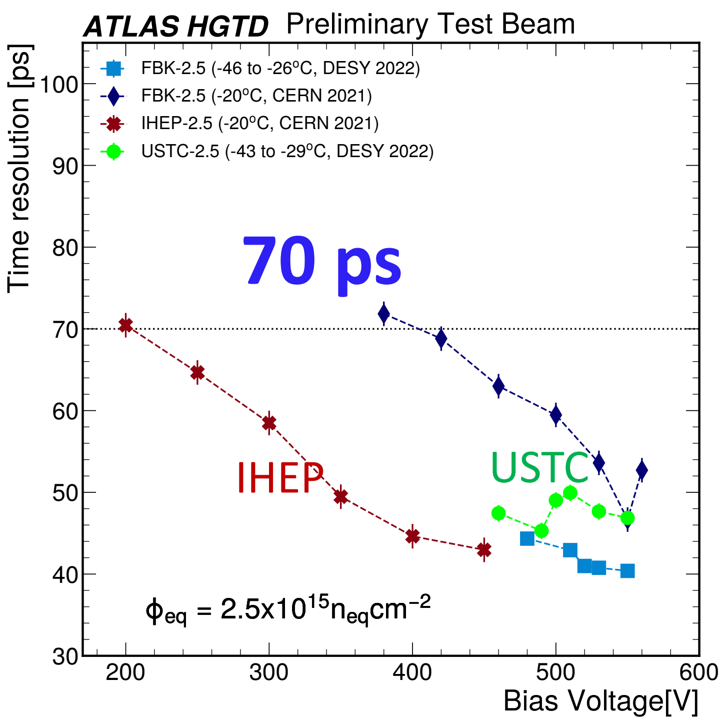


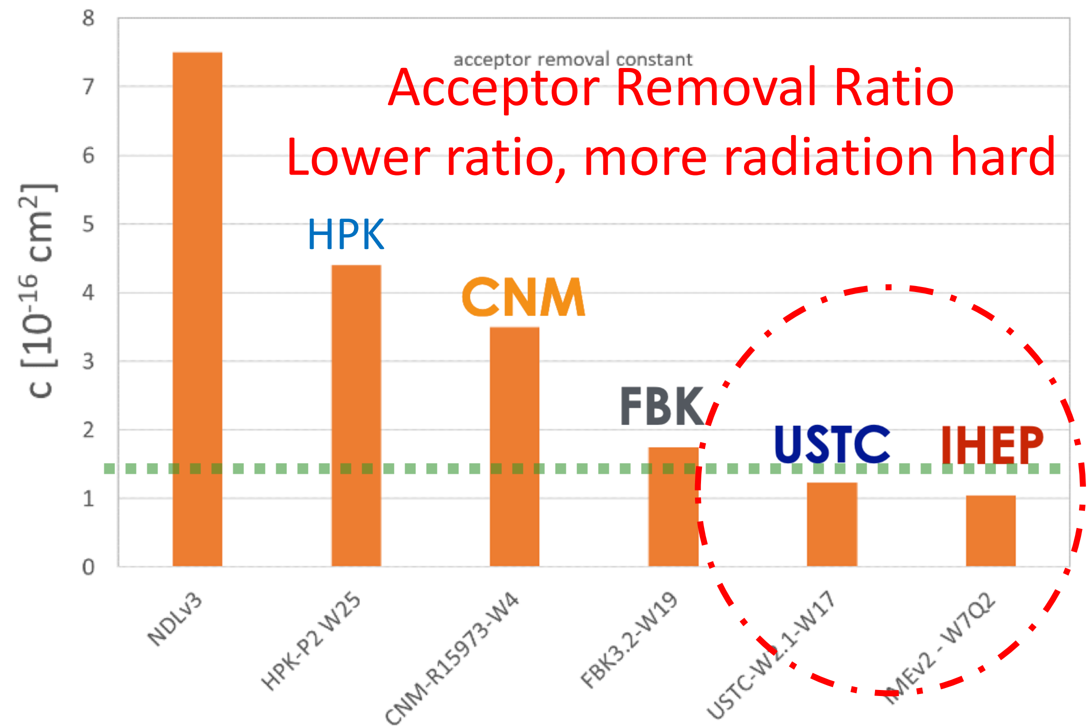


LGAD sensor after Irradiation

- IHEP-IME LGAD with carbon-enriched doping
  - 34 fabrication steps, all masks and processes designed by IHEP, fabricated at IME
  - Significantly lower acceptor removal ratio, the most radiation hard
- After $2.5\times10^{15}\ n_{eq}/cm^2$, IHEP LGADs can operated much below 550 V

→ avoid single event breakdown

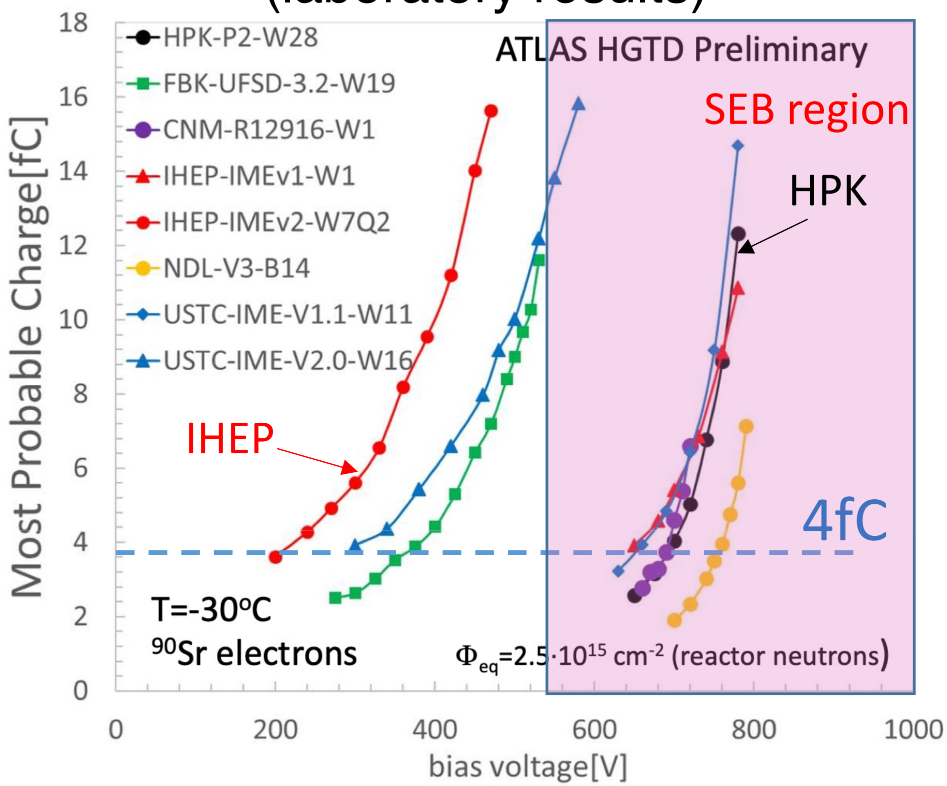




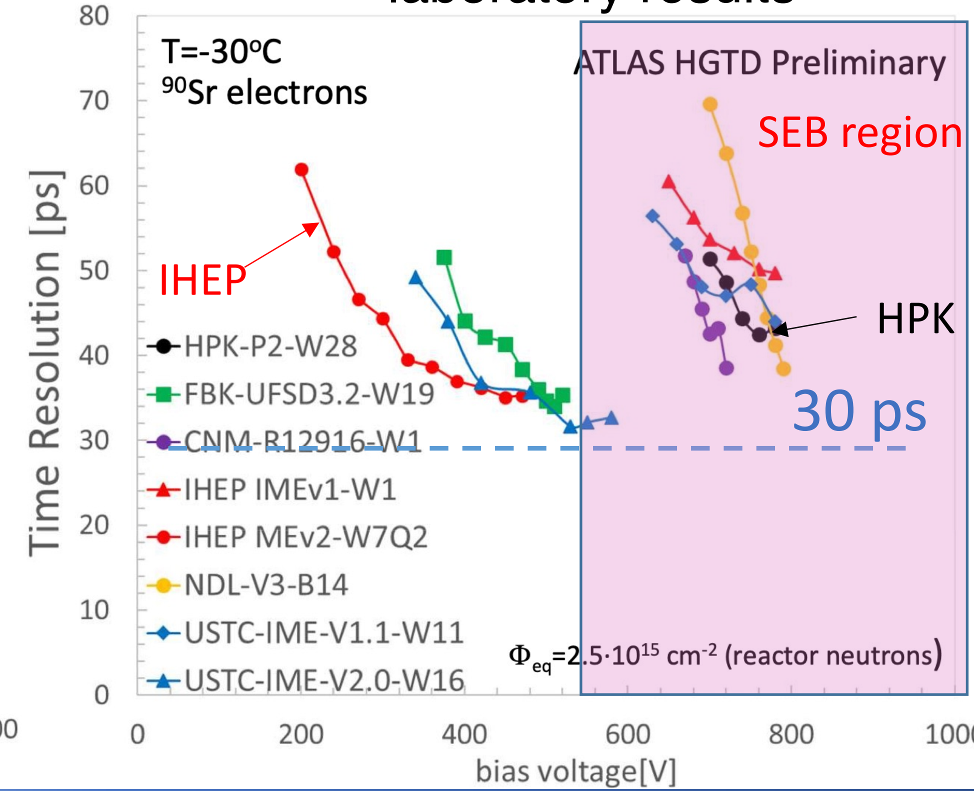
Performance of various LGAD prototypes at 2.5e15 cm^{-2} fluence

- Carbon enriched LGADs fulfil HGTD sensor requirements after irradiation
- Carbon-enrichment LGAD allows the sensors to be operated at low voltages
  - Single event break down (SEB) may happen if Operation Voltage >550V

Time resolution of LGADs Vs Bias Voltage
(laboratory results)



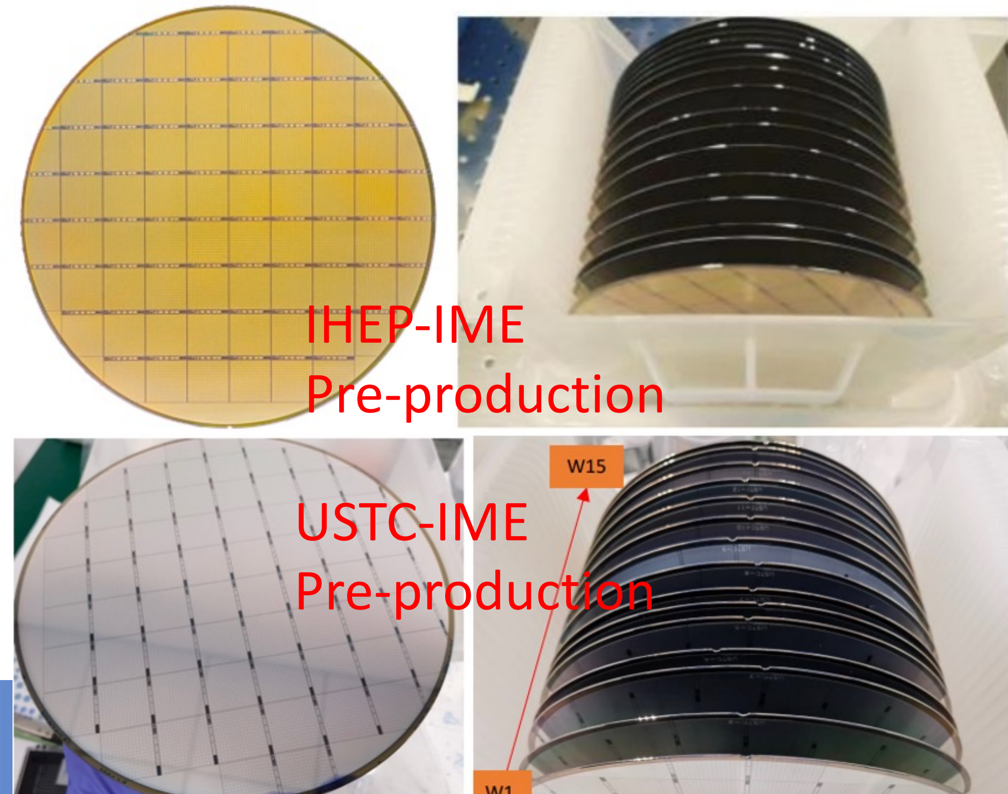
Charge collection Vs bias voltage
laboratory results



LGAD sensors

- CERN chosen IHEP-IME in HGTD sensor tendering, contract signed in 2025
  - Won the competition with Hamamatsu (Japan) and FBK (Italy)
- First time domestic silicon sensor was used by CERN in LHC experiment
- The production plan:
  - IHEP-IME: 90% (66% from CERN tendering+24% in-kind contribution): ~8 m^2
  - USTC-IME: 10% in-kind contribution

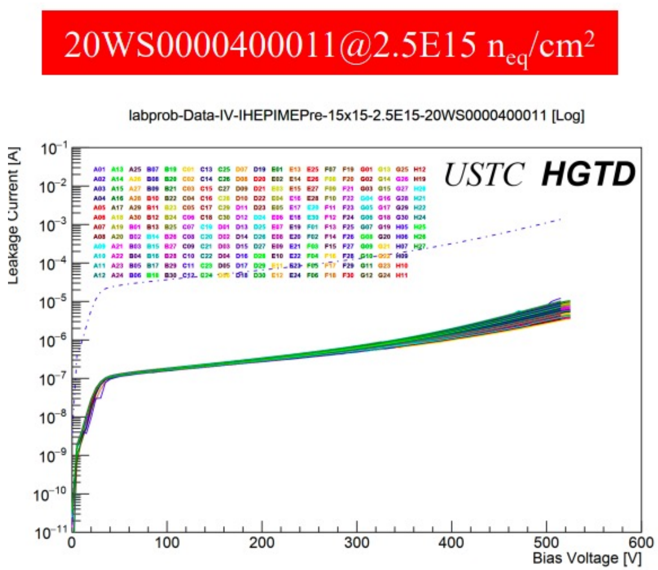
IHEP-IME sensor photo @CERN ATLAS point-1



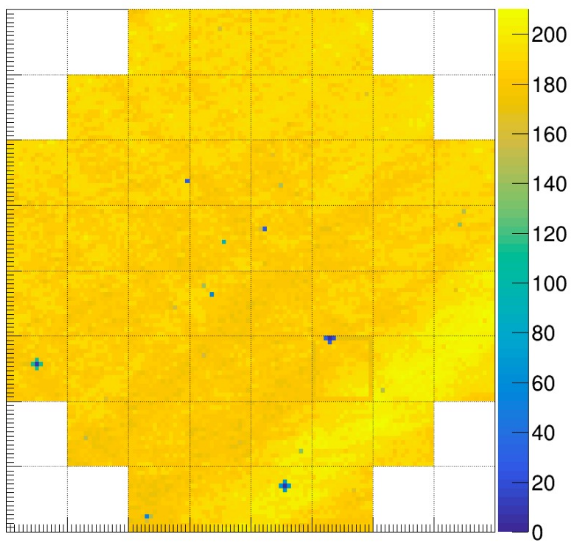
LGAD sensor pre-production

- IHEP and USTC have completed the pre-production
- Good uniformity before and after irradiation

LGAD current after irradiation

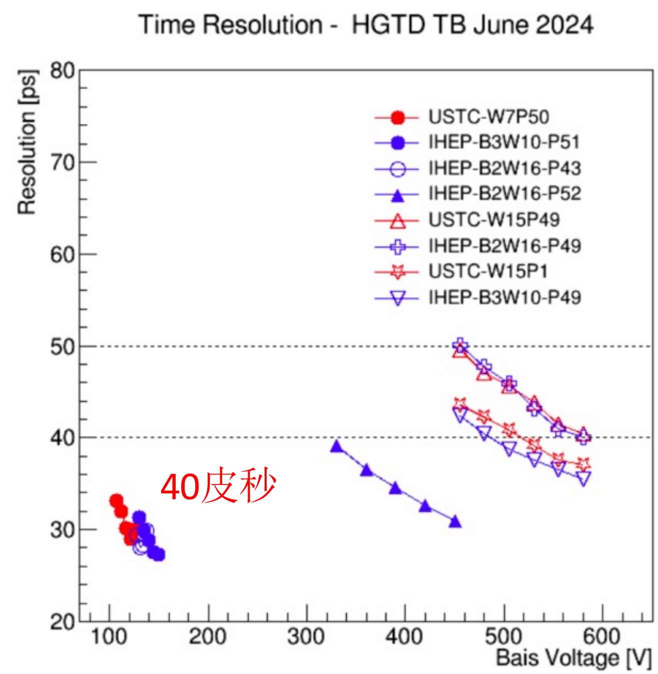


VBD uniformity



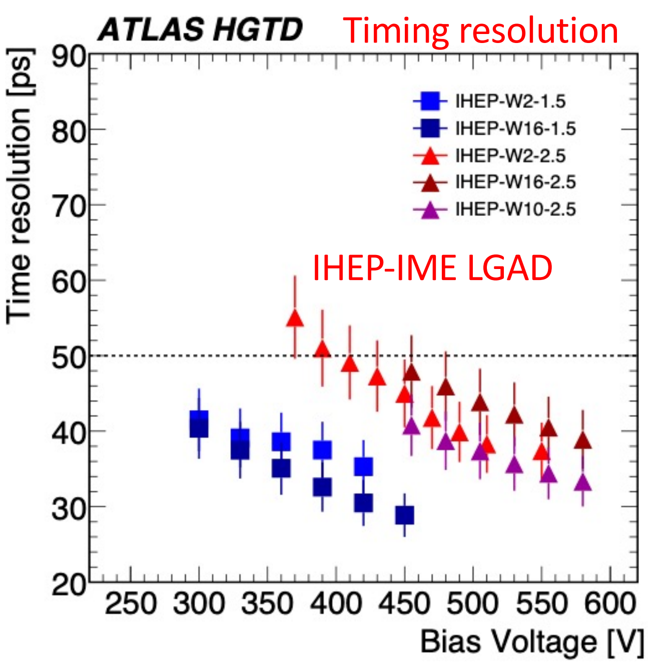
V_{BD} Map

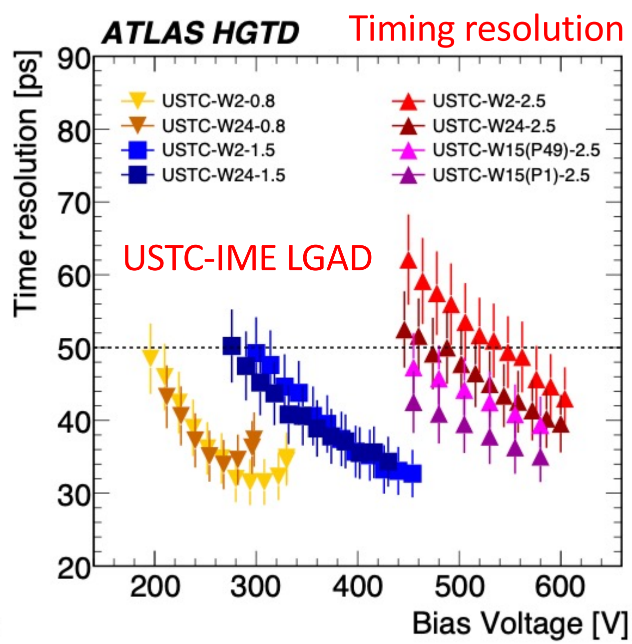
Timing resolution

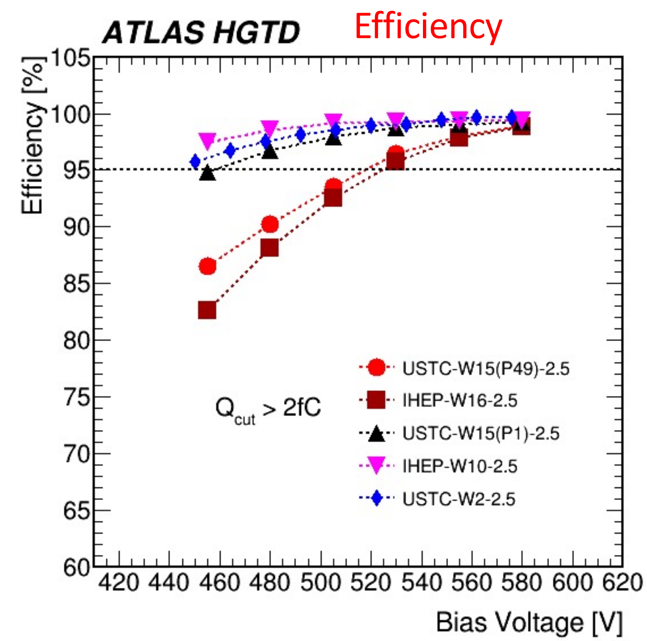


LGAD sensor pre-production: test beam result

- After irradiation, pre-production sensors still reached ~30ps， efficiency >95%
- Paper is coming out: https://arxiv.org/abs/2512.01855

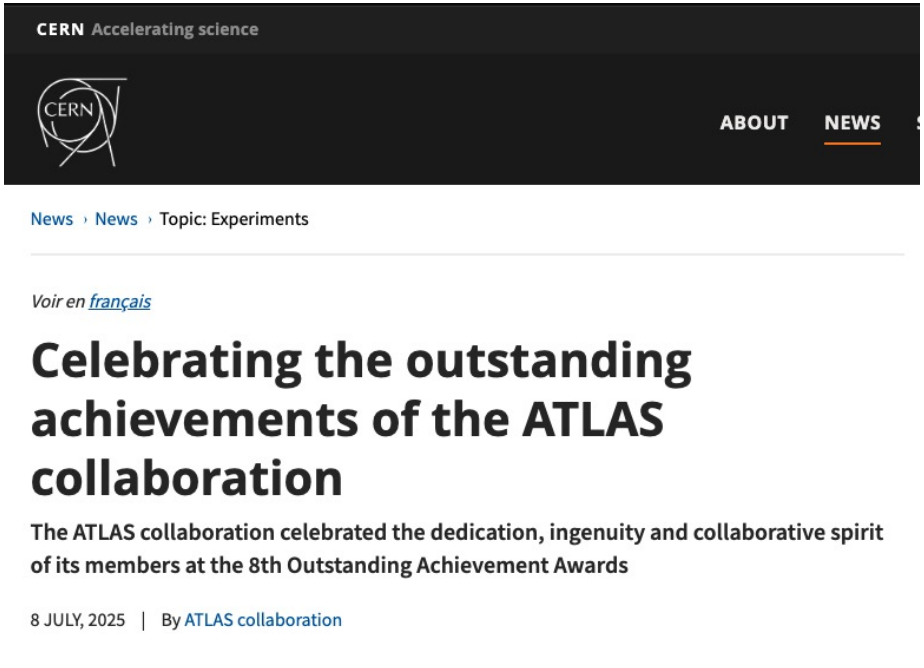






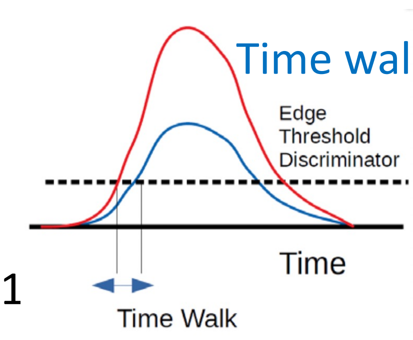
ATLAS Outstanding Achievement Award

- 3 IHEP and 1 USTC members won ATLAS outstanding achievement award
  - The list of ATLAS award for HGTD project: Bojan Hiti (Ljubljana), Alissa Howard (Ljubljana), Xuewei Jia (Munich MPI), Mengzhao Li (Beijing IHEP), Chihao Li (Michigan), Kuo Ma (Hefei), Theodoros Manoussos (CERN), Weiyi Sun (Beijing IHEP), Guilherme Tomio Saito (Sao Paulo), Iskra Velkovska (Ljubljana), Xiao Yang (CERN), Mei Zhao (Beijing IHEP)

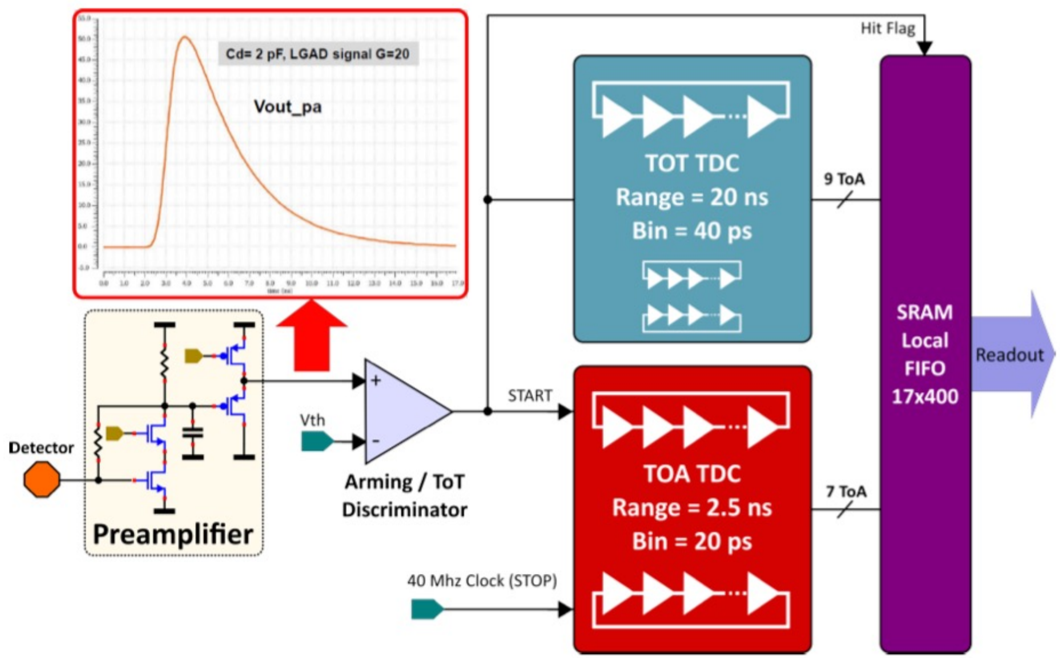


ALTIROC : Fast Timing ASIC

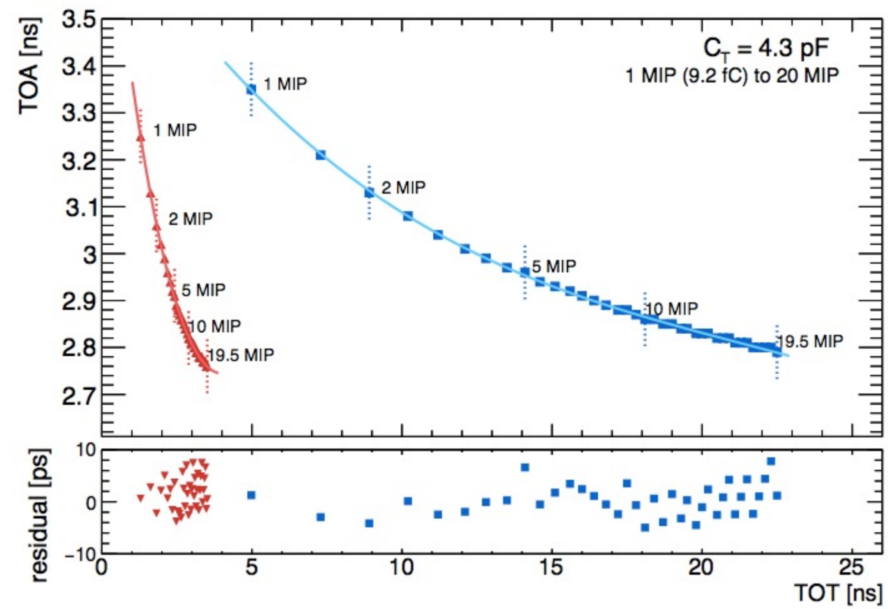
- 225 front-end channels in ALTIROC, each channel has
  - A preamplifier followed by a discriminator:
  - Two TDC (Time to Digital Converter) to provide digital **Hit data**
    - Time of Arrival (TOA) : Range of 2.5 ns and a bin of 20 ps (7 bits)
    - Time Over Threshold (TOT) : range of 20 ns and a bin of 40 ps (9 bits)
  - One Local memory: to store the 17 bits of the time measurement until L0/L1



ALTIROC timing ASIC in nutshell



Time walk correction with TOT



ALTIROC Architecture

ARCHITECTURE

3. Architecture: In-Pixel Fast Front-End plus Off-Pixel Trigger/Readout

ALTIROC is a complete HGTD data path, not merely an analog front-end.

LGAD input → **pre-amplifier** → **discriminat or** → **TOA / TOT TDC** → **pixel SRAM + zero suppression** → **trigger / luminosity processing** → **serializer / lpGBT**

LGAD input	pre-amplifier	discriminator	TOA / TOT TDC	pixel SRAM + zero suppression	trigger / luminosity processing	serializer / lpGBT
50 um LGAD 1.3 mm pad	~1 GHz front-end low jitter	leading-edge start / stop	TOA: 20 ps LSB TOT: 40 ps fine LSB	circular buffer hit-only write	L0 / L1 trigger S1 / S2-S1	to lpGBT 320M-1.28G

Why two TDCs per pixel?

TOA gives the hit time; TOT gives the pulse width. The TOT information is used to correct time walk from the leading-edge discriminator.

In ALTIROC1/2, TOA covers 2.5 ns with a 20 ps bin; TOT covers 20 ns with a 40 ps fine bin.

Why local pixel buffering?

HGTD timing data are not read out immediately; they wait for L0/L1 trigger decisions.

ALTIROC2 uses a 1400-deep circular buffer for about 35 us latency; ALTIROC-A reports 38.4 us latency.

The hard part is power integrity

ALTIROC is a large ASIC above 4 cm2 powered from one side. Simultaneous switching of analog FE, TDCs, SRAM and digital logic maps IR drop into threshold, LSB and timing degradation.

This is the core reason behind the ALTIROC2-to-3 redesign.

Architecture details are mainly from ALTIROC1 TWEPP2019, ALTIROC2 poster and ALTIROC3 TWEPP2024 material.

ALTIROC key specification

KEY METRICS

4. Functions and Key Specifications

Once fast front-end, buffering, triggering and luminosity counting are integrated, the question is whether all requirements hold simultaneously.

225	20 ps	2.2-2.5 fC	35-38 us
final 15 x 15 pixel matrix	TOA TDC LSB	detectable charge / threshold	trigger-latency buffer

Function side

Per-pixel TOA and TOT
TOT-based time-walk correction
Bunch-by-bunch luminosity hit counting
Two programmable timing windows W1/W2, producing S1 and S2-S1

Readout and clocking

Serial output from 320 Mb/s to 1.28 Gb/s
I2C slow control plus lpGBT fast commands
Internal clocks: 40 / 80 / 320 / 640 MHz
100 ps phase-shifter step, jitter below 5 ps

Power and reliability

ALTIROC1 power target: 4.4 mW/pixel
ALTIROC3 public figure: about 3 mW analog + 0.5 mW digital per pixel
Triple modular redundancy for configuration registers
ALTIROC2 ASIC-alone data stable up to 220 Mrad

<10 ps
time-walk residual scale reported for ALTIROC2

<25 ps
electronics jitter target/scale at 10 fC injection

340 Mrad
ALTIROC1 X-ray irradiation range

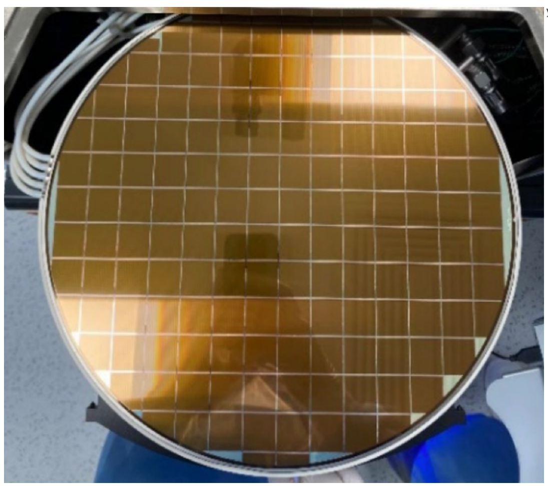
2 x 1.28 Gb/s
high-speed output capability reported for ALTIROC3

Numbers are compiled across ALTIROC1/2/3 public material; wording is kept at engineering scale rather than version-specific minutiae.

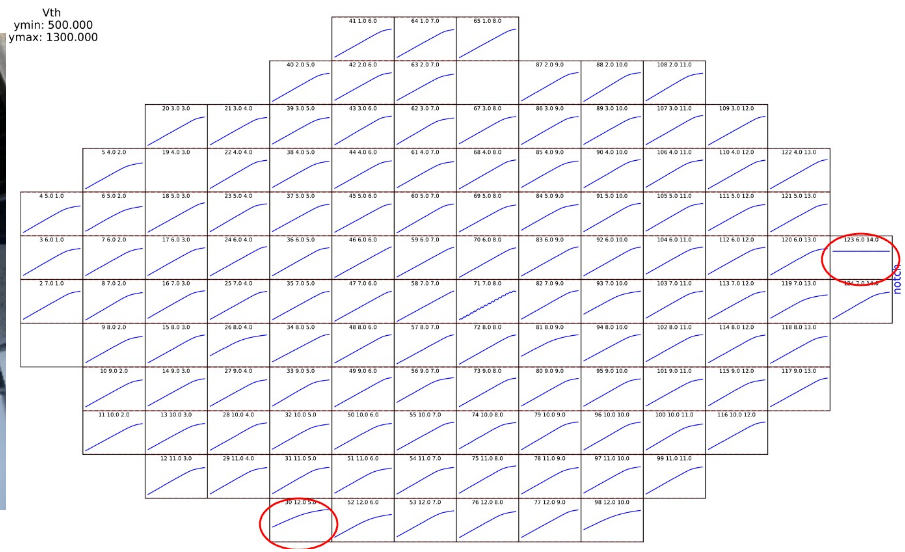
ALTIROC wafer tesing

- China and IJClab (France) share 50% of wafer level ALTIROC probing tests
- IHEP have setup the wafer testing system using fully automatic probe station
- IHEP, SJTU, SDU have done pre-production wafer testing， passed CERN review
    - Tested more than 14 wafers（~2000 ASICs）
    - ATLAS decided move 100% wafer testing to China after the review.

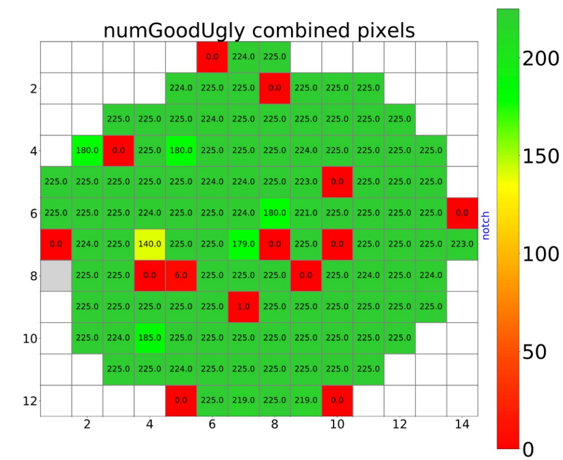
ALTIROC-A wafer



ASIC wafer test result



ASIC wafer test result

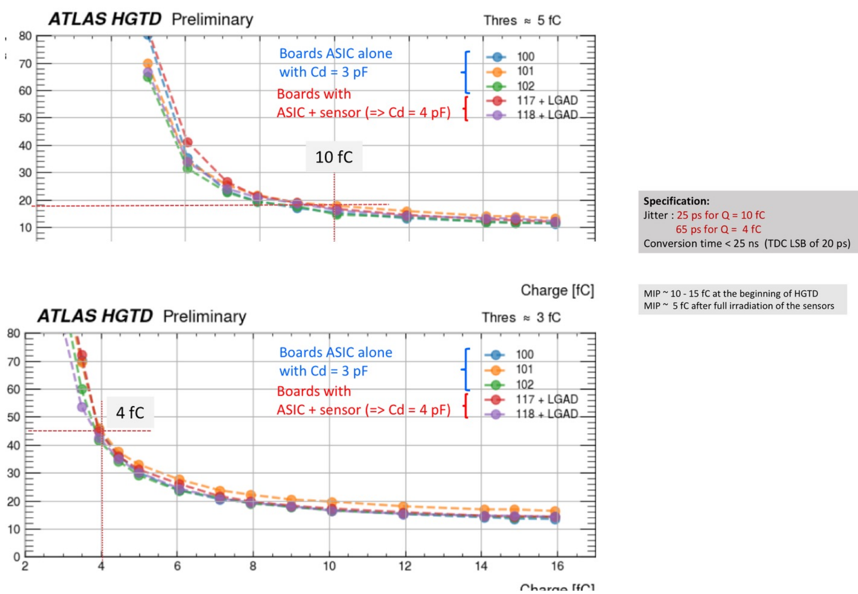


Other results of ALTIROC

PERFORMANCE

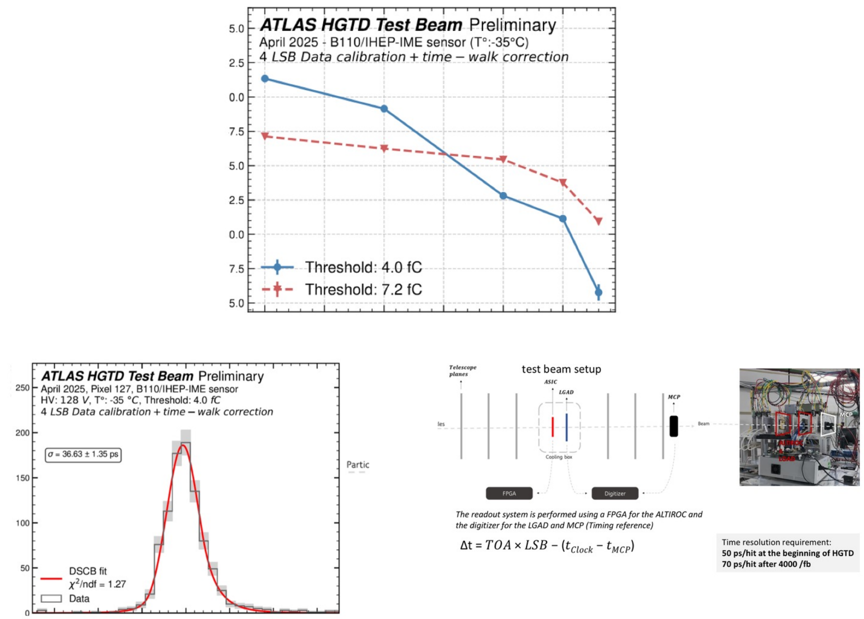
7. Representative Performance Results

Key source plots are cropped and enlarged so that jitter, threshold and beam-test results can be discussed directly.



Jitter vs charge: <25 ps at 10 fC; the 4 fC point remains within the HGTD end-of-life envelope.

Source: TWEPP 2025 AltirocA_twepp2025.pdf, p.8



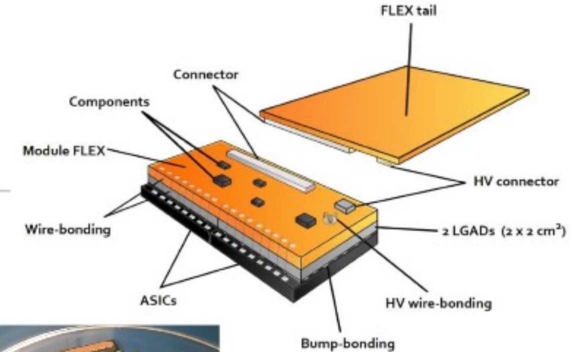
Test beam: cold hybrid boards reach about 40 ps average time resolution.

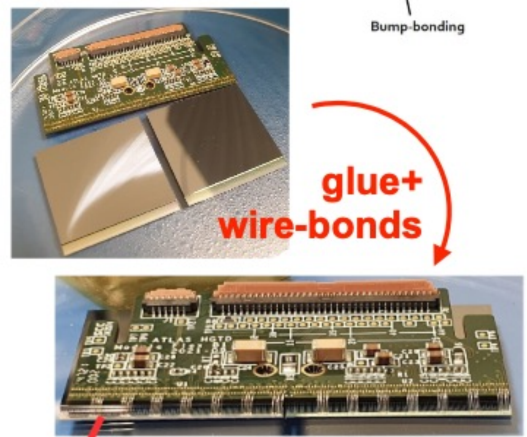
Source: TWEPP 2025 AltirocA_twepp2025.pdf, p.12

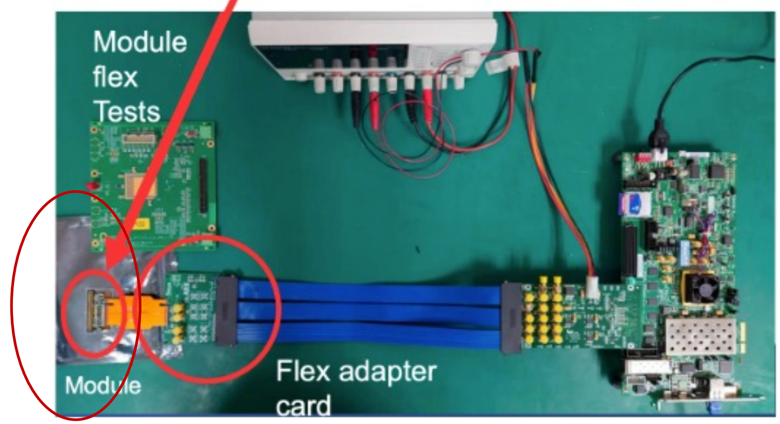
The page uses cropped source plots, not full-slide screenshots, to improve projector readability.

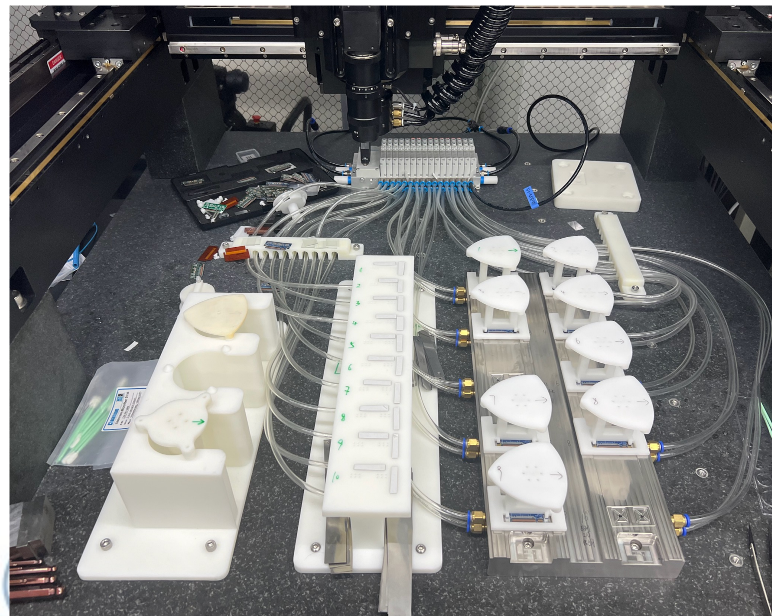
HGTD module assembly

- 6 module assembly site at HGTD
  - IHEP, USTC, Mainz, France, IFAE, Morocco
  - IHEP is largest site, 44% module assembly (~3000)
- IHEP developed module flex and gantry robot
  - Pattern recognition, glue dispending and assembly
  - Plan to assemble 10 modules each time



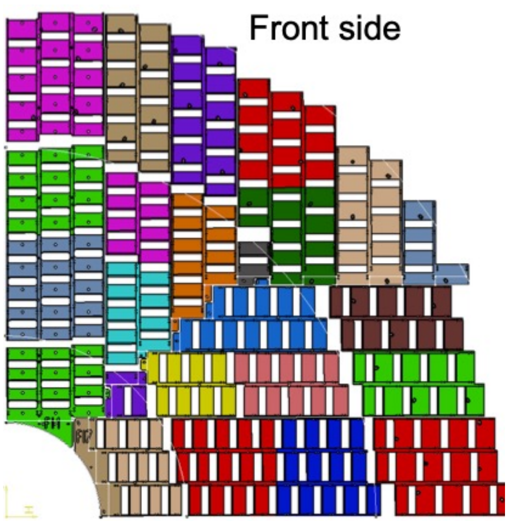






HGTD module loading

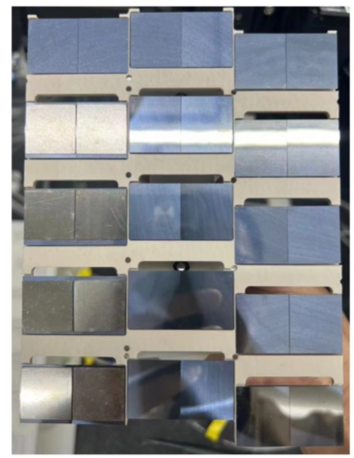
- IHEP loaded the first two ALTIROC3 detector units for demonstrator
  - Use Gantry system to position all 15 modules and glue dispending
  - Delivered to CERN, and integrated in 54-modules demonstrator
- IHEP/USTC are developing automatic loading with 1m^2 large gantry
  - Toward the final production rate



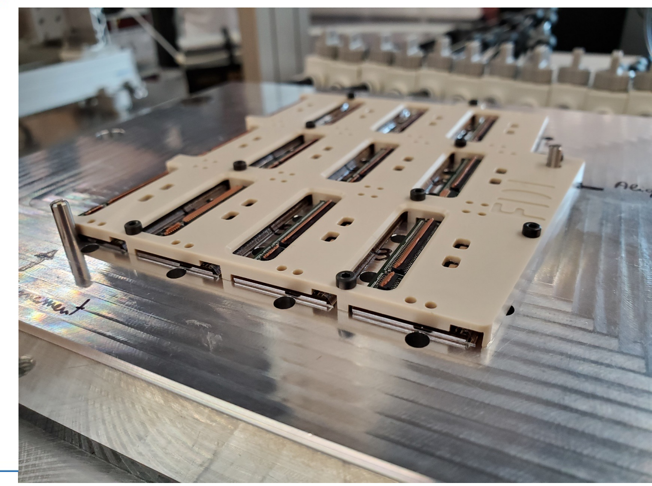
Gluing modules on support units

Dispensing with GluingTool

Backside view after removal

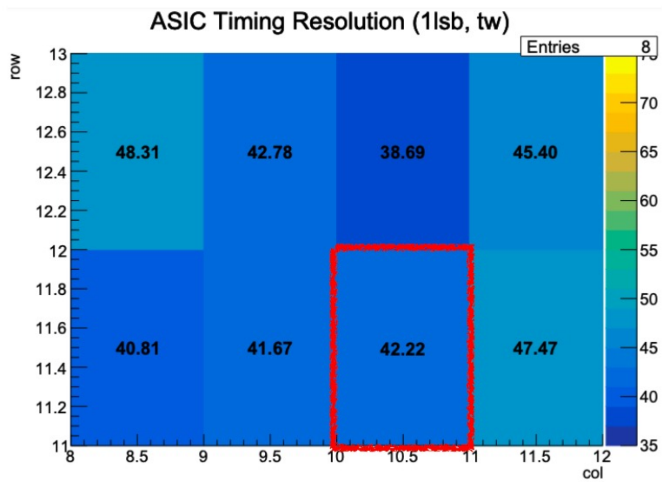


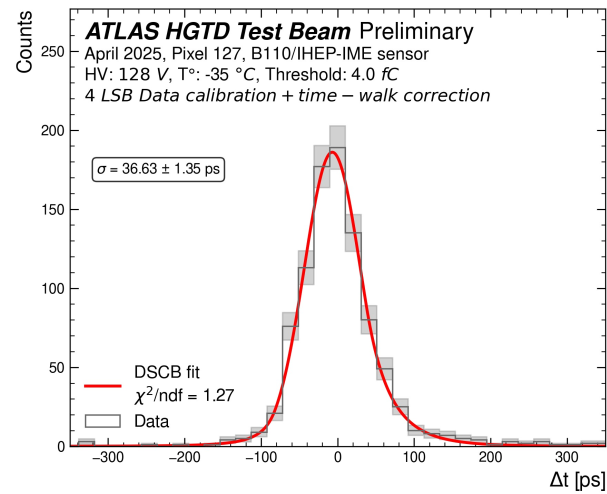
Loading modules on support units



HGTD Module beam tests

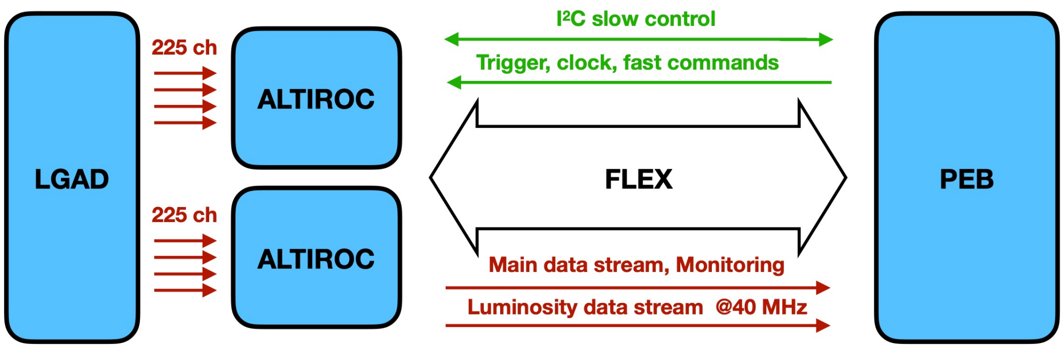
- Module level Test beam showed that
  - Individual channels can reach ~50ps level timing resolution
  - In next few years, HGTD will have 3M channels @ ~50ps resolution





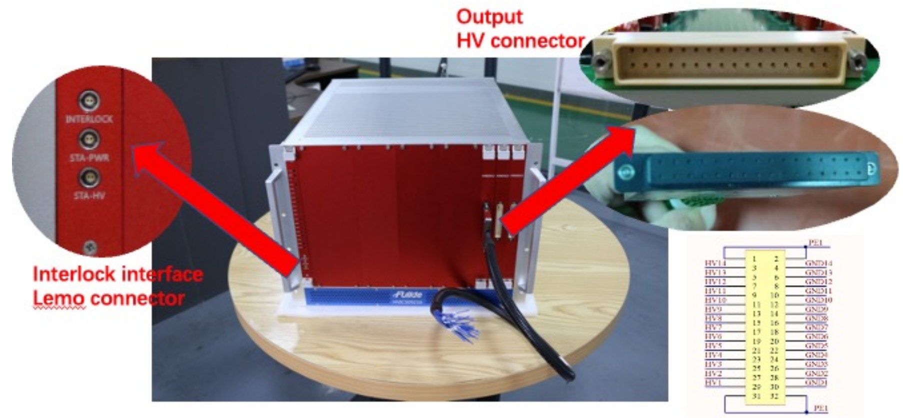
Peripheral Electronics Boards, flex tail, HV power supply

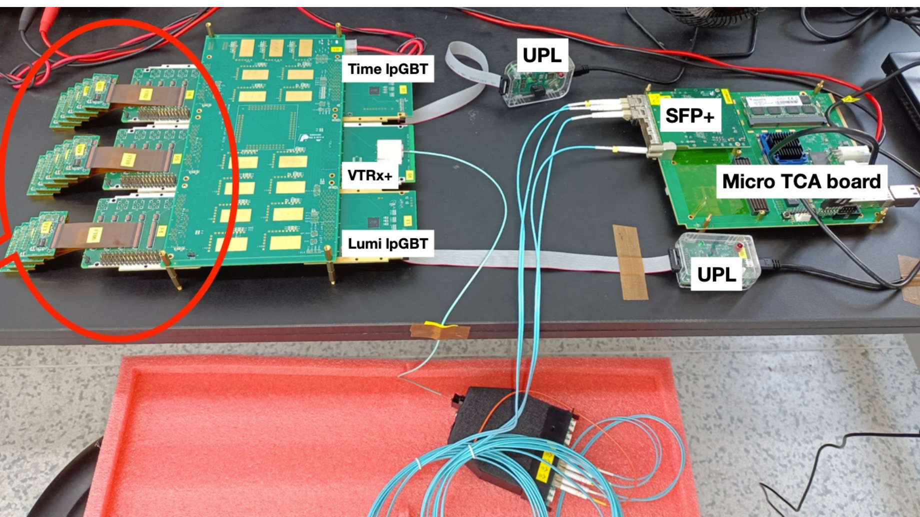
- IHEP and NJU developed Peripheral Electronics Boards prototype
- SDU developed long flex tail prototype (75cm)
- IHEP developed high voltage power supply prototype



Modular Peripheral Electronics Boards prototype

High voltage power supply prototype



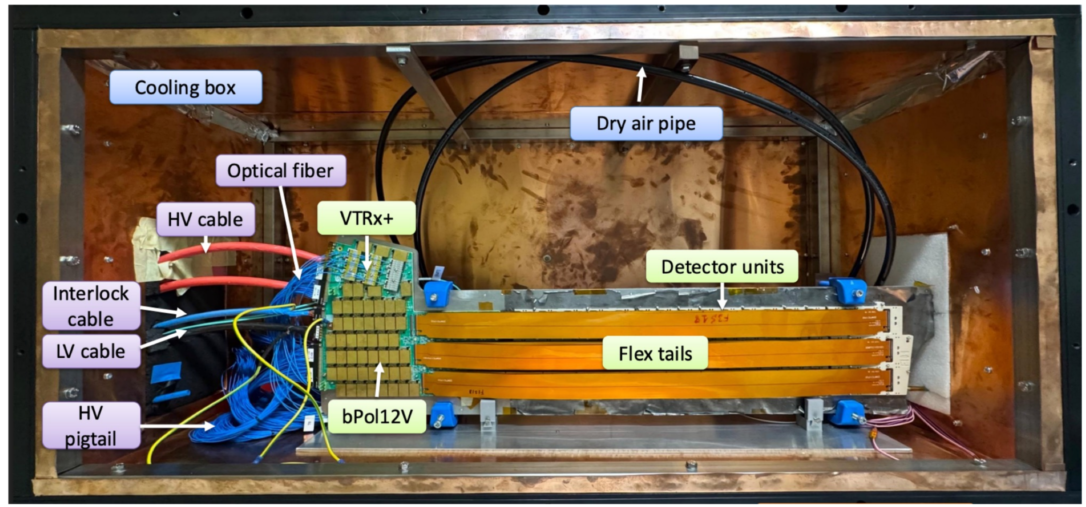


Long Flex tail prototype (75cm)

HGTD prototype demonstrator

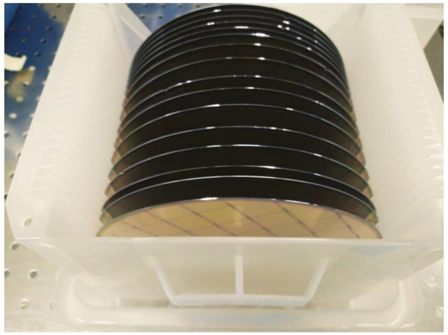
- **The China team played a leading role in the R&D of the large-scale prototype consisting of 54 modules.**
  - **1st validation of a high-time-resolution detector system**

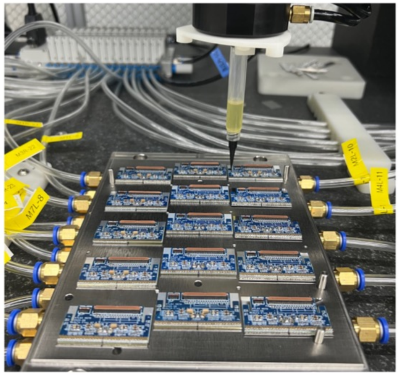
2025 ATLAS upgrade review
Group photo at HGTD prototype



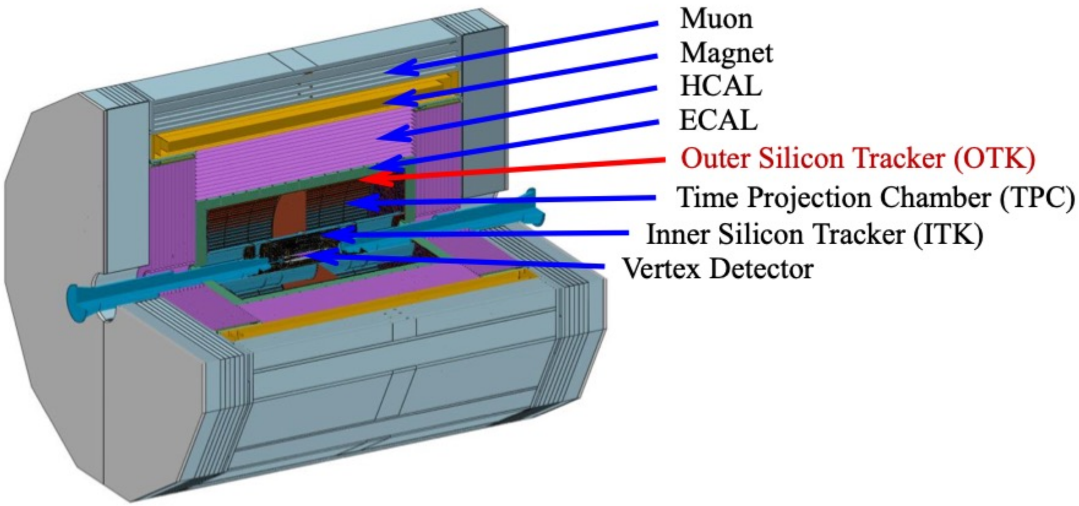
HGTD summary

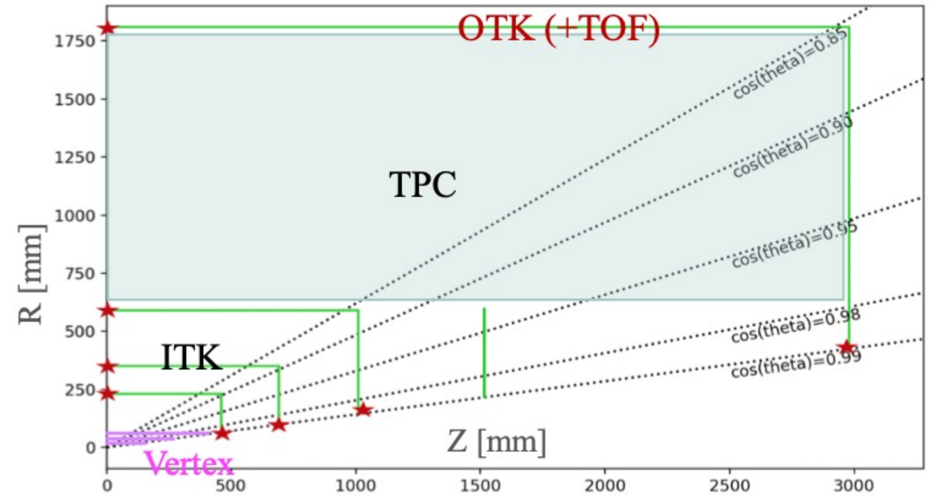
- **China group took important positions in HGTD, including project leader and conveners**
- **China is making key contributions to HGTD**
  - **100% (90% IHEP, 10%USTC) LGAD sensor**
  - **50% ASIC testing (IHEP, SJTU,SDU)**
  - **50% hybrization (IHEP), 44% module assembly (IHEP, USTC,SDU,SJTU)**
  - **100% front-end electronics board (IHEP, NJU), prototyped 1st full-size PEB**
  - **>16% high-voltage electronic systems(IHEP,SDU), HV supply pre-production done**
  - **33% flexible PCB tails (SDU), 1st prototyped tested**





CEPC outer tracker and AC-LGAD



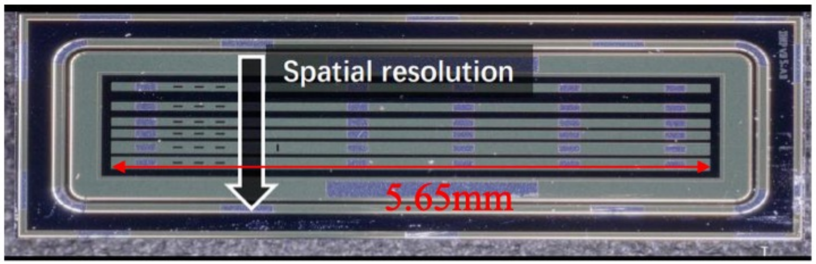


- **CEPC**-- measurement potential for precision tests of SM: Higgs, electroweak physics, flavor physics, QCD/Top
- Produce 10^{12} Z boson at Z pole: Rich flavor physics program
- **The LGAD based OTK (+TOF) detector** will be placed between TPC and ECAL
- Timing detector is complementary to gas detector for PID:
  improves the separation ability: 0-4 GeV for K/pi separation, 0-8 GeV for K/p separation
- **Barrel : ~65 m^2 , Endcap 20 m^2**

1st prototype of AC-LGAD for CEPC

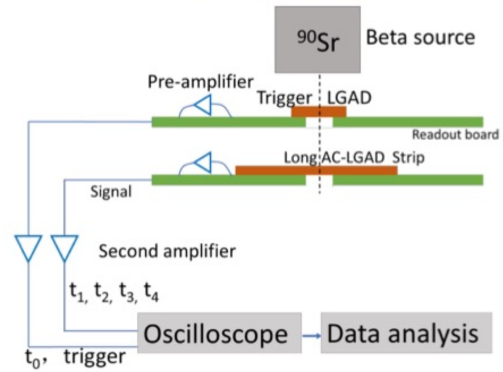
AC-LGAD R&D

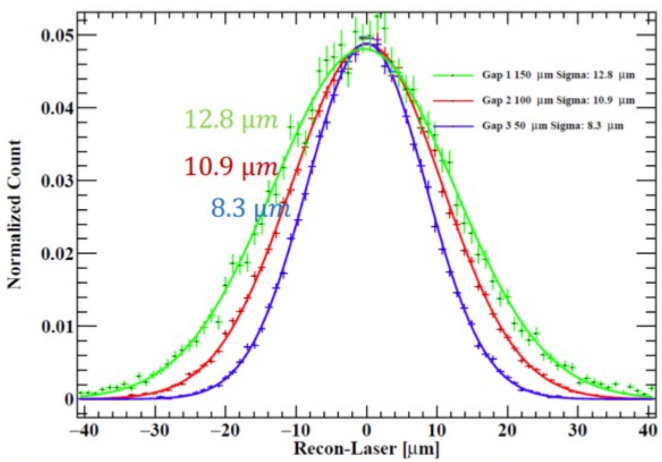
Spatial resolution: Laser testing
Timing resolution: Beta source test



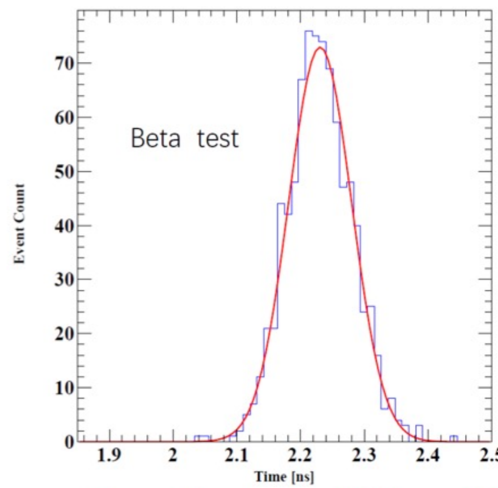
- Strip length 5.65mm
- pad-pitch size:
  100-250 um
  100-200 um
  100-150 um

^{90}Sr test setup





AC-LGAD with pitch size as 150um:
Best spatial resolution~8um (laser test)



Landau and jitter contribution

$$\sigma_{AC-LGADStrip} = \sqrt{\sigma_{\Delta T}^2 - \sigma_{Trigger}^2}$$

Trigger: 28.5ps

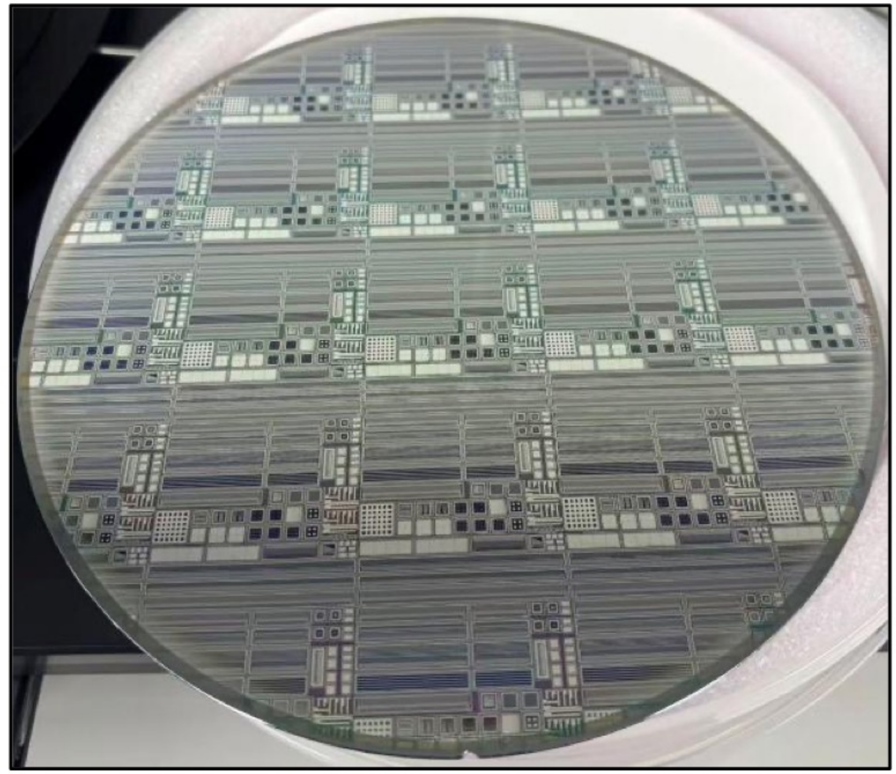
Time resolution: 37.5 ps

The performance of AC-coupled Strip LGAD developed by IHEP. NIMA. Volume 1062. May 2024. 169203

ATLAS EXPERIMENT

2nd prototype of AC-LGAD with long strip

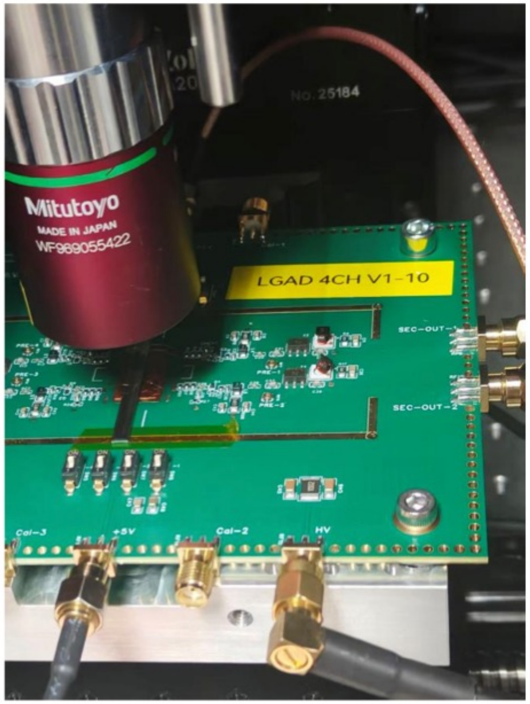
Wafer number	EPI thickness	n+ dose
1	50um	10p
2	50um	10p
3	50um	0.01p
7	80um	10p
8	80um	0.01p



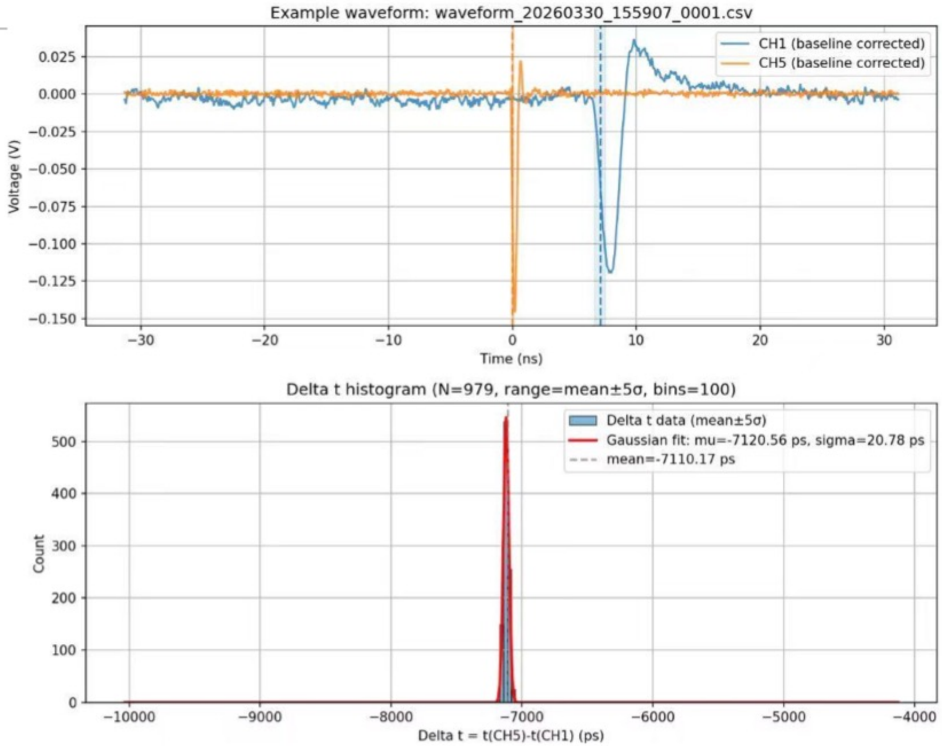
- Five wafers been delivered.
- Testing been done on wafer 1, wafer 7: I-V, C-V, and timing performance

2nd prototype of AC-LGAD with long strip: test result

Timing performance of AC-LGAD with 4cm long strip, pad-pitch size as 50-100um: ~20ps

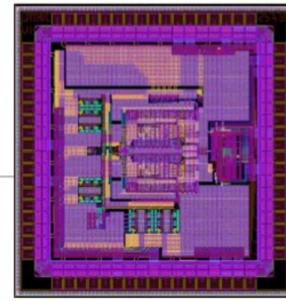


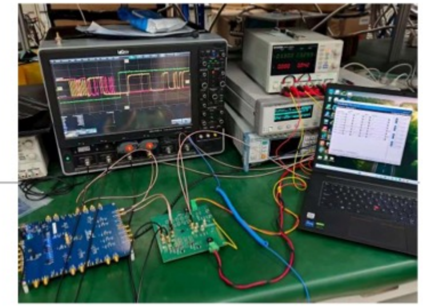
Laser intensity equal to 1MIP

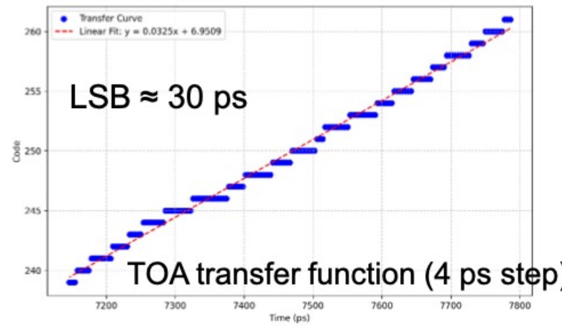


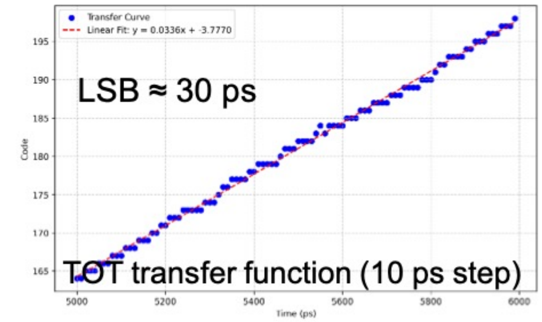
LGAD Readout ASIC (LATRIC0)

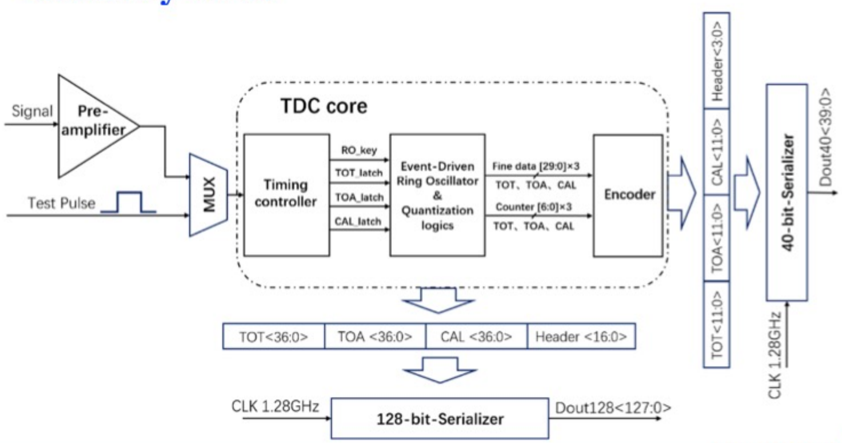
- **The first LGAD readout ASIC prototype, LATRIC-V0, submitted for tape-out in April, was delivered in August 2025**:
  - The ASIC integrates a pre-amplifier, a discriminator, a TDC, and a serializer for data output.
  - **The LSB is 29.8 ps, meeting the 30 ps design goal.** TDC power consumption is 0.1 mA (1.2 V) @ 0.5 MTPS (Mega-Trigger Per Second), 0.3 mA @ 1 MTPS, and 0.5 mA @ 2 MTPS.
- **The 8-channel LATRIC-V1 was submitted for tape-out in October 2025, and received in February 2026.**

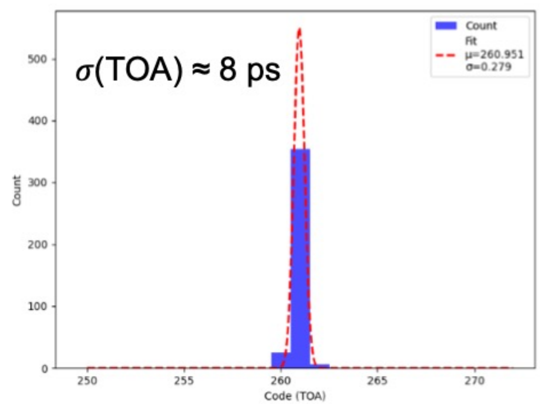


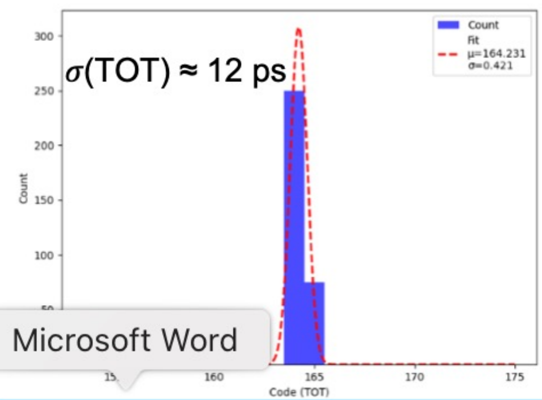








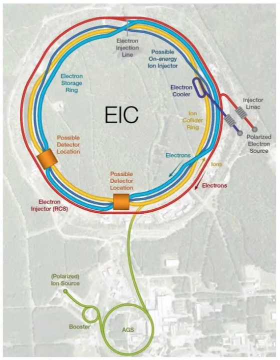




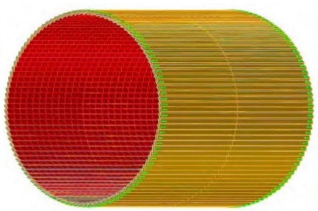
CEPC WORKSH

Other future Application of LGAD

Electron-Ion Collider (EIC)： Timing-tracker

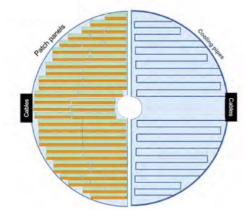


Barrel AC-LGAD detector



$10.9\ m^2$

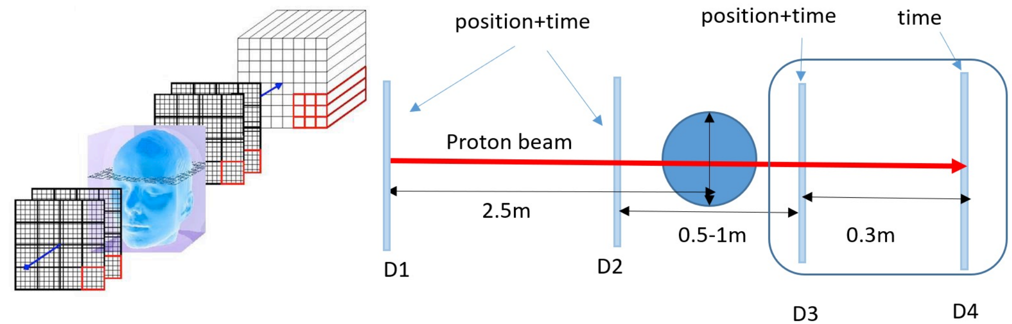
Hadron endcap AC-LGAD detector



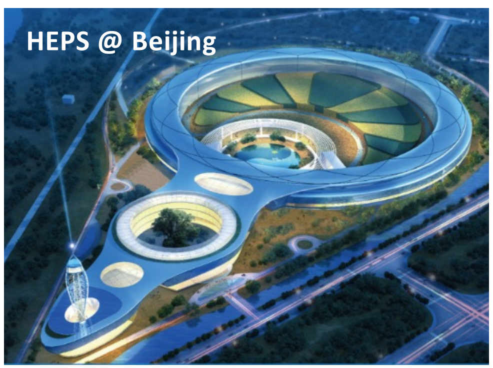
$2.22\ m^2$

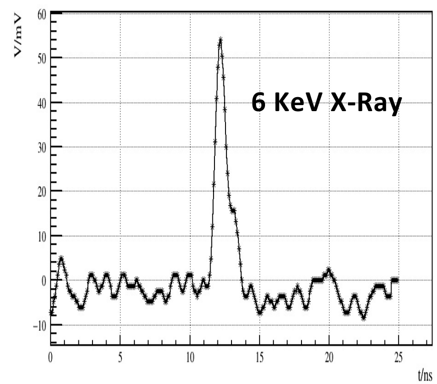
Nuclear Medicine Instruments：

Such as proton therapy and proton CT

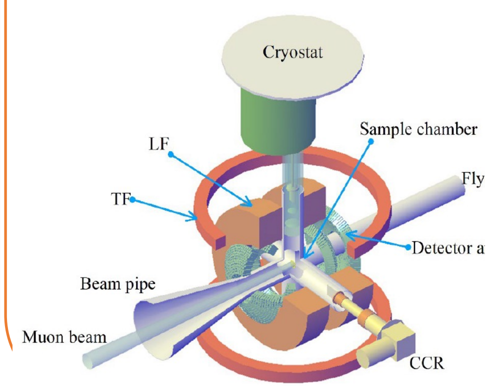


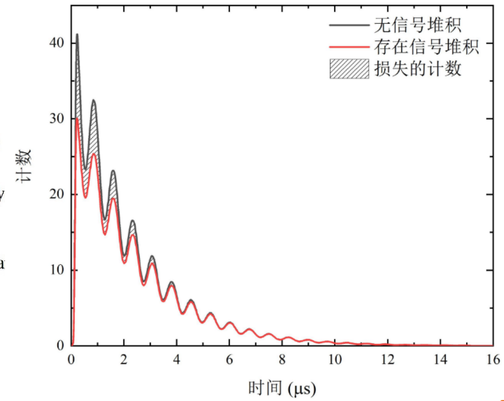
X-ray detectors @ advanced light sources





Muon MuSR based on LGAD (pileup reduction)





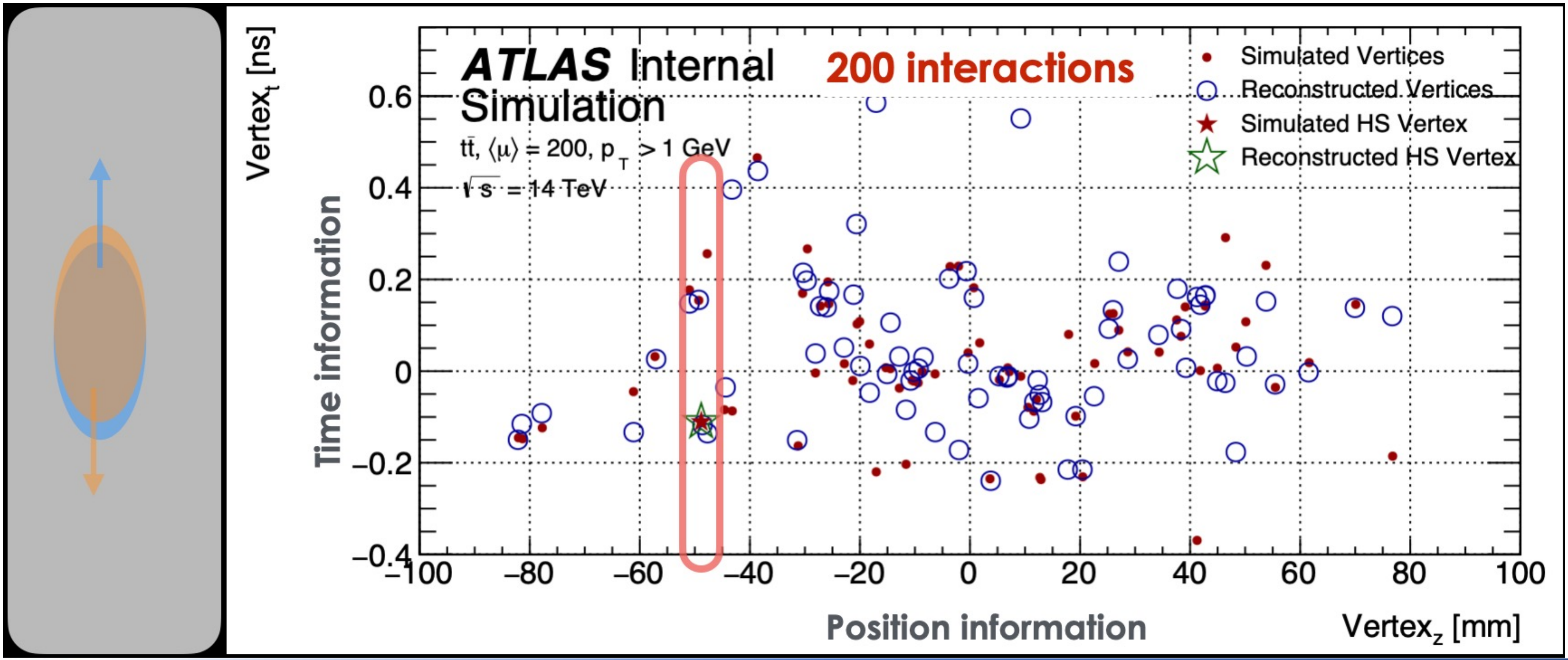
mzli@ihep.ac.cn

ATLAS EXPERIMENT

Backup

Motivation

- Pileup background is major challenges at high luminosity LHC
- High precision timing info can reduce the pileup by one order of magnitude



Motivation

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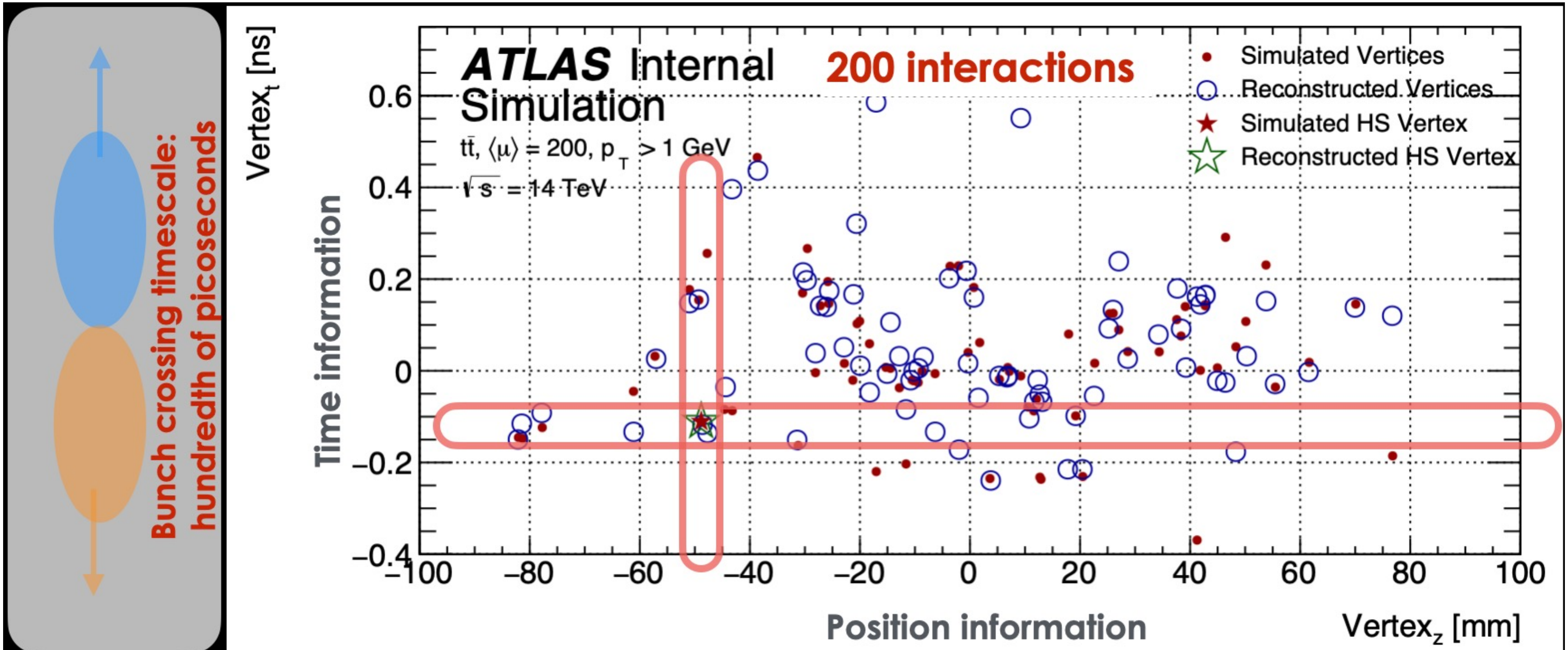
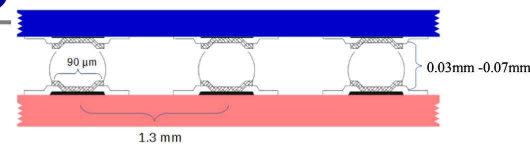
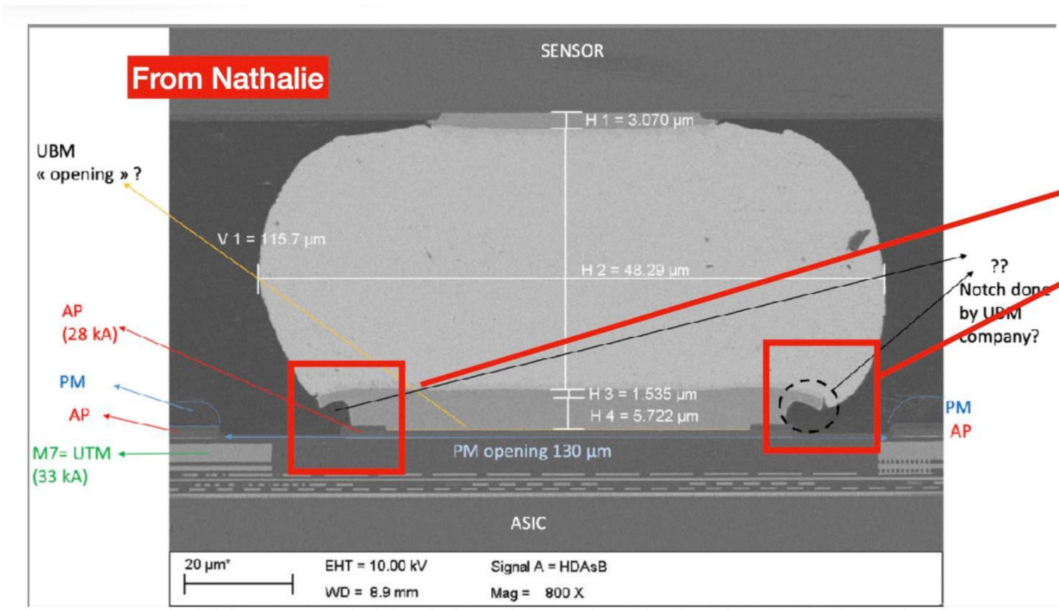


Major improvement in hybrid: new Polyimide layer ALTIROC2 VS ALTIROC3 hybrid

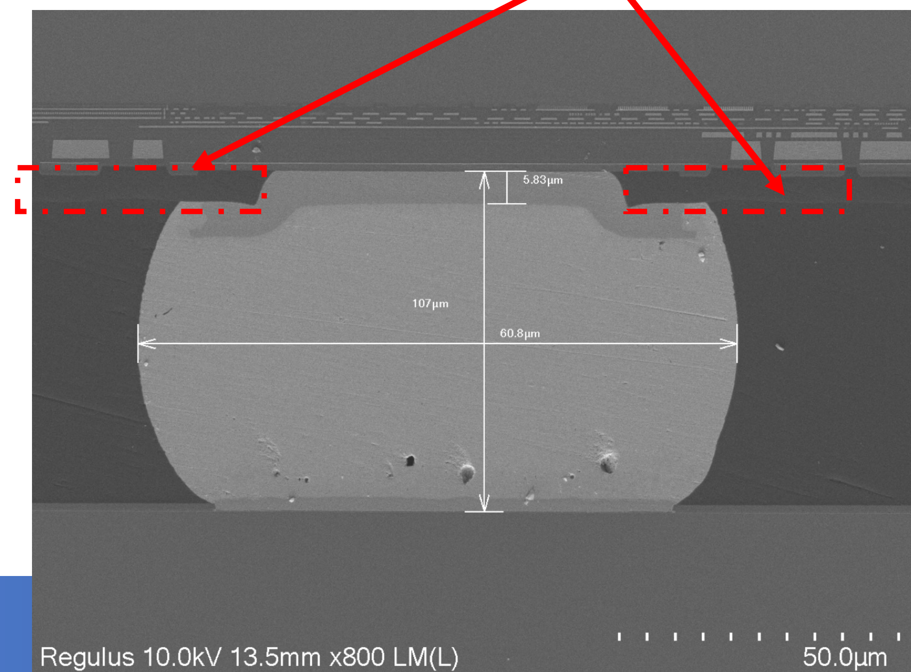


- Polyimide in ALTIROC3 deposited at NCAP/IHEP
  - Optimize to use Soft Polyimide material
  - More robust in thermal cycle, higher yield than ALTIROC2 hybrids.
- In ALTIROC3 hybrids prototyping phase, all ALTIROC3 UBM/thinning/dicing by IHEP/NCAP
- Next step to make the bump bonding thermal stability
  - Increase sensor thickness, increase the number of bumps

ALTIROC2 hybrid by TSMC with incorrect Polyimide

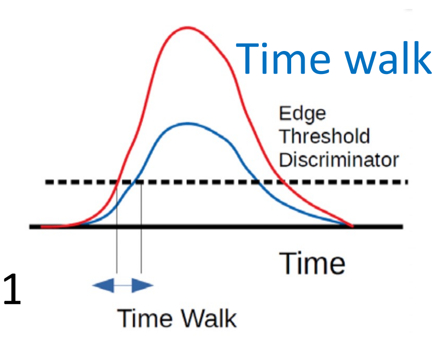


ALTIROC3 hybrid by NCAP/IHEP with correct Polyimide

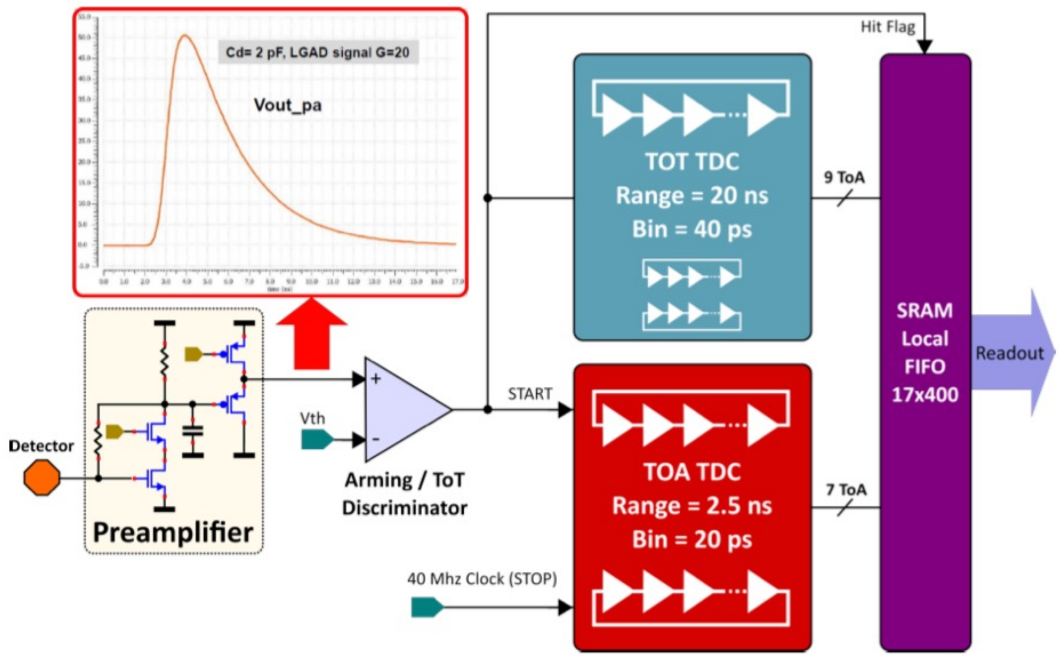


ALTIROC : Fast Timing ASIC

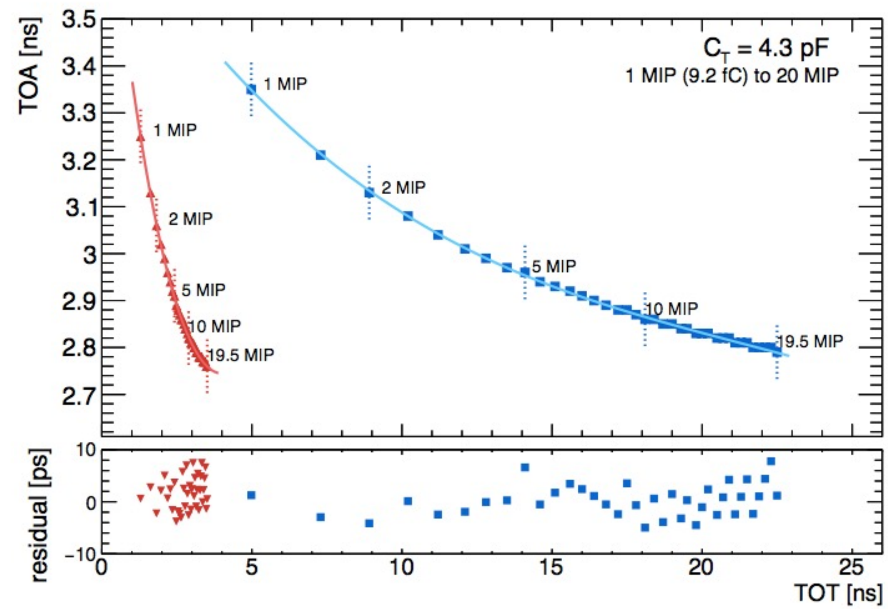
- 225 front-end channels in ALTIROC, each channel has
  - A preamplifier followed by a discriminator:
  - Two TDC (Time to Digital Converter) to provide digital **Hit data**
    - Time of Arrival (TOA) : Range of 2.5 ns and a bin of 20 ps (7 bits)
    - Time Over Threshold (TOT) : range of 20 ns and a bin of 40 ps (9 bits)
  - One Local memory: to store the 17 bits of the time measurement until L0/L1



ALTIROC timing ASIC in nutshell

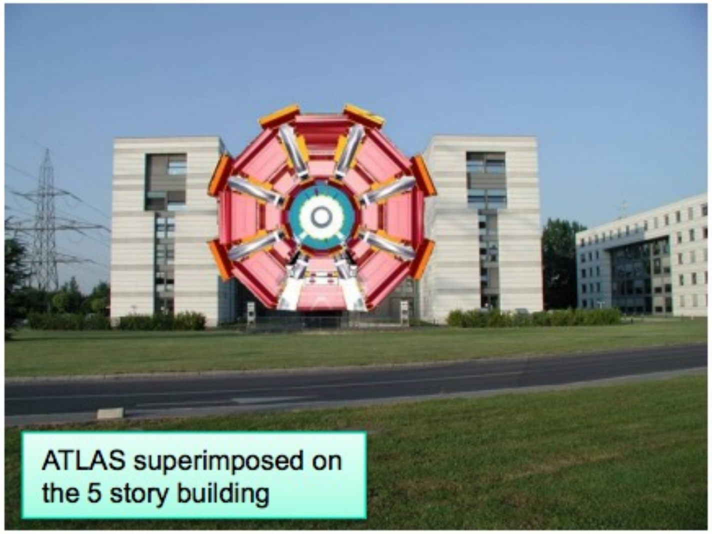


Time walk correction with TOT

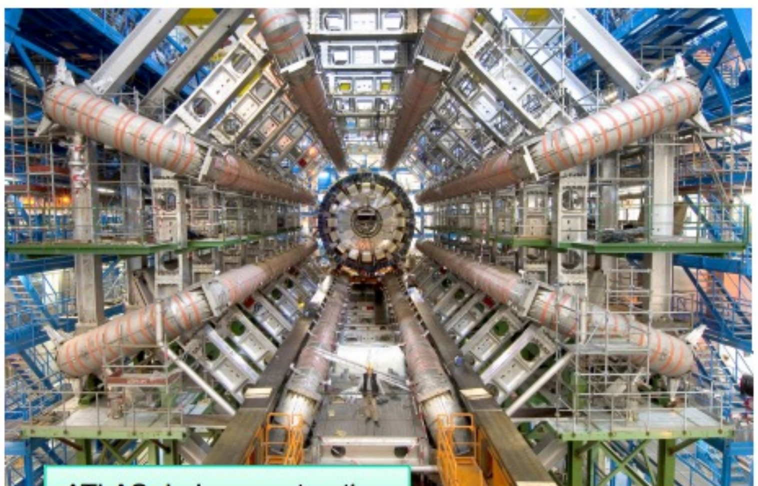


ATLAS experiment

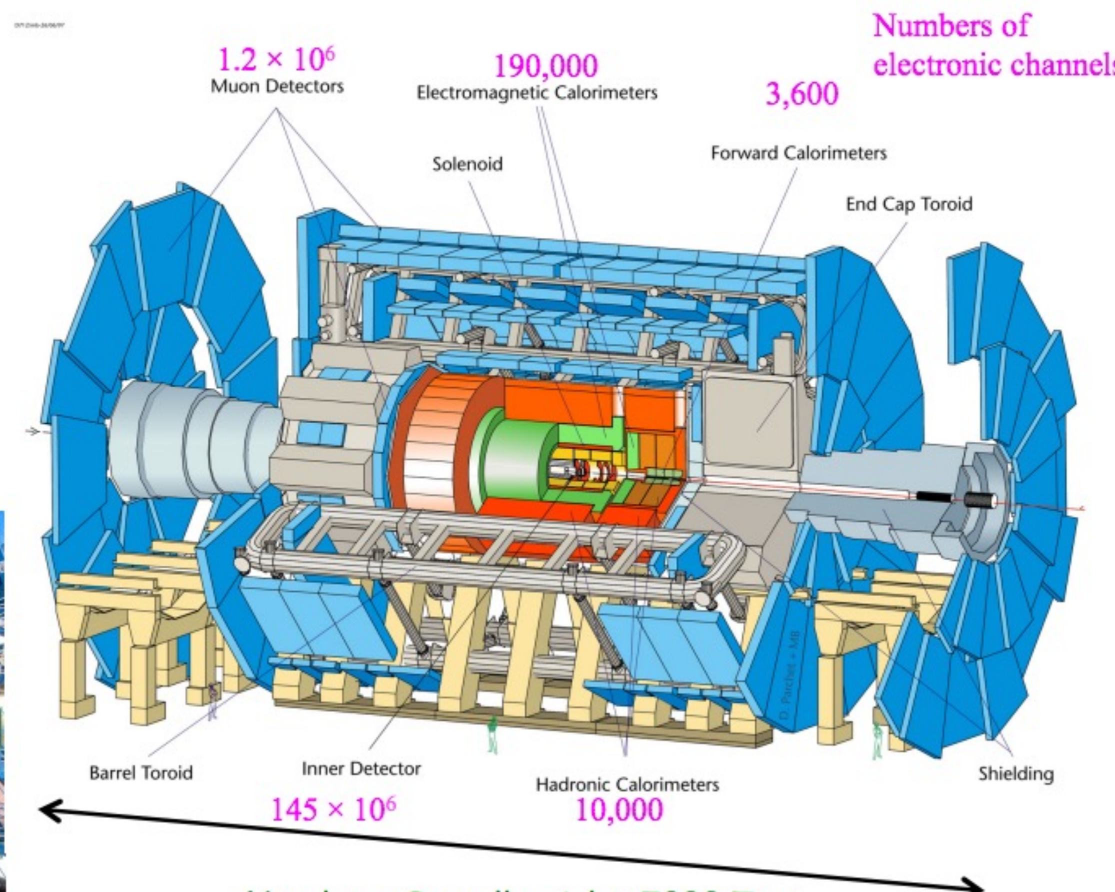
Designed & Built with cutting edge/innovative technologies by HEP physicists



ATLAS superimposed on the 5 story building



ATLAS during construction

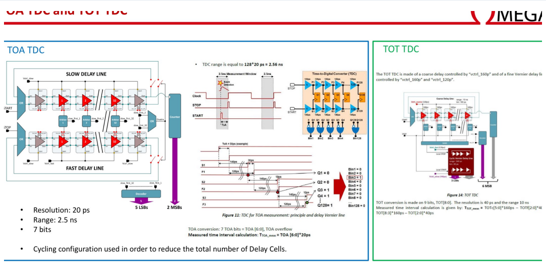


46 m long, Overall weight: 7000 Tons

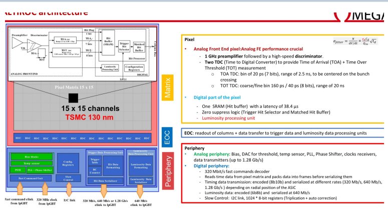
~3000 scientists from 174 Institutions and 38 Countries

9. 2.5 ns TOA, 38.4 us Buffer and Non-LHC Use

The 2.5 ns number is a fine-time measurement window, not a long-latency buffer.



TOA/TOT TDC: TOA is 7-bit, 20 ps LSB, 2.5 ns range; TOT range is 20 ns.
Source: TWEPP 2025 AltirocA_twepp2025.pdf, p.20



Pixel architecture: the trigger buffer is the in-pixel SRAM / hit buffer; ALTIROC-A reports 38.4 us latency.
Source: TWEPP 2025 AltirocA_twepp2025.pdf, p.5

1. What the 2.5 ns window means

It is the TOA TDC fine-time window, not the deep trigger buffer. ALTIROC measures fine time inside the 25 ns frame of the 40.08 MHz LHC bunch clock: 128 x 20 ps is about 2.56 ns.

2. Where the real buffer sits

Trigger latency is handled by in-pixel SRAM / hit buffers. ALTIROC2 public material often quotes about 35 us; ALTIROC-A quotes 38.4 us. Fine time is ns-scale, while trigger latency is tens of us.

3. Can it work outside LHC?

Yes, but not as a drop-in part. A practical system would use FPGA/PLL logic to generate or lock to a compatible 40.08 MHz reference, translate experiment triggers into ALTIROC fast commands, and tune phase with the on-chip phase shifter.

If the experiment lacks a stable periodic reference, if hit time drifts by much more than 2.5 ns relative to the reference, or if fully triggerless streaming is required, ALTIROC is no longer an optimal direct fit.

Portable idea: fast FE + TDC + trigger buffer. Non-portable constraint: the 40.08 MHz / 25 ns bunch-clock semantics.

Hybrid test beam result

- Hybrid functionality was validated by test beam
  - The EUDET telescope is used for track reconstruction
  - Sensor bias voltage is -180 V, corresponding to a charge of ~20 fC
  - ASIC threshold 4.8 fC
- Close to 100% efficiency in the center of the pixel (pad)
  - The gap between pixels (pads) is about 50μm