R&D of electronics system of MDC in STCF

Zhe Cao, on behalf of STCF-MDCH Group

University of Science and Technology of China

第十四届全国先进气体探测器研讨会

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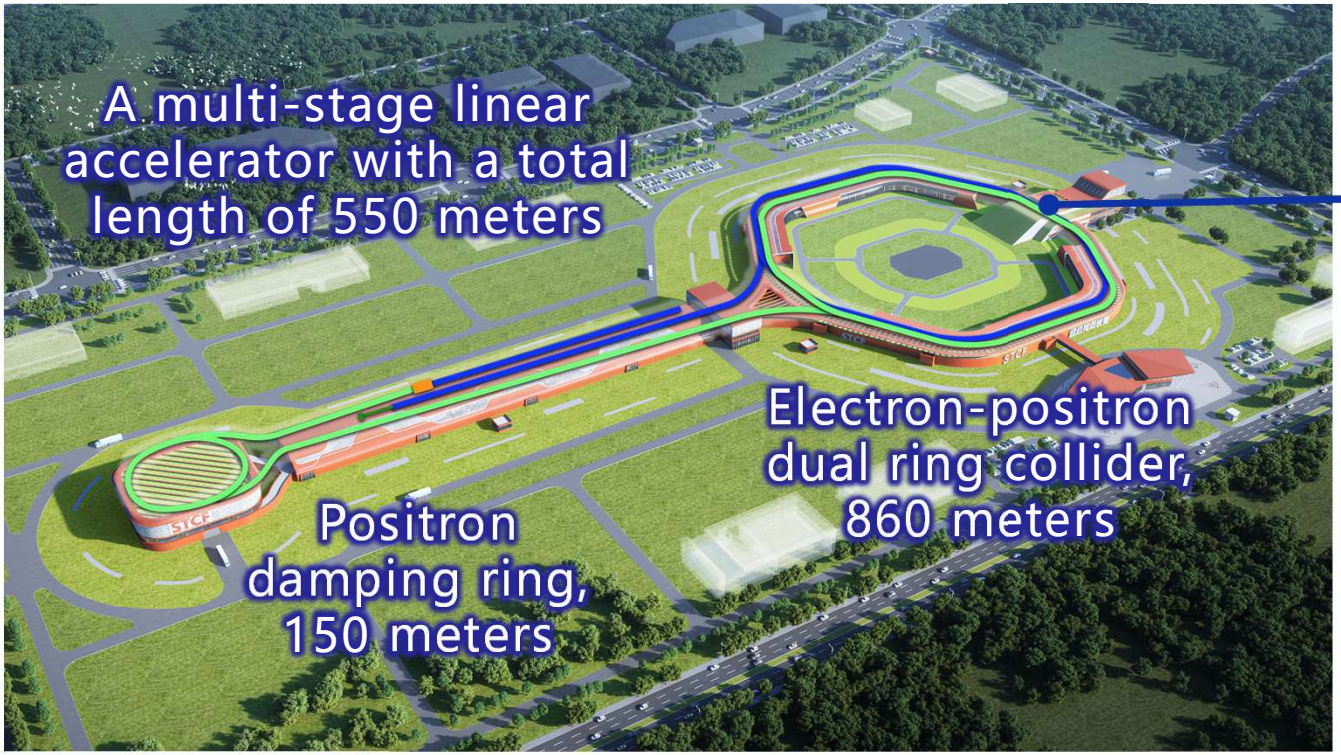
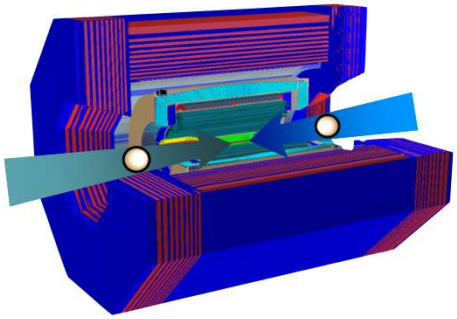
Outline

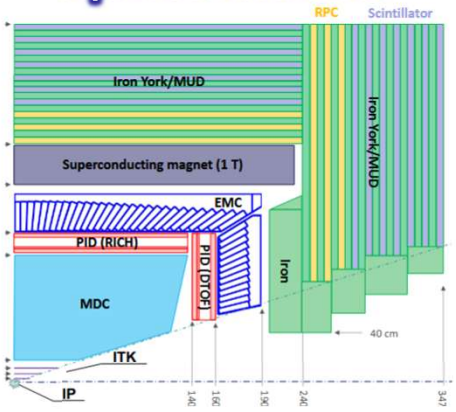
1. **Overview of STCF**
2. **Progress on Discrete Electronics**
   a) Online algorithm of waveform identification
   b) Prototype readout electronics: phase I, II, III
   c) Electronics tests & Detector integration tests
3. **Progress on the ASIC**
   a) Design and testing of the 1st & 2nd version MDC front-end ASIC
   b) Electronics tests & Detector integration tests
4. **Summary**

Super Tau Charm Facility (STCF)





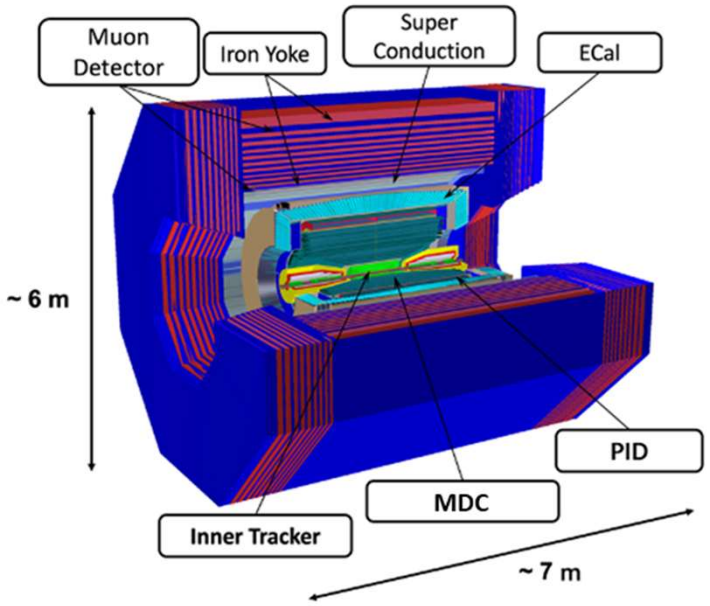
Particle detection spectrometer

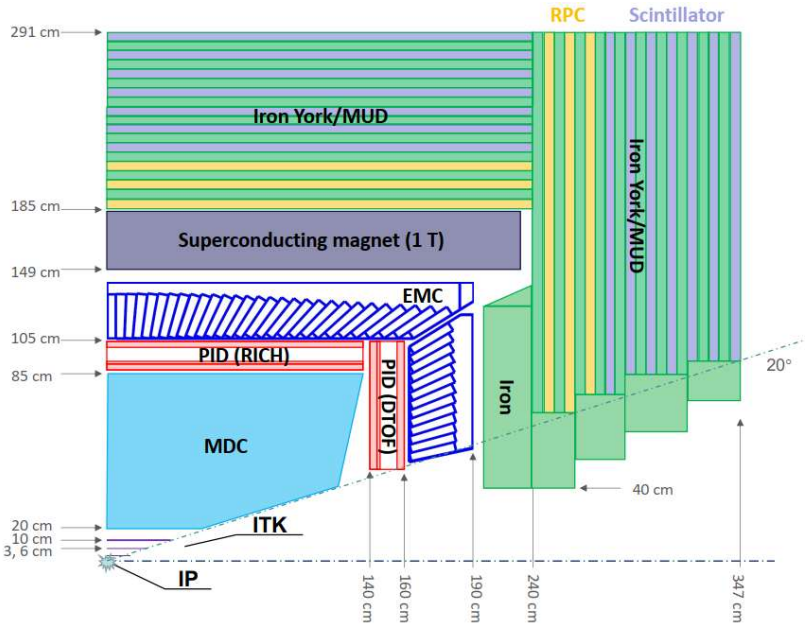


- A new generation of electron-positron collider: STCF
- Centroid energy: 2~7 GeV, Luminosity > $0.5\sim1\times10^{35}$ cm^{-2} s^{-1}

Super Tau Charm Facility (STCF)

STCF — Detector





- **Participates in the spectrometer triggering**
- **Complete system track reconstruction**
- **Combine PID to complete particle identification**

ITK Inner Tracker

$< 0.25\%\ X_0$ / layer

$\sigma_{xy} < 100\ \mu m$

MDC Main Drift Chamber

$\sigma_{xy} < 130\ \mu m$

$\sigma_p/p \sim 0.5\%$ @ 1 GeV

dE/dx ~ 6%

PID Particle Identification

π/K (and K/p) 3~4 σ separation up to 3.5 GeV/c

EMC Electromagnetic calorimeter

E range: 0.025~3.5 GeV

σ_E @ 1 GeV: 2.5% in barrel, 4% at endcaps

Pos. Res. : ~ 4 mm

MUD Muon detector

0.4 ~ 1.8 GeV

π suppression > 30

Main Drift Chamber (MDC)

- **Big challenge:**

  High luminosity → high hit rate → pileup

  - Innermost layer cell (~10mm) hit rate: ~400 kHz/ch
  - Probability of events piling up: ~18% within a 500 ns time window

- **Optimization strategies**

  - Design of ultra-small-size drift cell (~5 mm)
  - Design of **electronics for high hit rate**

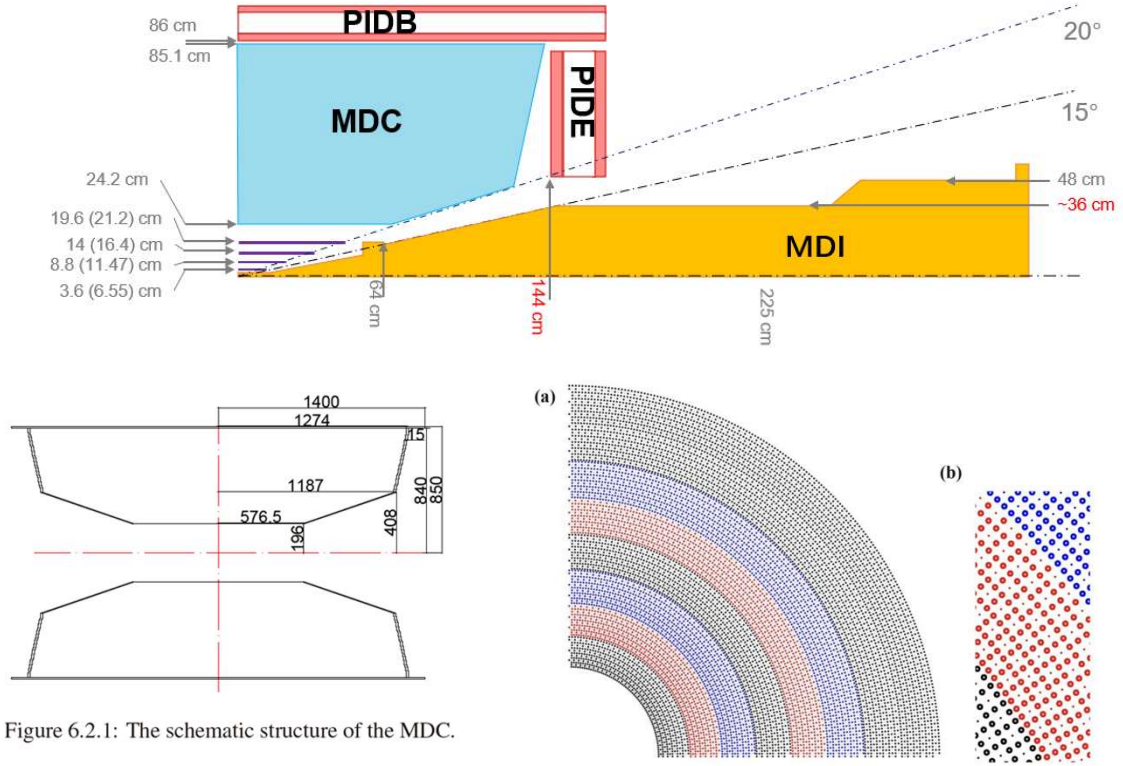
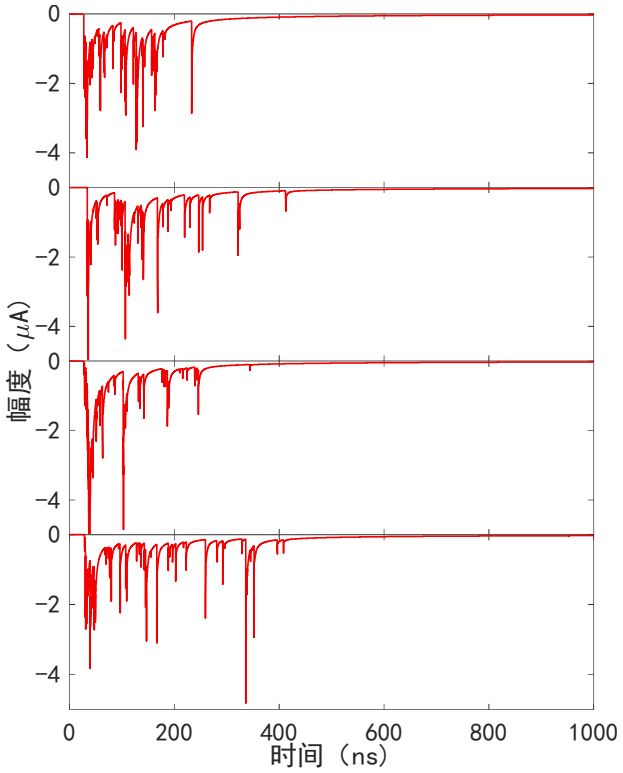


Figure 6.2.1: The schematic structure of the MDC.

Requirement and challenges for electronics

- **Measure requirement for electronics**
  - Dynamic range: 60 fC ~ 1800 fC
  - Most probable charge: 200 fC
  - Hit Rate of ultra-small-size drift cell ➔ ~210 kHz
  - Resolution of dE/dx ➔ charge measurement resolution < 8 fC
  - Resolution of position ➔ time measurement resolution < 1 ns
- **Challenges**
  - High hit rate of signal
  - Long duration of signal
  - Multi-peak & inconsistent waveform
  - Limited space for electronics & cooling system



Different waveform of 200 fC

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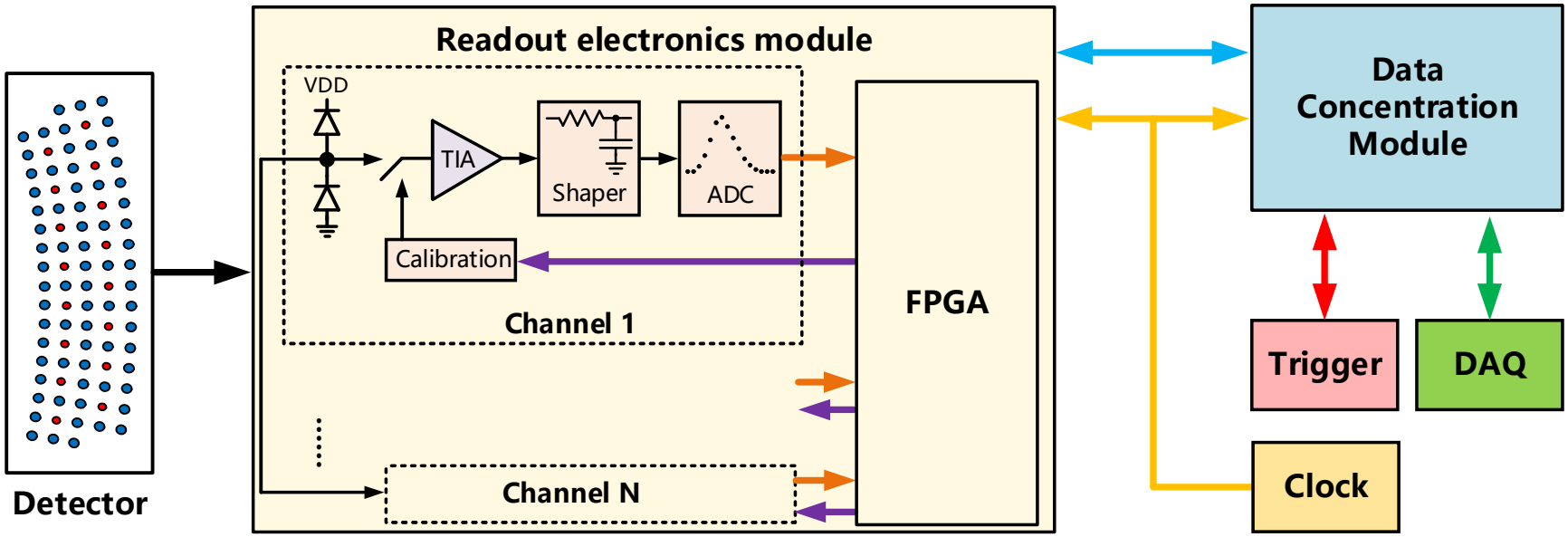
Structure of MDC electronics

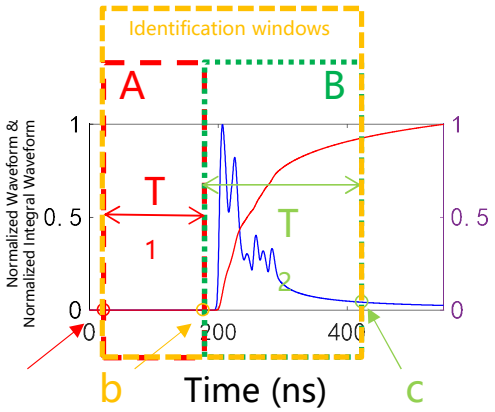
- Waveform digitization based electronics for Q & T readout of high count rate MDC



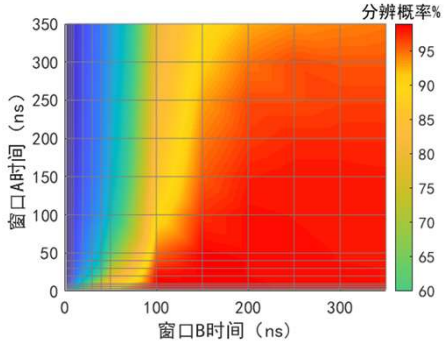
- Step of R&D
  - Phase I: principle verification module
  - Phase II: discrete component based prototype module
  - Phase III: ASIC based prototype module

Online algorithm of waveform identification

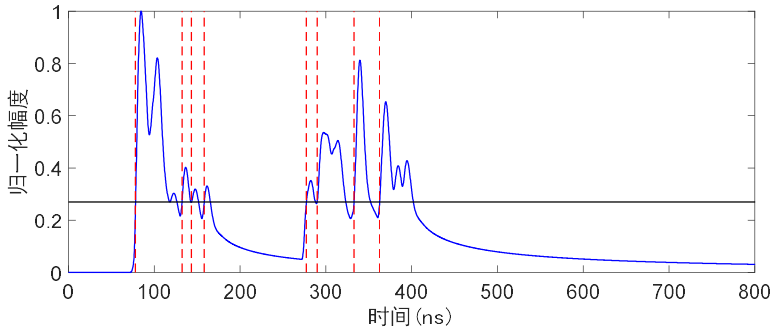
- **Proposed targeted waveform discrimination algorithm**
  - Perform over threshold judgment on the digitized waveform, extract information from over threshold data points, and obtain waveform resolution window based on the over threshold information
  - Extract the integral curve within the waveform resolution window
  - Transform the curve and find the peak value of the transformed curve
  - Calculate the starting position of the waveform through inverse transformation
  - Starting time selection



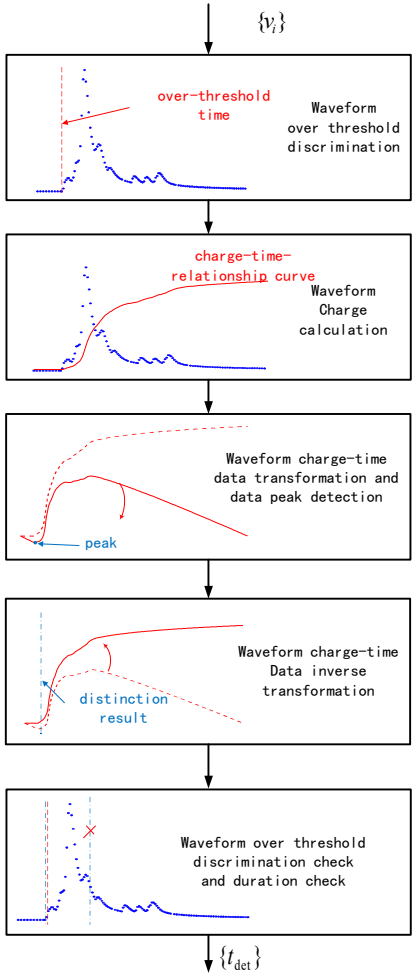
Identification time window definition



Identification rate vs window A and window B



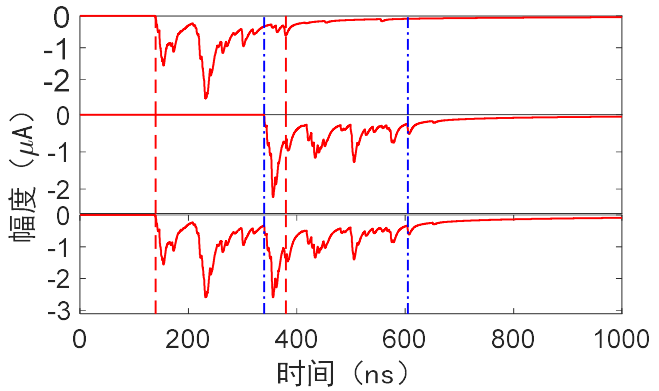
Slide time window for identification



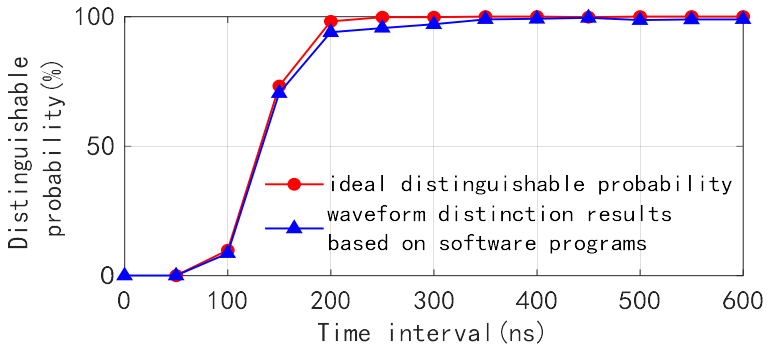
Flowchart of Algorithm

Online algorithm of waveform identification

- Detector simulation
  - Geant4 & Garfield++
  - Muon, proton, electron, kaon, pion…
  - Energy from 50 MeV to 1 GeV
- Electronics simulation
  - TIA + waveform digitization + online algorithm based on FPGA
- Identification rate is **95.8%**



Aliased waveform of adjacent signals

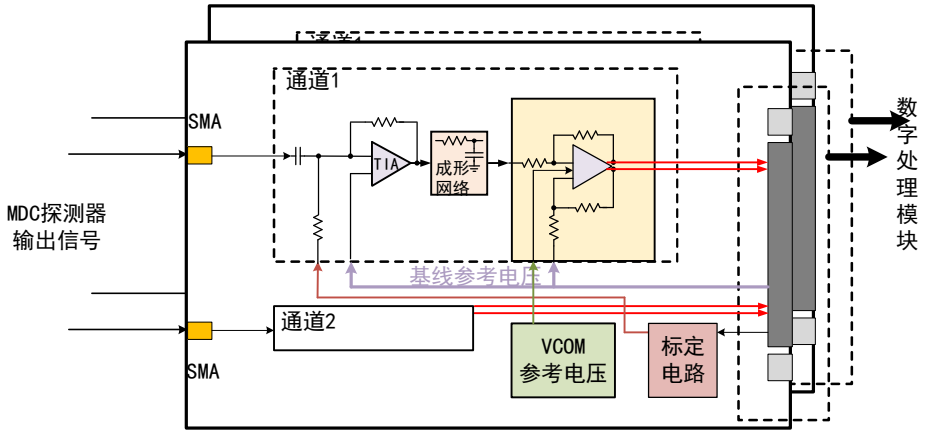


verification results of waveform detecting logic based on a software program

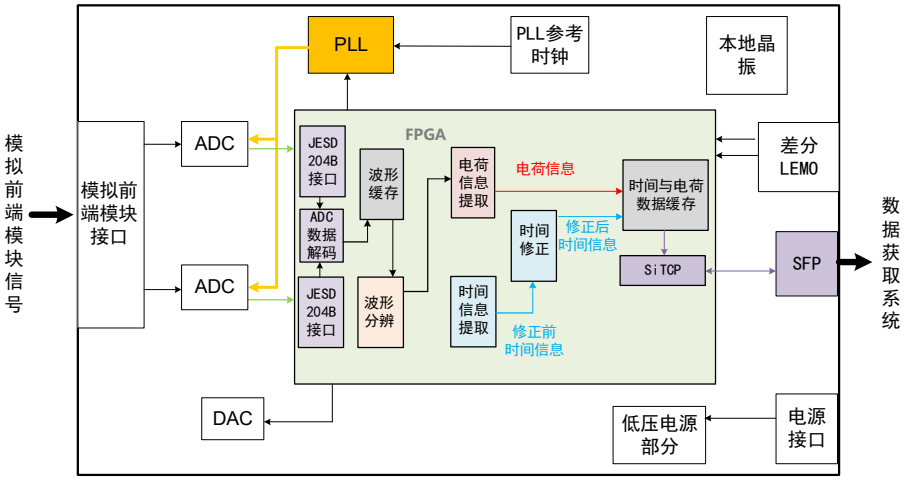
Gu J, et al. NIMA, 2024, 1064. DOI:10.1016/j.nima.2024.169353

Prototype readout electronics of phase I

- **Mother and daughter boards structure (4 ch)**
- **Daughter board (2 ch / board)**
  - TIA + shaper + single-end to differential amplifier
  - Gain: 20 kΩ
  - BW: 80 MHz
- **Mother board (Support 2 daughter boards)**
  - High speed ADC
    - 2 channels
    - 14 bits and 1 Gsps (for verification)
    - BW: 2 GHz
  - PLL
    - JESD204B compatible for ADC and FPGA
  - FPGA
    - XCKU060, verify for more channels in next phase
    - RocketIO for ADC and data interface
    - RAM for data cache
    - Logic for online calculation



Scheme of daughter board



Scheme of mother board

Prototype readout electronics of phase II

- **Analog Section**
  - TIA design inherited from the previous version, expanded from 2 to 16 channels.
  - Integrated 16-channel test interface to reduce noise introduced by external test boards.
- **ADC Section**
  - Replaced with a lower-sampling-rate, higher-integration ADC based on simulation results.
- **Digital Section**
  - Updated to accommodate the new ADC and 16-channel TIA architecture.

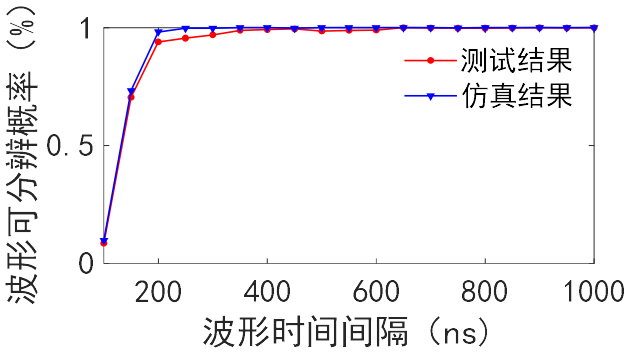
2 daughterboards + 1 motherboard for 4 channels

16-channel prototype system

Electronics tests

➢ Waveform identification

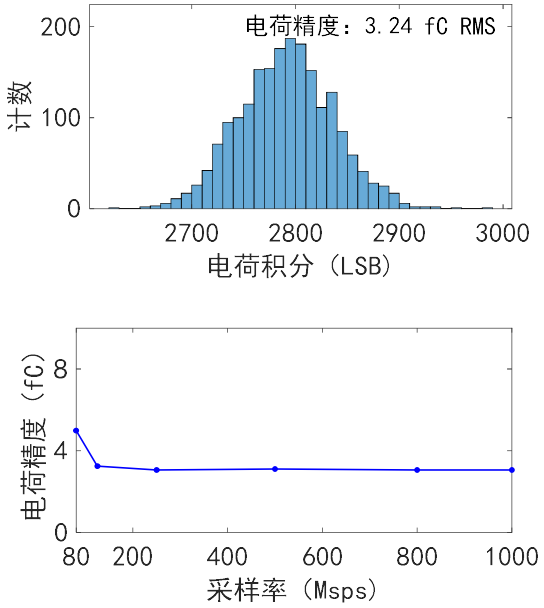
- above 95% at 125 Msps



Identification rate in different waveform duration at125 Msps

➢ Charge measurement

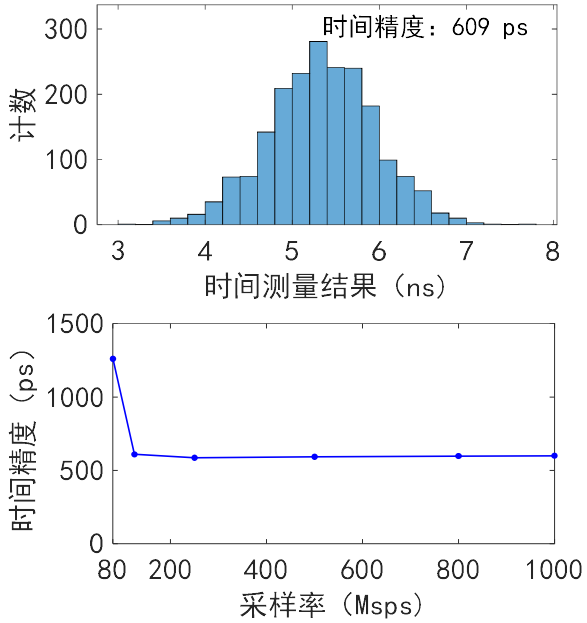
- 200 fC in different sample rate
- 3.24 fC RMS at 125 Msps



Charge resolution of 200 fC in different sample rate

➢ Time measurement

- 200 fC in different sample rate
- 609 ps RMS at 125 Msps

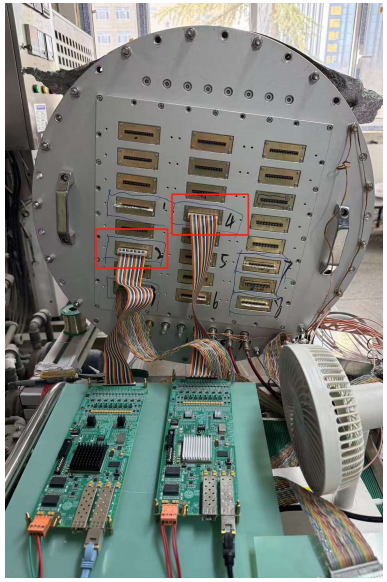


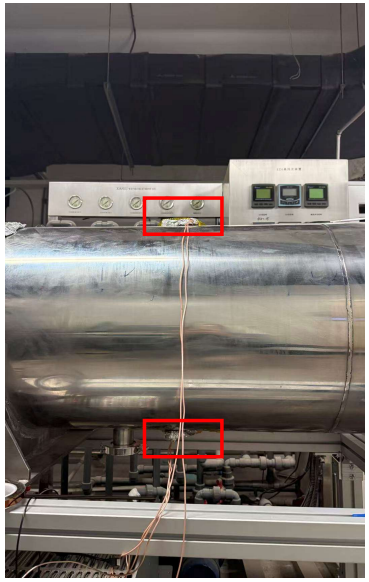
Time resolution of 200 fC in different sample rate

Detector integration tests

➢ Test setup

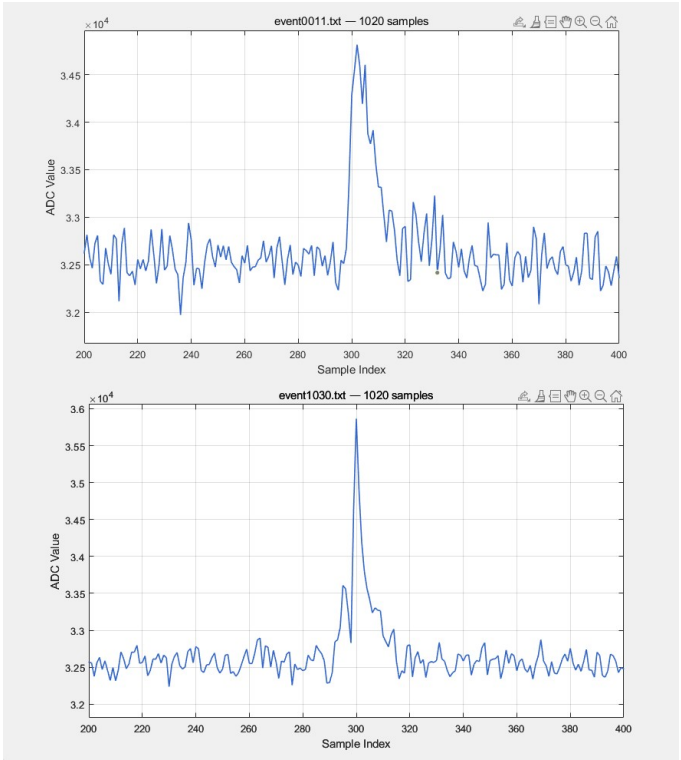
The upper and lower plastic scintillator pieces are used for external triggering, while the iron source signal adopts self-triggering





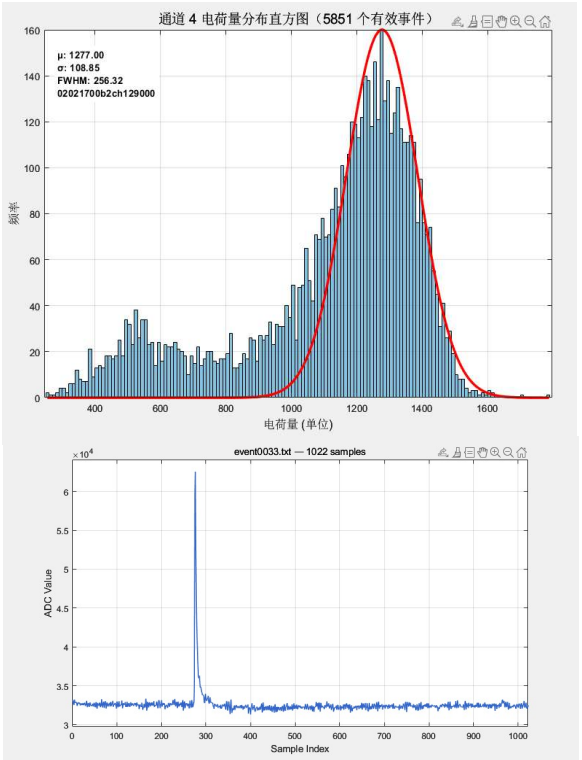
➢ Cosmic-Ray Test

Waveforms collected from the test show a clear multi-peak structure



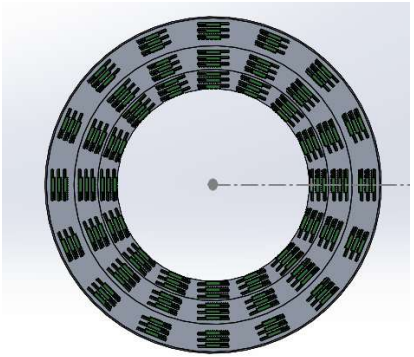
➢ Iron source testing

The measured ^{55}Fe spectrum resolution: ~21% (FWHM)

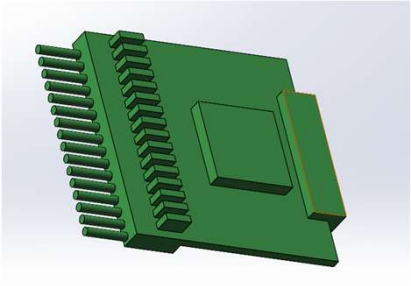


Prototype readout electronics of phase III

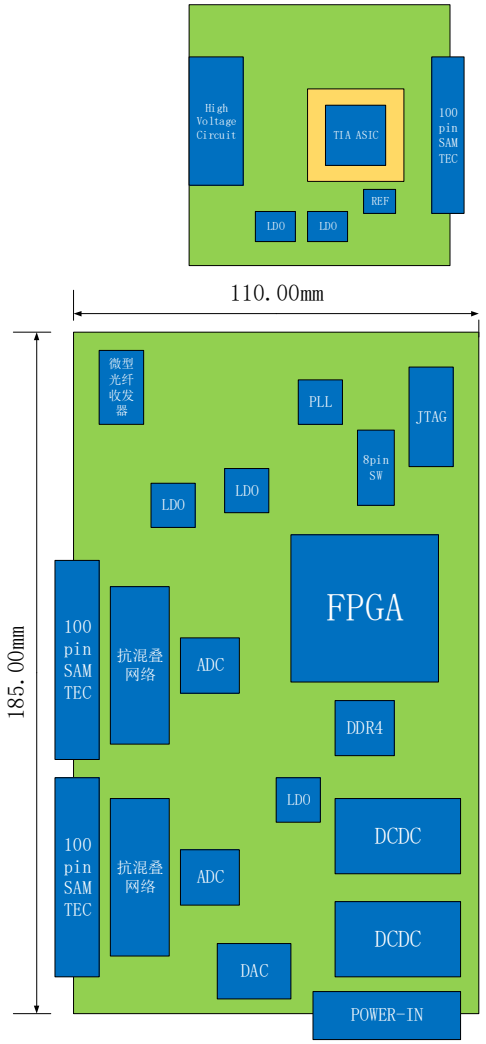
- **Improve on phase II electronics**
  - Design for the final MDC detector
  - Separate of analog board and digital board for installation
  - improves the overall level of integration
- **Analog board**
  - In the MDC
  - High voltage supply
  - Self developed ASIC (more detail later)
- **Digital board**
  - Out of the detector
  - Analog to digital converter
  - Online data processing in FPGA
  - Interface to trigger system and DAQ
- **On developing**
  - Reduce material budget



3 layers and 16 analog boards per layer



65 × 50 mm with 13 mm spacing



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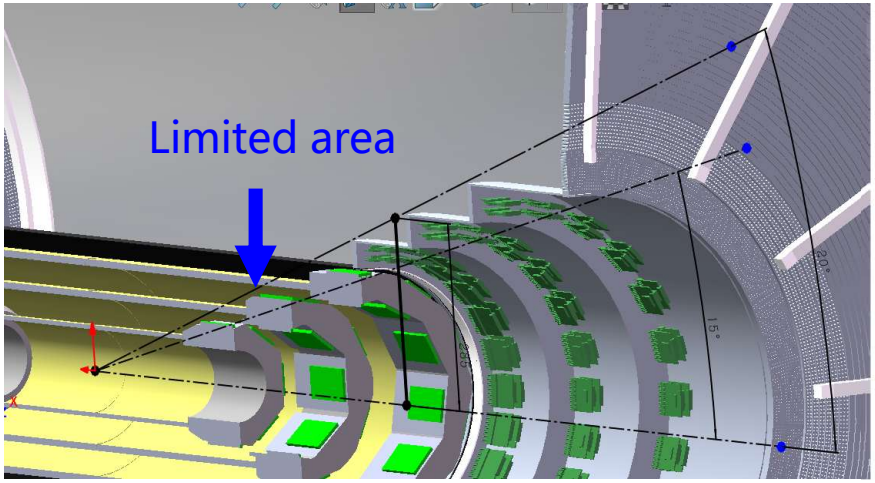
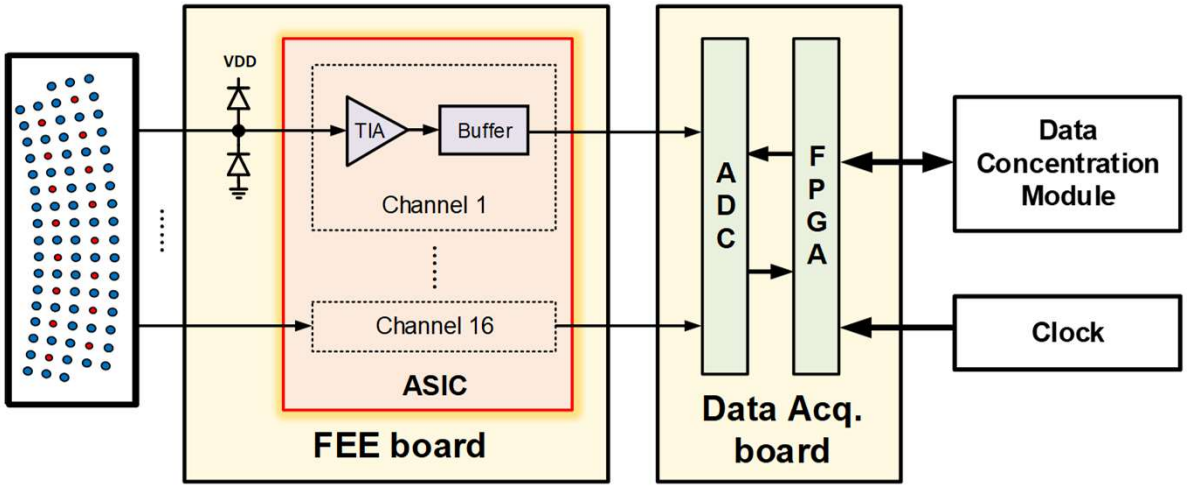
Requirements of MDC Front-end ASIC

- **To achieve a high-density and compact readout electronics of MDC, it is necessary to use the Application Specific Integrated Circuit (ASIC).**



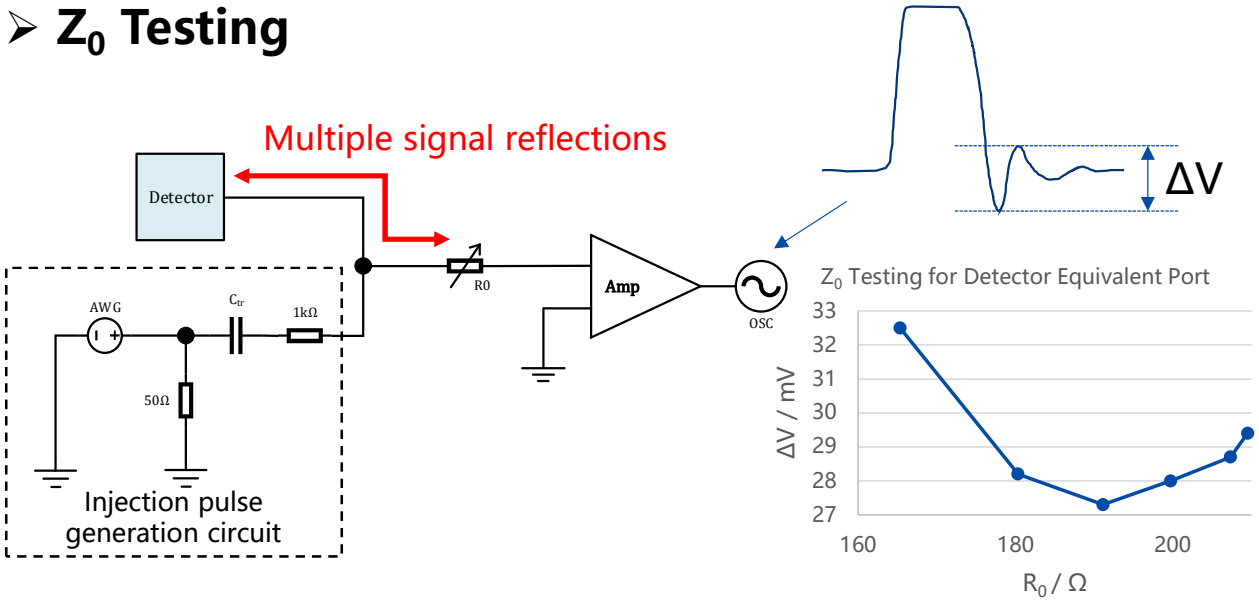
Structure of the MDC and its readout electronics



Block diagram of the readout electronics

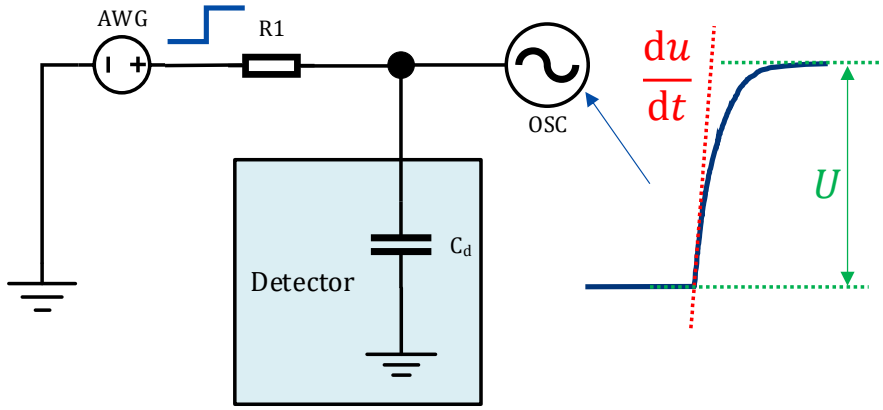
Z_0 and C_{eff} Testing for Detector Equivalent Port

➢ Z_0 Testing



- Optimize R_0 to minimize the reflection peak-to-peak value ΔV
- Since $Z_0(f)$ is frequency-dependent, the reflection cannot be perfectly canceled
- Combined with the input impedance of the Amp (24 Ω), the detector impedance is obtained as approximately **214 Ω**

➢ C_{eff} Testing

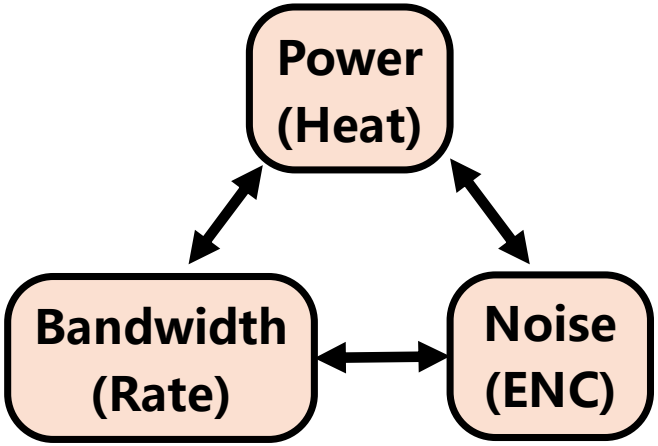


- A square-wave signal is injected into the detector via a known series resistor
- At the transition point, $I_{R1} = U/R1 = C_d \cdot du/dt$
- $\rightarrow C_d = \frac{U/R1}{du/dt} = \frac{0.1\ V/2\quad \Omega}{6.65\ MV/s} =$ **59 pF**
- Owing to distributed effects, this derived capacitance differs from the static capacitance of the detector

Requirements of MDC Front-end ASIC

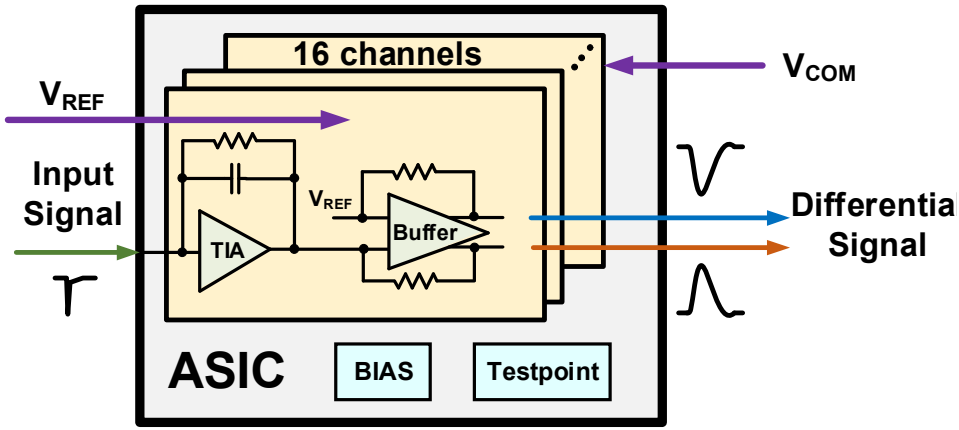
- **High integration** → **16 channels per chip**
- **Low noise & high bandwidth** → **Preamplifier works in the region between CSA and TIA**

Parameters	ASIC Requirements
Channels per chip	16
Maximum counting rate per channel	210 kHz
Charge measurement range	60 ~ 1800 fC
Area Equivalent Noise Charge (ENC)	< 8 fC RMS @ 50 pF C_{in}
Time resolution	≤ 1 ns RMS @ 50 pF C_{in}

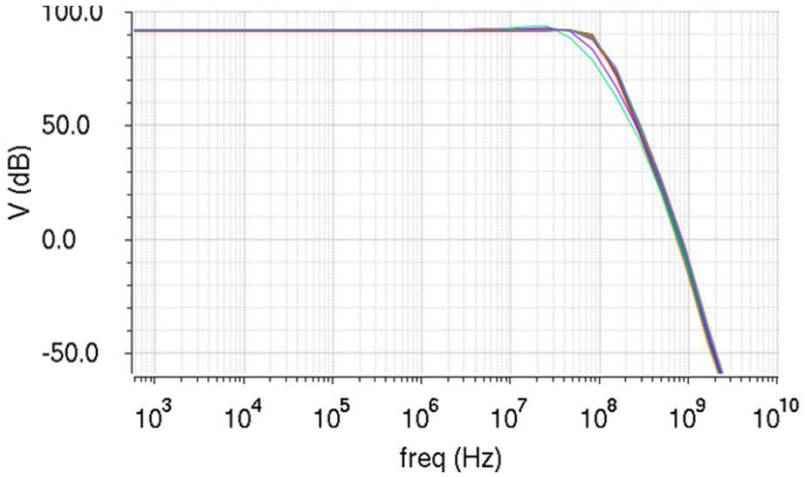


Design of the 1st version MDC ASIC

- **The design has undergone detailed optimization**
  - Size of input transistor is designed to match the MDC detector
  - Impedance of C_f is similar to R_f to perform low noise & high bandwidth
  - Low noise bias network
  - ……



Block diagram of the ASIC

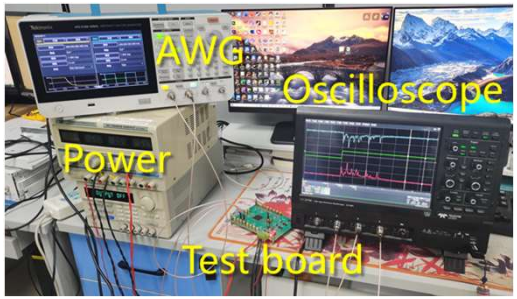


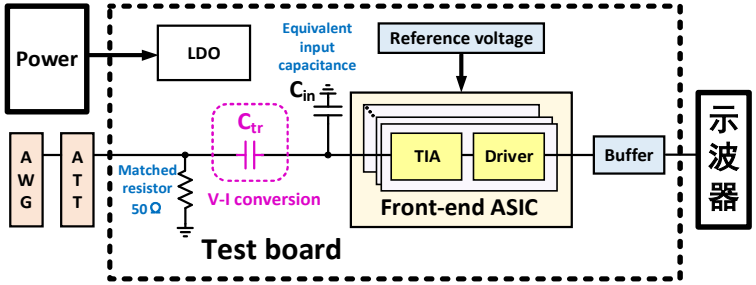
Magnitude response of the ASIC

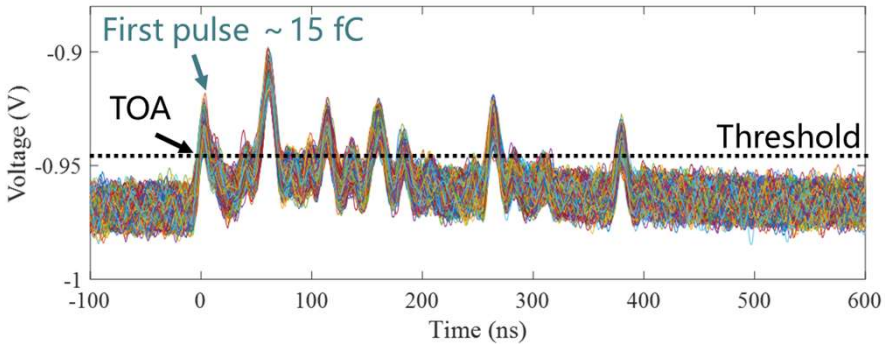
Electronics tests of the 1st version

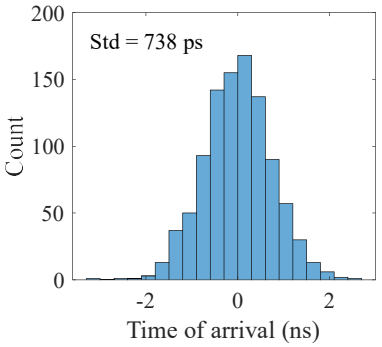
➢ Test setup

- AWG with a V-I conversion circuit is used to simulate the signal output by the MDC
- The typical MDC waveform is sent repeatedly to the front-end ASIC for measurement





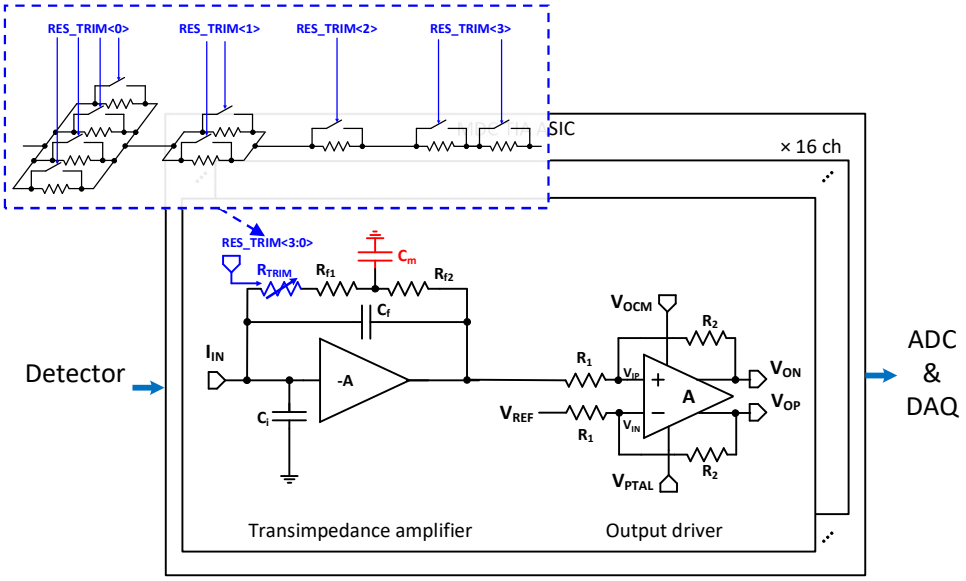




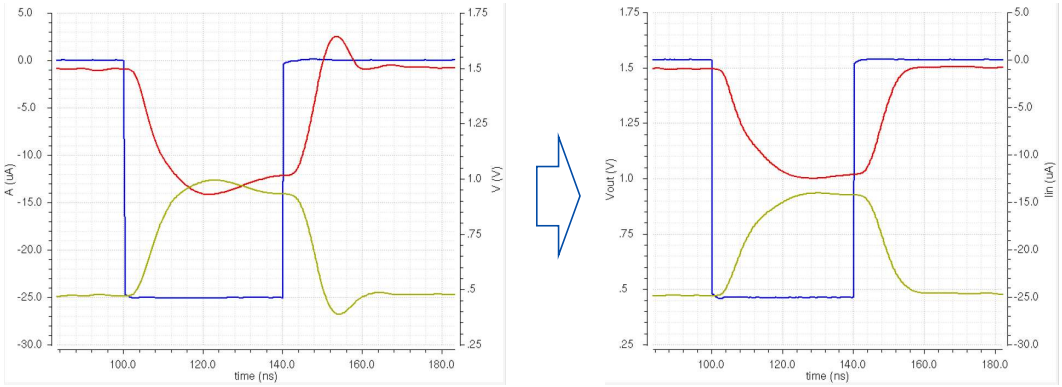
	Requirements	Test results
Area ENC	< 8 fC	< 2.9 fC
Timing resolution	< 1 ns	< 750 ps
Power consumption	< 349 mW/chn.	49.5 mW/chn.

Optimization in the 2nd version

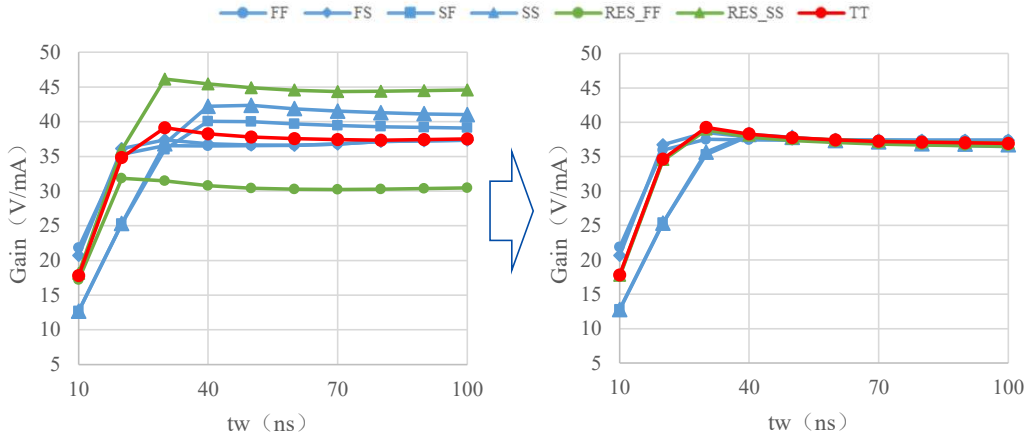
- Optimized feedback topology to improve circuit stability
- 16 different feedback resistance options have been designed and can be adjusted



Optimized ASIC Circuit Architecture



System Overshoot Optimization Simulation



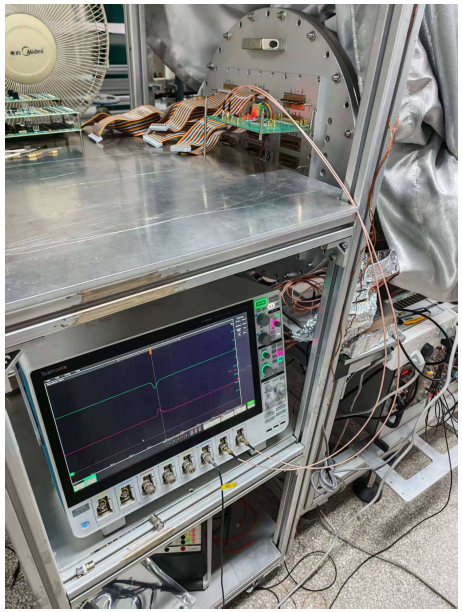
Suppressed Gain Deviation Against Process Variation

Detector integration tests of the 2nd version

➢ Test setup

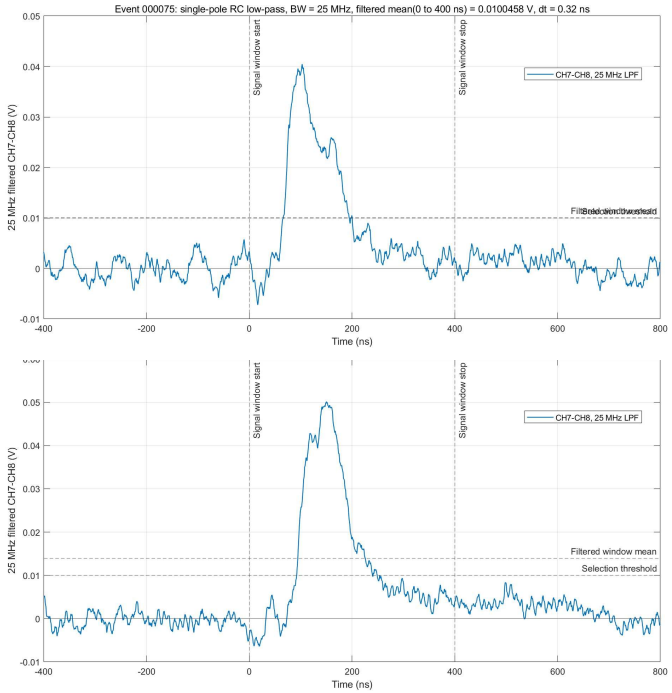
The same testbench as readout electronics evaluation

Readout by 3.125 Gsps 12-bit 500 MHz oscilloscope



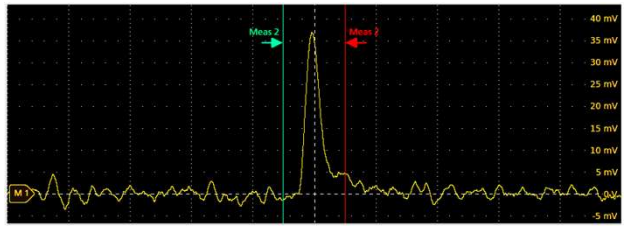
➢ Cosmic-Ray Test

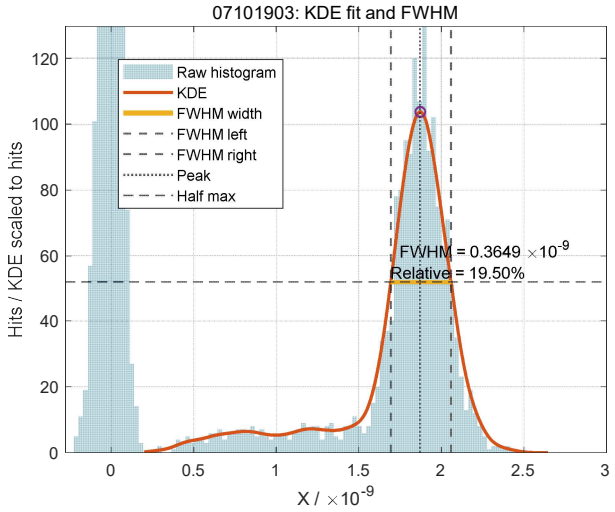
Waveforms collected from the test show a clear multi-peak structure



➢ Iron source testing

The measured ^{55}Fe spectrum resolution: ~20% (FWHM)





Outline

1. Overview of STCF
2. Progress on Discrete Electronics
   a) Online algorithm of waveform identification
   b) Prototype readout electronics: phase I, II, III
   c) Electronics tests & Detector integration tests
3. Progress on the ASIC
   a) Design and testing of the 1st & 2nd version MDC front-end ASIC
   b) Electronics tests & Detector integration tests
4. **Summary**

Summary

➢ Phased research results

- Online algorithm of waveform identification for high rate MDC
- 16-channel prototype electronics system
- High-integration, low-noise, high-bandwidth self-developed ASIC

➢ Electronics test

- Algorithm

  Identification rate is above 95% at 125 Msps
- Discrete Electronics

  Charge resolution of 200 fC is 3.24 fC RMS at 125 Msps

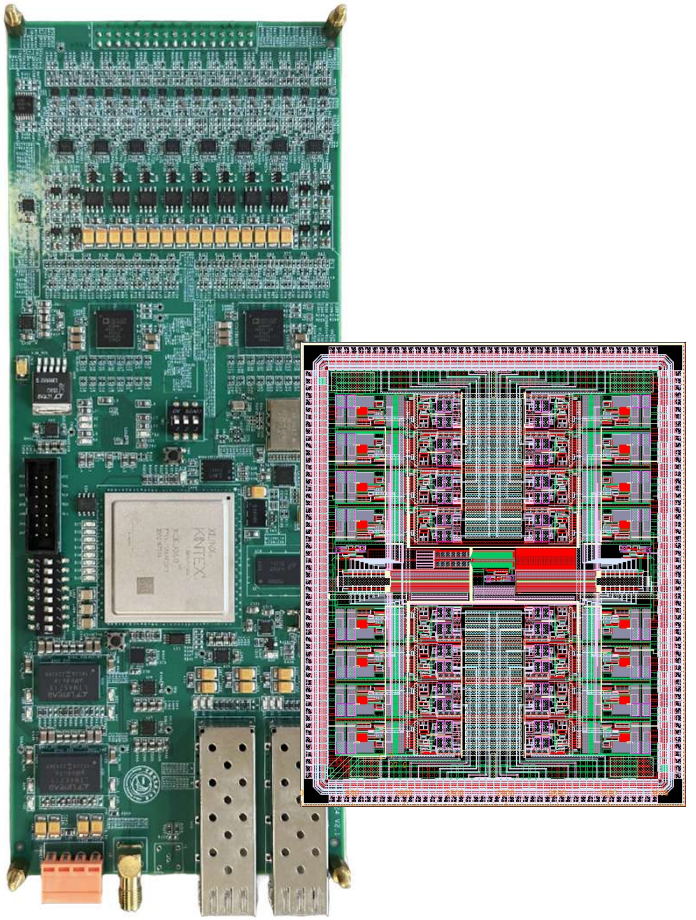
  Time resolution of 200 fC is 609 ps RMS at 125 Msps
- ASIC

  Charge resolution of 200 fC is 2.9 fC RMS

  Time resolution of ~15 fC is 750 ps RMS

➢ Detector integration tests

- Clear multi-peak structure for Cosmic-Ray
- Measured ^{55}Fe spectrum resolution: ~20% (FWHM)



Thank you!