单片高压CMOS像素传感器研制进展

— 面向CEPC ITK 和 LHCb UP升级

COFFEE

CMOS SENSOR IN
FIFTY-FIVE NM PROCESS

周扬 (中国科学院高能物理研究所)

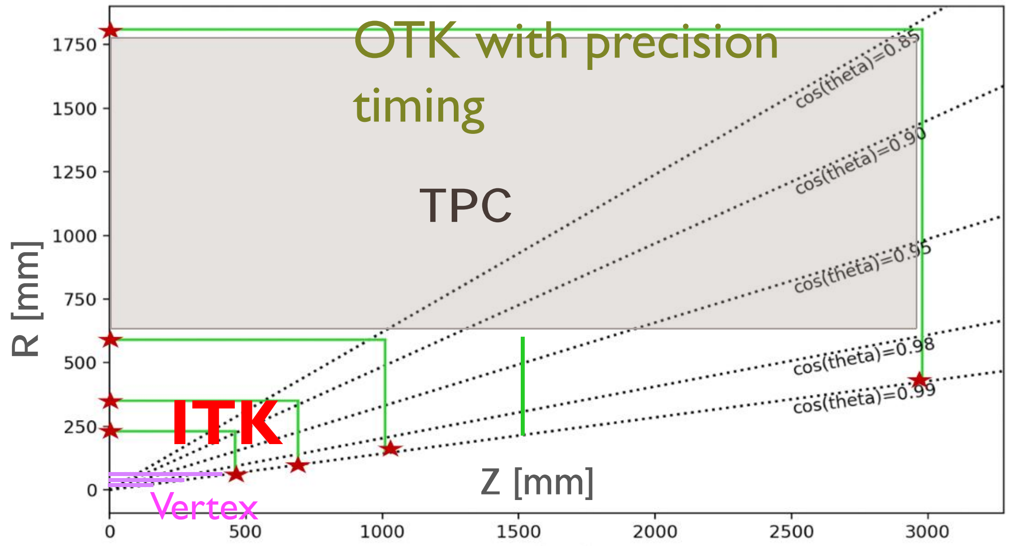
On behalf of the HV-CMOS pixel sensors in 55nm process collaboration

基于国产 55nm CMOS工艺平台

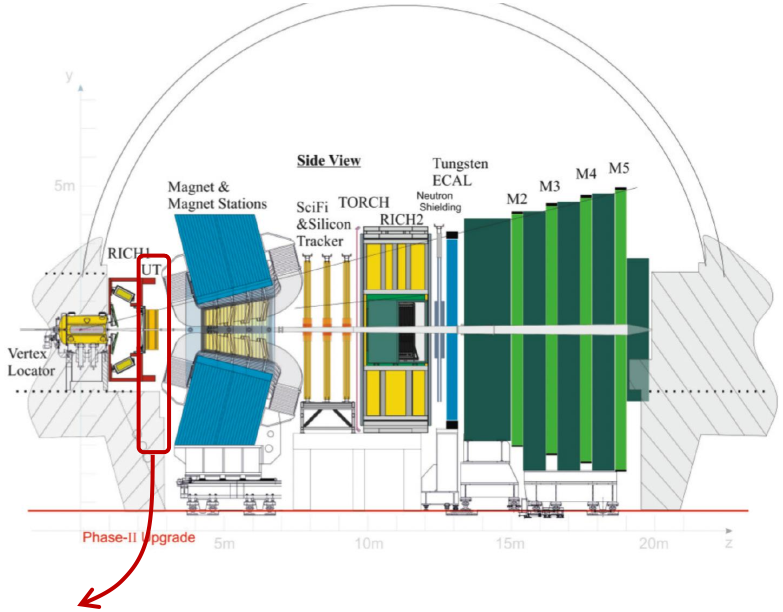
2026年超级陶粲装置研讨会, 西安，6. 30－7.5, 2026

研发背景和目标

两个应用场景需求驱动：

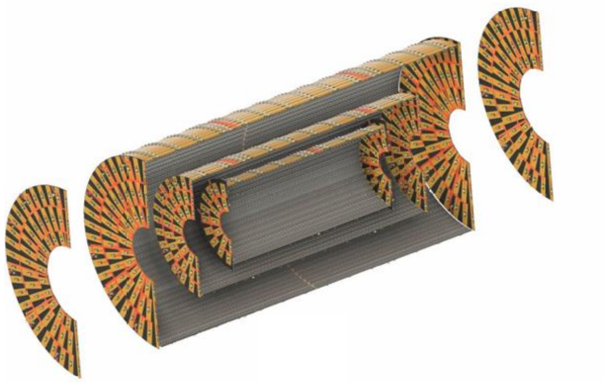


环形正负电子对撞机（CEPC） 内层径迹探测器 (ITK)

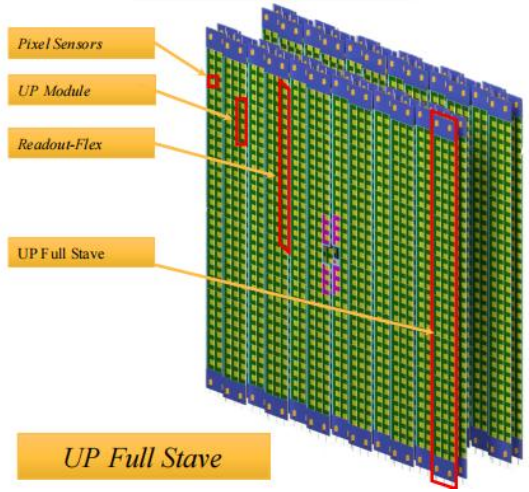


LHCb 上游径迹探测器二期升级（Upstream tracker upgrade II)

核心性能需求



CEPC ITK：3 barrels layers + 4 pairs of endcap disks



LHCb UP：4 layers of endcap

- **时间分辨: ~ 3 — 5 ns for 精确标记束团对撞时间**（precise tagging of bunch crossing ~23 ns for CEPC, 25ns for LHCb);
- **位置分辨: ~8 μm** in the R-φ (bending) direction for CEPC, with less stringent requirements for LHCb;
- **平均功耗: < 200 mW/cm^2 ;**
- **粒子击中率处理能力: > 100 Mhits/s/cm^2 for LHCb UP；**
- **抗辐照能力: 250 Mrad & $4\times10^{15}n_{eq}/cm^2$；**
- **芯片厚度（低物质量）： < 200** μm;

对探测器技术的挑战

由新物理信号精确测量的需求驱动，未来高能物理对撞机实验的亮度显著提升、测量精度需求更高，这对内层径迹探测器技术提出了前所未有的挑战：现有技术无法同时满足综合性能需求！

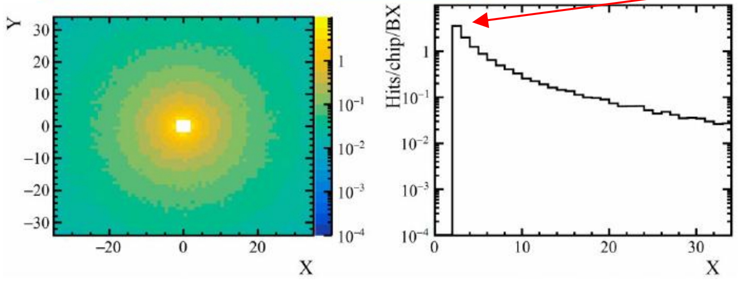
- 更高的击中率的处理能力！
- 更高的位置分辨精度！
- 更高的时间分辨精度！
- 更低的物质量（功耗）！
- 更高的抗辐照能力！

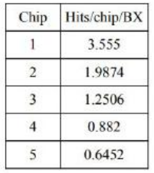
高压CMOS单片集成像素探测器（HV-CMOS Monolithic Pixel Sensor）作为基准技术方案，是最接近综合性能需求的技术类型，然而，国际技术前沿水平和目标需求仍有巨大差距，仅以高击中率的处理能力为例：

技术前沿和需求之间仍有显著差距！

LHCb UP二期升级

Minibias L=$1.0\times10^{34}\ cm^{-2}s^{-1}$

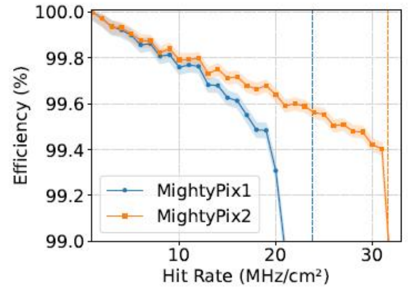




Chip	Hits/chip/BX
1	3.555
2	1.9874
3	1.2506
4	0.882
5	0.6452

极端位置芯片面临的击中率：

~100MHz/cm²



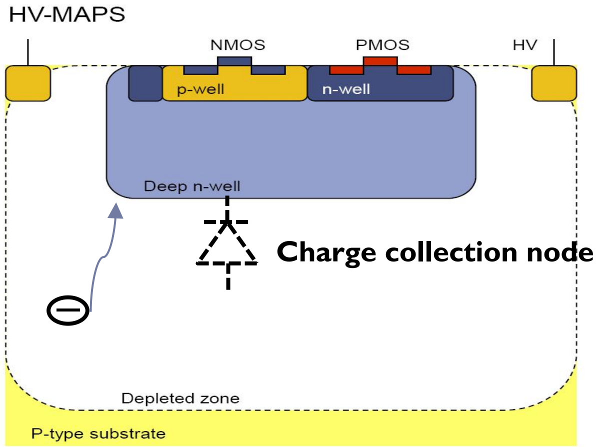
当前国际技术前沿芯片击中率处理上限在~30MHz/cm²

https://doi.org/10.1088/1748-0221/19/04/C04045

HV-MAPS：高压CMOS单片集成像素探测器

目标综合设计指标

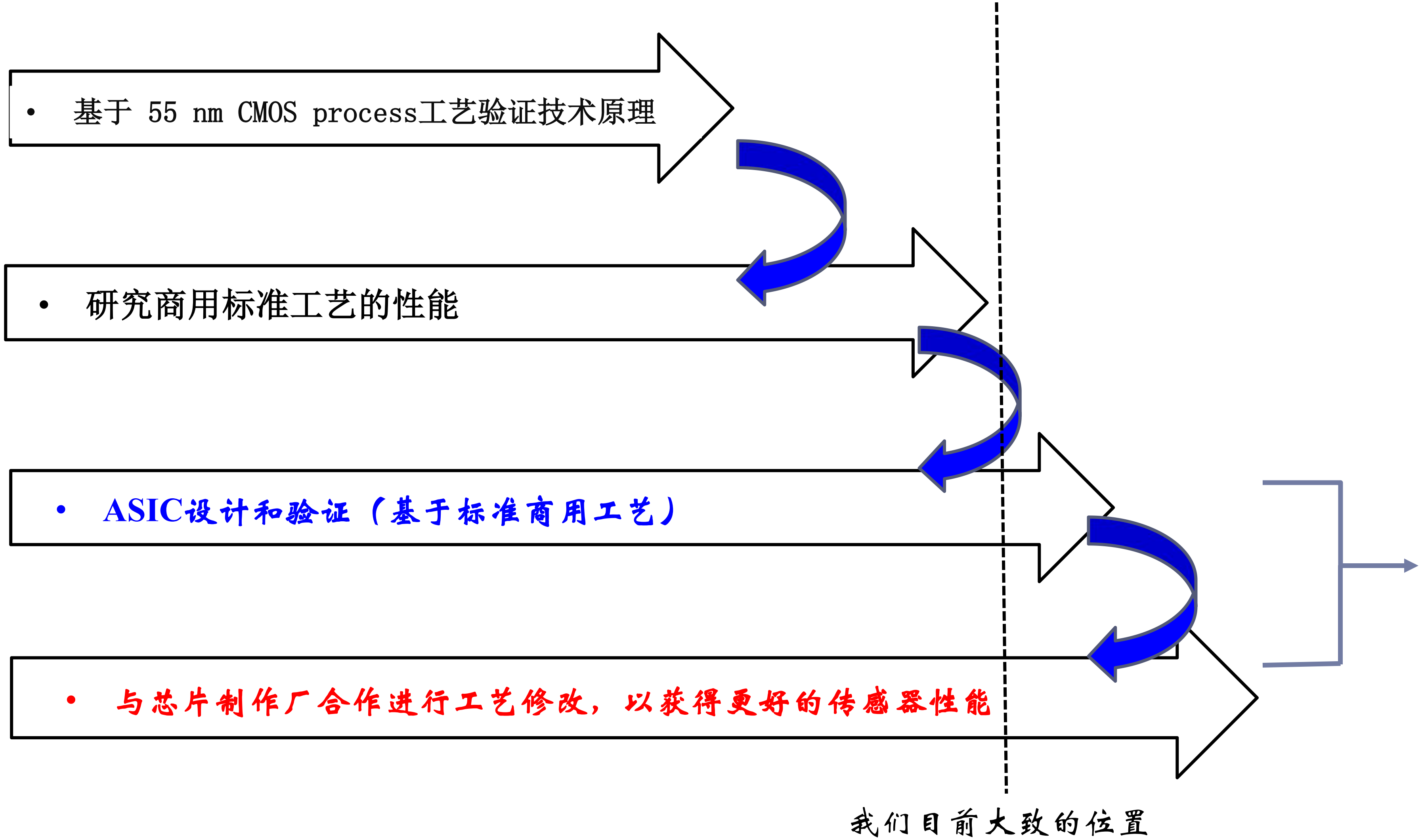
Performance Metrics	Sensor Design Specifications
Time resolution	~3–5 ns
Spatial resolution (Pixel size）	~ 30 μm × 150 μm
Power dissipation	< 200 mW/cm^2
Max hit rate	~100 MHz/cm^2
Radiation tolerance	250 Mrad & 4×10^{15} neq/cm^2
Sensor thickness	< 200 μm
Sensor dimension	~2cm×2cm，~90% sensitive area



典型 HV-MAPS的横截面（包含一个像素）简要示意图.

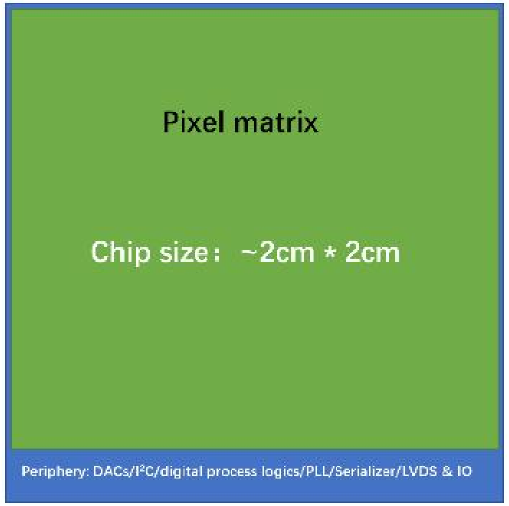
- 传感器可以实现全耗尽，天然具有快速的信号收集和较好的抗辐照能力（NIEL）；
- 该技术类型的探索始于2000年初，目前国际上已研发设计出多款芯片，整体性能表现出色. Such as ATLASPix， MuPix，LF-MonoPix，RD50-MPW series ，RadPix，MightyPix …… (均基于 180 nm/150 nm CMOS 工艺设计制作).
- 我们基于国产55 nm CMOS工艺平台，研究旨在同时满足两类应用场景的整体性能需求，同时为高能物理领域拓展MAPS技术的工艺选型空间（目前非常稀有，尤其是在先进工艺节点）.

并行开展的主要任务



- 基于 55 nm CMOS process工艺验证技术原理
- 研究商用标准工艺的性能
- **ASIC设计和验证（基于标准商用工艺）**
- **与芯片制作厂合作进行工艺修改，以获得更好的传感器性能**

我们目前大致的位置

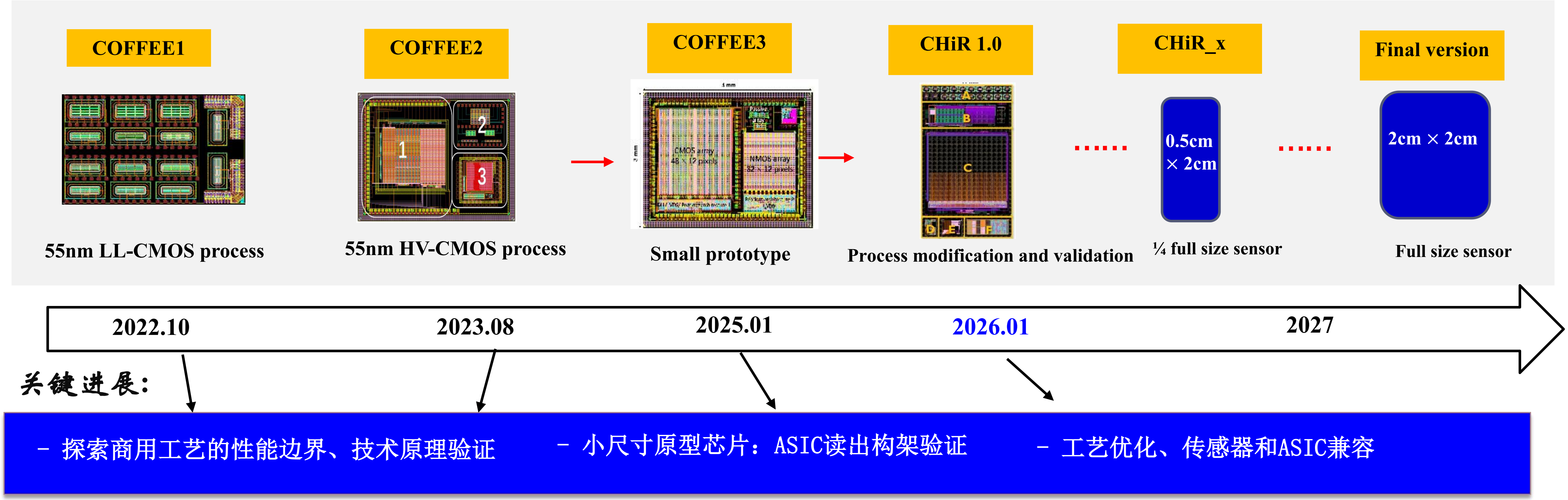


Performance Optimization Combining modified Process and Validated ASIC.

COFFEE 系列芯片研发路线图：CMOS sensOr in Fifty-Five nm process

需要逐步攻克的核心问题：

先进CMOS工艺上传感器的实现、ASIC读出构架、传感器和ASIC的兼容、全功能集成、大尺寸全功能芯片集成



COFFEE1 — 55nm LL-CMOS process

COFFEE2 — 55nm HV-CMOS process

COFFEE3 — Small prototype

CHiR 1.0 — Process modification and validation

CHiR_x — 0.5cm × 2cm — ¼ full size sensor

Final version — 2cm × 2cm — Full size sensor

2022.10

2023.08

2025.01

2026.01

2027

关键进展：

- 探索商用工艺的性能边界、技术原理验证
- 小尺寸原型芯片：ASIC读出构架验证
- 工艺优化、传感器和ASIC兼容

COFFEE2设计概要

三个独立的功能区域：以技术原理验证和工艺评估为设计目标

1. **Passive diode arrays：**
   - Various sensing structures: DNW size, distances, with/without P-stop；

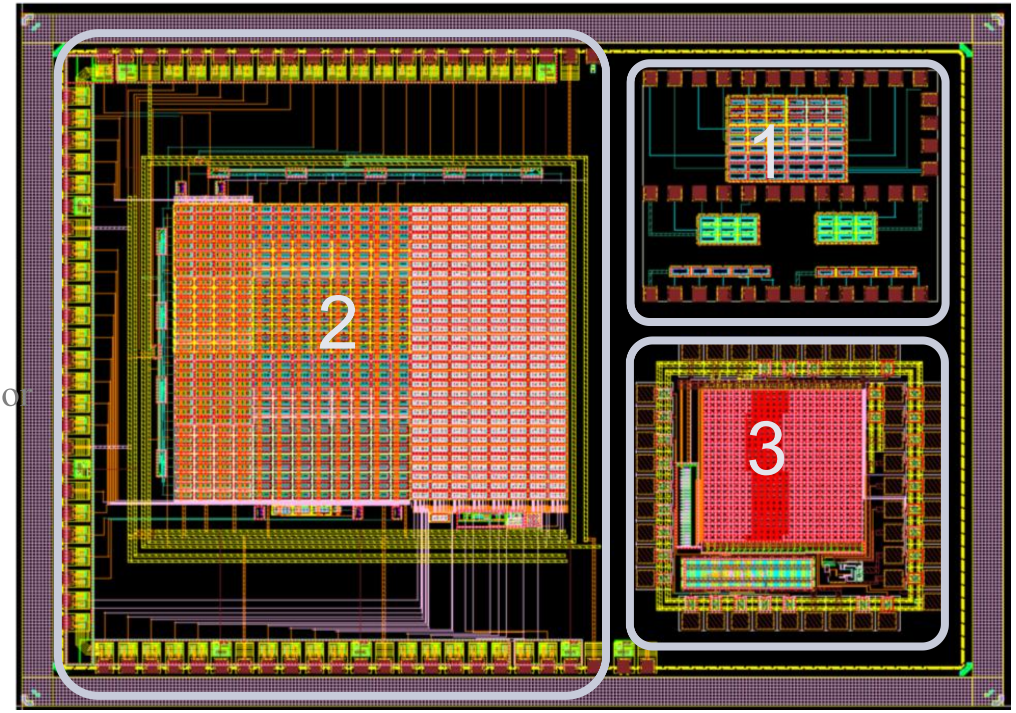
For the commercial process characteristics study

2. **An active pixel matrix including 3 variations of pixel design：**
   - To quantitatively evaluate the "cross-talk" issue of HV-CMOS pixel sensor technology in the new process and guide the overall design of the future detector chip

For charge sensing diode + in-pixel AFE study

3. **An active pixel matrix with a new readout architecture：**
   - Very small pixel size 25×25μm² (for a HV-CMOS pixel sensor);
   - New matrix readout architecture;
   - Digital peripheral data processing included;

For new architectures in 55nm process @ Designed by KIT



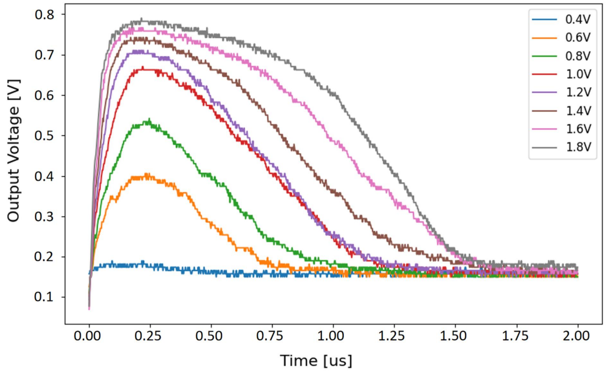
The COFFEE2 design includes three independent regions.

Published paper: 1. NIMA Volume 1069 P169905 (2024) https://doi.org/10.1016/j.nima.2024.169905;
2. 2025 JINST 20 C03023 . https://doi.org/10.1088/1748-0221/20/03/C03023;
3. 2025 JINST 20 C10011. https://doi.org/10.1088/1748-0221/20/10/C10011;

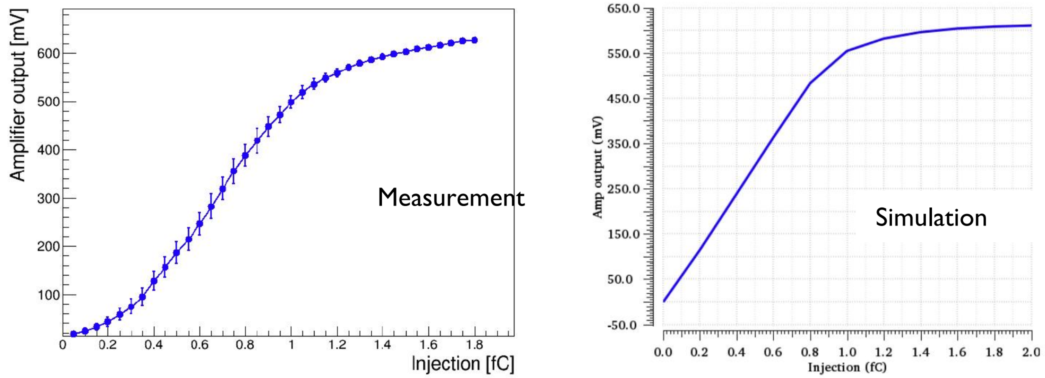
商用标准工艺性能评估: COFFEE2测试结果

COFFEE
CMOS SENSOR IN
FIFTY-FIVE NM PROCESS

- **The in-pixel amplifier & comparators work as the simulation predicts**

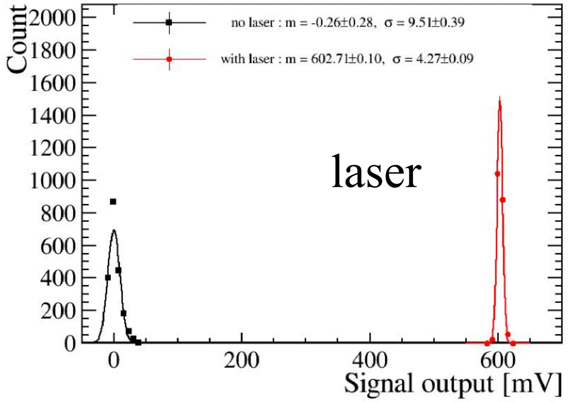


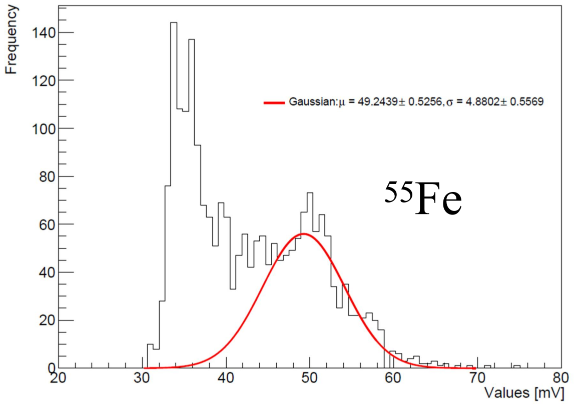
The CSA output versus different injection voltages

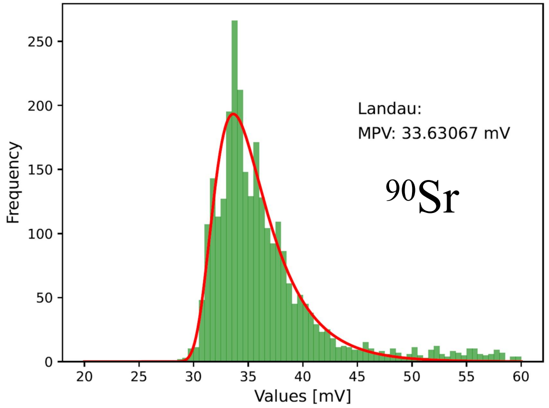


CSA output as function of charge injection

- **Clear response to laser/ ^{55}Fe / ^{90}Sr sources:** depleted depth ~ 10 μm @ sensor bias -30V

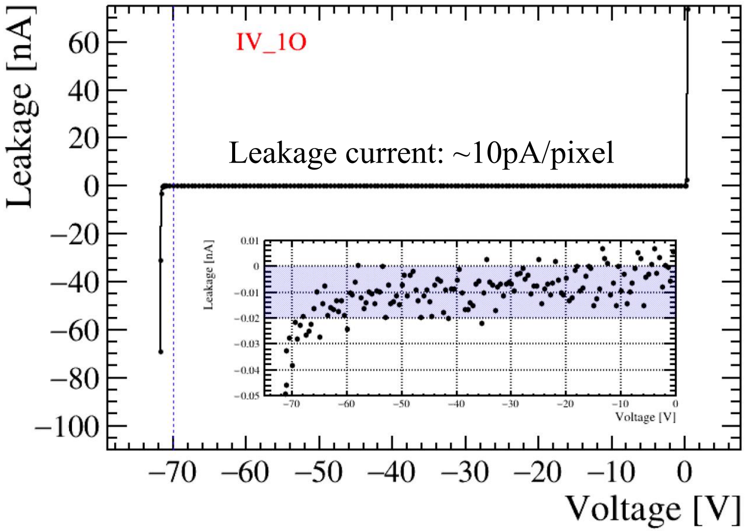






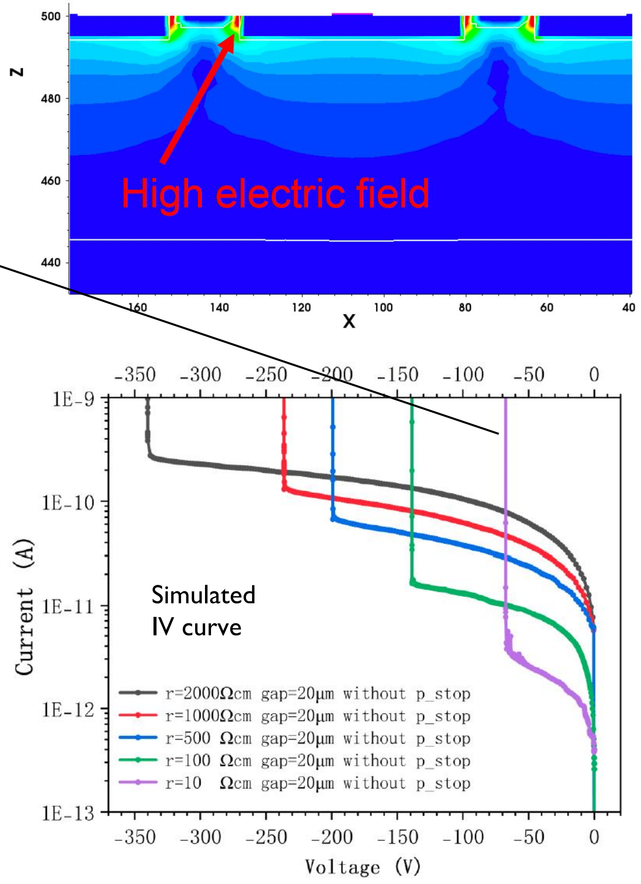
商用标准工艺性能评估: COFFEE2测试结果

- **工艺局限性1：击穿电压～-70V；主要瓶颈在于商用标准晶圆阻值 10 Ω·cm.**

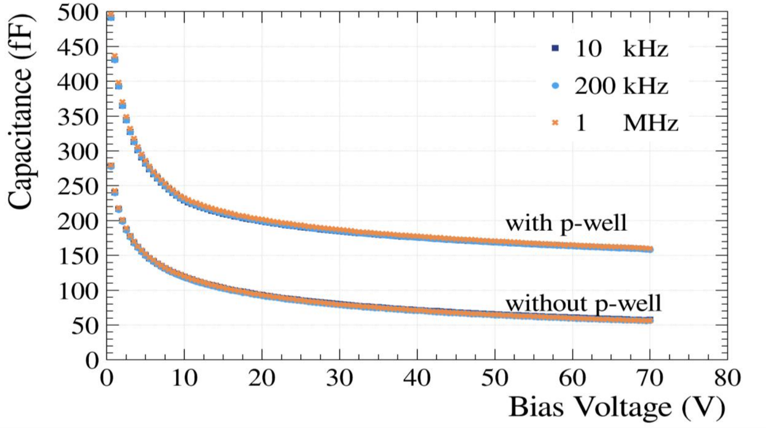


IV curve test result

Breakdown takes place between DNW and p-type surface. Lowering p-type concentration at DNW edge (using high-resistivity wafers) improves breakdown voltage.



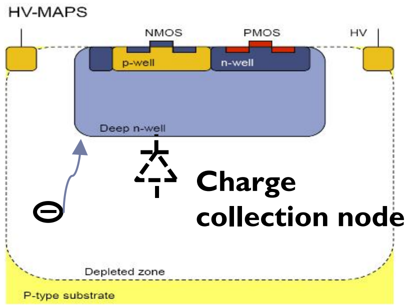
TCAD simulation



CV test results of a pixel with or without P-well inside.

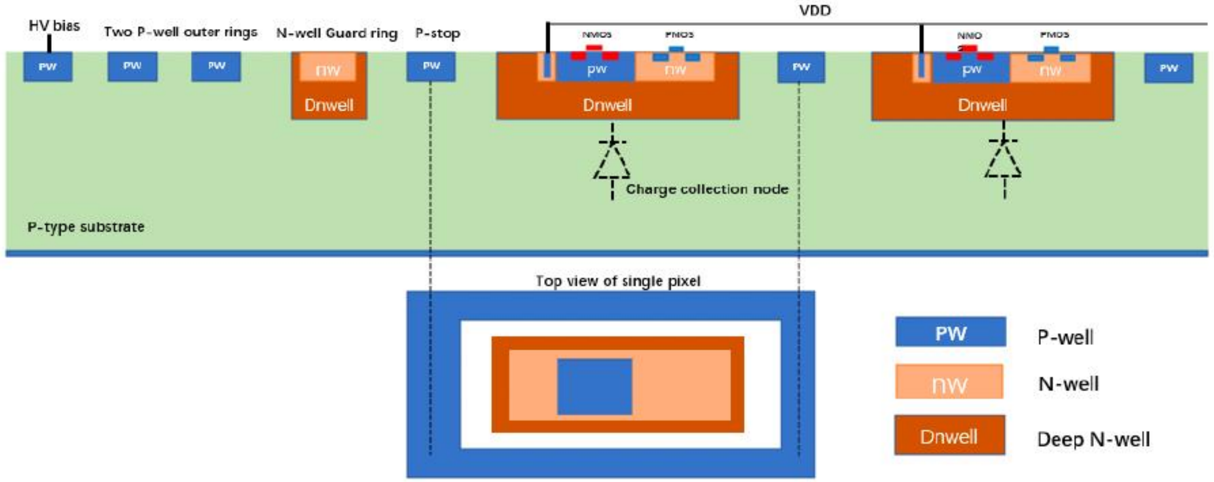
Pixel layout size:40×145 μm²

P-WELL inside version cover ~50% area of the pixel



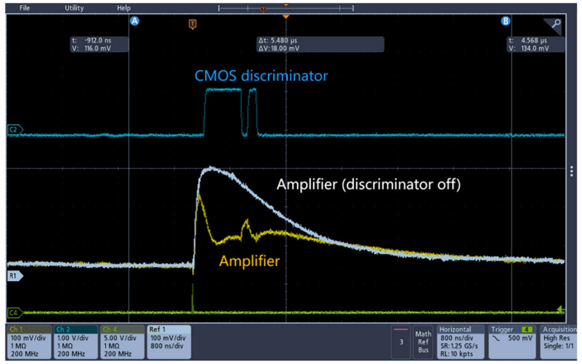
- **C_{diode} is ～200 fF, dominated by P-well-to-DNW capacitance.**

商用标准工艺性能评估: COFFEE2测试结果

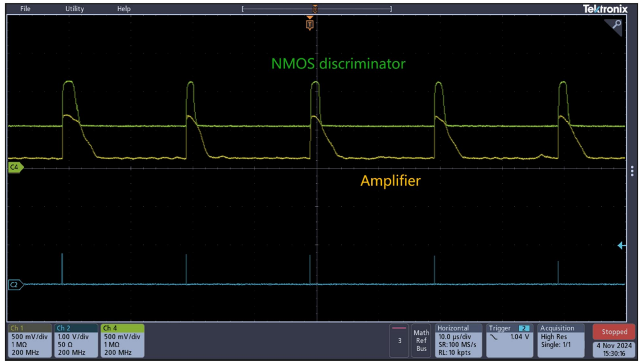


In-pixel CMOS comparator design

In-pixel NMOS comparator design



(a)



(b)

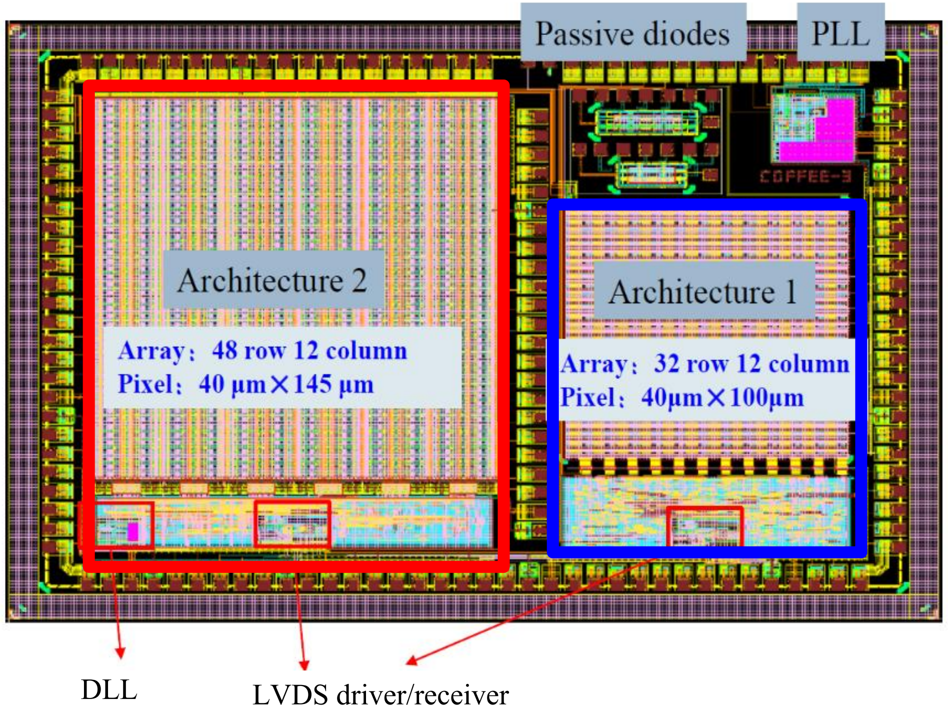
- ➢ 工艺局限性2：像素内ASIC设计

像素内数字信号的翻转，会通过N阱（PMOS管的bulk）引起传感深N阱端的抖动，进而被像素内放大器放大，引发“串扰”现象。可通过只使用NMOS管的像素内设计避免。

测试中观测的“串扰”现象：

- (a) CSA output when the CMOS discriminator on (yellow) and off (white) with the corresponding CMOS discriminator output (blue);
- (b) CSA output (yellow) when the NMOS discriminator on (green).

ASIC读出构架设计和验证：小尺寸原型芯片COFFEE3



COFFEE3 layout，3×4 mm².

核心设计：

- 两种独立的读出构架，设计均可扩展至全尺寸芯片（~2×2 cm²）；
  - 读出构架 1：像素内 NMOS设计，避免当前工艺条件下的“串扰”风险；
  - 读出构架 2：像素内CMOS设计，释放设计自由度，为未来可能的工艺修改做准备
- 均包含与阵列工作匹配的外围数字电路和必要的模拟IP；

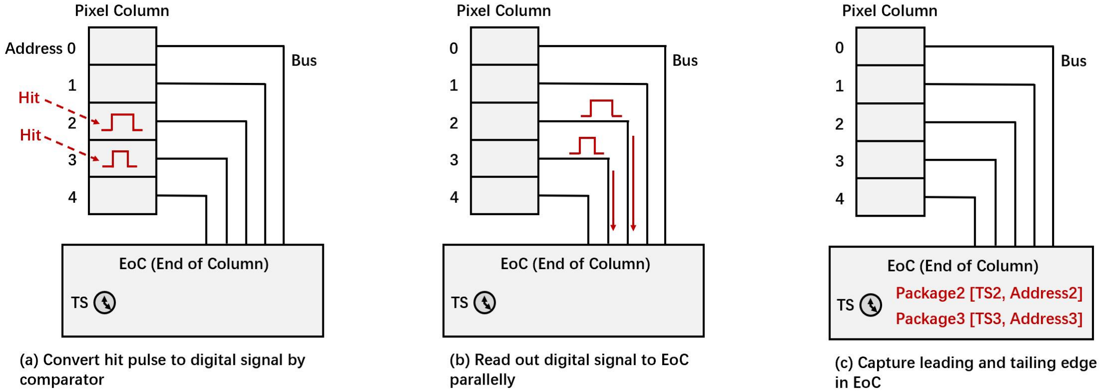
期望回答的问题：

1. 是否可以满足目标应用的综合性能需求？时间分辨、位置分辨、功耗、抗辐照能力等；
2. 先进工艺能够在哪些方面带来HV-MAPS技术类型性能瓶颈的突破？（180 nm -> 55 nm）

两种读出构架：各自的特点和潜在优势

读出构架 1：像素内使用NMOS比较器实现数字化，信号实时并行传输到列底端，在EoC部分添加时间戳、像素地址等信息。

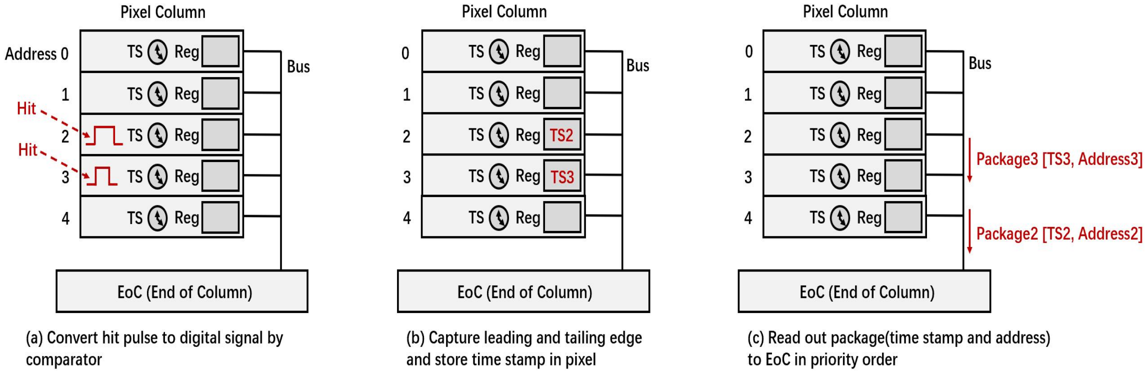
读出构架 2：在像素内集成TDC，信号脉冲的到达时间、结束时间和地址信息先存储在像素本地，再按优先级次序读出到列底端（EoC）



(a) Convert hit pulse to digital signal by comparator

(b) Read out digital signal to EoC parallelly

(c) Capture leading and tailing edge in EoC



(a) Convert hit pulse to digital signal by comparator

(b) Capture leading and tailing edge and store time stamp in pixel

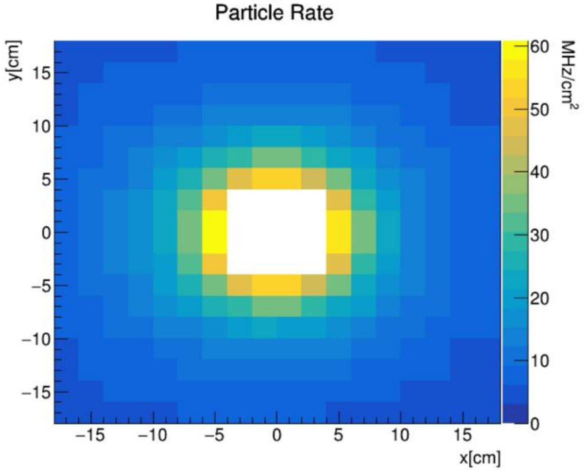
(c) Read out package(time stamp and address) to EoC in priority order

潜在优势:

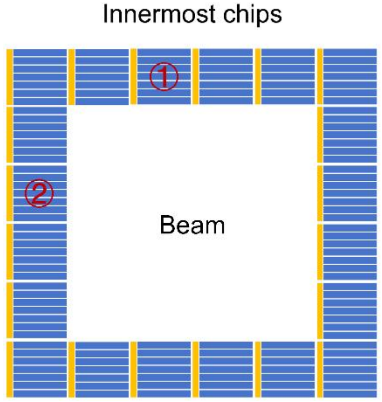
- 低功耗、高位置分辨精度

- 像素内更高的集成度，在高击中率场景下提供精确的时间信息；

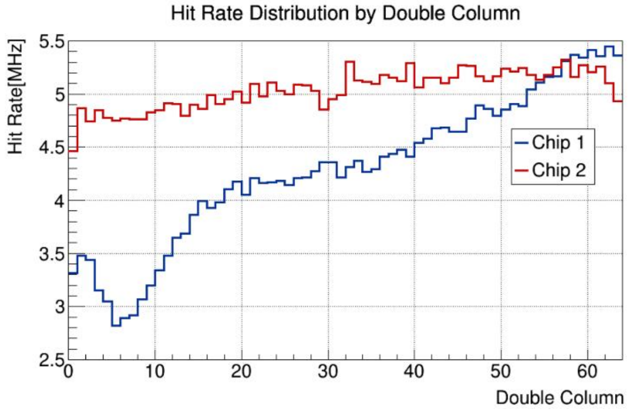
关键的设计指标：物理数据 --》芯片系统级仿真



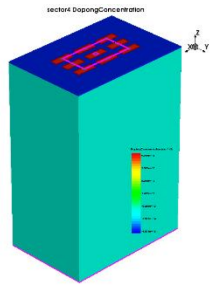
LHC未来升级后，LHb UP位置50,000 次系统对撞束团（BXID）物理仿真数据



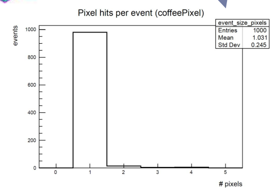
探测器上芯片的具体排布方式，以最终芯片摆放方式，确定最极端位置芯片的击中率情况



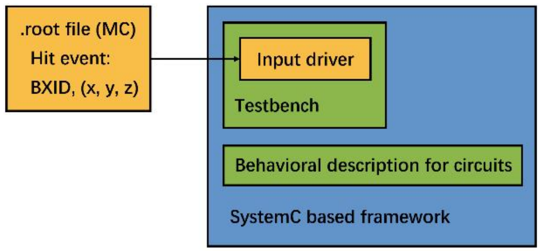
极端位置芯片，在芯片内部不同像素位置的击中率变化



TCAD给出电场条件



ALLpix²提供信号收集信息



.root file (MC)
Hit event:
BXID, (x, y, z)

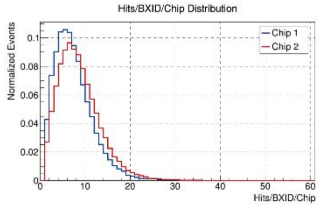
Input driver

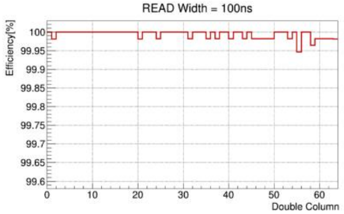
Testbench

Behavioral description for circuits

SystemC based framework

结合ASIC设计构架， 基于System C的给出芯片系统级仿真，保证 >> 99%的探测效率

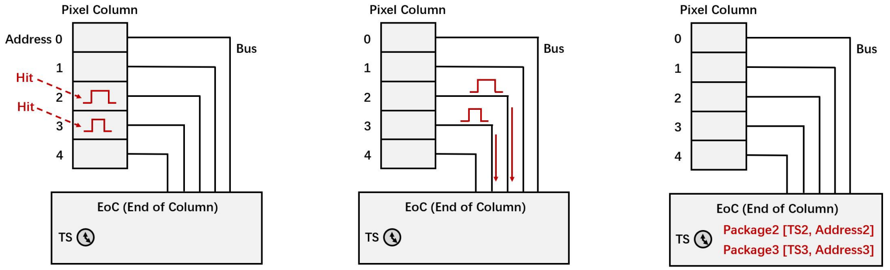




- **模拟pile-up**：模拟信号宽度；
- **数字pile-up**：数据读出速度、FIFO深度；
- **芯片数据吞吐量等**：片上数据压缩算法，二级数据汇总方案等

读出构架1的设计考虑: 加强高击中率处理能力

读出构架 1: 像素击中信号先并行传输到阵列底部

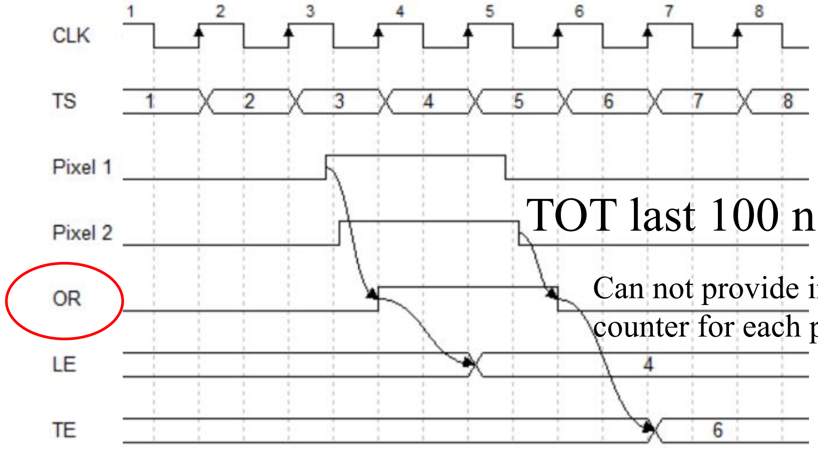


(a) Convert hit pulse to digital signal by comparator

(b) Read out digital signal to EoC parallelly

(c) Capture leading and tailing edge in EoC

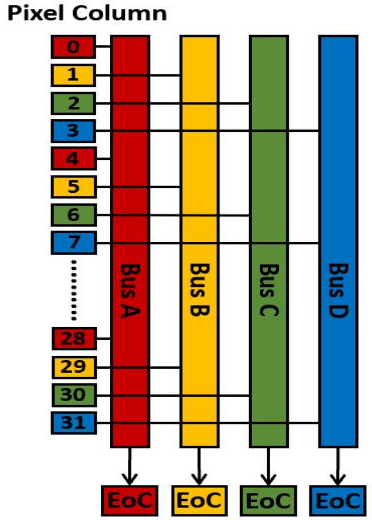
Each column shares an EoC module



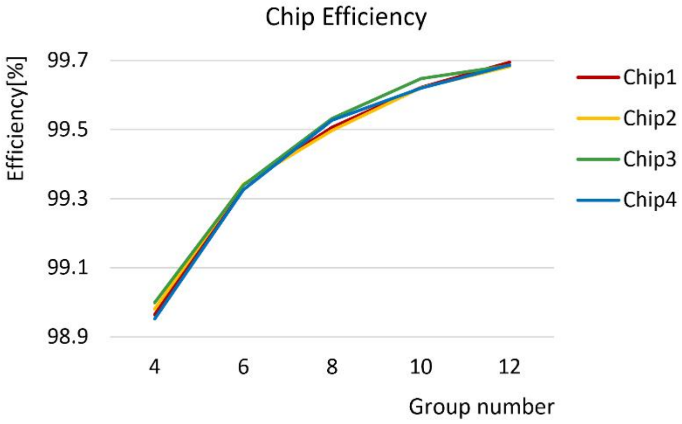
TOT last 100 ns -1.6 μs

Can not provide independent time stamp counter for each pixel at EoC

每列像素共享一个EoC处理模块



One pixel column architecture in COFFEE3.

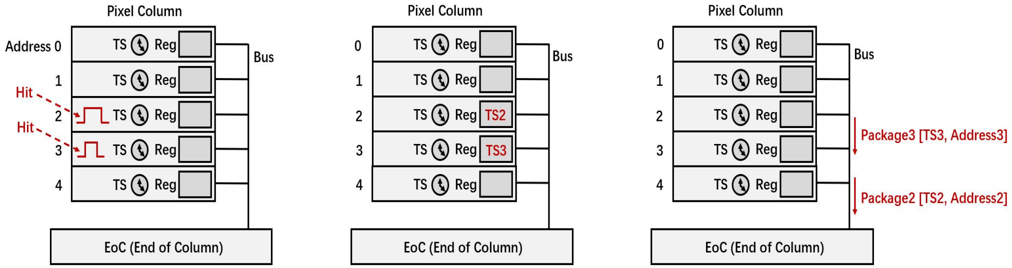


At UP extreme positions, digital logic induced efficiency loss is ~1%.

- 局限性: 击中率较高 (eg. > 数十 Mhz/cm²)
  - 时间标记信息会不准确;
  - 探测效率损失;
- 我们在阵列底部的数字算法设计中，对每列像素进行了分组和每组中也增加了额外的状态机，该设计在100Mhz/cm²的条件下，依然可以保证较高的探测效率（读出构架引入的探测效率损失 < 1%），并提供精确的时间标记。

读出构架2的设计考虑：更高的集成度、未来更多的可能性

读出构架 2： 击中信息先存储在像素本地，再按优先级次序读出到阵列底部。(Efficiency > 99.9% @ UP while READ ≤ 100 ns).

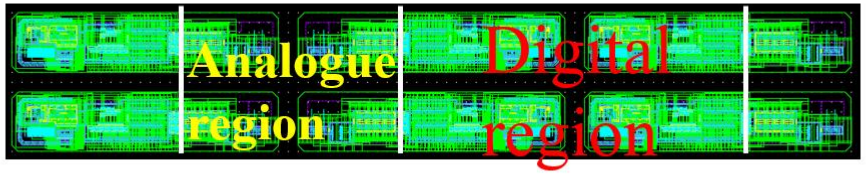


(a) Convert hit pulse to digital signal by comparator

(b) Capture leading and tailing edge and store time stamp in pixel

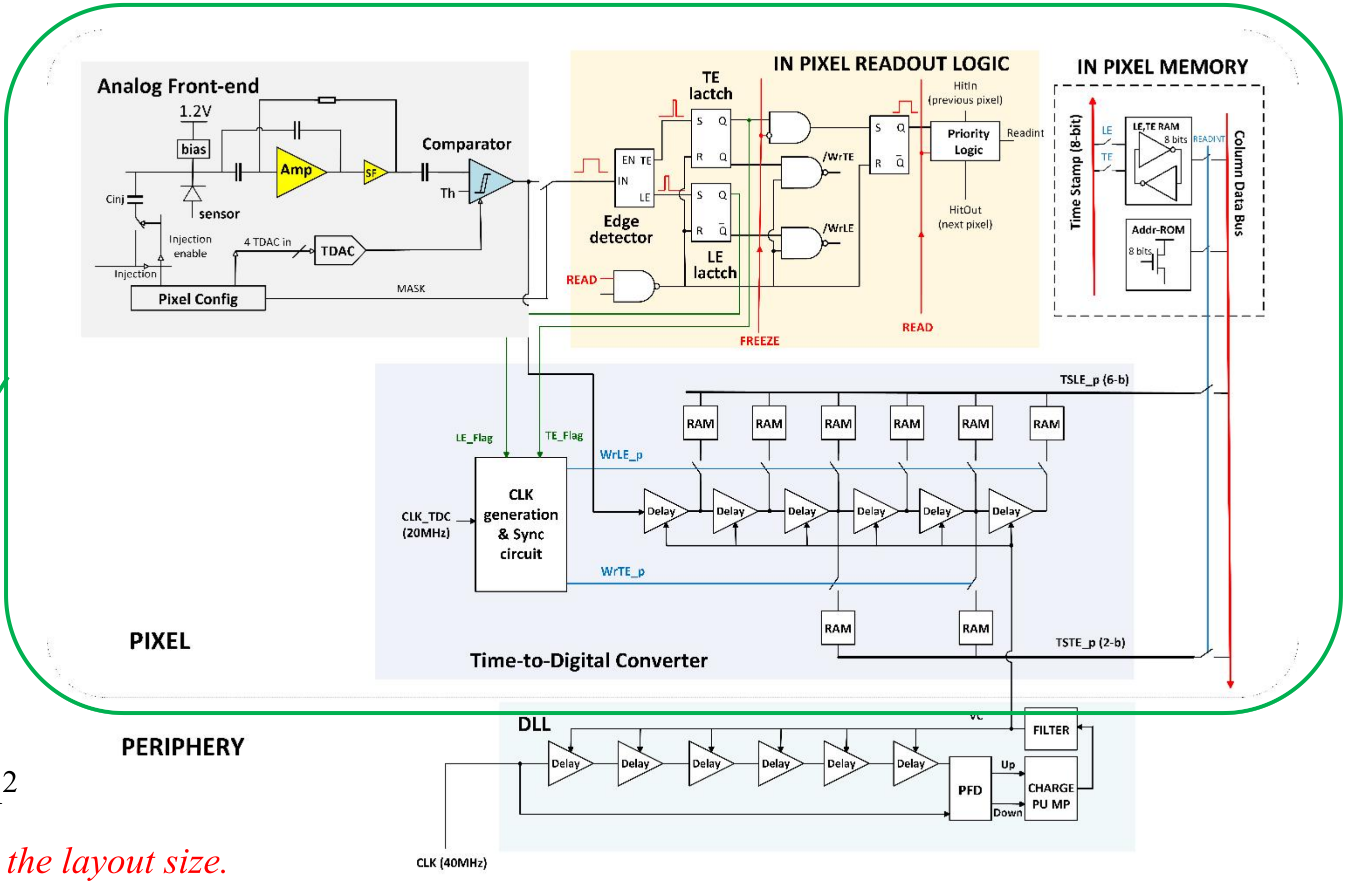
(c) Read out package(time stamp and address) to EoC in priority order

相比构架1，再更高的击中率场景下，时间信息也是准确的.



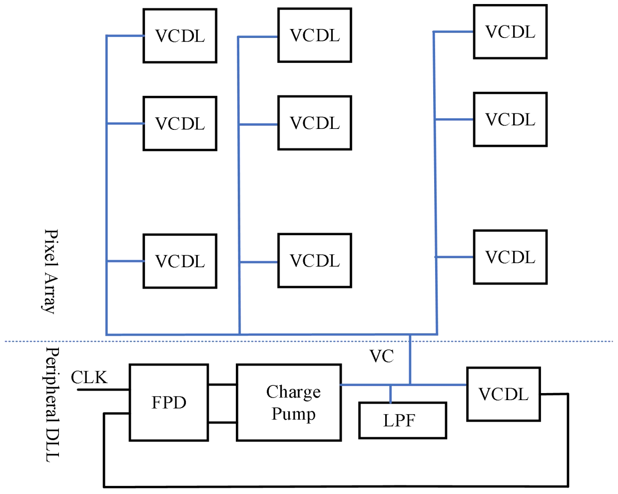
Layout of 2×3 pixels，signal pixel size is 40×145 μm²

The actual manufacturing size will be scaled down to 0.9 times the layout size.

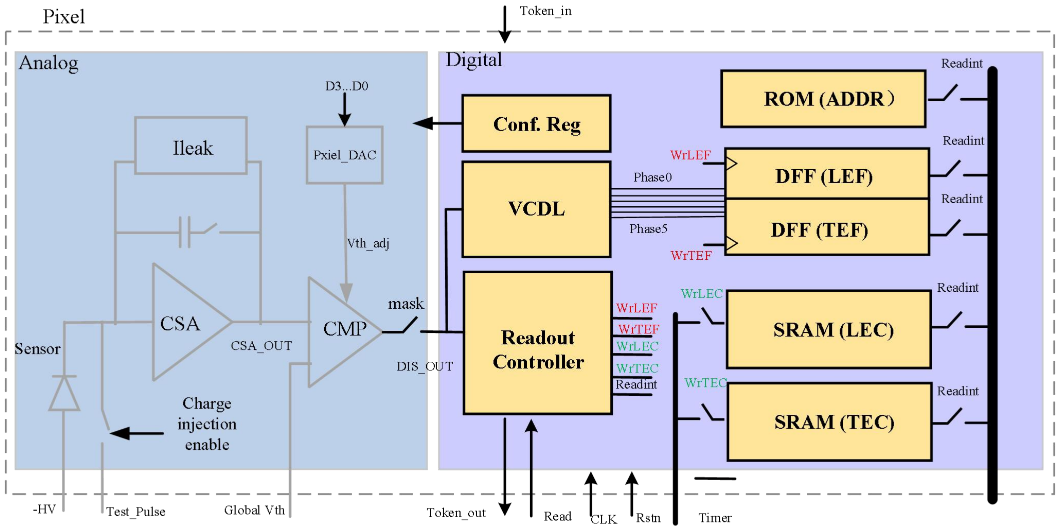


- **像素内更高的集成度：** 有限面积的单像素内集成了**模拟放大器、比较器、4-bit的像素内DAC，优先级读出逻辑，基于延迟链结构的粗-细时间戳TDC、时间和地址存储器、像素工作模式配置逻辑**等；

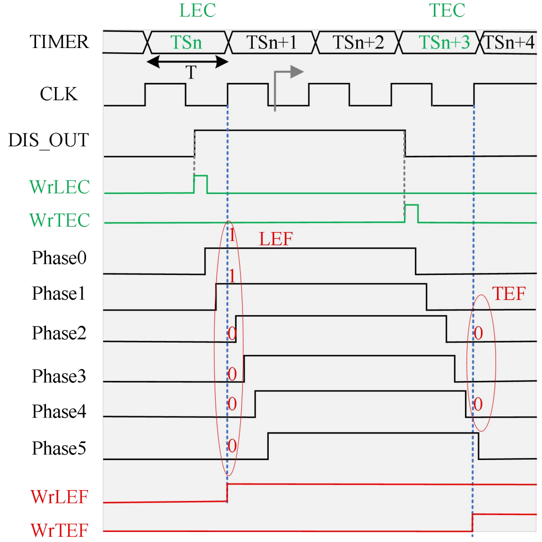
读出构架2的设计考虑：降低功耗



Peripheral DLL and duplicated in-pixel VCDL



The comparator output is used for VCDL



6 phases are used for Leading edge and 2 of them are used for tailing edge.

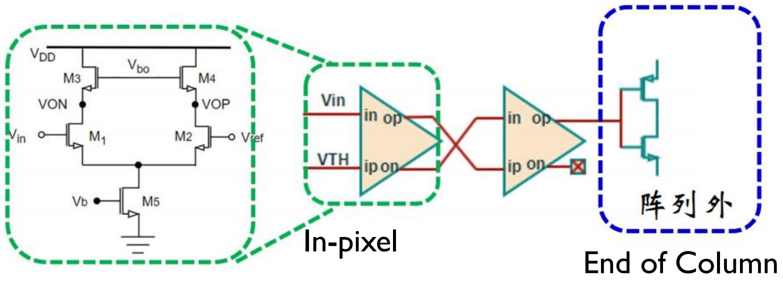
像素级TDC的低功耗设计考虑：

4.16ns fine timestamp for LE

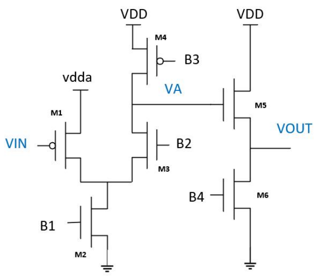
- ➢ 像素内仅包含一个小的VCDL结构，共用的DLL被放置在像素阵列外部；
- ➢ 只有被击中的像素里的TDC电路工作：几乎没有静态功耗；
- ➢ 仅20MHz的慢速时钟分发给阵列：在像素内转换成40Mhz的粗时间戳;
- ➢ 信号到达前沿（LE）和后延（TE）共享一条延迟链，ToT信息几乎没有额外的功耗支出；

像素内模拟前端设计考虑

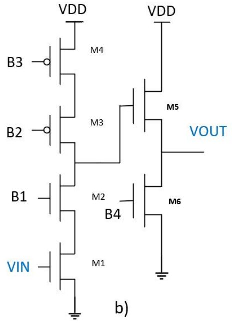
- CSA+NMOS comparator in Architecture1



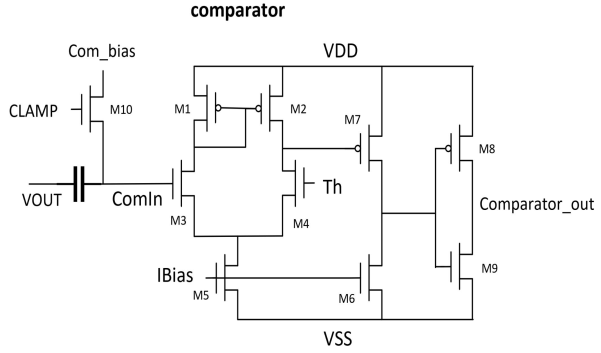
- CSA+CMOS comparator in Architecture 2



2). CSA2: fold-cascode + SF



1). CSA1: cascode + SF

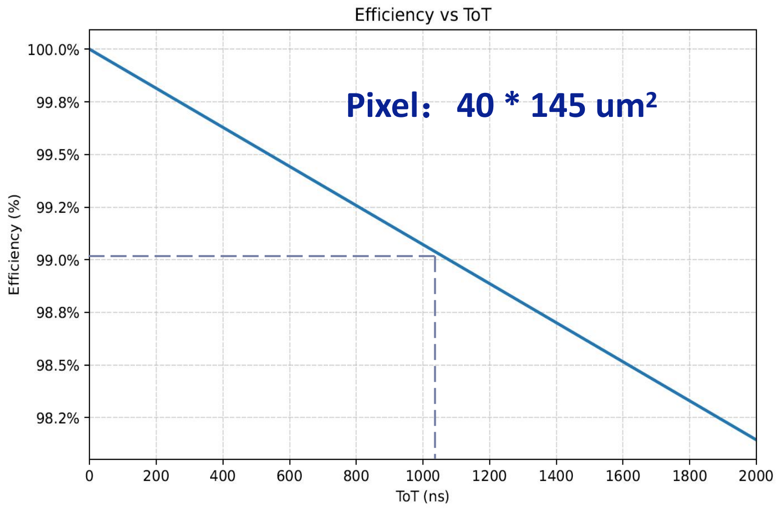


核心关注性能:

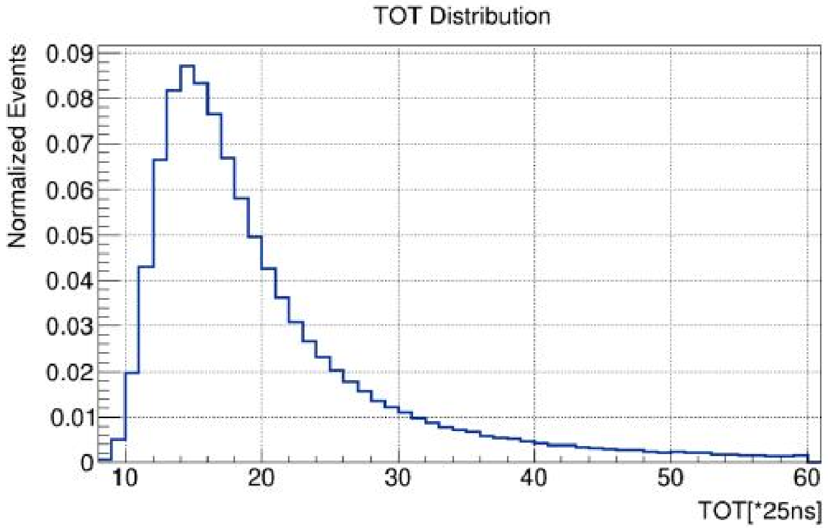
- **响应时间:** 不同信号量的时间游走效应，影响时间分辨;
- **功耗：** 整体功耗的主要来源;
- **TOT：** 模拟事例堆积、时间分辨补偿等;
- **噪声：** 影响时间分辨、探测效率、假击中率等;

像素内模拟前端设计考虑

- **过阈时间ToT（Time over Threshold）：**



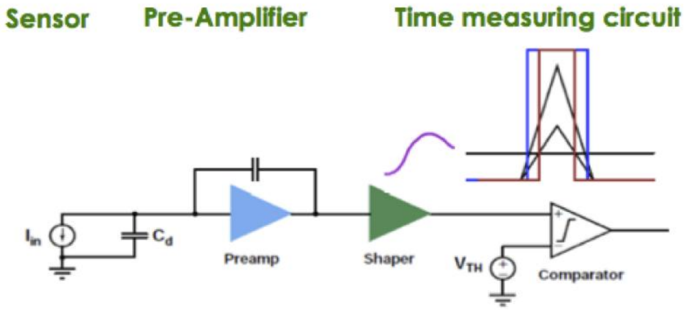
Efficiency vs ToT while the hit density @ 100 Mhz/cm²
(only analogue part)



Simulation results of ToT distribution of a MIP in HV-CMOS pixel sensor (2ke- --> 20ke-).

The maximum ToT (for MIP) is limited to ~1μs, ensuring far less than 1% efficiency loss due to analogue pile-up while the hit density reaches 100Mhz/cm².

时间分辨预算分配



Typical time measurement detector structure.

$$\sigma_{\mathrm{t}}^2 = \sigma_{\mathrm{TW}}^2 + \sigma_{\mathrm{J}}^2 + \sigma_{\mathrm{TDC}}^2 \cdot$$

（TOT compensation not included）

Signal charge distribution、analog front-end design、comparator threshold setting, etc.

Electronics noise、threshold inconsistency from pixel to pixel, etc.

TDC quantization noise：
Time stamp bin size/√12

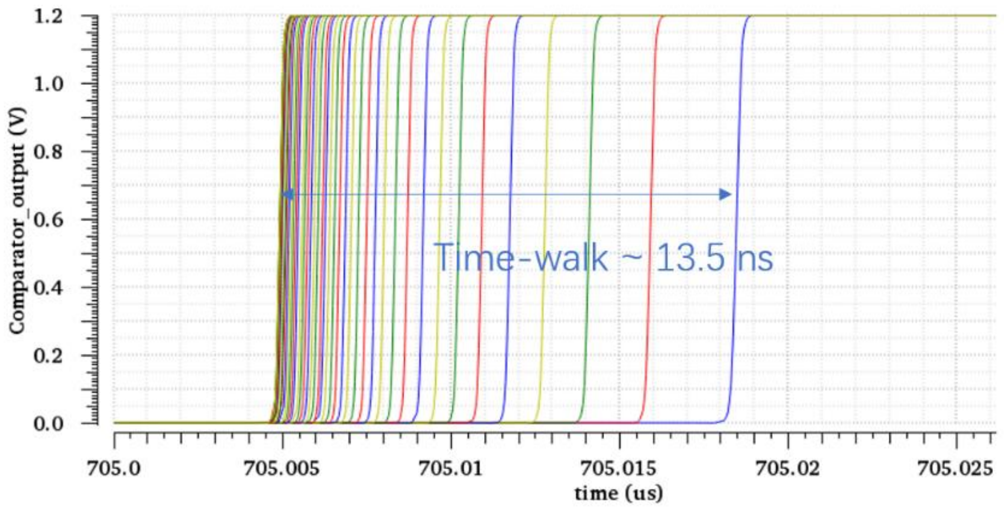
$(4\ \mathrm{ns})^2$ $\quad < (2\ \mathrm{ns})^2$ $\quad < (2\ \mathrm{ns})^2$

Time resolution < 5 ns

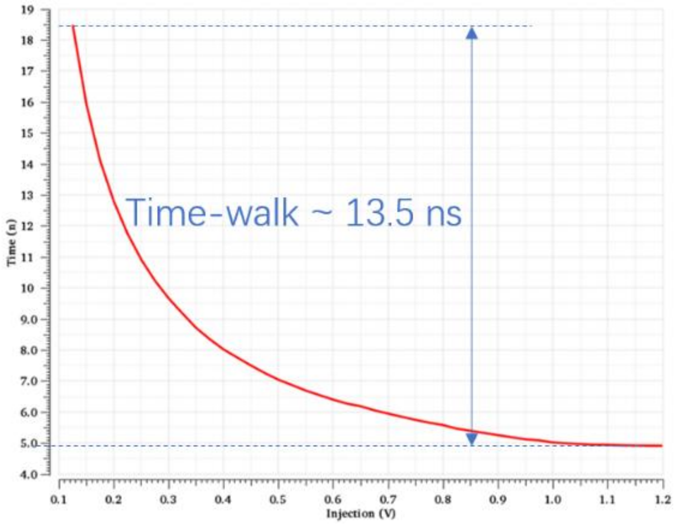
The current analysis does not incorporate TOT compensation, clock delay (~1ns, compensable), or clock jitter (ps-level) effects. **The final performance highly depends on the final process condition we could access.**

像素内模拟前端

- ◆ **The time-walk:** simulations for MIP in fully depleted 200 μm thick sensor.



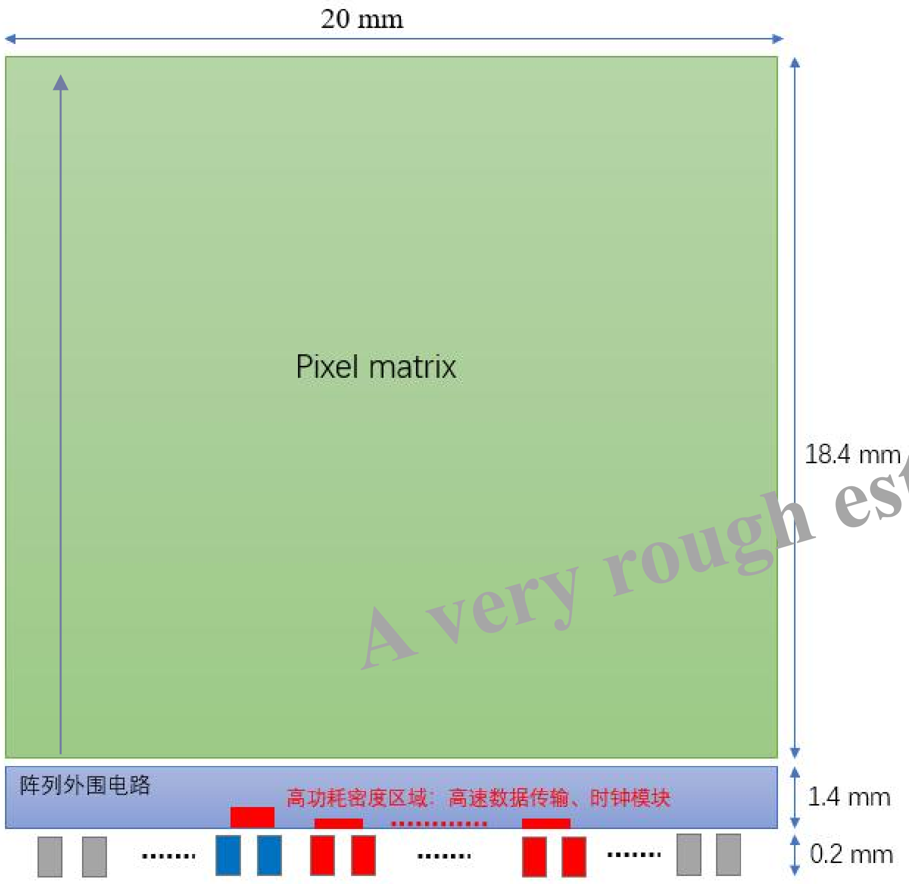
Time walk: 13.5 ns



Time of Arrive: 5 ns - > 20 ns

- ◆ **Power:** ~ 10 μW/pixel for in pixel CSA + Comparator
- ◆ **Noise:** 与传感器电容高度相关（基于商用标准工艺的结果见测试部分）

最终芯片功耗和面积预估（仿真值）



Estimated layout of a full size HV-CMOS sensor.

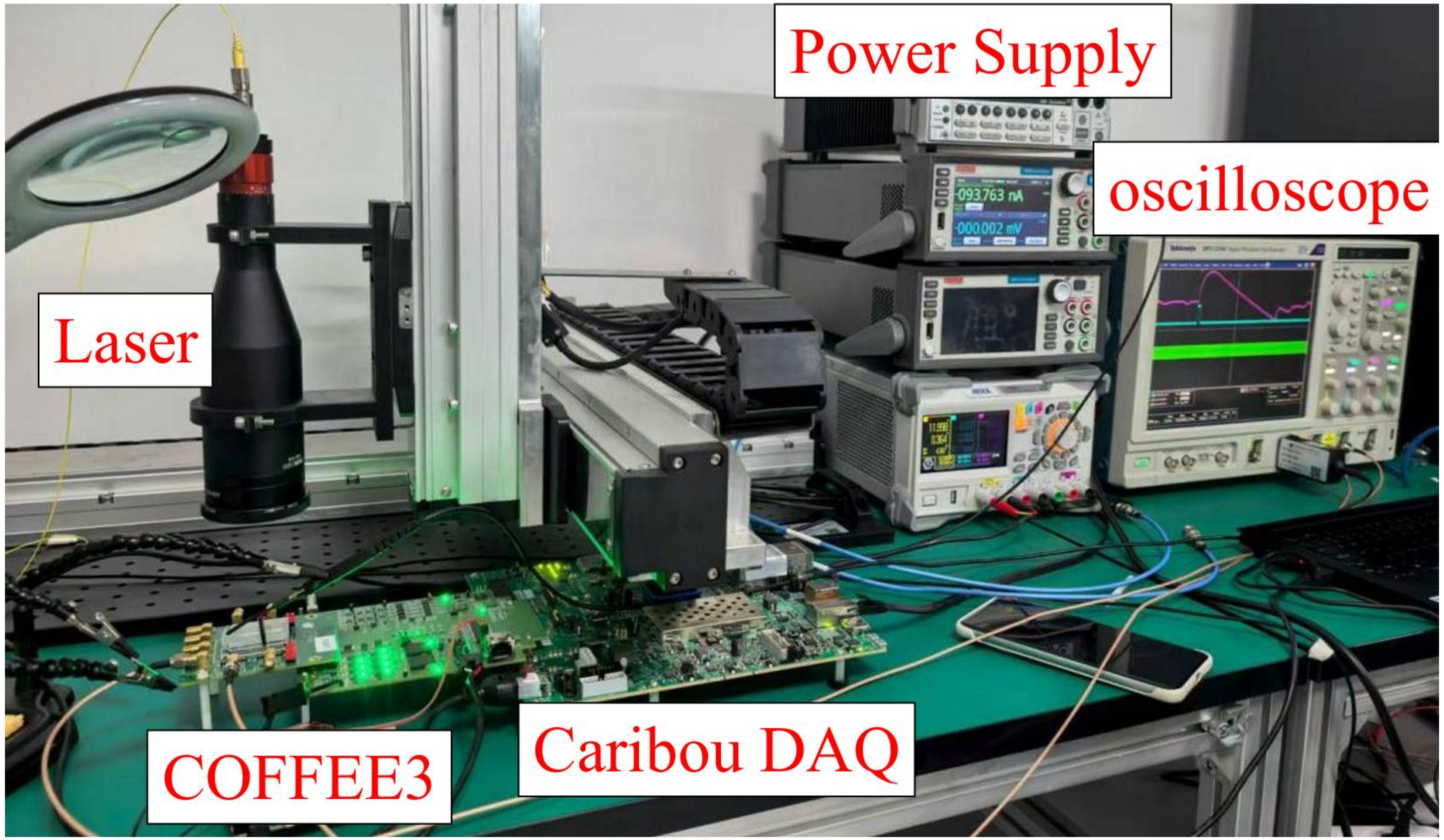
A very rough estimation

Estimated overall power consumption and area (based on architecture 2)

--- on the expectation of using high-resistivity wafers in the future.

	Pixel matrix	**Peripheral**	**Overall**
Area	20 × 18.4 mm^2	20 × 1.6 mm^2	20 × 20 mm^2
Total power consumption	~580 mW	~ 22 mW (may overly optimistic)	~ 602 mW
Power density	**~158 mW/cm^2**	**~123 mW/cm^2**（estimate one data Transmitter channel）	**~ 150 mW/cm^2**（hit density related dynamic power not included yet）

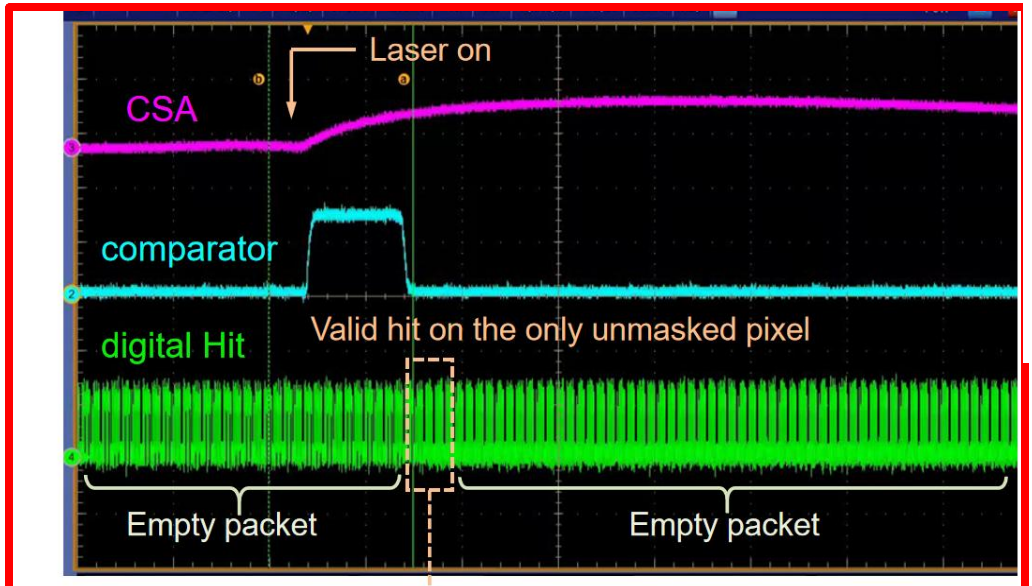
COFFEE3 初步测试结果



完整读出构架的激光信号响应

Architecture 2: in-pixel TDC

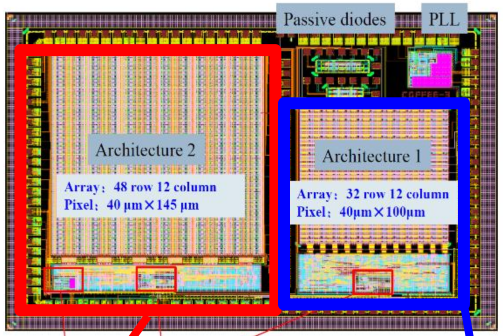
Architecture 1: in-pixel NMOS design



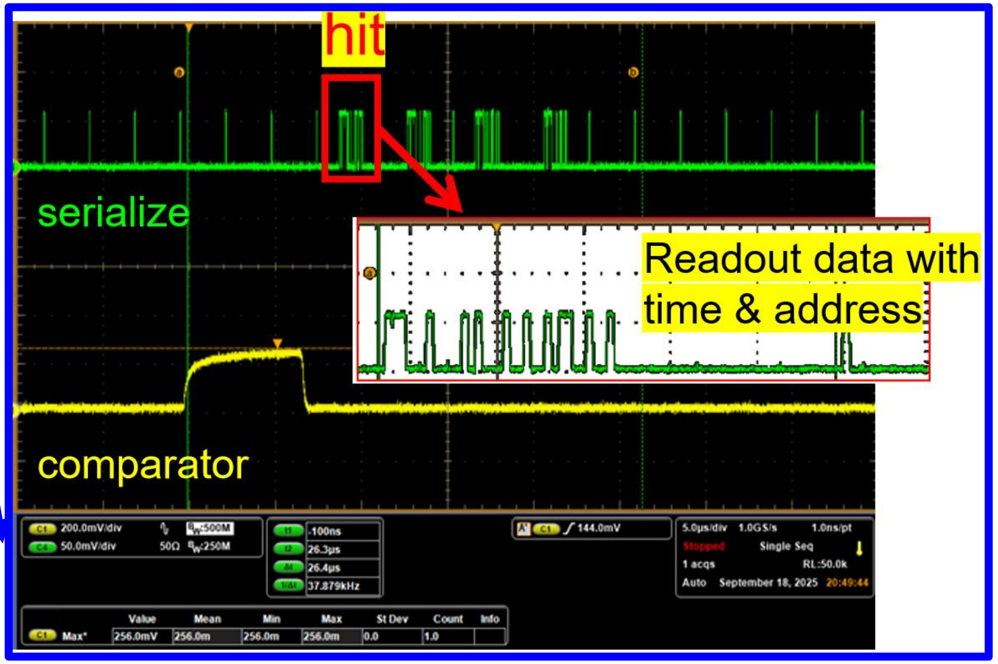
4 bit	4 bit	8 bit	8 bit	6 bit	2 bit	7 bit	3 bit
header	CHIP_TS	LE_coarse	TE_coarse	LE_fine	TE_fine	Addr_Row	Add_Col
0 1 1 0	0 1 0 1	0 0 0 1 0 1 1 0	0 1 1 0 1 0 1 1	1 1 0 0 0 0	0 0	0 0 0 0 0 0 1	0 0 0

A valid transmission packet corresponding to a hit

Correct row & column address



Layout of COFFEE3



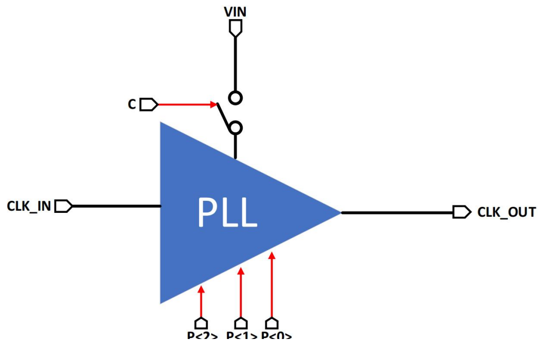
The full readout chain works for both of the two readout architectures.

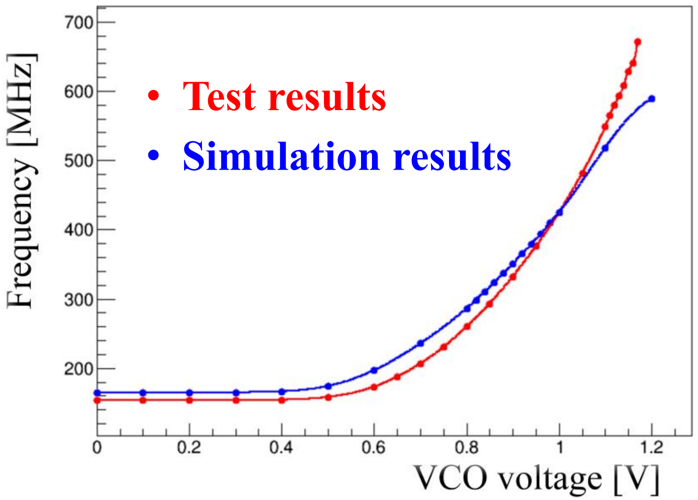
Sensing diode → in-pixel (CSA\comparator\TDC) → EOC (digital peripheral) -> data link-> DAQ

初步测试结果：阵列外围模拟模块

All the functional modules designed in COFFEE3 work:

- PLL works ups to 640Mhz
- LVDS driver/receiver works at 640 Mhz support 1.28 Gbps data link
- Delay line for in-pixel TDC works as expected





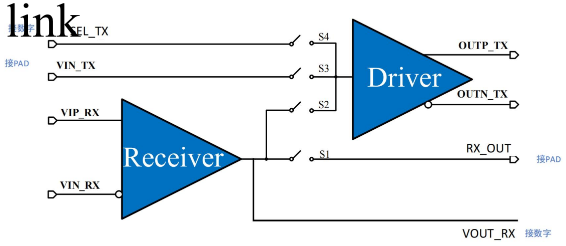
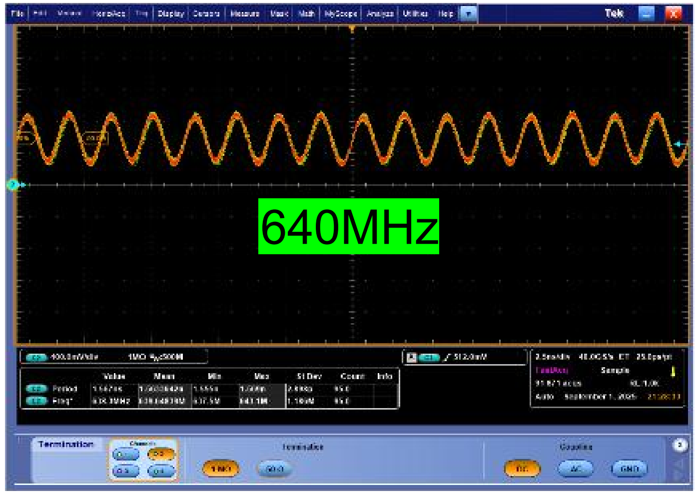
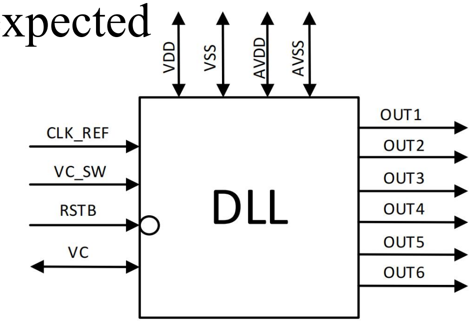
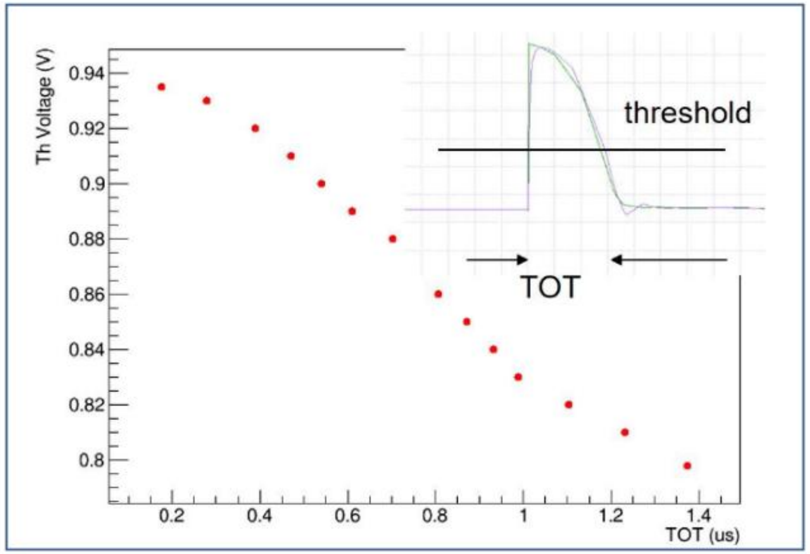


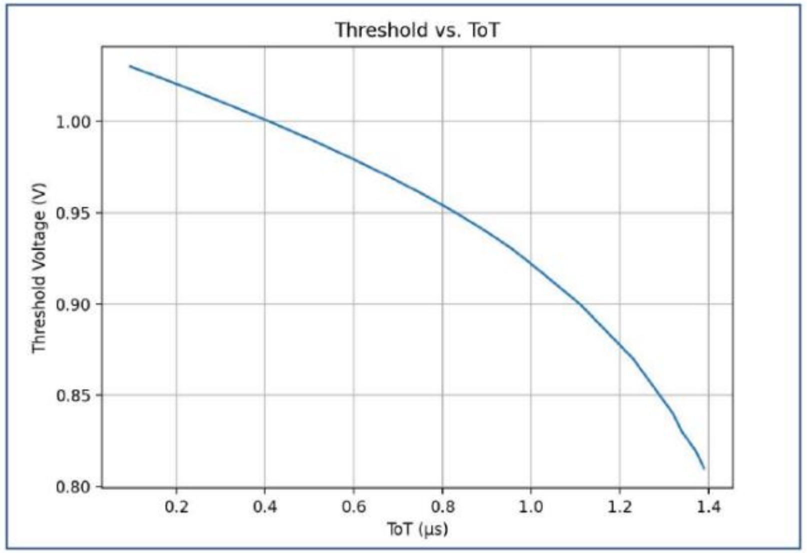
Fig 3.1.1 LVDS block diagram



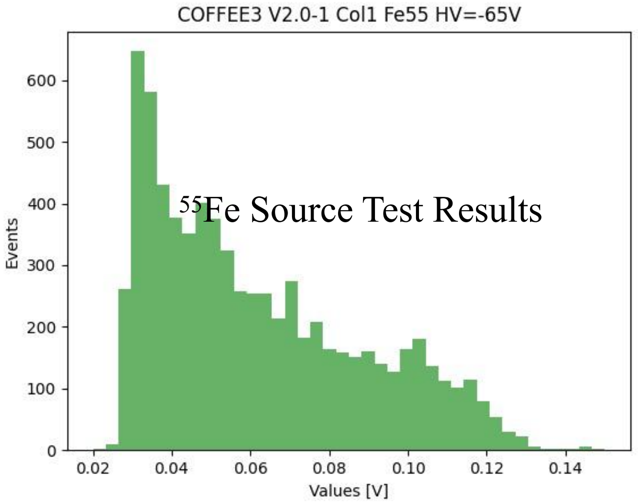


初步测试结果：像素内模拟前端





Measured TOT-threshold relationship matches simulation results.



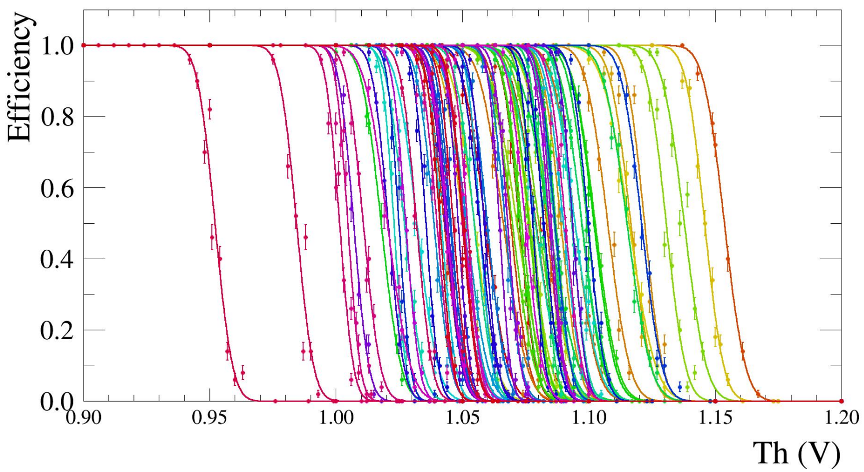
^{55}Fe Source Test Results

No significant calibration peak (1640e^{-} for 5.9 keV X-ray) is observed.

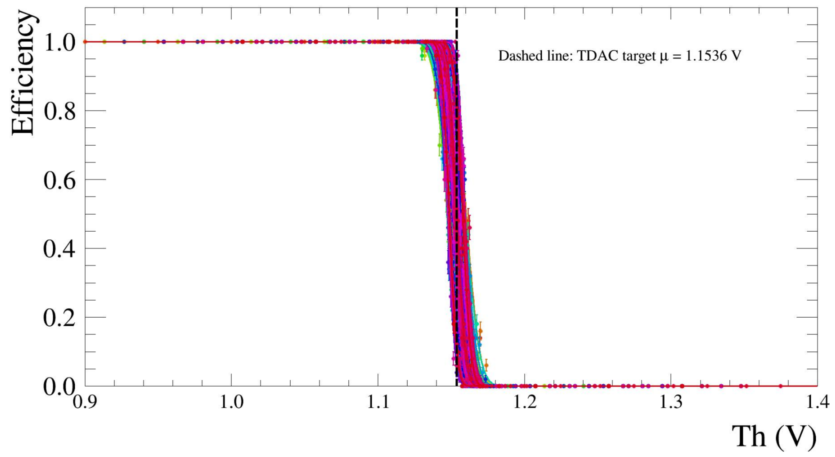
初步测试结果：噪声

S-curve results of the In-pixel TDC version: Each pixel integrates a 4-bit DAC for threshold tunning

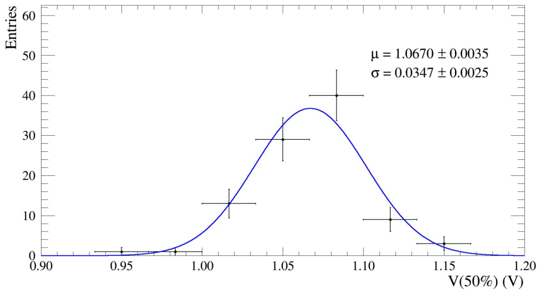
Before threshold tunning



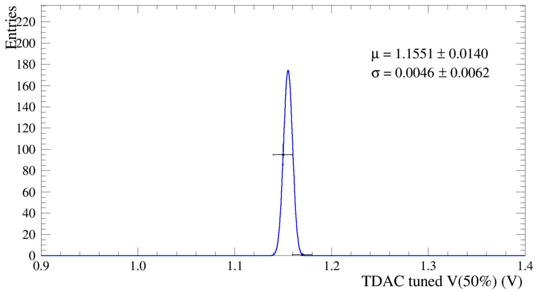
After threshold tunning



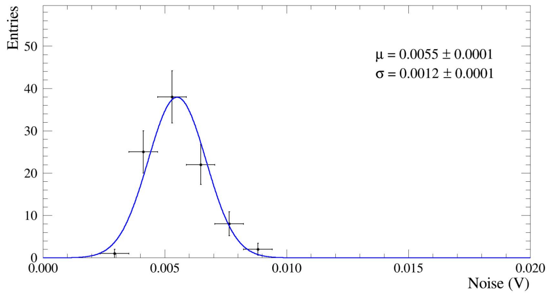
Threshold Variation Noise: 34.7mV



Threshold Variation Noise: 4.6 mV

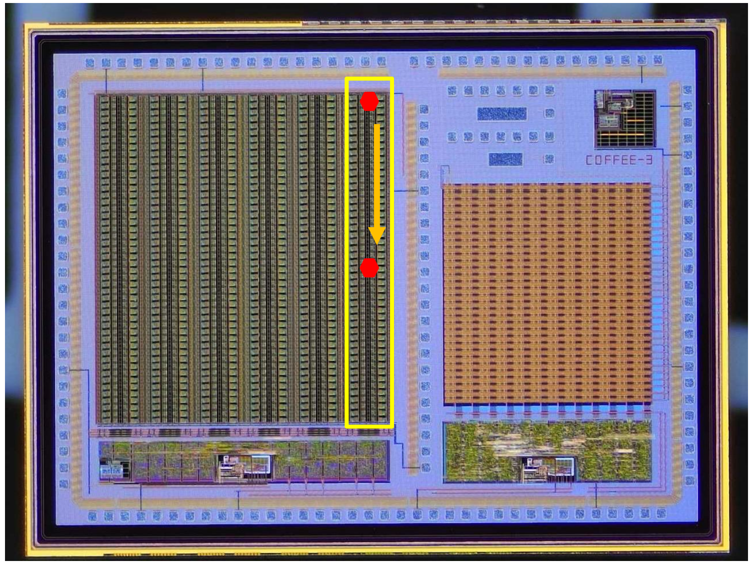


Temporal Noise:5.5 mV



If we take 0.1V as the calibration peak of ^{55}Fe, noise after tunning **would be ~ 120 e$^-$** (results are just obtained, very preliminary and need further confirmation.)

初步测试结果：激光信号响应

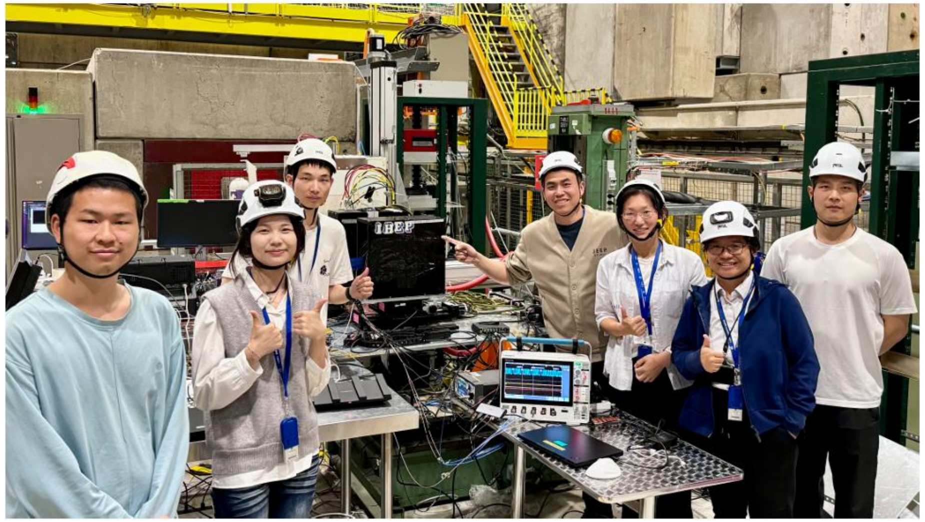


Laser response test of pixel array:

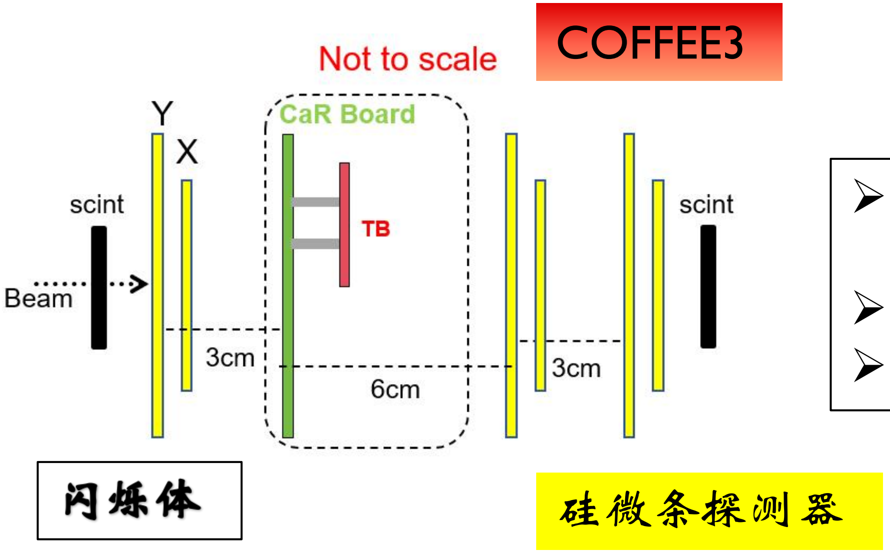
1000 laser injections per position with a 200 μm moving step, covering an equivalent pixel interval of ~5 pixels (180 μm, pixel size = 36 μm).

2column×48 rows pixel

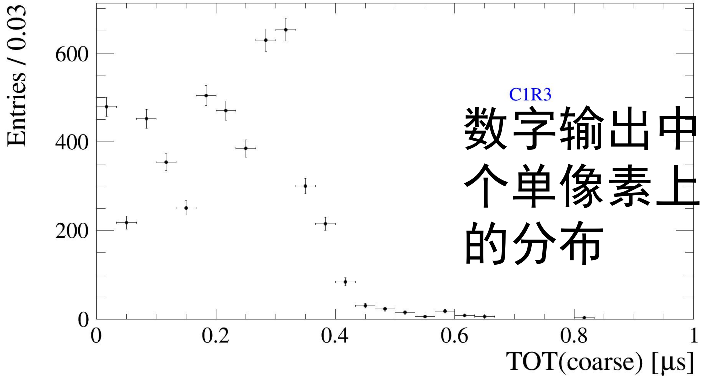
初步测试结果：束流实验



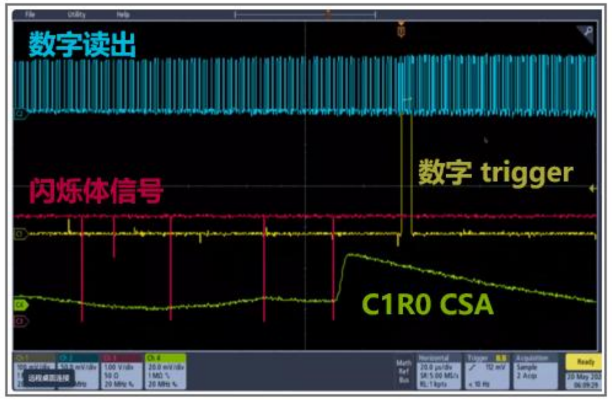
Setup on 19th May COFFEE placed between Si strip layers @ H6/PP156 @ SPS.



- ➢ COFFEE3在首次束流实验中观测到了MIP信号；
- ➢ 进一步的分析正在进行中；
- ➢ 为下一次束流实验积累了经验；



数字输出中记录到的一个单像素上击中的TOT的分布

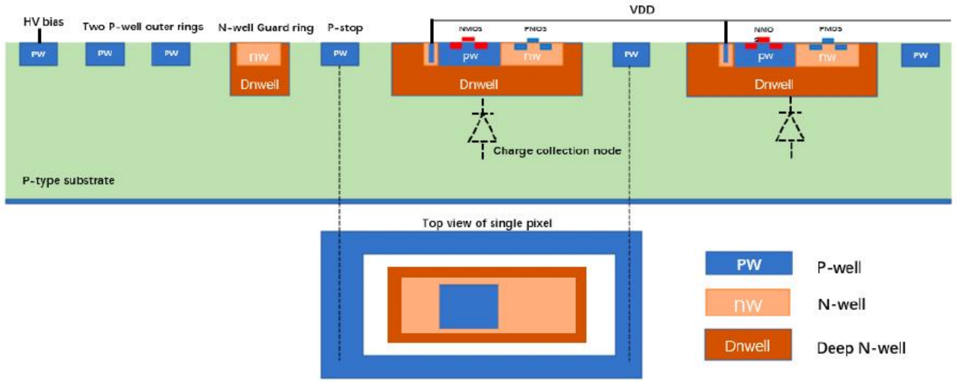


示波器中记录到的MIP击中在COFFEE3芯片上产生的模拟波形（绿色）、数字信号（蓝色）

CEPC Silicon Inner Tracker meeting (May 26, 2026) · Indico of IHEP (Indico) by Yimingt

The preliminary test results are positive

However, standard commercial 55nm HV-CMOS process is by no means the ideal MAPS process



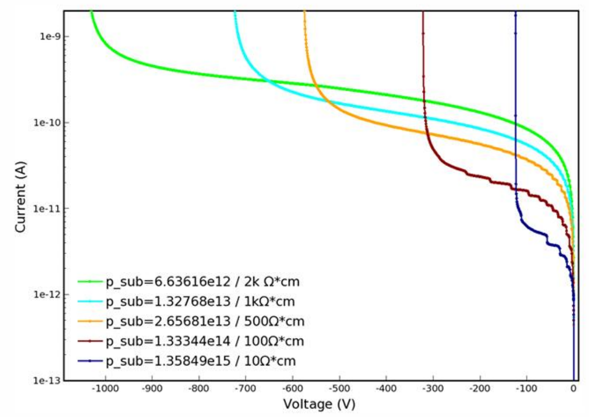
1. Triple-well process → cross-talk risks between sensor (deep-n) and PMOS transistors； → **Restrict the flexibility of in-pixel design;**
2. Break down at ~-70V; → **Extremely limits the SNR.**
3. No access of high-resistivity wafers;

In collaboration with the Foundry, some process modifications have just been made

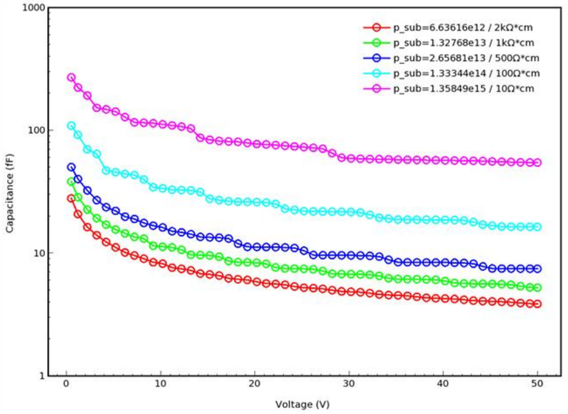
for better sensor performances

工艺修改目标：显著提升信噪比

Modifications：

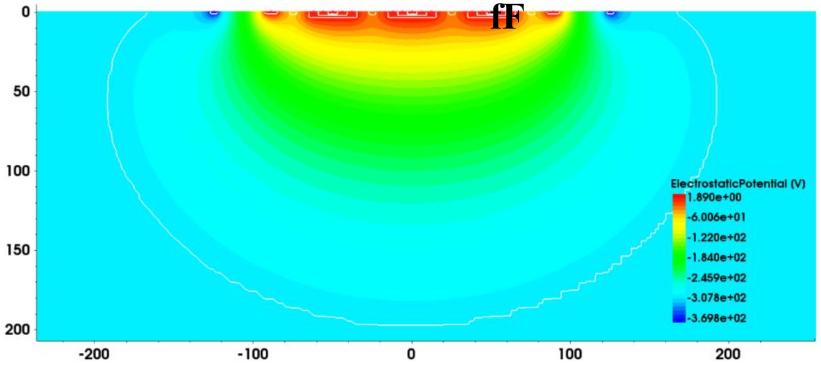


- Breakdown V: **70 --> > 400V**



- Capacitance of VDNW/p-sub: **~ hundreds fF --> ~ tens of fF**

- ◆ Add layers: Deep-PW & Very-deep-NW;
- ◆ Change doping rules affecting breakdown voltage;
- ◆ Replace wafer: from 10 Ω·cm --> >1k/2k/4k Ω·cm;



- Depletion depth: ~10 μm → >200 μm

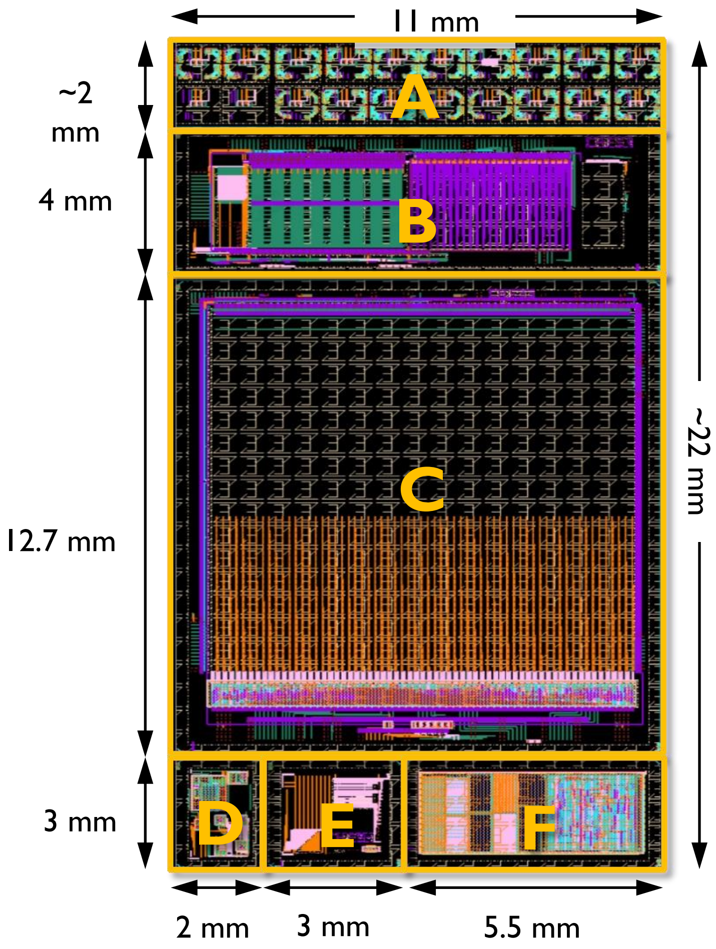
Huge S/N gain : Signal increase >10 times, while C_{diode} reduce

基于修改工艺的首次流片: CHiR 1.0

*CHiR (COFFEE-HiRes)

20倍的COFFEE3面积，包含6个主要的区域，以实现不同的验证目标：

- **Guard rings & Passive sensor design validation:**
  - **(A)** 20 arrays of 3x4 passive pixels with diff guard ring designs, each can be diced into individual 1x1 mm^2 chip;
- **In-pixel FE and Active pixel matrix design validation:**
  - **(B)** 9 variations of in-pixel FE designs & 12 variations of pixel sizes;
  - **(C)** A 256 × 64 pixel matrix (pixel size 38 μm x 150 μm) with digital periphery;
- **Analogue IP & Digital modules and transistors validations**
  - **(D)** necessary analog IPs: PLL, DAC, LVDS, SLDO …
  - **(E)** alternative small pixel arrays and SLDO versions
  - **(F)** digital modules and transistors for TID and SEE studies



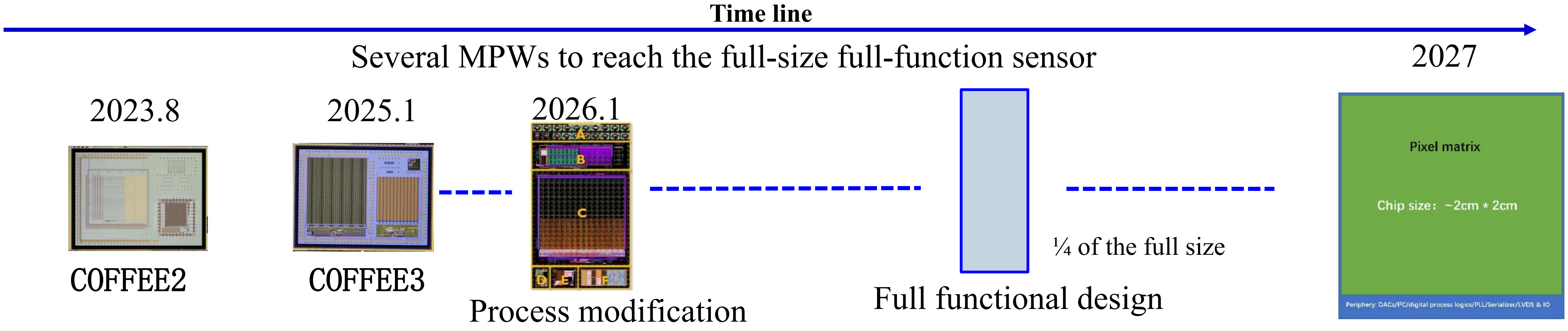
Layout of CHiR1.0, submitted Jan. 24, 2026

第一批芯片预计本月初返回

Answers to many key questions can be expected!

总结和展望

- 我们已基于商用 55 nm HV-CMOS 标准工艺完成 COFFEE2/3 芯片的设计；初步测试结果实现了设计目标，更多性能测试工作正在开展中;
- 基于修改工艺完成的首款芯片CHiR 1.0已完成设计和流片提交；诸多核心关键问题有望得到解答。若进展顺利，后续设计优化工作将依托该修改工艺落地实施。
- 我们期望可以在 2027 年底完成全尺寸、全功能芯片的设计。



Time line

Several MPWs to reach the full-size full-function sensor

2023.8

COFFEE2

2025.1

COFFEE3

2026.1

Process modification

¼ of the full size

Full functional design

2027

Pixel matrix

Chip size: ~2cm * 2cm

Periphery: DACs/I²C/digital process logics/PLL/Serializer/LVDS & IO

Target: Time resolution ~ ns; Spatial resolution ~10 μm; Power dissipation < 200mW/cm^2 ;

致谢

本项研究工作的研发团队: Random ranking

Leyi Li, Xiaoxu ZHANG, XiaoMin WEI, Weiguo LU, Pengxu LI, Mei ZHAO, Yang ZHOU, Bingchen Yan, Anqi WANG, Yuanhong JIAO, Yang CHEN， Yujie WANG, Huimin Wu, Zexuan ZHAO, Yu ZHAO, Zheng Wei, Jianpeng DENG, Zhan SHI, Kunyu XIE, Xinhao XIE, Xiaolong WANG, Ziying ZHANG, He HUANG, Junyuan YAN, Shenyao TANG, Ruoshi DONG, Yang CHEN, Xuekang LI， Xinyang GUO, Zhuojun CHEN, Zhiyu XIANG, Zijun XU, Zeng CHENG, Kang LIU, Qinze Li， Yisheng Fu， Tianyu Shi， Menke CAI, Boxing WANG, Yuman CAI, Hui ZHANG, Mingjie FENG, Lei ZHANG, Meng WANG, Hongbo ZHU, Yiming Li, Jianchun WANG ……..

& **Independent KIT design in COFFEE2**: Hui ZHANG, Ruoshi DONG, Ivan PERIC；

Thanks for your attention!