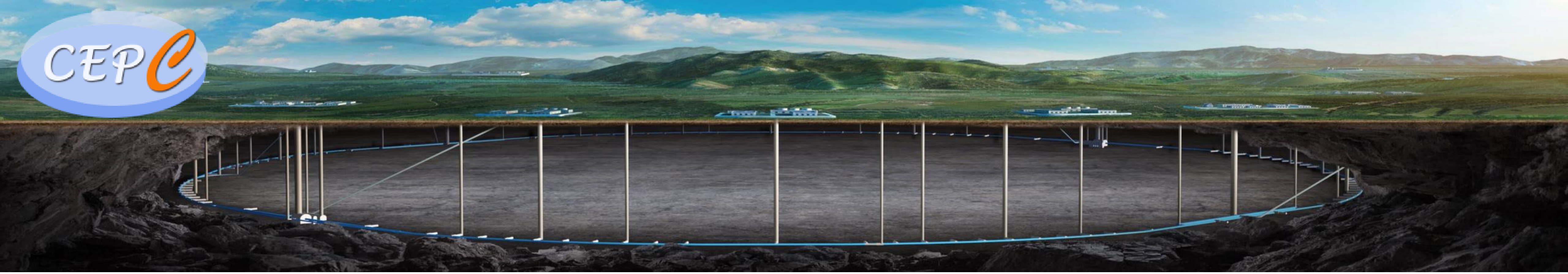


CEPC Vertex Detector & TaichuPix Development

Wei Wei

(On behalf of the CEPC Vertex Detector group)

中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences

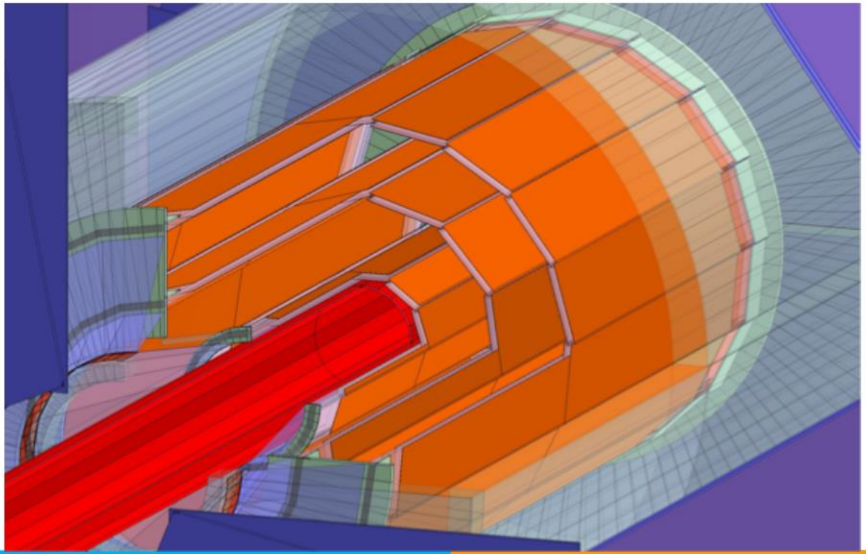
July. 1st, 2026, STCF Workshop, Xi’an

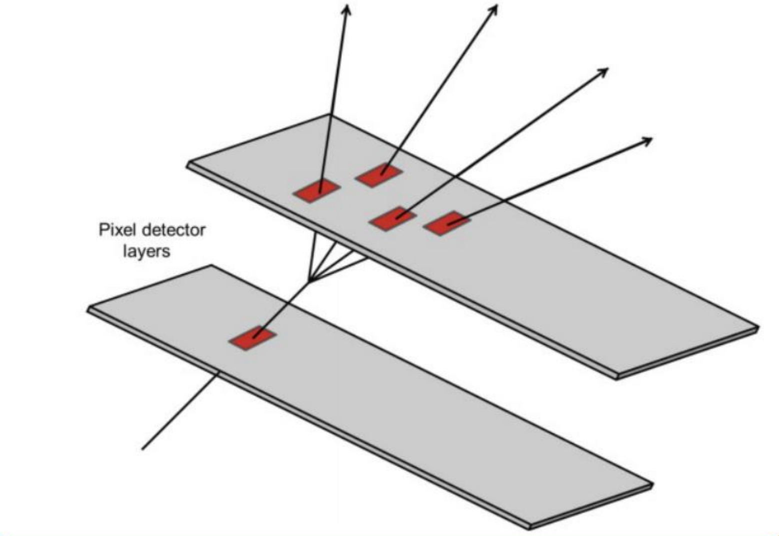
Content

- CEPC requirement for Vertex Detector
- R&D on Taichupix Development
- Baseline scheme on curved MAPS
- Future consideration

Introduction: vertex detector

- Vertex detector optimized for first 10 year of CEPC operation (ZH, low lumi-Z runs)
  - Low lumi Z runs is ~20% instant luminosity of high lumi Z runs
- Motivation:
  - Aim for impact parameter resolution and vertexing capability
  - For H → bb/ H → cc/ H → light quark or gluons analysis
  - The observation H → cc or H → gg is important goal for CEPC





Vertex Requirement

- Inner most layer (b-layer) need to be as close to beam pipe as possible
  - **Challenges:** b-layer radius (11mm) is smaller compared with ALICE ITS3 (18mm)

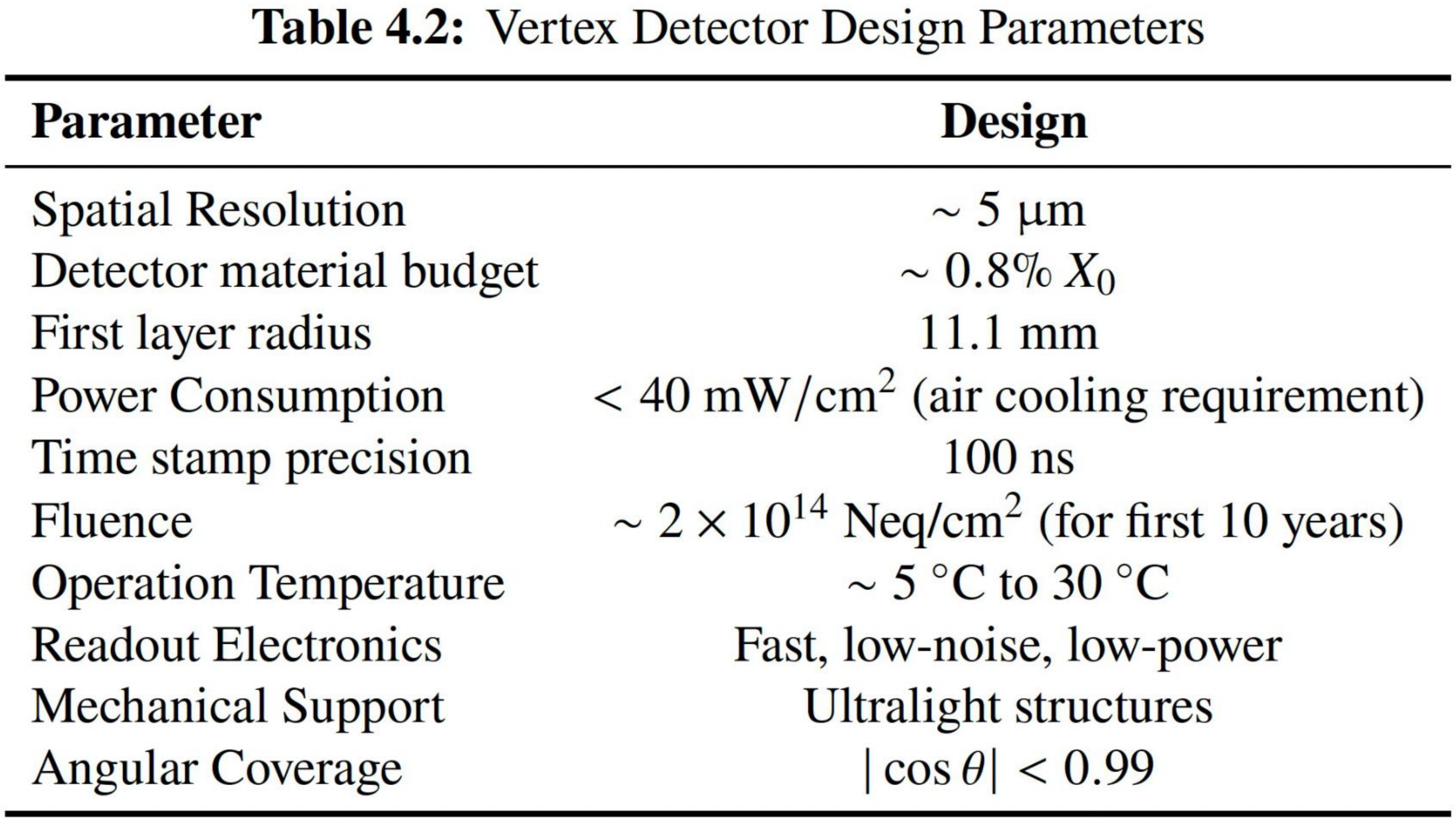


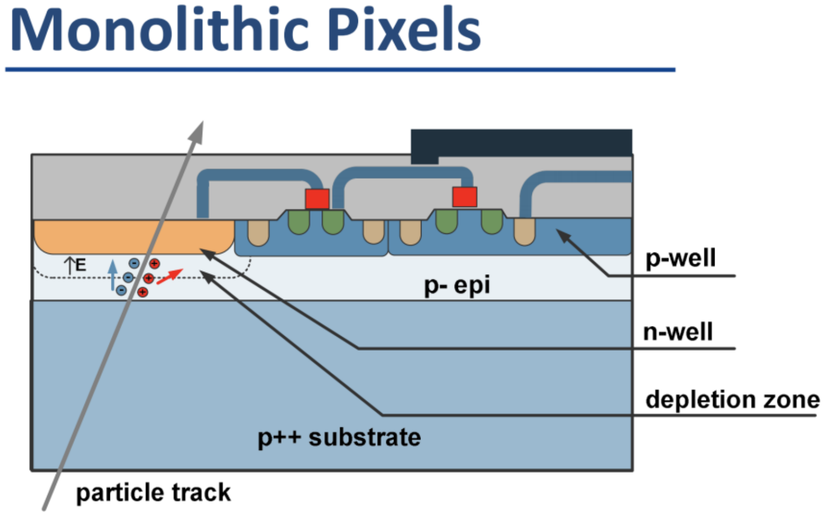
Table 4.2: Vertex Detector Design Parameters

Parameter	**Design**
Spatial Resolution	$\sim 5\ \mu\mathrm{m}$
Detector material budget	$\sim 0.8\%\ X_0$
First layer radius	11.1 mm
Power Consumption	$< 40\ \mathrm{mW/cm}^2$ (air cooling requirement)
Time stamp precision	100 ns
Fluence	$\sim 2 \times 10^{14}\ \mathrm{Neq/cm}^2$ (for first 10 years)
Operation Temperature	$\sim 5\ ^\circ\mathrm{C}$ to $30\ ^\circ\mathrm{C}$
Readout Electronics	Fast, low-noise, low-power
Mechanical Support	Ultralight structures
Angular Coverage	$\lvert\cos\theta\rvert < 0.99$

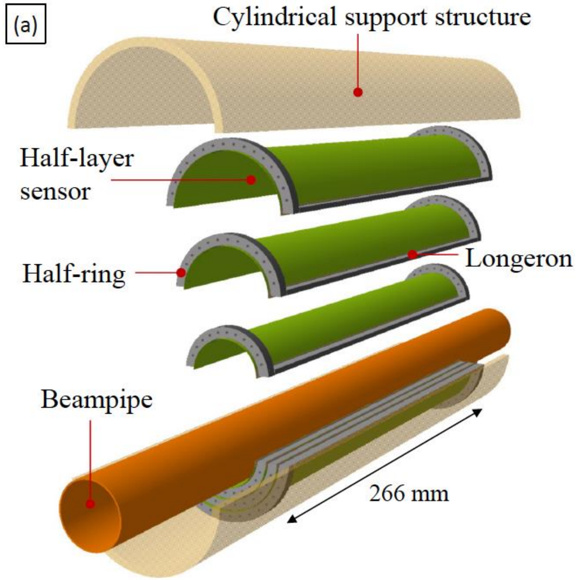
Technology survey and our choices

- Curved MAPS chosen as baseline for Reference detector TDR. arXiv:2510.05260
  - Baseline: based on curved CMOS MAPS (Inspired by ALICE ITS3 design[1])
    - Advantage: 2~3 times smaller material budget compared to alternative (ladder)
  - Alternative: Ladder design based on CMOS MAPS

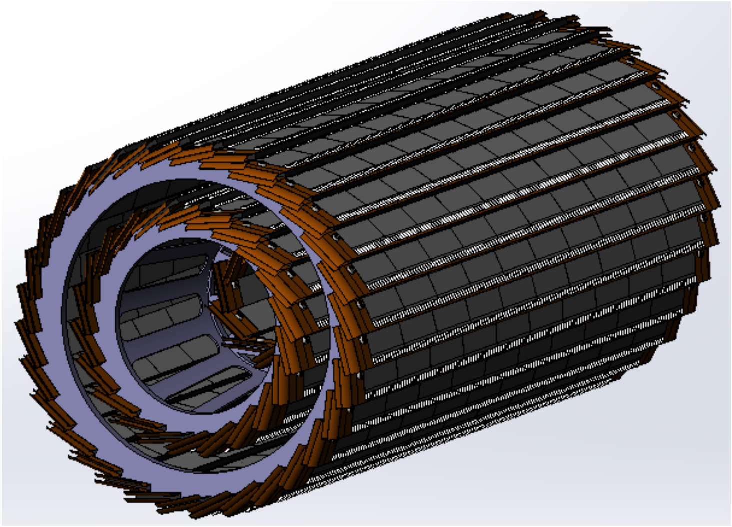
Monolithic active Pixel CMOS (MAPS)



Baseline: curved MAPS

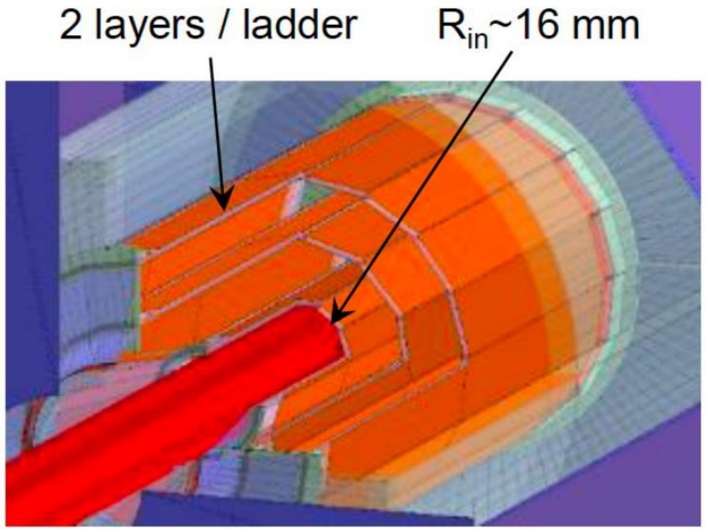


Alternative: ladder based MAPS



[1] ALICE ITS3 TDR: https://cds.cern.ch/record/2890181

Silicon Pixel Chips for Vertex Detector



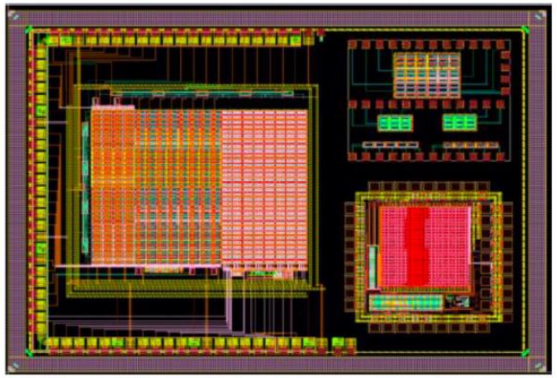
Goal: σ(IP) ~ 5 μm for high P track

CDR design specifications

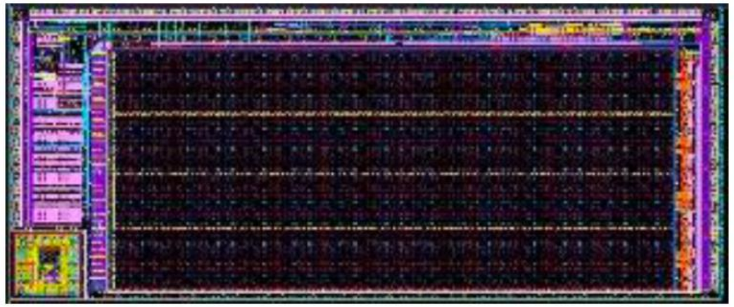
- **Single point resolution ~ 3μm**
- **Low material (0.15% X_0 / layer)**
- **Low power (< 50 mW/cm^2)**
- **Radiation hard (1 Mrad/year)**

Silicon pixel sensor develops in 5 series:
JadePix, TaichuPix, CPV, Arcadia, COFFEE

Develop **COFFEE** for a CEPC tracker using SMIC 55nm HV-CMOS process



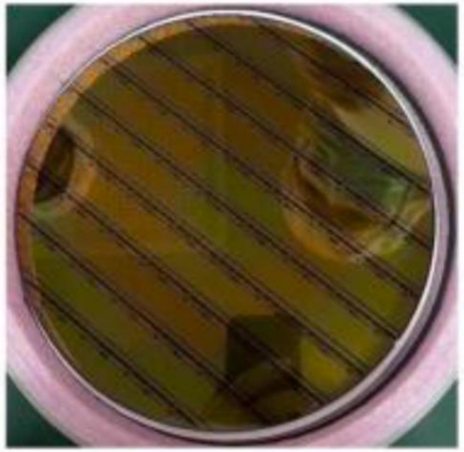
JadePix-3 Pixel size ~16×23 μm^2



Tower-Jazz 180nm CiS process
Resolution 5 microns, 53mW/cm^2

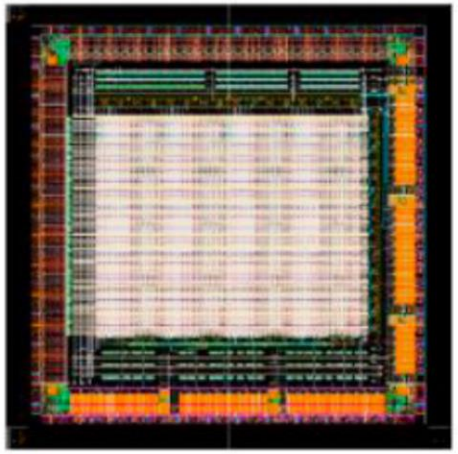
MOST 1

TaichuPix-3, FS 2.5x1.5 cm^2
25×25 μm^2 pixel size



MOST 2

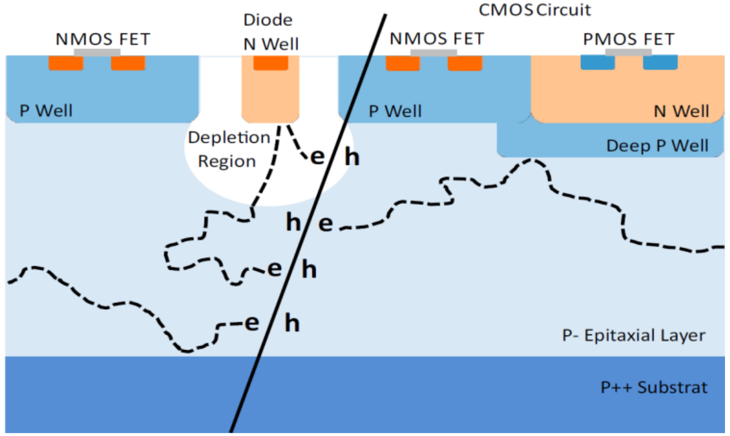
CPV4 (SOI-3D), 64×64 array
~21×17 μm^2 pixel size



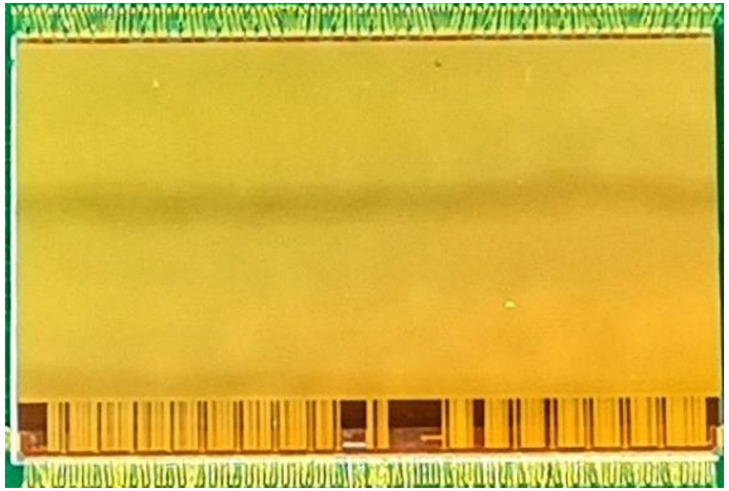
Arcadia by Italian groups
for IDEA vertex detector
LFoundry 110 nm CMOS

TaichuPix prototypes overview

- Motivation: a large-size & full functionality pixel sensor for the first 6-layer vertex detector prototype
- Major challenges for design
  - Small pixel size → high resolution (3-5 µm)
  - High readout speed (dead time < 500 ns @ 40 MHz) → for CEPC Z pole
  - Radiation tolerance (per year): 1 Mrad TID
- Completed 3 rounds of sensor prototyping in a 180 nm CMOS process
  - Two MPW chips (5 mm × 5 mm)
    - TaichuPix-1: 2019; TaichuPix-2: 2020 → feasibility and functionality verification
  - 1st engineering run
    - Full-scale chip: TaichuPix-3, received in July 2022 & March 2023
- Design team： IHEP, NPU, CCNU, SDU, IFEA, NJU



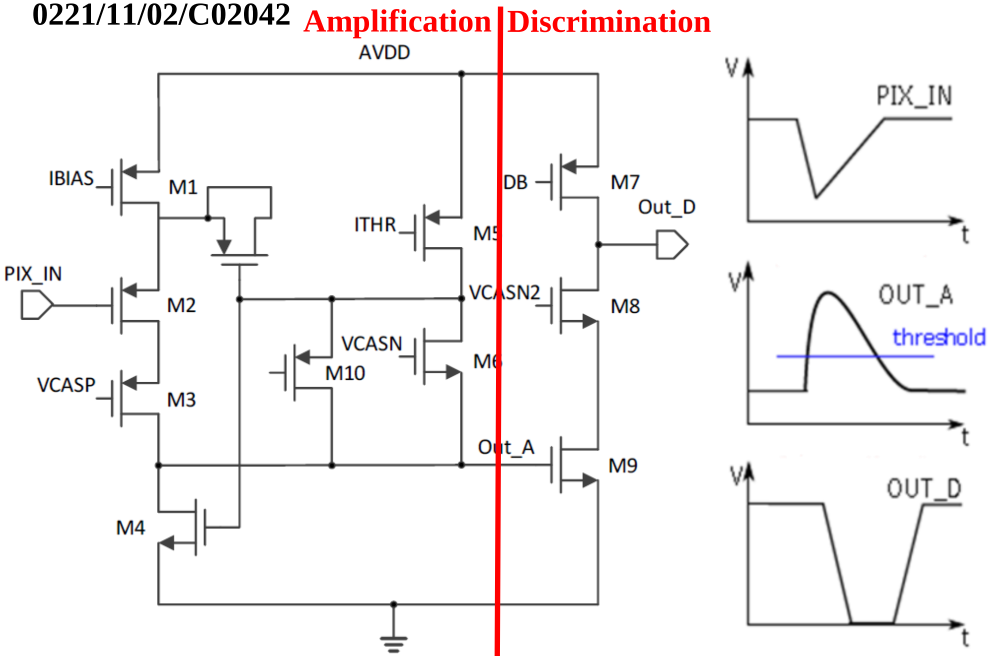
CMOS monolithic pixel sensor

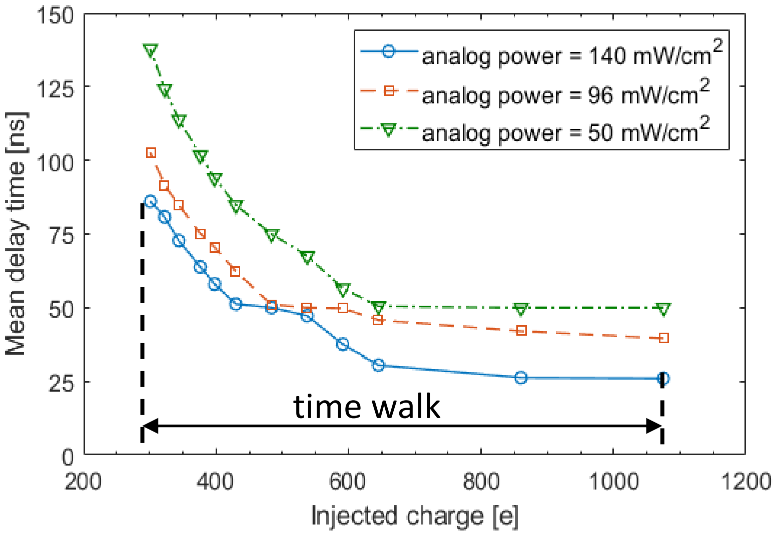


TaichuPix-3
(15.9 × 25.7 mm^2)

Pixel architecture – Analog

D. Kim et al. DOI 10.1088/1748-0221/11/02/C02042

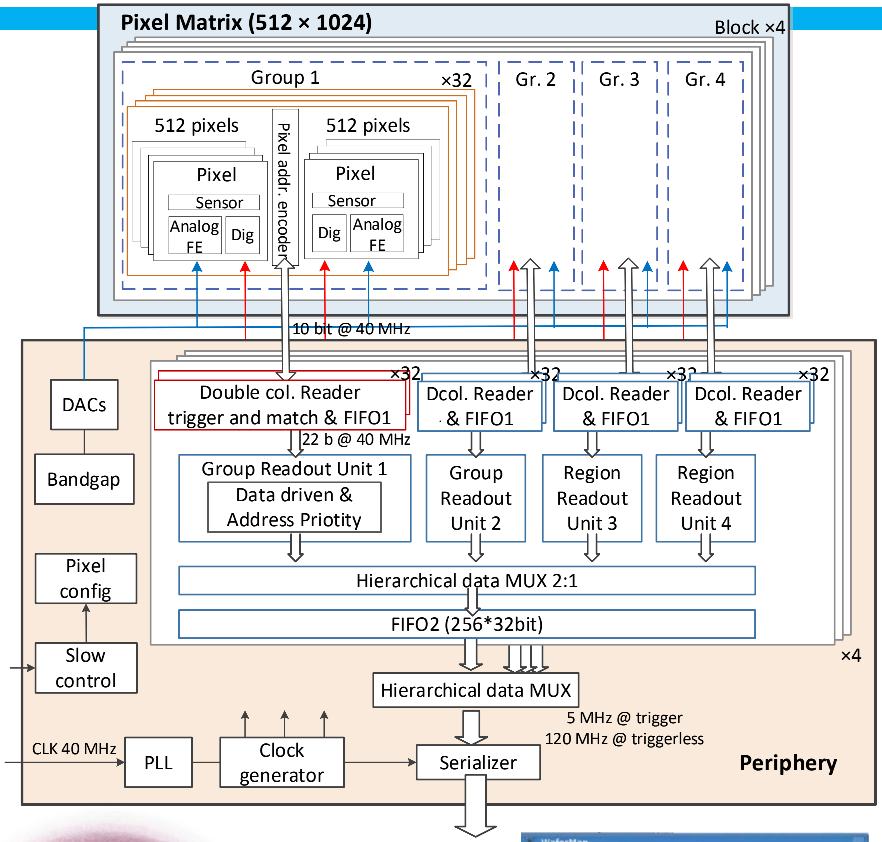


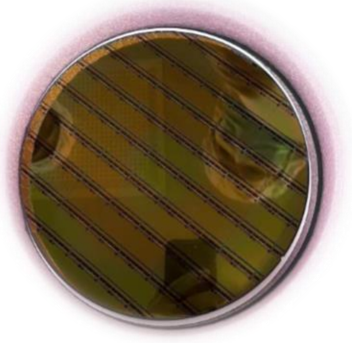


Delay time of FASTOR with respect to the pulse injection vs. injected charge. The delay time was measured by the timestamp of a step of 25 ns.

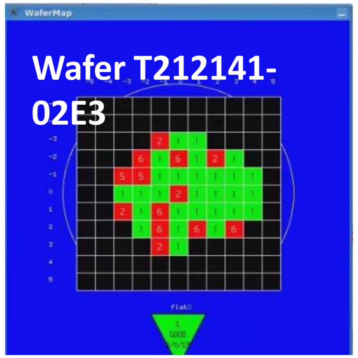
- Digital-in-Pixel scheme: in pixel discrimination & register
- Pixel analog is derived from ALPIDE (and benefit from MIC4 for MOST1)
  - As most of ATLAS-MAPS sensors' scheme
- Biasing current has to be increased, for a peaking time of ~25ns
  - for 40MHz BX @ Z pole
- Consequence:
  - Power dissipation increased
  - Faster CIS process has to be used
    - With faster charge collection time, otherwise only fast electronics is of no meaning

TaichuPix sensor architecture





8-inch wafer

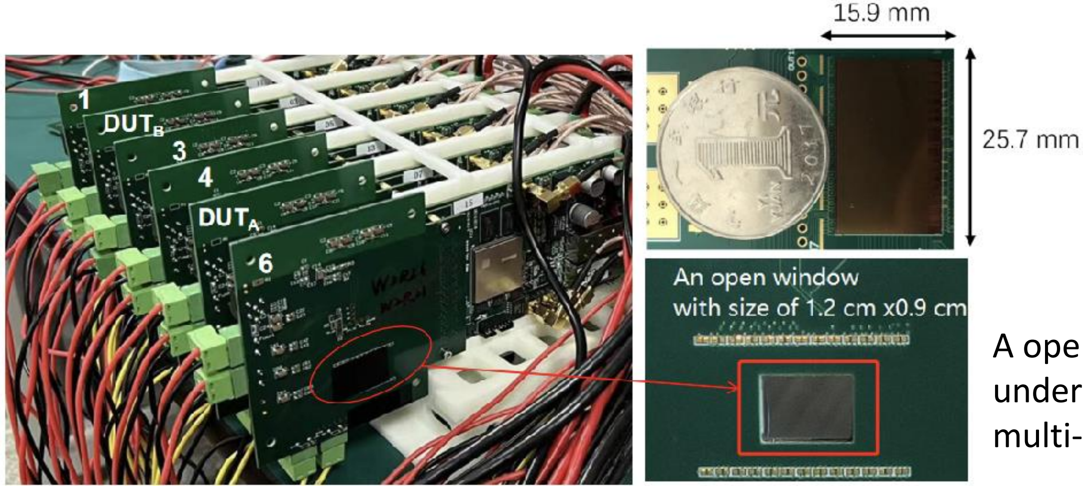


An example of wafer test result (yield ~67%)

- **Pixel 25 μm ╳ 25 μm**
  - Continuously active front-end, in-pixel discrimination
  - Fast-readout digital, with masking & testing config. logic
- **Column-drain readout for pixel matrix**
  - Priority based data-driven readout
  - Time stamp added at end of column (EOC)
  - Readout time: 50 ns for each pixel
- **2-level FIFO scheme**
  - L1 FIFO: de-randomize the injecting charge
  - L2 FIFO: match the in/out data rate between core and interface
- **Trigger-less & Trigger mode compatible**
  - Trigger-less: 3.84 Gbps data interface
  - Trigger: data coincidence by time stamp, only matched event will be readout
- **Features standalone operation**
  - On-chip bias generation, LDO, slow control, etc.

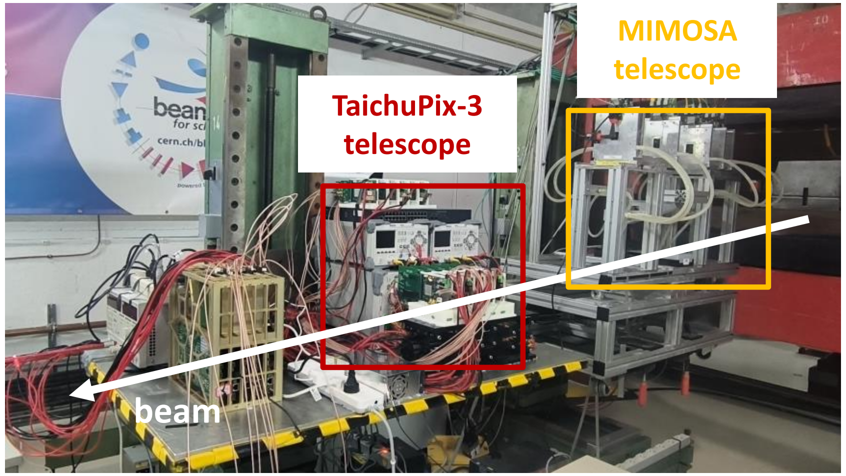
TaichuPix-3 telescope

- The 6-layer of TaichuPix-3 telescope built
  - Each layer consists of a TaichuPix-3 bonding board and a FPGA readout board

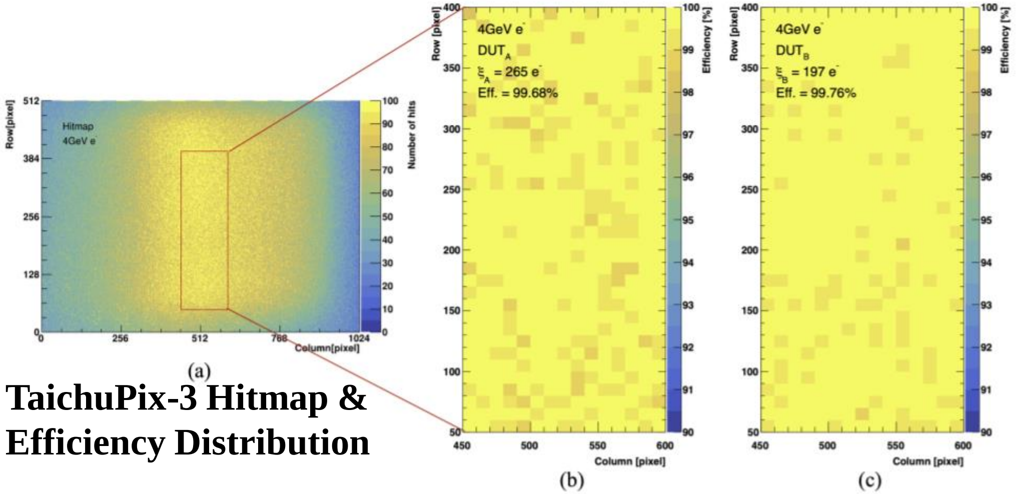


A open window on PCB under TC3 chip to reduce multi-scattering

6-layer TaichuPix-3 telescope



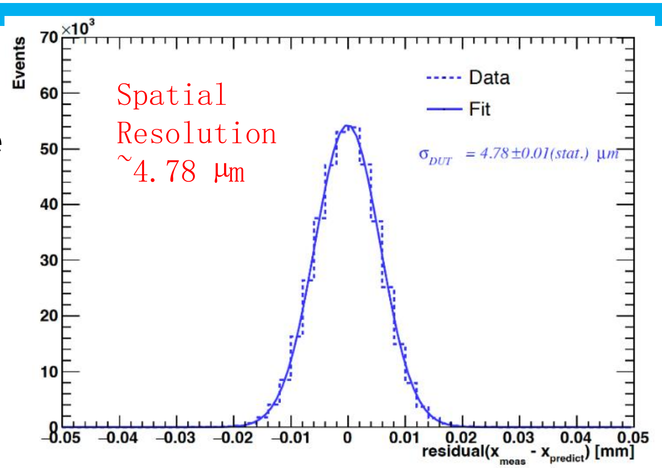
- **Setup in the DESY testbeam**
  - TaichuPix-3 telescope in the middle
  - Beam energy: 4 GeV mainly used
  - Tests performed for different DUT (Detector Under Test)



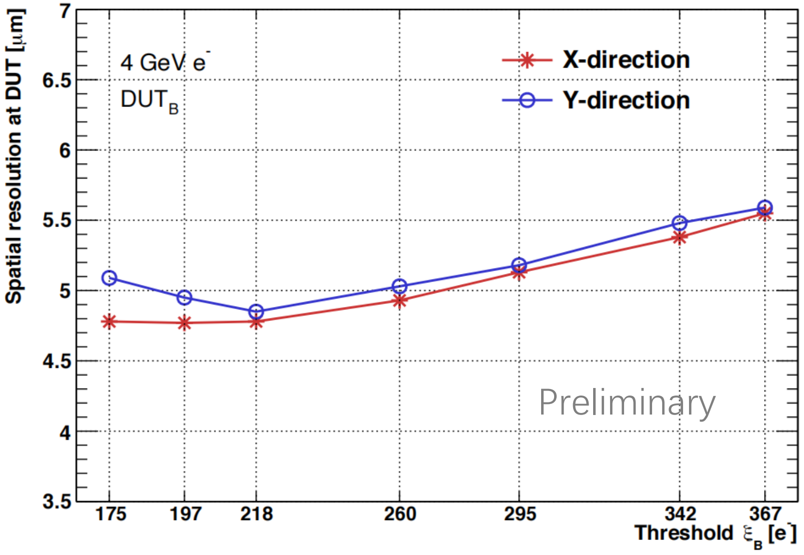
TaichuPix-3 Hitmap & Efficiency Distribution

TaichuPix-3 beam test result

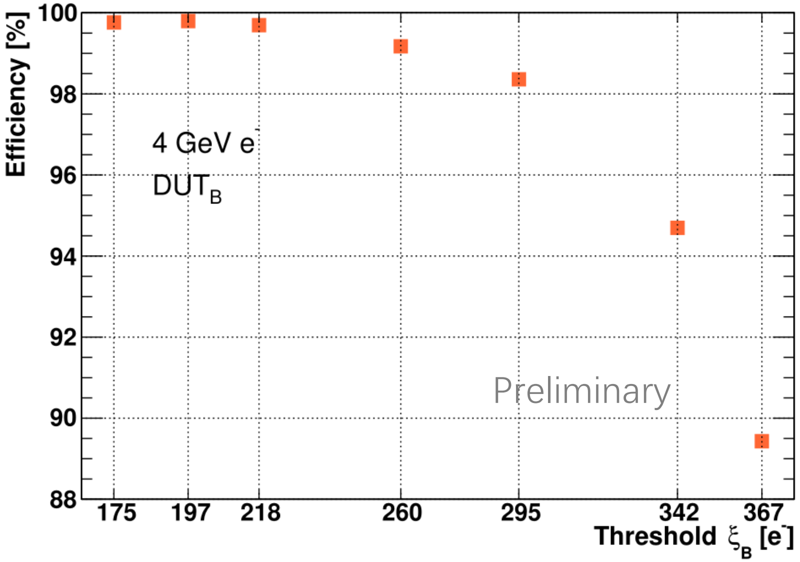
- Spatial resolution
  - Gets better when decrease the pixel threshold, due to the increased cluster size
  - A resolution < 5 μm achieved, best resolution is 4.78 μm
- Detector efficiency
  - Decreases with increasing the threshold, detection efficiency >99.5% at threshold with best resolution



Distribution of residual X

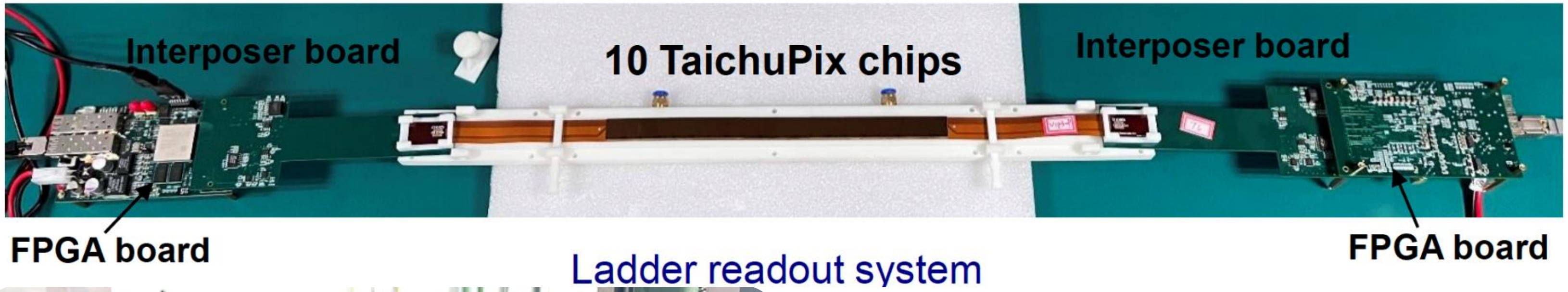


Spatial resolution vs. pixel threshold



Detection efficiency vs. pixel threshold

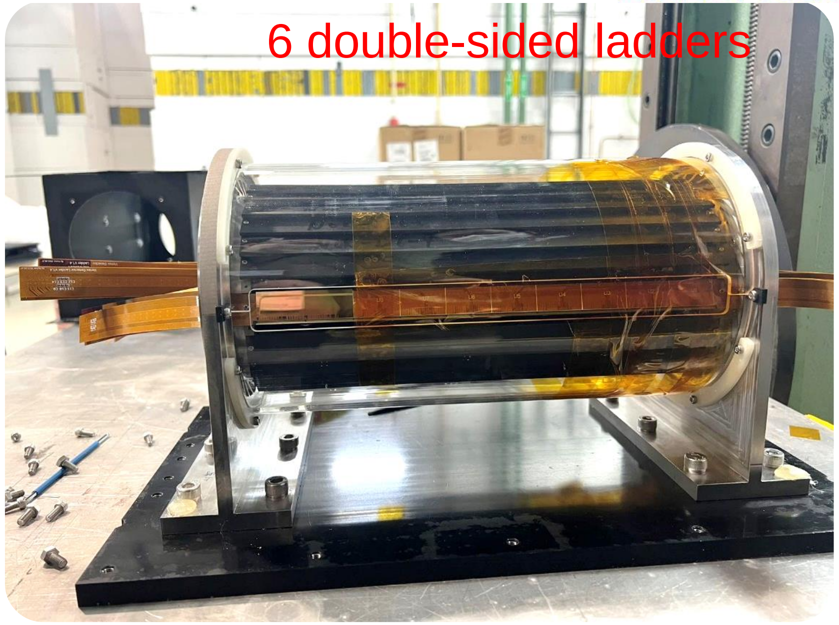
Vertex detector prototype

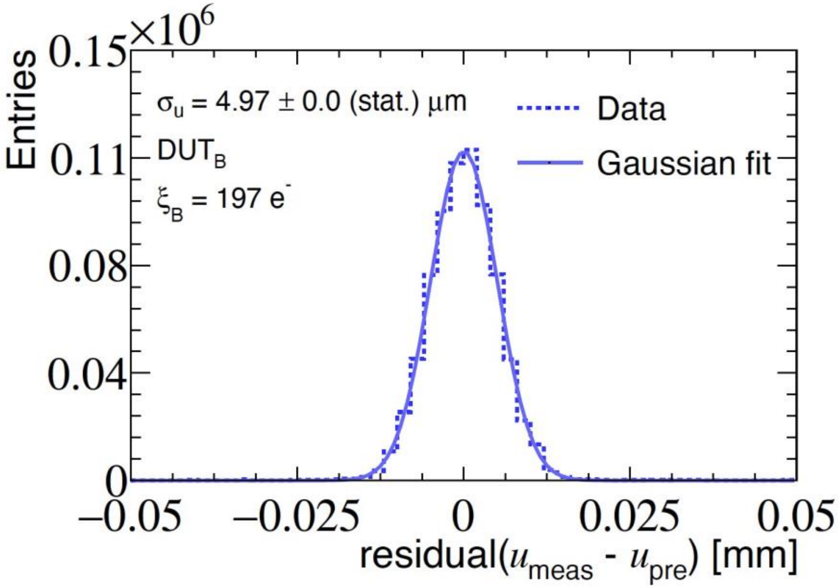


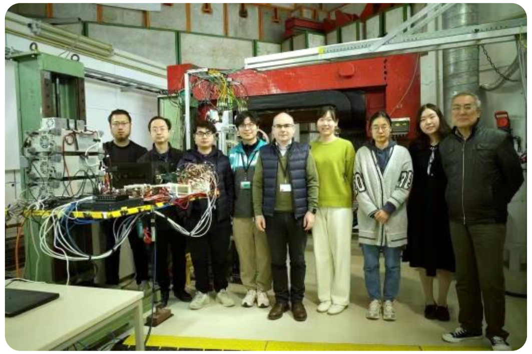
Ladder readout system

TaichuPix-based prototype detector tested at DESY in April 2023

Spatial resolution ~ **4.9 μm**





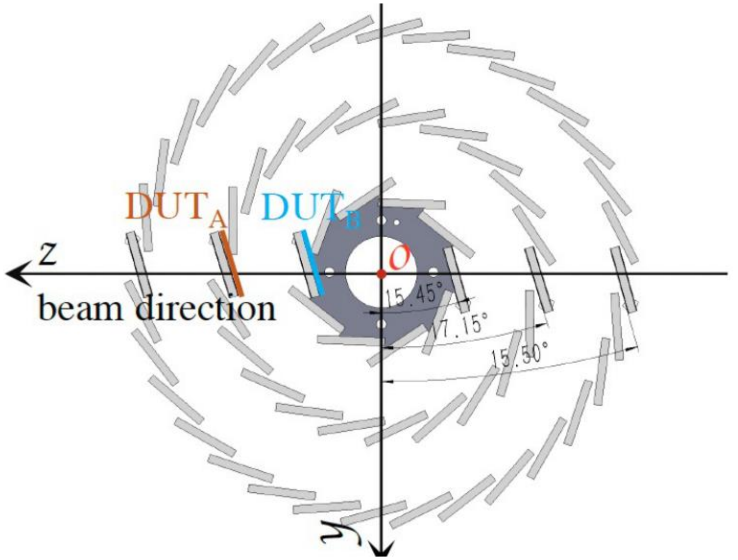


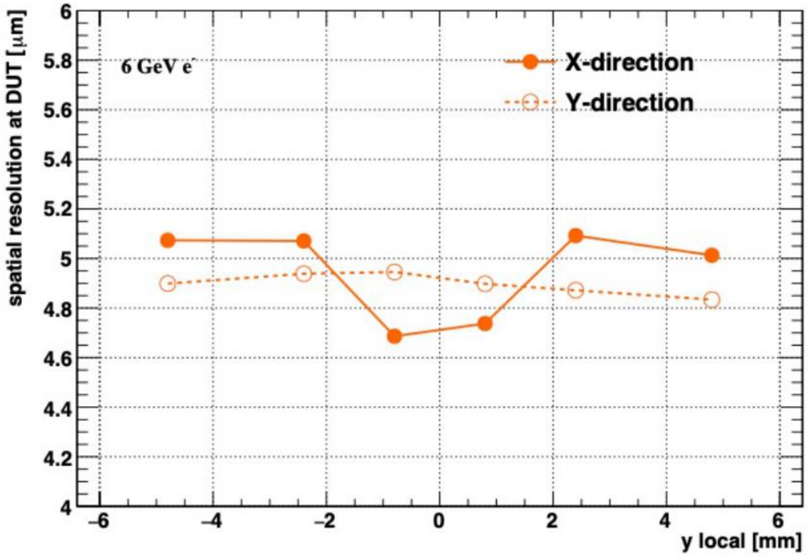
	Status	CEPC Final goal
Detector integration	Detector prototype with ladder design	Detector with bent silicon design

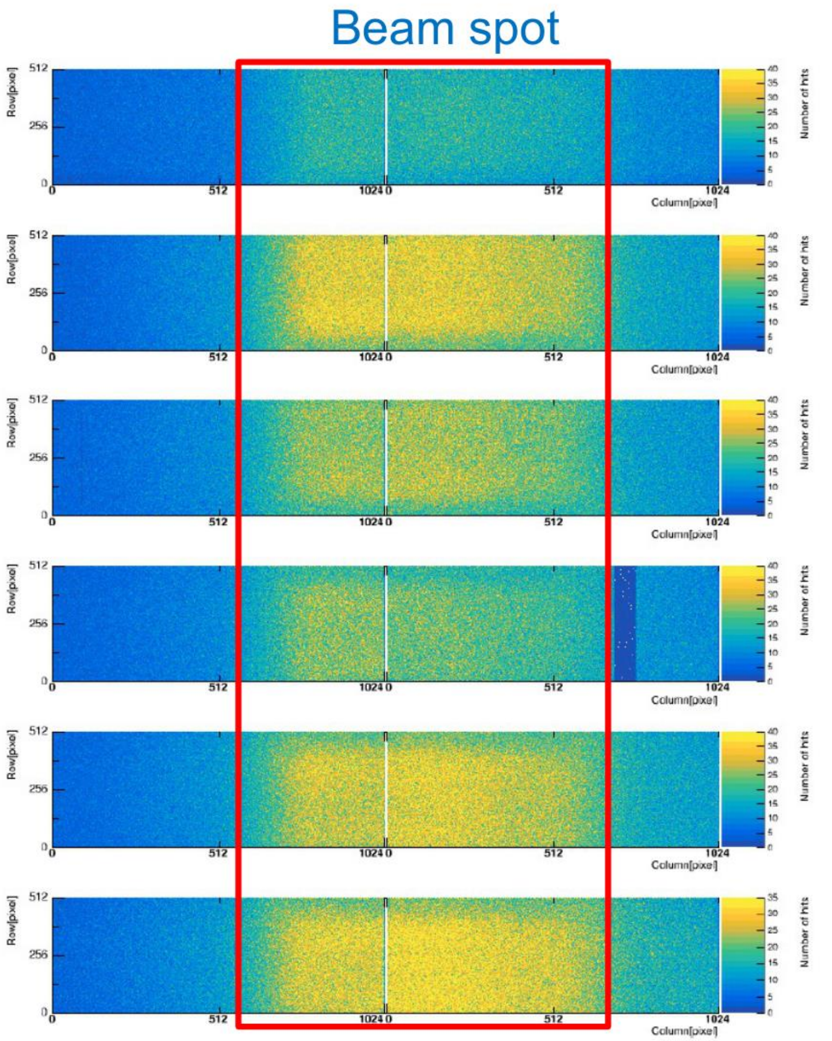
R&D efforts and results: vertex detector prototype beam test

Hit maps of multiple layers of vertex detector

Spatial resolution ~ **5 μm**



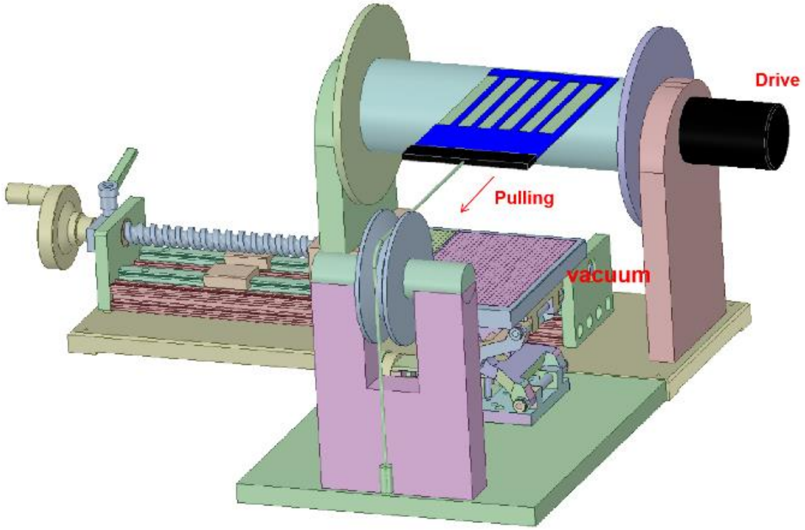


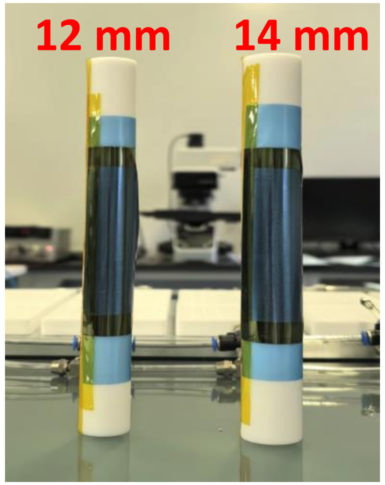


	Status	CEPC Final goal
Spatial resolution	4.9 μm	3-5 μm

R&D efforts curved MAPS

- CEPC b-layer radius (11mm) smaller compared with ALICE ITS3 (radius=18mm)
- Feasibility : Mechanical prototype with dummy wafer can curved to a radius of 12mm
  - The dummy wafer has been thinned to 40μm





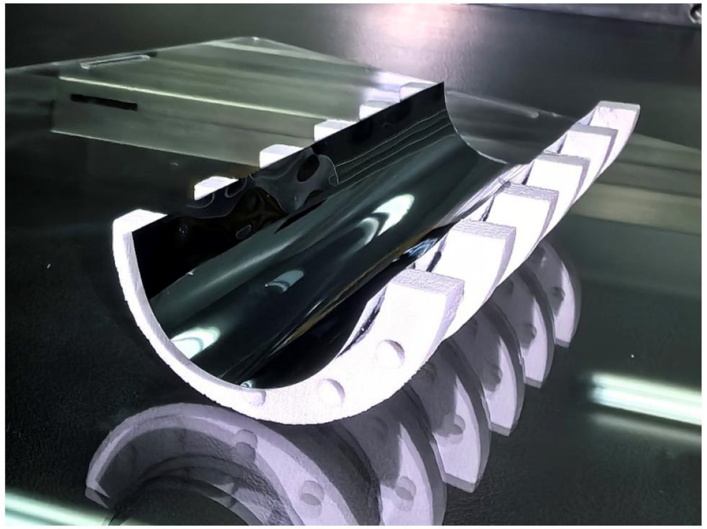


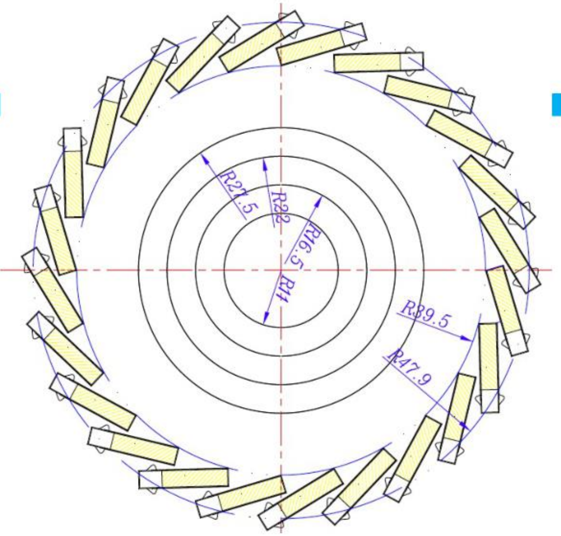
Figure 4.26: 12 mm bending radius.

	Status	CEPC Final goal
Bent silicon with radius	Bent Dummy wafer radius ~12mm	Bent final wafer with radius ~11mm

R&D status and final goal

Key technology	Status	CEPC Final goal
CMOS chip technology	Full-size chip with TJ 180nm CIS	65nm CIS
Detector integration	Detector prototype with ladder design	Detector with bent silicon design
Spatial resolution	4.9 µm	3-5 µm
Detector cooling	Air cooling with 1% channels (24 chips) on	Air cooling with full power
Bent CMOS silicon	Bent Dummy wafer radius ~12mm	Bent final wafer with radius ~11mm
Stitching	11╳11cm stitched chip with Xfab 350nm CIS	65nm CIS stitched sensor

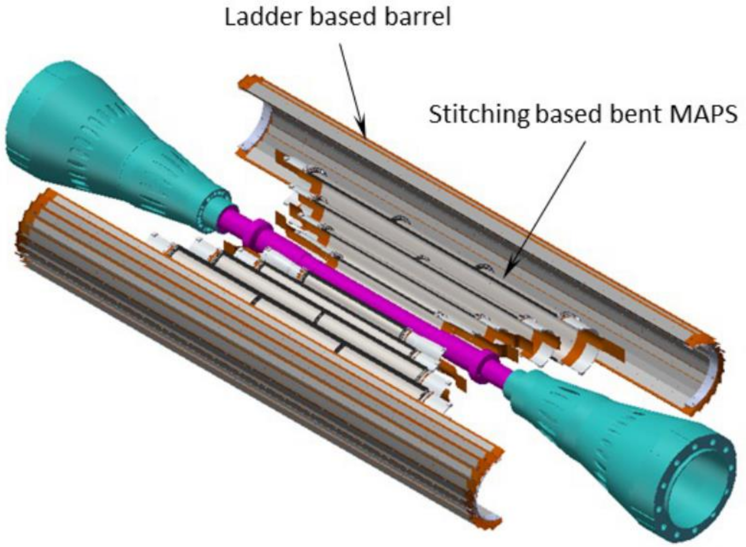
Baseline in Ref-TDR: bent MAPS

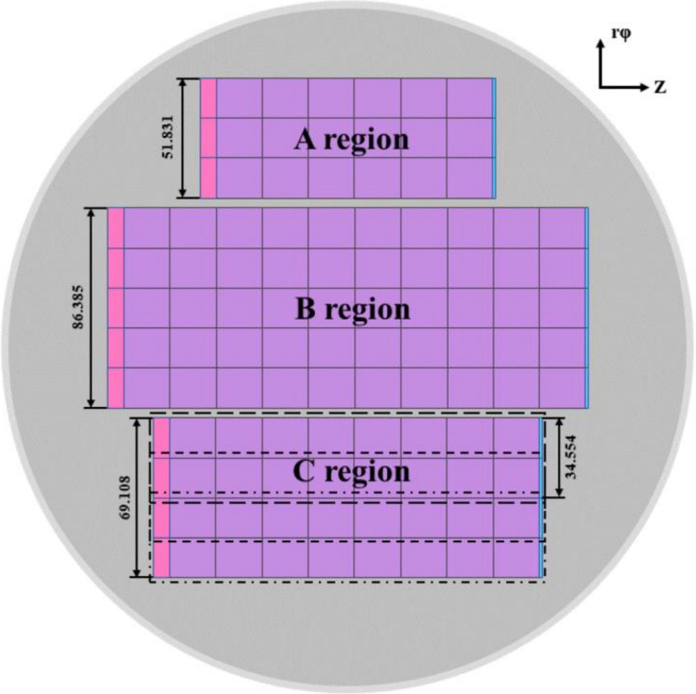


- 4 single layer of bent MAPS + 1 double layer ladder
  - Material budget is much lower than alternative option
- Use single bent MAPS for Inner layer (~0.15m^2)
  - Low material budget 0.06%X0 per layer
  - Different rotation angle in each layer to reduce dead area

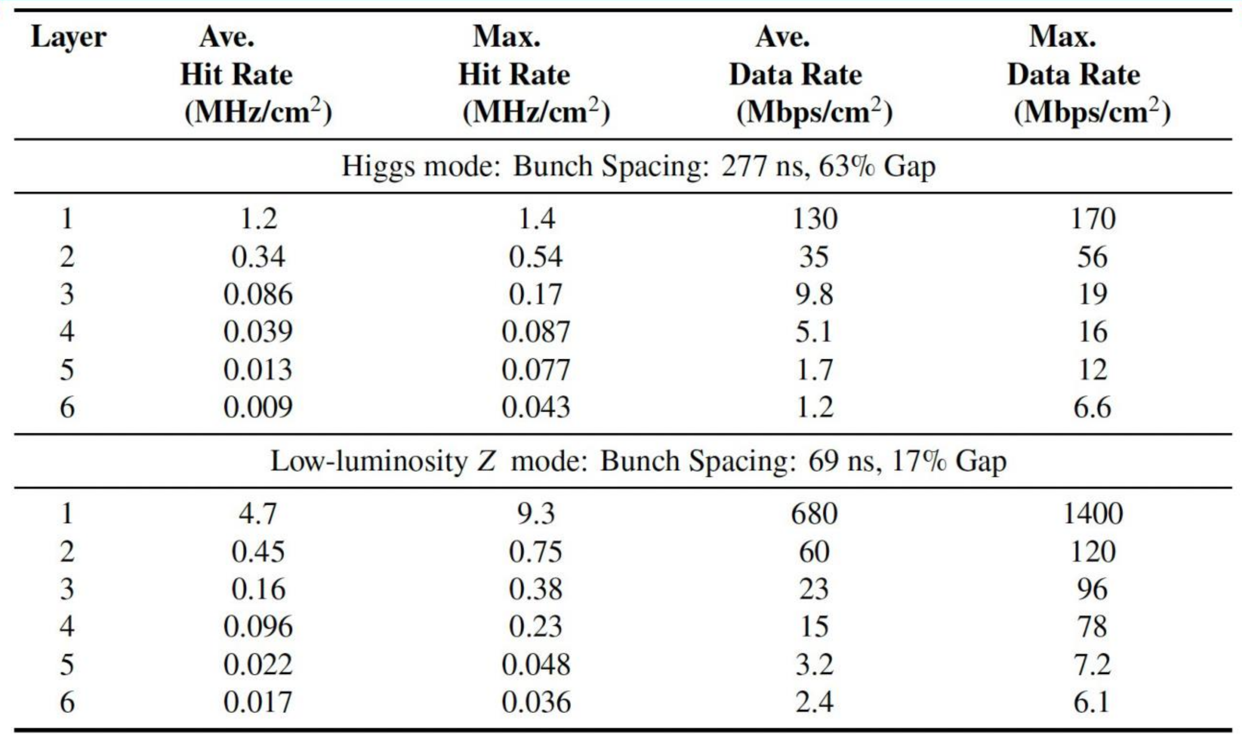
layer/VXD X	radius .mm	length .mm
layer 1	11.06	161.4
layer 2	16.56	242.2
layer 3	22.06	323.0
layer 4	27.56	403.8
VXD 5	39.50	682.0

Long barrel layout (no endcap disk)
to cover cos θ<=0.991

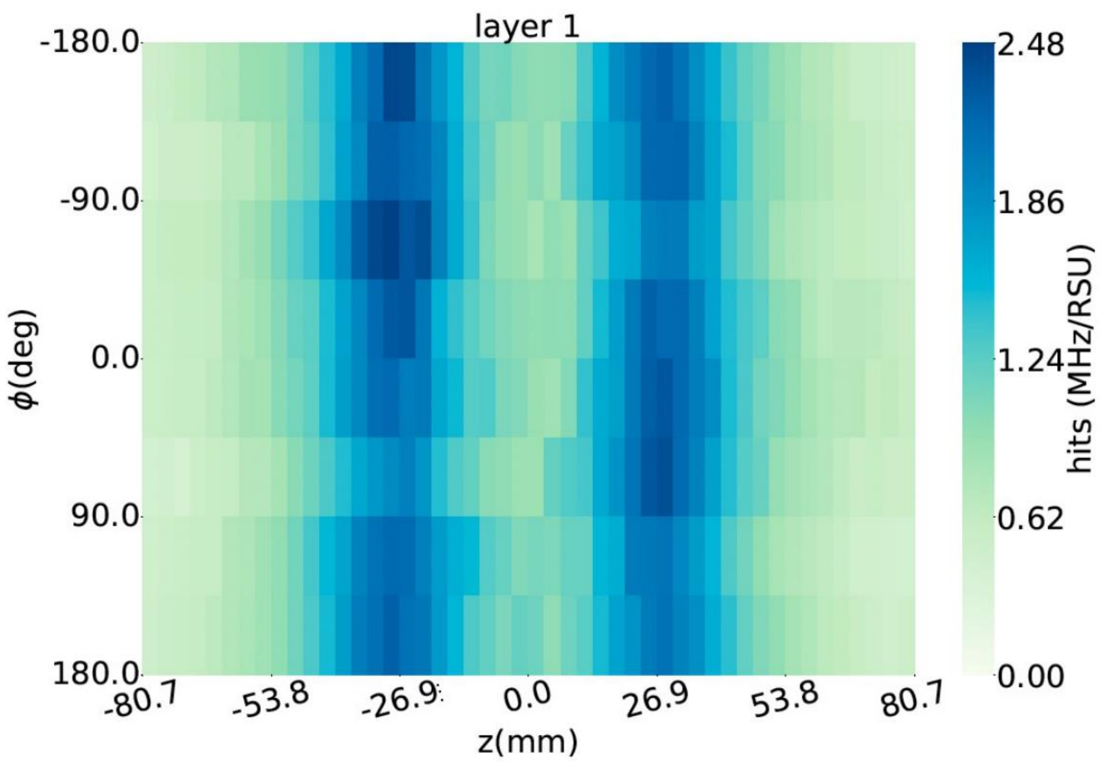




Data rate estimation of vertex detector



Layer	Ave. Hit Rate (MHz/cm^2)	Max. Hit Rate (MHz/cm^2)	Ave. Data Rate (Mbps/cm^2)	Max. Data Rate (Mbps/cm^2)
Higgs mode: Bunch Spacing: 277 ns, 63% Gap				
1	1.2	1.4	130	170
2	0.34	0.54	35	56
3	0.086	0.17	9.8	19
4	0.039	0.087	5.1	16
5	0.013	0.077	1.7	12
6	0.009	0.043	1.2	6.6
Low-luminosity Z mode: Bunch Spacing: 69 ns, 17% Gap				
1	4.7	9.3	680	1400
2	0.45	0.75	60	120
3	0.16	0.38	23	96
4	0.096	0.23	15	78
5	0.022	0.048	3.2	7.2
6	0.017	0.036	2.4	6.1



- **Data rate is dominated by background from pair production**
  - **Estimated based on old version of software**
- **WW runs and low Lumi Z runs (20% of high lumi Z)**
- **Data rate @1Gbps per chip for triggerless readout**

Detailed design： Electronics

– Stitching layer : stitching and RDL metal layer on wafer to replace PCB

– Outer layer (L5/L6) : flexible PCB （ also used in alternative layout)

  - Signal, clock, control, power, ground will be handled by control board through flexible PCB

Stitching layers : ALICE ITS3 like stitching

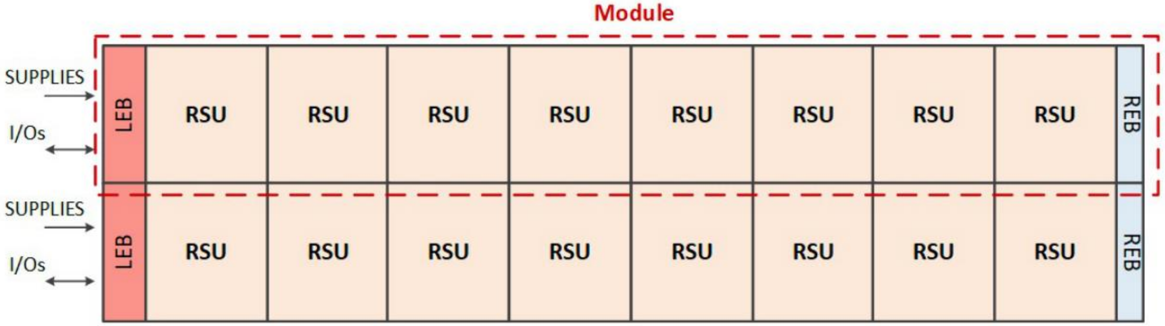


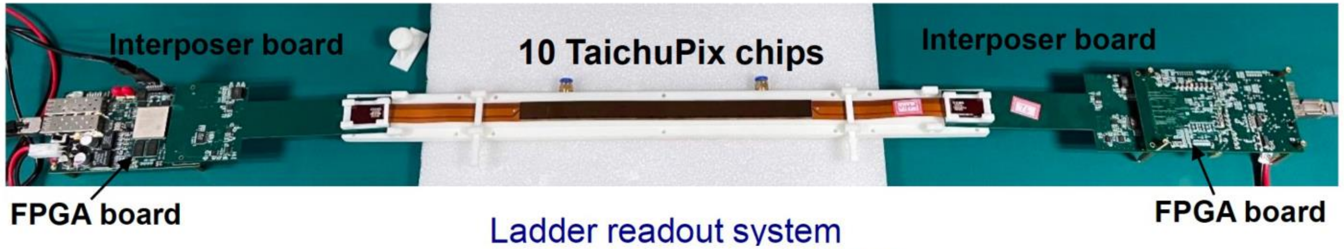
Figure 4.15

Table 4.12, Estimates of average power dissipation per unit area

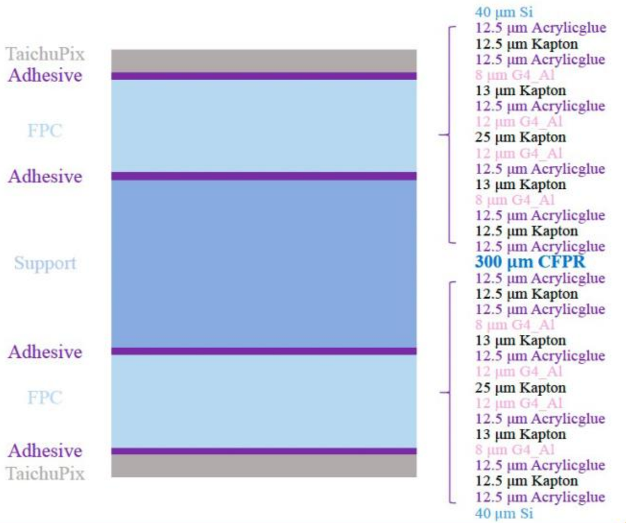
	Power density [mW/cm^2]
Repeated Sensor Unit	38
Left-End Block	485

[1] ALICE ITS3 TDR: https://cds.cern.ch/record/2890181

Outer layer (layer 5/6,)： flexible PCB

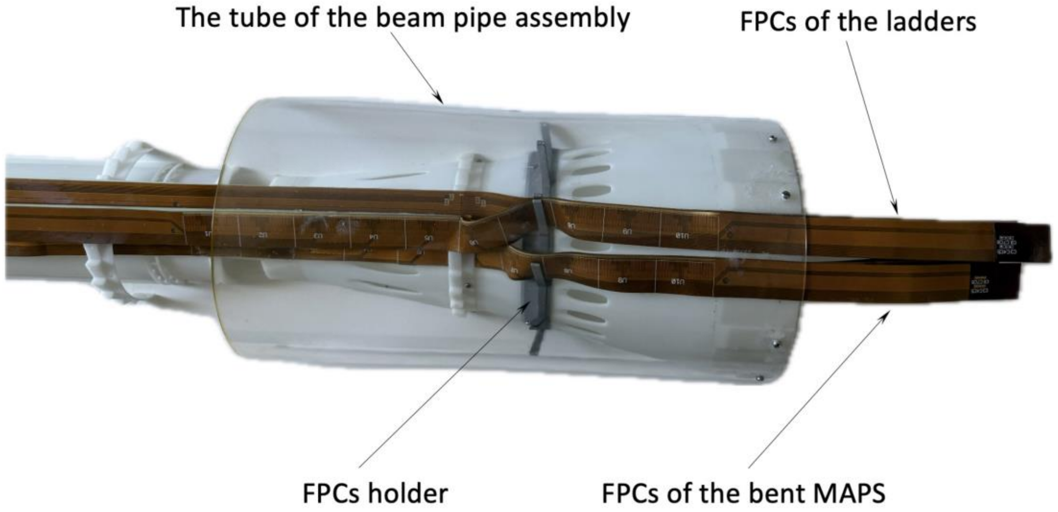


Ladder readout system



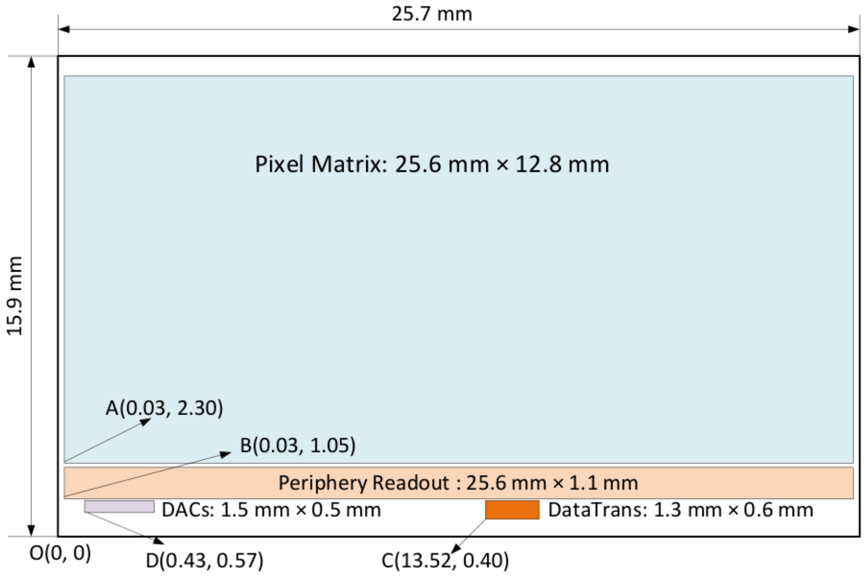
Mockup to validate cable routing

- Full-size 3D printed vertex detector and beam-pipe mockup
  - Validate there is enough space for cable routing and air cooling channel
  - The total cross-sectional area available for air cooling in the inner four layers is 12.6 cm^2



Chip design for ref- TDR and power consumption

- Power consumption
  - **Fast priority digital readout** for 40MHz at Z pole
  - 65/55nm CIS technology
  - Power consumption can reduced to ~40mW/cm²
- Air cooling feasibility study
  - Baseline layout can be cooled down to ~20 ℃
    - Based on 7 m/s air speed, estimated by thermal simulation

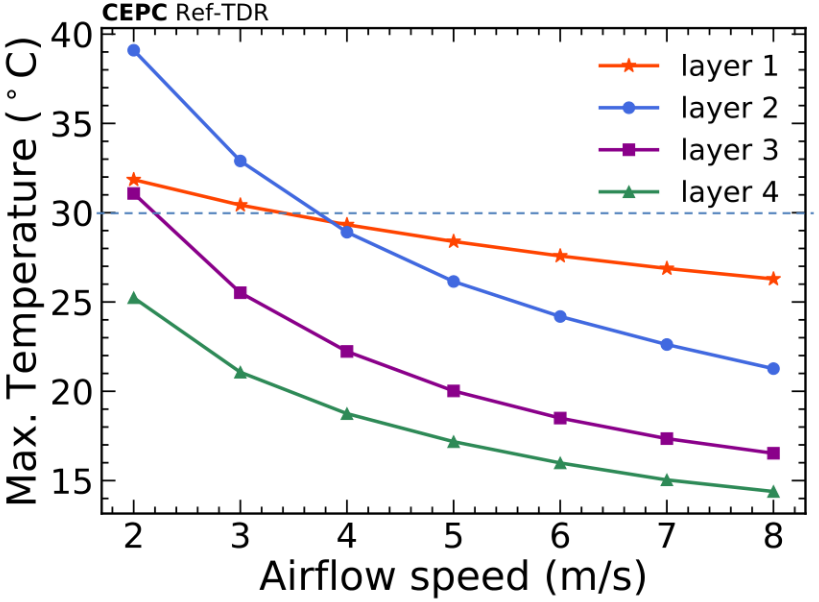


	Matrix	**Periphery**	**DataTrans.**	**DACs**	**Total Power**	**Power density**
TaiChu3 180nm chip @ triggerless	304 mW	135 mW	206 mW	10 mW	655 mW	160 mW/cm²
65nm for TDR @ 1 Gbps/chip (TDR LowLumi Z)	60 mW	80 mW	36 mW	10 mW	186 mW	~45 mW/cm²

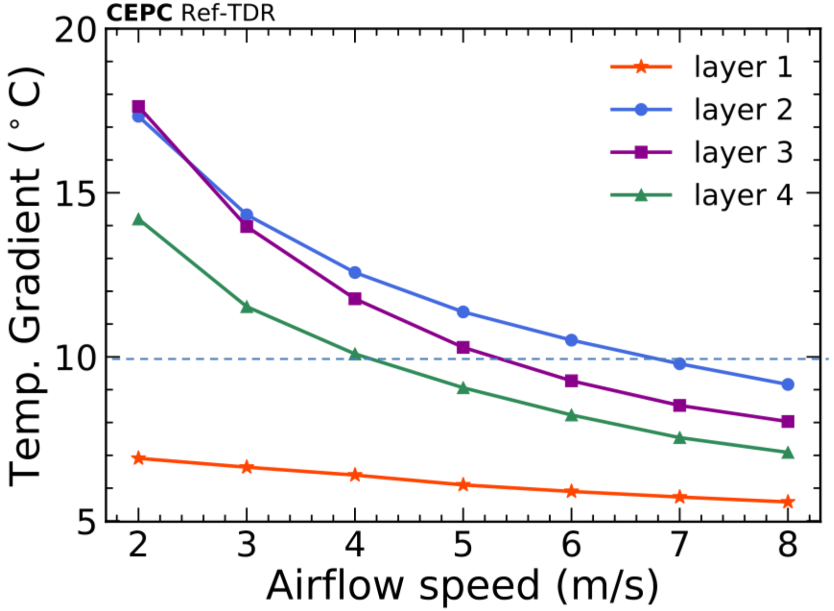
Thermal simulation

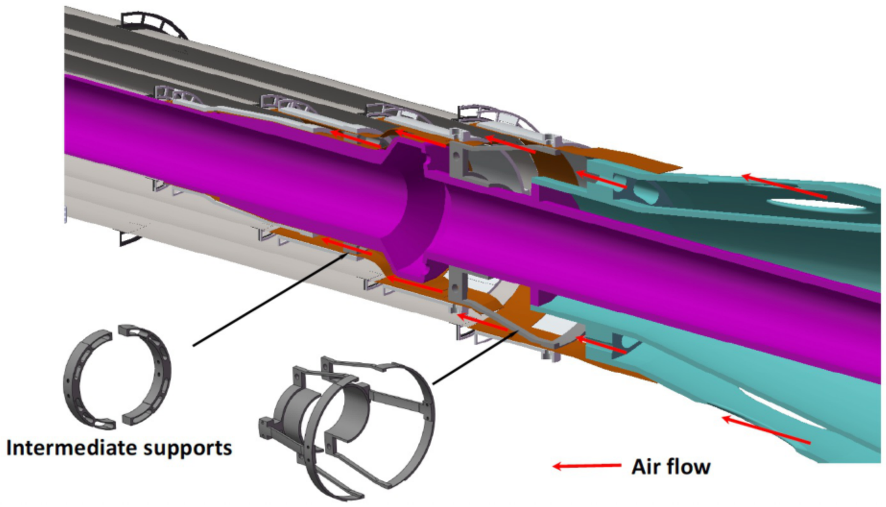
- New thermal simulation, baseline air speed increased from 3.5m/s to 7m/s
  - All Obstacles and Thermal gradients considered (just included support structure and flexible cable)

Maximum temperature in stitching layers



Temp. Gradient in stitching layers

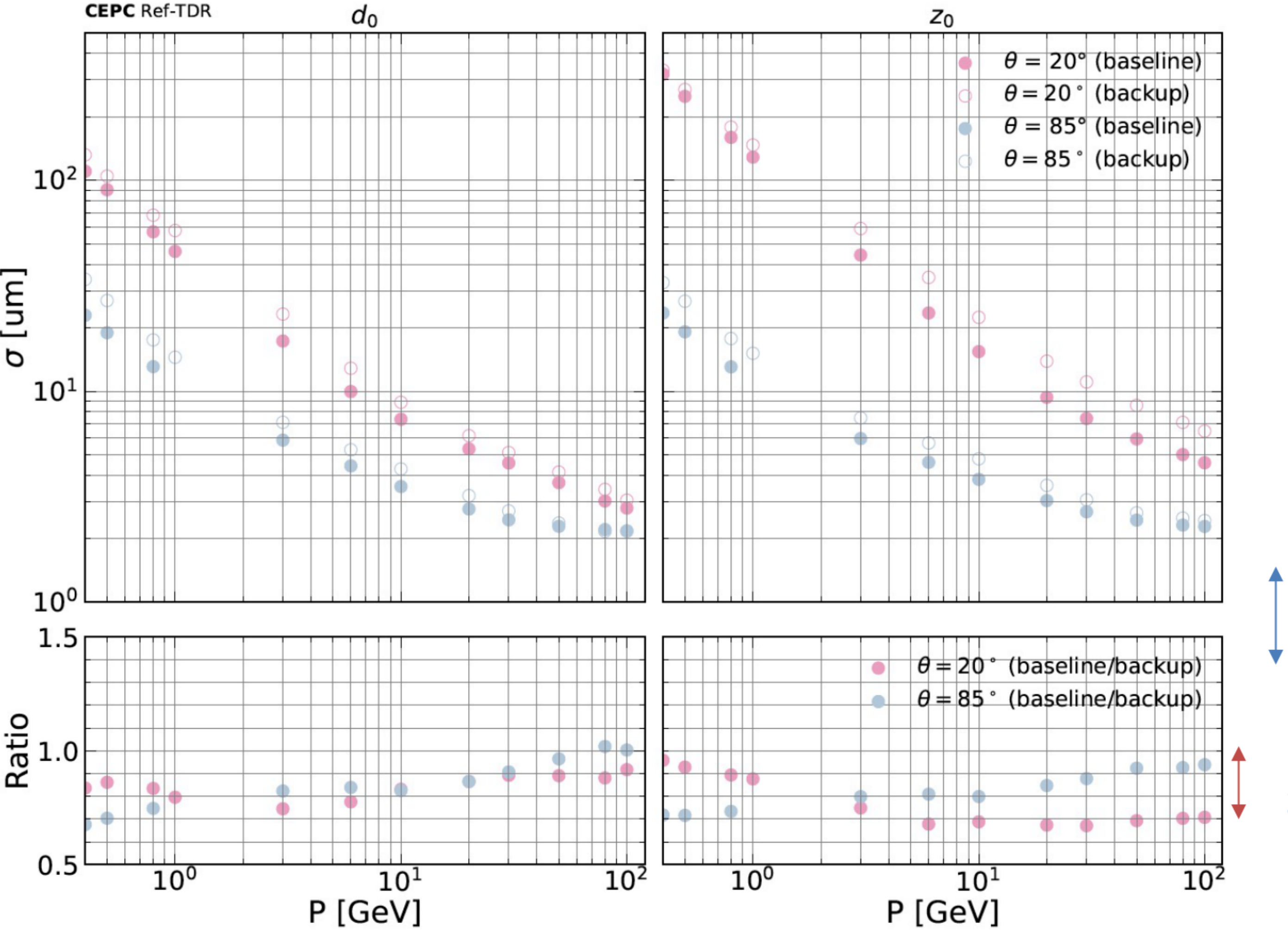




Performance: impact parameter resolution

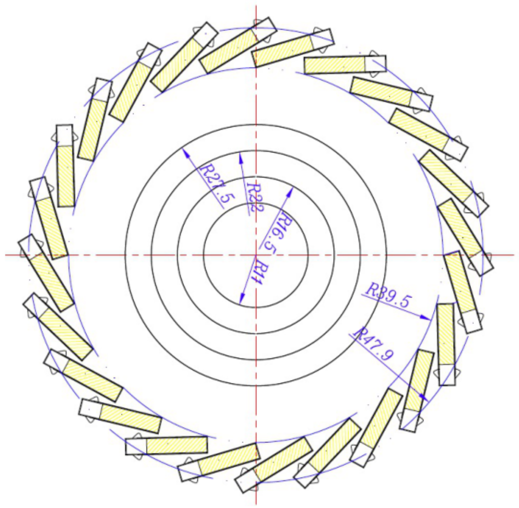
- Baseline has better resolution than alternative (ladder) (25-40%) in low momentum

d0 resolution: Baseline Vs backup layout

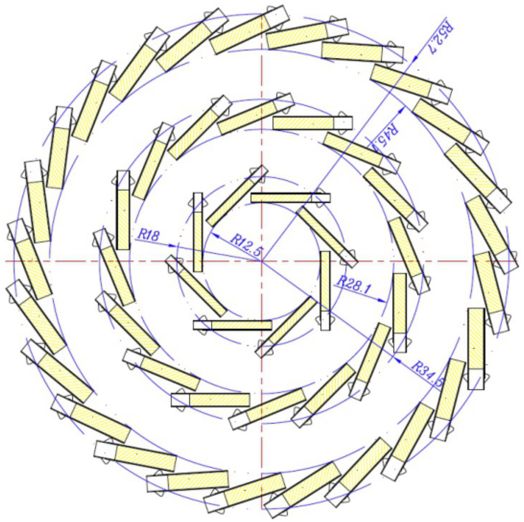


30%

Baseline layer
4 stitching +
1 double layer ladders

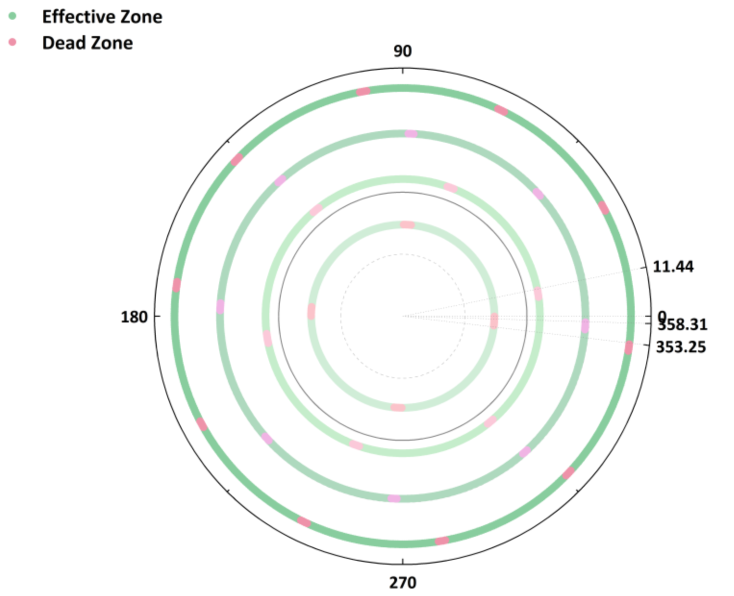


Backup layout
3 double layer ladders



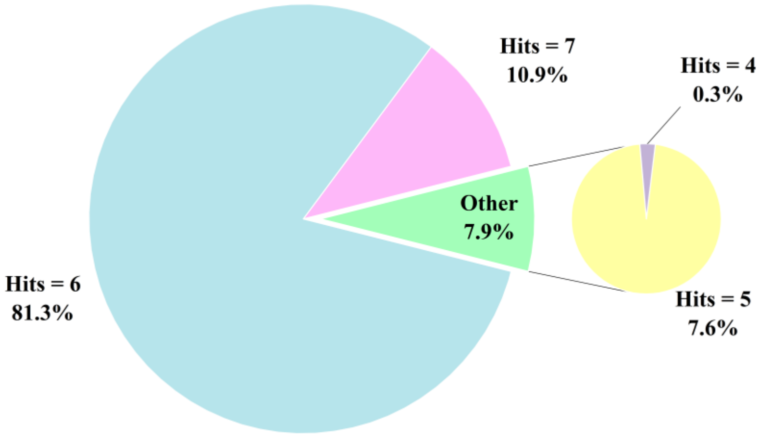
Performance: Efficiency

- A few percent Inefficiency expected in stitching layer
- Sensor (RSU) has inefficiency region in power stitch
- 99.7% of the track with >=4 hits (6 hits expected)

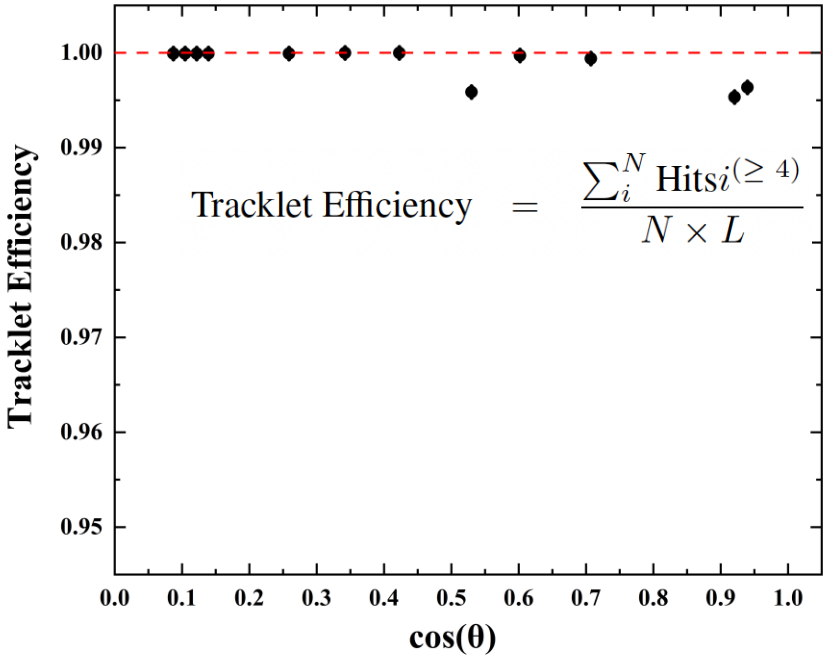


Schematic diagram of the Inner layer placement of the vertex detector stitching scheme.

Number of hits



Tracklet efficiency



$$\text{Tracklet Efficiency} = \frac{\sum_i^N \text{Hits}\, i^{(\geq 4)}}{N \times L}$$

RSU design

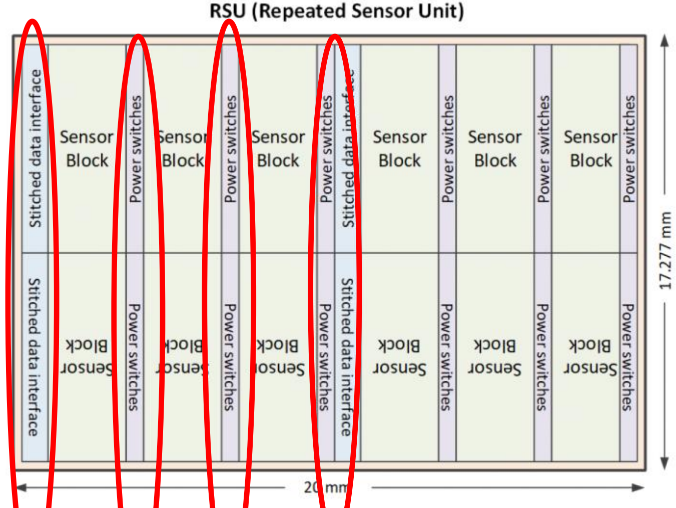


Figure 4.50: Proposed floor-plan for a repeated sensor unit (RSU) (not to scale). It contains several identical senso
blocks. Each of them has a pixel matrix with its own biasing generator, slow control and periphery readout circuit. Eac
sensor block can be selectively switched on/off. The stitched data interface blocks are used to transmit control signals an
data to the edge of the stitching sensor.

Research team

- IHEP: 8 faculty, 2 postdoc, 5 students
- CERN: Recent joint R & D collaboration in HLMC 55nm aiming for ALICE3 upgrade
- IPHC/CNRS: Christine Hu et al (3 faculty): Collaboration in FCPPL and DRD3
  - CEPC Jadepix design, ALICE ITS3 upgrade (especially on MAPS design, stitching)
- IFAE: Chip design , Sebastian Grinstein et al (2 faculty)
  - CEPC Taichupix chip design, ATLAS ITK pixel and HGTD upgrade
- ShanDong U.: Stitching chip design (3 faculty, 1 postdoc, 3 students)
- CCNU: chip design, ladder assembly (2 faculty , 3 students)
- Northwestern Polytechnical U. : Chip design (5 faculty, 2 students)
- Nanchang U. : chip design, (1 faculty, 1 students)
- Nanjing: irradiation study, chip design : (2 faculty, 4 students)

Choice of technology for next R & D

- Next step foundry: SK hynix system fab in Wuxi China (90nm technology with stitching feasibility

	Requirements	TPSCo 65 nm	HLMC 55 nm	HC90L
Feature size	55 – 90 nm	65 nm	55 nm	90 nm
Epitaxial layer thickness	10 - 25 μm	10 μm	3-5 μm	4 – 8.5 μm (default) Can be changed to 20μm
Resistivity of epi-layer	> 1 kΩ•cm	~130 Ω•cm	Low resistivity ~10 Ω•cm	30-50 Ω•cm (default) Can upgraded to 5kΩcm
Availability of deep N-well	Yes	Yes	Yes	Yes
Availability of deep P-well	Yes	Yes	Yes	Optional
Numbers of metal layers	> 6	Max. 7	Max. 5	Max. 5
Availability of stitching	Yes	Yes	Yes	Yes
Cost (NRE)		~7.0 M RMB	~6.0 M RMB	2~3 M RMB

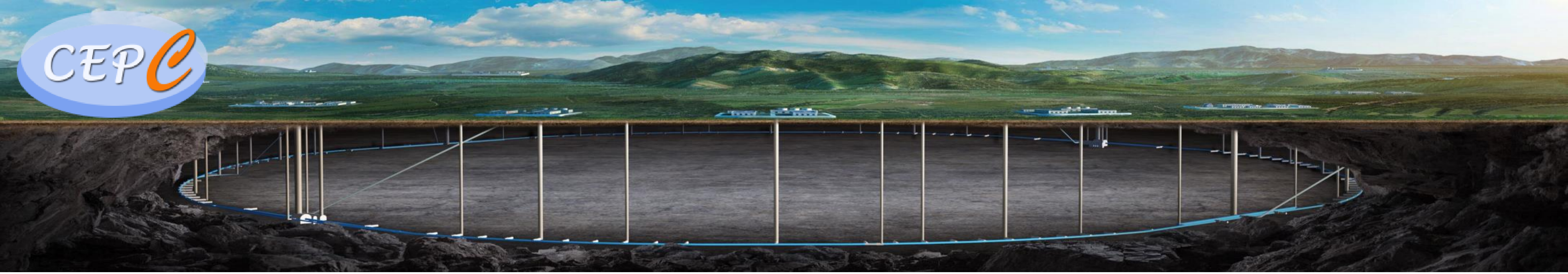
CEPC vertex detector Working plan

- Development of 1st engineering run using MAPSs with HC90L 90nm technology
  - Prototype full size RSU-like sensor
  - Validate sensor and electronics performance without stitching
  - Expect to finalize the design by the end of 2026

- Work together with mechanics group on thermal mockup
  - Test air cooling and the vibration
- Longer term: Explore CIS stitching MAPSs sensor with HC90L 90nm
- Final goal: Built prototype close to ref-TDR design

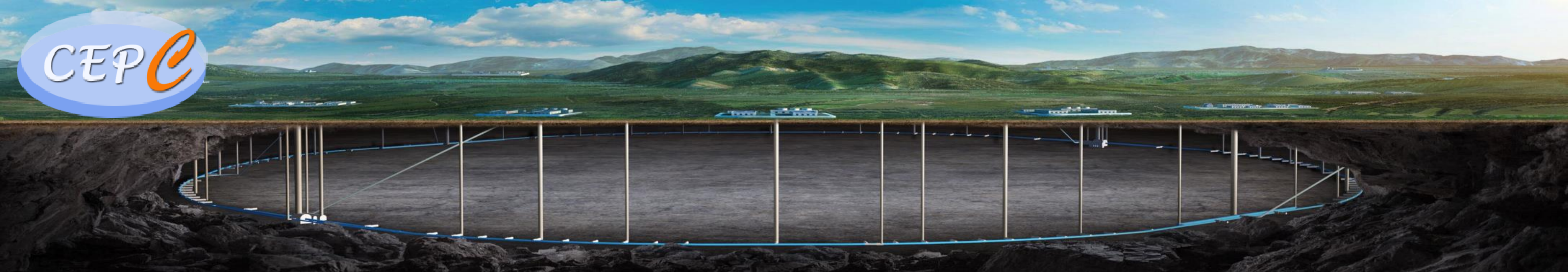
Summary

- Curved MAPS option chosen as baseline for Reference detector TDR. （arXiv:2510.05260）
- We active expanding international collaboration and explore synergies with other projects
  - We are member of ECFA DRD3 collaboration
  - Interested in to TPSCo 65nm runs in DRD3
  - Plan to propose HC90L MAPS R & D project to DRD3 in near future.



Thank you for your attention!

中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences

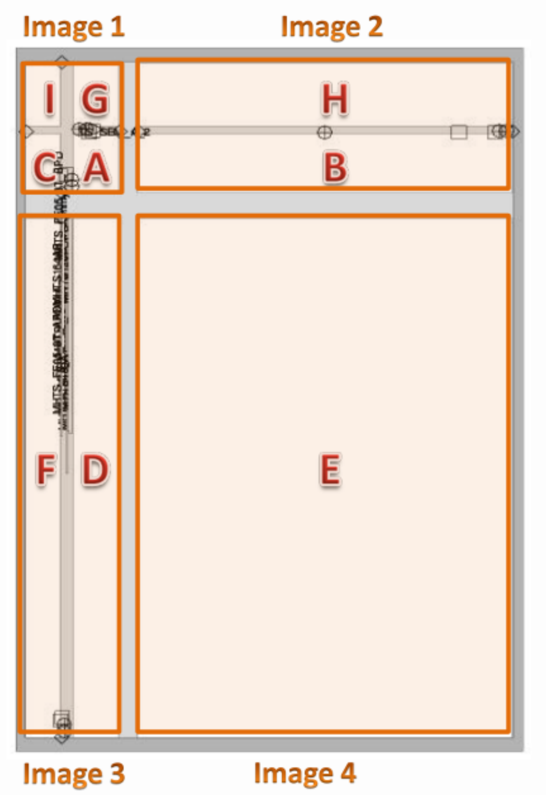


Backup Slides

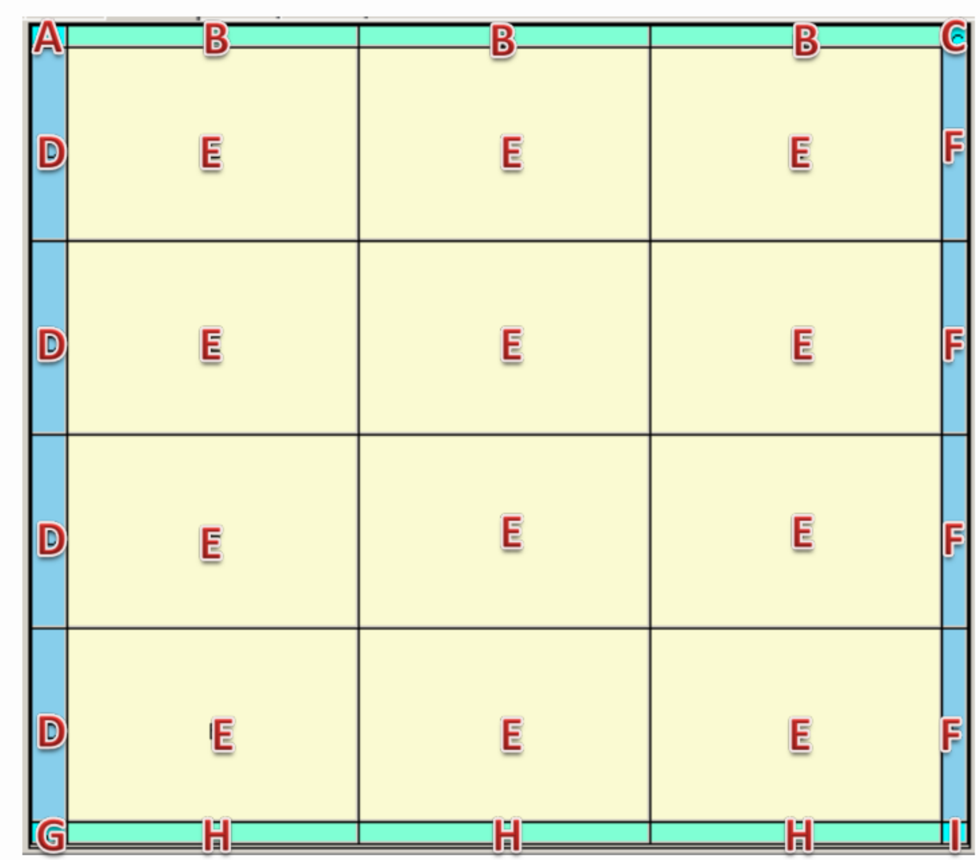
中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences

Principles of stitching

- **Design reticle is divided into segments, correspond to sub-frames of the photo-masks. During the photo-lithographic, these sub-frames are selectively exposed onto adjacent locations according to a pre-established pattern.**



Reticle with segments



Exposures on the wafer and resulting circuits

A Stitching MAPS for CEPC

- RSU
  - 像素阵列-像素单元设计
  - RSU外围读出逻辑
  - 数据读出接口
  - 偏置电路
  - 慢控配置
  - Stitching良率控制策略
- LT CAP
  - 数据接口：
    - ➢ 数据汇总-编码-输出驱动
    - ➢ 慢控配置接口
- RT CAP
- 全局backbone设计
  - 数据backbone
  - 电源backbone

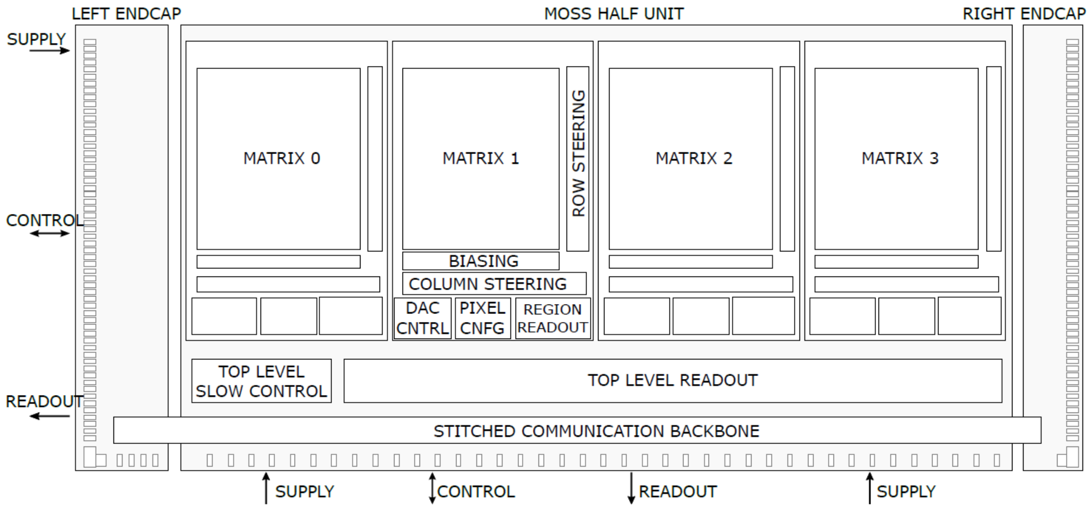
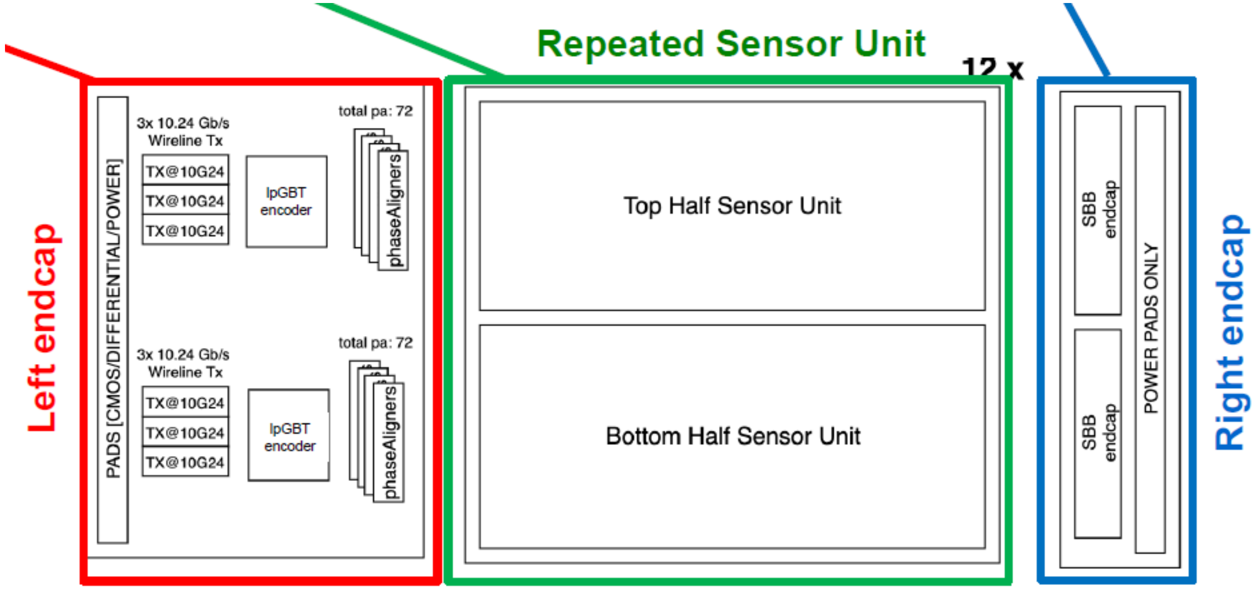


Figure 3.12: Block diagram of one bottom half unit of a RSU in the MOSS.



Ref.: Ola Groettvik @ TWEPP2023

LEC @ Stitching

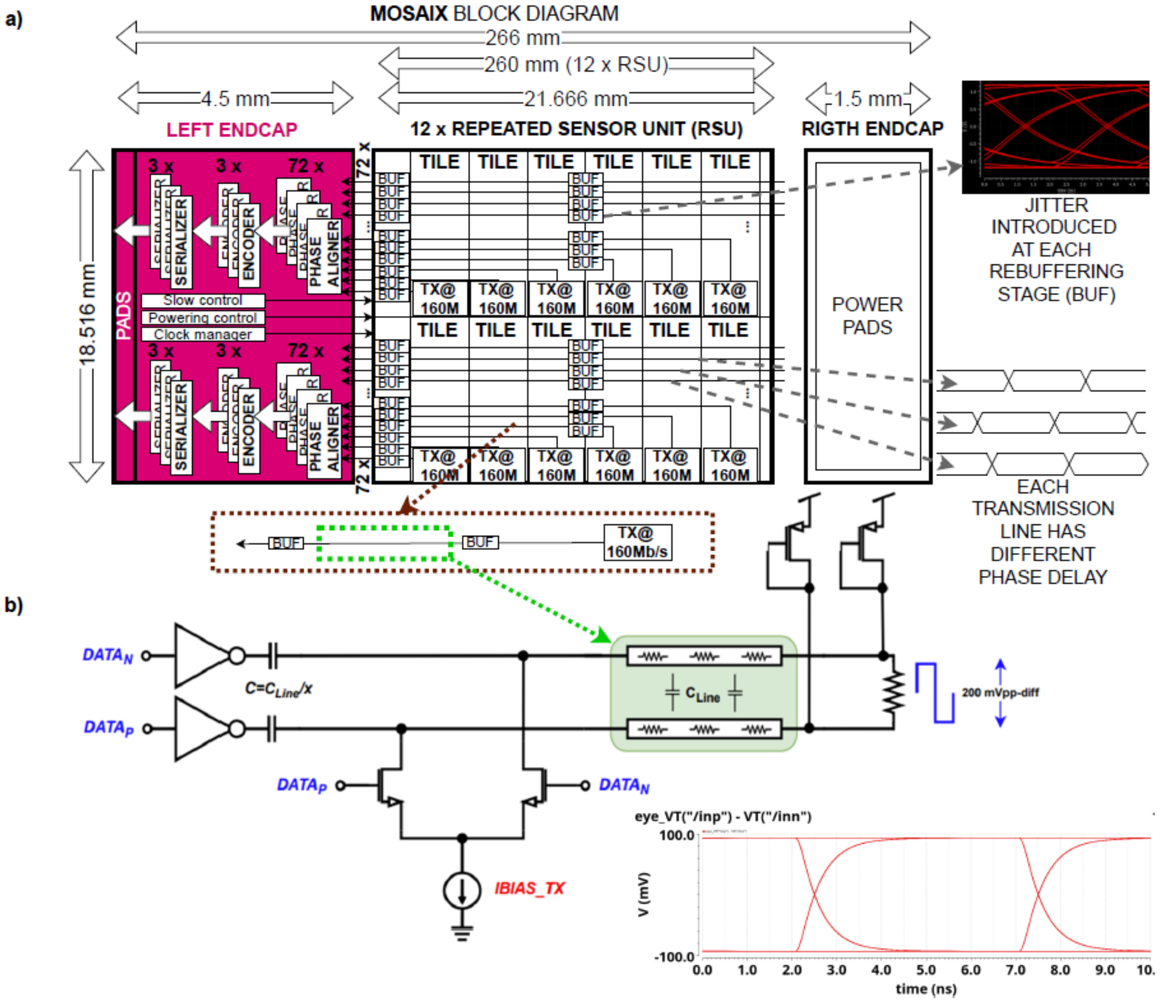


Figure 3. Block diagram of MOSAIX: a) data transmission path from tiles (TX @ 160 Mb/s) to the left endcap b) simplified schematic of one section of an on-chip transmission link with the simulated eye-diagram of the analog model of the section.

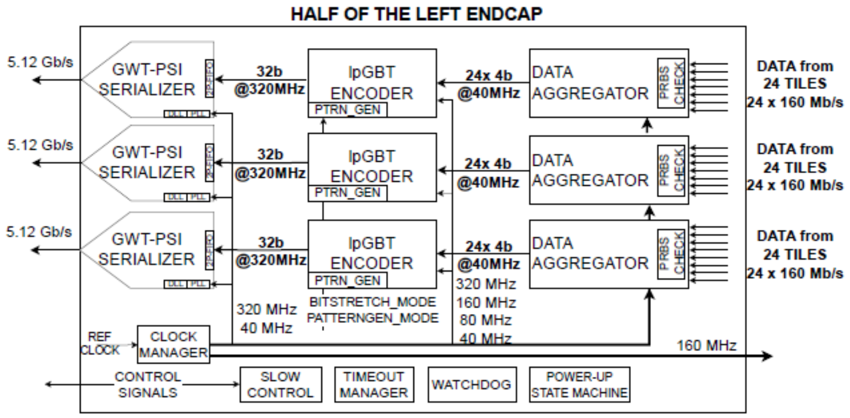
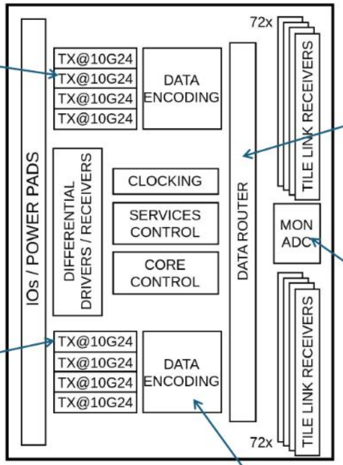


Figure 4. Block diagram of a half of the left endcap.

LEC: data hub



8x GWT-PSI
high speed serializer

forwards data to
different serializers

local power supply voltages
unit bias voltages

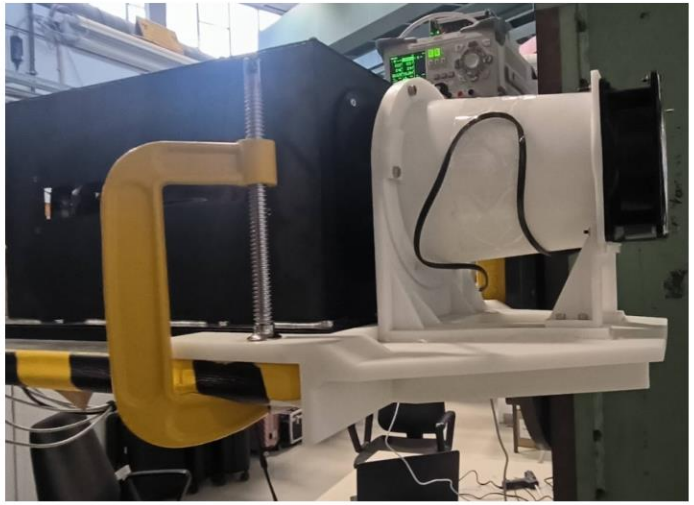
connects to VTRX+

lpGBT frame encoder

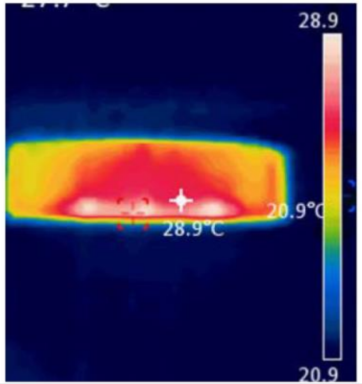
Ref.: https://doi.org/10.1088/1748-0221/19/04/C04050

R&D efforts: Air cooling in vertex prototype

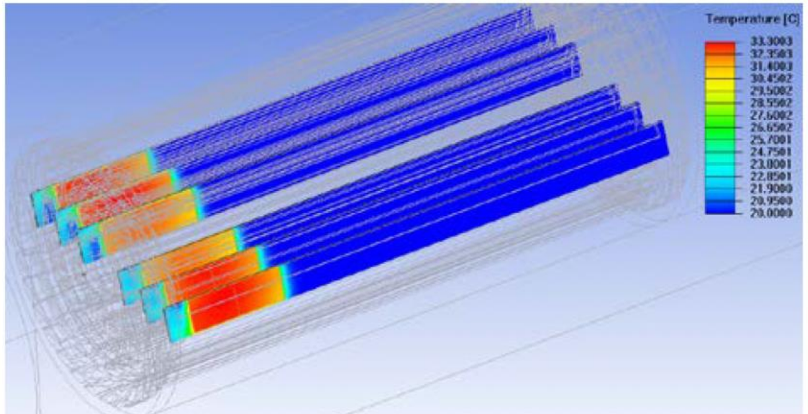
- Dedicated air cooling channel designed in prototype.
  - Measured Power Dissipation of Taichu chip: ~60 mW/cm^2 (17.5 MHz in testbeam)
  - Before (after) turning on the cooling, chip temperature 41 °C (25 °C)
    - In good agreement to our cooling simulation
    - No visible vibration effect in spatial resolution when turning on the fan



Chip temperature under cooling during beam test: Max 28.9 ℃



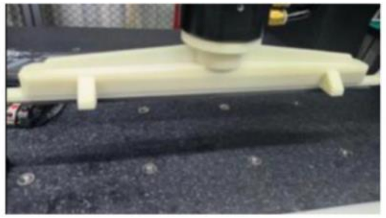
Prototype cooling simulation： Max 33.3 ℃



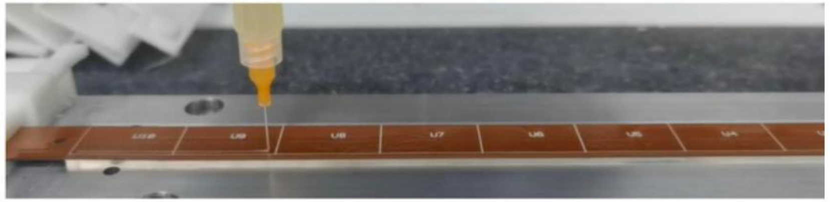
Key technology	Status	CEPC Final goal
Detector cooling	Air cooling with 1% channels (24 chips) on	Air cooling with full power

TaichuPix3 vertex detector prototype

New pickup tools

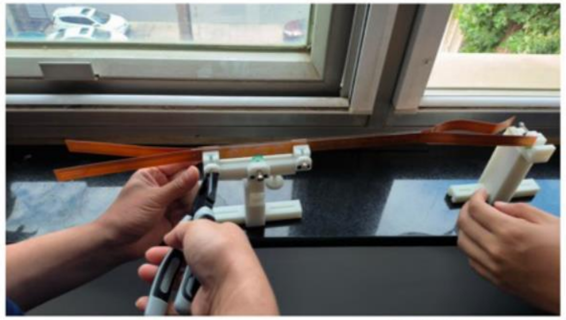


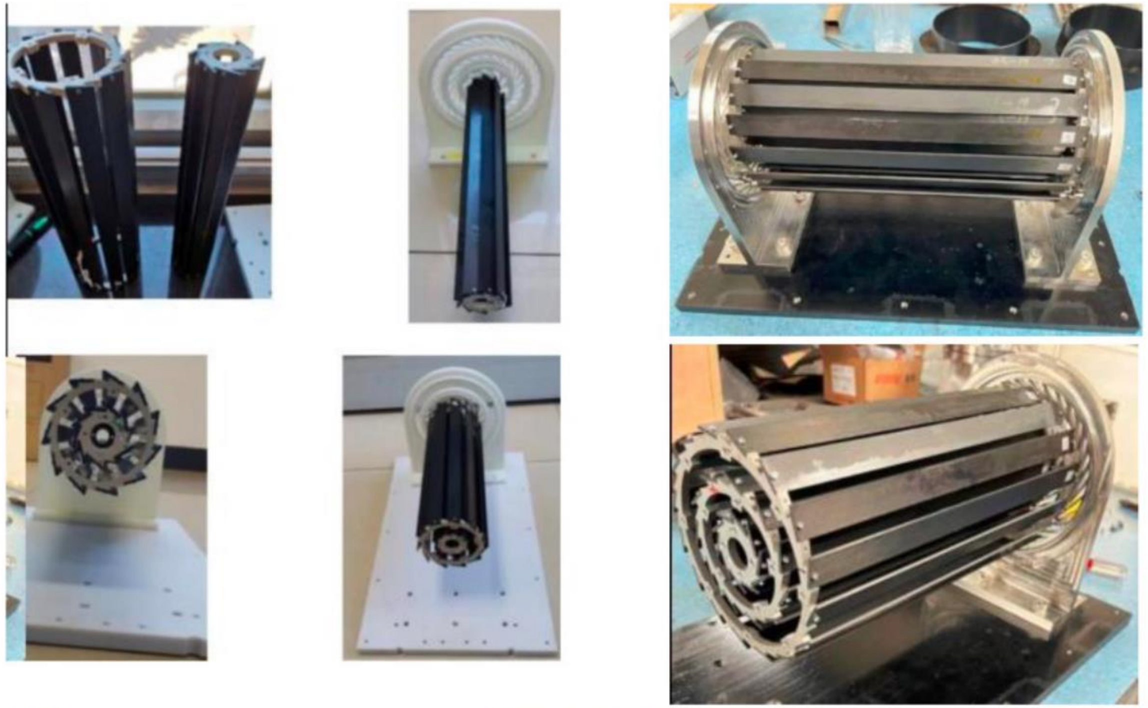
Dummy ladder glue automatic dispensing using gantry



Ladder on wire bonding machine

Dummy Ladder on holder





The first vertex detector (prototype) ever built in China

Ladder support tools

Ladder loaded on vertex detector

Vertex Requirement

- 1st priority: Small inner radius, close to beam pipe (11mm)
- 2nd priority: Low material budget <0.15% X0 per layer
- 3rd priority: High resolution pixel sensor： 3~5 μm