STCF 超级陶粲装置 Super Tau-Charm Facility

STCF硅像素内径迹探测器研究进展

徐来林，秦家军代表ITKM工作组

中国科学技术大学

超级陶粲装置研讨会•西安

2026.07.01

目录

- 研究背景
- STCF MAPS芯片设计
- STCF MAPS芯片测试
- 模块和机械设计
- 总结

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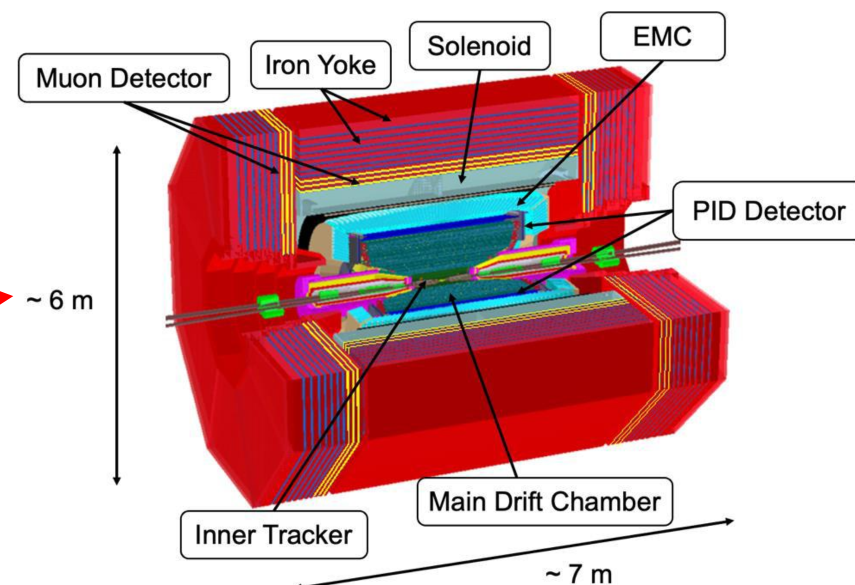
Super Tau-Charm Facility

- 超级陶粲装置(**Super Tau-Charm Facility , STCF**)
  - 国内新一代正负电子对撞机
  - 质心能量 2~7 GeV，亮度>0.5×10^{35} $cm^{-2}s^{-1}$@4 GeV
  - 具备进一步提升峰值亮度和实现束流极化的潜力



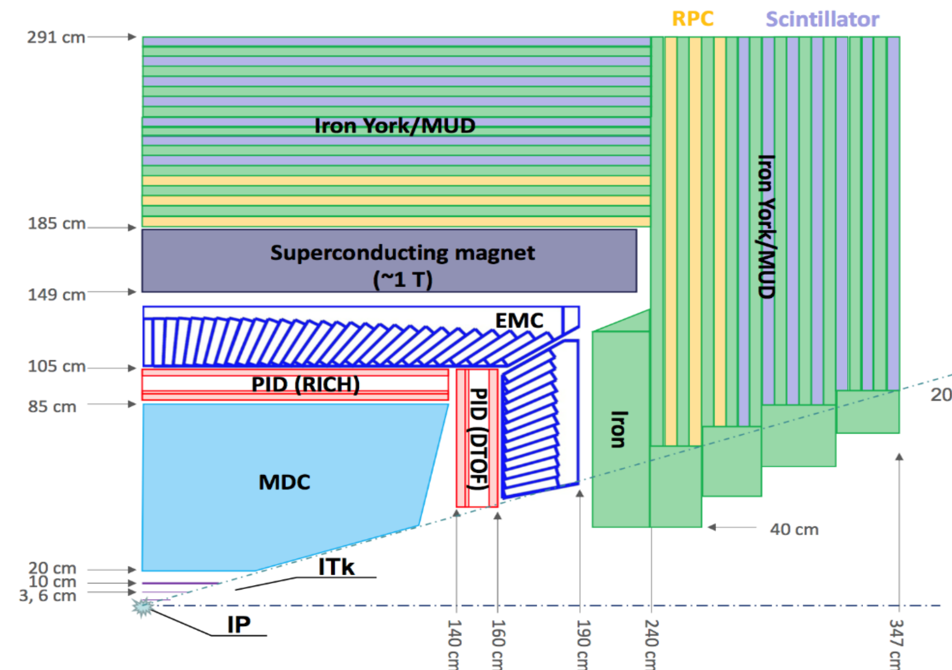
STCF ITK物理需求

- STCF物理目标

Solid angle coverage: 93%·4π
(polar angle: 20°~160°)

Inner tracker(ITK)
- ~ 0.3%X_0/layer
- σ_{xy}<100 μm

Main drift chamber(MDC)
- σ_{xy} < 130 μm
- σ_p/p~ 0.5% @ 1GeV
- dE/dx ~ 6%



Front. Phys. 19, 14701 (2024)

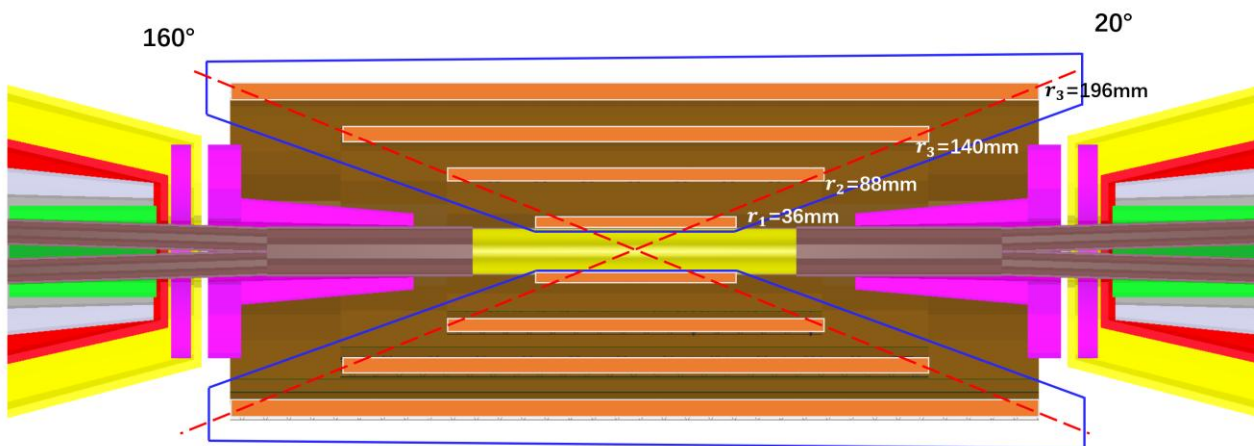
Process	Physics Interest	Optimized Sub-detector	Requirements
$\tau \to K_s \pi \nu_\tau$,	CPV in τ sector,		acceptance: 93% of 4π; trk. effi.:
$J/\psi \to \Lambda\bar{\Lambda}$,	CPV in hyperon sector,	Tracker	> 99% at p_T > 0.3 GeV/c; > 90% at p_T = 0.1 GeV/c
$D_{(s)}$ tag	Charm physics		$\sigma_p/p = 0.5\%$, $\sigma_{\gamma\phi} = 130\ \mu$m at 1 GeV/c

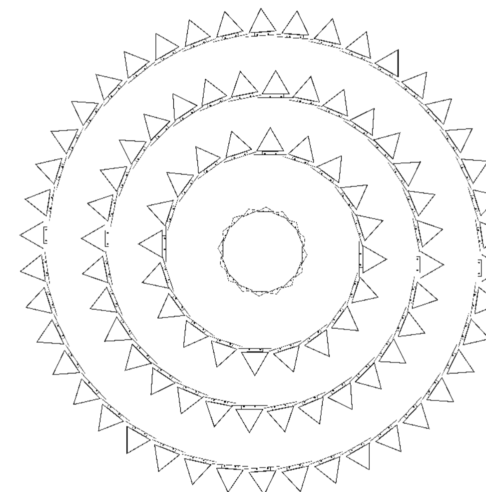
- 低动量能区粒子径迹探测的挑战
  - ◇ 多次库伦散射，径迹探测效率低
  - ◇ 如：BESIII的径迹重建效率在100MeV迅速降低

小收集极MAPS是STCF ITK的候选方案之一

- 低物质量是Inner Tracker的必要条件

STCF ITKM设计





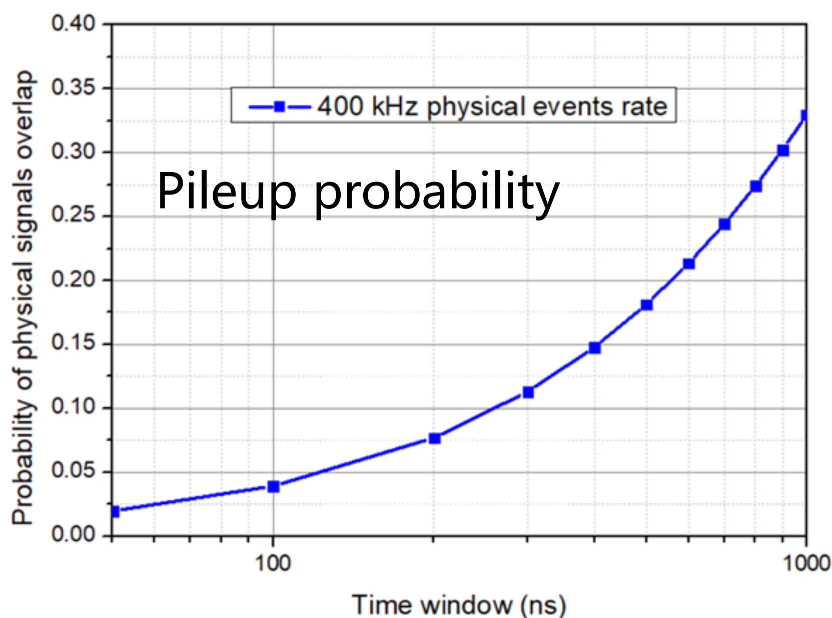
层数	半径 (mm)	长度 (mm)	Stave数	Stave上芯片数	面积 (cm^2)
1	36	250	12	12	576
2	88	510	15	50	3000
3	140	800	24	78	7488
4	196	1100	32	108	13824

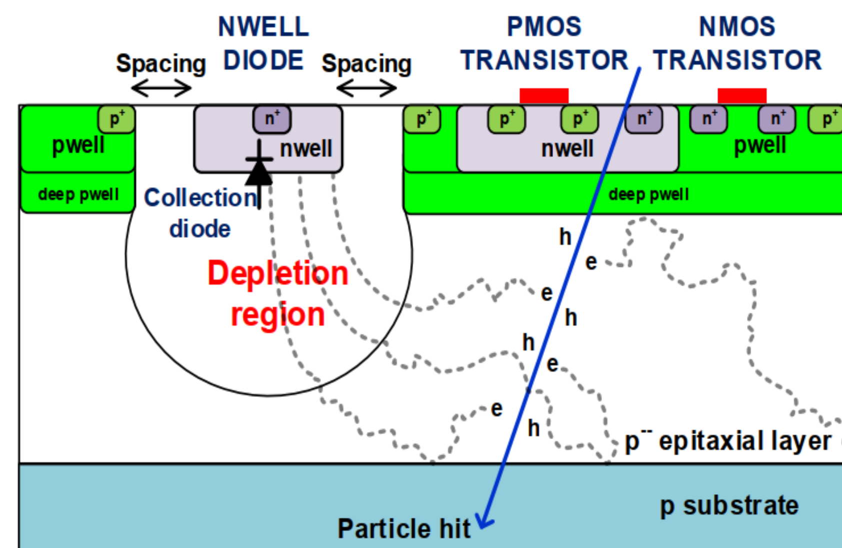
❖探测器结构设计
- 四层探测器
- 接收角度范围为20° ~160°
- ~6200 chips
- 总面积：~2.5 m^2

STCF MAPS设计目标

- MAPS设计需求
  - 位置分辨： ≤ 100 μm
  - 物质量：单层 ≤ 0.3% X_0
  - 功耗： ~ 50 mW/cm^2
  - 时间分辨： ≤ 50 ns -> ≤ 20 ns（去堆积）
  - 能量测量（ToT）
    - time walk修正、多次散射修正

	Requirements
Hit position resolution	$<100\,\mu m$
Hit time resolution	$\sim 20\,ns$
Power consumption	$\sim 50\,mW/cm^2$
Material budget	$\sim 0.3\%\ X_0$ per layer
Hit rate	$>1\,MHz/cm^2$
TID	$>1.0\,Mrad/year$
NIEL	$>1.0\times10^{11}\ 1\,MeV\ n_{eq}/cm^2/year$





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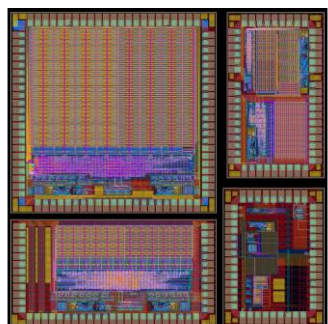
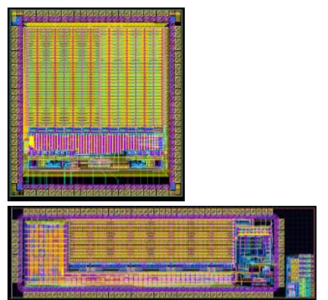
MAPS原型芯片总览

TJ180nm	GSMC130nm	BCIS90nm	IRAY180nm
国外成熟工艺	国内工艺	国内工艺	国内工艺
低阻衬底+高阻外延（>1kΩ·cm）	高阻衬底	低阻外延 (<10Ω·cm)	高阻外延层
四阱工艺	四阱工艺	三阱	四阱工艺、N-blanket

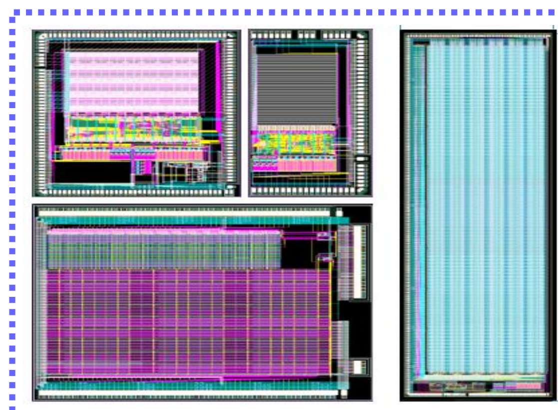


CharTPix-TJ-v0.1
2024.12回片

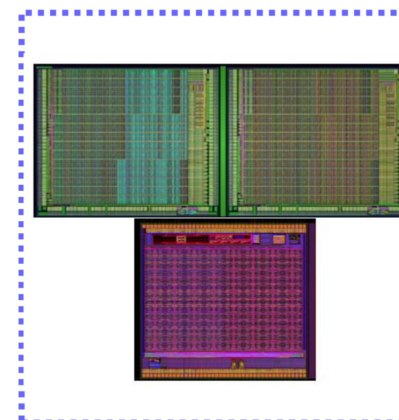


CharTPix-TJ-v0.2
预计2026年7月回片

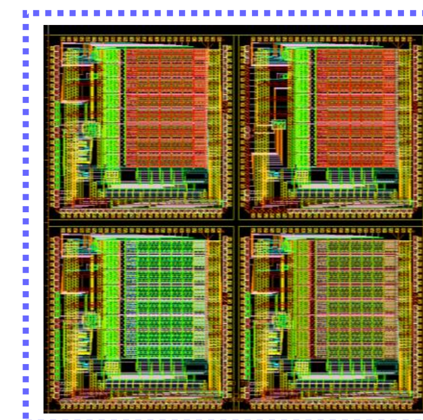
CharTPix-GSMC-v0.1
2025.6回片



CharTPix-BCIS-v0.1
2025.1提交流片
2025.6回片



CharTPix-IRAY-v0.1
2025.9回片



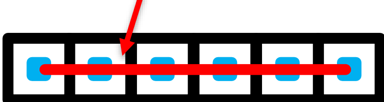
Zhang R Y, et al. Simulation of MAPS and a MAPS-based inner tracker for the Super Tau-Charm Facility. NIMA, 2026, https://doi.org/10.1016/j.nima.2026.171383.

CharTPix-TJ

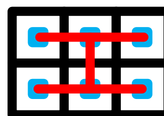
- Sensor尺寸考虑
  - 位置分辨要求不高→选择较大尺寸像素，减少读出电路规模，进而降低功耗
  - 尝试、比较多种规格的sensor设计

diode　　metal

A: pixel
30μm×30μm



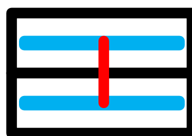
B: Pixel-based
180μm×30μm



C: Pixel-based
90μm×60μm

金属线连接:小输入电容

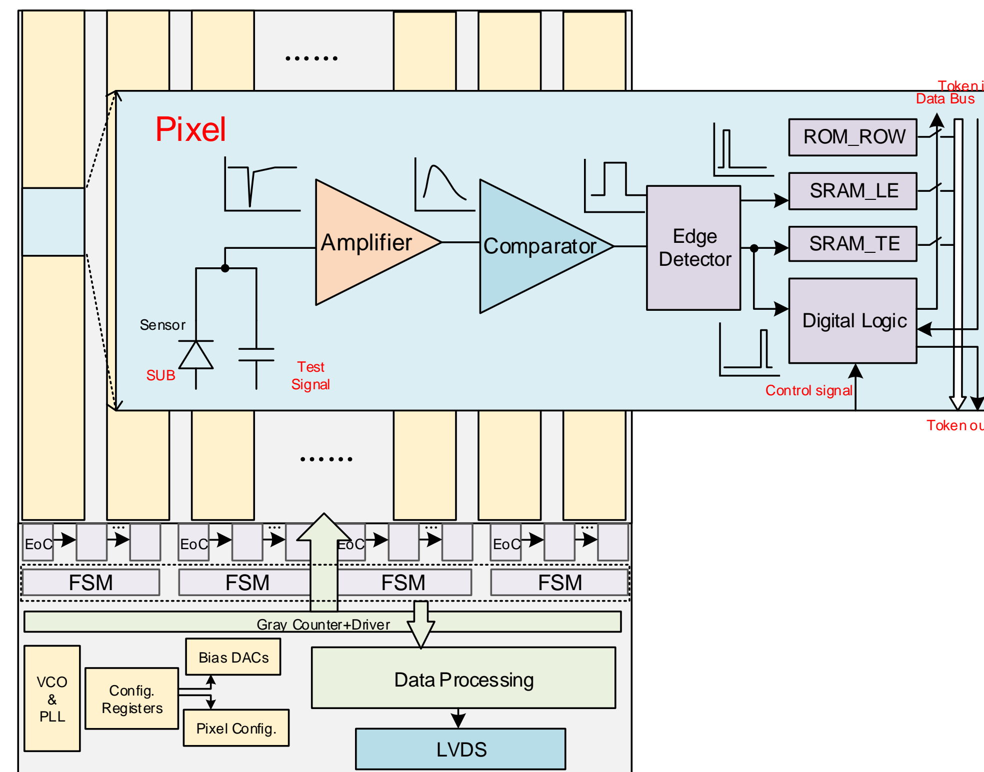
D: Strip-based
180μm×30μm



E: Strip-based
90μm×60μm

有源区连接:更快的电荷收集速度

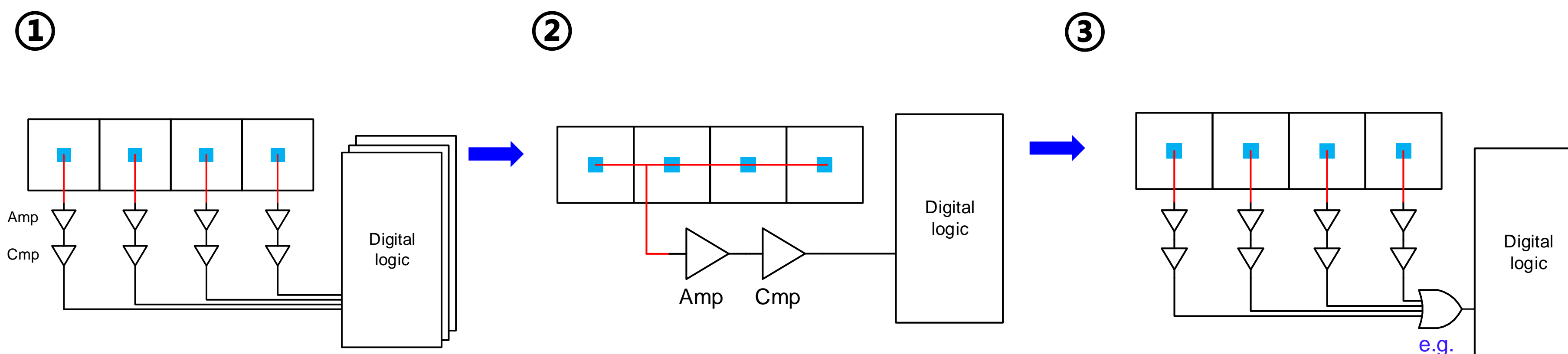
Xuan D W, et al. A low power monolithic active pixel sensor prototype for the STCF inner tracker[J]. NIMA, 2025, 1080: 170725. https://doi.org/10.1016/j.nima.2025.170725



- 像素内电路
  - 放大甄别，提取前后沿
  - 前后沿分别锁存时间戳
- 列级读出电路
  - 列优先级读出（Column-Drain）
- 外围电路

CharTPix-GSMC/TJ_v0.2

- 不增加功耗的前提下，高空间分辨/时间分辨可提供更多的可能
  - 提出基于超级像素的新型读出架构



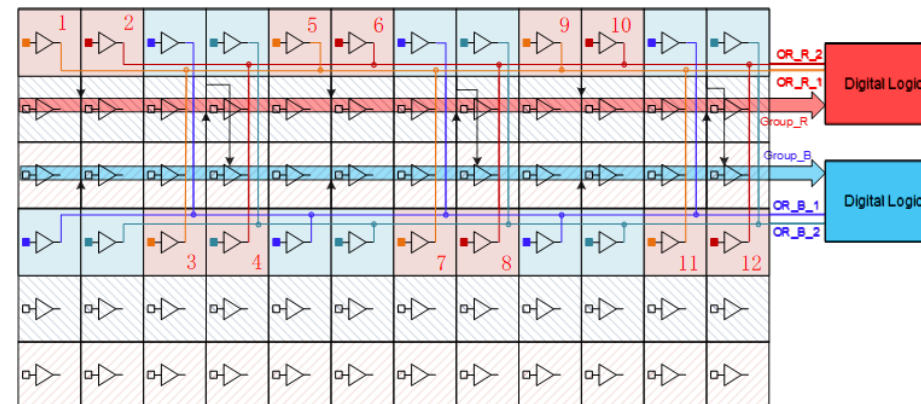
传统定时MAPS
- ✓ 小像素→定时快、噪声小
- ✓ 读出通道多→功耗高

TJ MAPS
- ✓ 大像素→定时较慢、噪声较高
- ✓ 读出通道少→功耗低

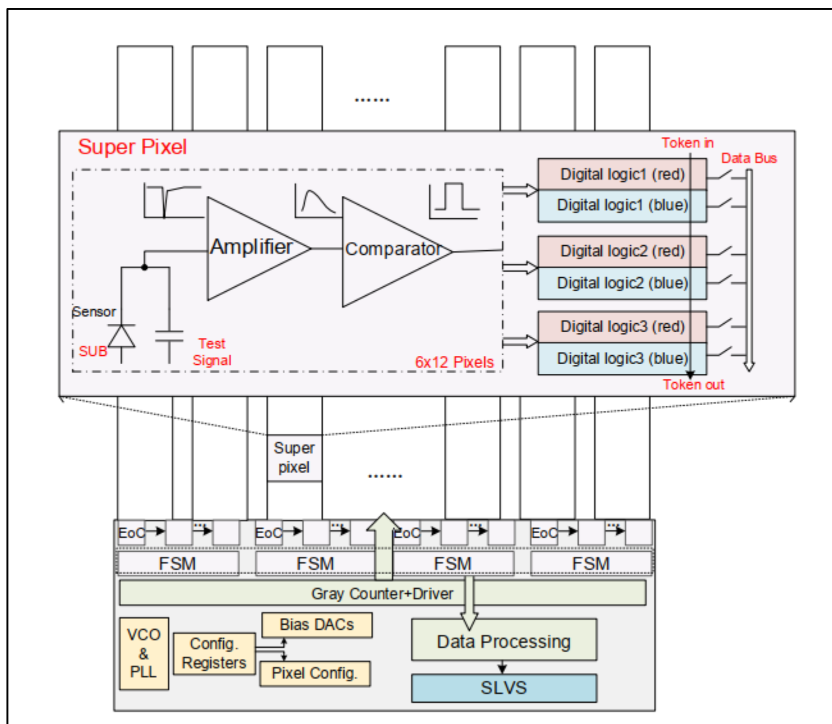
基于超级像素读出的MAPS
- ✓ 小像素→定时快、噪声小
- ✓ 读出通道少→数字功耗低

CharTPix-GSMC/TJ_v0.2

- Pixel Core：Layout可重复的最小阵列
  - Core size: 6×12 pixel
  - Cluster area小于3×4 pixel时，不损失pixel的信息



同时提供高精度位置分辨和高精度时间分辨



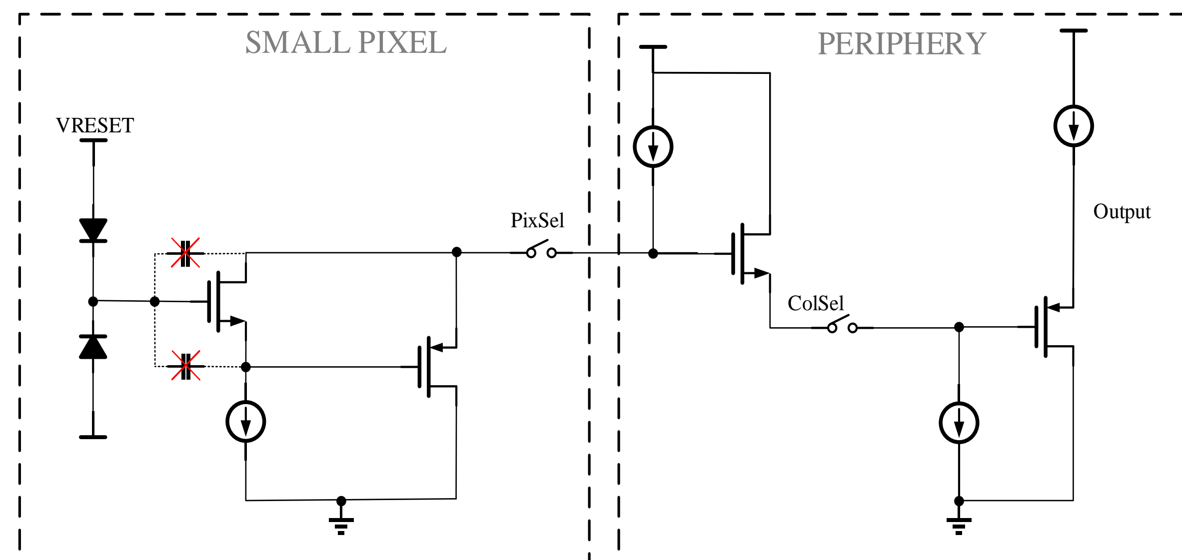
芯片参数	
工艺	GSMC 130 nm
芯片尺寸	6.1 mm×22.0 mm
像素阵列	576(行)×144(列)
像素尺寸	33.2 μm×33.2 μm
芯片功耗	44.5 mW
单像素功耗	150 nA/pix
ToA	13-bit (5-bit Fine+8-bit coarse)
ToT	8-bit

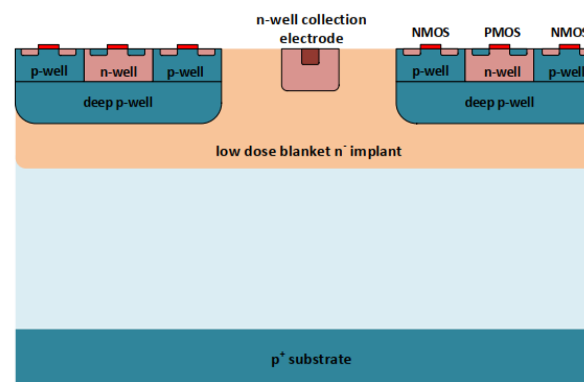
D. Xuan et al., "CMOS MAPS With a Novel Readout Scheme for High Luminosity Particle Colliders," in IEEE Transactions on Nuclear Science, vol. 72, no. 3, pp. 217-224, March 2025, doi: 10.1109/TNS.2024.3459082.

CharTPix-IRAY

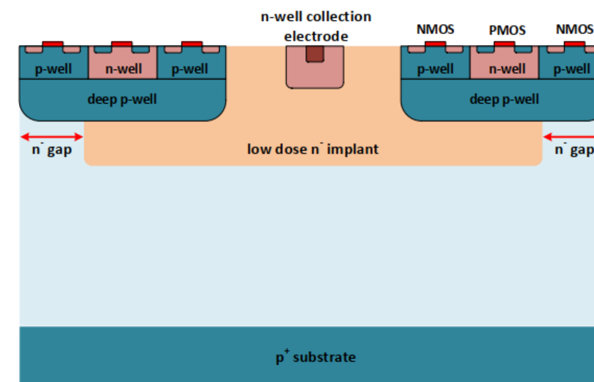
- CharTPix-IRAY：纯模拟读出，使用行选列选的方式读出一个像素子阵列
- 四种不同设计方案
  - 添加n型轻掺杂层，且使用多种像素间的间隙参数
  - 国内自主研发的Modified工艺，并在此基础上进行二次改进

	Chip1	Chip2	Chip3	Chip4
Process	Standard	Modified	N-gap (= 2.5 μm)	N-gap (= 4 μm)
n型层	×	√	√	√
间距	\	0	2.5 μm	4 μm





Modified



Modified with N-gap

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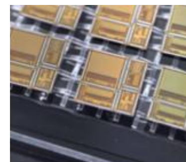
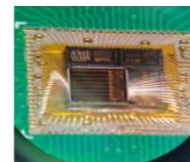
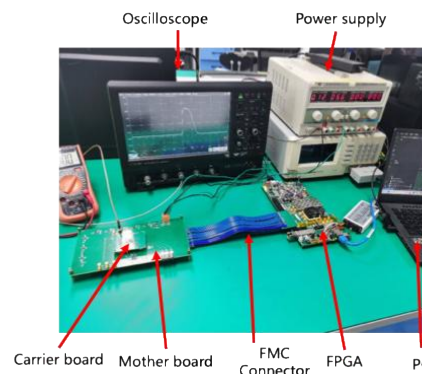
MAPS芯片测试

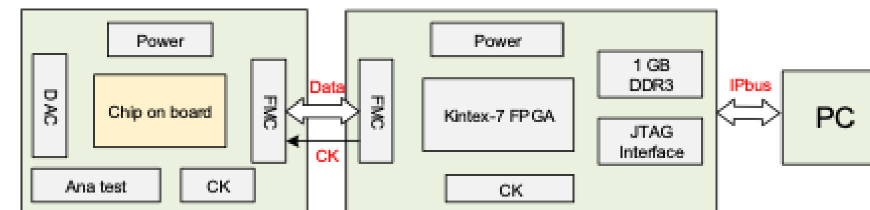
- CharTPix_TJ_v0.1:
  - Electronics test: Basic electrical performance testing
  - Laser test: Preliminary detection efficiency and position resolution testing
  - Fe55, Sr90 test: Characterize charge collection performance and calibrate the injection capacitance
- CharTPix_GSMC_v0.1
  - Electronics test
  - Fe55, Sr90 test
- CharTPix-IRAY-v0.1
  - Fe55 test
- Beam test: Evaluation of detection efficiency and position resolution
  - CharTPix_TJ_v0.1
  - CharTPix_GSMC_v0.1


CharTPix-TJ-v0.1 chips

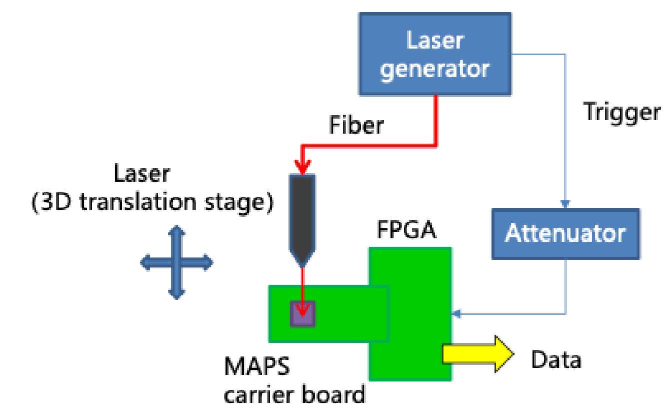

After wire bonding

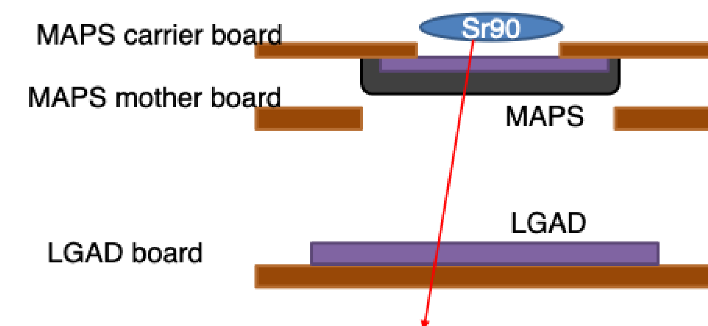
Carrier board





Test system block diagram





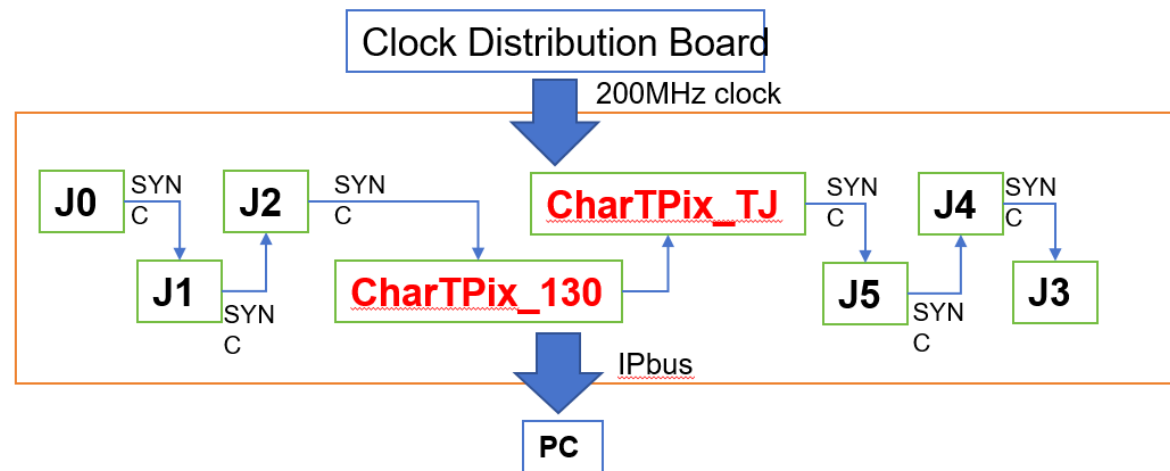
CERN束流测试

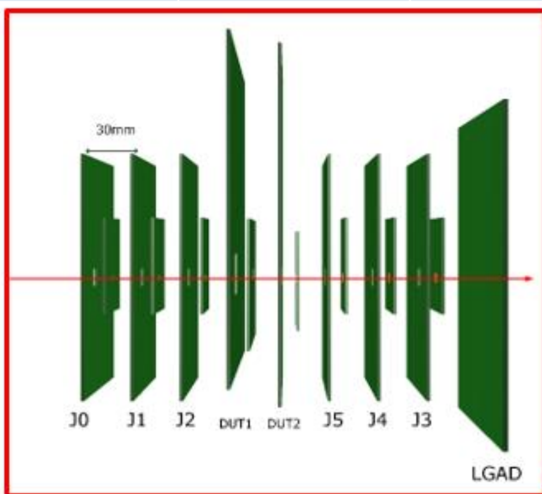
- CERN PS(Proton Synchrotron)

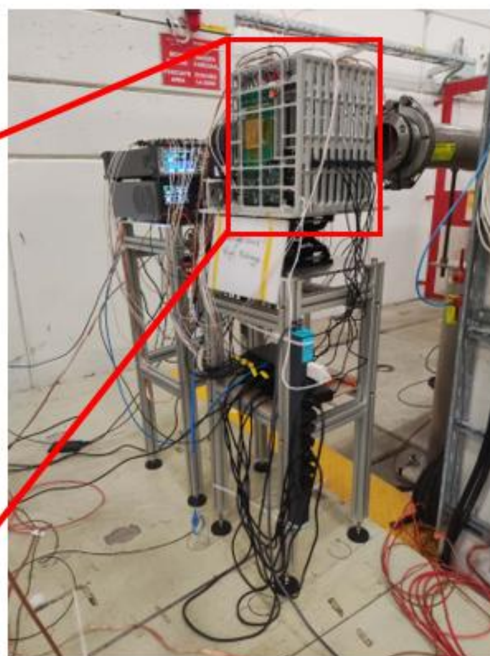
束流望远镜：

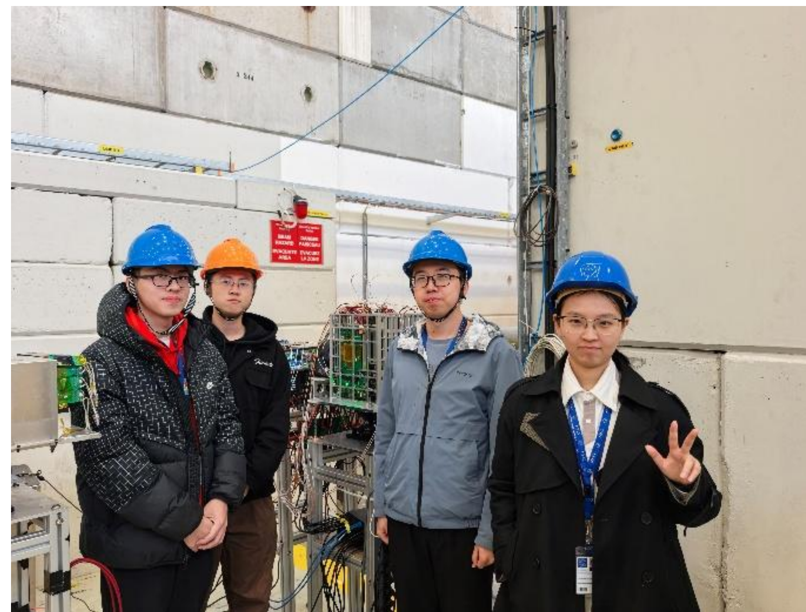
- 6层Jadepix-3芯片作为径迹参考探测器（J0-J6）
- 1层LGAD作为时间参考探测器
- 2层DUT：CharTPix-TJ和CharTPix-GSMC

束流种类	束流动量	事例数
muon	10GeV/c	~50w
e+	1-3.5GeV/c	~20w
强子	10GeV/c	~300w
	4GeV/c	~200w
	其它	~100w



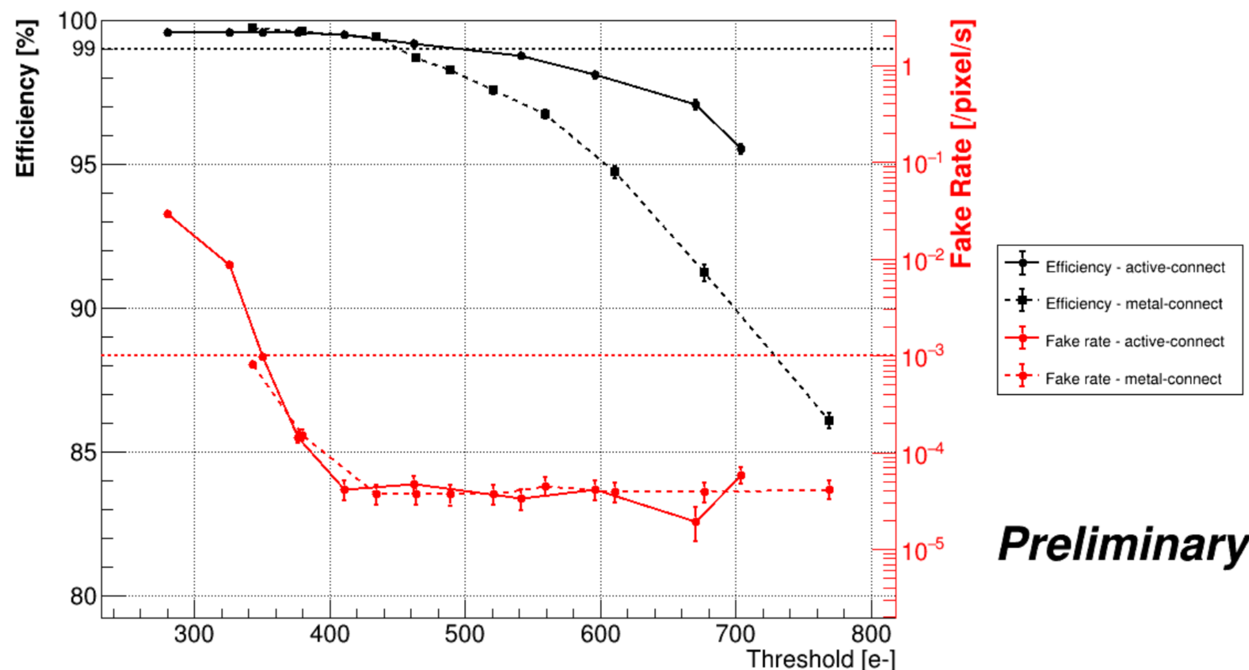


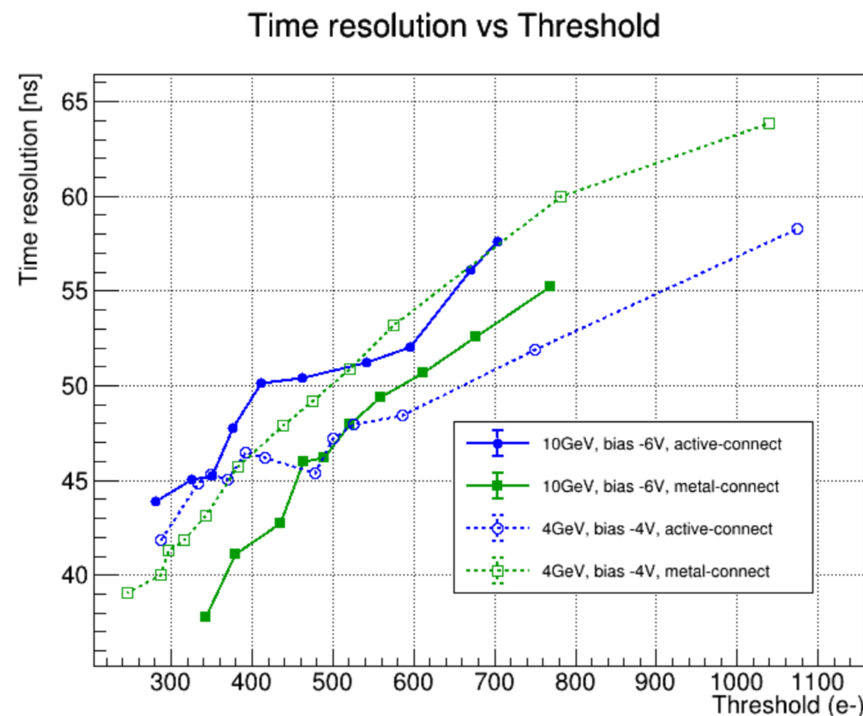




束流测试结果分析-CharTPix-TJ-v0.1

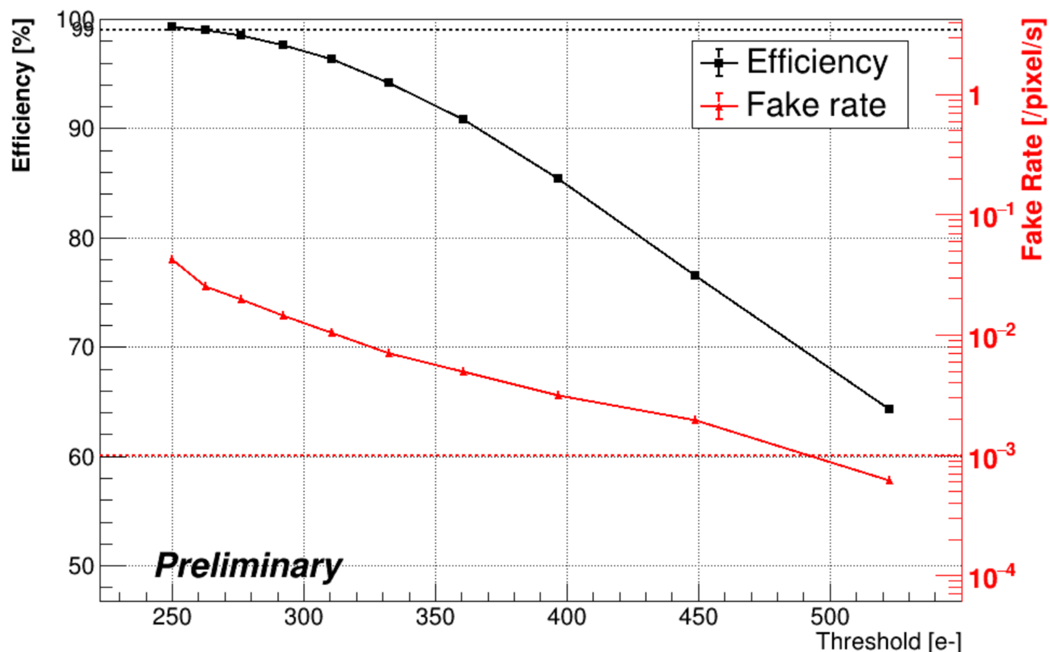
- CharTPix-TJ的误触发率在4e-4/pixel/s水平，与ALPIDE相当，在要求误触发率小于1e-3/pixel/s、效率大于99%情况下有100-200e的调节空间
- 时间测量精度低阈值下好于50 ns





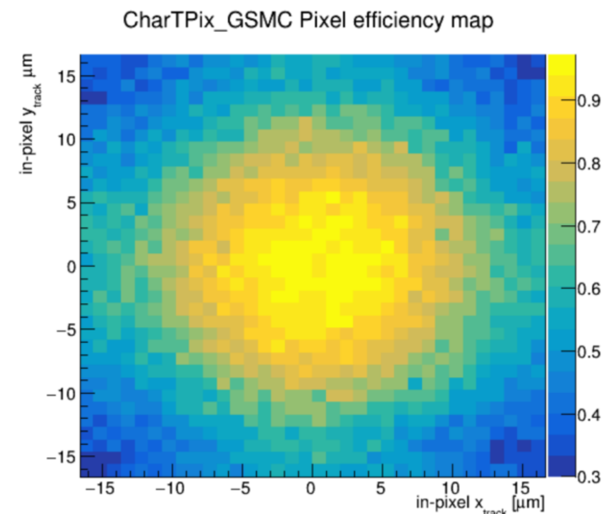
束流测试结果分析-CharTPix-GSMC-v0.1

CharTPix-GSMC误触发率，比TJ工艺高出1-2个量级

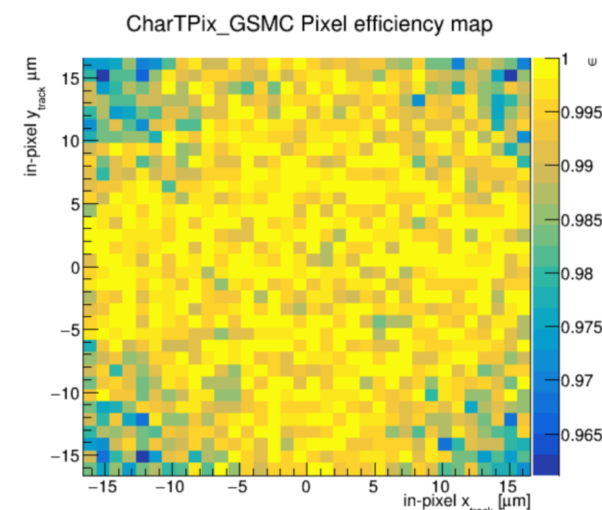


CharTPix-GSMC

阈值523e
（最高）

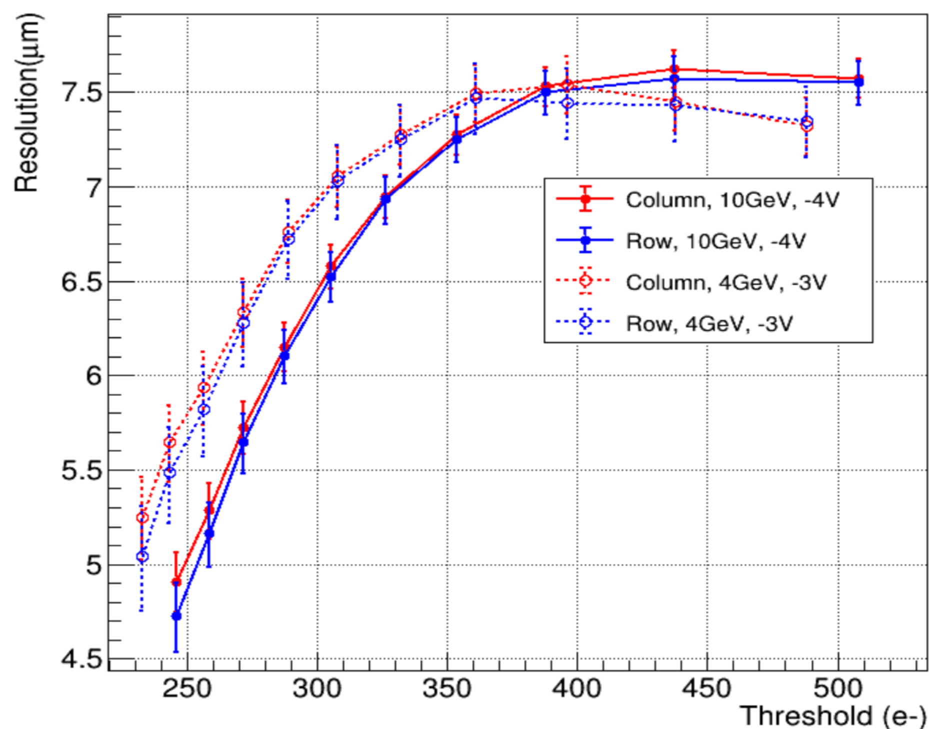


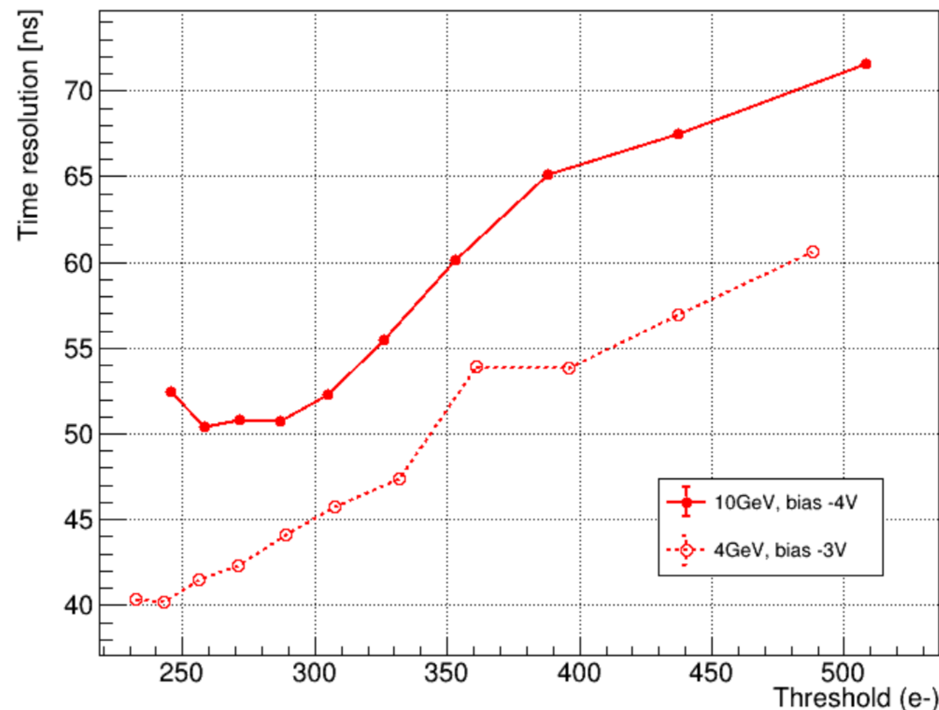
阈值250e
（最低）



效率

束流初步分析-CharTPix-GSMC-v0.1





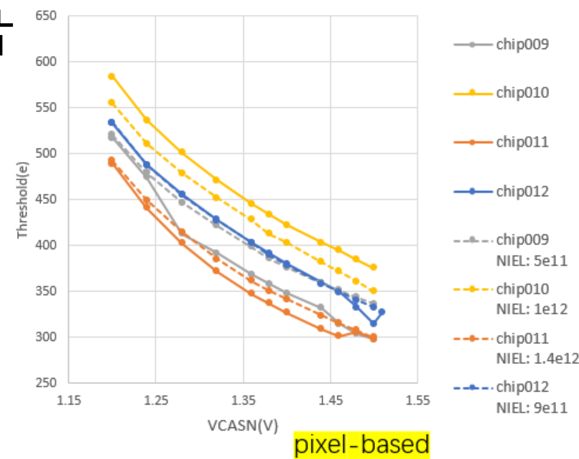
- 在250e阈值下能达到5 μm的空间分辨
- 在250e阈值@SUB = -4 V下时间分辨约为50 ns

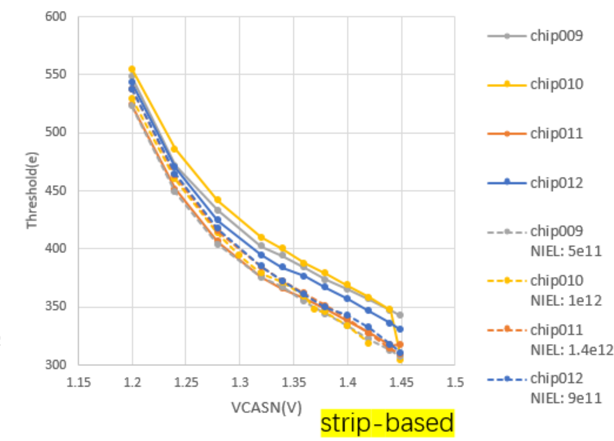
NIEL辐照测试

在散裂中子源（CSNS）反角白光中子谱仪上照射芯片

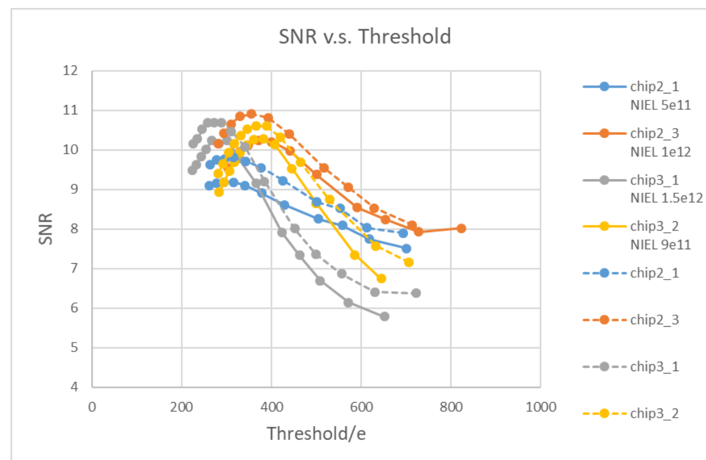
- TJ, IRAY, GSMC三种芯片为一组进行测试
- 每种工艺四块芯片照射4种不同剂量

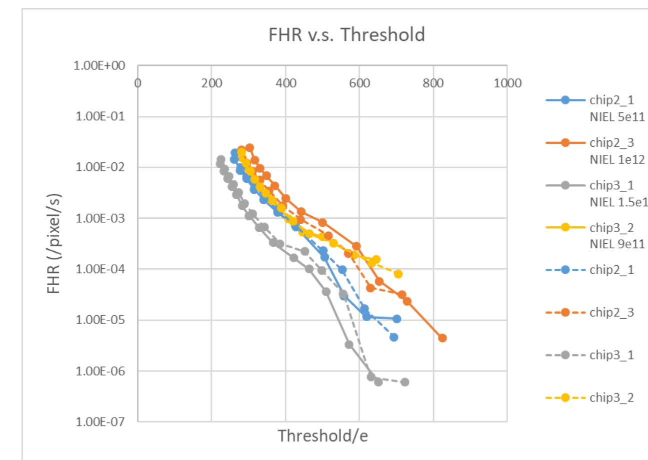
	测试时间(h)	NIEL剂量(1MeV ne	TID剂量(Gy)
低剂量	8.00E+00	**5.07E+11**	9.93E-01
中剂量1	1.60E+01	**1.01E+12**	1.99E+00
中剂量2	1.38E+01	**8.74E+11**	1.71E+00
高剂量	2.18E+01	**1.38E+12**	2.71E+00





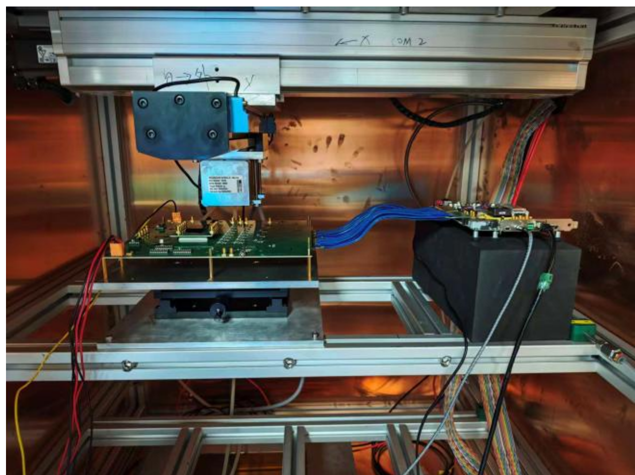
TJ MAPS: • 辐照前后阈值、Mismatch、热噪声、漏电流无明显差异





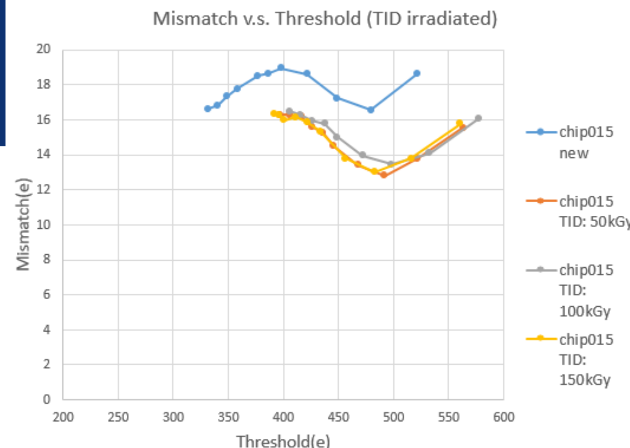
GSMC MAPS:
- 阈值没有明显差异，TN和Mismatch略有增大
- 热像素数量、误触发率无明显增高；漏电流无明显变化

TID辐照测试

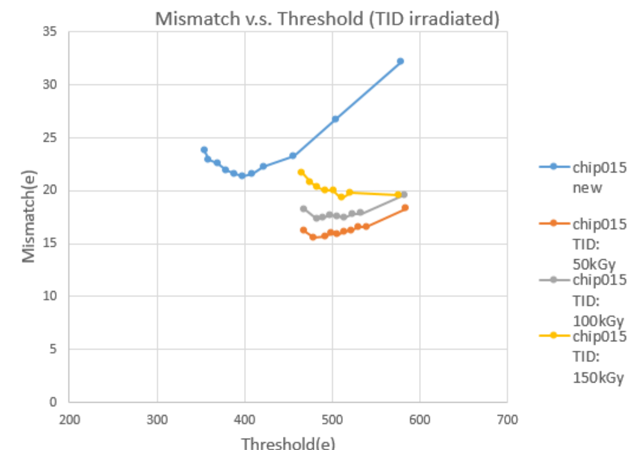


TJ MAPS

Mismatch

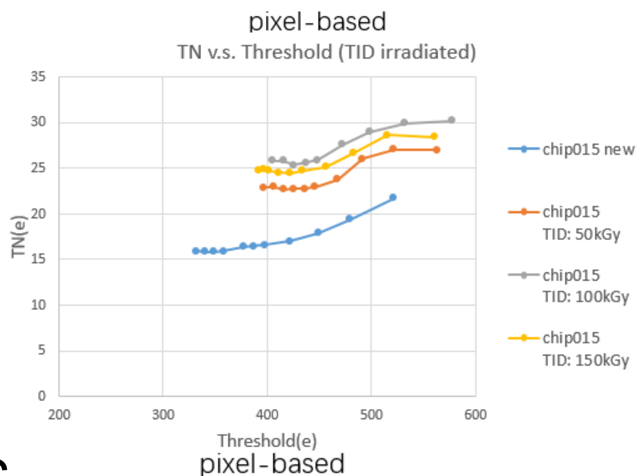


pixel-based

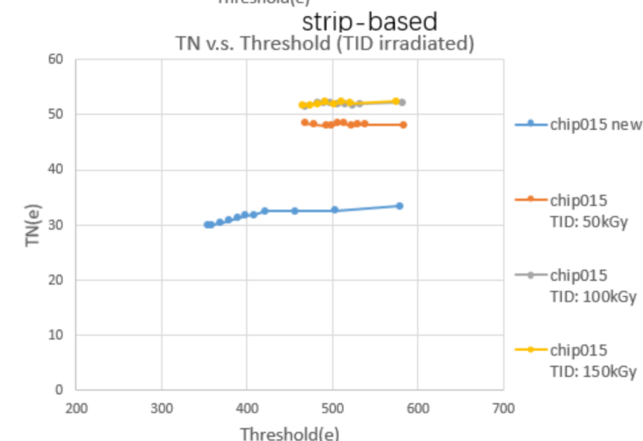


strip-based

Thermal Noise



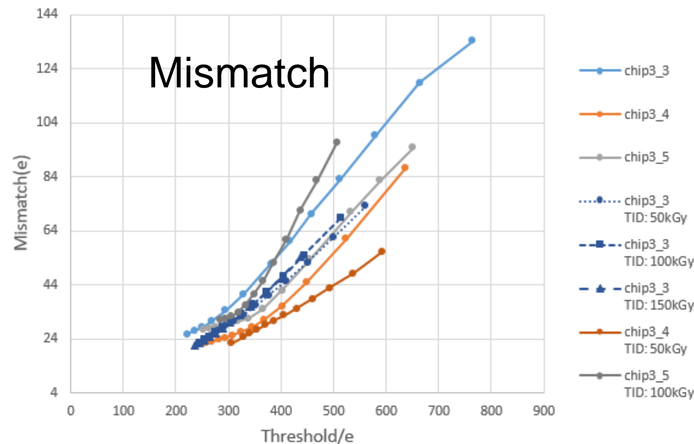
pixel-based

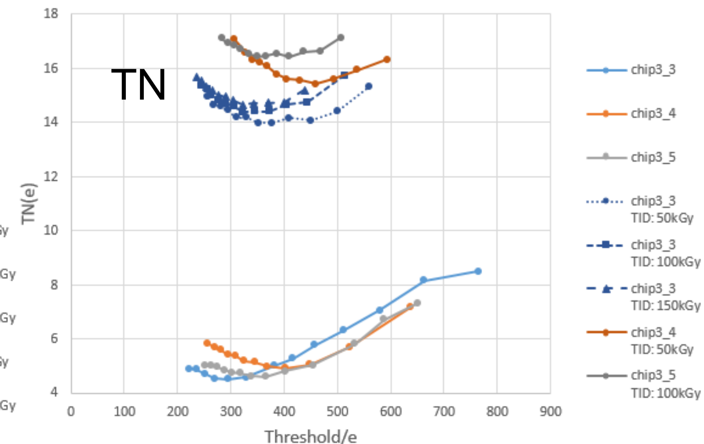


strip-based

- 利用X光机进行辐照
- 辐照剂量：50 kGy, 100 kGy 和150 kGy
- 对比辐照前后的主要性能

GSMC MAPS

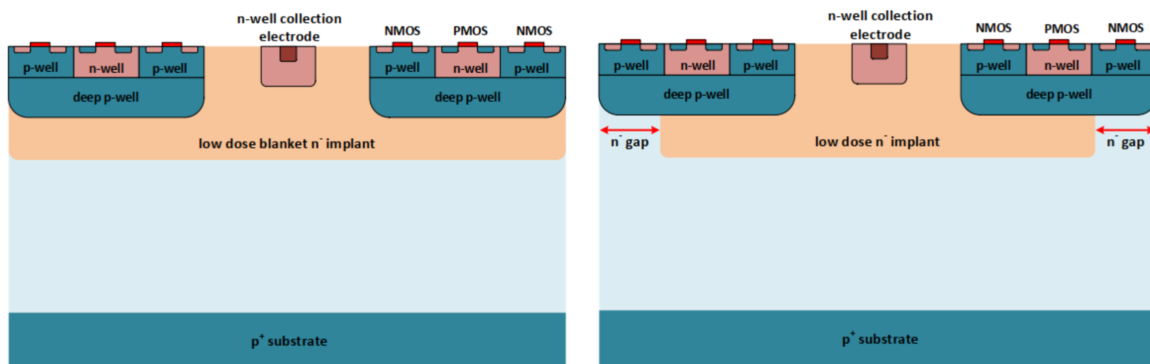


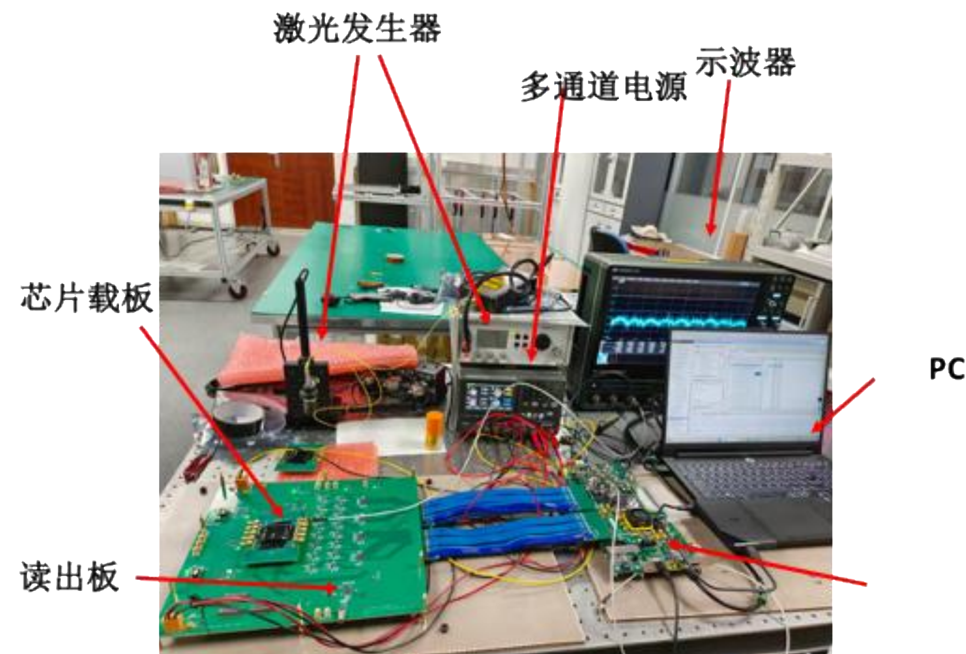


TID辐照后的芯片性能有较大变化，主要表现为TN增大，误触发率增大，mismatch有所减小

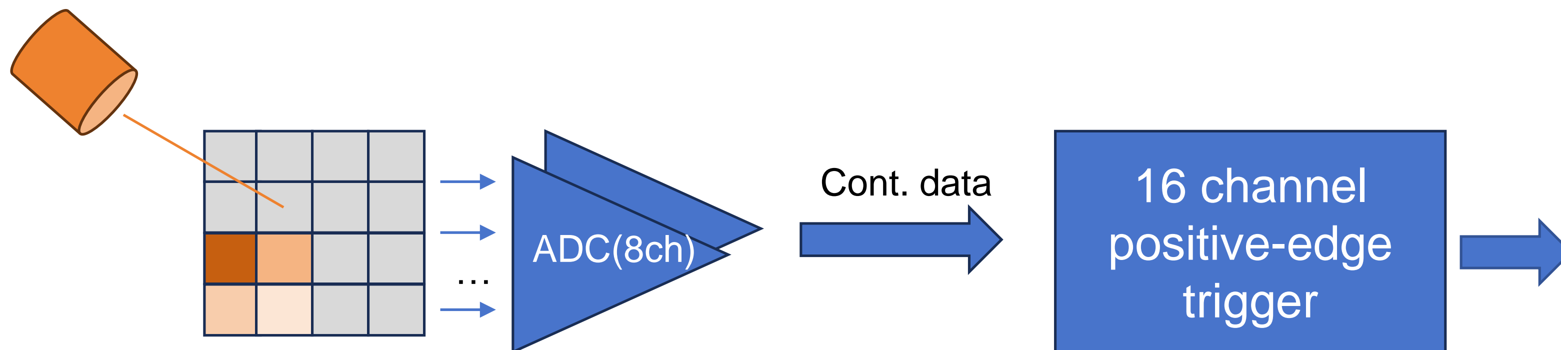
目前正在CERN进行辐照后的束流实验

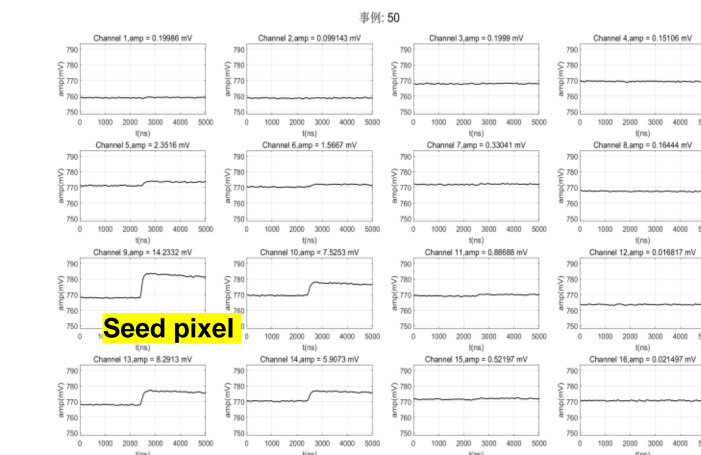
CharTPix-IRAY-v0.1





	Chip1	Chip2	Chip3	Chip4
Process	Standard	Modified	N-gap (= 2.5 μm)	N-gap (= 4 μm)

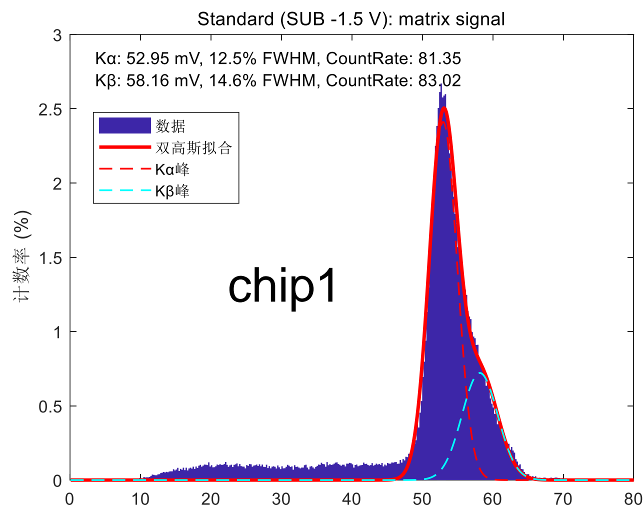


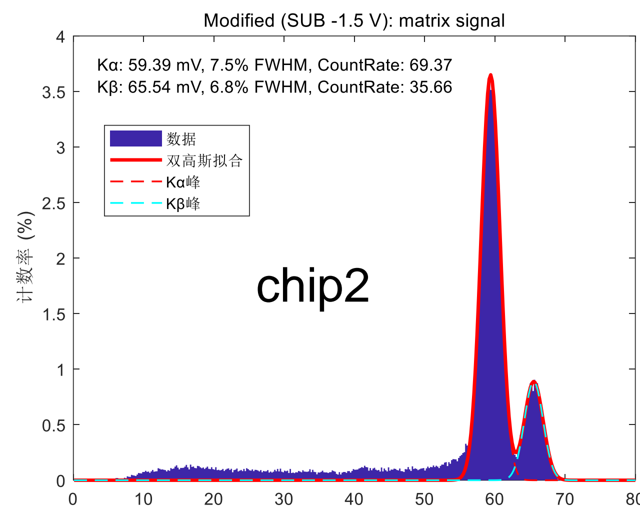


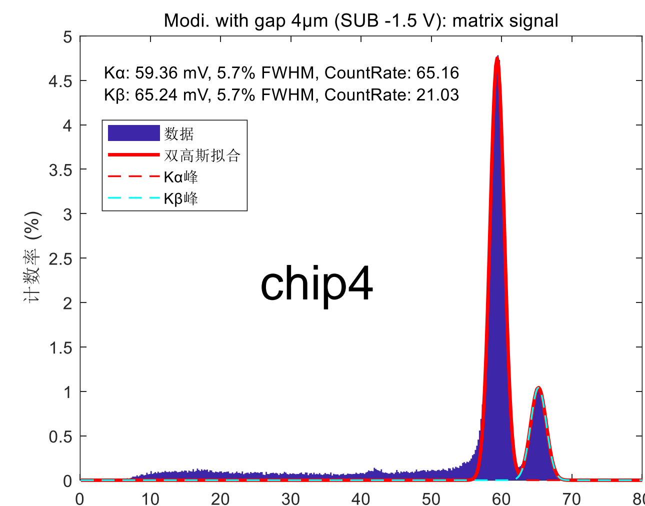
CharTPix-IRAY-v0.1：^{55}Fe放射源测试

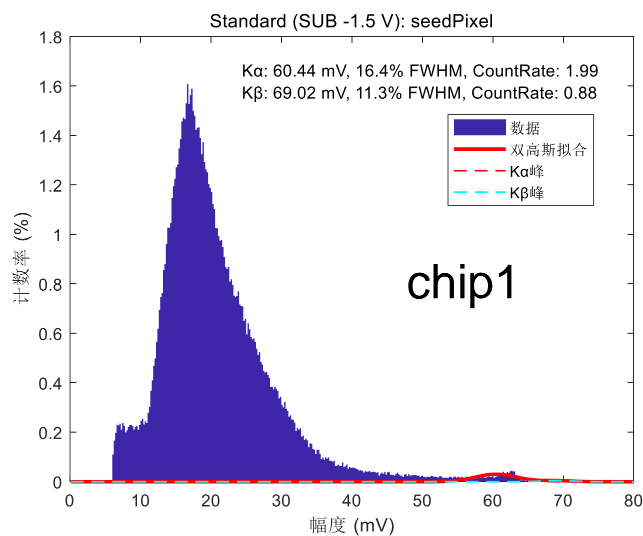
- 全阵列测试均能看见Kα全能峰，具备电荷全收集能力
- modified with gap的seed能谱收集峰位置为Kα峰处，耗尽区增大，大部分事例被单像素全收集

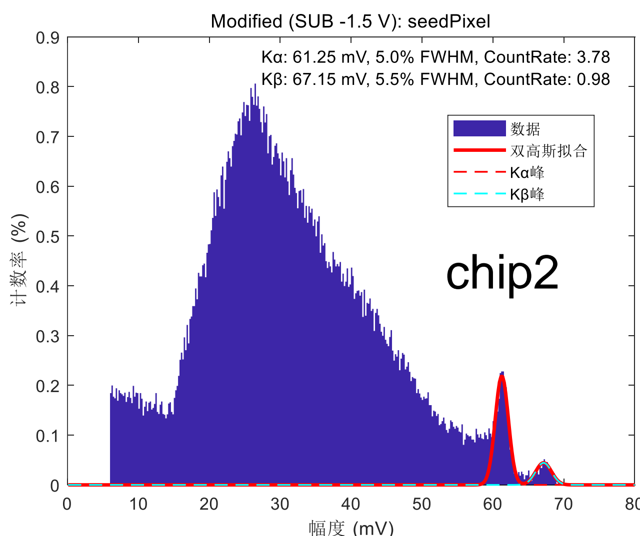
	Chip1	Chip2	Chip3	Chip4
Process	Standard	Modified	N-gap (= 2.5 μm)	N-gap (= 4 μm)

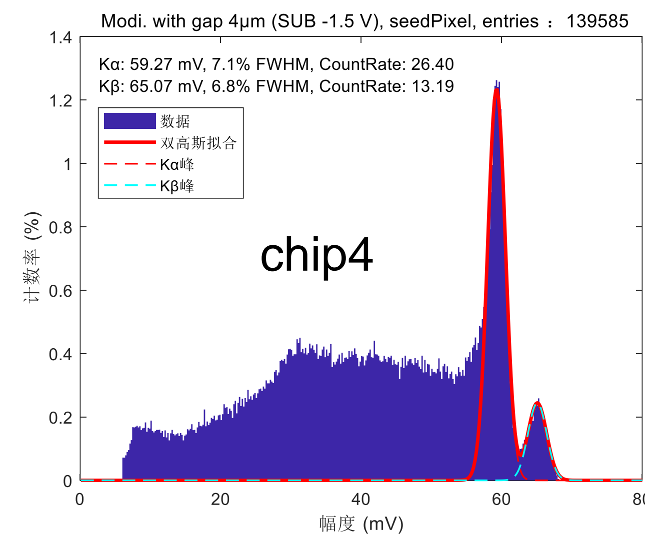








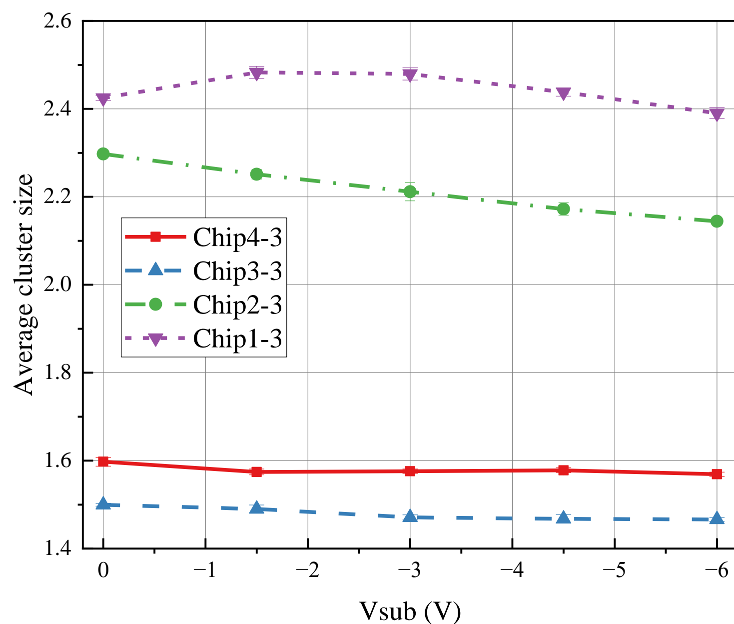


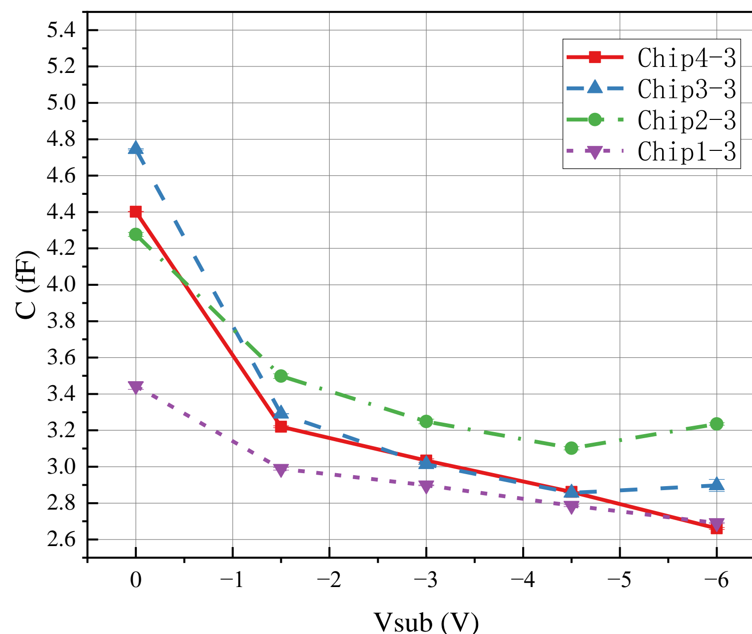


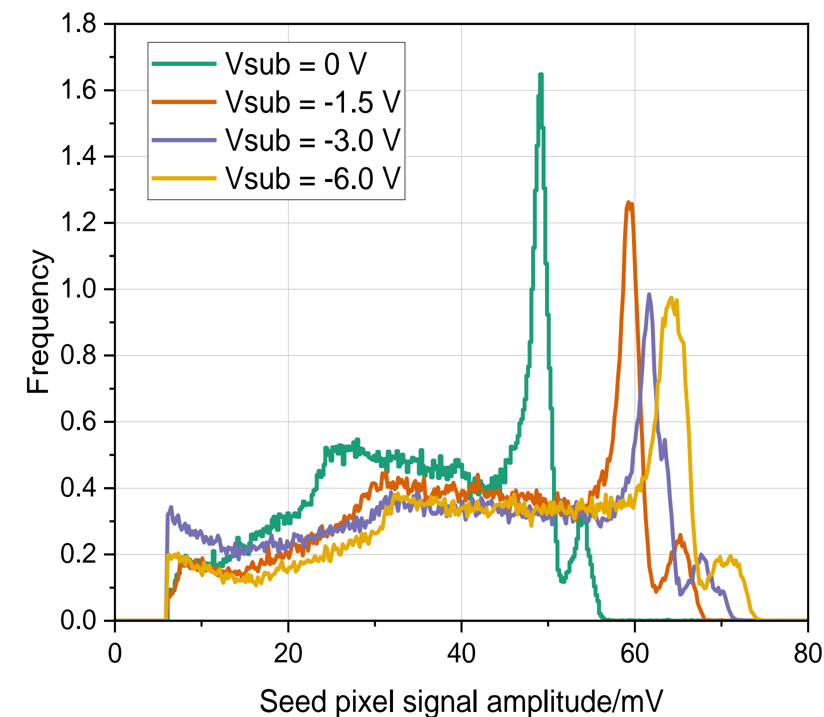
CharTPix-IRAY-v0.1

- average cluster size从大到小依次为：1→2→4→3
- 随着负偏压增大，校准峰的位置向右移动，表明sensor电容逐渐减小

	Chip1	Chip2	Chip3	Chip4
Process	Standard	Modified	N-gap (= 2.5 μm)	N-gap (= 4 μm)







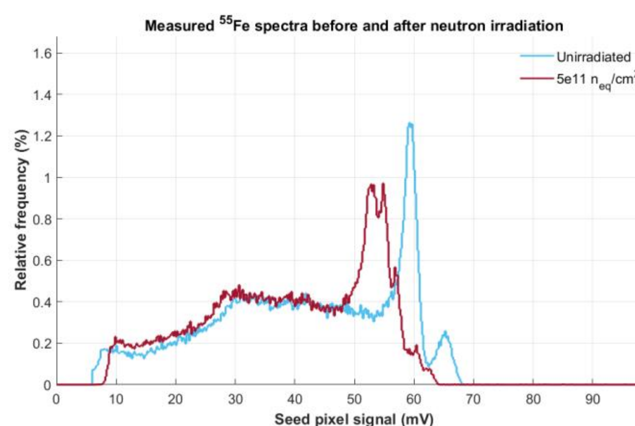
CharTPix-IRAY-v0.1：辐照测试

中国散裂中子源（CSNS）反角白光谱仪 -- NIEL

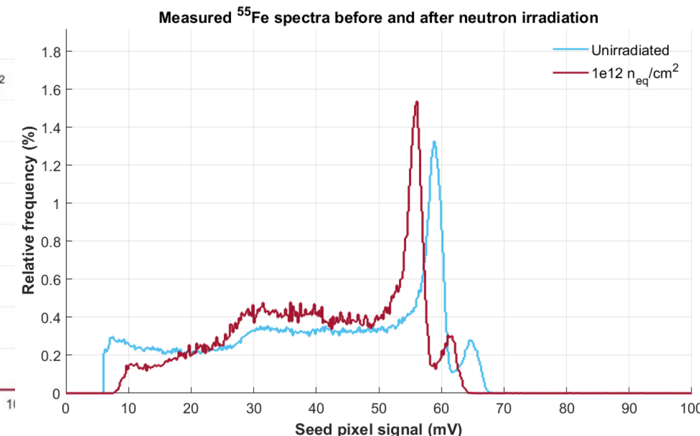
芯片	剂量
Chip1-3	9e11/cm^2
Chip4-3	5e11/cm^2
Chip4-4	1e12/cm^2
Chip4-5	1.4e12/cm^2

辐照后

- Seed pixel校准峰分裂：像素间不一致性增大
- 校准峰位置左移：Sensor电容增大



Chip4-3



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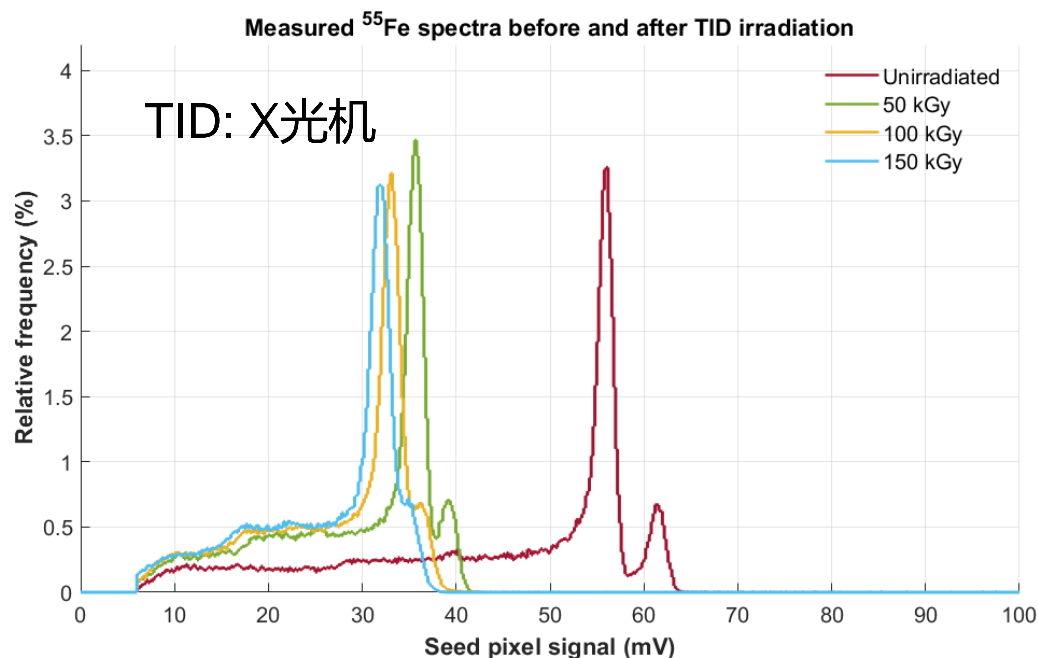
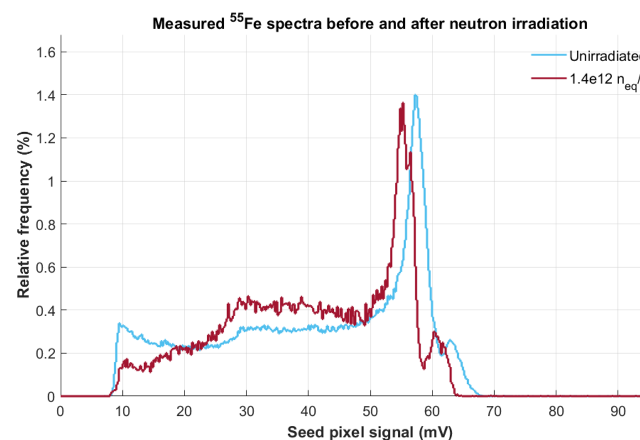
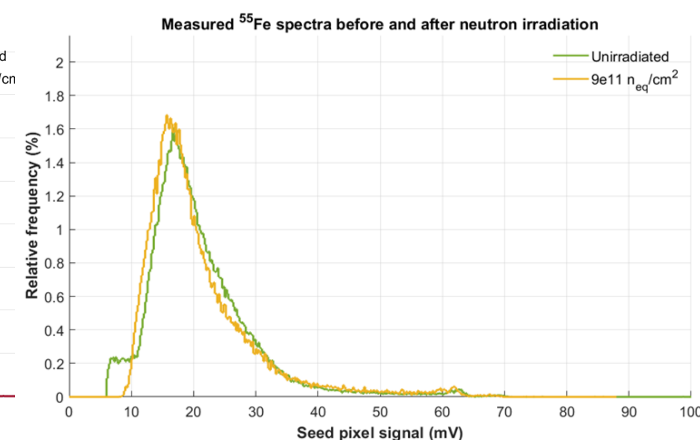




Chip4-5



Chip1-3

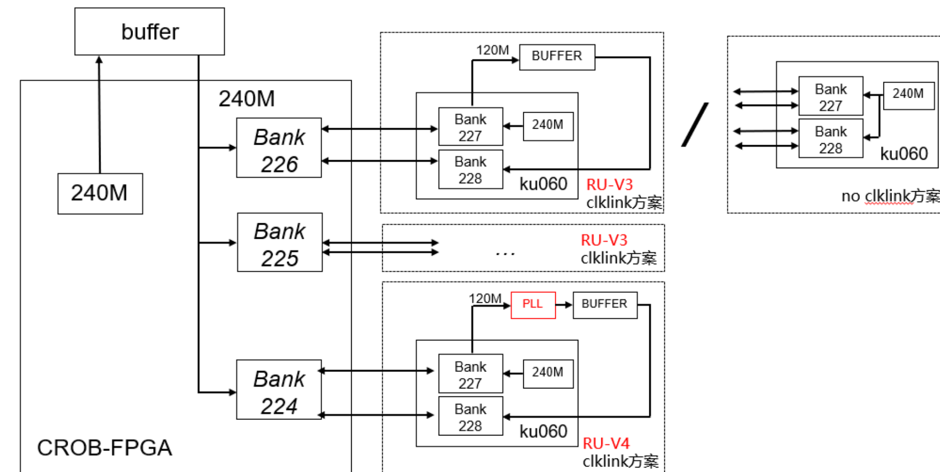
MAPS读出电子学

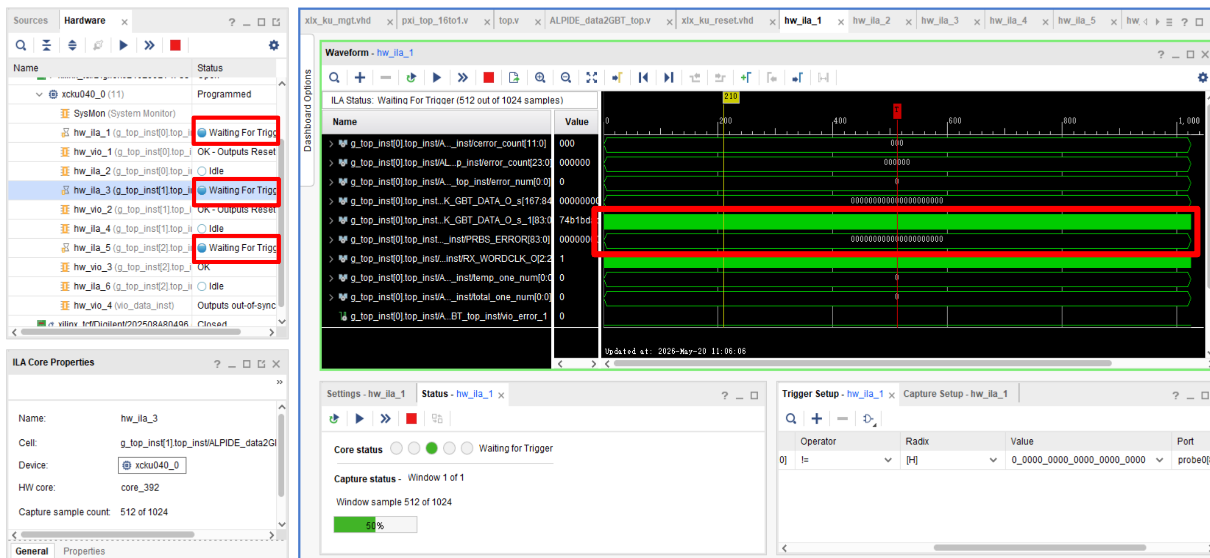
构建了MAPS载板→读出模块（RU）→ DAQ CROB链路

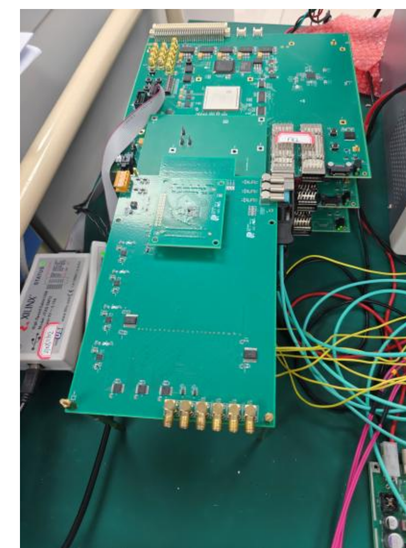
- 数据链路稳定建立连接，上行数据正确传输
- 下行配置功能正常

多通道汇总测试

- 使用一个CROB汇聚三块RU数据
- 能实现3个RU双向稳定传输
- 在27小时无误码，BER<1E-14，置信度99%







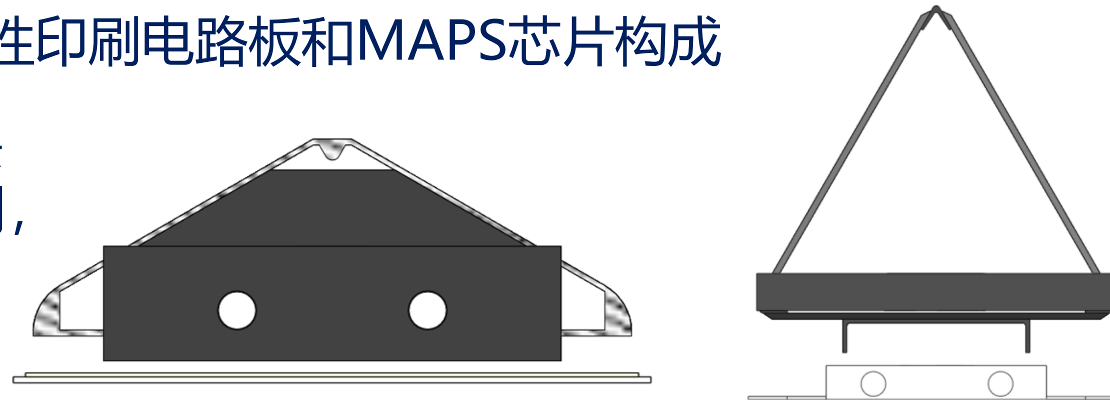
目录

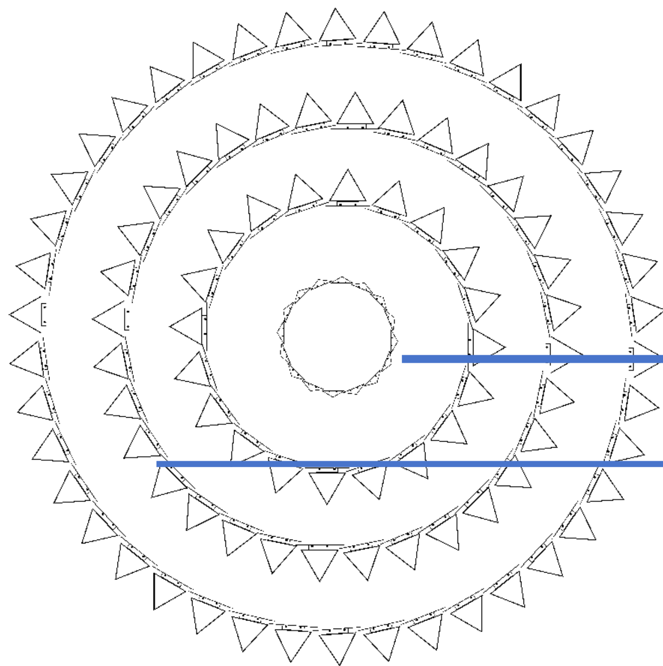
- 研究背景
- STCF MAPS芯片设计
- STCF MAPS芯片测试
- 模块和机械设计
- 总结

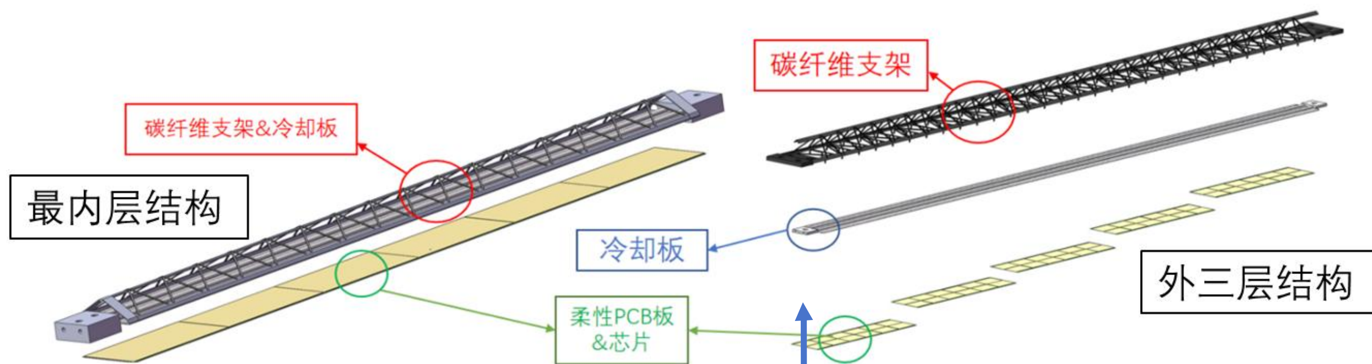
STCF

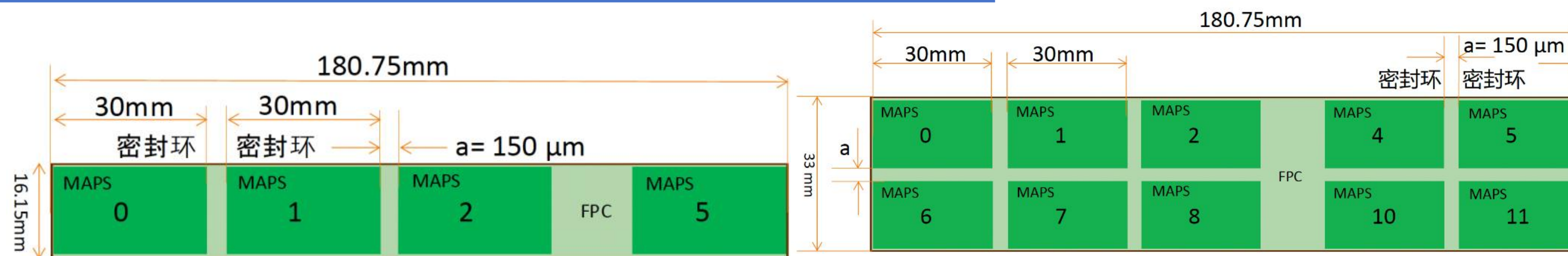
Stave模块设计

- ❖ Stave模块由碳纤维三角桁架、水冷冷却板、柔性印刷电路板和MAPS芯片构成
- ❖ 针对ITKM四层设计了两种不同结构的stave模块
  - 最内层结构携带单列芯片，外三层结构相同，携带两列芯片，仅长度不同



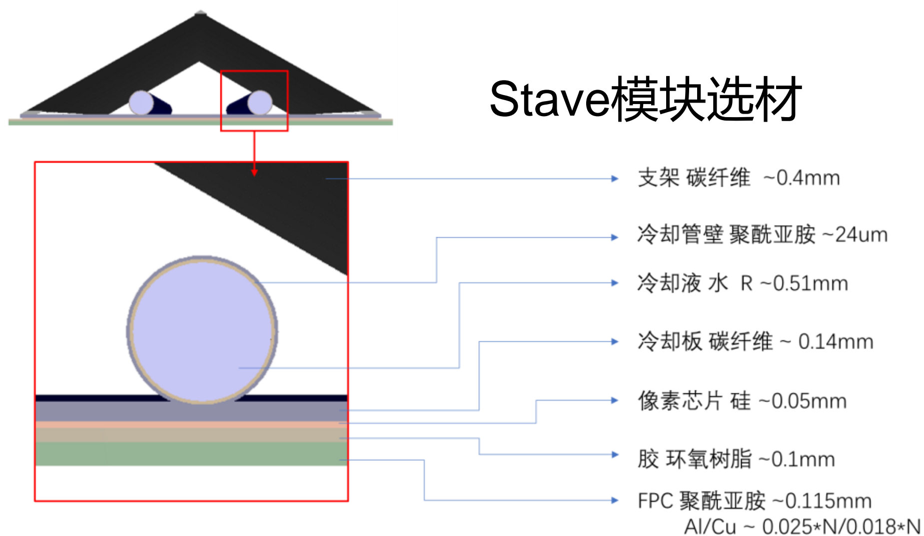


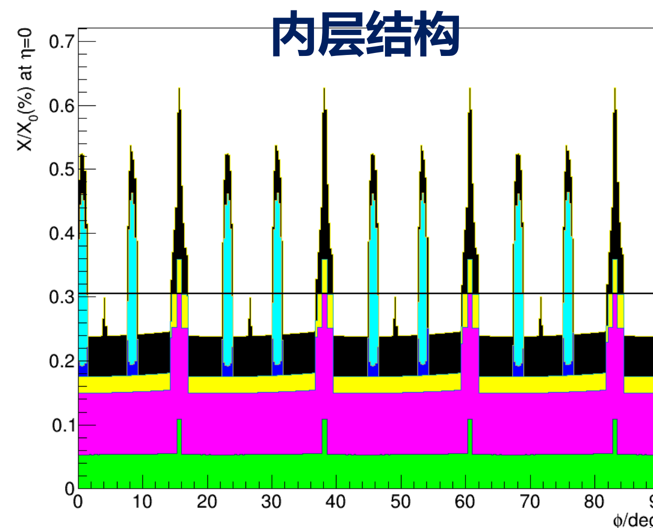


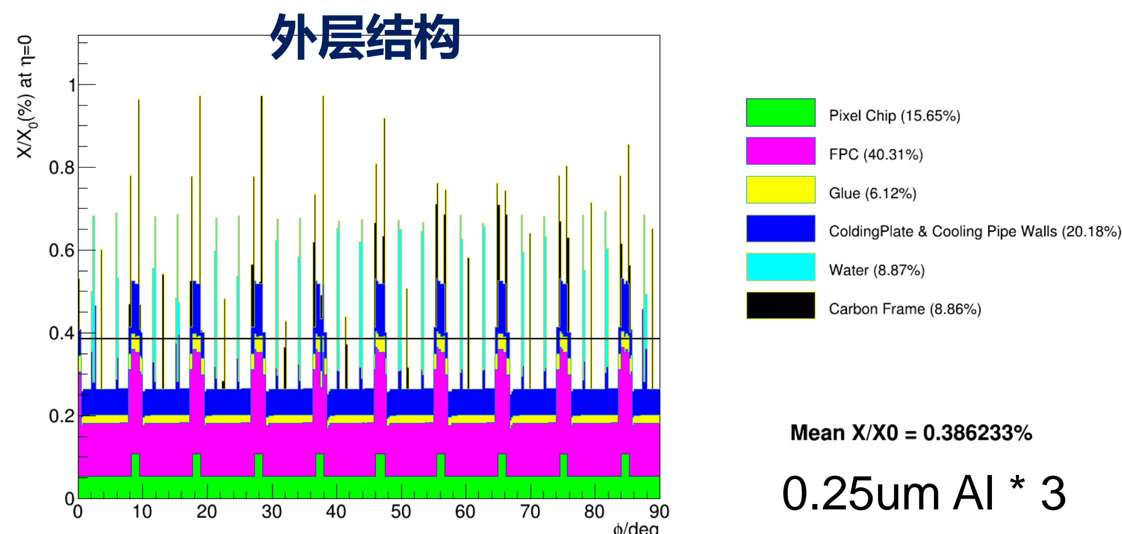


R[mm]	36	88	140	196
L[mm]	180.75	556.5	842.2	1150

Stave模块设计



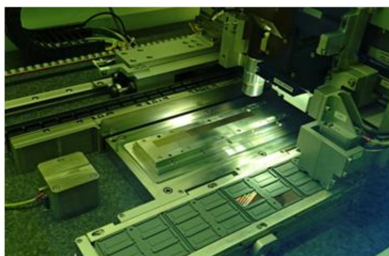




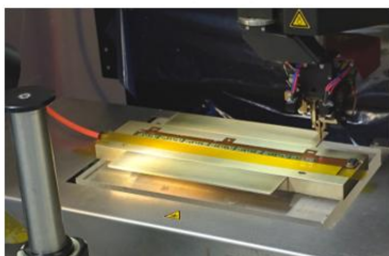
平均物质量沿φ方向的分布

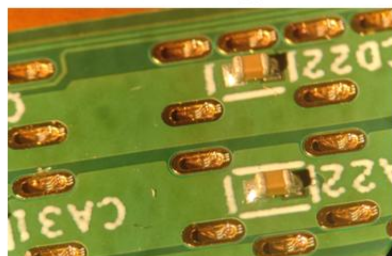
- ❖ 基于当前设计的stave模块，内层结构约0.31% X/X0物质量，达到目标。外层结构约0.39% X/X0物质量（以FPC三层铝计算）
- ❖ 在保证供电压降的前提下优化外层物质量，将是接下来的重点工作

Stave模块设计


芯片摆放对齐

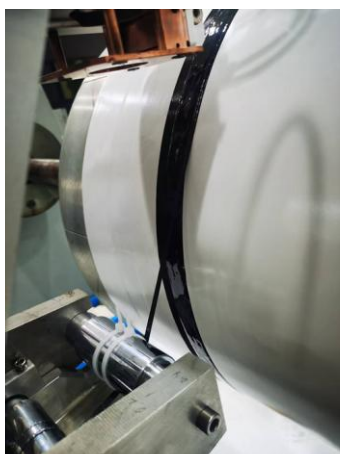
芯片-PFC粘合固化


芯片-PFC绑线


完成绑线的FPC焊盘

- Stave生产工艺已验证可行
- 与中科院宁波材料所达成合作，第一批stave碳纤维部件样品已完成制作，正在迭代优化中

- 基于Dummy ALPIDE芯片 + 铜基1*7FPC完成了两个混合集成电路（HIC）模块的制作
- 集成精度优于5um，绑线质量合格


预浸料加工

冷却板固化

M55碳纤维缠绕成型

冷却板

M55J缠绕成型

探测器服务桶的整体结构设计

- ❖ 设计对称式服务桶结构，支撑四层探测桶（桶径分别为：3.6cm, 8.8cm, 14cm和19.6cm）
- ❖ 设计分体式轮盘结构，将服务桶固定在MDC内筒
- ❖ 设计四爪法兰结构，将服务桶与MDI绑定安装

MDC

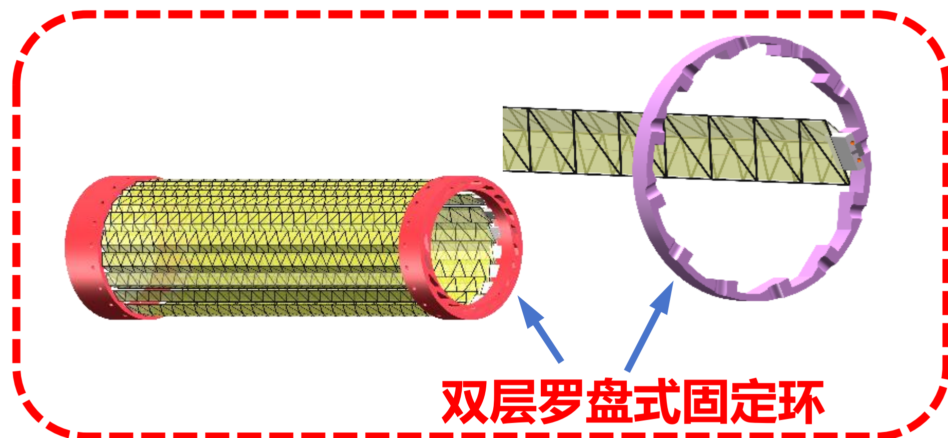
服务桶与MDC之间的连接

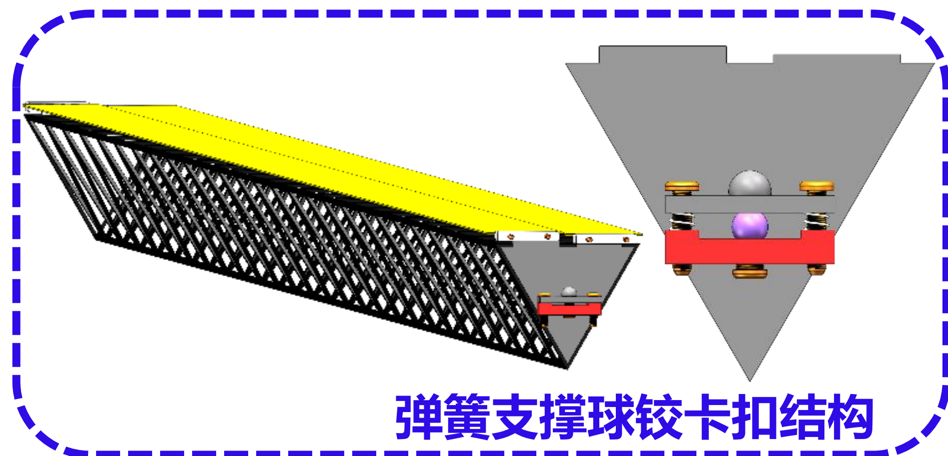
服务桶与MDI之间的绑定

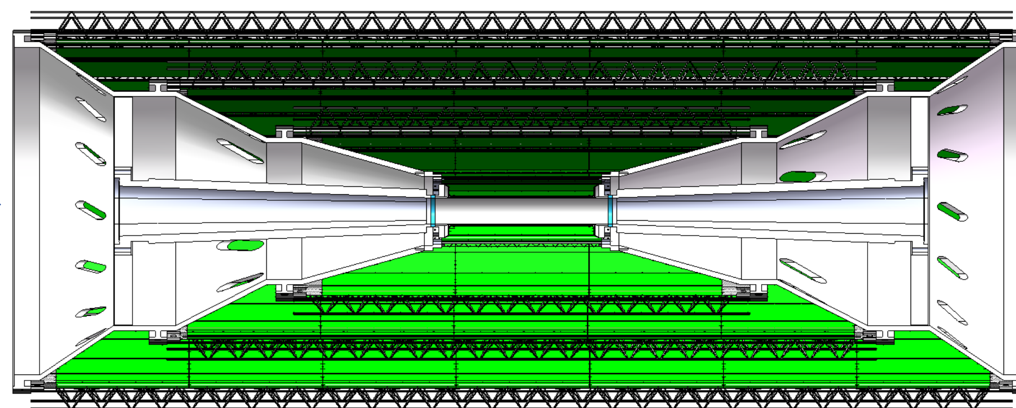
探测器桶部结构

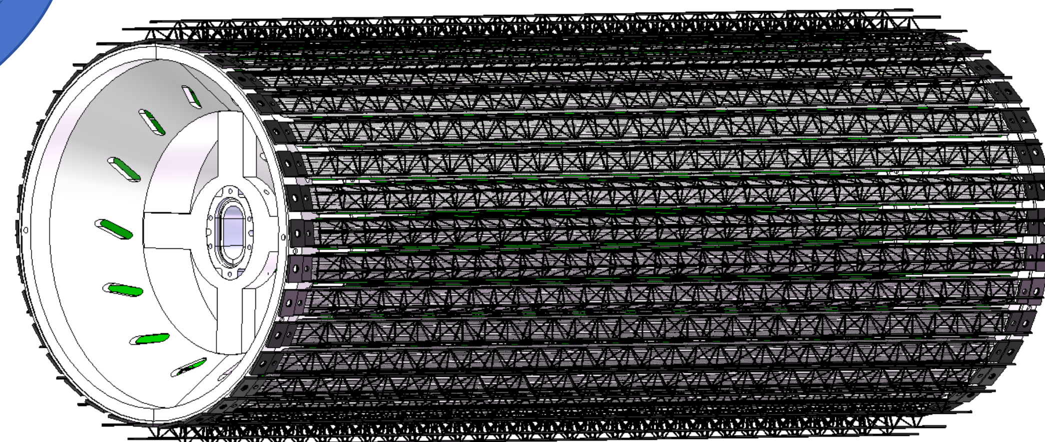
STCF

- 设计双层罗盘式固定环结构，通过螺钉将内层Stave安置于服务桶相向小端面
- 设计弹簧支撑球铰卡扣结构，将外层Stave安置于服务桶外壁平台









总结

- STCF MAPS要求
  - 位置+时间+能量测量、低功耗、低物质量
- MAPS设计
  - 基于TowerJazz180工艺：CharTPix-TJ
    - 第一版MAPS芯片：探测效率>99%，时间精度好于50 ns (without TOT correction)
    - 第二版芯片即将回片
  - 基于GSMC130 工艺：CharTPix-GSMC
    - 基于新型读出架构设计
    - 第一版MAPS芯：探测效率>99%，位置精度~5 μm，时间精度好于50 ns (with TOT correction)
  - 基于Iray180工艺：CharTPix-IRAY
    - 改进型工艺，开展了小阵列原型验证芯片的研制和测试
    - 电荷收集性能显著提升
- 模块组装设计
  - 完成Stave结构设计和生产工艺验证
  - 完成碳纤维部件的试制，正在优化迭代中
  - 初步完成了ITKM主体设计及ITKM的Stave、Support service的安装方案

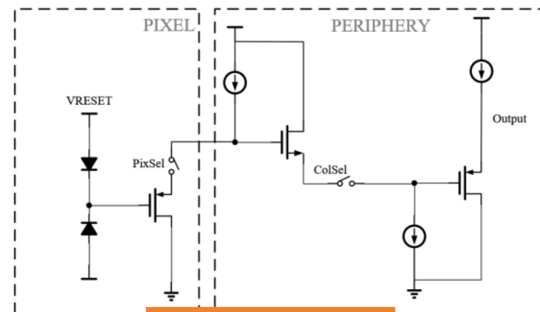
超级陶粲装置
Super Tau-Charm Facility

谢谢！

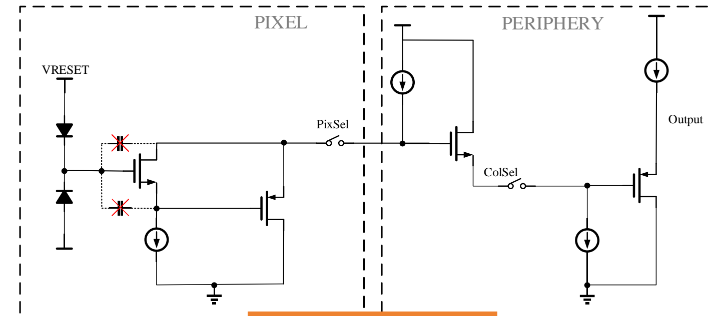
Iray test chip

- ❖ Sensor纯模拟读出
  - 多种像素子阵列
  - 优化输入端等效电容/电路增益
  - 提高信噪比：减小信号损失
- ❖ 模拟前放设计
  - 基于传统cascode结构

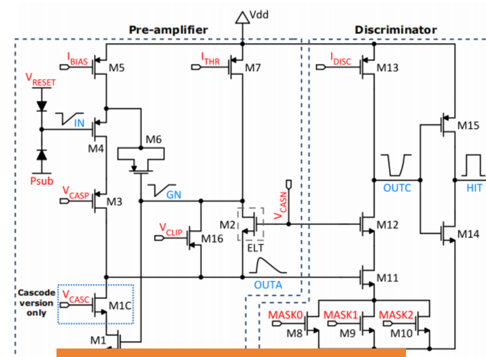
工艺	TJ180	IRAY180
Pitch (μm)	35.6×35.6	30.0×30.0
Threshold (e^-)	153	124
ENC (e^-)	5.4	7.7
MISMATCH (e^-)	4.7	/
σ_{Jitter} (ns)	1.1 (400 e^-)	2.0
模拟功耗(mW/cm²)	16.3	24.0



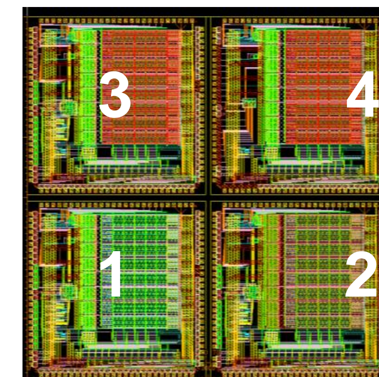
大像素读出



小像素读出



传统cascode结构



Iray test chip

❖N-blanket注入

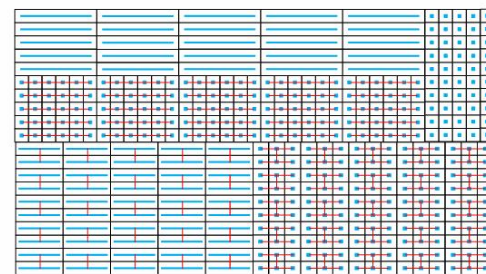
- Chip2-4在Chip1基础上添加N-blanket注入

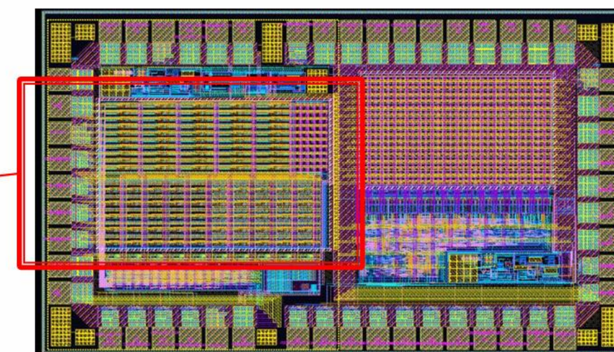
	Special process	Analog pixel array	Analog front-end test circuit	Transistor test array
Chip1	DPW special NW diode	√	√	×
Chip2	DPW special NW diode modified	√	√	×
Chip3	DPW special NW diode n-gap=2.5 μm	√	√	×
Chip4	DPW special NW diode n-gap=4 μm	√	×	√

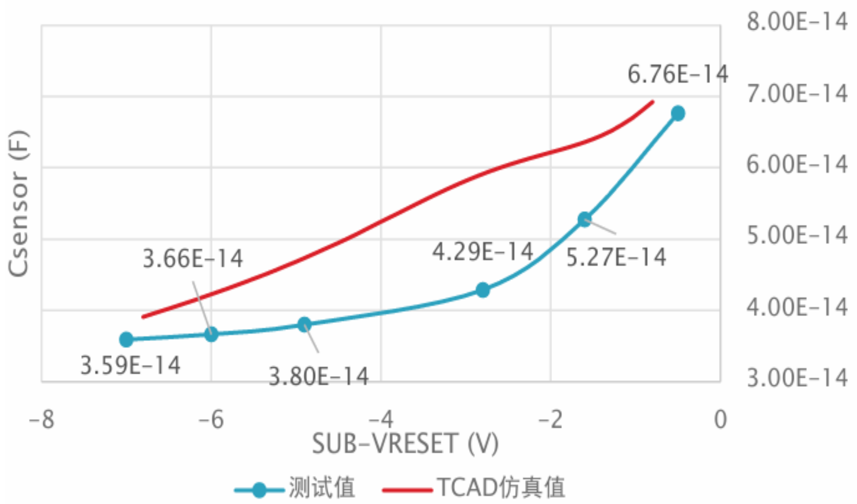
CharTPix-TJ-v0.1： Fe55放射源测试

Chip4 (模拟读出)测试：Sensor寄生电容

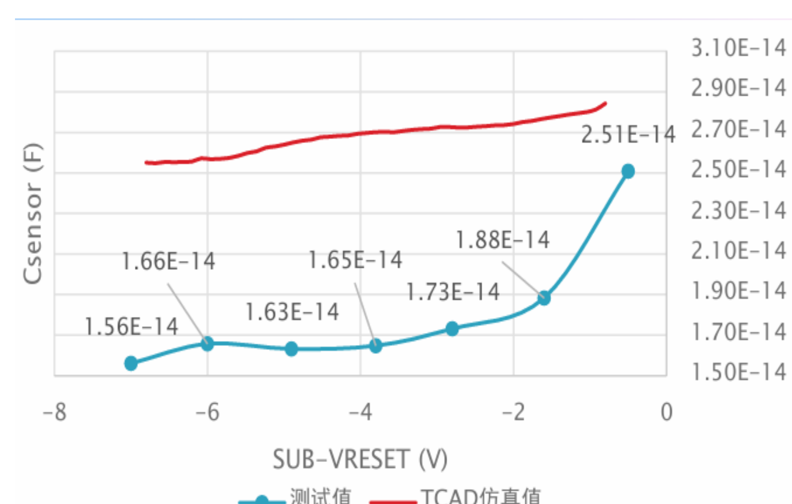
- 利用Fe55全能峰标定sensor电容
- 测试与仿真结果有一定差距，但已经是比较接近
- 为后续改版和国产工艺的研究提供重要参考



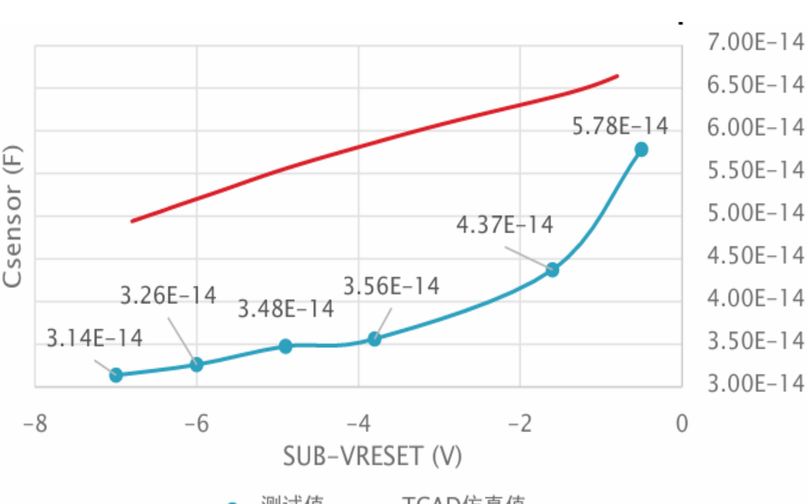




1×6 strip-based像素



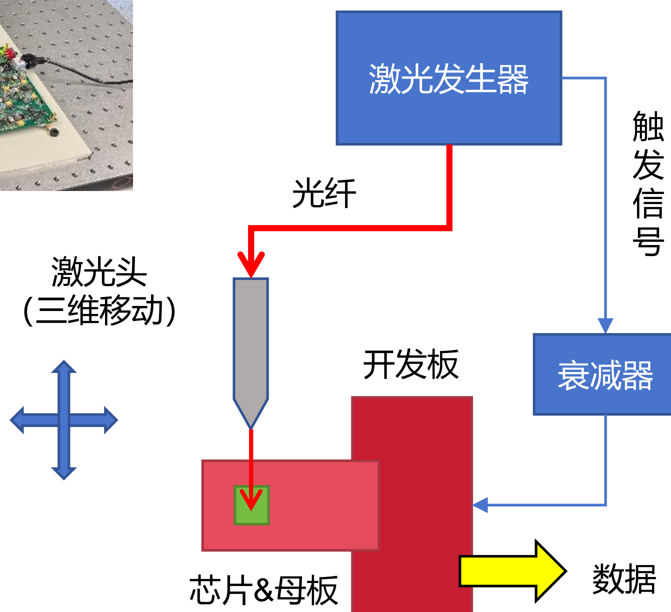
1×6 pixel-based像素

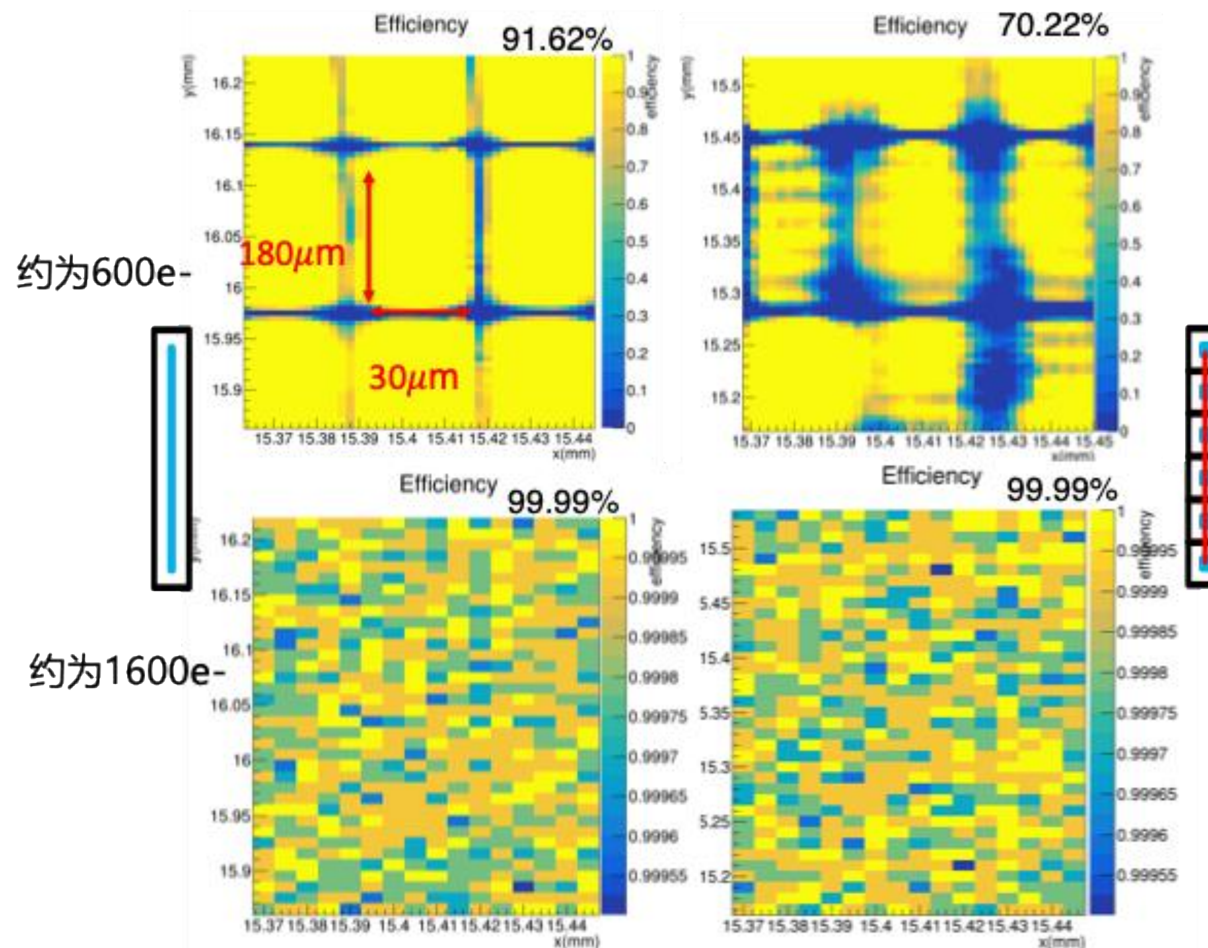


2×3 strip-based像素

CharTPix-TJ-v0.1：激光测试

- 红外皮秒激光测试
  - 高精度三维移动平台（1μm精度）
  - 激光强度可调，利用S-curve标定激光强度



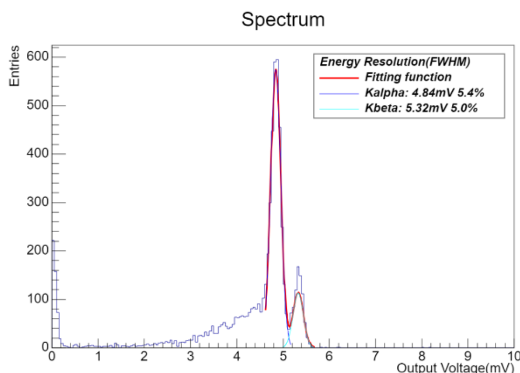


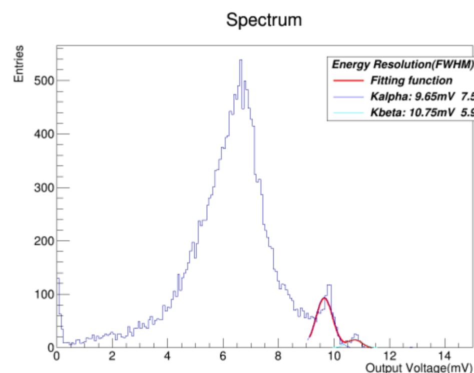
CharTPix-TJ-v0.1： Fe55放射源测试

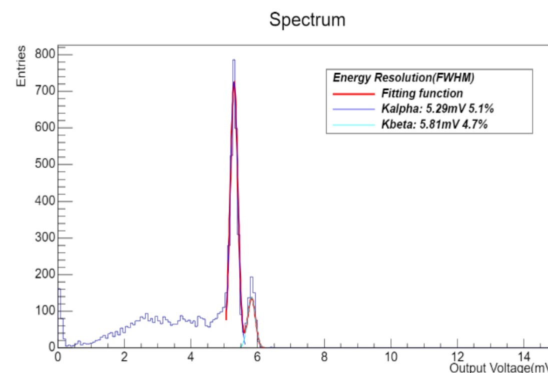
Chip4 (模拟读出)测试

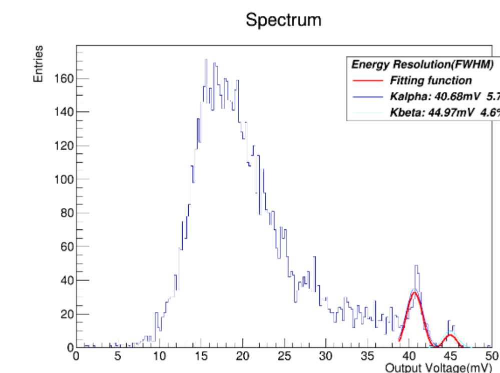
- Strip型能观测到明显的全能峰 →更好的电荷收集效率
- Sensor上升时间可以好于20ns

能谱

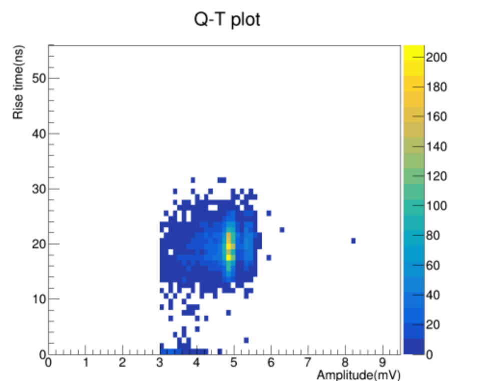


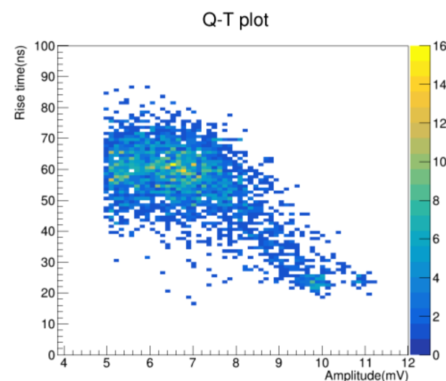


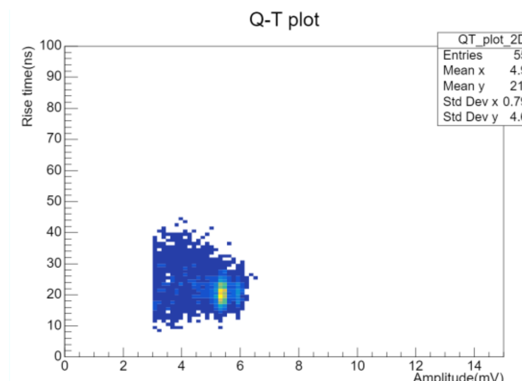


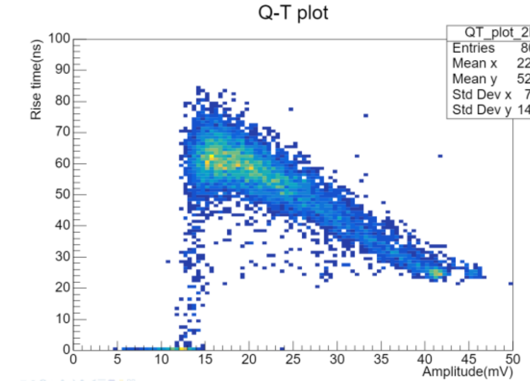


上升时间



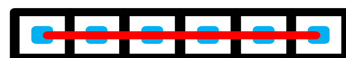




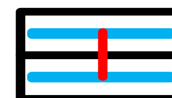


1×6 strip-based

1×6 pixel-based



2×3 strip-based

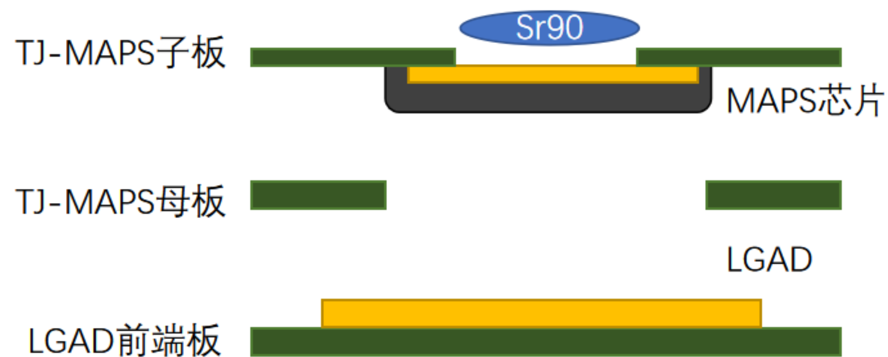


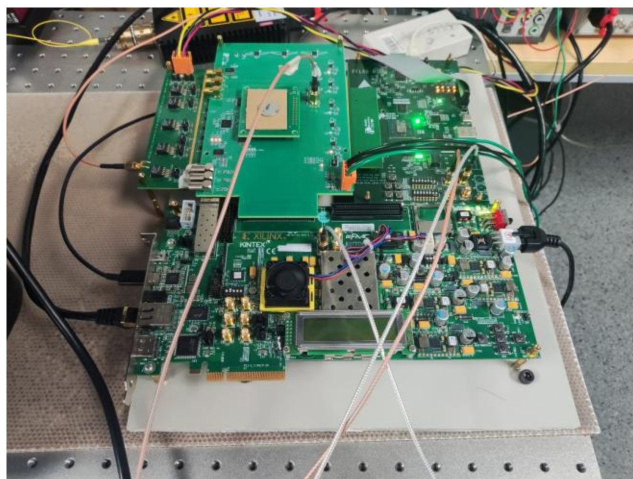
1×1 ALPIDE-like

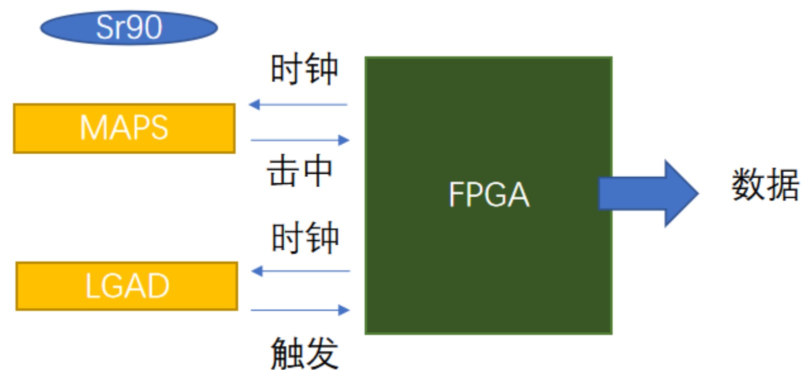
CharTPix-TJ-v0.1： Sr90放射源测试

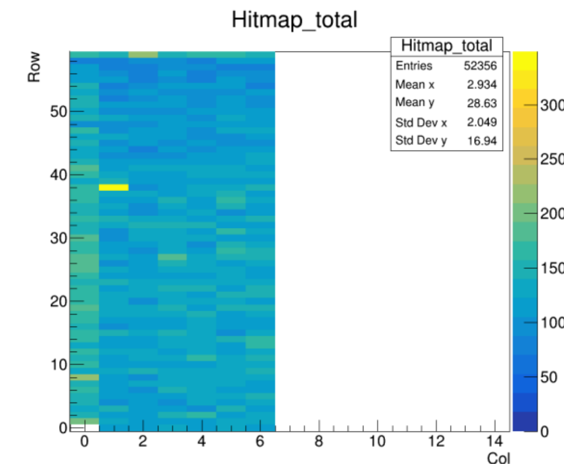
Chip3 时间分辨性能测试

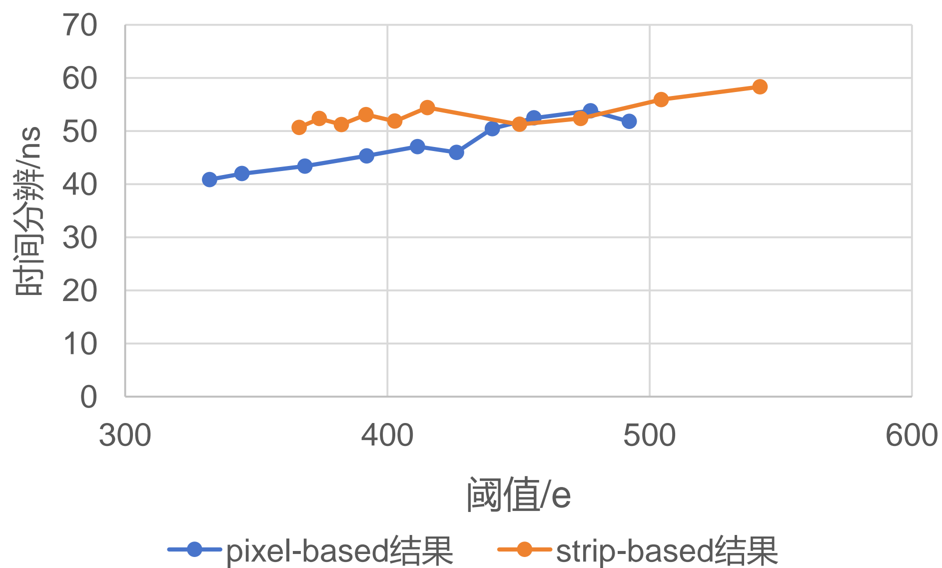
LGAD提供触发和参考时间

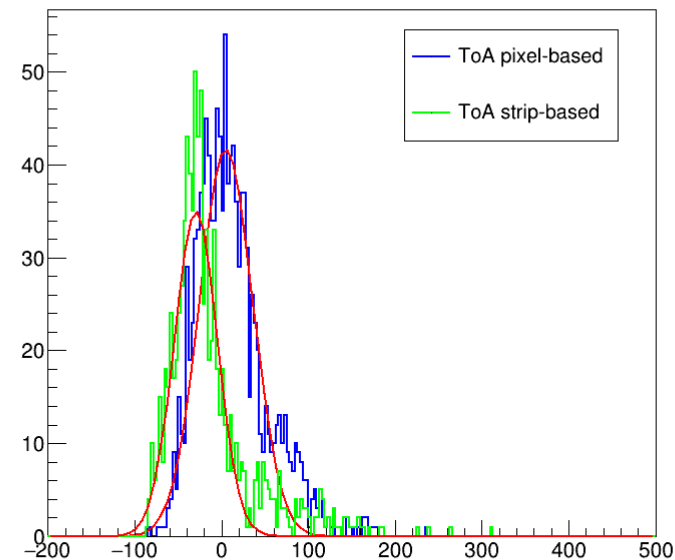










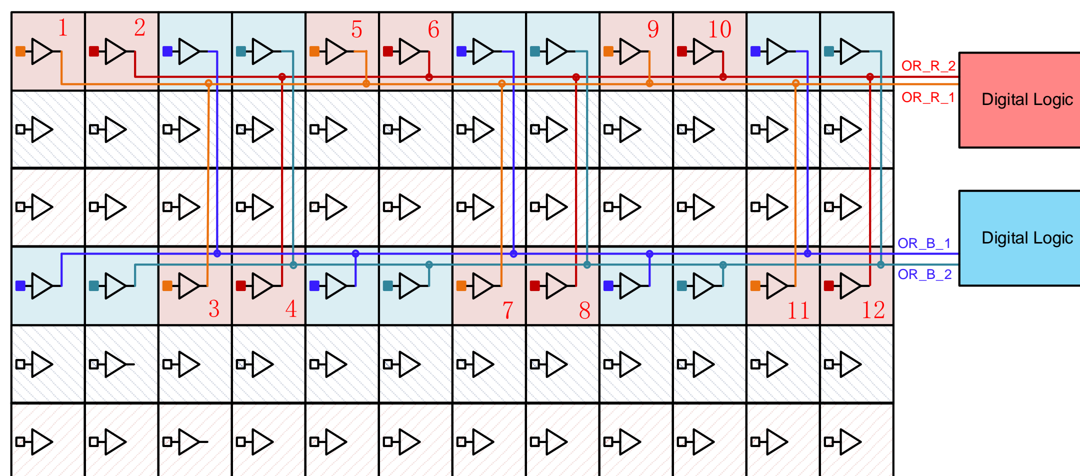


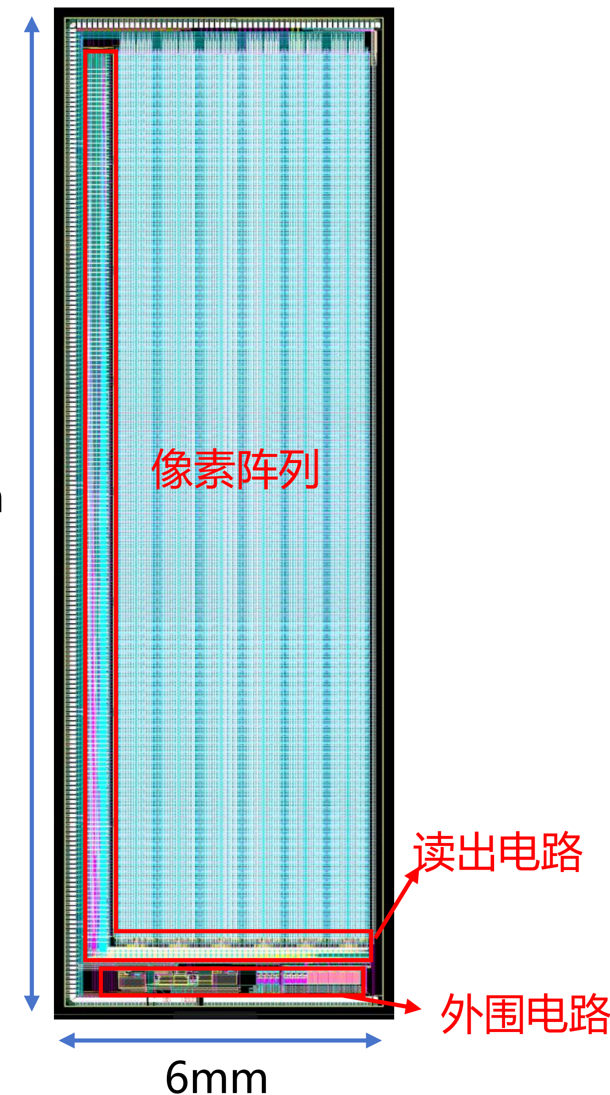
- 时间分辨能好于50ns →基本实现了预期设计指标

CharTPix-GSMC-v0.1

- Chip4:基于超级像素读出方案
  - 通过在超级像素本地合并读出通道，以降低数字功耗
  - 使用起停型VCO提高时间测量精度
  - 高位置分辨(33.2 μm pitch)、高时间分辨(2 ns LSB)、低功耗(<50mW/cm²)

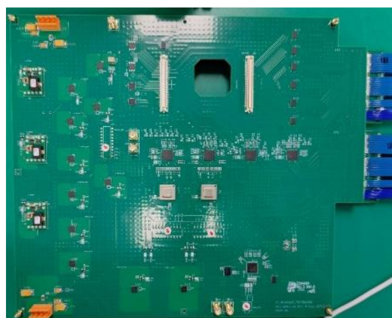
芯片参数	
工艺	GSMC 130 nm
芯片尺寸	**6.1 mm×22.0 mm**
像素阵列	576(行)×144(列)
像素尺寸	33.2 μm×33.2 μm
芯片功耗	44.5 mW
单像素功耗	150 nA/pix
ToA	13-bit (5-bit Fine+8-bit coarse)
ToT	8-bit





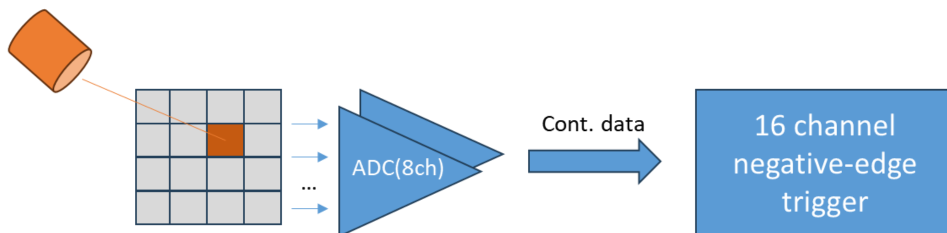
CharTPix-GSMC-v0.1：3T芯片测试结果

- 模拟读出芯片测试
  - ❖Pitch 28μm×28μm，4×4像素阵列输出
  - ❖放射源测试：Fe55



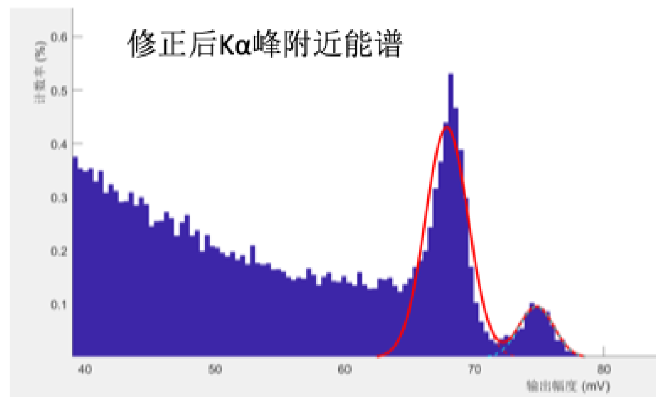
3T芯片读出母板

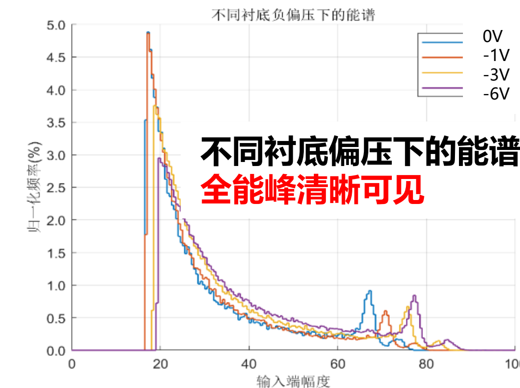
3T芯片读出子板

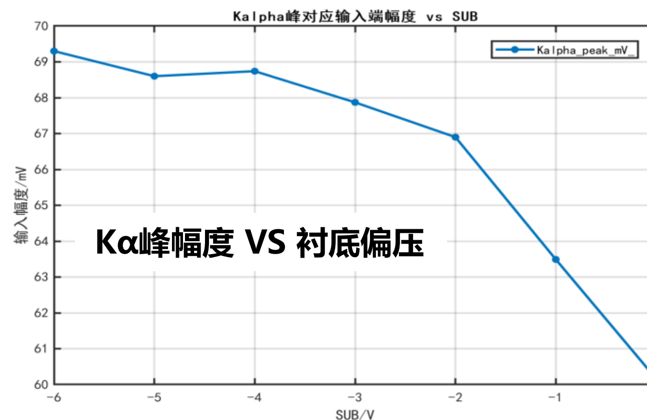


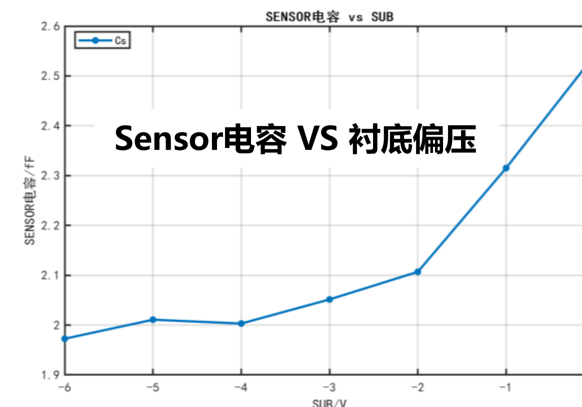
放射源测试示意图

- ❖ 观测到清晰的Fe55能谱
- ❖ 随着负偏压增大，Kα峰对应的信号幅度增大，sensor电容降低
- ❖ 从-1V到-6V，电荷收集性能有所改善





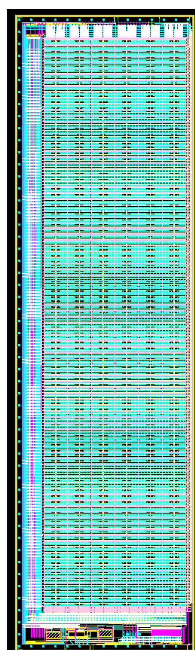


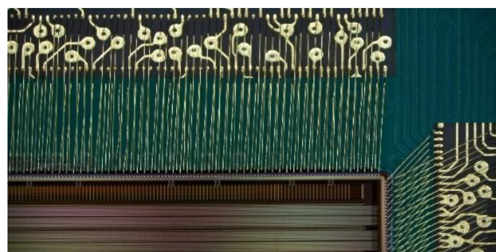


CharTPix-GSMC-v0.1：超级像素芯片

基于超级像素读出方案的原型验证芯片测试

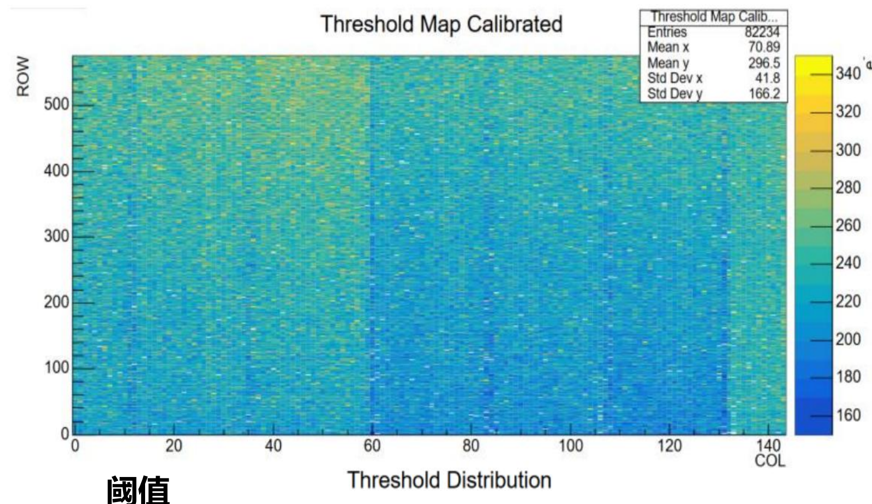
- ❖芯片尺寸：22.0 mm×6.1 mm
- ❖像素阵列：576(行)×144(列)
- ❖像素大小：33.2 μm×33.2 μm
- ❖Position + ToA + ToT





GSMC Chip4打线照片

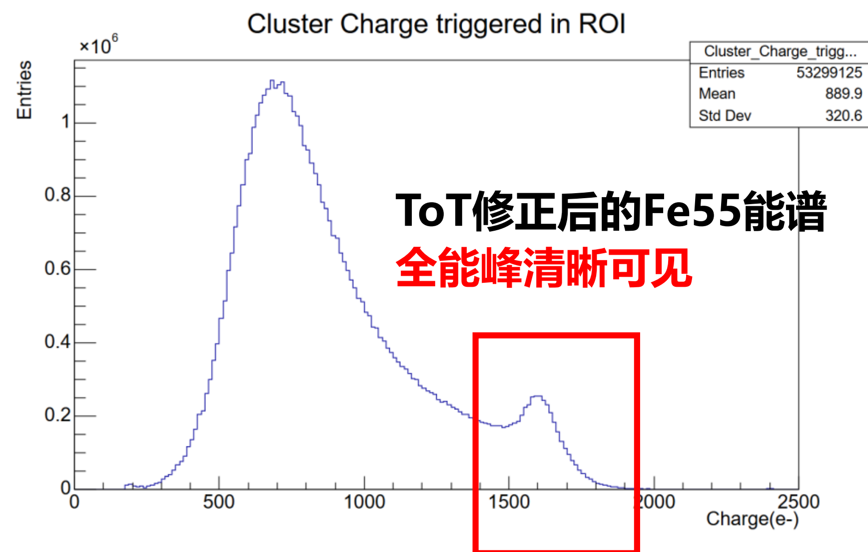
GSMC Chip4测试平台



阈值

Threshold Distribution

Threshold: 225.1e
Mismatch: 26.5e
Thermal Noise：6.6e
@SUB=-4 V

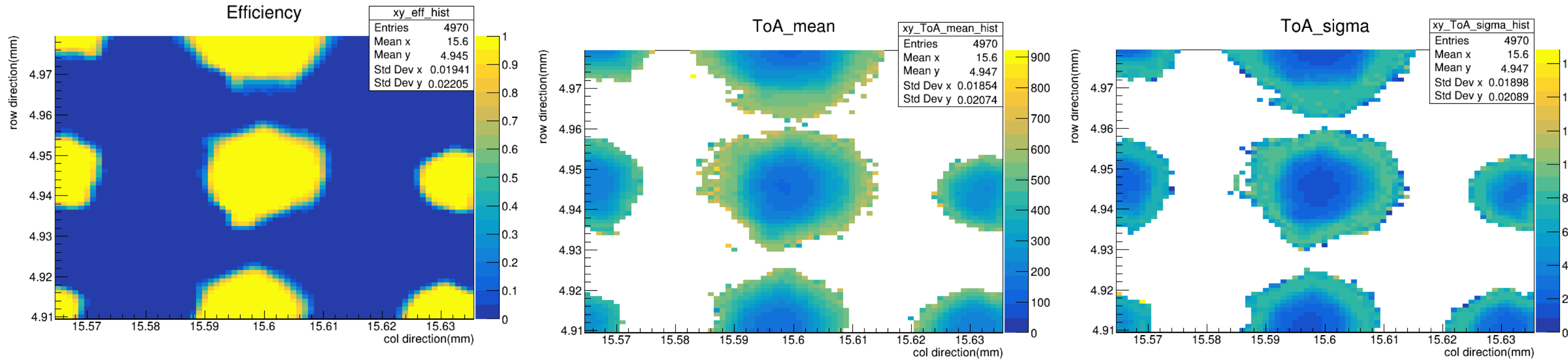


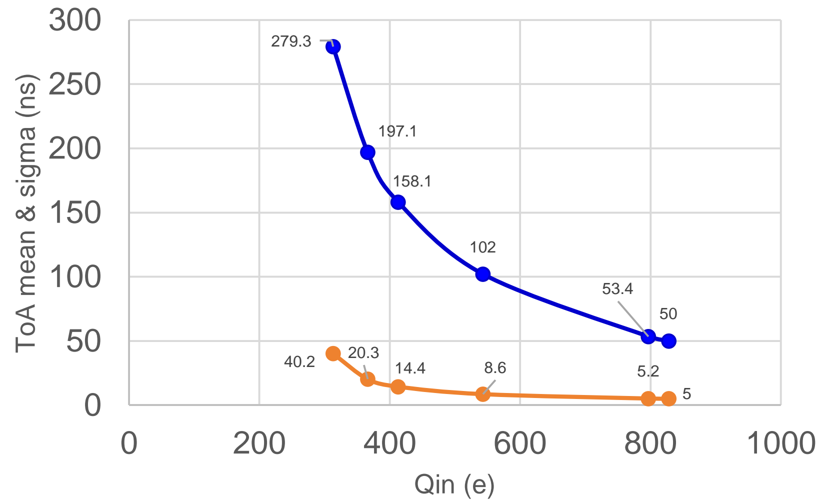
ToT修正后的Fe55能谱
全能峰清晰可见

Time Walk标定后，ToA std由150 ns → 86 ns

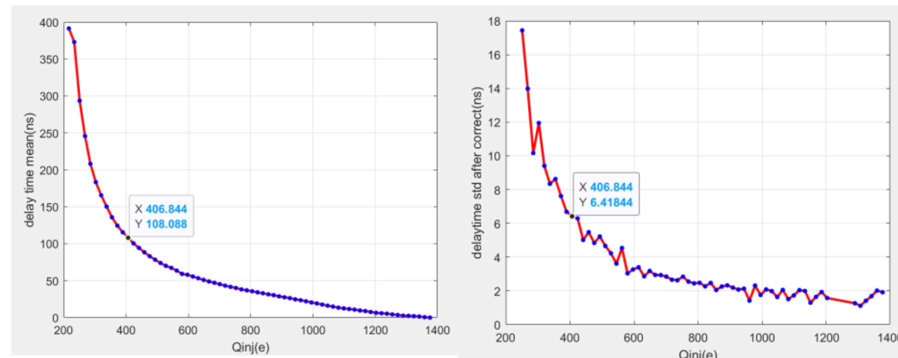
CharTPix-GSMC-v0.1：超级像素芯片

基于超级像素读出方案的原型验证芯片测试：激光测试





激光固定于像素中心处(15.599,4.945)
ToA mean~ ns, sigma~14.4 ns@413 e⁻，与电学自测试结果相近→验证了电路本身的时间分辨性能



Chip4_2_2，像素r33_c89：
- ✓ ToA mean~108.1 ns,
- ✓ ToA sigma~6.4 ns@406 e⁻

模块和机械设计

- ITKM是由MAPS芯片拼成的四层桶状结构，基本结构单元是Stave模块
- 机械结构提供支持和制冷、走线
- 实现低物质量（平均0.3%X0每层）是关键技术挑战