

Compact front-end readout electronics for SiPM-based radiation detectors

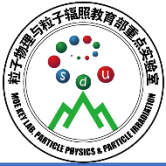
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Meng¹, Kaining Wang¹, Siyuan Luo²

1. Shandong University

2. University of South China

Hefei, Oct-16th 2026

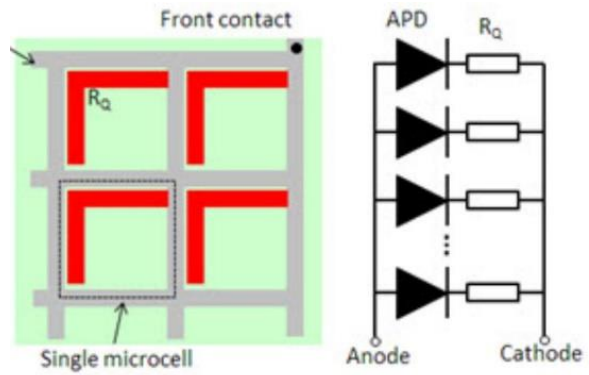




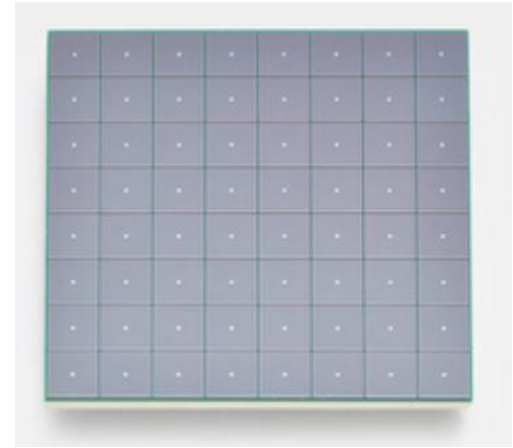
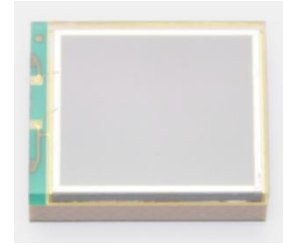
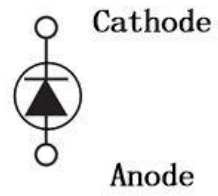
Outline

- SiPM detector
- Readout electronics
 - ✓ Single SiPM readout
 - ✓ SiPM array readout
 - ✓ QDC/QTC circuit
- Application-1: TOF PET
 - ✓ Electronics performance
 - ✓ Detector evaluation
- Application-2: Muography
- Summary

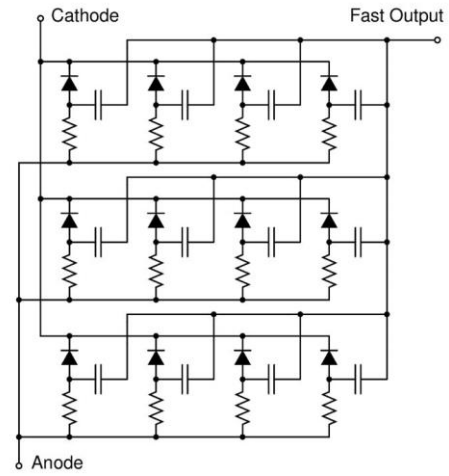
SiPM detector



Hamamatsu, FBK,
AdvanSiD, KETEK

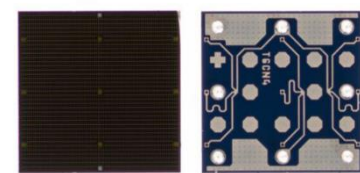
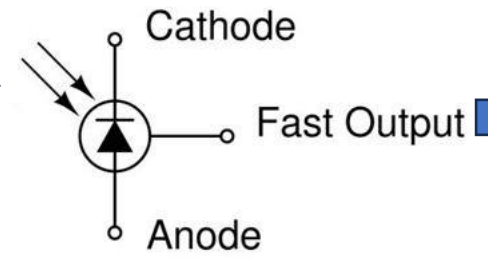


From Hamamatsu

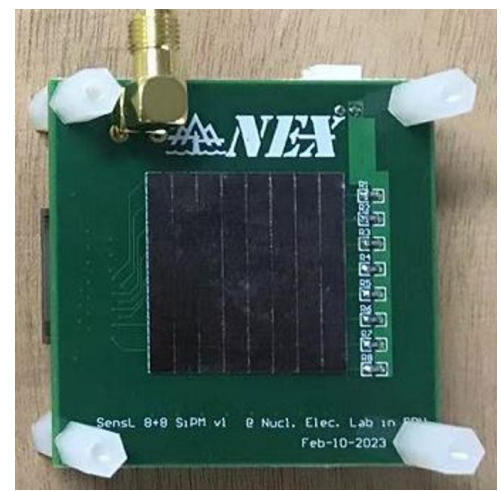


From Onsemi

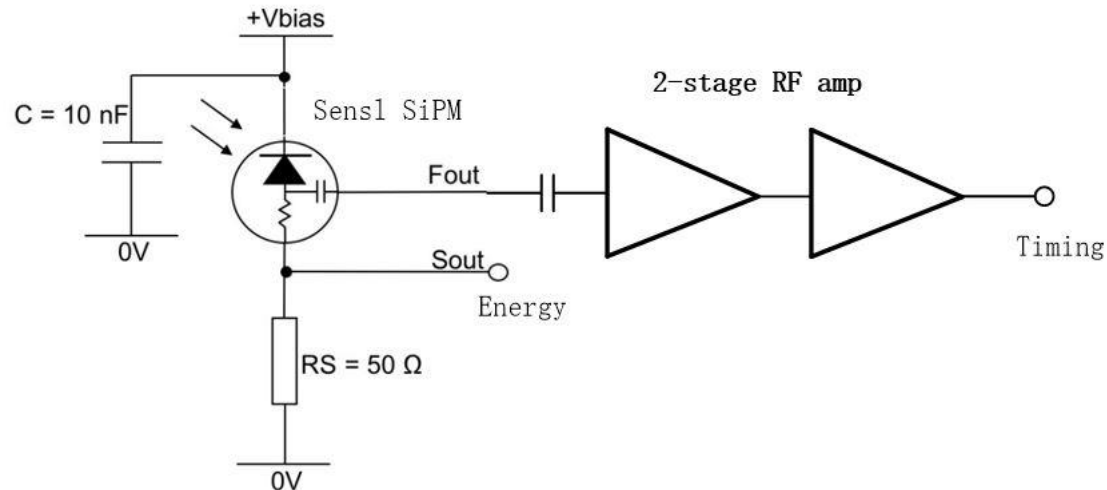
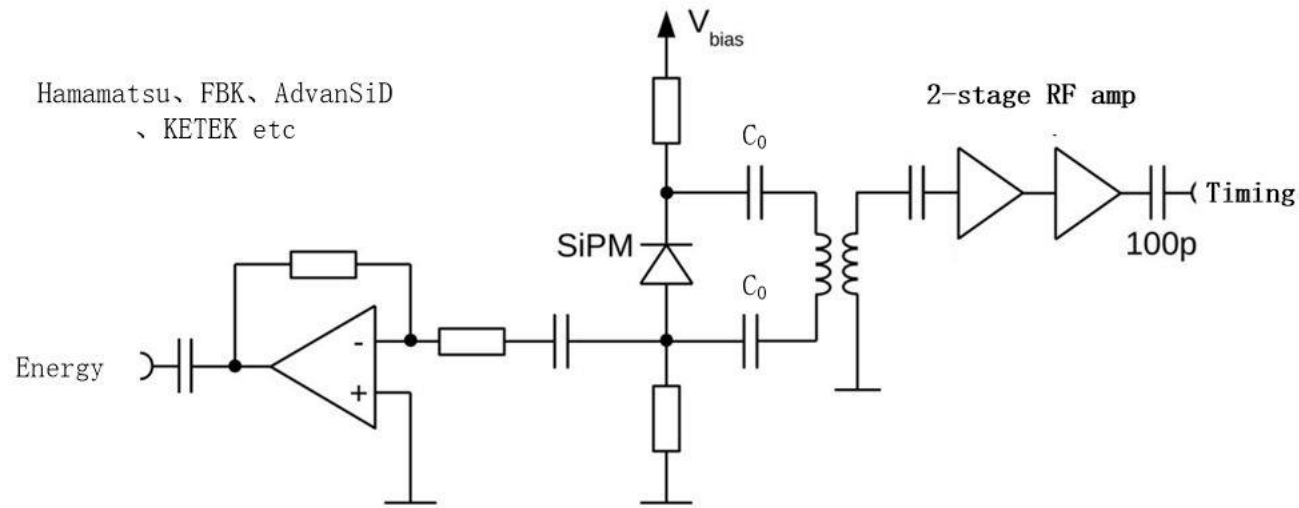
Onsemi



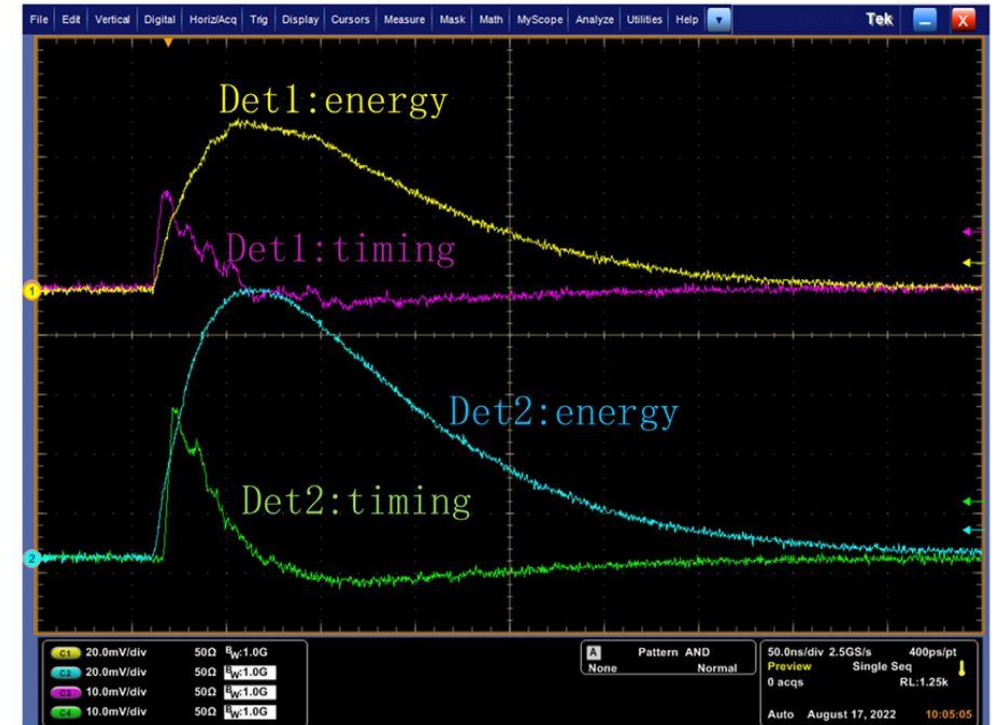
8×8 ch array

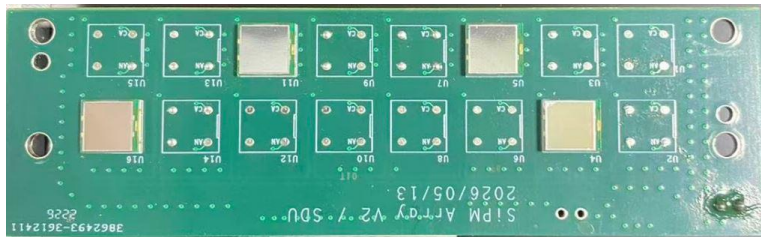


Single SiPM readout

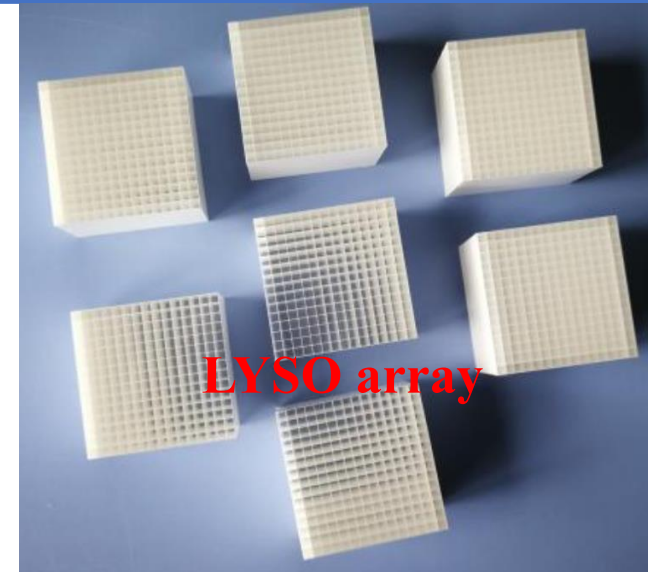


MAR 6+ circuit

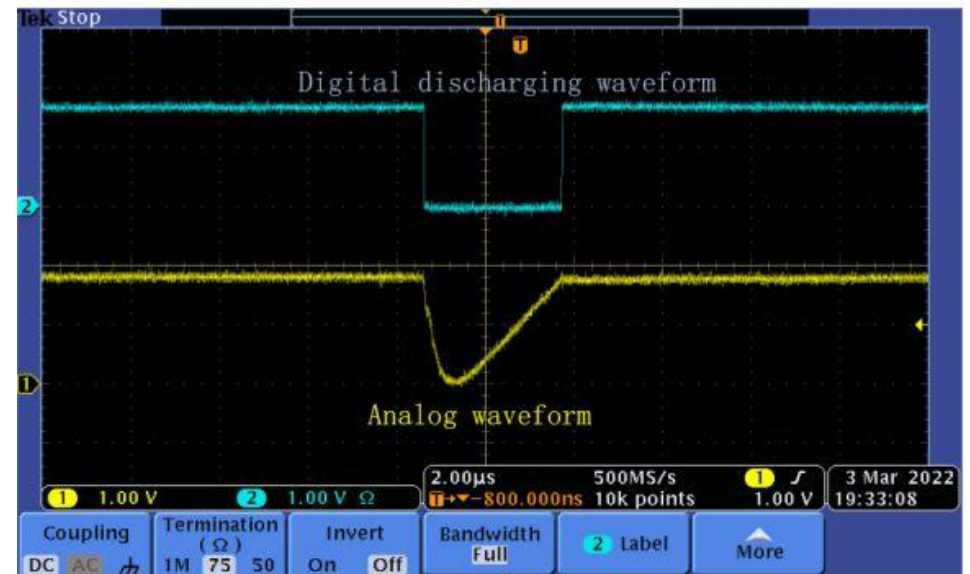
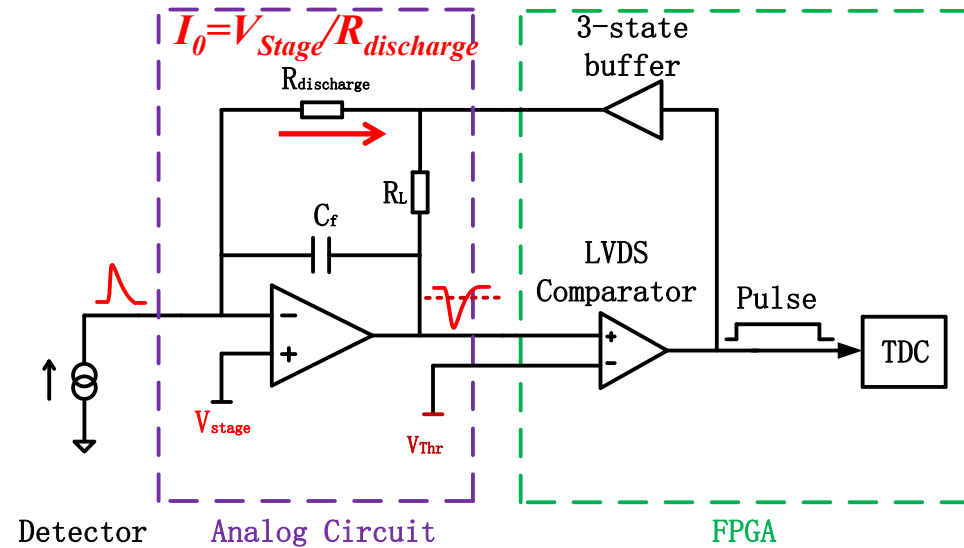
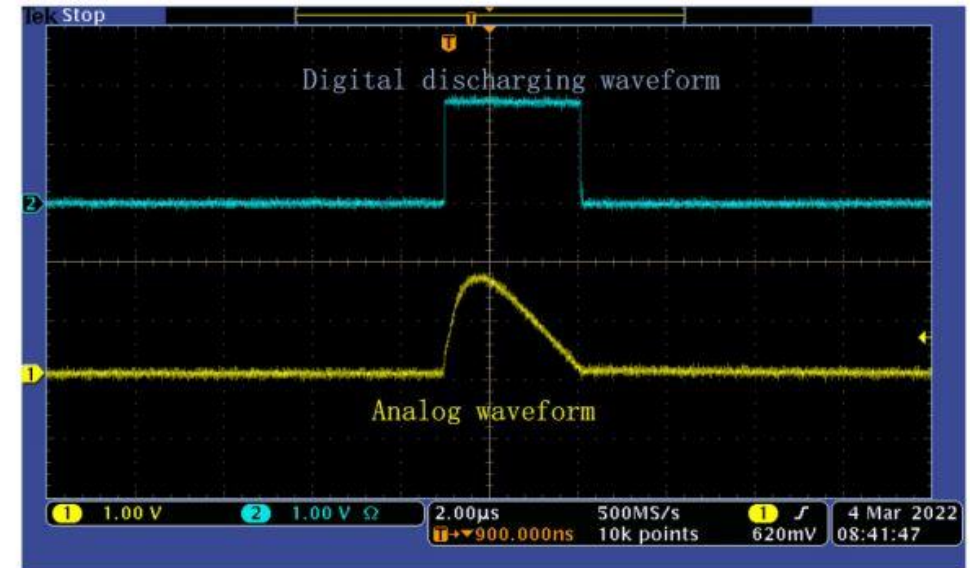
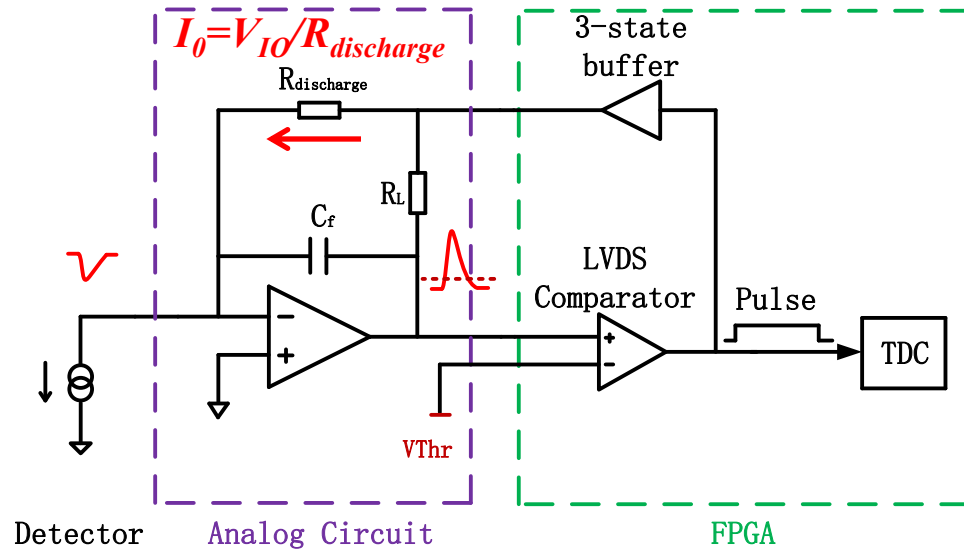


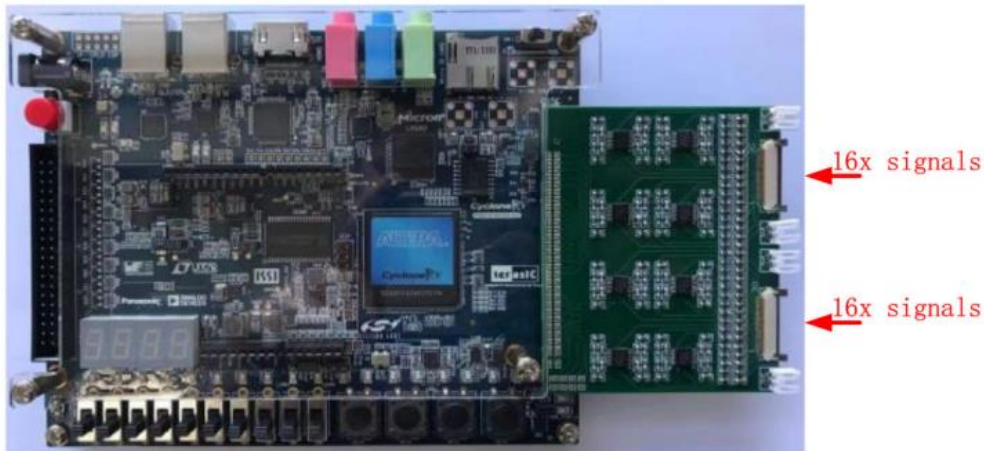


Multiple SiPM in Muography



SiPM array in PET system





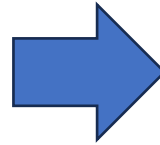
FPGA development board

32-ch front end
analog board

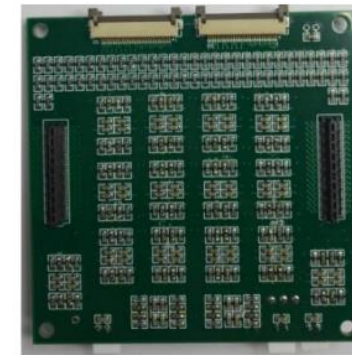
Z. Liu, et al, IEEE TRMPS, (2023) 7(1),pp.11-17

Different versions:

- 1、32-cha prototype: C5G starter development board;
- 2、64-cha dQDC: 70mmx70mm;
- 3、ASIC->lower consumption & compactness。 。 。



Top view
(a)



Bottom view
(b)

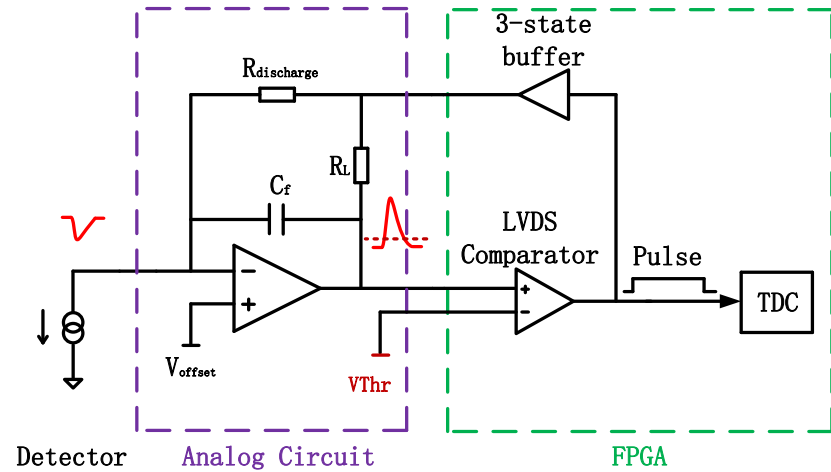


Top view
(a)

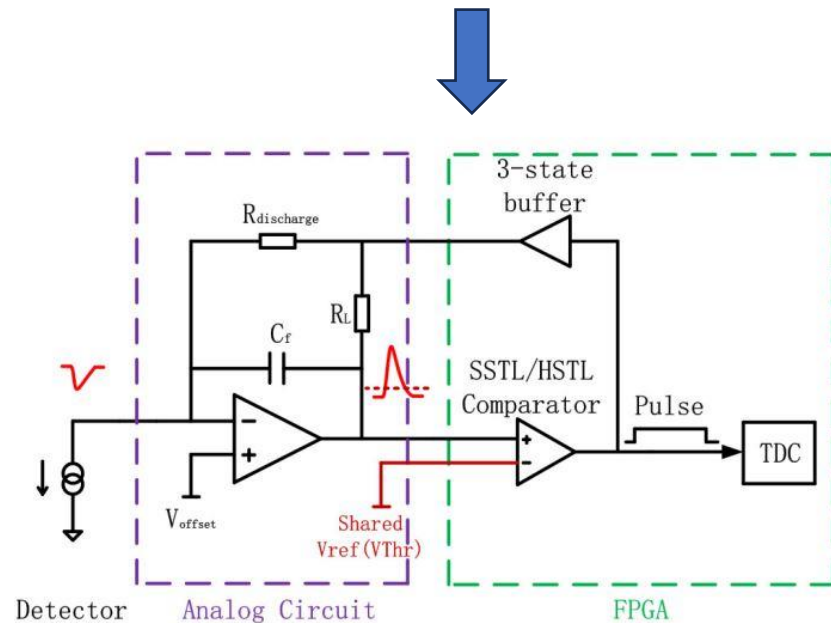
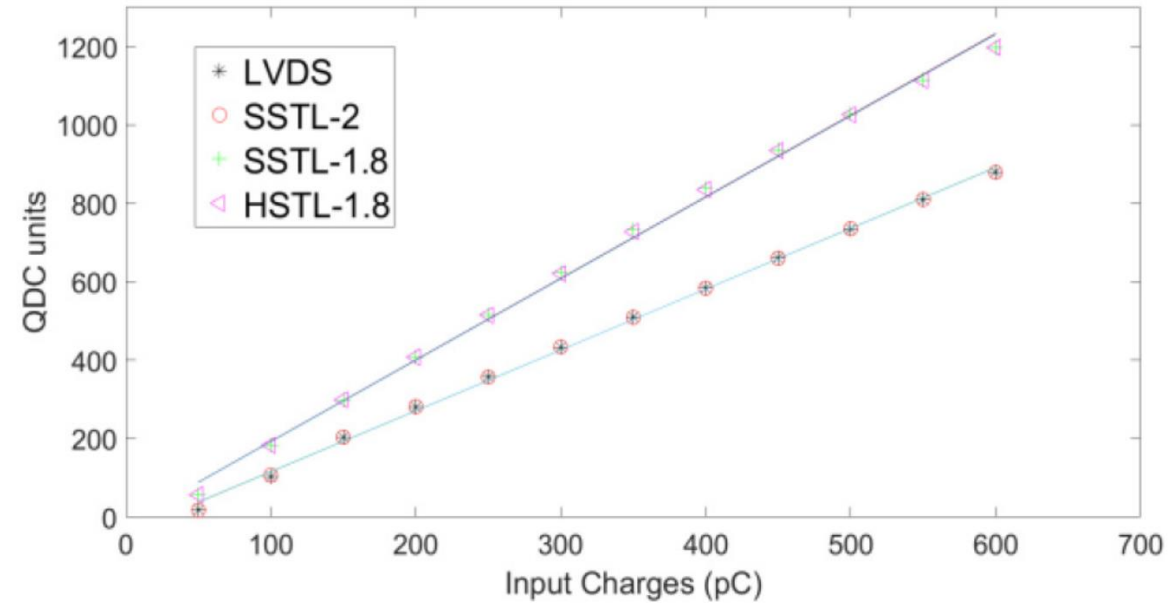


Bottom view
(b)

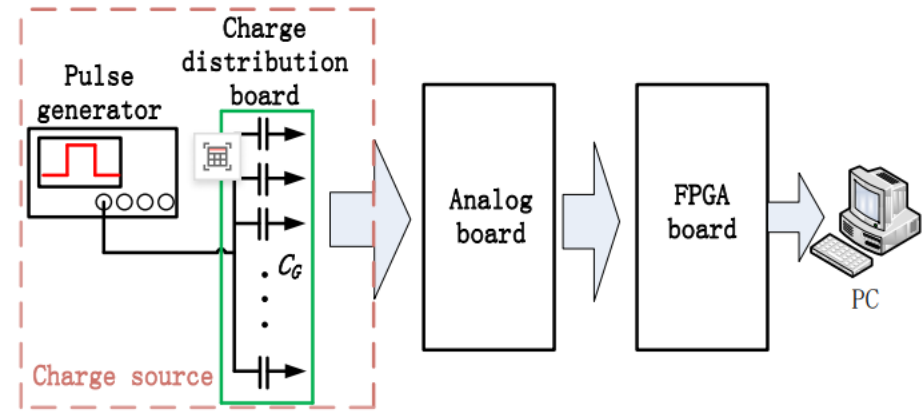
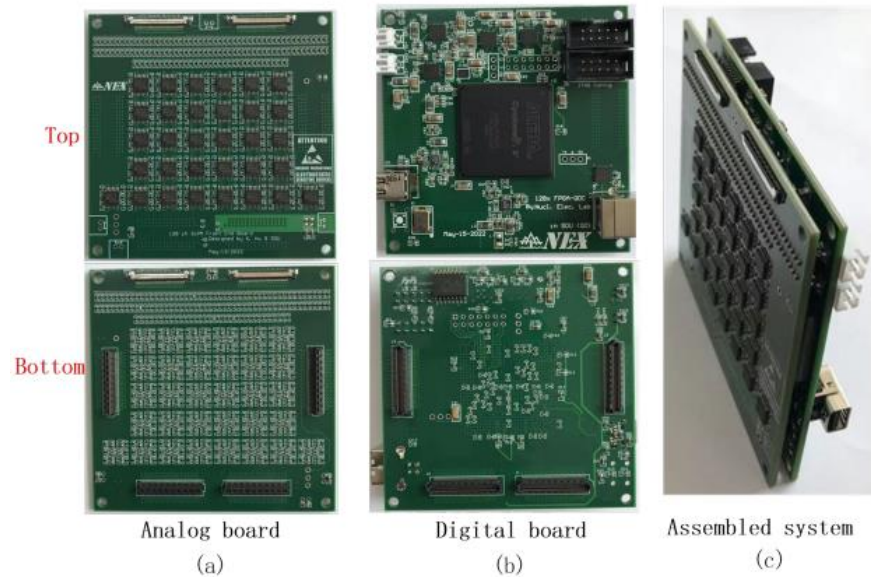
Bo Wang(王博), et al, *NIM A*, 2024



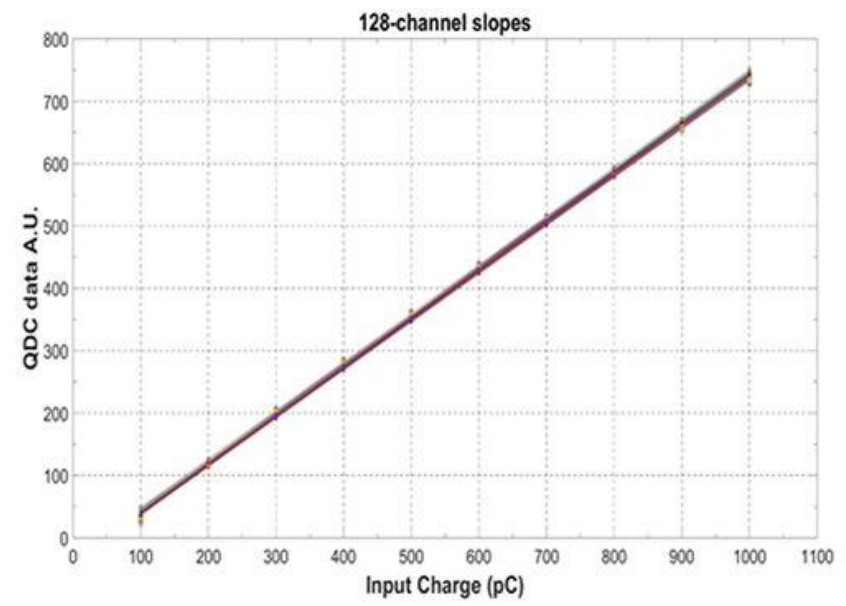
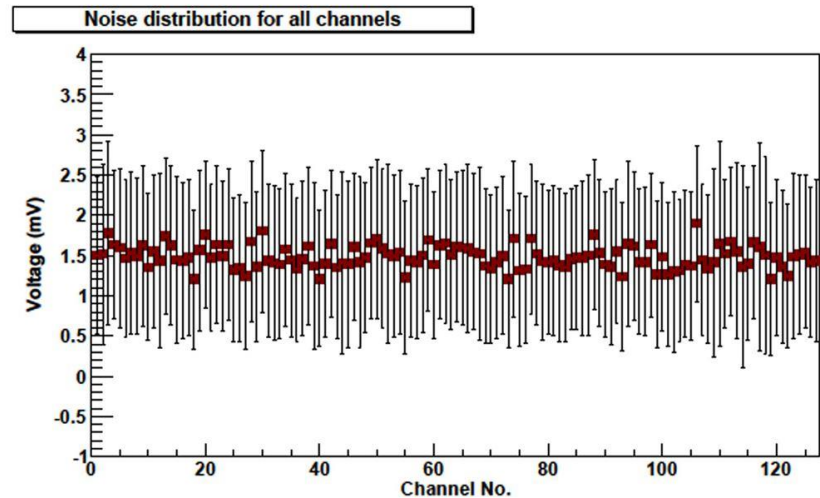
- FPGA LVDS receiver: two pins in FPGA**
 - FPGA-dQDC needs three I/O pin;



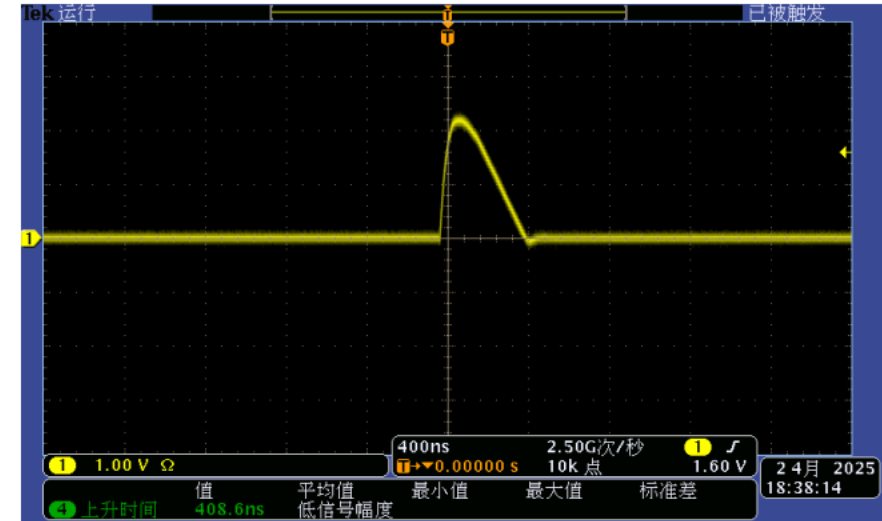
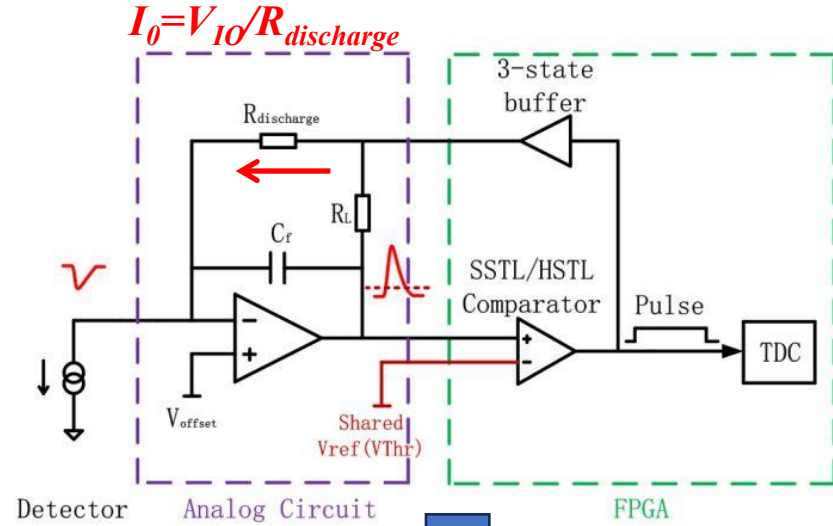
- FPGA voltage-referenced receiver: all share one or two VREF pins (threshold)**
 - SSTL-2, SSTL-1.8, HSTL-1.8,
 - INL :0.87%, 1.00%, and 1.06%



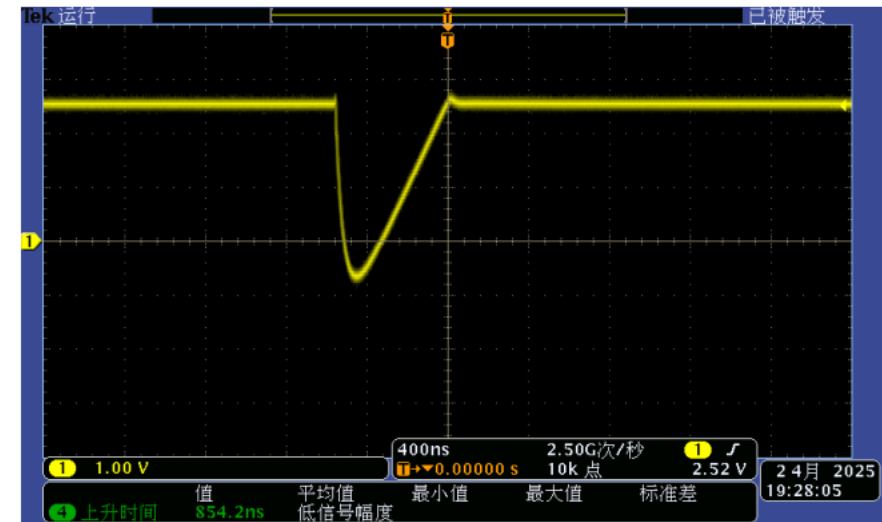
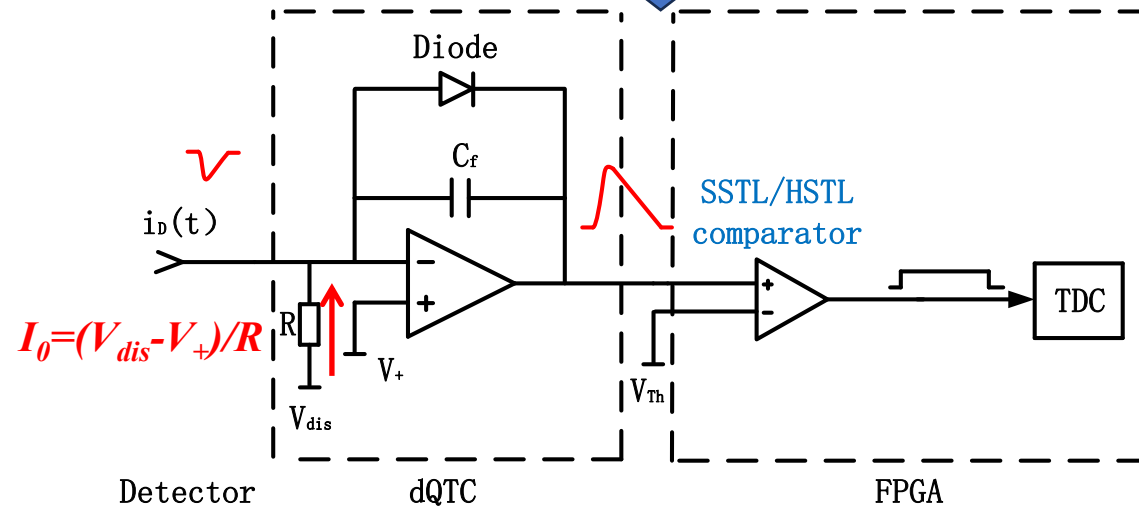
128-cha dQDC: 80mmx80mm;



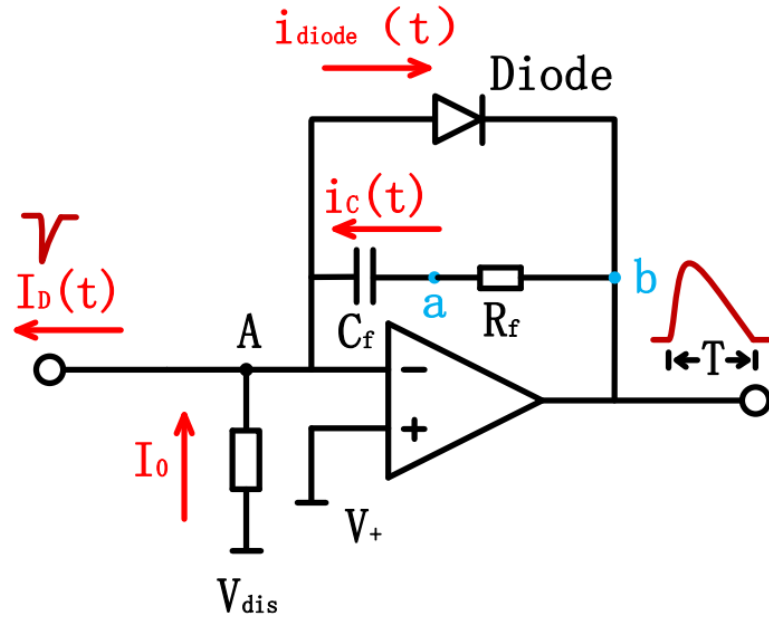
How to increase its compactness?



(a)



(b)

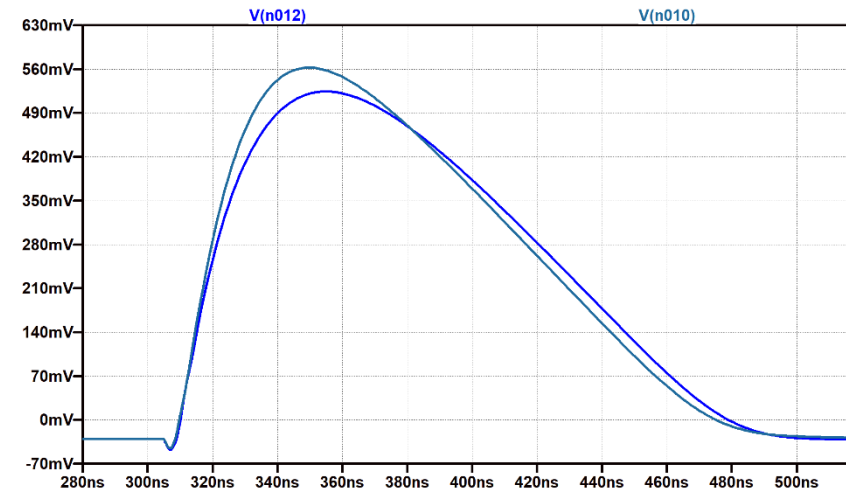


**Feedback resistor R_f in series with C_f :
increase timing performance**

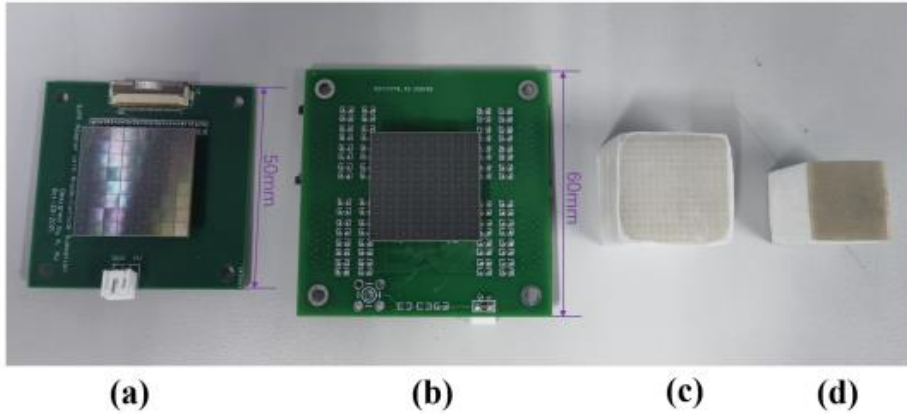
Without R_f : $\left. \frac{dU_o}{dt} \right|_{t=T_{start}} = \frac{1}{C_f} (I_D(T_{start}) - I_0)$

$$\text{With } R_f: \left. \frac{dU_b}{dt} \right|_{t=T_{start}} = R_f \left. \frac{dI_D(t)}{dt} \right|_{t=T_{start}} + \frac{1}{C_f} (I_D(T_{start}) - I_0)$$

$$\left. \frac{dU_b}{dt} \right|_{t=T_{start}} > \left. \frac{dU_o}{dt} \right|_{t=T_{start}}$$



Application 1: PET & TOF PET detector evaluation

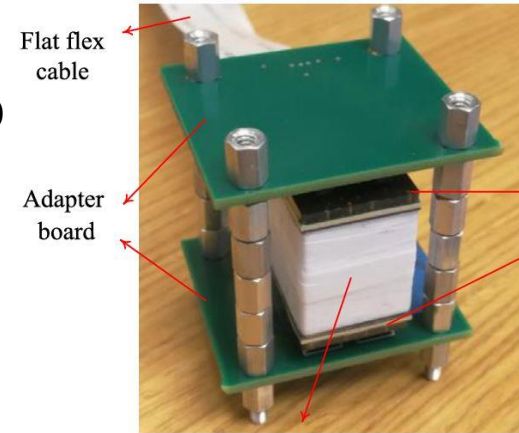
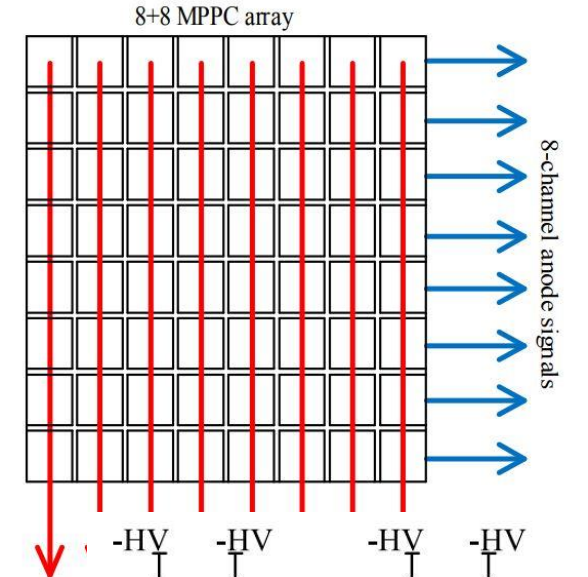


8x8 array
/8+8 array

8x8 MPPC array

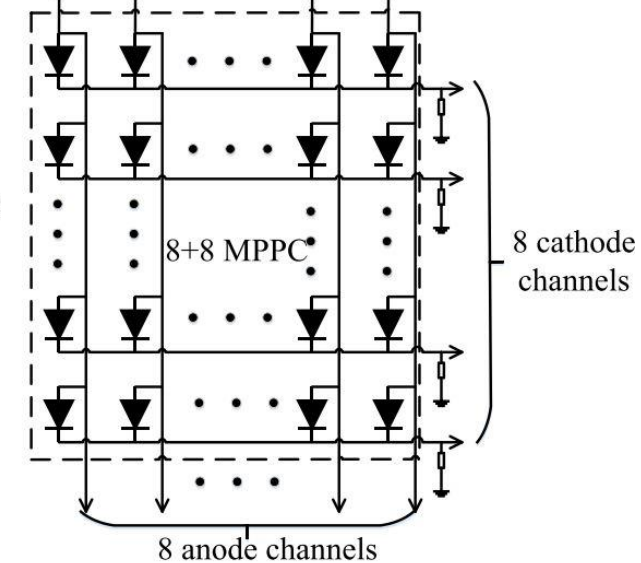
A-1	A-2	A-3	A-4	A-5	A-6	A-7	A-8
B-1	B-2	B-3	B-4	B-5	B-6	B-7	B-8
C-1	C-2	C-3	C-4	C-5	C-6	C-7	C-8
D-1	D-2	D-3	D-4	D-5	D-6	D-7	D-8
E-1	E-2	E-3	E-4	E-5	E-6	E-7	E-8
F-1	F-2	F-3	F-4	F-5	F-6	F-7	F-8
G-1	G-2	G-3	G-4	G-5	G-6	G-7	G-8
H-1	H-2	H-3	H-4	H-5	H-6	H-7	H-8

Note: common cathode

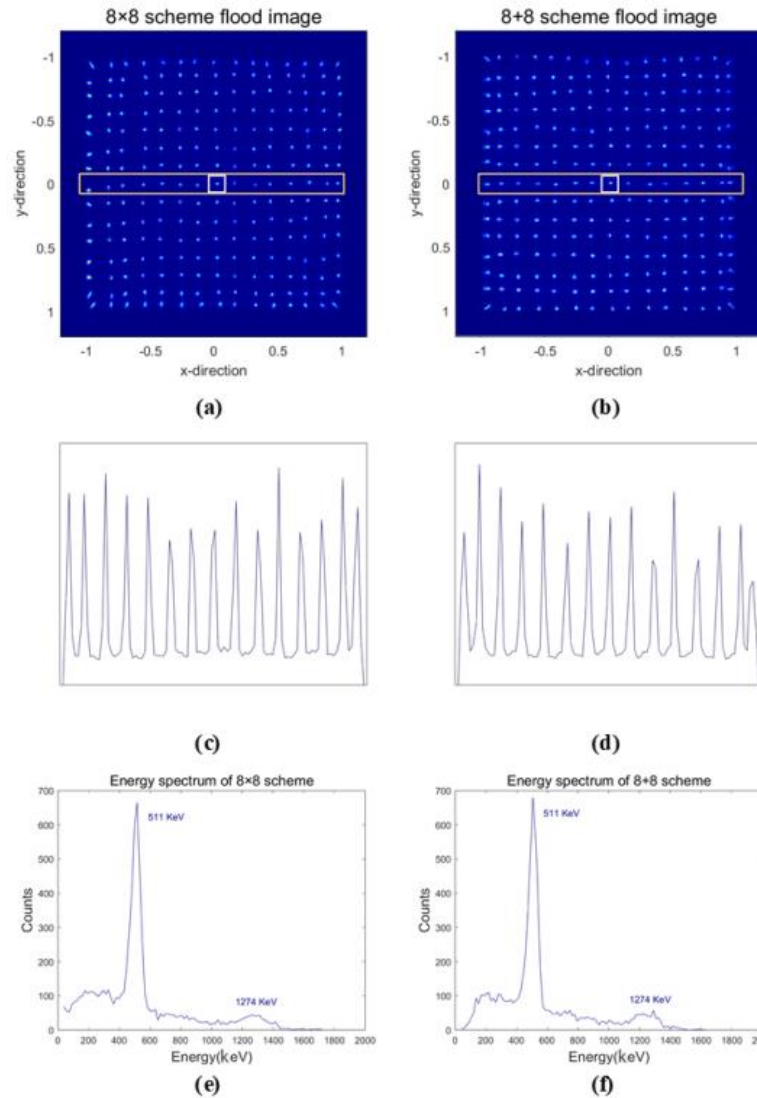


15x15 LYSO array

8+8 MPPC

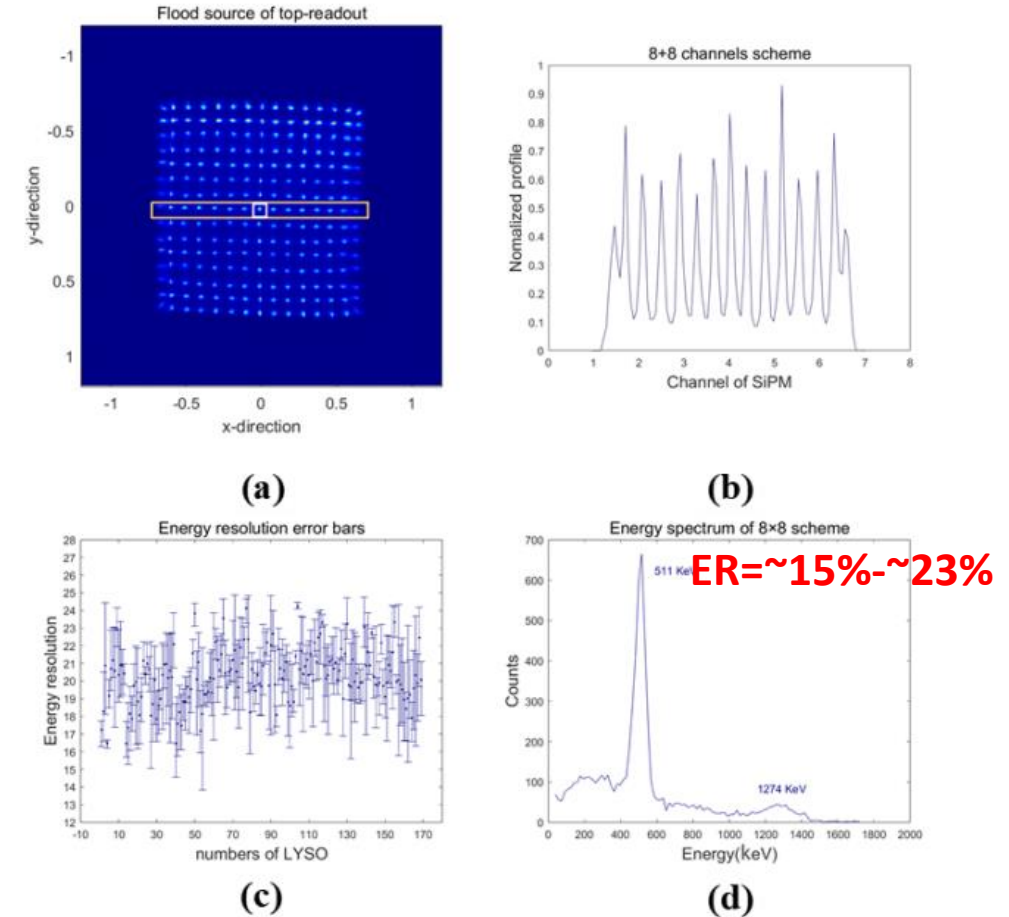


Scintillator array: (1) 15x15 array of 1x1x20 mm³ LYSO bars;
(2) 15x15 array of 1.5x1.5x20mm³ LYSO bars ;
SiPM array: 8+8/8*8 array of 3x3 mm² SiPMs;
Electronics: 128-cha FPGA-dQDC circuit.



ER= $\sim$ 12% $\sim$ 18%

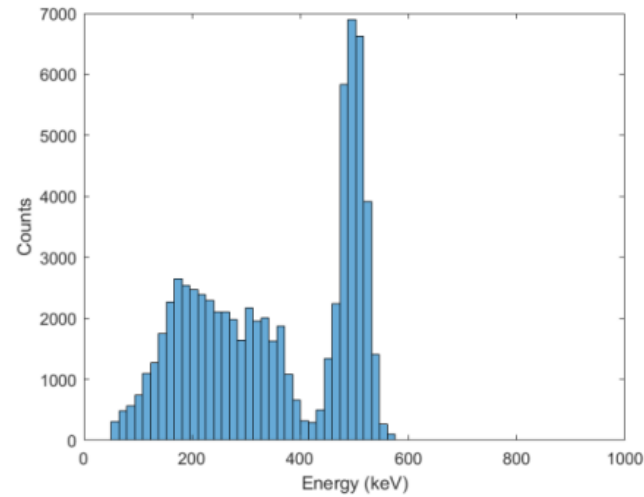
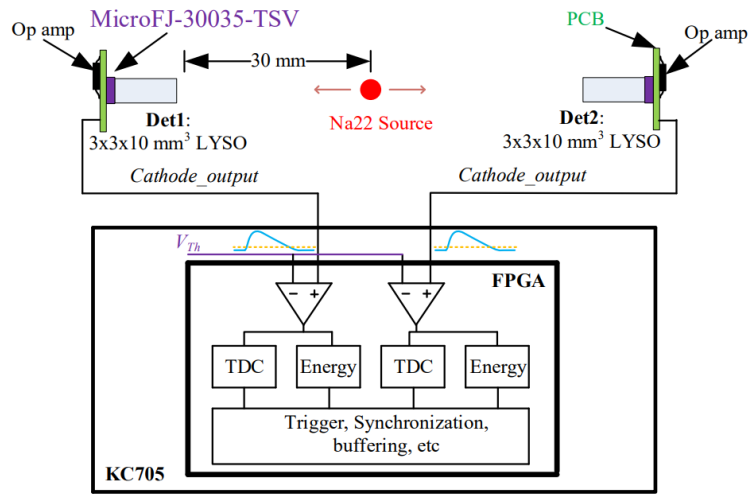
15x15 array of 1.5x1.5x20mm³ LYSO bars



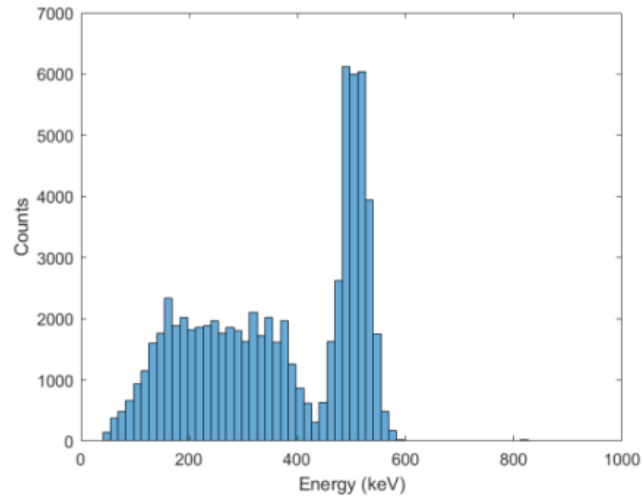
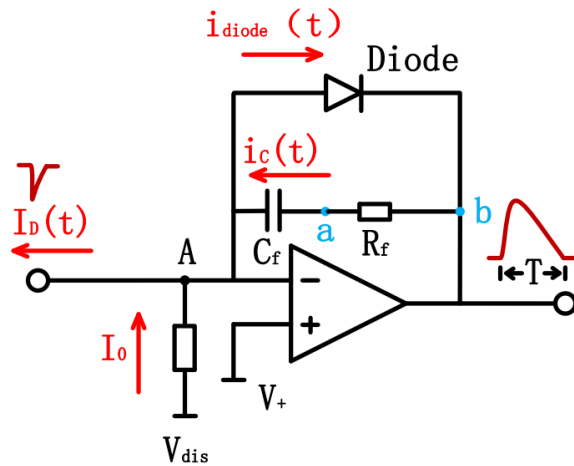
ER= $\sim$ 15% $\sim$ 23%

15x15 array of 1x1x20mm³ LYSO bars

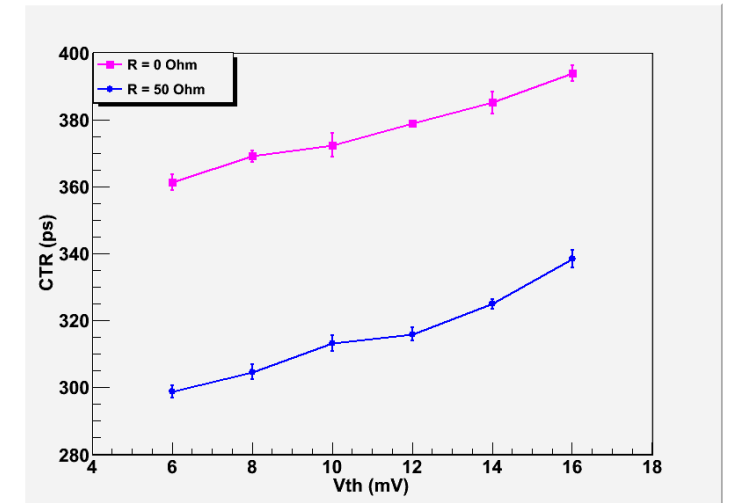
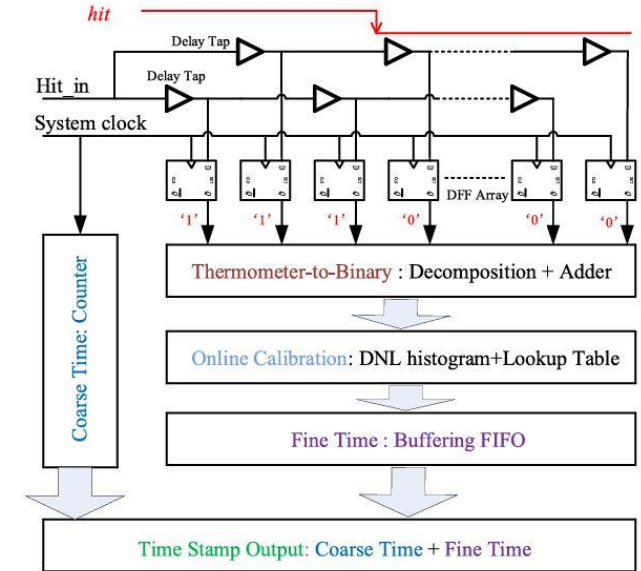
Timing performance evaluation



(a)



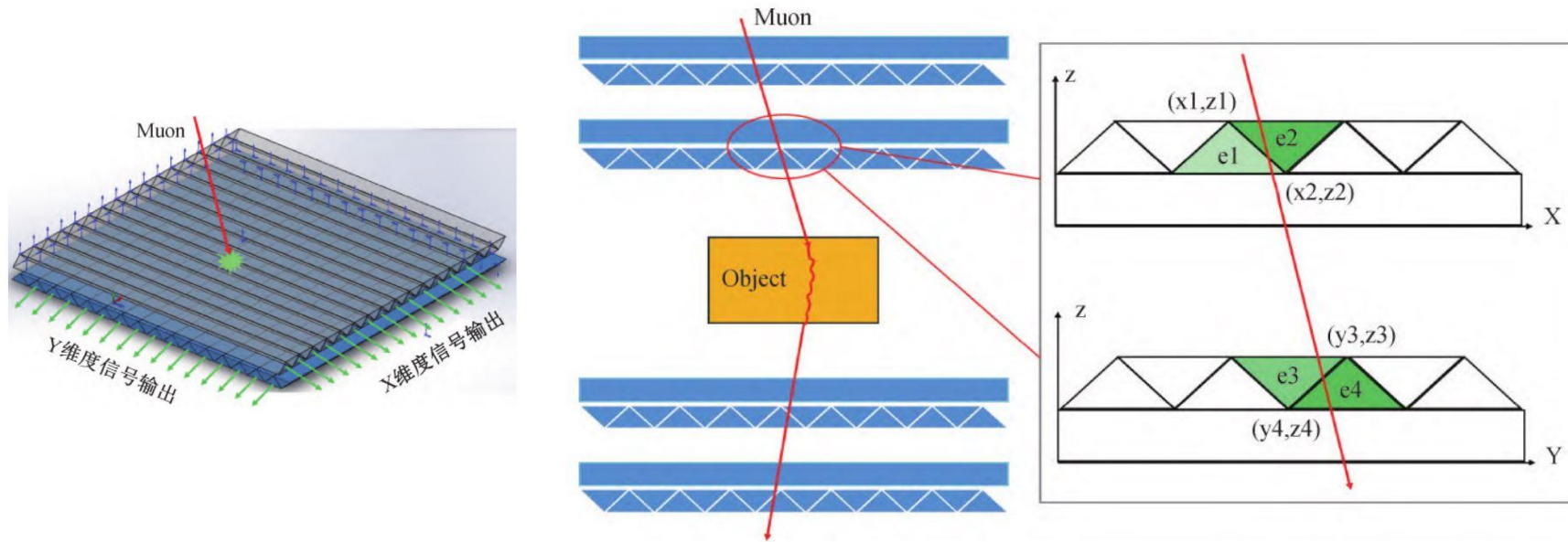
(b)



The ER can be lower than 10%

The CTR can be lower than 300 ps

Application 2: Muography

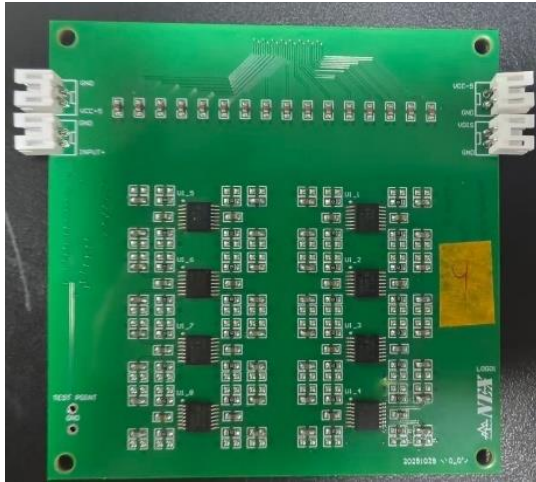


$$x = \frac{E_1 x_1 + E_2 x_2}{E_1 + E_2}, z = \frac{E_1 z_1 + E_2 z_2}{E_1 + E_2}$$

$$y = \frac{E_3 y_3 + E_4 y_4}{E_3 + E_4}, z = \frac{E_3 z_3 + E_4 z_4}{E_3 + E_4}$$

□ The scintillators :

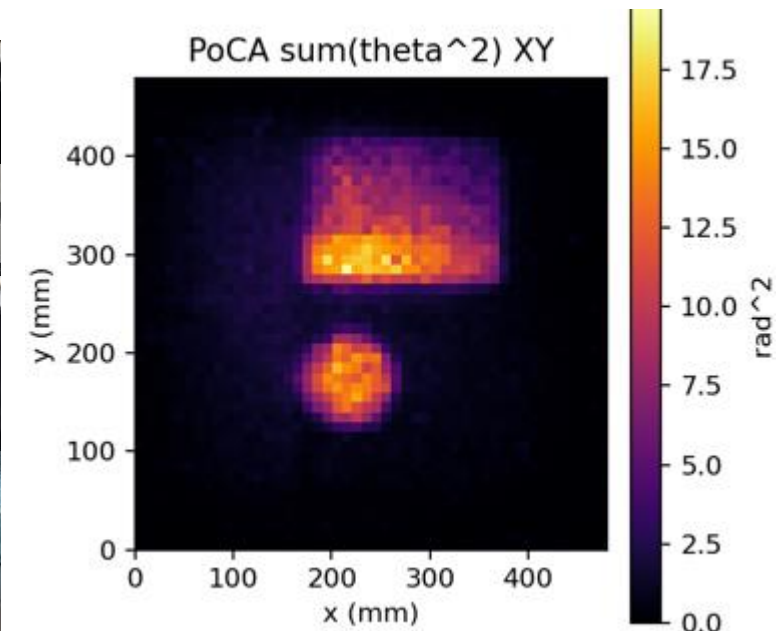
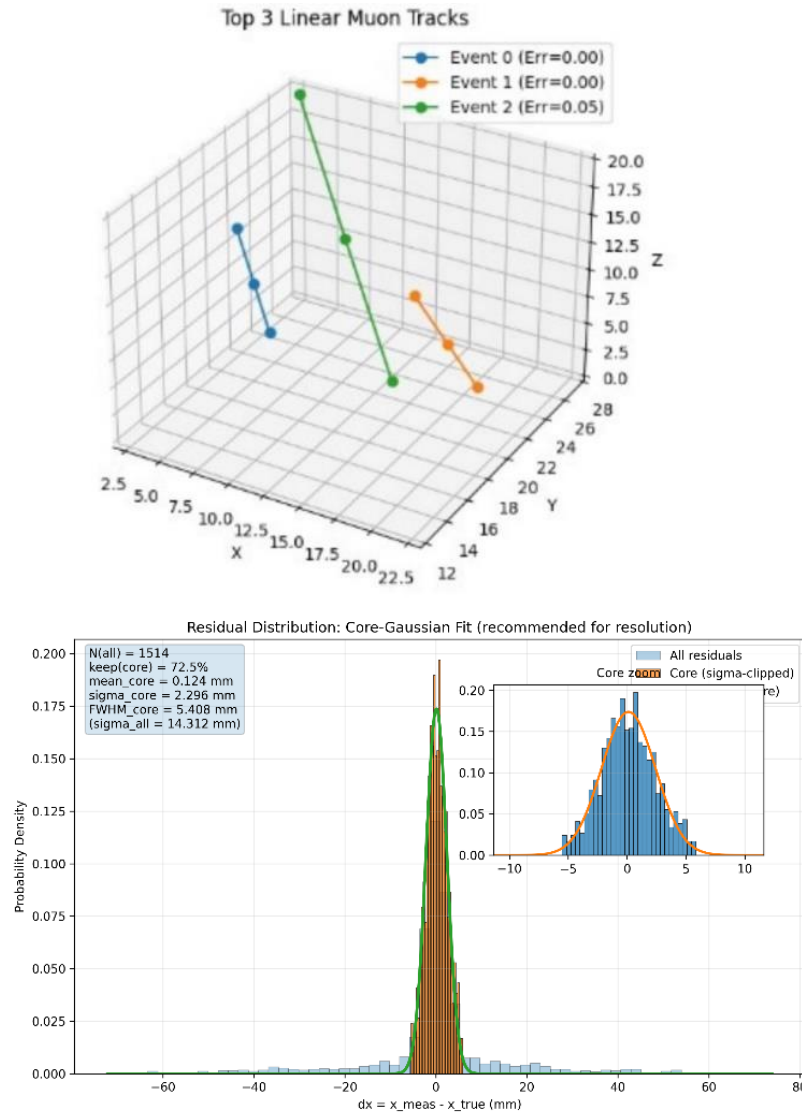
- ✓ triangular cross-section:
- ✓ arranged in an overlapping configuration along the X and Y directions.
- ✓ charge centroid method for muon hit position reconstruction。



64-cha FPGA-QTC circuit

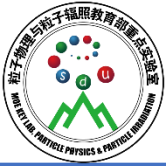


Muography device



Position resolution $\sim 2.2 \text{ mm}$

A Lead ball (dia $\sim 10\text{cm}$) and two lead bricks (20cm x 10cm x 5cm) are used for scattering imaging.



- ✓ Developed compact FPGA-QDC/QTC system for SiPM based radiation detector;
- ✓ Applied to electronics system for PET and muography;
- ✓ In the future, we plan to achieve more channels of electronics system. The QDC/QTC based ASIC is another option.

Thanks for your listening!