

Resistive Micromegas for Future Collider Experiments

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on behalf of the RHUM collaboration:

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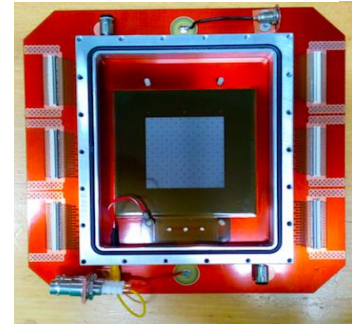
The RHUM project

- Project born and grown within RD51 and now well established inside DRD1 Collaboration
 - Collaboration between INFN-Roma Tre and INFN-Napoli, in partnership with INFN-Bari, CERN PBC Workshop and industry (ELTOS)
- Goal: develop a **MicroPatternGaseousDetector**, based on the **Micromegas** technology, able to work efficiently at particle rates up to **several MHz/cm²**
- Implement a **small pad readout** to reduce the occupancy
 - $O(\text{mm}^2)$ for high-rate capability and good spatial resolution in both coordinates
- Optimize the **spark protection resistive scheme** to achieve stable operation at high rate/gain
- Demonstrate the **detector scalability** to large surfaces
- **Technology transfer to reduce cost and allow large production**
- Demonstrate flexibility for medium-to-low rate applications (e.g. FCC-ee muon detectors) using charge capacitive-sharing readout



RHUM

**Resistive
High
granularity
Micromegas**



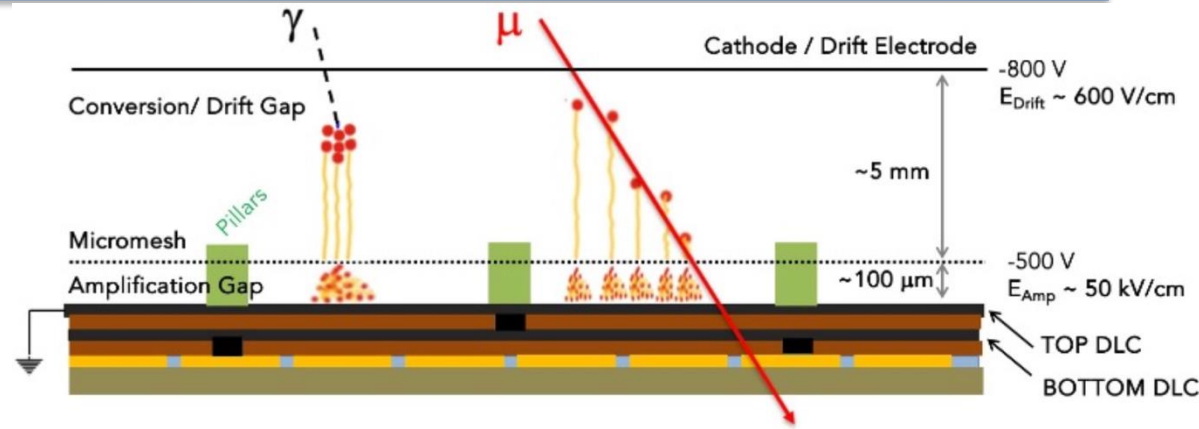
Micromegas technology

- Resistive Micromegas technology
→ cover readout copper strip/pad with a resistive insulator to suppress discharges

- Drift region of $\sim 5\text{ mm}$ width
(→ $E \sim 60\text{ V/mm}$) and

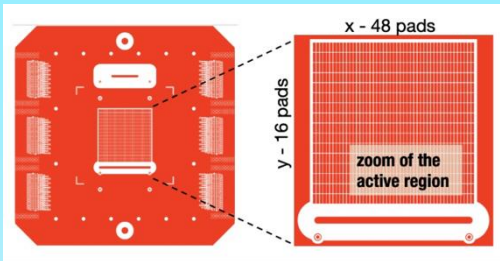
Amplification region of $\sim 100\text{ }\mu\text{m}$ ($E \sim 5\text{ kV/mm}$) separated by a metallic micro-mesh, supported by small size (sub-mm) diameter pillars

- Geometrical and electrical configuration to guarantee a **fast charge evacuation**
 - fundamental for high-rate applications
- Extensively studied **different solutions for the resistive layout** on small prototypes
 - **Optimal configuration**: Double layer of resistive foils based on Diamon Like Carbon (DLC) structures connected through conducting vias – DLC foil resistivity of $20\text{--}40\text{ M}\Omega/\square$
- Demonstrated to be a **solid detector technology for HEP experiments**

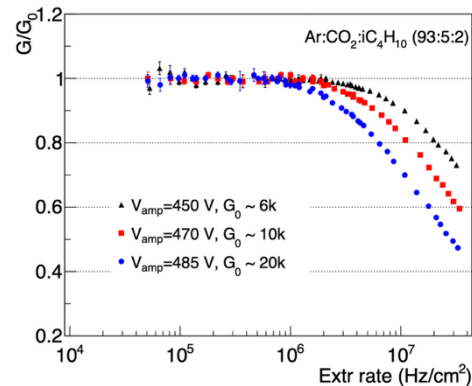


The prototypes size evolution & key performances

Small-size prototypes

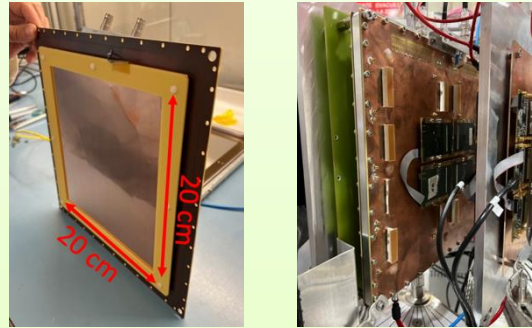


Active area: $4.8 \times 4.8 \text{ cm}^2$
active region

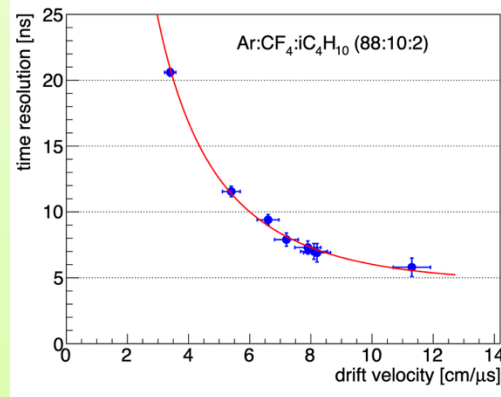


Very good rate capability with stable gain up to 10 MHz/cm^2

Medium-size prototypes

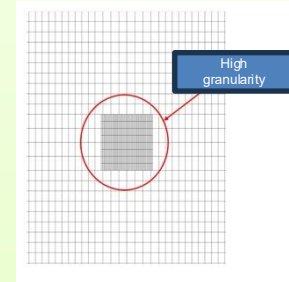


Active area : $20 \text{ cm} \times 20 \text{ cm}$

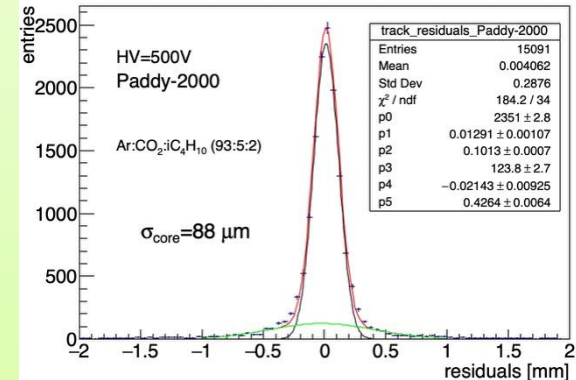


Measured resolution for the medium size prototype $\sim 6 \text{ ns}$ at $v_{\text{drift}} \sim 11 \text{ cm}/\mu\text{s}$

Large-size prototypes



Active area : $50 \text{ cm} \times 40 \text{ cm}$

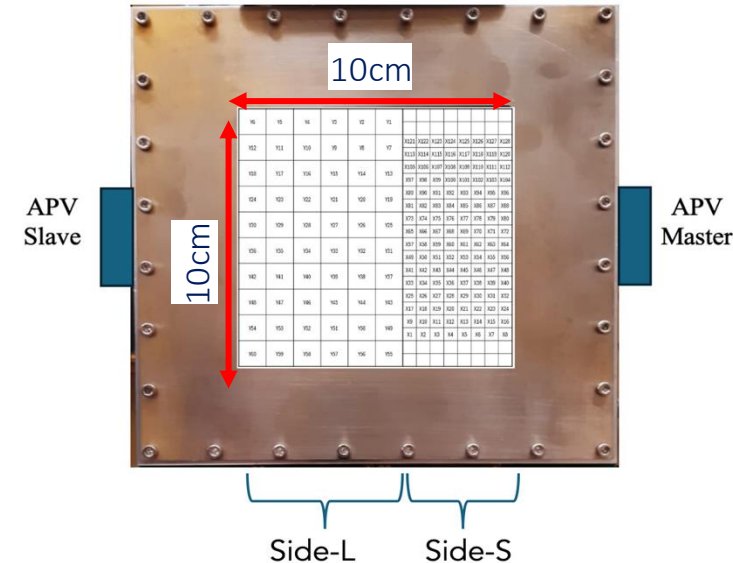
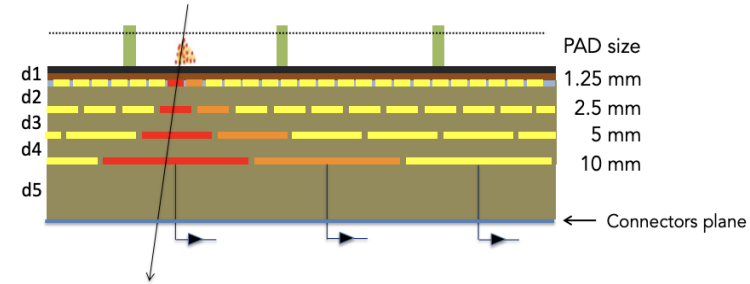


Efficiency and resolution performances for the large size prototype preserved wrt small prototypes

Prototype implementing the capacitive sharing

Concept from R. De Oliveira and K. Gnanvo et al.,
NIMA 1047 (2023) 167782)

- **Capacitive coupling** between stacked pad layers spreads the signal over coarse readout pads.
- Small internal pads set the charge-sharing scale. Only the last layer connects to the electronics.
- First $10 \times 10 \text{ cm}^2$ prototype: a **single DLC resistive layer**, suitable for low- and medium-rate applications



Pad size of “top-layer” (signal induction): $1.25 \times 1.25 \text{ mm}^2$

Two different readout regions :

Side-L: 3 sharing layers , $10 \times 10 \text{ mm}^2$ readout:

$1.25 \times 1.25 \text{ mm}^2 \rightarrow 2.5 \times 2.5 \text{ mm}^2 \rightarrow 5 \times 5 \text{ mm}^2 \rightarrow 10 \times 10 \text{ mm}^2$

Side-S: 2 sharing layers + $5 \times 5 \text{ mm}^2$ readout:

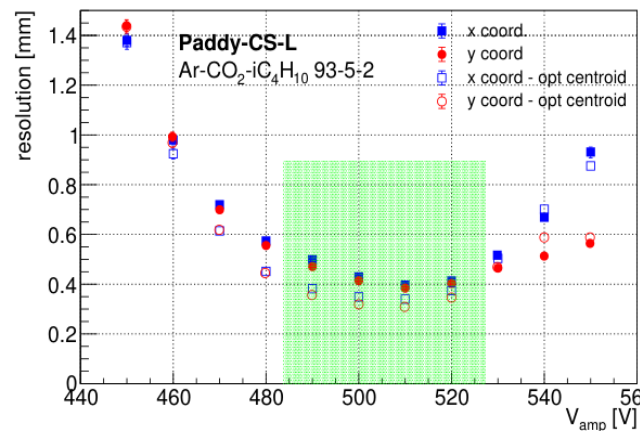
$1.25 \times 1.25 \text{ mm}^2 \rightarrow 2.5 \times 2.5 \text{ mm}^2 \rightarrow 5 \times 5 \text{ mm}^2 \rightarrow 5 \times 5 \text{ mm}^2$

[JINST 21 P03017](#)

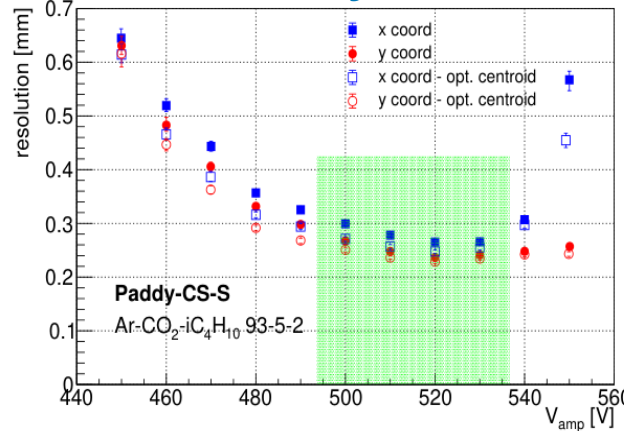
Performances for small-size prototype

- **Resolution** measured in the region with **large pads (Paddy-CS-L)** $\sim 320\mu\text{m}$
 - factor $\sim 1/30$ of the readout pad size
- **Resolution** measured in the region with **small pads (Paddy-CS-S)** $\sim 250\mu\text{m}$
 - factor $\sim 1/20$ of the readout pad size
- **Efficiency for perpendicular tracks** at **$\sim 98\%$** , comparable with the prototypes non implementing the capacitive sharing

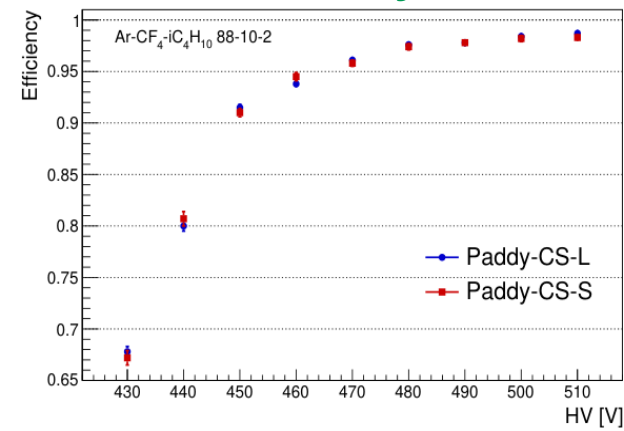
Paddy-CS-L



Paddy-CS-S



Efficiency

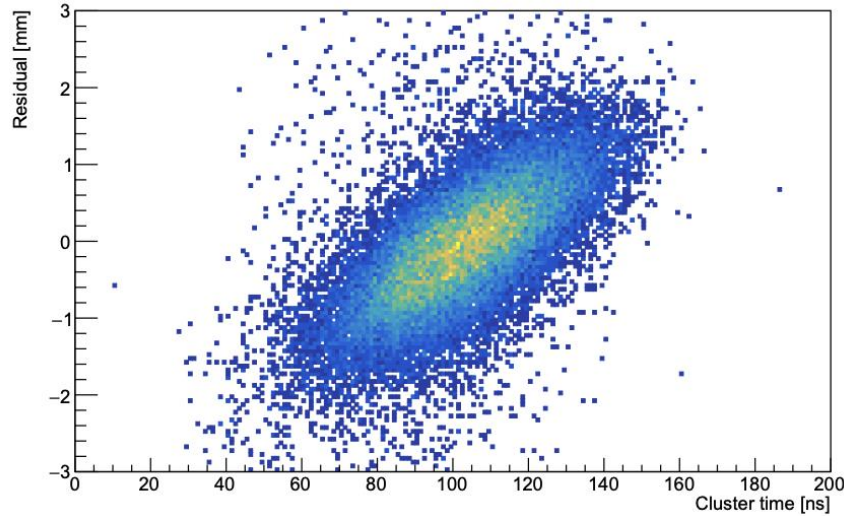


- **Channel count reduced by factors 64 (L) and 16 (S), relative to a fully instrumented $1.25 \times 1.25 \text{ mm}^2$ readout layer**

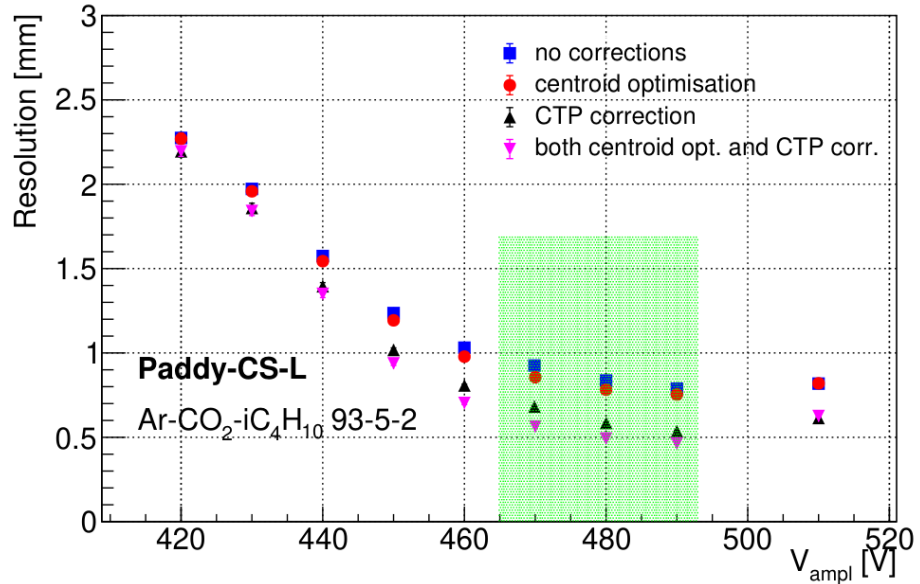
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Performances with inclined tracks

- Performance of the first micromegas-CS prototype also tested with TB data collected with the detector rotated by $\sim 38^\circ$



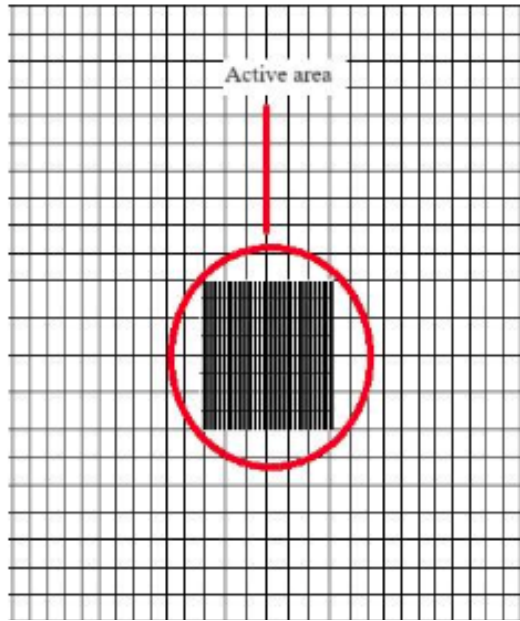
- Cluster Time Projection (CTP) uses the correlation between cluster time and centroid bias.
- The correction depends on the track angle (measured e.g. from external tracker)



- Resolution below 500 μm** with CTP ($\sim 40\%$ improvement) – 1/18 of the pad size
- Efficiency above 99%** at plateau (effect of pillar dead region reduced with inclined tracks)

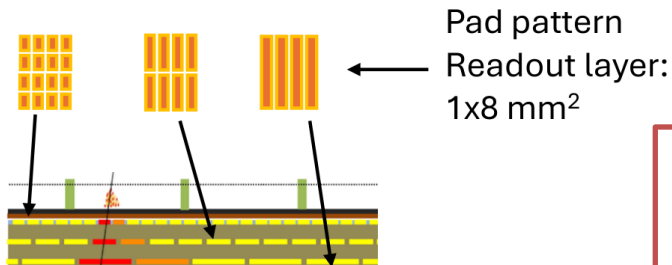
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Capacitive sharing over large areas



- Prototypes with **different pad geometries** and multilayer **capacitive layouts** have been developed and tested in test-beam campaigns performed in 2025–2026
- **Implemented the CS concept** in a **larger area** prototype
 - Design developed on top of the 50x40 cm² double DLC prototype
- **Outer region:** 10 × 10 mm² readout pads with a 2.5 × 2.5 mm² internal pad layer (2.5 × 2.5 mm² → 5 × 5 mm² → 10 × 10 mm²)
- **Central region:** two sharing layers to spread charge along the y direction (while the x direction unchanged)
 - This CS layout targets applications where a better precision is needed alongside one coordinate compared to the other (e.g., momentum measurement in a magnetic field)

1st layer: 1x2 mm² 2nd layer: 1x4 mm²

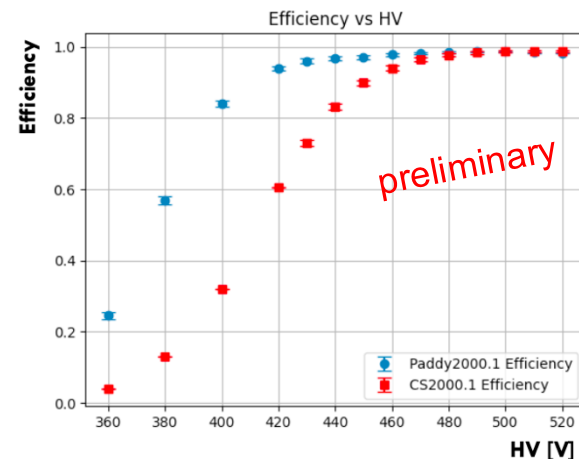
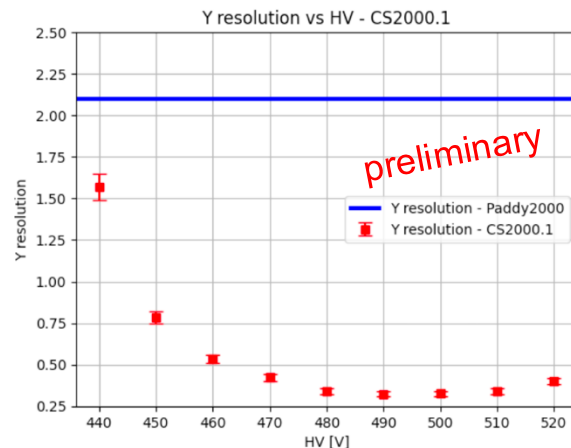
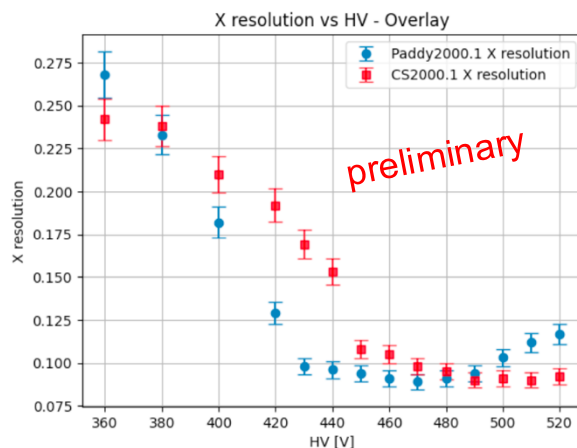


Capacitive-sharing layout

Internal region :	1x2 mm ²
Sharing layer. :	1x4mm ²
Readout layer :	1x8mm ²

Capacitive sharing over large areas

- Performance comparison performed between the the 50x40cm² detector implementing the CS and the the 50x40cm² detector without CS (Paddy 2000)



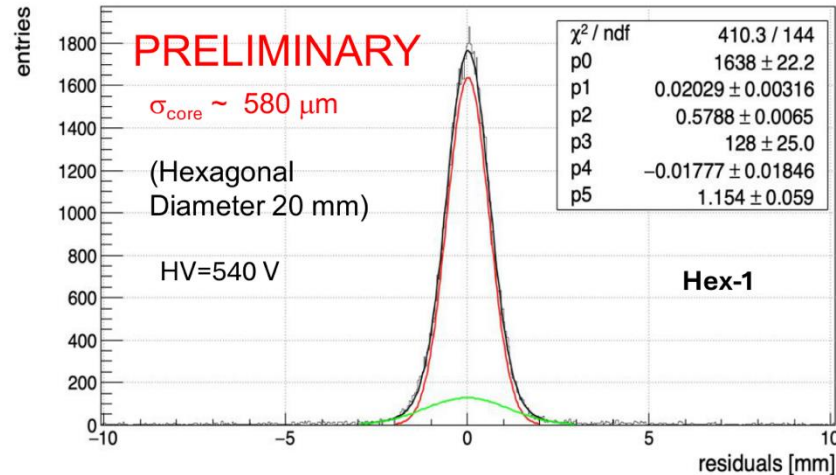
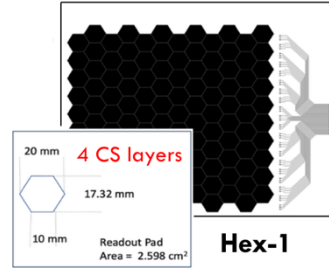
- Comparable **spatial resolution** alongside the **non-CS coordinate** of **~80 μm**
- Improved **spatial resolution** alongside the **CS coordinate** of **~300 μm**
- **Higher gains** are **needed to achieve the same performance** on the non-CS coordinate and similarly for the efficiency
 - Size of the shift currently under investigation
- **Resolution** in the **outer region** with 10x10 mm² pads **~500 μm** in both coordinates

Exploring hexagonal geometries

- Investigated also non-rectangular pad geometries
- Two prototypes with an active area of $\sim 20 \times 20 \text{ cm}^2$, single DLC, hexagonal pad

HEX-1

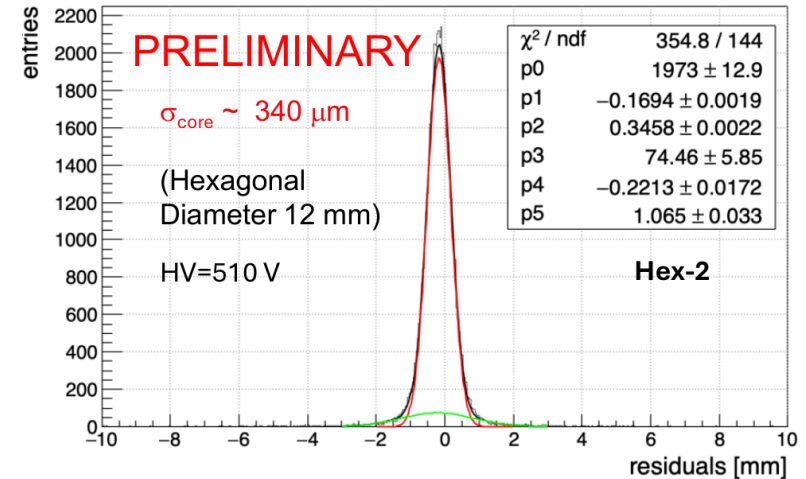
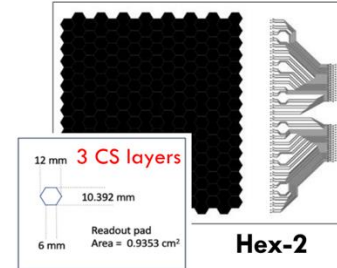
4 sharing layers + readout
20 mm pad diameter



Core width $\approx 580 \mu\text{m}$ at 540 V

HEX-2

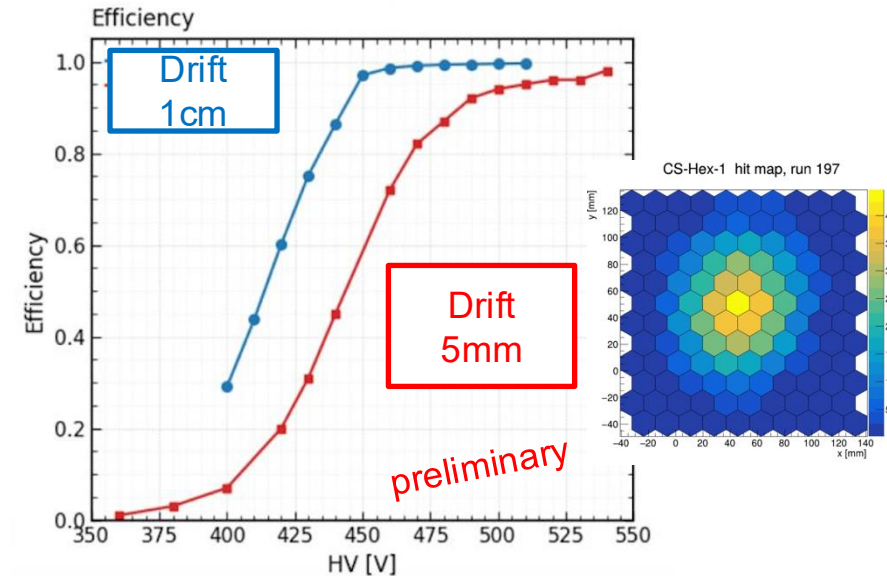
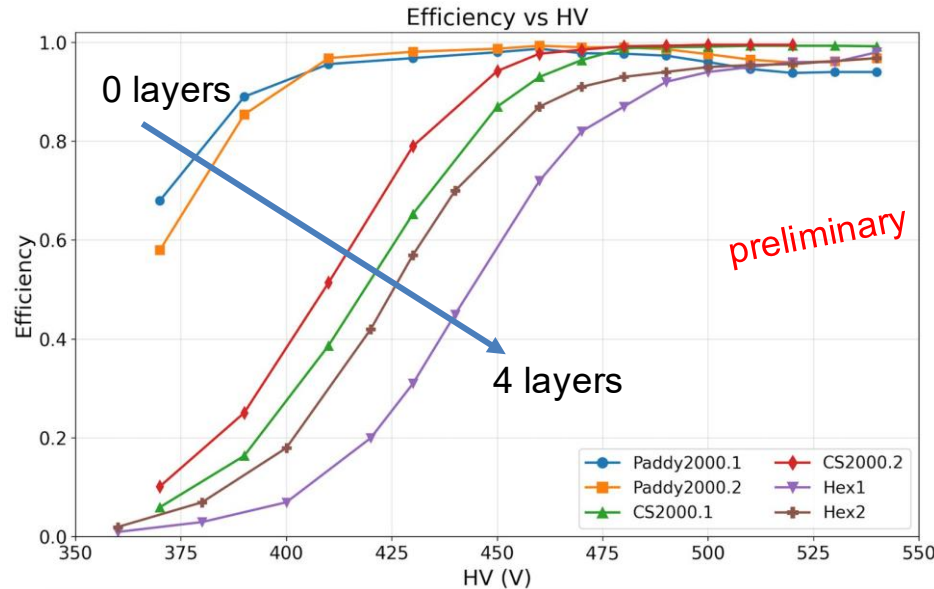
3 sharing layers + readout
12 mm pad diameter



Core width $\approx 340 \mu\text{m}$ at 510 V

Signal sharing and operation margin

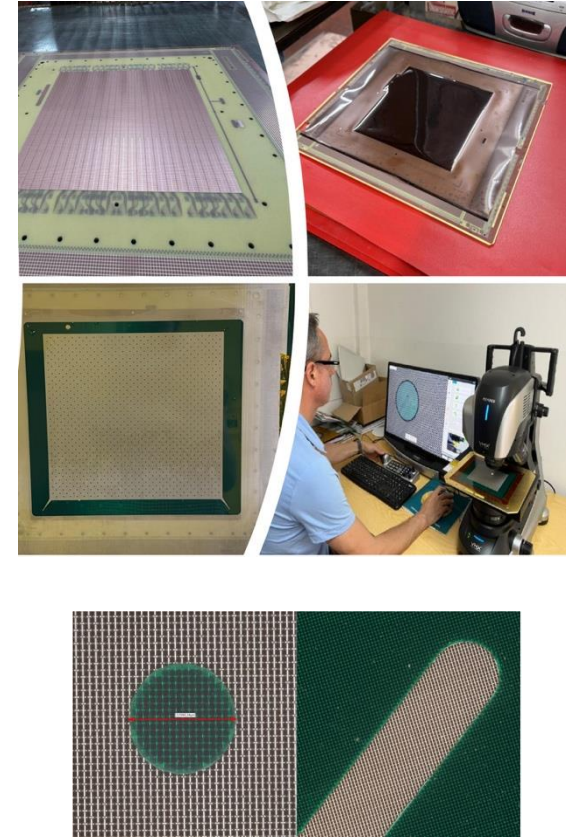
- In general, with more sharing layers the signal collected by the readout pad is reduced
- Higher gain recovers efficiency
 - The layer count is therefore a design parameter that influences operating voltage



- Efficiency plateau can be extended by increasing the primary ionization → increase drift gap
- Beam test results with 1cm drift gap (instead of 5mm) for **HEX1** chamber (4 layers)
 - Fully efficient ~98% @500V, resolution ~580 μ m (like the 5mm drift gap @ 540V)

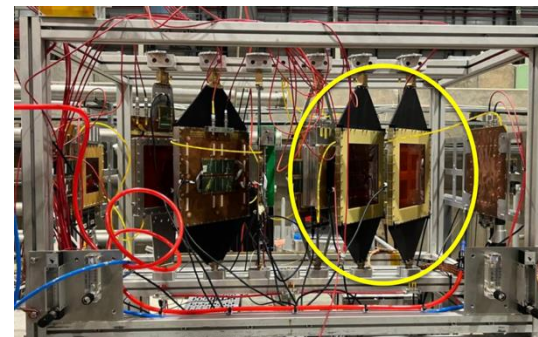
Technology Transfer to industry

- The Micromegas bulking process embeds the mesh in supporting pillars. This step requires **processes beyond standard PCB manufacturing**
- In 2022, we established a **collaboration with ELTOS S.p.A.**, a leading Italian PCB manufacturer already involved in the production of ATLAS Micromegas detectors
- The collaboration aims to **transfer the most critical manufacturing steps** to industry, simplifying and automating the process while potentially reducing costs
- Following the initial production of a small detector with a single DLC layer, a **new production batch** was completed at ELTOS in June 2026

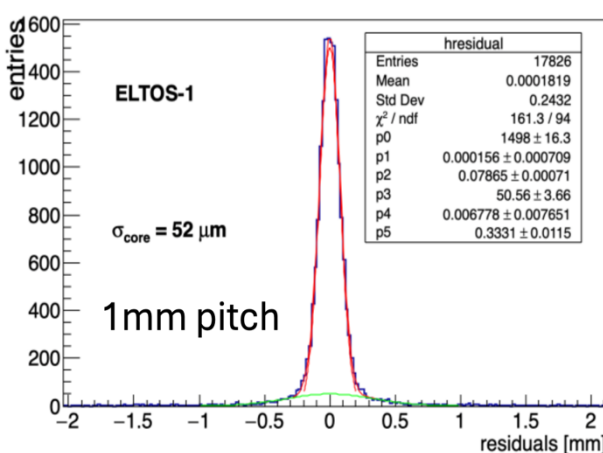


ELTOS 20x20cm² prototypes: beam-test results

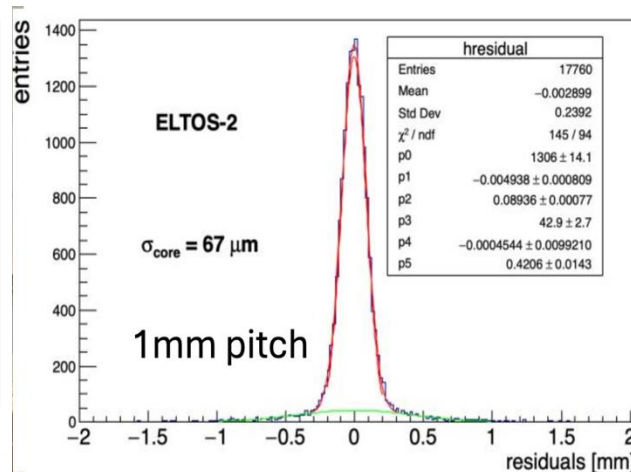
- Two industrial prototypes 20x20cm² with 1 x 8 mm² pads
- Layout similar to the 20x20cm² prototype built at CERN
 - Standard (no CS) readout , single DLC
- Preliminary results from beam-test campaign @ CERN in July 2026



ELTOS-1

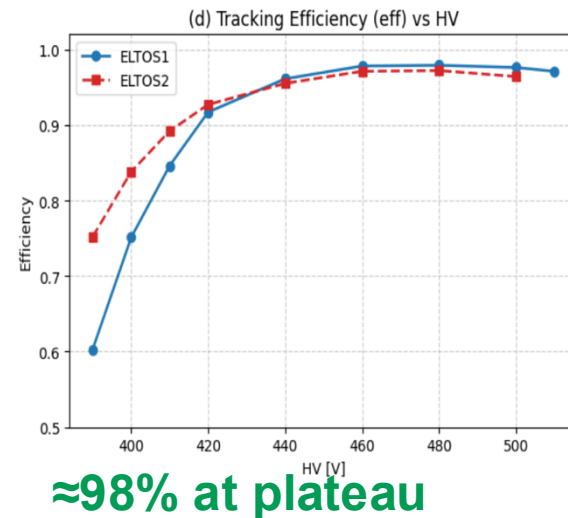


ELTOS-2



Spatial resolution ~60μm

Efficiency (0°)



- Comparable performances wrt 20x20cm² prototypes built at CERN PCB Workshop

- Several Small Pads Micromegas prototypes have been built employing different solutions for the resistive layout
 - Best performances for high-rate with Diamond-Like Carbon (DLC) resistive foils
- Performances achieved with prototypes up to 50x40cm²:
 - stable operation up to 20 MHz/cm² with gain >10⁴
 - detector efficiency > 97% (limited by pillars for $\perp$ tracks, ~100% otherwise)
 - position resolution < 100 μ m
 - Time resolution down to 6ns with fast gas mixture (@v_{drift} ~11cm/ μ s)
- Started exploring different layouts to cope with different requirements
 - Various prototypes built exploiting capacitive sharing concept for low-medium rate applications (FCC-ee oriented)
 - Very promising to maintain good spatial resolution and drastically decreasing the number of readout channels, to follow up the optimization according to specific requirements
- Design simplification and cost reduction on the way
 - Production of first working bulk micromegas prototypes at industry (ELTOS)
 - Very promising results. An essential step towards mass production for future large experiments.

Thank you!

Backup

- Cluster timing predicts centroid position bias:
 - Earlier than the central time $\rightarrow$ negative bias
 - Later than the central time $\rightarrow$ positive bias

Central time is the expected time for charge deposited halfway across the drift gap along the particle track.

