



Development of front-end electronics for the Belle II electromagnetic calorimeter upgrade

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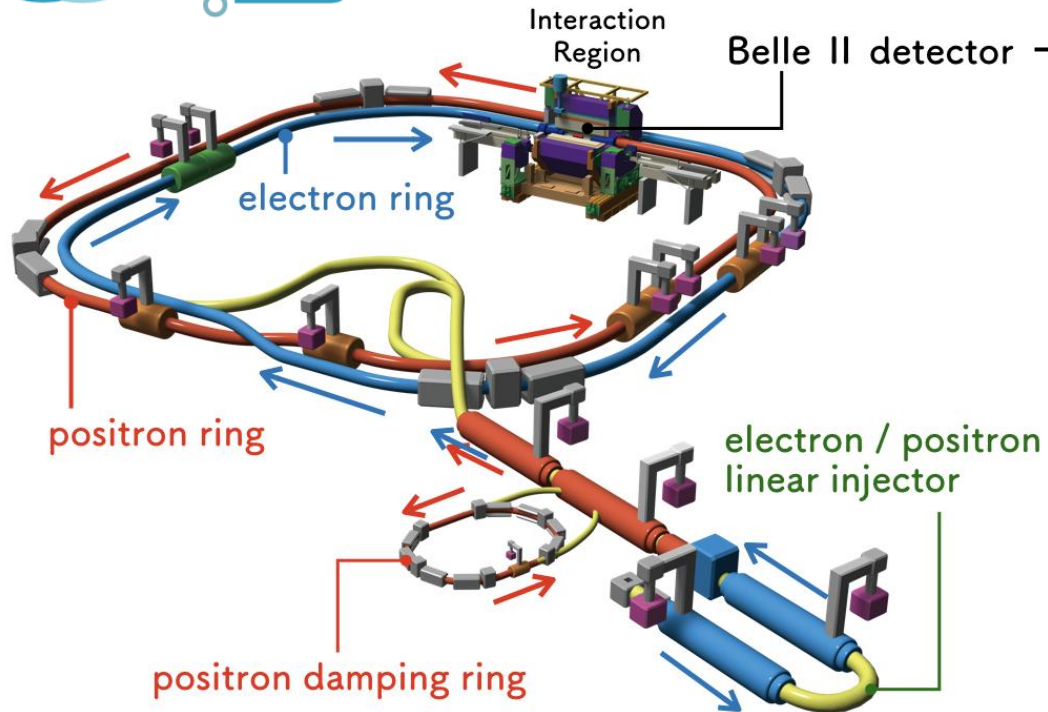
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Outline

- SuperKEKB and Belle II
- Calorimeter upgrade motivation, overview and simulation
- New front-end electronics board
 - Main components, first digitization tests
- Conclusions

SuperKEKB and Belle II



Pixel Detector (PXD)

Silicon Vertex Detector (SVD)

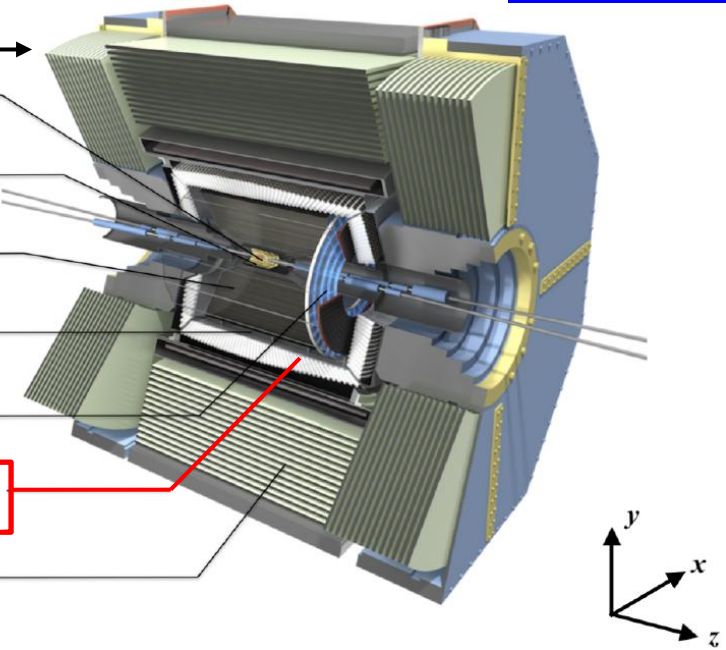
Central Drift Chamber (CDC)

TOP counter (TOP)

Aerogel RICH counter (ARICH)

Electromagnetic Calorimeter (ECL)

K_L^0 /Muon Detector (KLM)

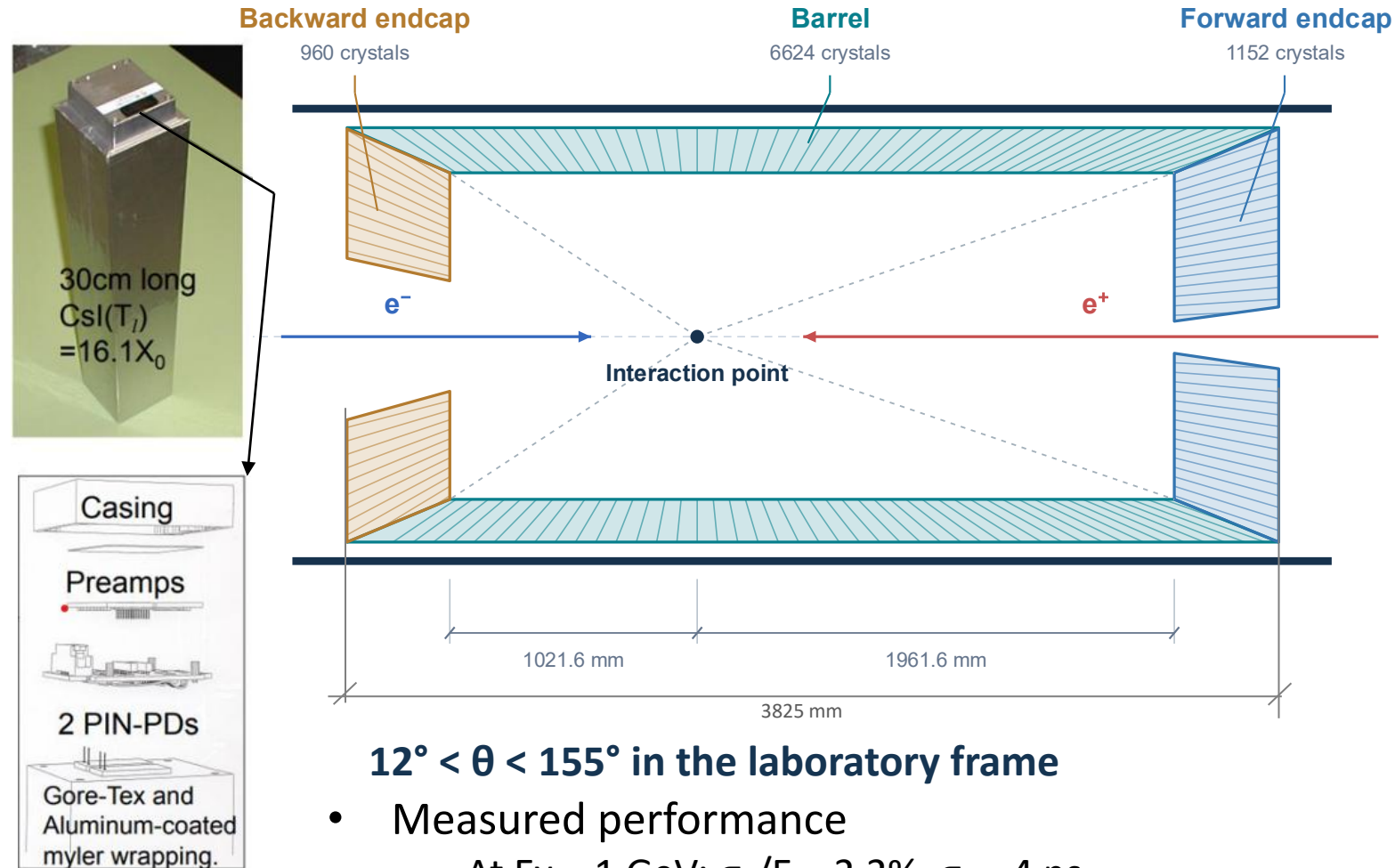


- SuperKEKB e^+e^- B factory @ KEK (Tsukuba, Japan)
 - e^+ 4 GeV (LER) + e^- 7 GeV (HER)
 - Target $L = 6 \times 10^{35} \text{ cm}^{-2} \text{ s}^{-1}$

- Belle II detector at beam collision point
- Physics beyond the Standard Model at the intensity frontier (CKM matrix elements, CPV studies, rare B,D, τ decays, and more)

The Electromagnetic Calorimeter (ECL)

- 8736 CsI(Tl) crystals read out by PIN photodiodes
- $\sim 1 \mu\text{s}$ scintillation decay makes pile-up noise rejection essential $\Rightarrow$ waveform sampling
- Goals
 - Measure photon energy, direction and time from $\sim 20 \text{ MeV}$ to 7 GeV
 - Electron identification, neutral trigger and online luminosity monitoring
- More details in the [talk by A. Kuzmin](#)

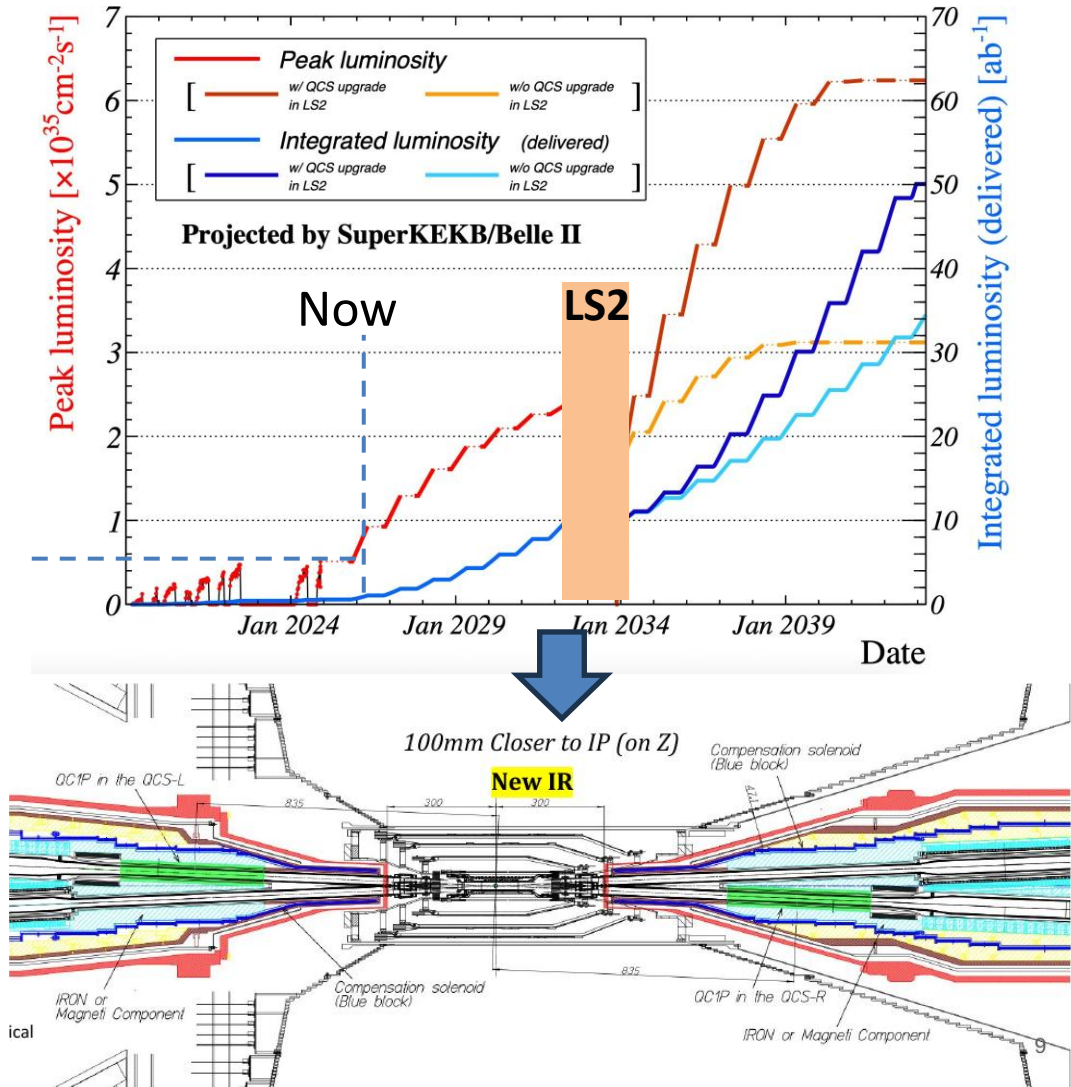


$12^\circ < \theta < 155^\circ$ in the laboratory frame

- Measured performance
 - At $E_\gamma \approx 1 \text{ GeV}$: $\sigma_E/E = 2.2\%$, $\sigma_t = 4 \text{ ns}$
 - π^0 mass resolution: $\sigma_m = 5.4 \text{ MeV}/c^2$

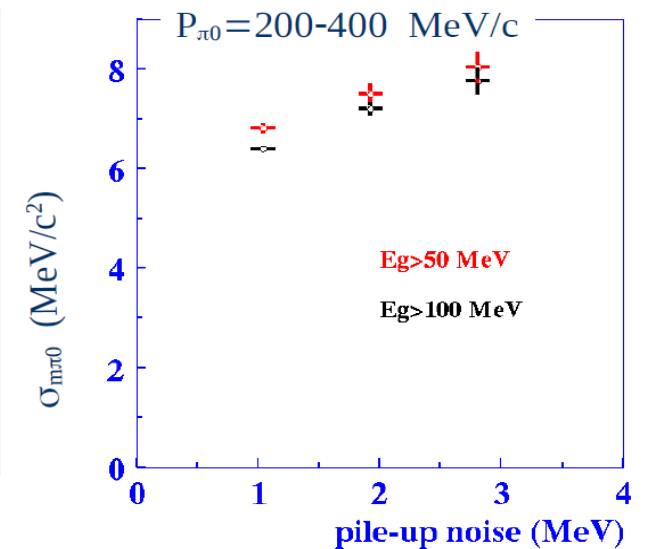
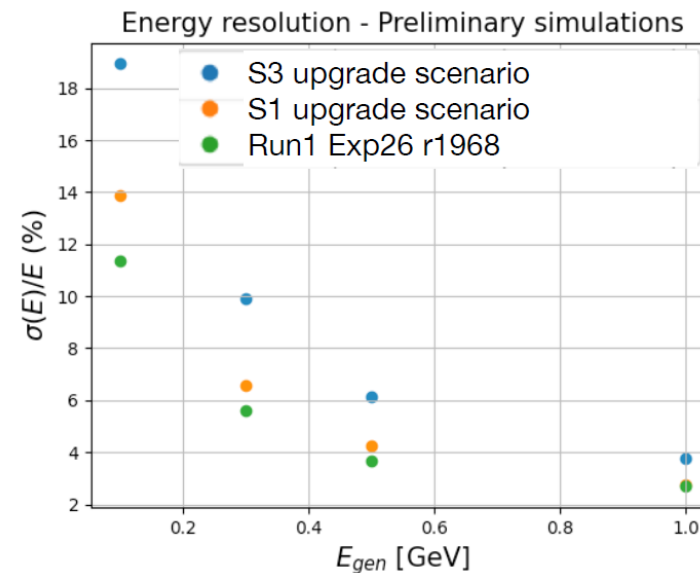
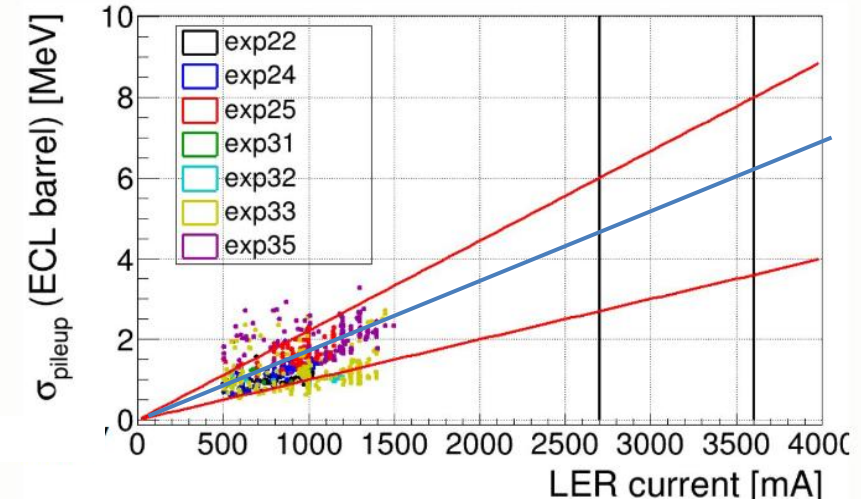
SuperKEKB Upgrade: Long Shutdown 2

- Achieved so far
 - Peak luminosity $5.32 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ (2026.06.30)
 - Belle II recorded 914 fb^{-1} (incl. off-resonance)
- Before Long Shutdown 2 (LS2), present run
 - Increase currents and reduce vertical β^*
 - Tune sextupoles and off-momentum optics
 - Improve injection, collimation and fast beam aborts
 - Goal luminosity: $2.4 \times 10^{35} \text{ cm}^{-2} \text{ s}^{-1}$
- LS2: new final-focus system, planned for 2032
 - Upgrade the interaction region and beam pipe
- After LS2, goals:
 - luminosity $6 \times 10^{35} \text{ cm}^{-2} \text{ s}^{-1}$
 - Integrated luminosity $\sim 50 \text{ ab}^{-1}$



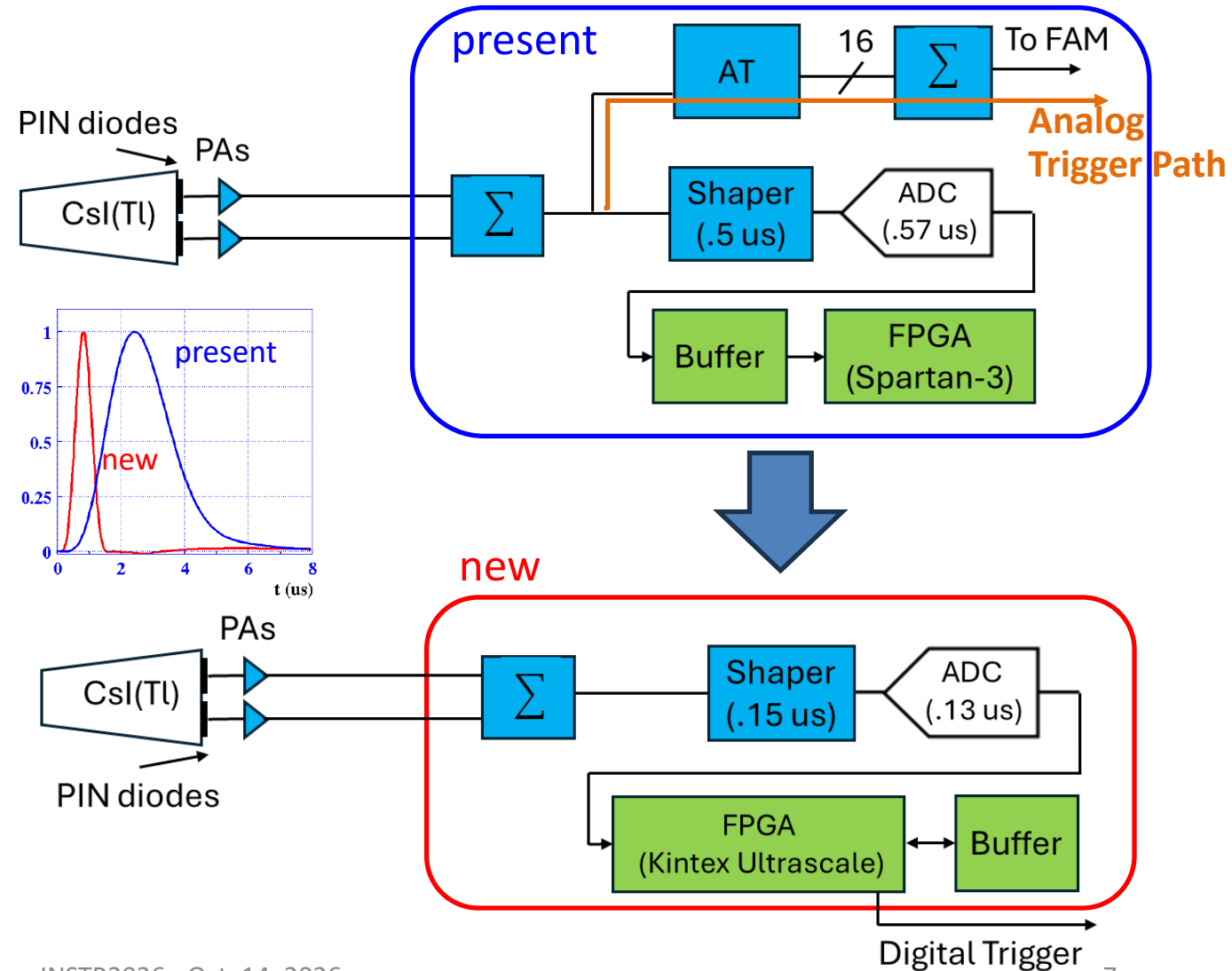
Impact of SuperKEKB Upgrade on ECL

- **Beam-induced background (BIB)** increases pile-up noise, which degrades ECL energy and timing resolution
- In “high” BIB scenarios after LS2, expected degradation of photon energy resolution below 1 GeV
- Increase per-crystal energy threshold mildly mitigates the effect
- Idea: faster signal shaping to reduce pile-up and improve energy/timing resolution



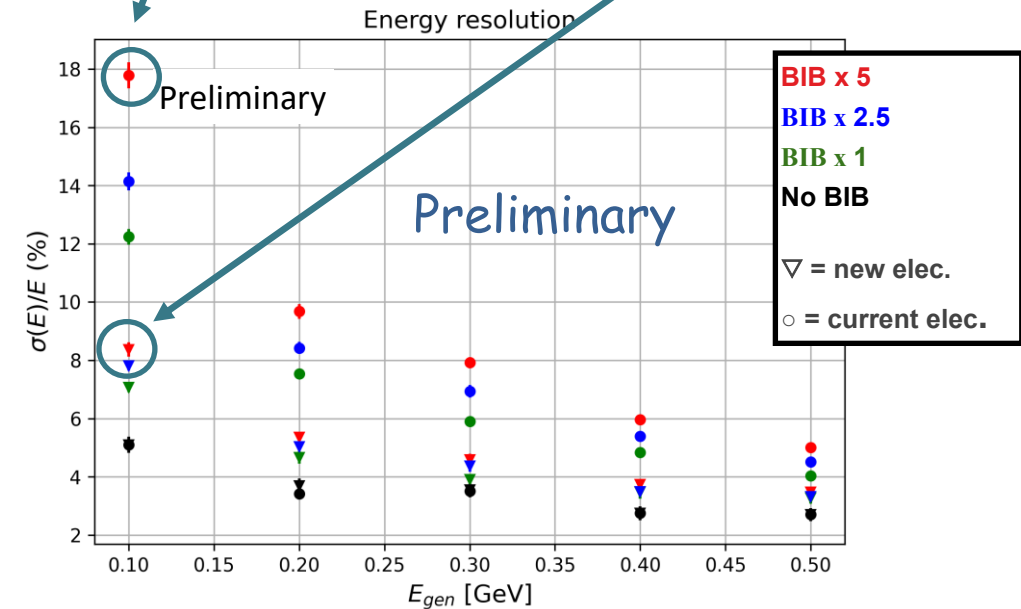
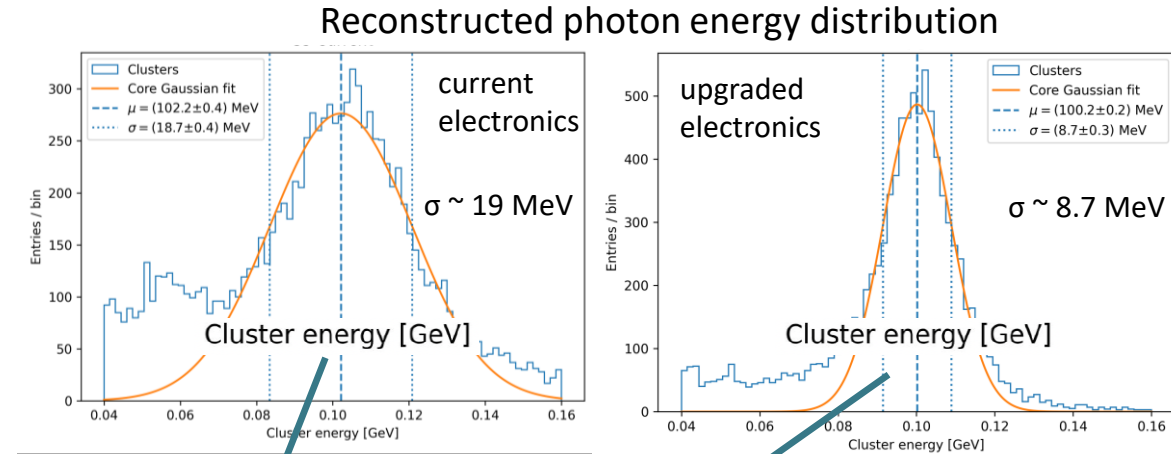
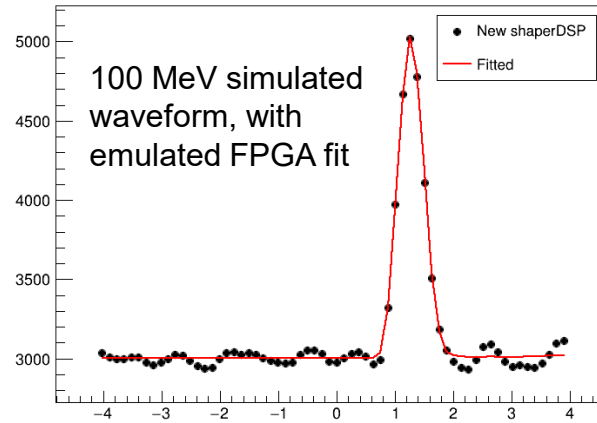
ECL Upgrade: Front-end Electronics

- Shaping time
 - 500 $\rightarrow$ 150 ns
- ADC sample rate
 - 1.7 $\rightarrow$ 7.9 MHz
- Trigger cell granularity
 - 4x4 $\rightarrow$ (down to) 1x1
- FPGA
 - Spartan-3 $\rightarrow$ Kintex UltraScale
- Both readout and trigger path become digital
 - Optical trigger links at ~ 3.5 Gbps



Simulation Studies

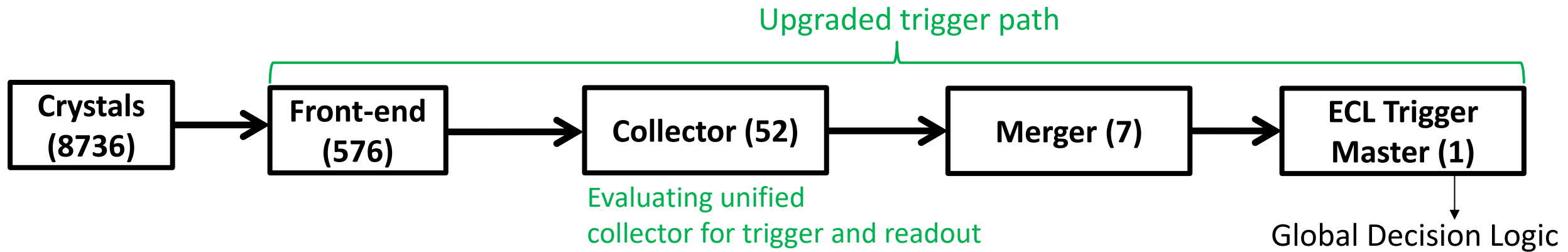
- Simulation and reconstruction with upgraded electronics included in Belle II analysis software framework (BASF2)
- Reconstructed photon energy resolution w/ upgraded vs current electronics
 - in high BIB post-LS2 scenarios: upgraded electronics improves approximately by 2x
 - without BIB, energy resolution for new and current electronics is compatible as expected



BIB scenarios defined in Table 3.3 of <https://arxiv.org/pdf/2406.19421>

ECL Electronics Upgrade: Trigger Chain

- New front-end board → new trigger chain
 - Several trigger path topologies being considered



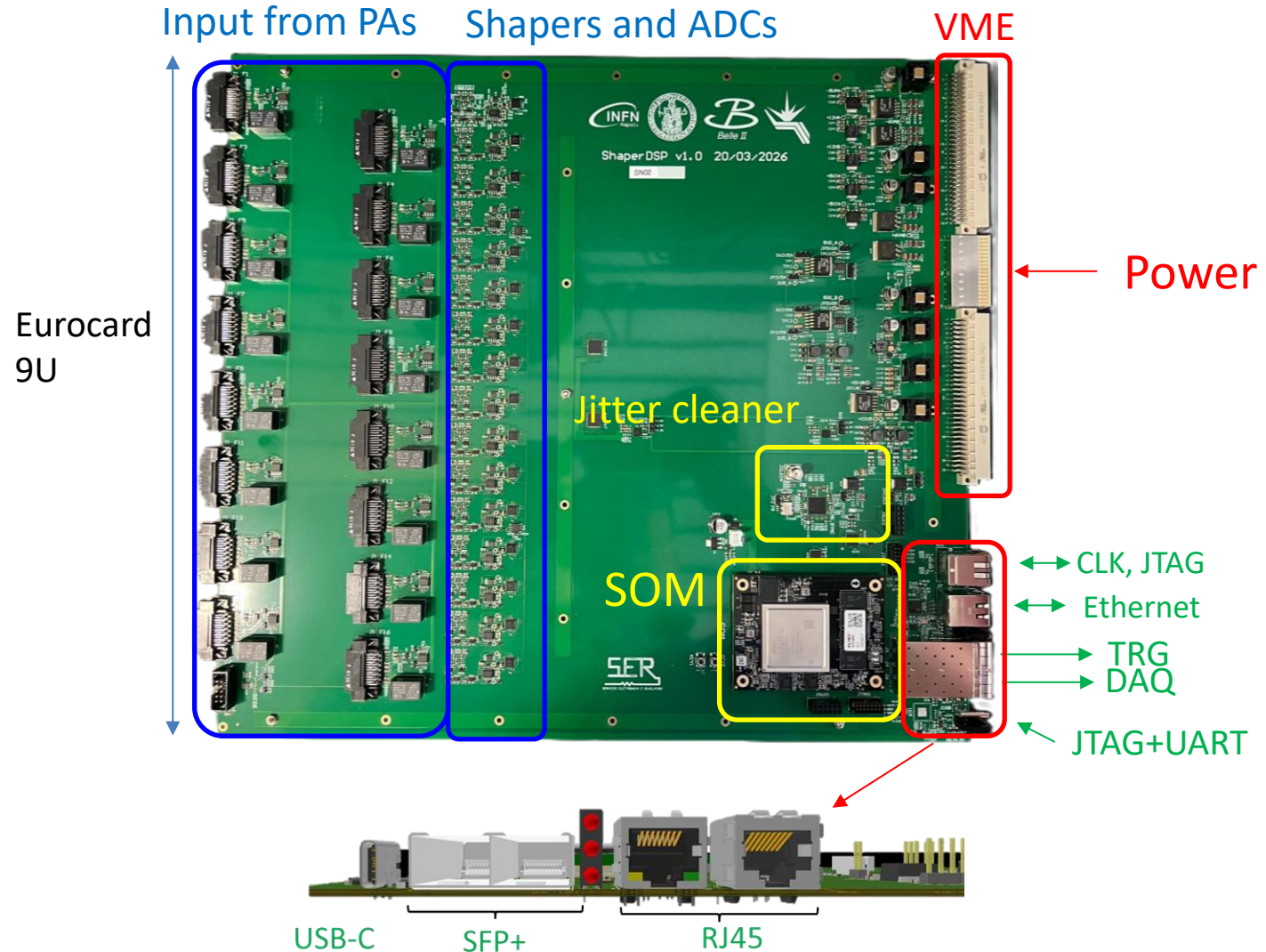
Data payload size for 1 crystal

1 bit (hit) + 7 bits (timing, LSB=1ns) + 18 bits (energy, LSB=0.05 MeV) = 26 bits

Option under study: trigger cells with 1 x 1, 1 x 2 or 2 x 2 sizes

A SOM-based Front-end Board: ShaperDSP

- Detector-interface and form factor retro-compatible
- 16 channels per board
- System-on-Module (Alinx ACKU040)
- 18-b 10-MSps ADCs (LTC2386-18)
- Jitter cleaner (LMK04828)
- CPLD (MachXO3LF-2100)
- 2 SFP+ cages for optical links
 - up to 10 Gbps per link, routed to two GTHs
- 2 RJ45
 - Gigabit Ethernet PHY + custom interface for retro-compatibility
- 1 USB-C w/ 4 independent channels (2 UART + 2 JTAG)



ALINX ACKU040 System-on-Module

Key Features

- AMD/Xilinx Kintex Ultrascale :

- ◆ 20nm FPGA fabric

- ◆ Up to 1.5M system logic units with Gen 2 3D ICSc

- ◆ 8.2 TeraMAC DSP Compute Performance

- ◆ Enhanced system logic unit packaging reduces dynamic power consumption

- Pluggable module with 4 x Panasonic board-to-board connectors

- 4 GByte (64-bit) DDR4 SDRAM

- 2 x 16 MB QSPI Flash

- Conservative FPGA choice for potential radiation-related issues
 - UltraScale+ family discarded due to SELs [1,2], for UltraScale no SELs observed [3,4]

Serial output to trigger/readout paths

- Gigabit transceivers

- ◆ 20 x GTH, up to 16.3 Gbps

- User I/Os

- ◆ 359 FPGA I/Os (104 3.3v + 255 1.8V)

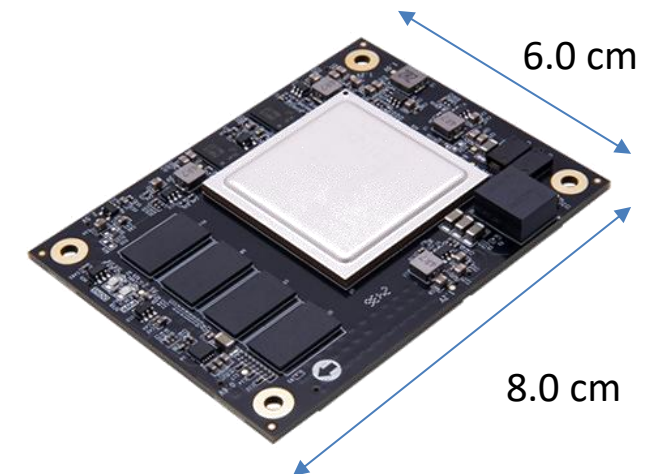
- Work temperature range of -40°C to +85°C

- 12V single supply

- Dimensions: 80 x 60 mm form factor

Serial input from ADCs

AMD Kintex UltraScale
XCKU040 + 4 GByte DDR4



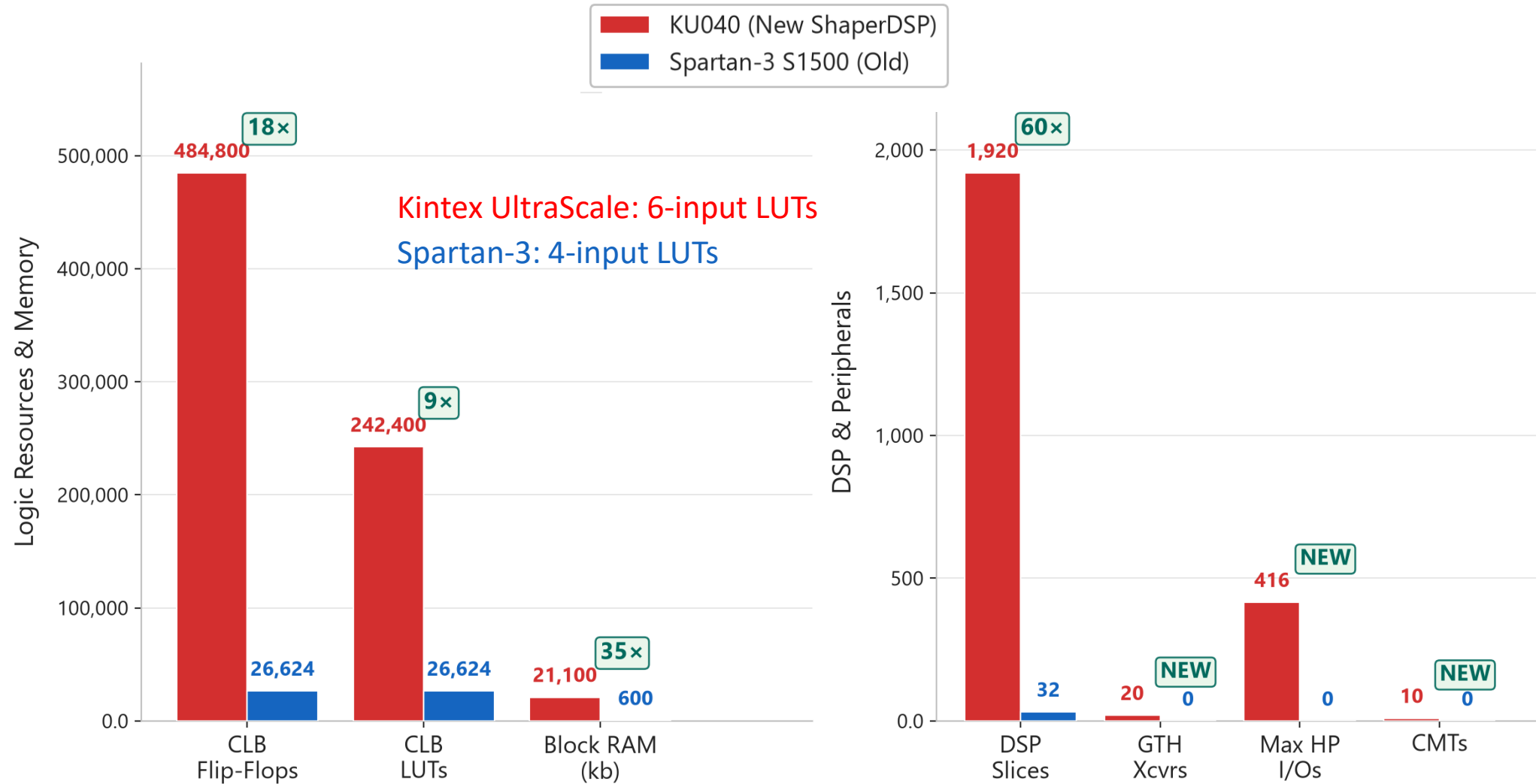
[1] DOI:[10.1109/NSREC.2018.8584313](https://doi.org/10.1109/NSREC.2018.8584313)

[2] DOI: [10.1109/NSREC.2018.8584296](https://doi.org/10.1109/NSREC.2018.8584296)

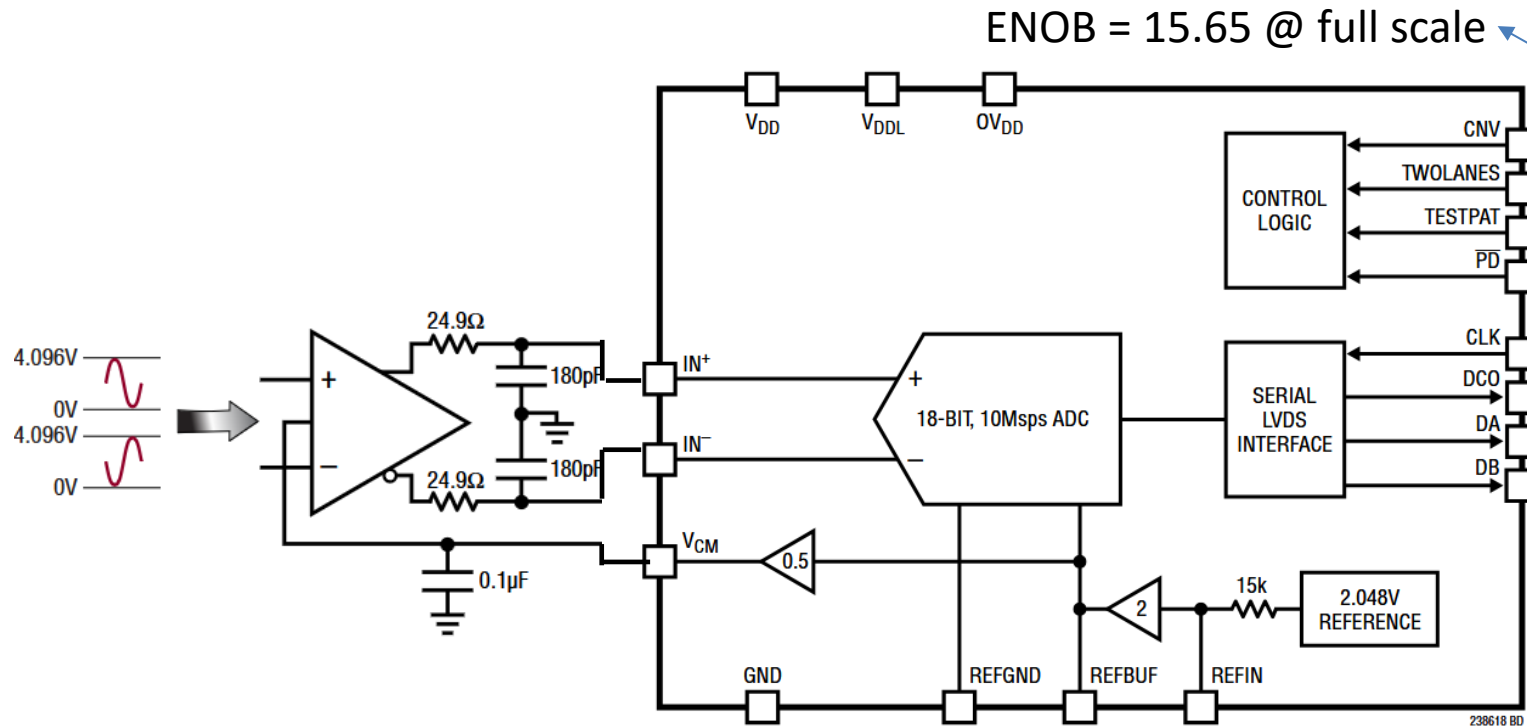
[3] <https://shorturl.at/VgGcK>

[4] <https://tinyurl.com/mrxfv438>

FPGA Logic Resources



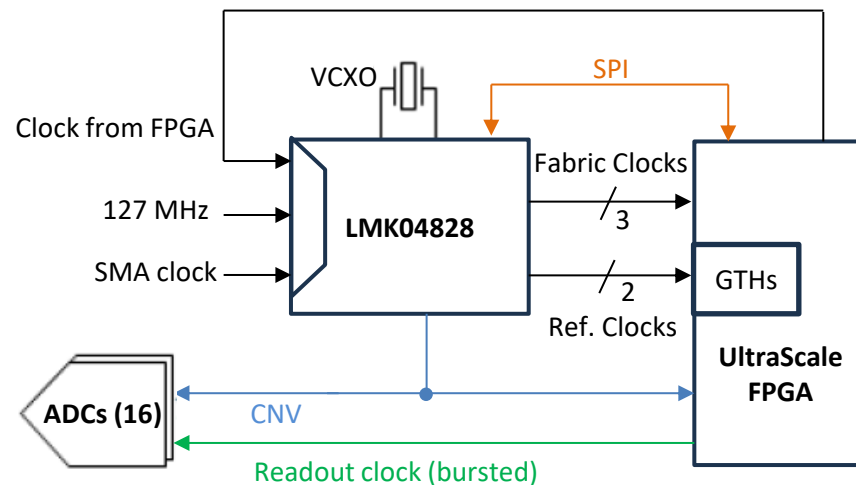
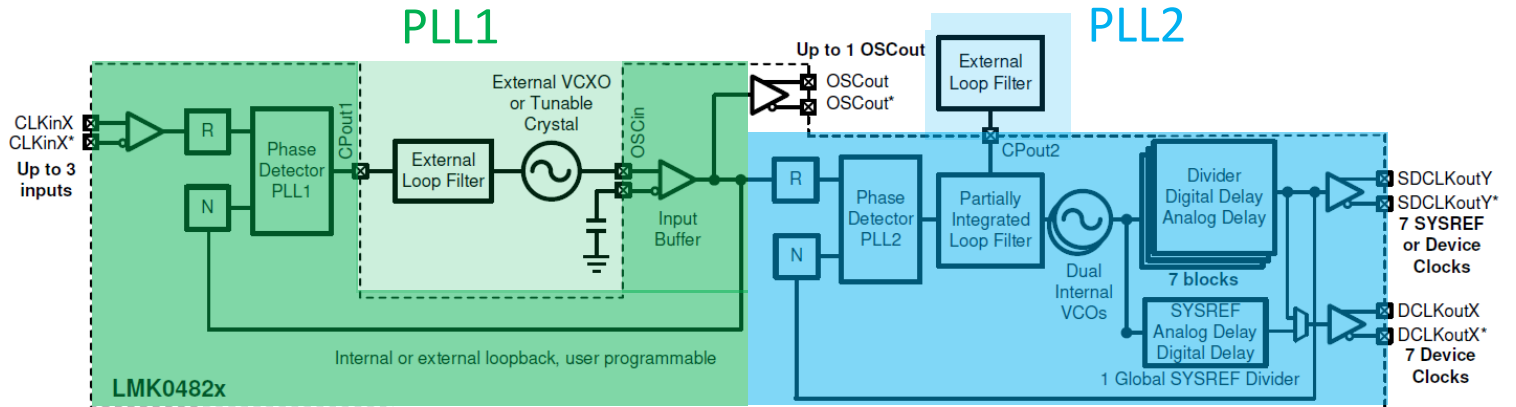
Analog Devices LTC2386-18 ADC



- 10Msps Throughput Rate
- No Pipeline Delay, No Cycle Latency
- 95.7dB SNR (Typ) at $f_{IN} = 1\text{MHz}$
- 102dB SFDR (Typ) at $f_{IN} = 1\text{MHz}$
- Nyquist Sampling Up to 5MHz Input
- Guaranteed 18-Bit, No Missing Codes
- $\pm 1.75\text{LSB}$ INL (Max)
- 8.192V_{P-P} Differential Inputs
- 5V and 2.5V Supplies
- Internal 20ppm/°C (Max) Reference
- Serial LVDS Interface
- 97mW Power Dissipation
- 32-Pin (5mm × 5mm) QFN Package
- SAR Architecture

Texas Instruments LMK04828 Jitter Cleaner

- Ultra-Low RMS Jitter
 - 91 fs RMS Jitter (100 Hz to 20 MHz)
- Dual Loop PLL Architecture
- Up to 14 differential outputs
- Three selectable inputs
- On ShaperDSP, receives and ...
 - Belle II 127-MHz clock from collectors
 - Debug clock from FPGA
 - External debug clock (SMA)
- ...provides
 - [conversion signal to ADCs](#)
 - Three system clocks to FPGA fabric
 - Two reference clocks to GTHs (SerDes)

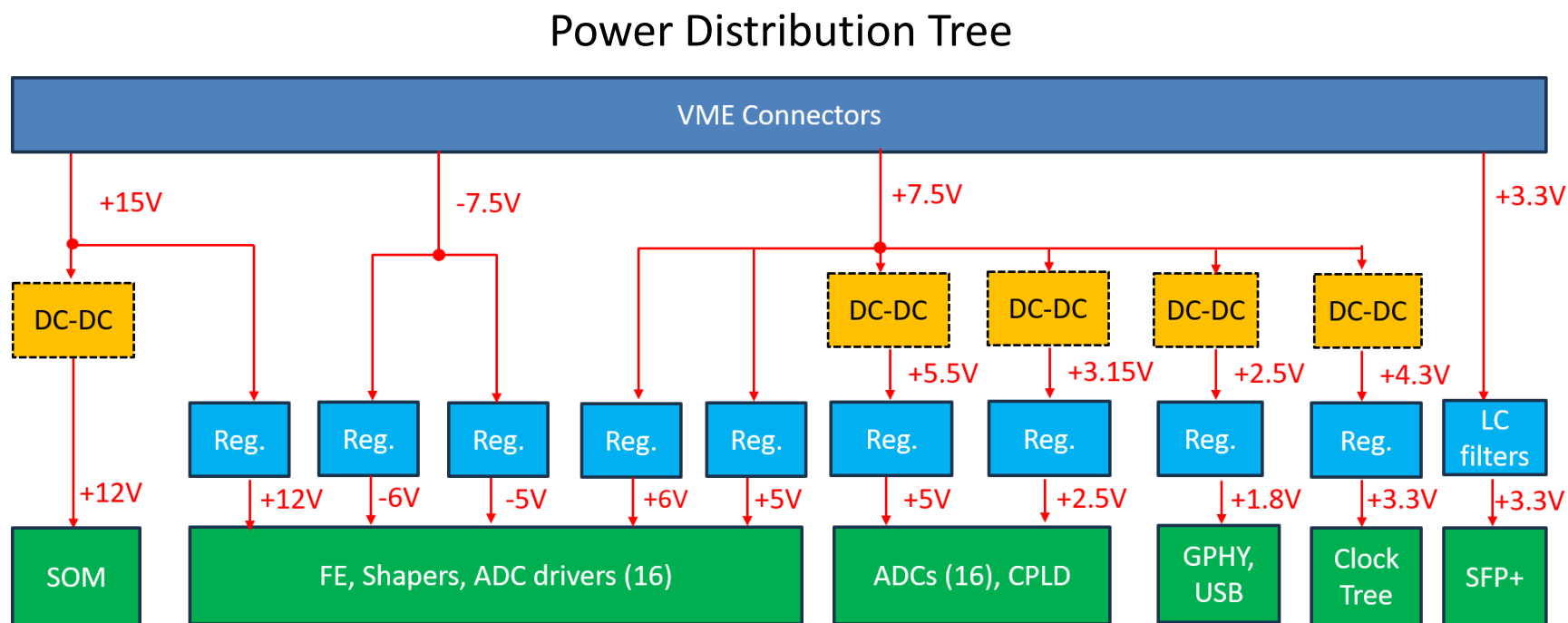


Power-on Quiescent Consumption

- Total 20.2 W (unconfigured FPGA and jitter cleaner, no fan)
 - Of which 18.0 W (89%) is on $\pm 7.5\text{V}$ power lines (analog, ADC, CPLD, GPHY, clock tree)

SN01 – Power consumption

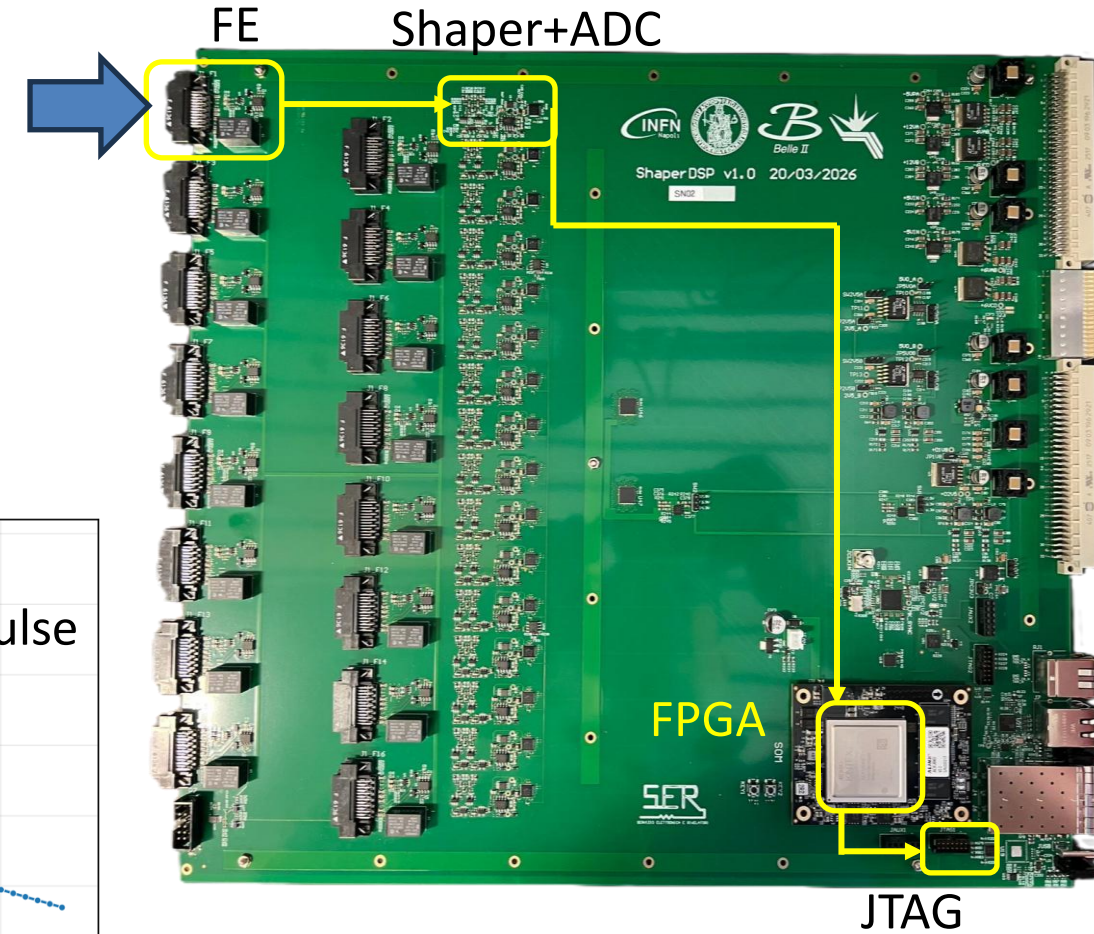
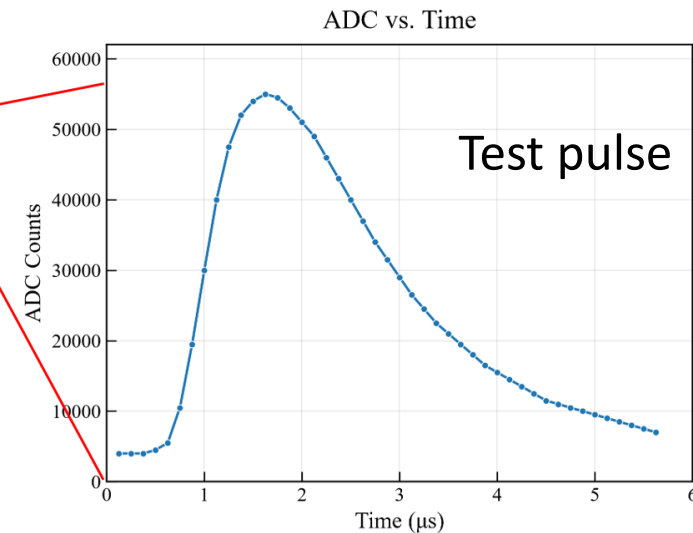
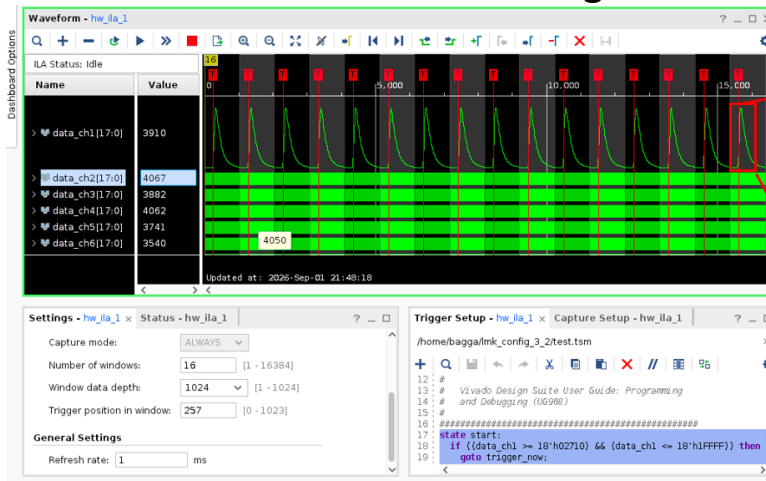
Voltage (V)	Current (A)	Power
+15	0.129	1.93 W
-7.5	0.77	5.78 W
+7.5	1.63	12.23 W
+3.3	0.089	0.29 W
Total power		20.2 W



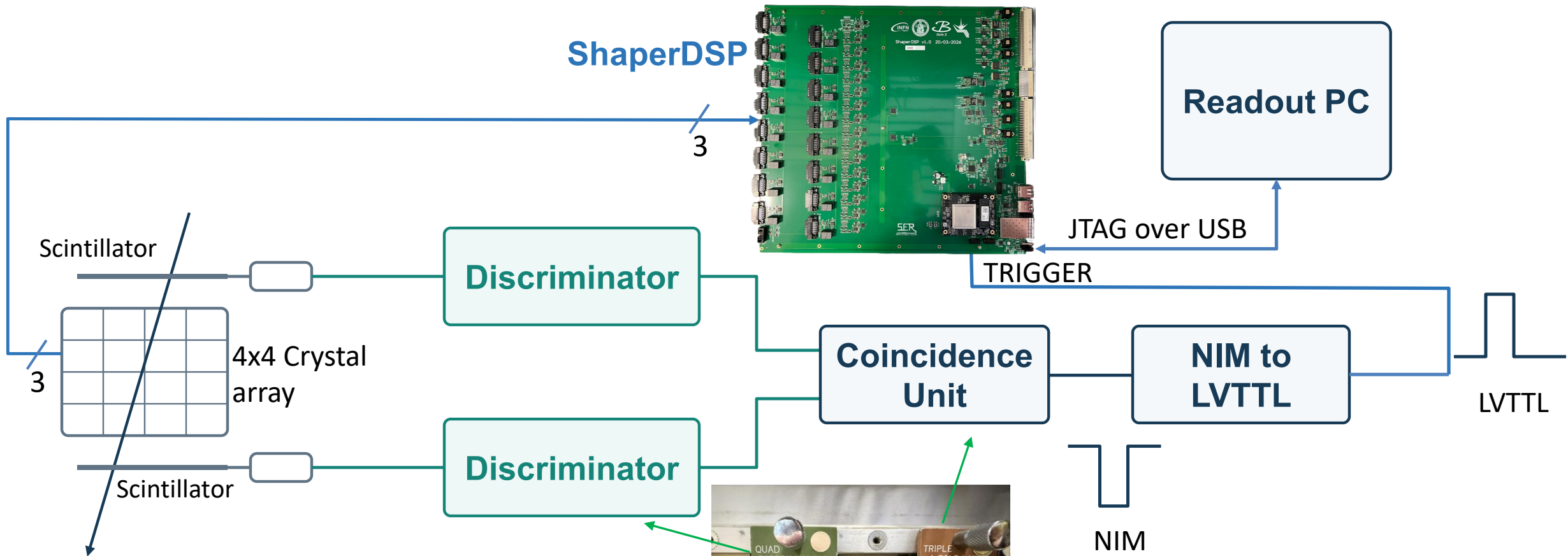
Digitization Tests

- Proof of principle of the electronics chain in the new ShaperDSP board
 - Analog front end $\rightarrow$ shaper $\rightarrow$ ADC $\rightarrow$ FPGA $\rightarrow$ JTAG
- The board supports dedicated input for test pulses, selectively enabled at each channel

Vivado Hardware Manager



Trigger Setup for Cosmics

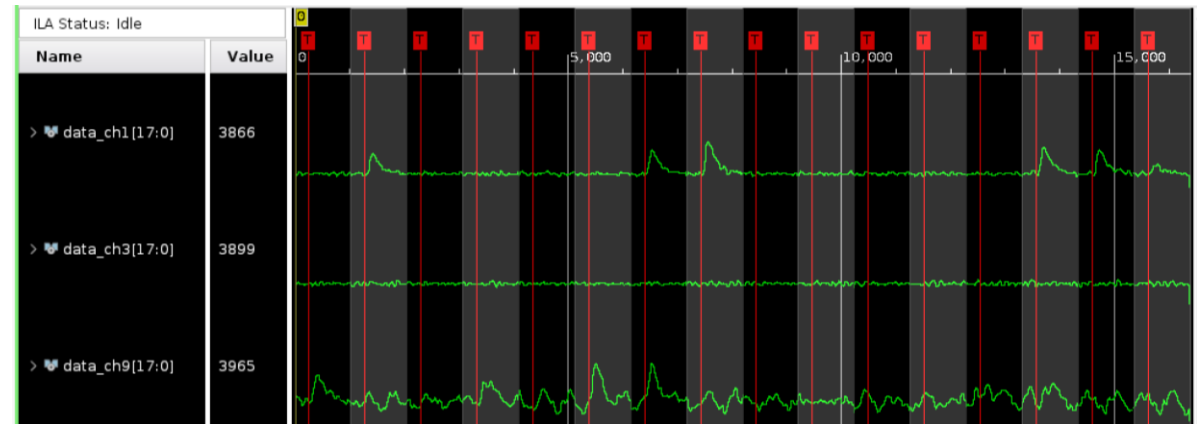
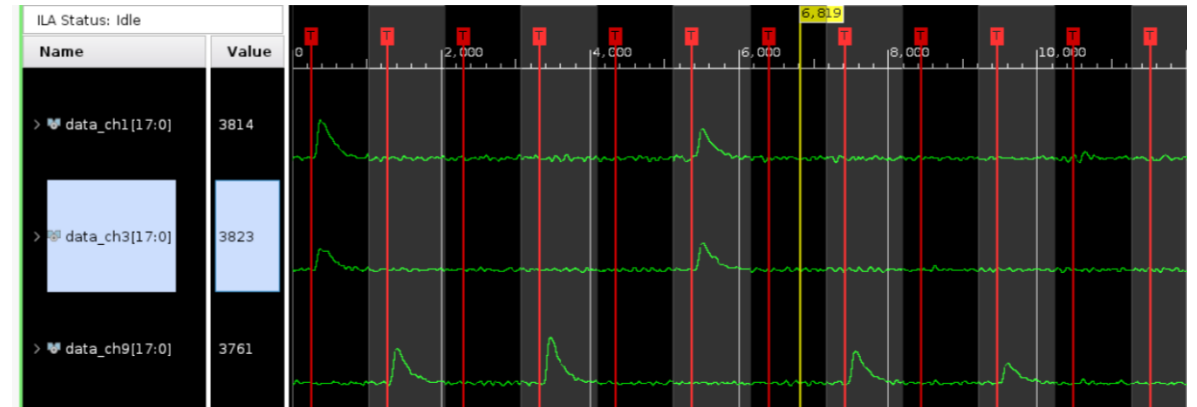


Tests with 3 channels connected simultaneously
(limited number of adapters available)



Cosmic Signal Digitization

- Triggered and collected over 10,000 events
- ADC data reception timing to be adjusted in FPGA (sampling of DA lines)
- Noise (pedestal width) is being investigated and will be compared to previous version of the front-end electronics



Conclusions

- The ECL Upgrade will deliver significantly more powerful electronics
 - For better pile-up noise rejection and signal processing in the front-end
- Simulation of reconstruction performance confirms better energy resolution for new electronics in high-BIB scenarios
- New front-end electronics prototype has been produced and basic preliminary tests are successful
- Next steps
 - Measure noise and compare with present electronics
 - Complete shaping in FPGA gateway after digitization, e.g., digital tail suppression, readout via Ethernet and optical transceivers
 - Measure power consumption with full gateway running
 - Continue designing other modules in the trigger chain upgrade