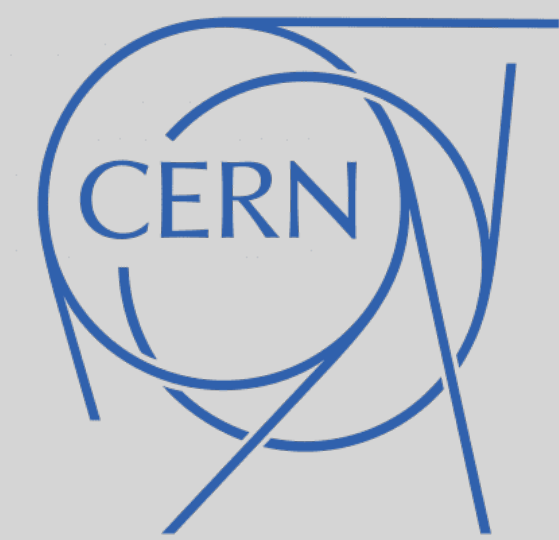




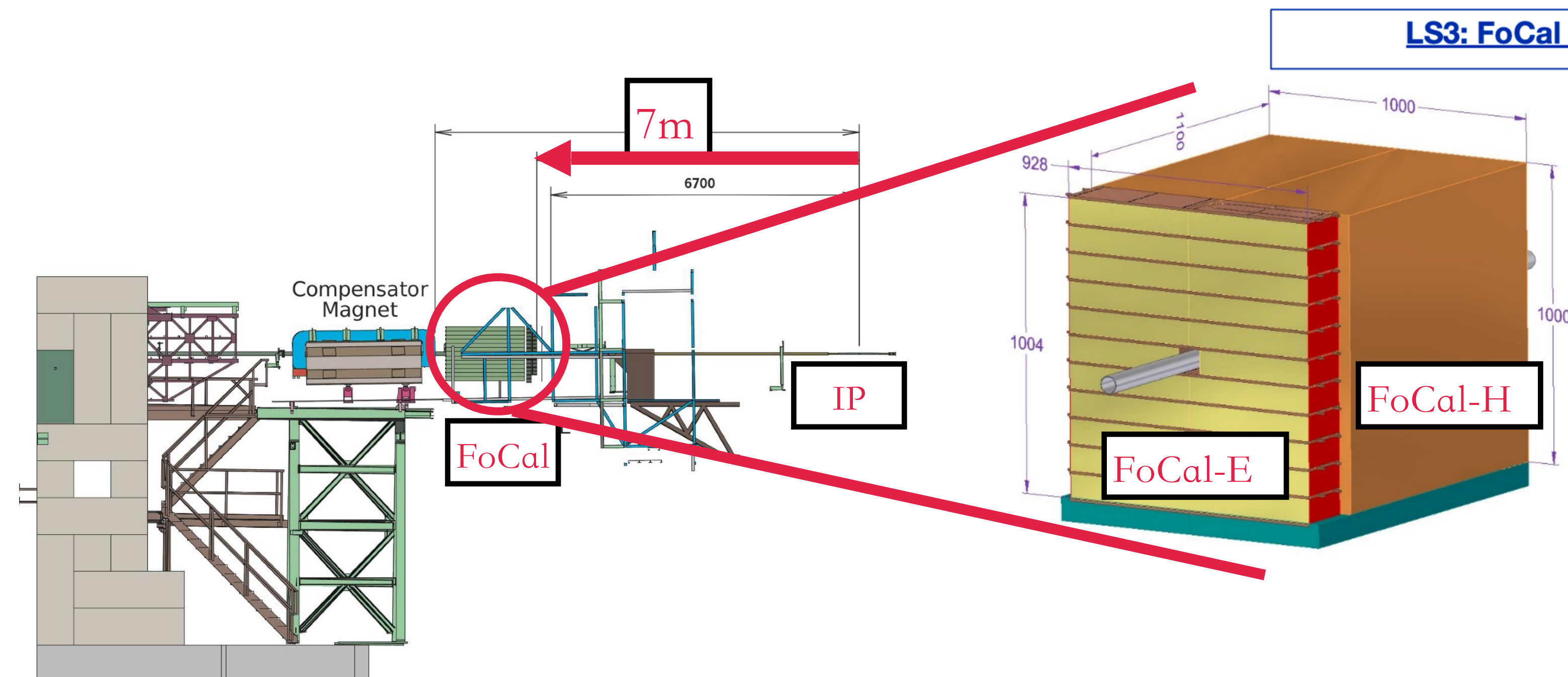
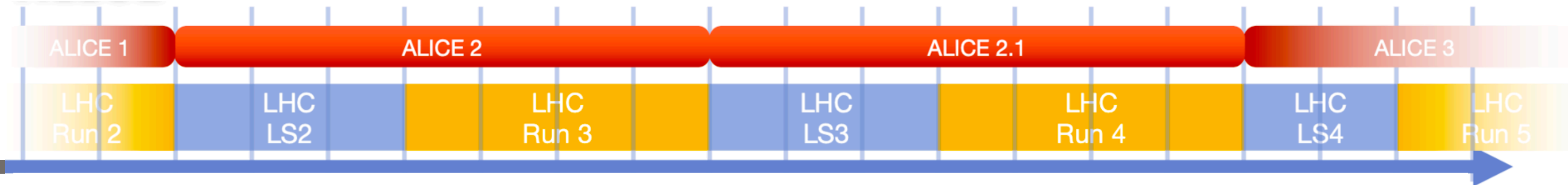
Production Testing and Assembly of ALPIDE Pixel Layers for the ALICE FoCal

Jie Yi

Central China Normal University
on behalf of the ALICE Collaboration

The 2026 International Conference on Instrumentation for Colliding Beam Physics (INSTR 2026)

13 October 2026



LS3: FoCal & ITS3

LS4: ALICE 3

- During the LHC LS3 period, ALICE will add a **new** calorimeter detector (**Forward Calorimeter**, FoCal)
- The TDR was approved by the LHCC in March 2024

Public Notes & Paper:

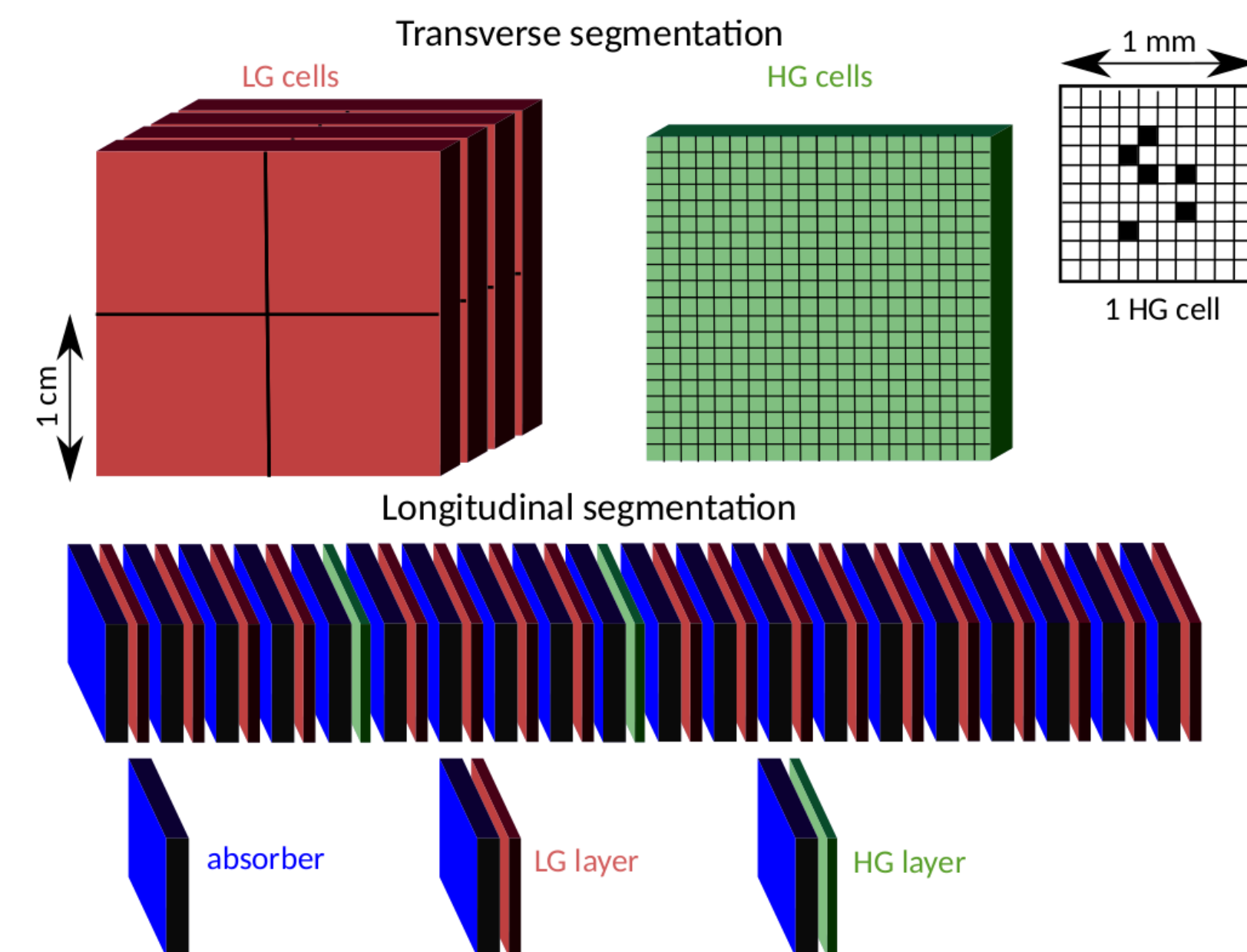
- TDR ([CERN-LHCC-2024-004](https://cds.cern.ch/record/2811111/files/CERN-LHCC-2024-004.pdf))
- Letter of Intent ([CERN-LHCC-2020-009](https://cds.cern.ch/record/2711111/files/CERN-LHCC-2020-009.pdf))

•FoCal-E

- Highly-granular, longitudinally-segmented **silicon-tungsten** (Si+W) electromagnetic calorimeter.
- 18 pad layers ($1 \times 1 \text{ cm}^2$) + 2 pixel layers ($29.24 \times 26.88 \mu\text{m}^2$).
- Designed for detecting **direct photons** and **neutral pions**.

•FoCal-H

- A metal-scintillator sampling calorimeter ($1.6 \times 1.4 \text{ cm}^2$).
- Constructed from copper grooved plates filled with scintillating fibers.

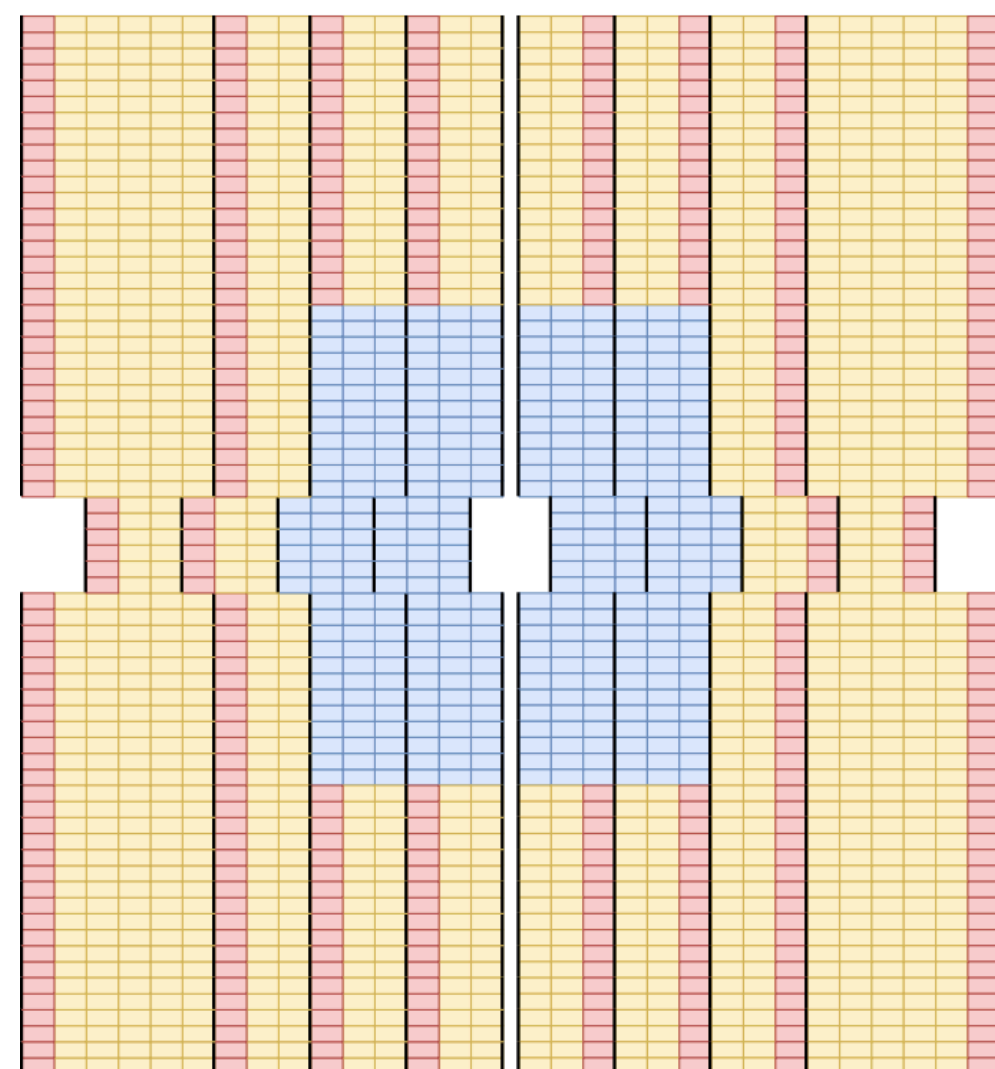


From Pixel Layer to ALPIDE Chip

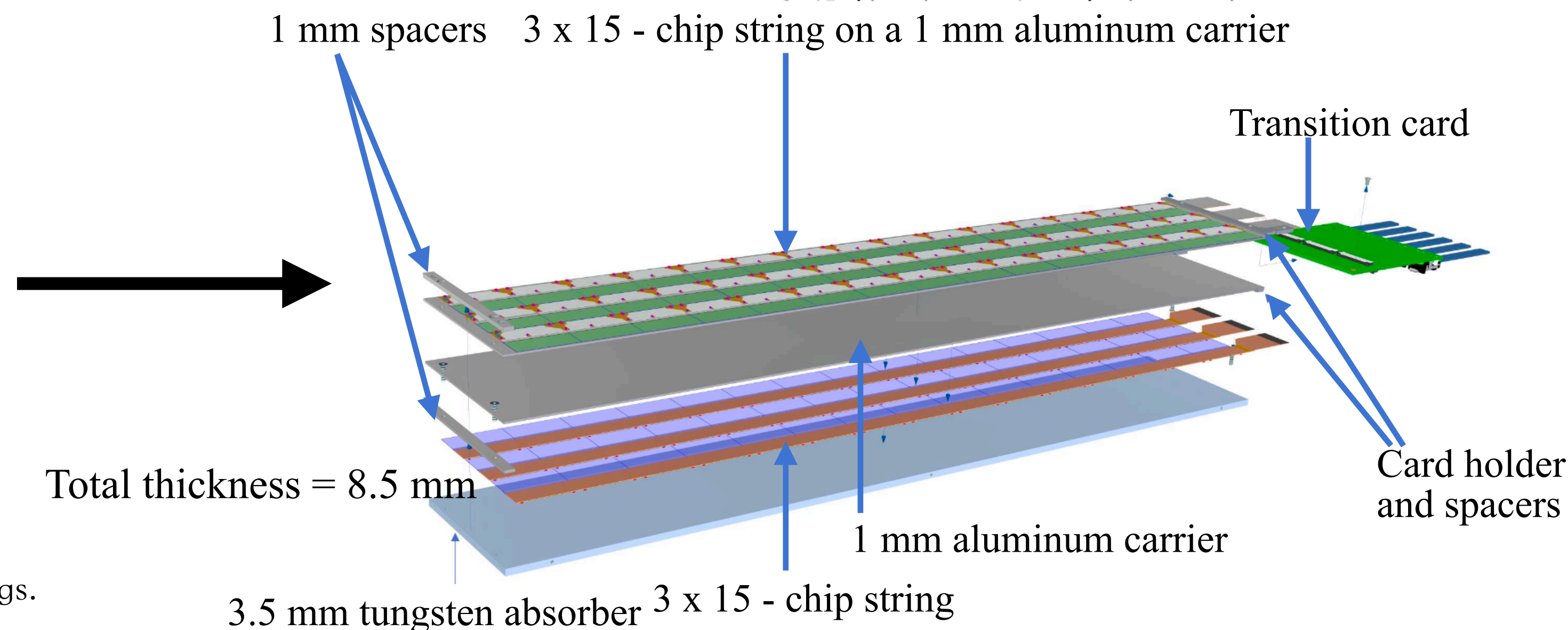
ALPIDE modes:

- Inner Barrel
- Outer Barrel Master
- Outer Barrel Slave

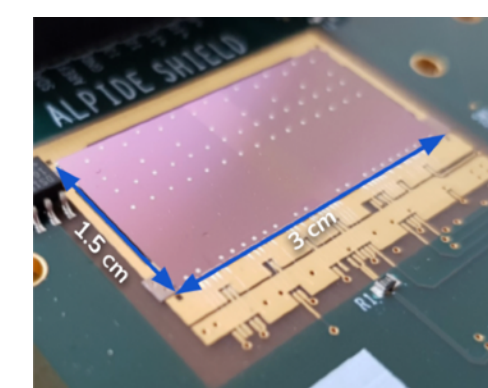
Note: Pixel layer is not to scale



- The pixel layer consists of 22 modules, each containing 6 chip strings.
- The chip strings are divided into Inner Barrel & Outer Barrel strings.
- Each string has 15 or 12 ALPIDE (ALice Pixel DEtector) chip.
- Each pixel has: amplification, discrimination, MEB, test charge injection, masking ...



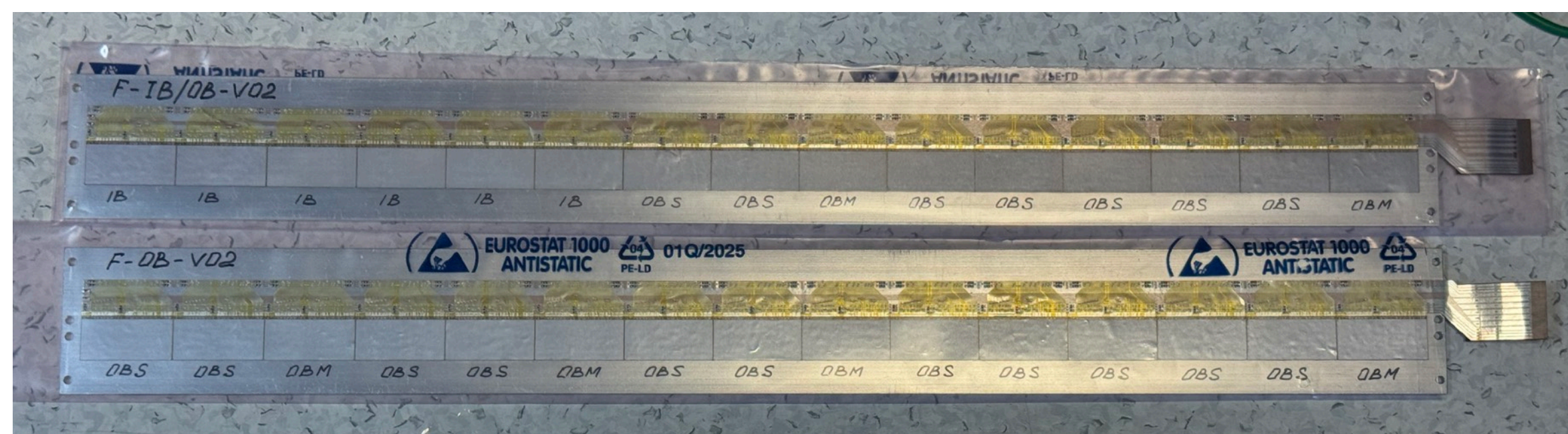
Total thickness = 8.5 mm



ALPIDE Sensor:

1024 × 512 pixels

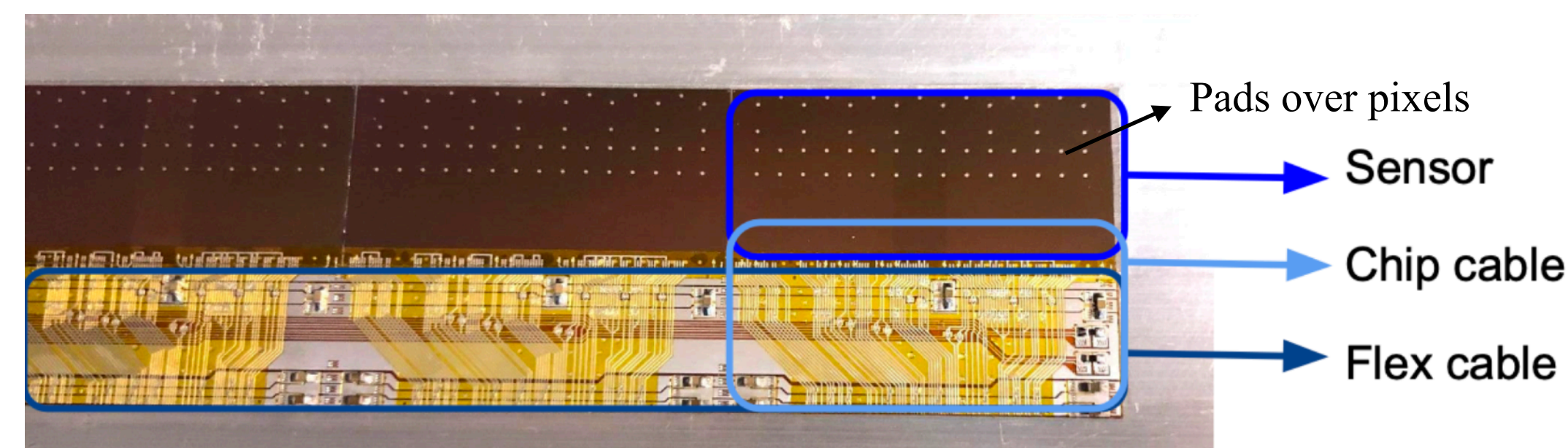
Chip ≈ 3 cm x 1.5 cm



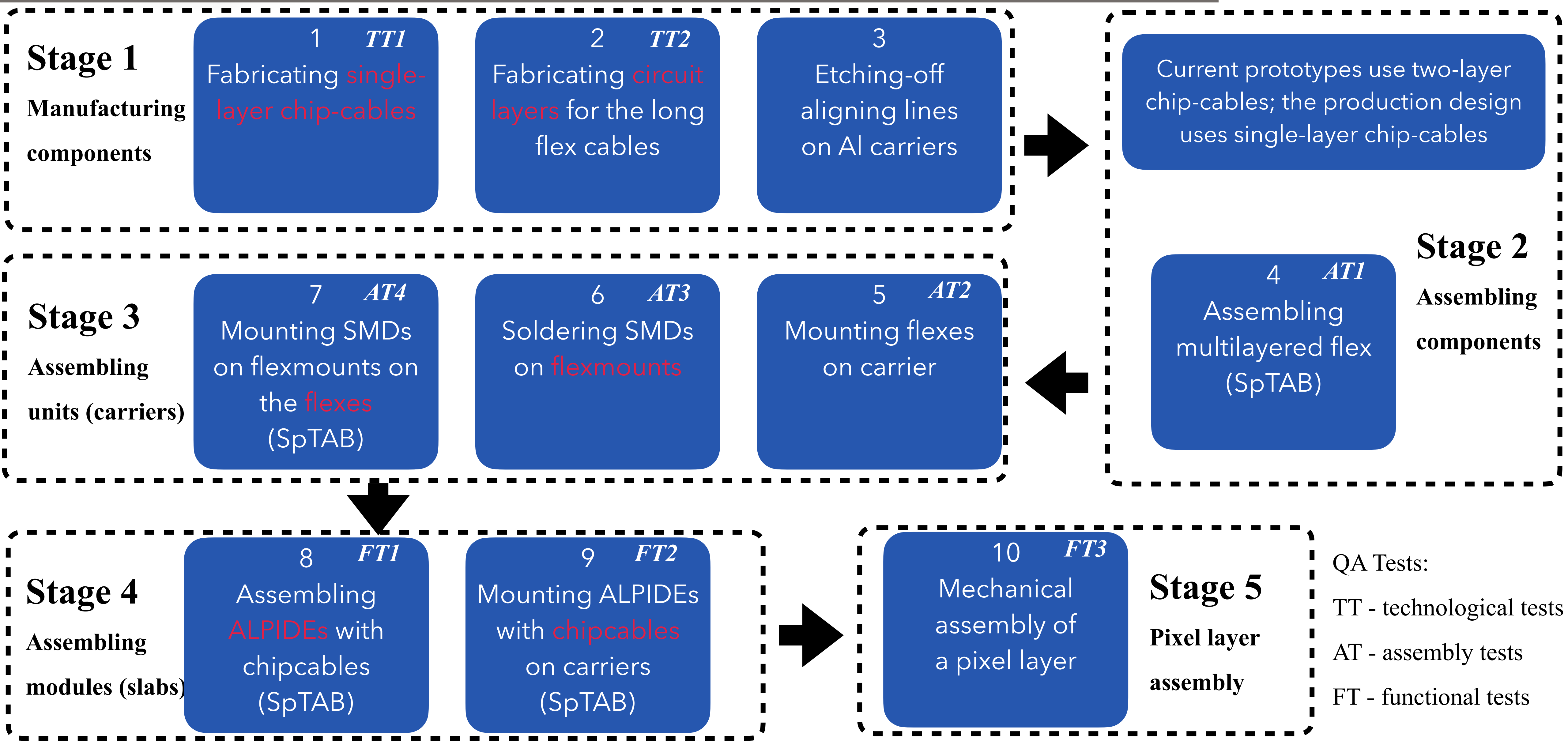
Two ALPIDE Strings at UiB IFT lab

String-flex tail

Connect to TCB



Layer Assembly Workflow at LTU

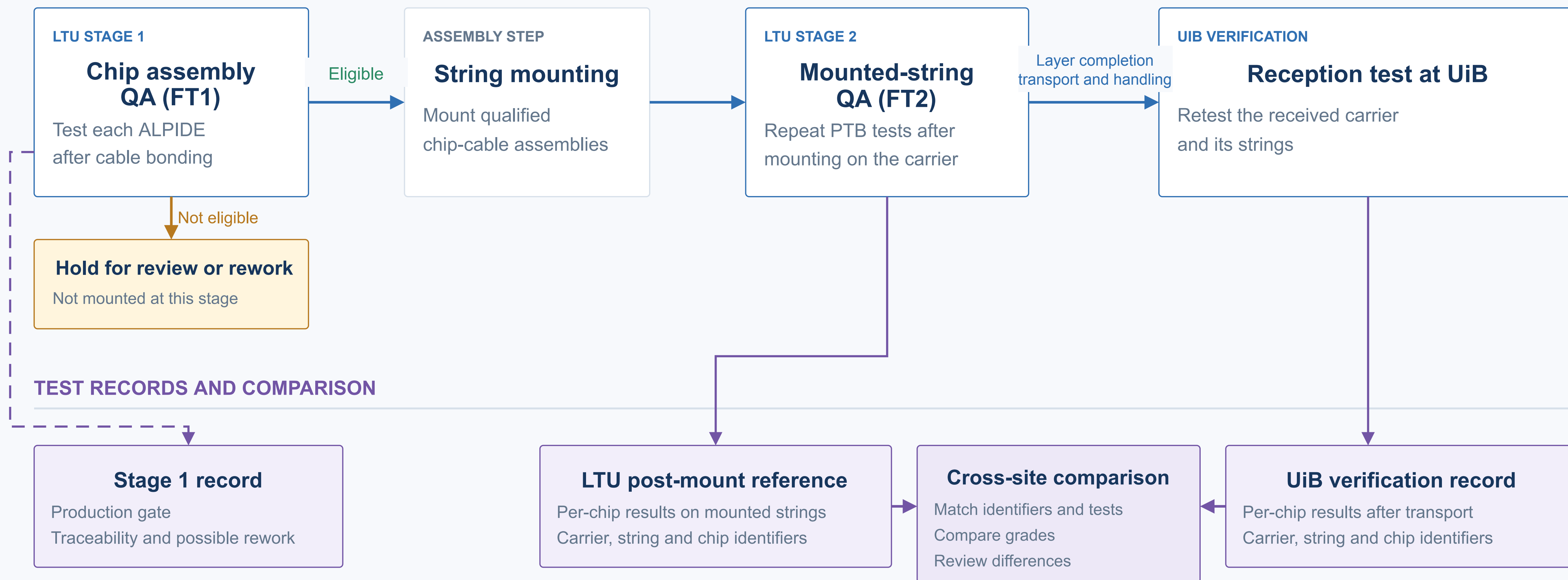


Cross-site record review

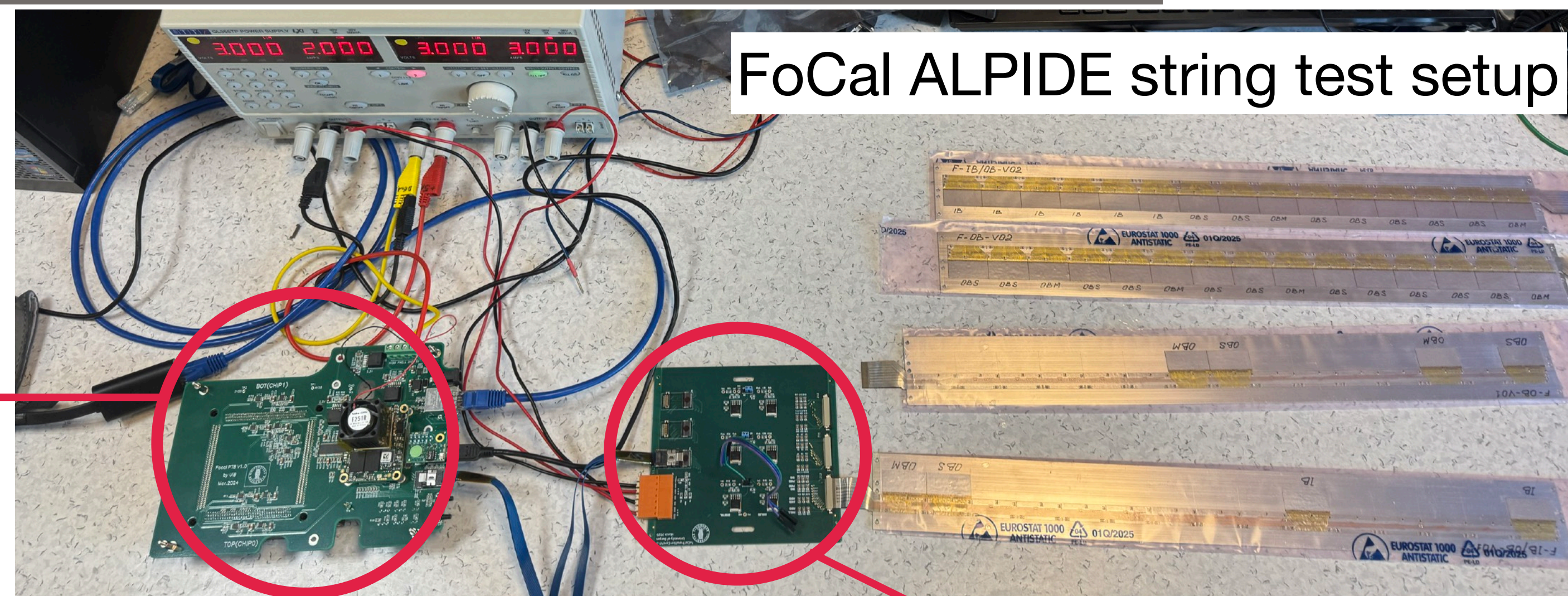
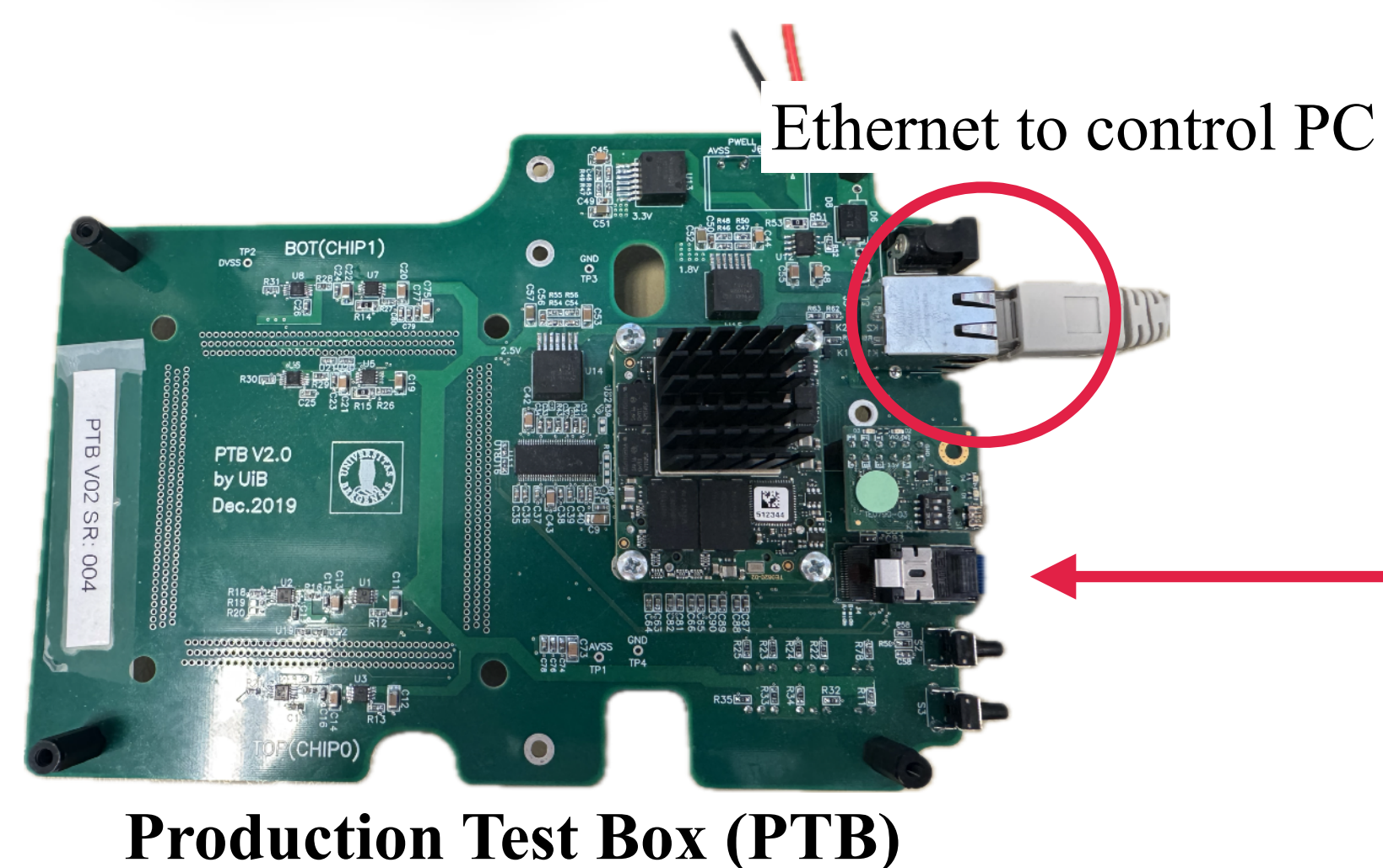
Two production gates at Research and Production Enterprise “LTU” (RPE LTU), followed by post-transport verification at University of Bergen (UiB)

LTU · KHARKIV

UiB · BERGEN



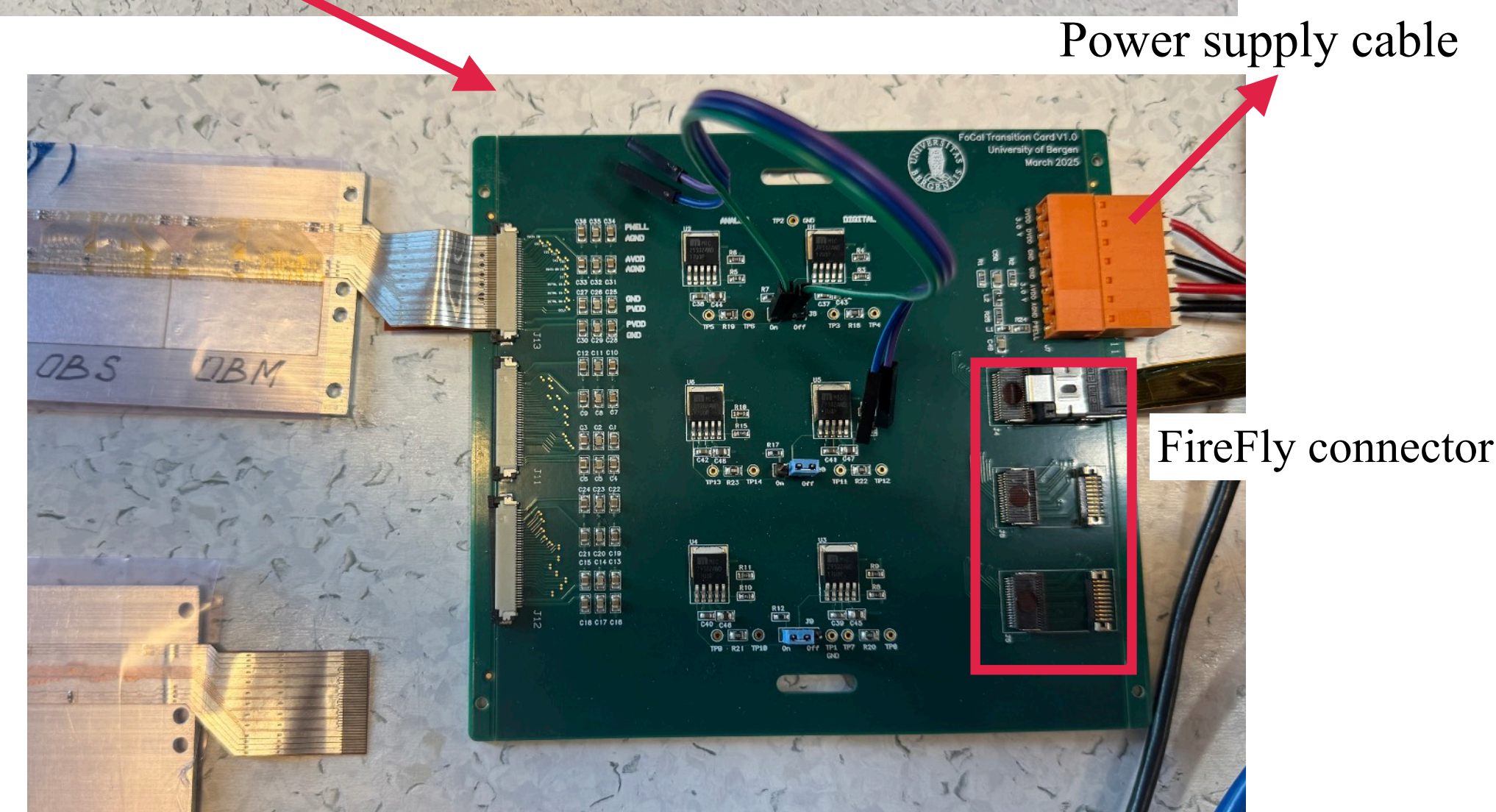
FT1 qualifies each chip assembly before string mounting. FT2 verifies functionality after mounting.



- A FoCal PTB-based test setup is being prepared in Bergen for FoCal ALPIDE string testing.
- Communication with ALPIDE chips through the FoCal PTB has been established.

The **Mini-TC** distributes external power and connects the three strings to the **PTB**.

The **PTB** handles clock, slow control, high-speed readout, and Ethernet communication.



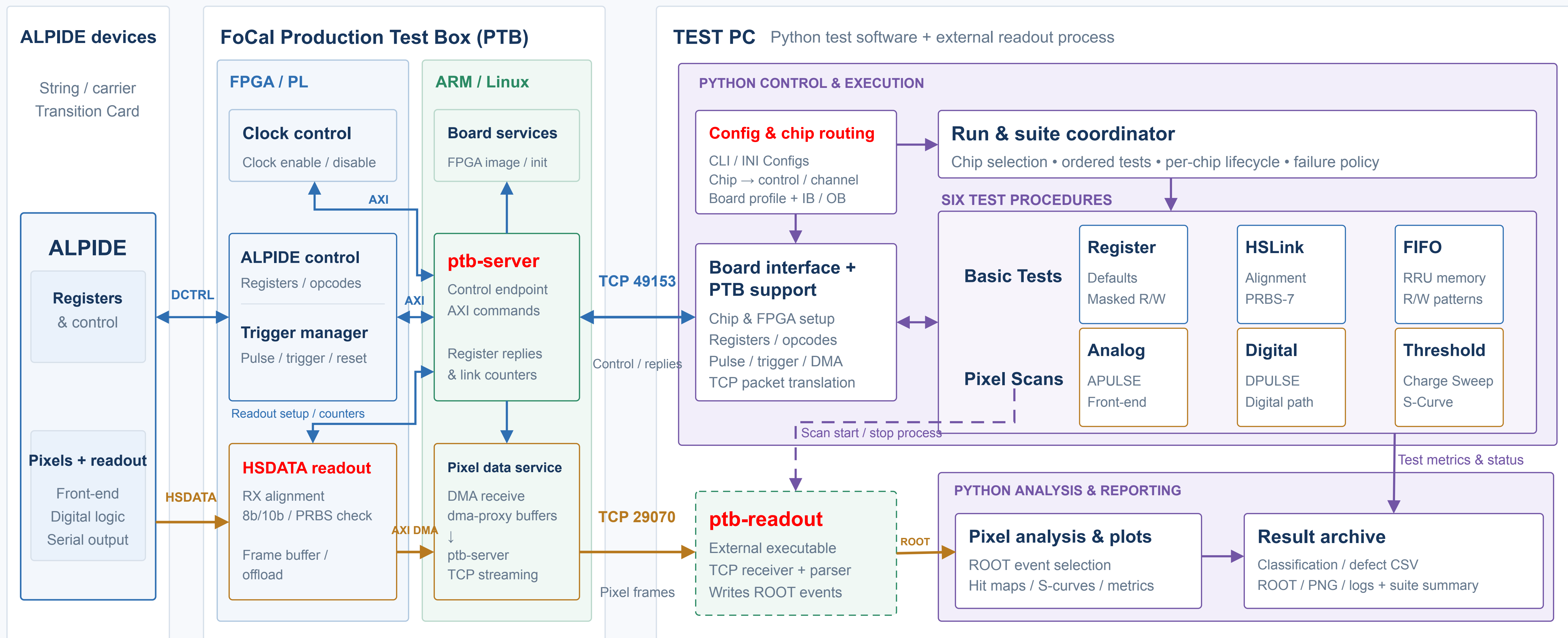
Connect strings to ZIF connectors



Bergen FoCal ALPIDE Production Test System



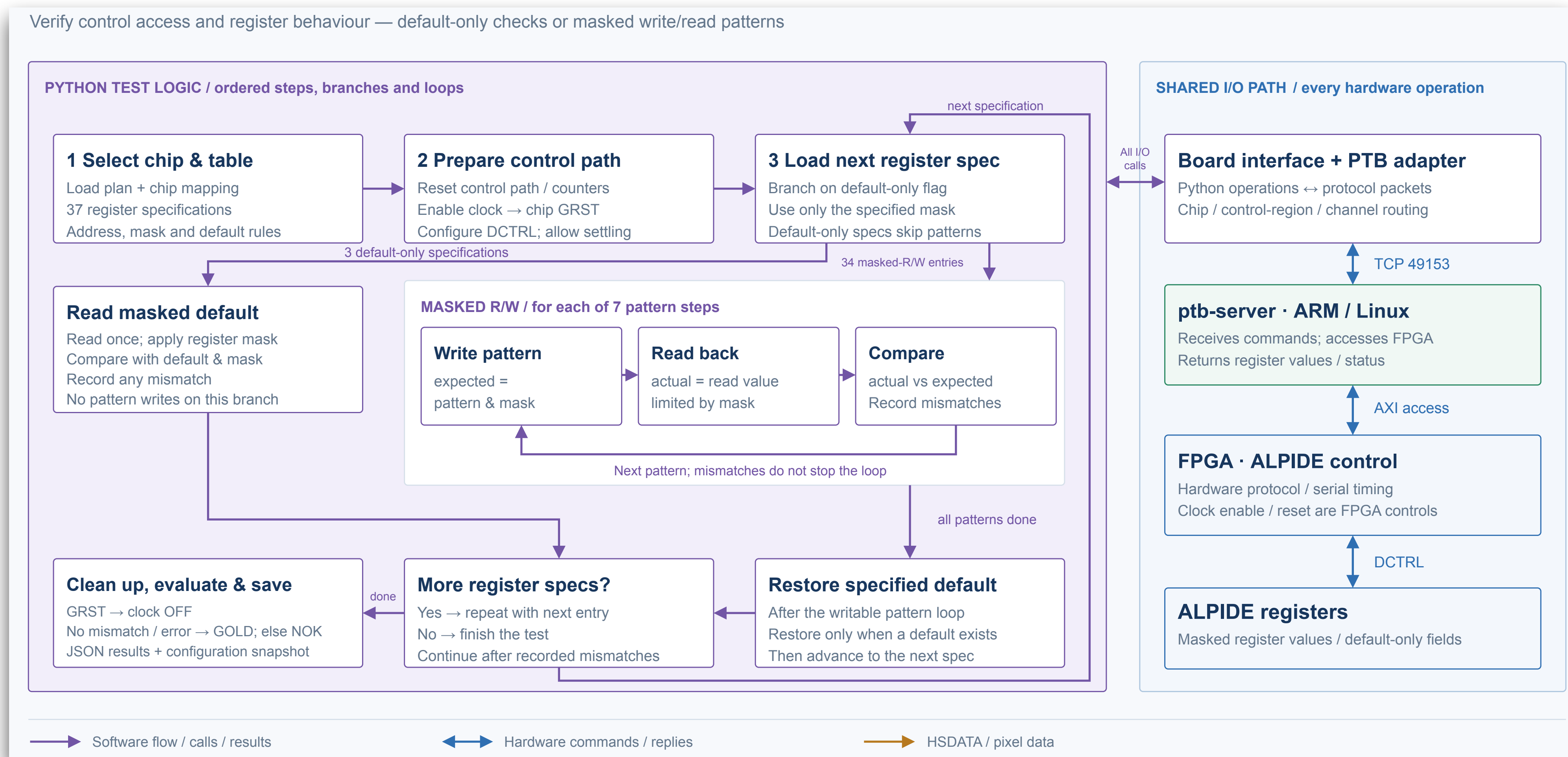
From chip control to reproducible test results



Basic tests provide GOLD/NOK. Pixel scans provide graded chip classifications.

	Test	What it checks	Main output
Basic Functionality 	Register	Register access and read-back integrity	Checked registers and mismatch list
	High-speed link	Link alignment and serial-data integrity	Alignment status and error counters
	FIFO	FIFO memory write/read integrity	Failed patterns and memory locations
Pixel Scans 	Analog scan	Front-end response to injected charge	Hit map, dead/noisy pixels and missing frames
	Digital scan	Digital pixel response and masking	Hit map and response/masking metrics
	Threshold scan	Pixel threshold and response uniformity	Threshold map, mean/RMS, and fitted S-curve

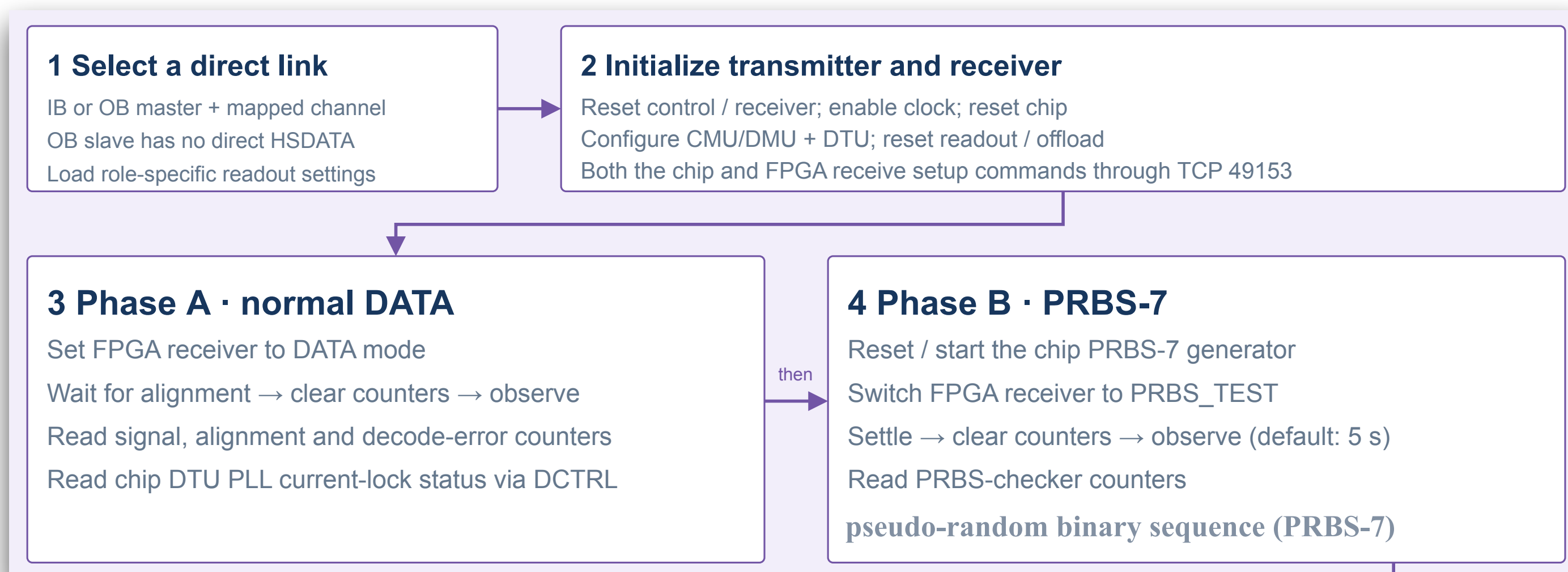
Register Test



The register test checks all 37 specifications and assigns NOK when any mismatch occurs.

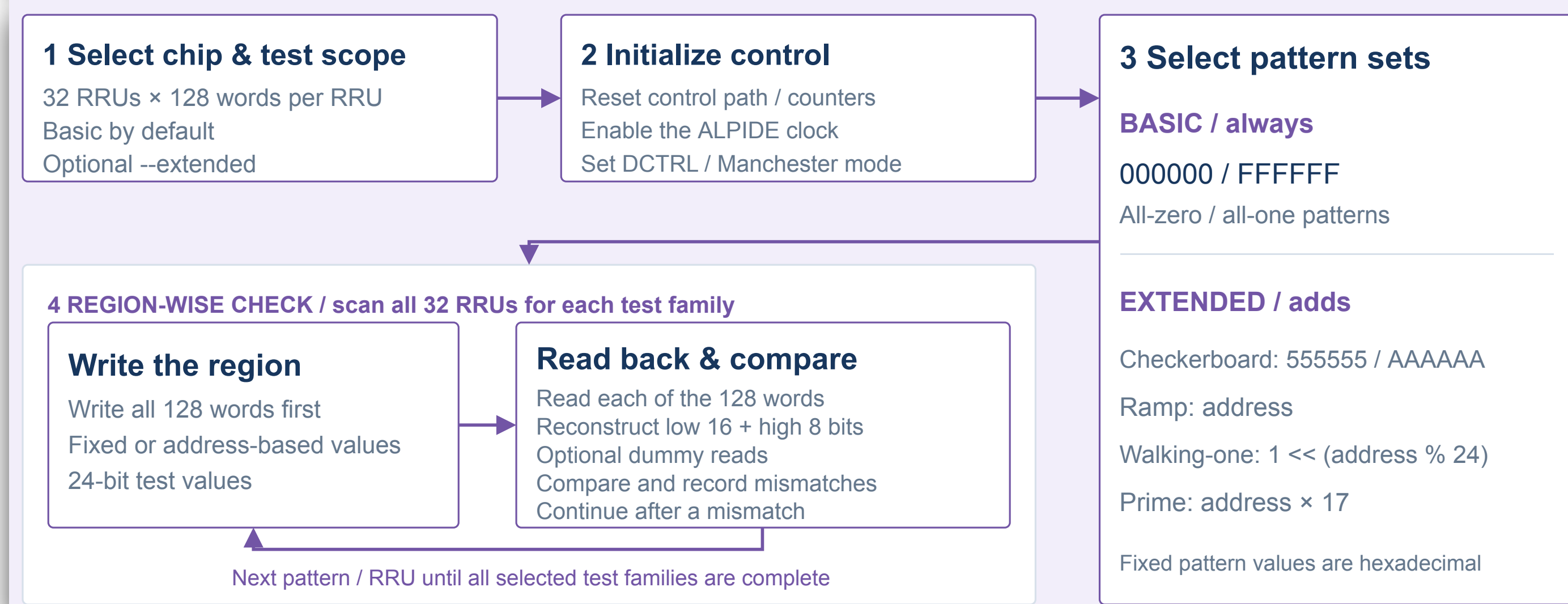
High Speed Link Test

Check link alignment and decoding ; data integrity



FIFO Test

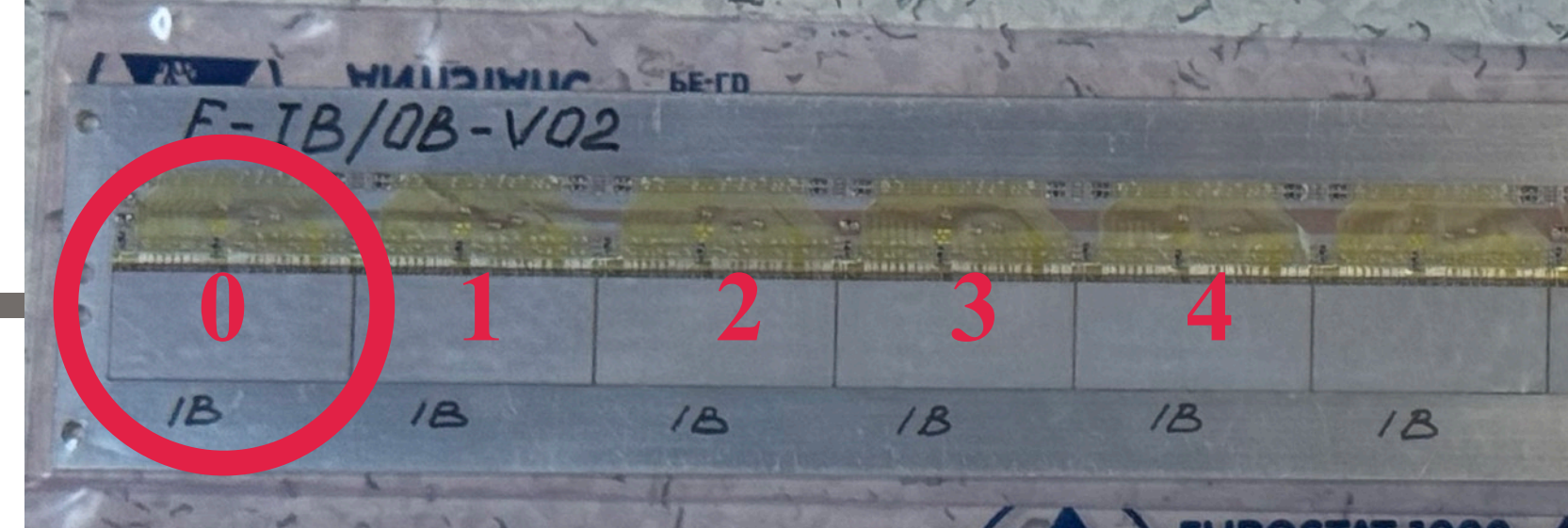
Check FIFO memory write/read integrity



The high-speed link is tested in DATA and PRBS-7 modes. The FIFO test covers all 4,096 memory locations.



Basic Functionality Verified



FIFO memory coverage

All 16,384 write/read checks passed (4/4 patterns per address; 0 failures)

REGISTER TEST

GOLD

37 / 37

selected registers verified
0 mismatches

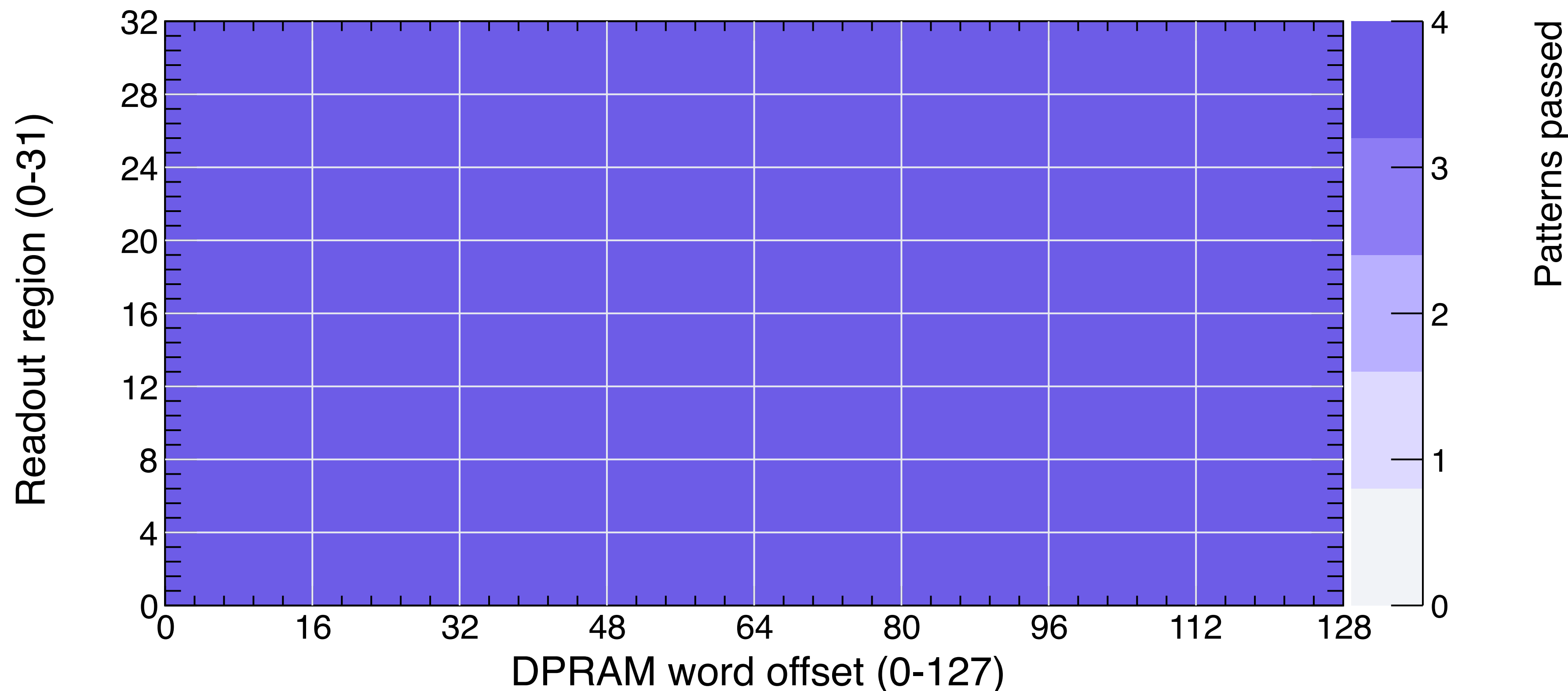
HIGH-SPEED LINK

GOLD

ALIGNED

0 errors

Control access, link alignment and
FIFO memory are operational.



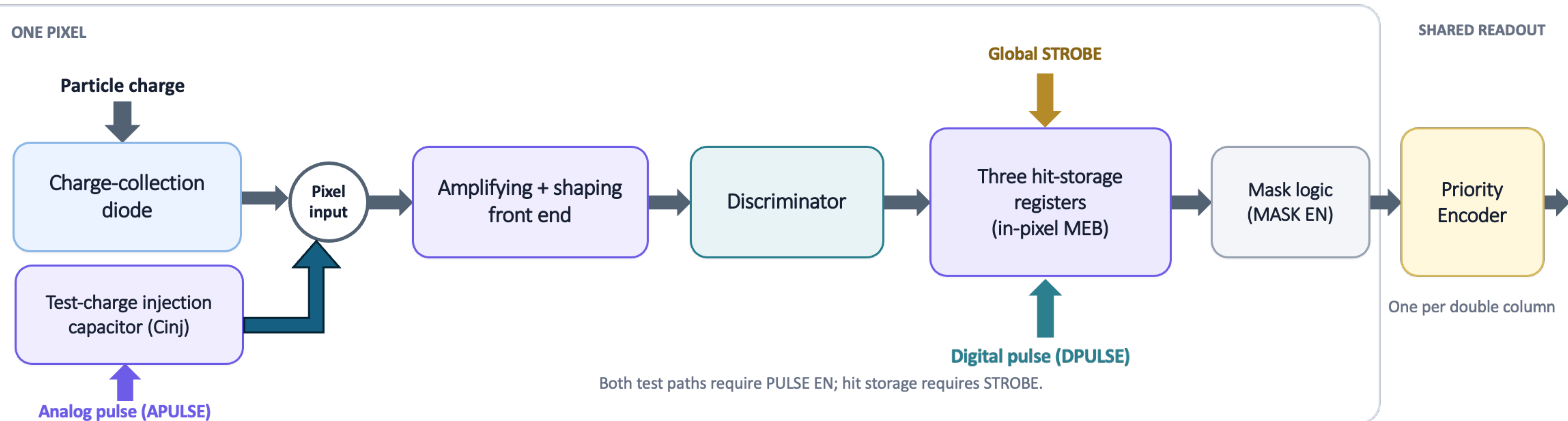
Patterns: 0x000000 | 0x555555 | 0xAAAAAAAA | 0xFFFFFFFF

16384/16384 checks **passed** | **0 failures**

Source: UiB FIFOTest run 2026-08-06 | chip0 | 32 regions x 128 offsets

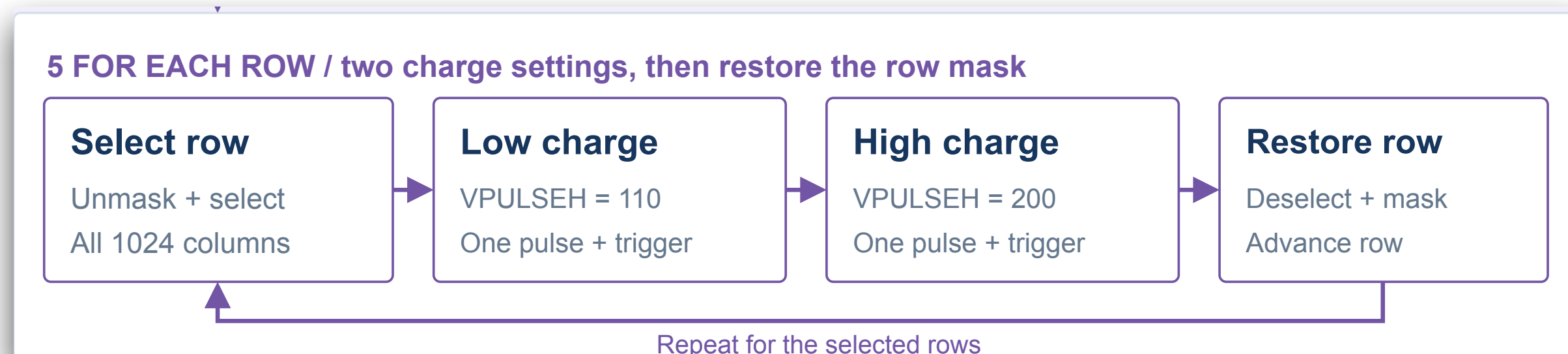
ALPIDE Pixel Signal and Test Paths

Functional block diagram

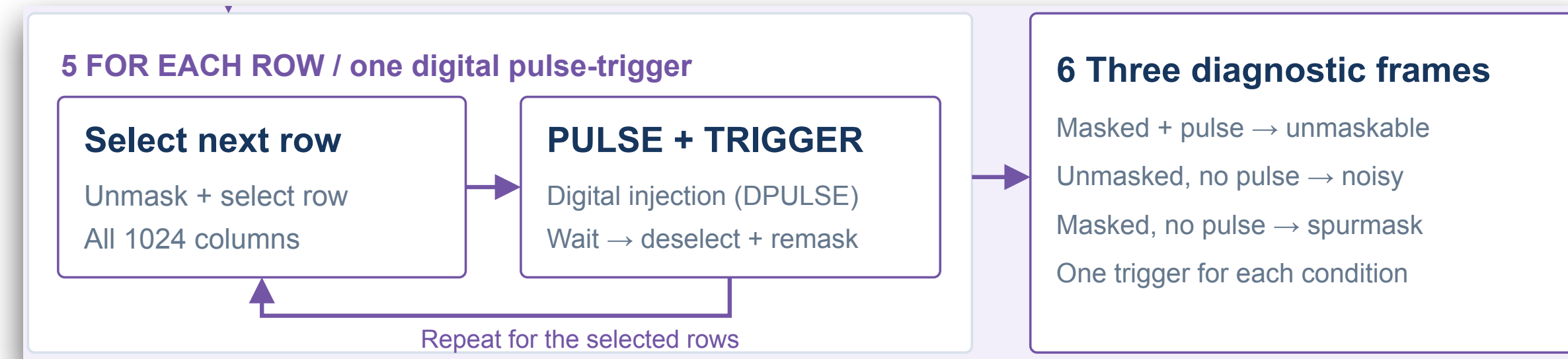


Analog pulsing includes the charge-sensitive front end; **digital** pulsing bypasses it. Both use the same hit-storage and readout path.

Analog Scan

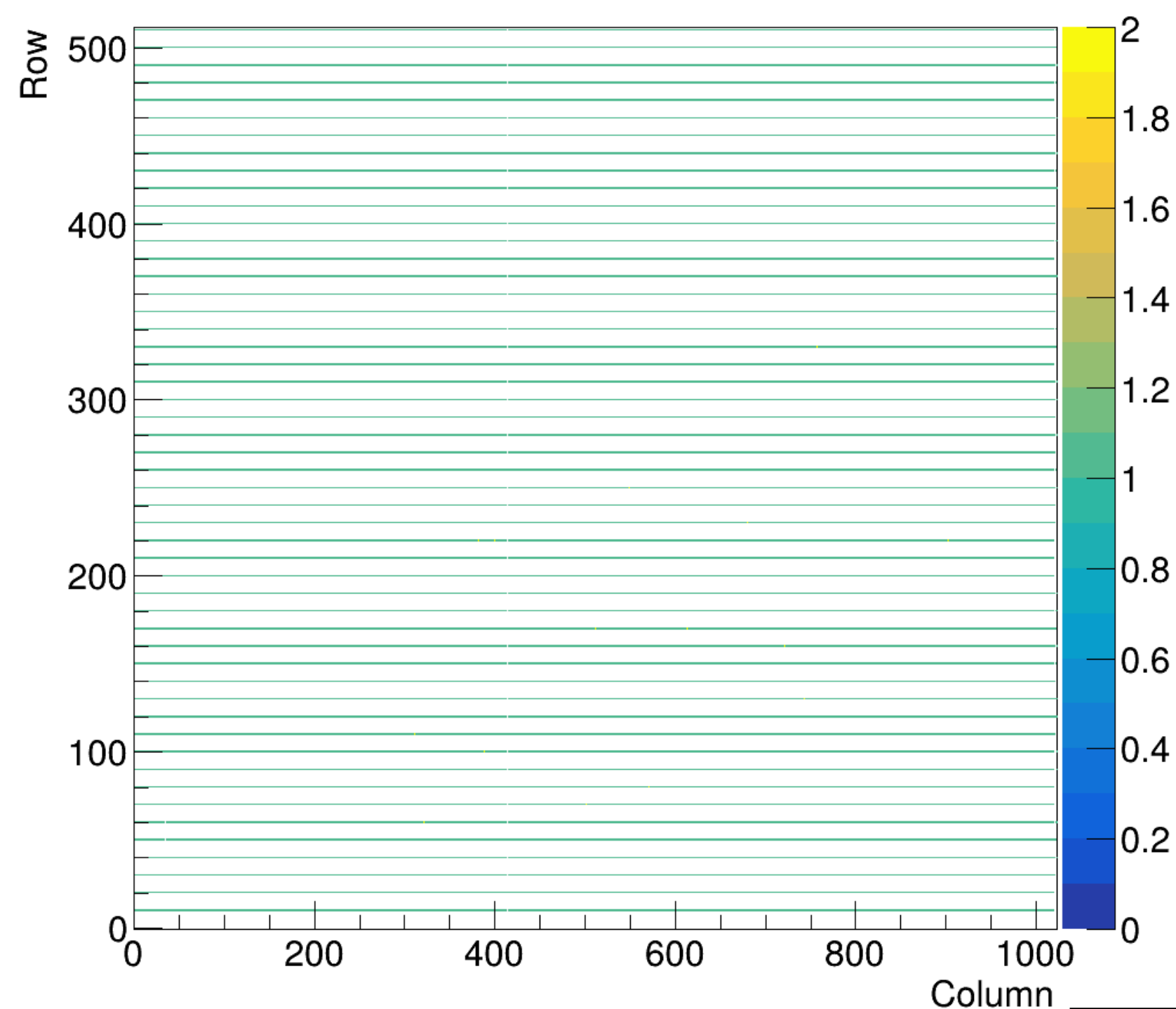


Digital Scan



AnalogScan sparse hits chip 5

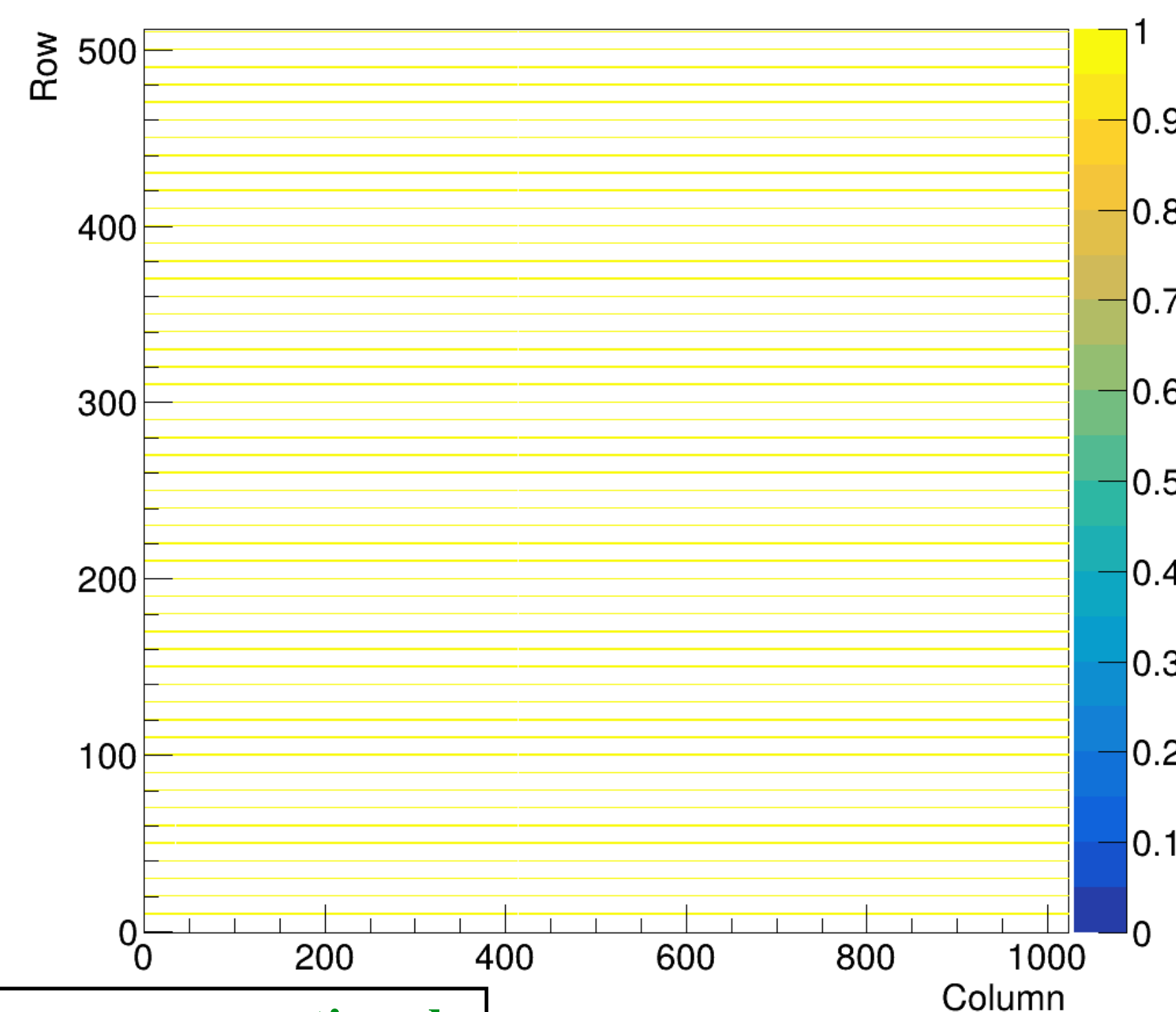
SILVER



noisy_fraction: 0.036%
dead_fraction: 0.29%

DigitalScan pulsed hits chip 5

SILVER



Unpulsable: 0.13%
Unmaskable: 0.0038%
Noisy: 0.15%
Spurmask: 0.0017%

Both analog and digital scans are operational.

The core FoCal ALPIDE test chain is operational in Bergen

Summary

- The FoCal PTB controls assembled ALPIDE strings and records traceable per-chip results.
- All basic tests passed, and the test system operated as expected.
- Analog and digital scans reproduce the expected pixel-response pattern.

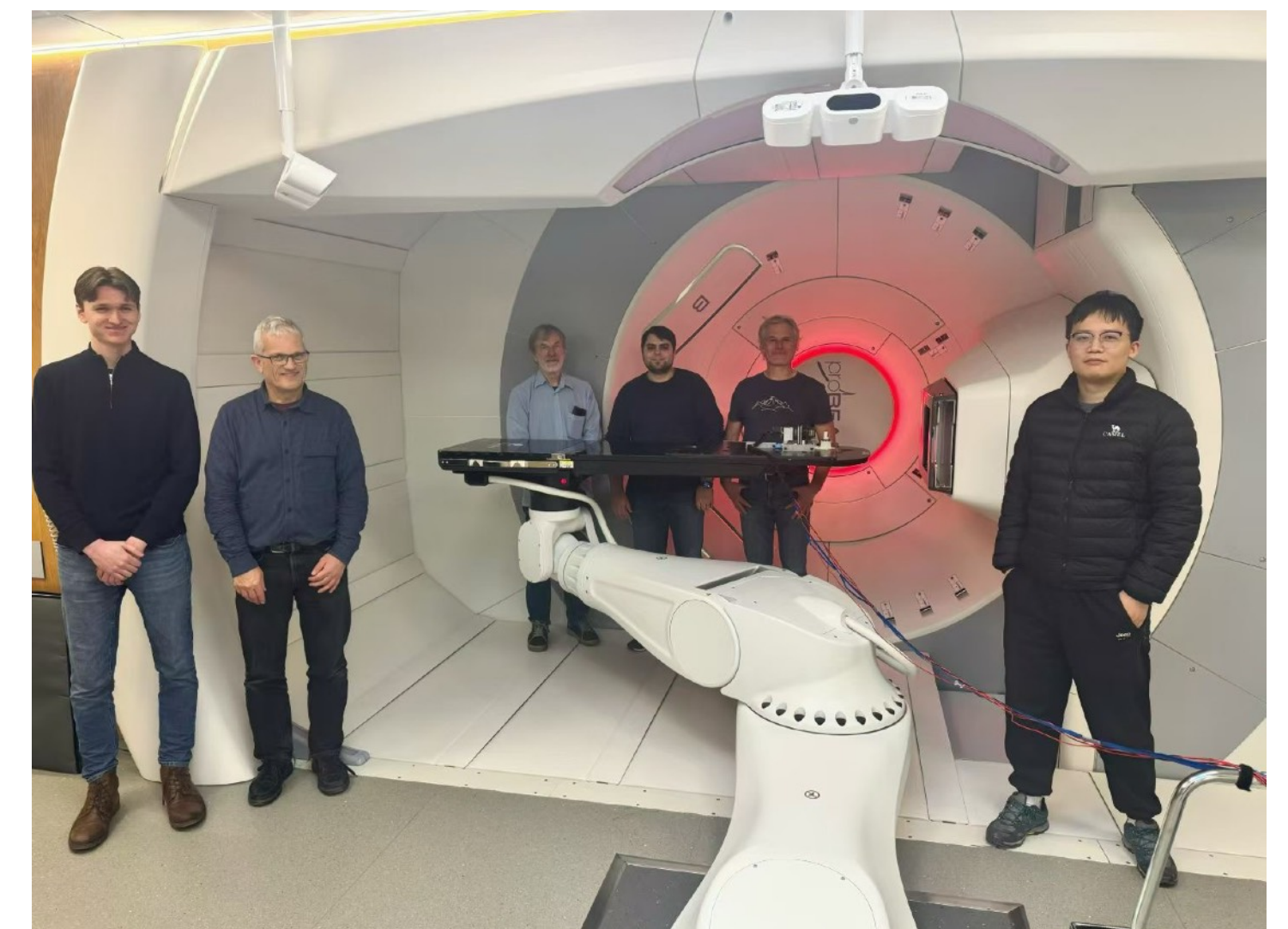
Next steps

- Complete threshold S-curve and noise extraction for pixel calibration.
- Extend test procedures to OB strings.
- Compare LTU and UiB results after transport.

Thank you for your attention



First pCT ALPIDE Beam Test at Haukeland Hospital, 2026





Backup

Test	GOLD condition	Lower grades / NOK
Register	All configured register patterns read back correctly	Any mismatch → NOK
High-speed link	Link aligned; decode errors = 0; PRBS errors = 0	Otherwise → NOK
FIFO	All tested memory values read back correctly within the configured attempts	Any unresolved mismatch → NOK
Analog scan	Dead and noisy pixel counts satisfy the limits below	Worst of the two counters sets the grade
Digital scan	All four fault counters satisfy the limits below	Worst counter sets the grade
Threshold scan	Nested cuts on fitted-pixel fraction, mean threshold, RMS and RMS/mean	See Backup slide B and the implementation caveat

Grade	Analog dead / noisy, full matrix	Digital unpulsable, sparse / full	Digital unmaskable / noisy / spurmask
GOLD	<50 / <50	<5 / <50	each <50
SILVER	<2100 / <2100	<210 / <2100	each <2100
BRONZE	<5240 / <5240	<524 / <5240	each <5240
WOOD	<450000 / <550000	<4500 / <45000	each <45000
NOK	otherwise	otherwise	otherwise

In analog sparse mode, all metrics should be scaled down by factor 10
In digital sparse mode, only unpulsable should be scaled down by factor 10.

Parameter	GOLD	SILVER	BRONZE	NOK
Pixels with fitted threshold	>99%	>95%	>80%	otherwise
Average threshold	3.86–14.48 DAC	2.23–15.33 DAC	2.0–17.5 DAC	otherwise
Threshold dispersion, RMS	1.08–2.86 DAC	0.99–2.91 DAC	0.9–3.5 DAC	otherwise
Relative dispersion, RMS/mean	20–30%	10–30%	10–50%	otherwise



Abbreviations and Explanation



Term	Full form		Meaning
pCT	Proton Computed Tomography		Reconstructs proton relative stopping power from tracked protons.
CT	Computed Tomography		Imaging method; the opening slide contrasts proton CT with X-ray CT.
RSP	Relative Stopping Power		Material stopping power relative to water.
DTC	Digital Tracking Calorimeter		Pixel-layer detector that tracks protons and measures their remaining range.
ALPIDE	ALICE Pixel Detector		Monolithic active pixel sensor used as the basic detector unit.
ALICE	A Large Ion Collider Experiment		CERN experiment for which the ALPIDE sensor was originally developed.
MAPS	Monolithic Active Pixel Sensor		Sensor and readout electronics integrated in the same silicon chip.
QA	Quality Assurance		Checks and records used to qualify assemblies before detector integration.
UiB	University of Bergen		Bergen site performing post-transport verification.
LTU	Proper name: Research and Production Enterprise "LTU" (RPE LTU)		Kharkiv production and assembly site; LTU is not expanded as a university name.
TT	Technological Tests		Checks fabrication quality after manufacturing flex or cable layers.
AT	Assembly Tests		Checks workmanship after bonding, soldering, alignment or mounting steps.
FT	Functional Tests		Powered electrical tests after ALPIDE bonding, mounting or layer assembly.
SMD	Surface-Mount Device		Small component soldered directly onto a flex or printed circuit board.
SpTAB	Single-point Tape Automated Bonding		Ultrasonic bonding of aluminium flex leads to aluminium pads.
Al	Aluminium (chemical symbol)		Material of the string carrier; a symbol, not an acronym.

Term	Full form		Meaning
PTB	Production Test Box		FPGA-based board that controls and reads out ALPIDE assemblies during QA.
TC	Transition Card		Interface between ALPIDE flex connections and the readout electronics.
Mini-TC	Mini Transition Card		Test adapter connecting three strings to the PTB.
ZIF	Zero Insertion Force		Connector that clamps a flex tail without high insertion force.
ESD	Electrostatic Discharge		Static-charge hazard controlled by grounding and an ESD strap.
FPGA	Field-Programmable Gate Array		Implements timing, control, triggering and high-speed data capture.
PL	Programmable Logic		FPGA fabric in the PTB processing device.
FIFO	First In, First Out		Ordered data buffer; the FIFO test checks memory write/read integrity.
DPRAM	Dual-Port Random-Access Memory		Memory used for the readout FIFO in each ALPIDE RRU; the FIFO test writes and reads patterns at its addressed locations.
RRU	Region Readout Unit		ALPIDE block that transfers one matrix region into a region FIFO.
AXI	Advanced eXtensible Interface		Internal bus connecting PTB processor and FPGA logic.
DMA	Direct Memory Access		Transfers pixel data to memory without per-word CPU handling.
ARM	ARM processor architecture		Runs embedded Linux and board services on the PTB.
TCP	Transmission Control Protocol		Ethernet transport used by the PTB control and pixel-data services.
PC	Personal Computer		External computer running the Python test and analysis software.
CLI / INI	Command-Line Interface / initialization-file format		How tests are launched and configured.
R/W / RX	Read/Write / Receive		Register/FIFO operations and link-receiver alignment.
ID / ChipID	Identifier / chip identifier		Selects and traces a chip within its module/string.

RMS: Root Mean Square

Extended FIFO memory patterns

Each pass writes 128 offsets per RRU, then reads back and compares

Pattern	Stored word at offset a	Main check
Ramp	$\text{word}[a] = a$ $a = 0, 1, 2 \rightarrow 000000, 000001, 000002$	Address decoder: each offset has a distinct value.
Walking-one	$\text{word}[a] = 1 \ll (a \bmod 24)$ $a = 0, 1, 2, 24 \rightarrow 000001, 000002, 000004, 000001$	Exercises one data bit at a time. Repeats every 24 offsets.
Prime	$\text{word}[a] = 17 \times a$ $a = 0, 1, 2 \rightarrow 000000, 000011, 000022$	Address decoder with more bit changes than Ramp.

Basic: all-zero and all-one words. Extended adds checkerboard and these three address-dependent passes.

“Prime” means multiply by 17. The written values are not a sequence of prime numbers.