



Design and Characterization of a 64-Channel ASIC Readout Board for the HIAF-HIRIBL Gamma-Ray Array

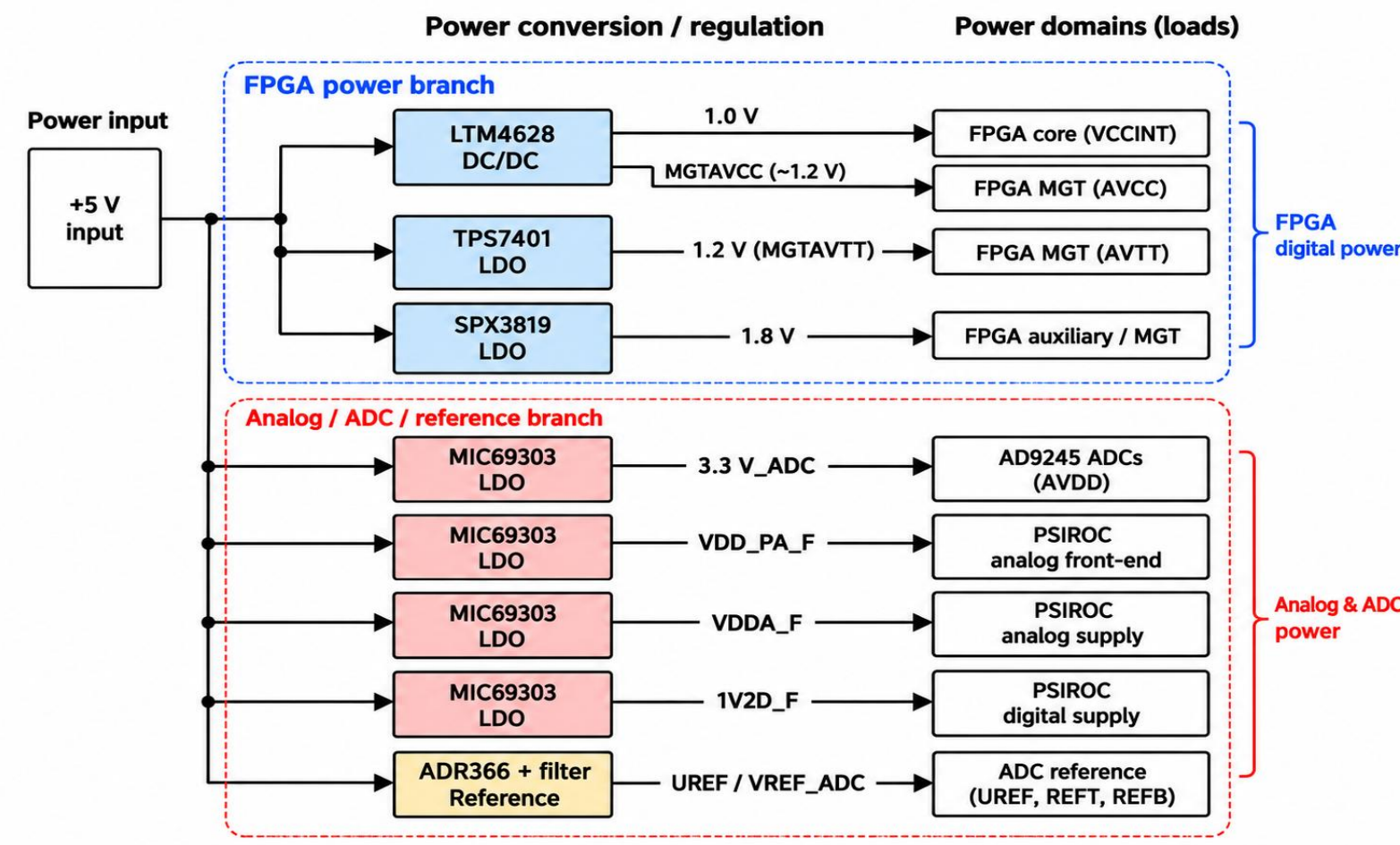
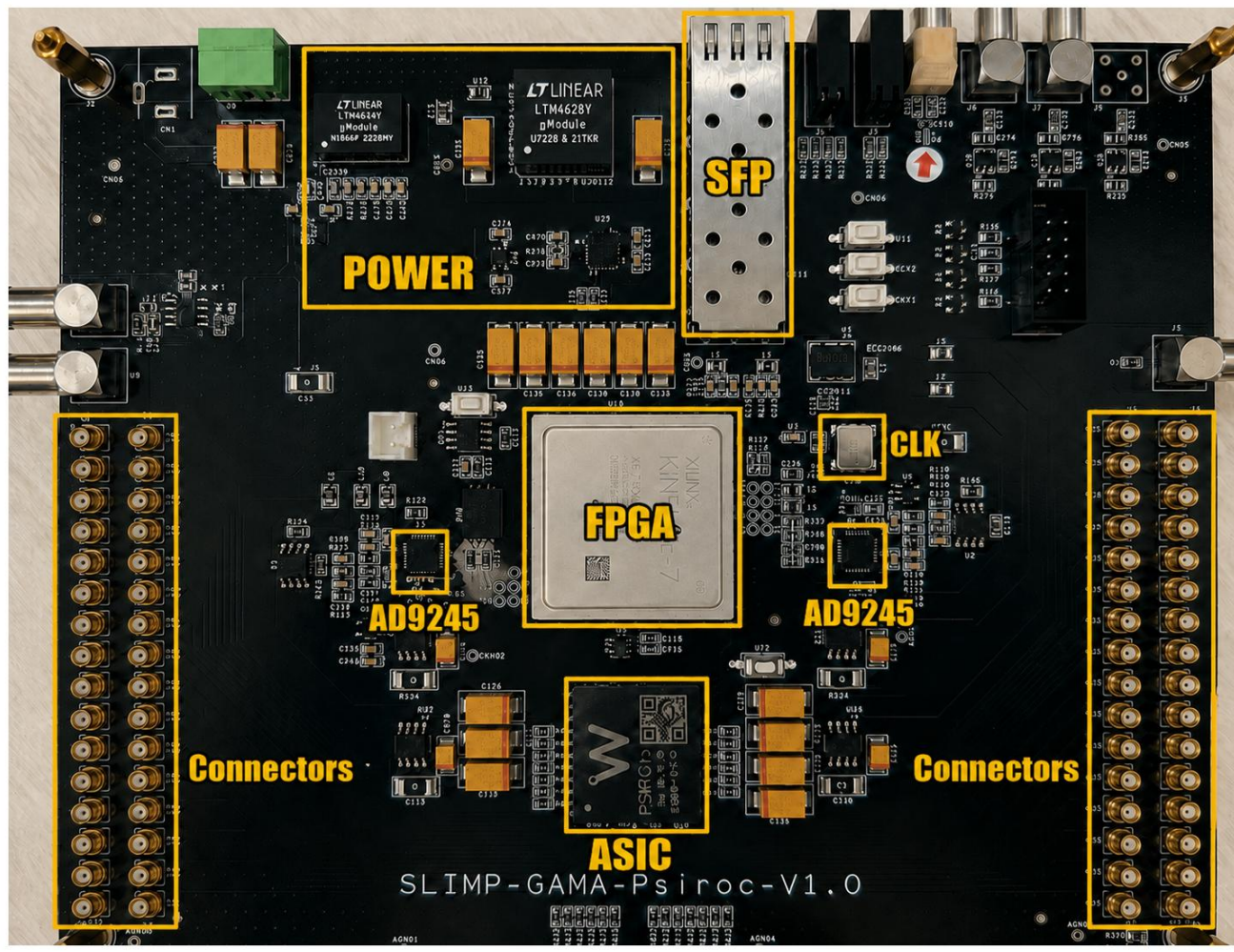
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Abstract

We developed a 64-channel PSIROC readout board for CsI(Tl)-APD detector units in the HIAF-HIRIBL gamma-ray array. Parallel high-gain (HG) and low-gain (LG) paths, two 14-bit ADCs, and FPGA-controlled acquisition provide configurable amplitude measurement and continuous event transfer. Electronic injection tests, a 24 h acquisition run, and ^{60}Co measurements characterize the single-board prototype. The results demonstrate low noise, sub-percent integral nonlinearity, and resolved 1173 and 1332 keV photopeaks.

Detector Requirements and Board Design

- The planned HIAF-HIRIBL gamma-ray array has 1024 CsI(Tl)-APD channels for gamma-ray and light charged-particle measurements.
- One PSIROC ASIC processes 64 inputs through HG/LG shaping and peak-hold chains. Two AD9245 ADCs independently digitize the multiplexed outputs at 14 bits and 40 MSPS.
- A dedicated power network separates FPGA digital, analog, ADC, and ASIC rails. The board draws 4.57 W from 5.0 V with all 64 channels enabled.

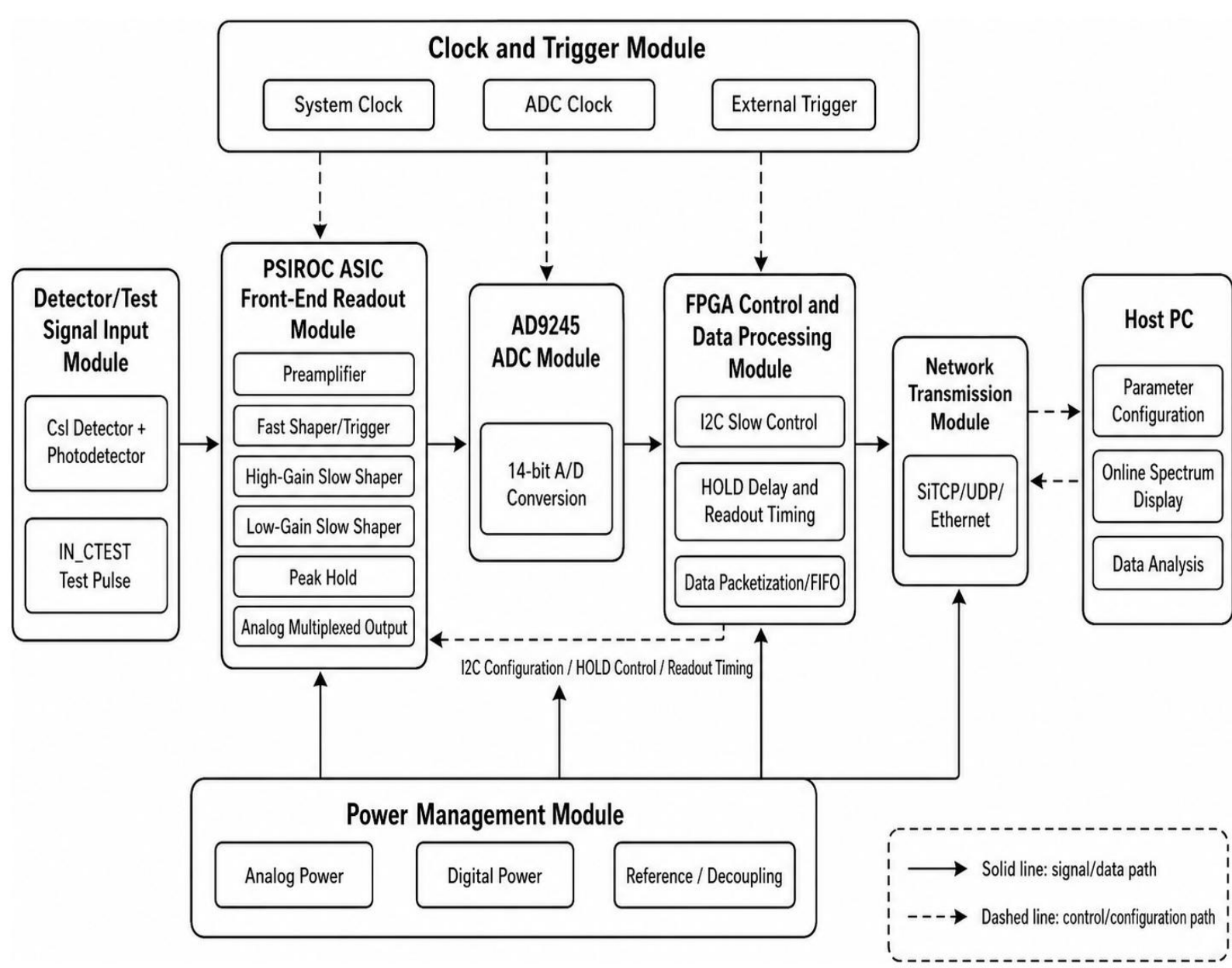


Readout board and power-conversion architecture

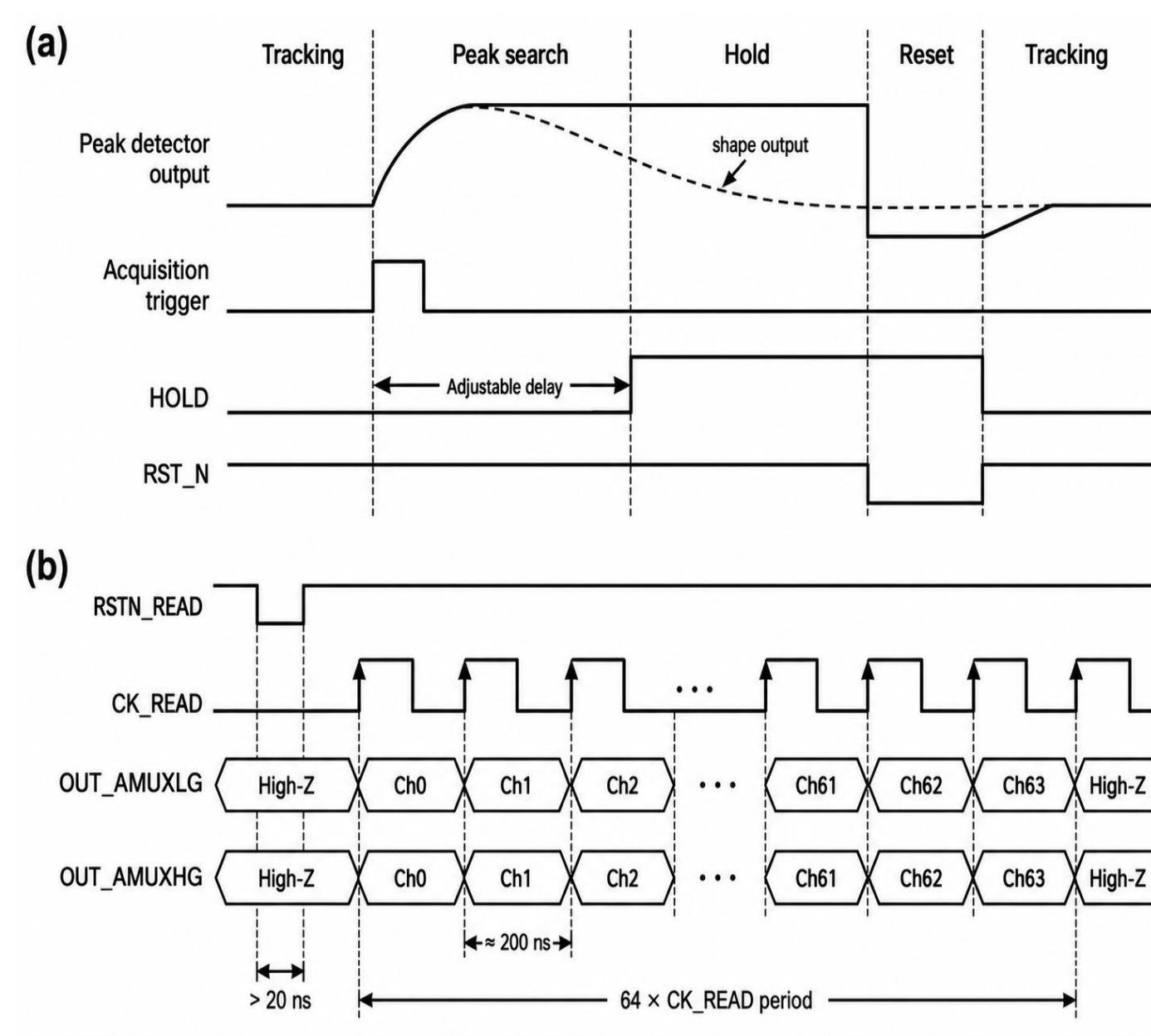
Measured board power: 4.57 W at 5.0 V, all channels enabled.

FPGA Control and Readout Timing

- The FPGA controls ASIC configuration, HOLD generation, CK_READ timing, dual HG/LG sampling, event assembly, and Ethernet transfer.
- The timing diagram shows RST_N, CK_READ, OUT_AMUXHG, and OUT_AMUXLG. Each channel is read with about 200 ns spacing before event packetization.



FPGA control, data processing, and network transfer

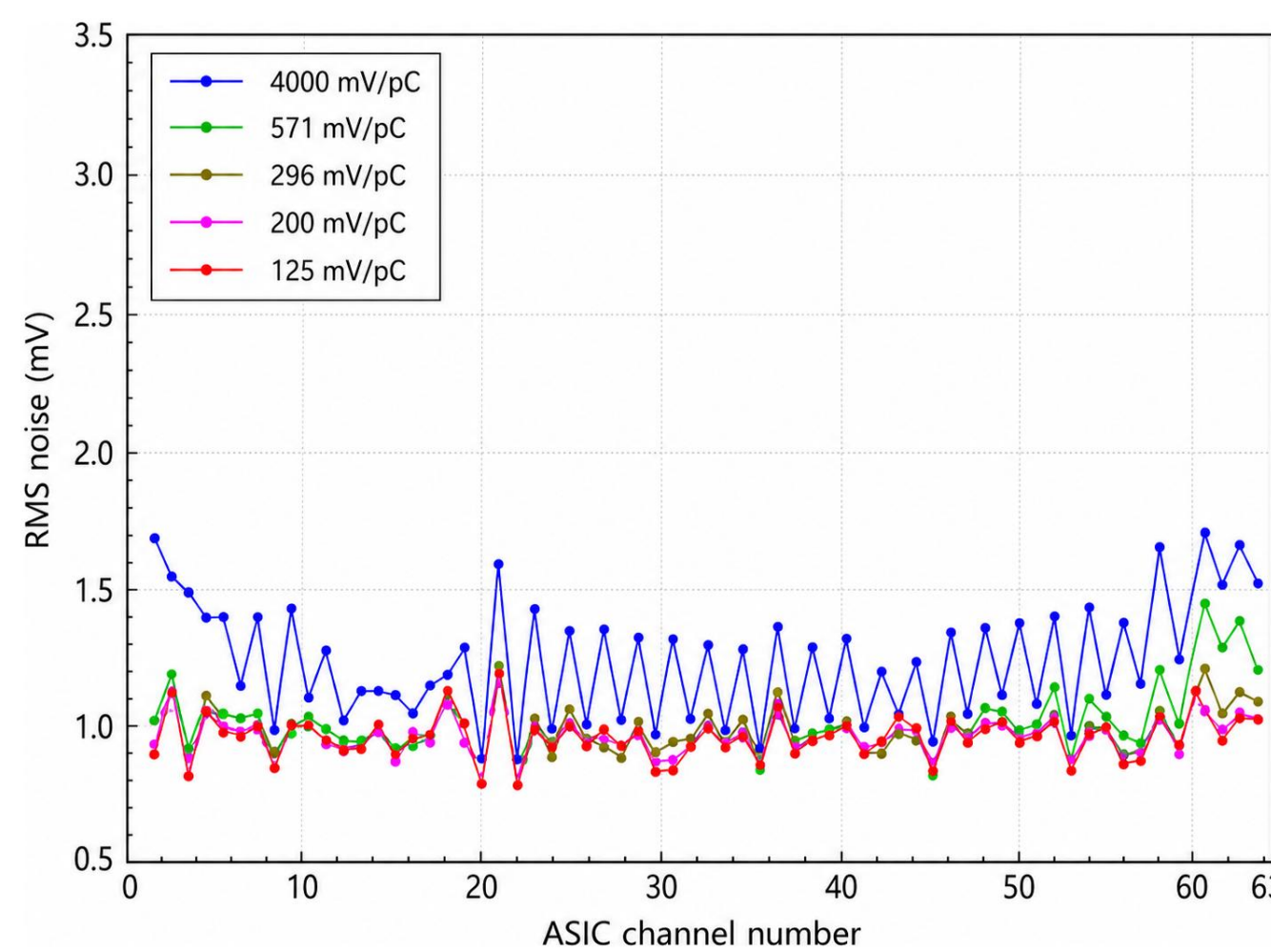


ASIC readout timing

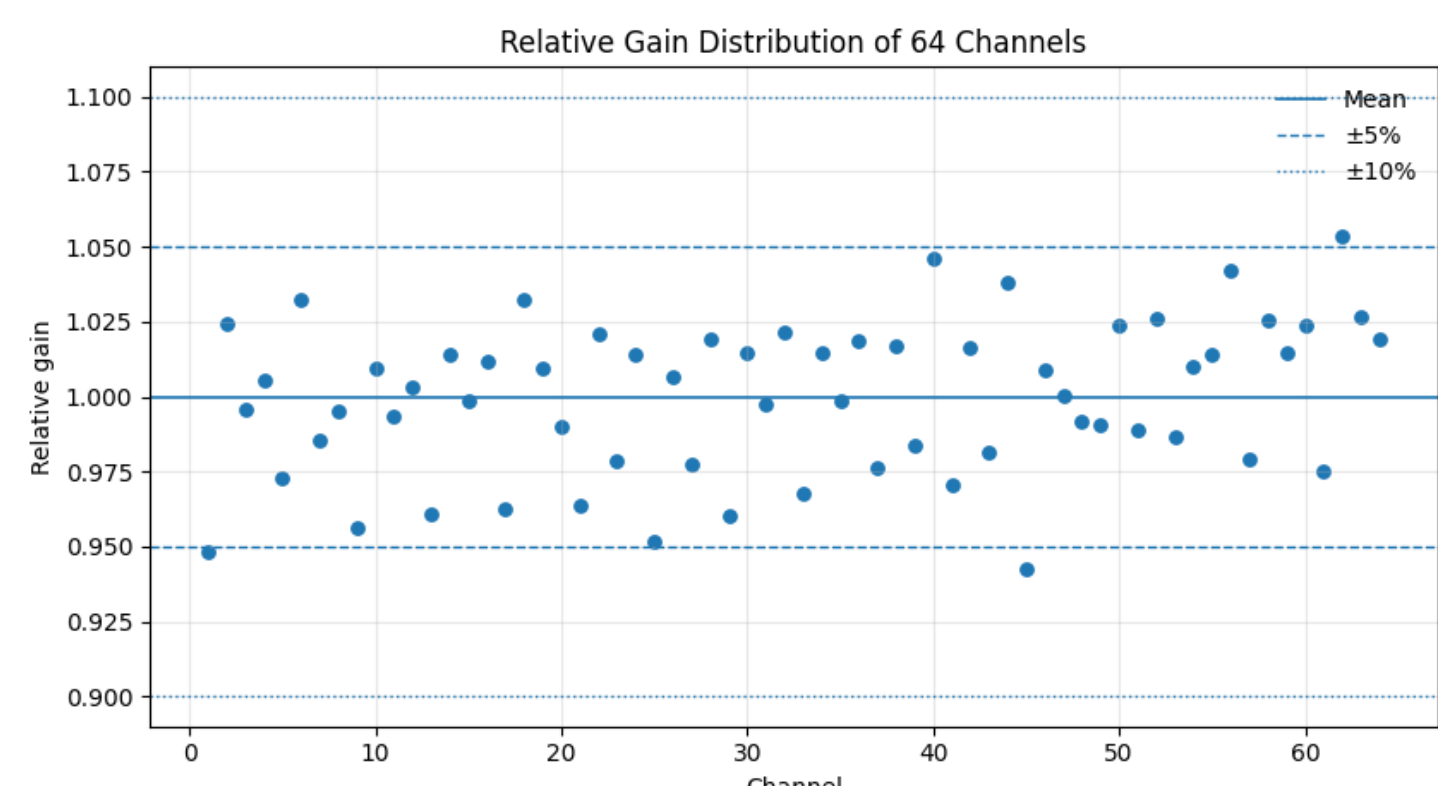
- At a 3 μs shaping time, HOLD follows an accepted trigger by 3.0 μs (120×25 ns). The 64-channel scan takes 25.6 μs at 400 ns per channel.

Noise and Channel Uniformity

- Noise measurements use 10^5 baseline samples per channel at -380 V APD bias, with test injection disabled.
- RMS noise is <1.4 mV at 125–571 mV/pC and <1.7 mV at 4000 mV/pC. No isolated high-noise channel appears.
- The relative-gain coefficient of variation is 2.54%. 61/64 channels lie within $\pm 5\%$ of the mean. The largest deviation is 5.73%, motivating individual channel calibration.

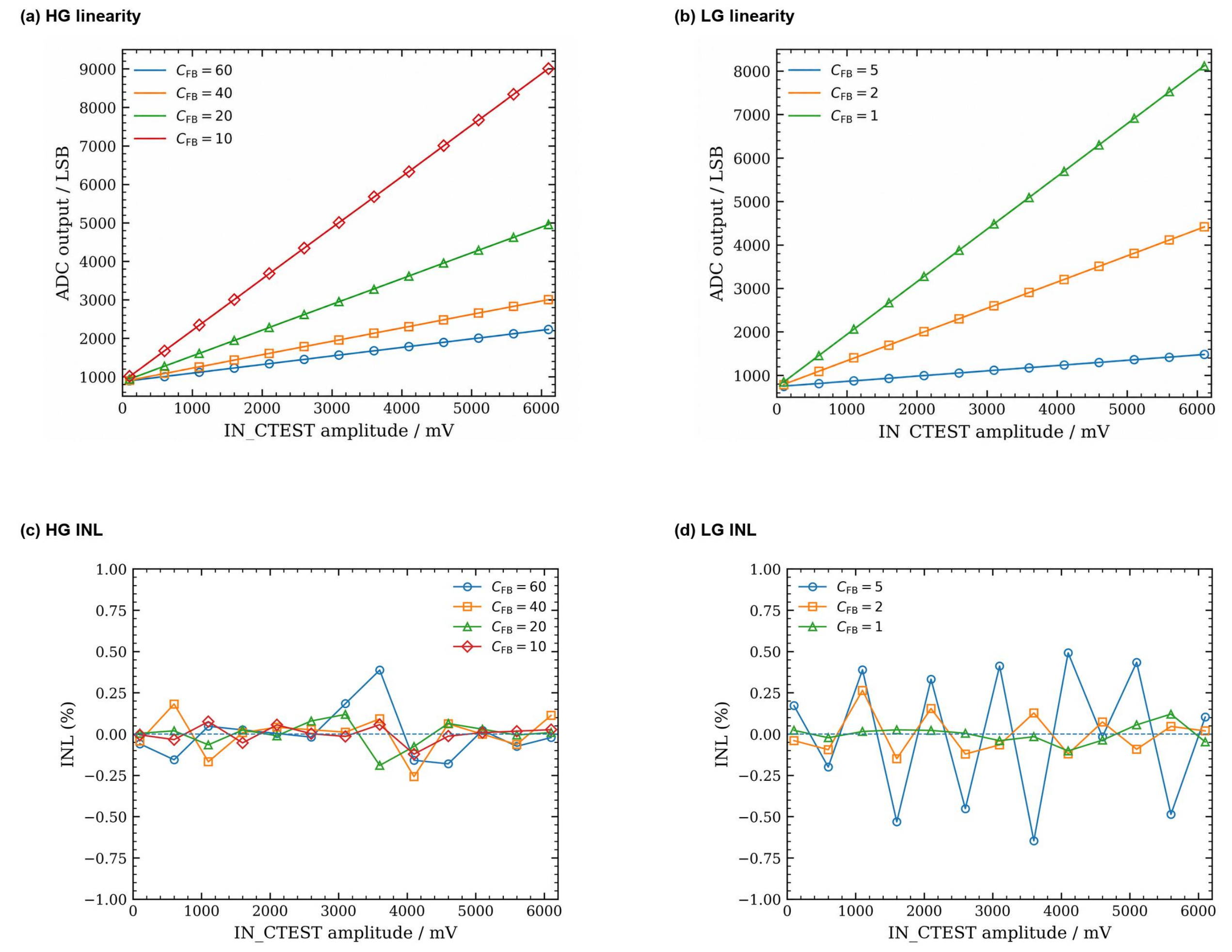


64-channel noise distribution and relative gain



Linearity and Integral Nonlinearity

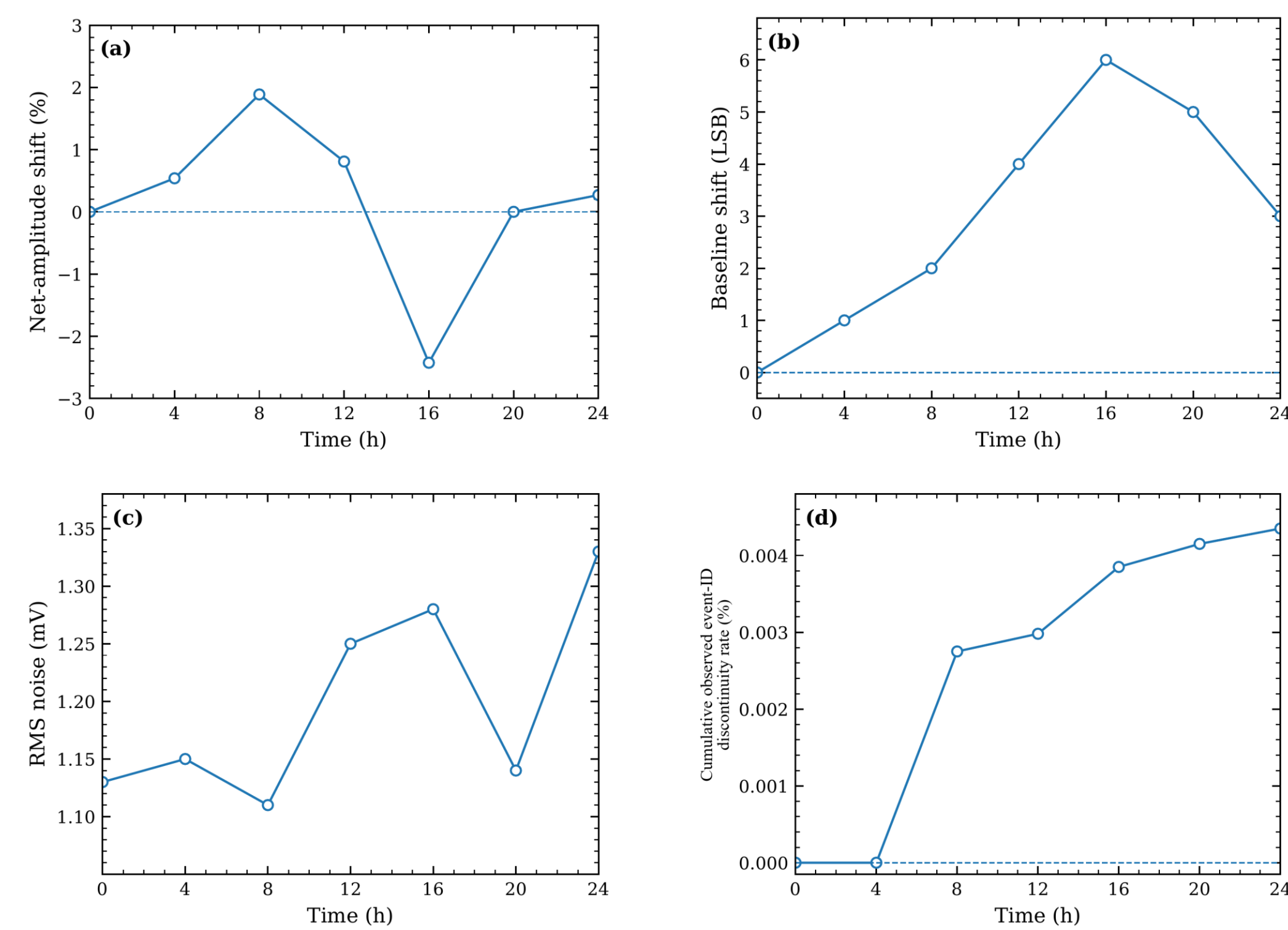
- Charge-injection scans vary the input amplitude and feedback code. Smaller feedback capacitance increases the HG/LG conversion gain.
- INL is the residual from a least-squares line, normalized to the effective output span. Maximum |INL| is 0.387% for HG and 0.646% for LG across the tested settings.



HG: codes 60, 40, 20, 10. LG: codes 5, 2, 1.

Trigger Rate and 24 h Stability

- Periodic triggers are recorded through 31 kHz. At 32 kHz, the recorded rate falls to 16.001 kHz, constraining busy time to $31.25 \mu\text{s} < T_{\text{busy}} \leq 32.26 \mu\text{s}$.
- A 500 mV pulse at 20 kHz drives the 24 h test. The recorded rate varies by $<0.01\%$, with no software crash or network disconnection.



Net amplitude, baseline, RMS, and event-ID continuity

24 h metrics

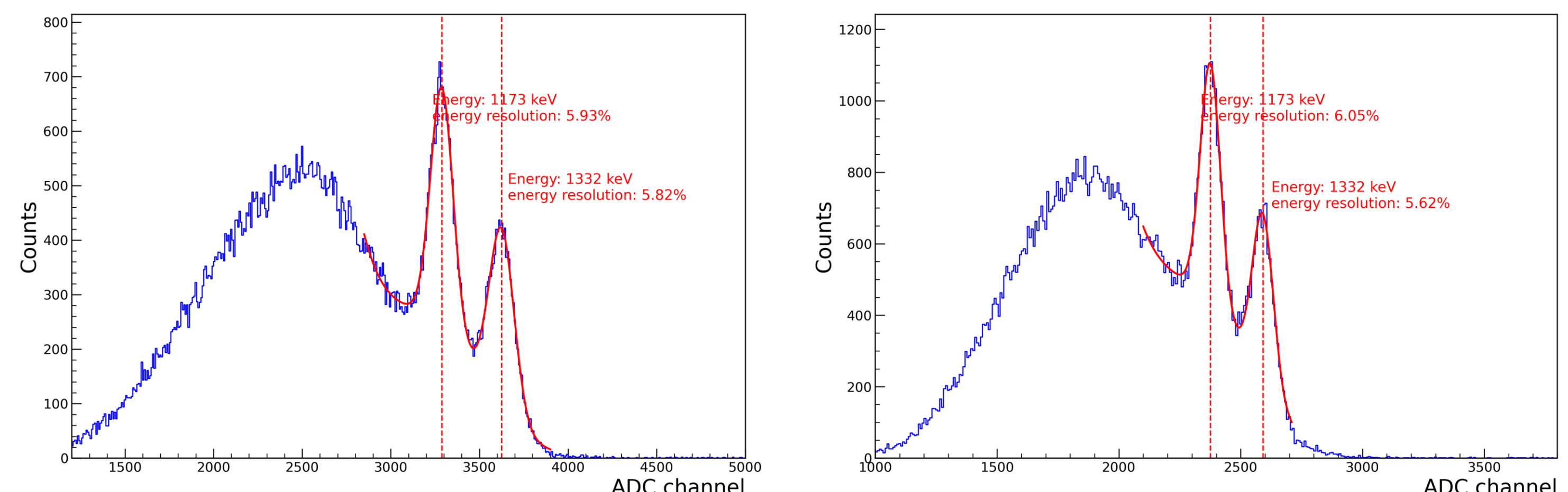
Net amplitude
max. 2.43%
final +0.27%

RMS noise
1.11–1.33 mV

Observed ID
discontinuity
0.00435%

^{60}Co Spectroscopy with CsI(Tl)-APD

- The same 130 mm CsI(Tl) crystal and S8664-1010 APD at -380 V are used for all configurations, with fixed geometry and trigger conditions.
- All eight gain settings resolve 1173 and 1332 keV photopeaks. FWHM resolution is 5.62–6.41% for HG and 6.58–7.19% for LG. The best value is 5.62% at 1332 keV (HG code 32).



HG code 20: 5.93% / 5.82%. HG code 32: 6.05% / 5.62%.

Summary: The single-board prototype achieves 64-channel dual-gain amplitude readout, $|\text{INL}| < 0.65\%$, and continuous acquisition at 20 kHz for 24 h. Random-trigger response and array-level operation remain to be evaluated.