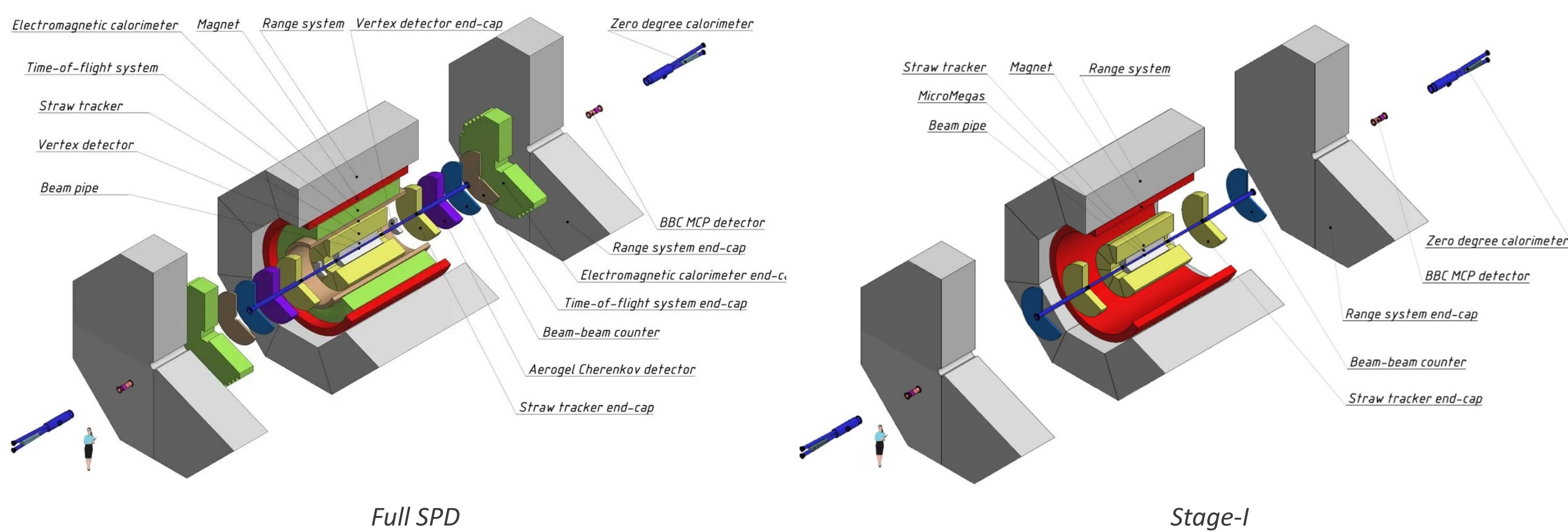


SPD-NICA | Stage-I

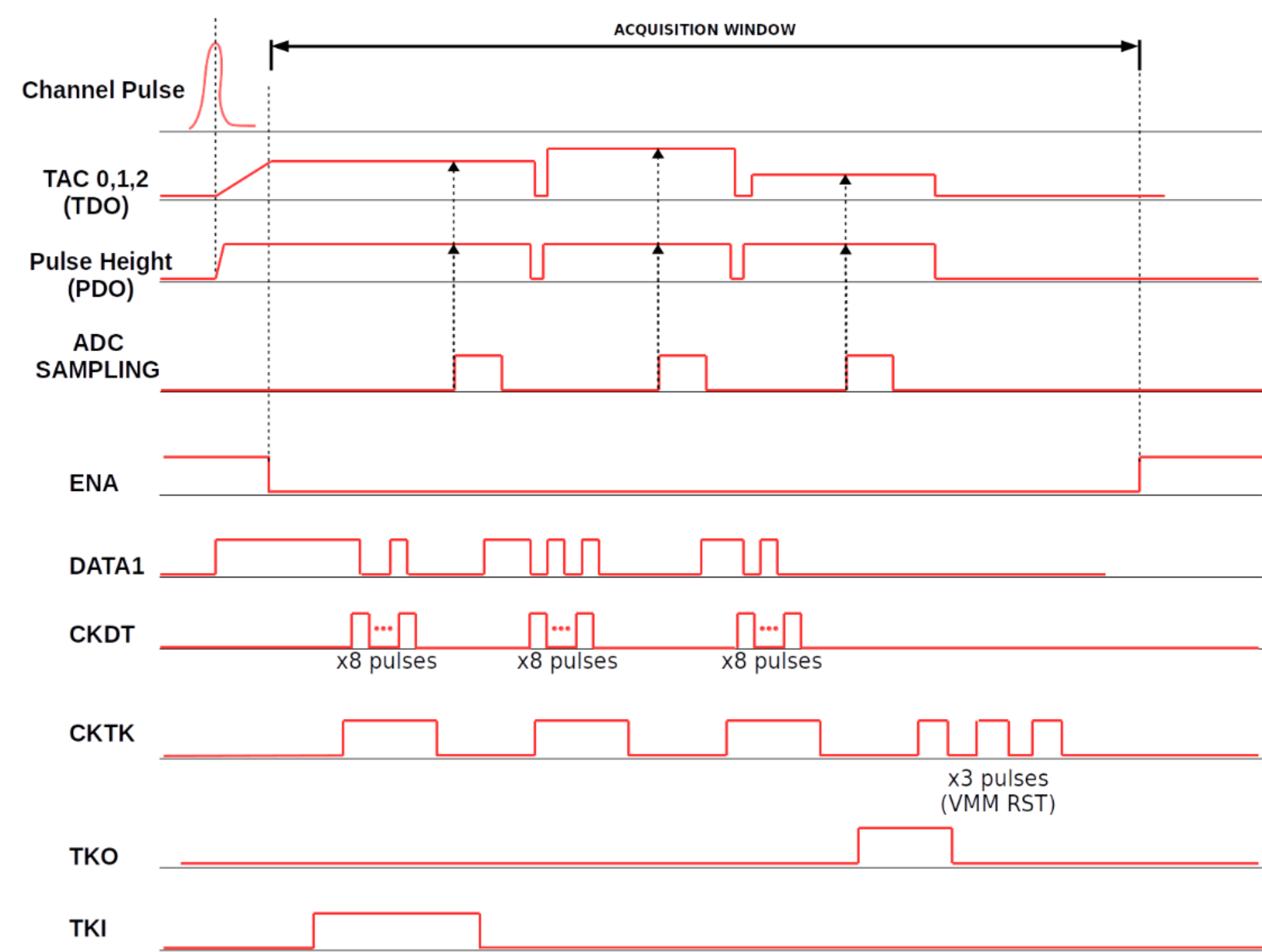
SPD is the Spin Physics Detector at the NICA Collider at JINR, Dubna. At Stage-I there will be no silicon vertex detector, time-of-flight, Cherenkov counter or fully assembled calorimeter. This means that the Straw Tracker performs both track reconstruction and particle identification.

- The readout has to serve ~30 000 channels
- Better than 200 μm spatial resolution
- Simultaneous 20% charge resolution for dE/dx PID



Sample-and-hold

The new design utilizes a mode of operation of the VMM3a ASIC that is not commonly used. Operating in Two-Phase Mode prevents the ASIC from a known channel-latching issue while measuring Time-at-Threshold. A significant improvement in the digitization resolution is shown below. The main drawback is the speed. While a series of channels is digitized, the whole VMM3a ASIC has to be shut down and accepts no new events.



- Once the process is complete the ASIC can be switched readout phase. The first set of amplitude and time voltages is made available at the analog outputs. The address of the channel is serialised and made available at the digital output using six data clocks.

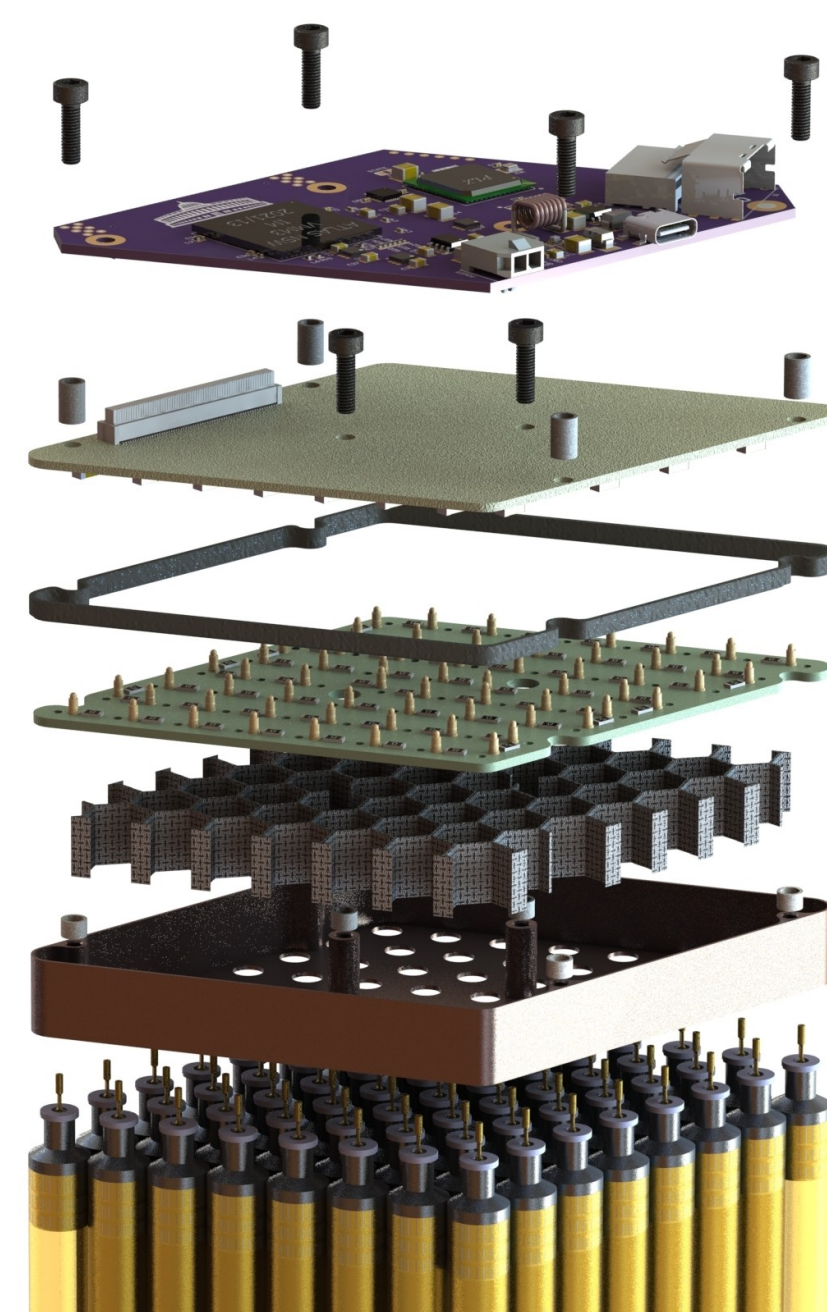
VMM sample-and-hold readout. While ENA is low the chip is read out and accepts no new hits. That interval is the dead time.

On-chamber stack

Because of the space limitations, the front-end readout chain has been designed as a stack of three different boards. A high-voltage distribution board is directly attached to the detector, a “motherboard” with AC-coupling capacitors is placed on top, and the readout electronics is then installed. A fully assembled tower is shown below:



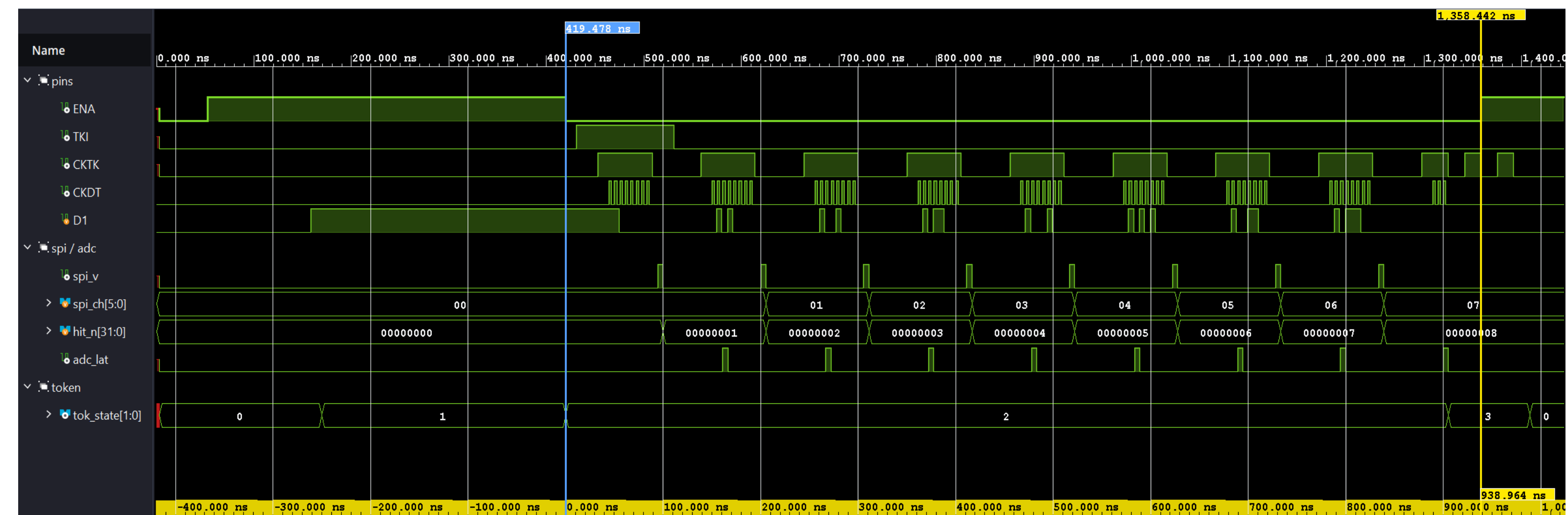
Readout “diamond” on the barrel high-voltage motherboard



Readout efficiency

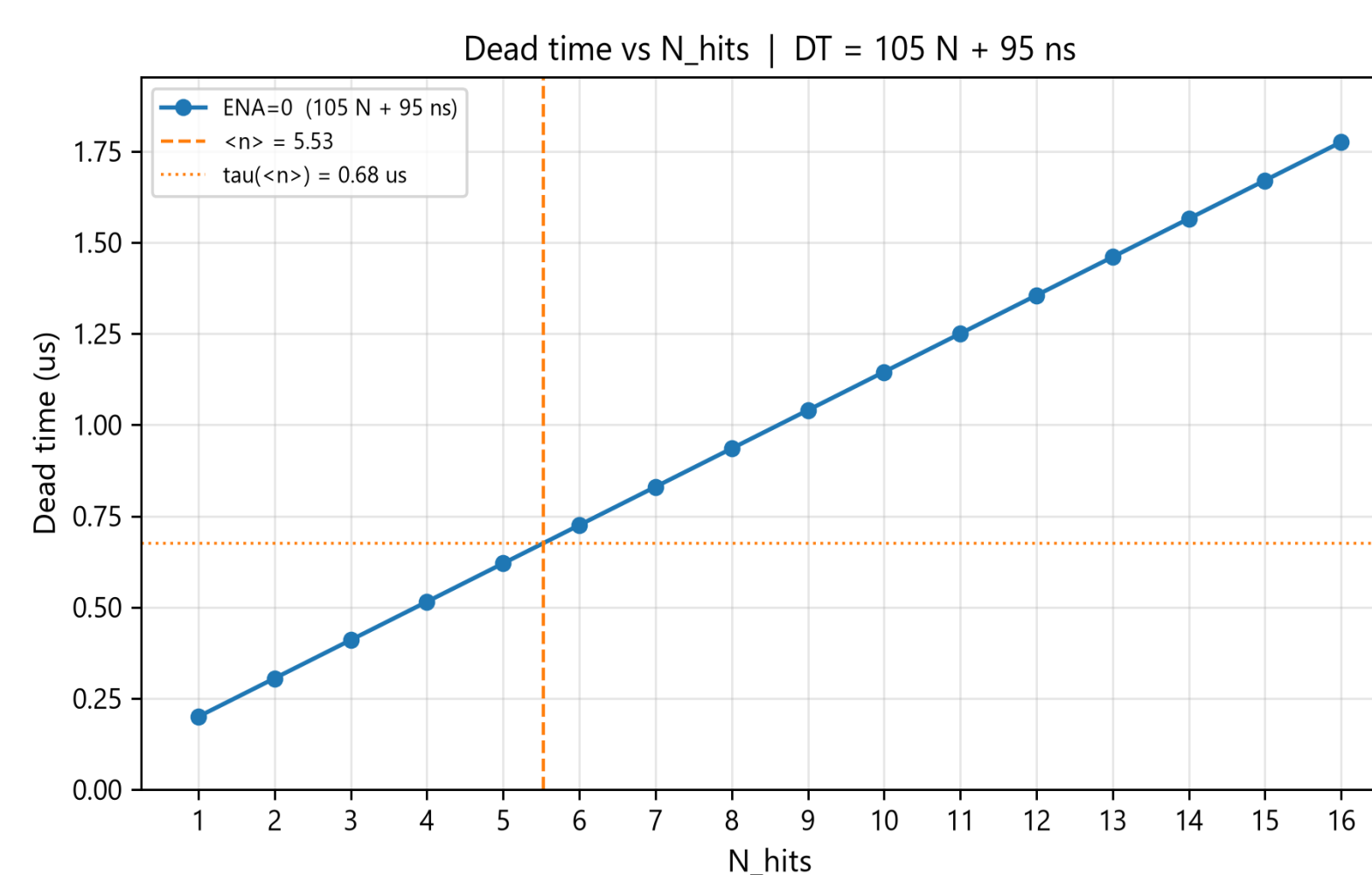
The main challenge was to achieve reasonable dead time. Readout depends on the token injection time and on both edges of CKTK. Below about 40–50 ns on either the high or the low half, channels could get skipped, hits could get duplicated, the event could be lost, or the readout may hang.

Typical event size in the straw tracker cell will be 8 channels. As shown on the plot below, in our new design with Spartan-7 FPGA we managed to reduce the dead time to less than 1 μs . While this time is still worse than in the normal continuous-readout mode of the VMM3a ASIC, it is more than enough to operate with the hit rate of 10–20 kHz per channel which is reasonable for the SPD Stage-I.

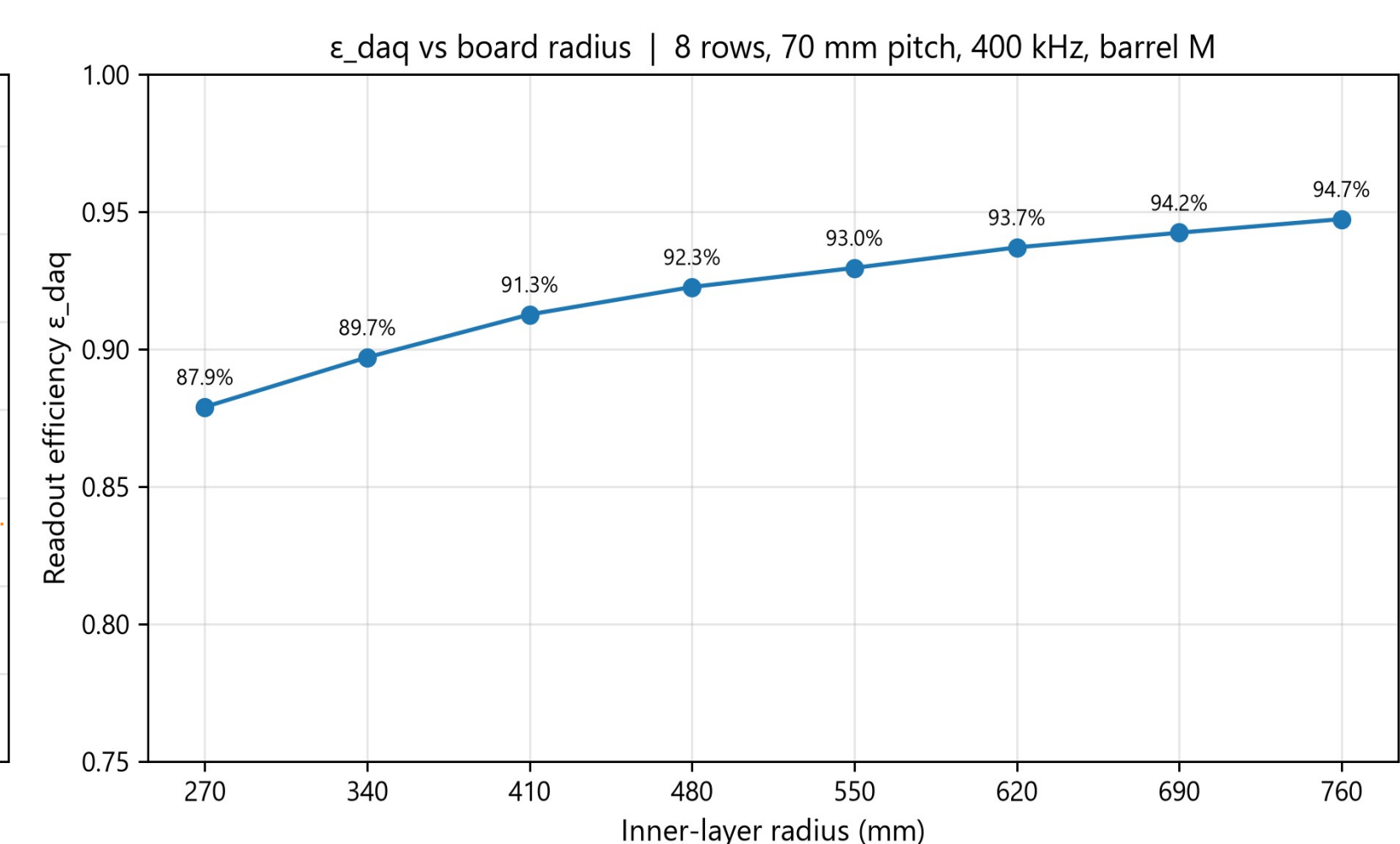


Stable sample-and-hold timing

$DT(N) = 105 N + 95 \text{ ns}$. An eight-hit event takes 940 ns.



Dead time $DT(N) = 105 N + 95 \text{ ns}$



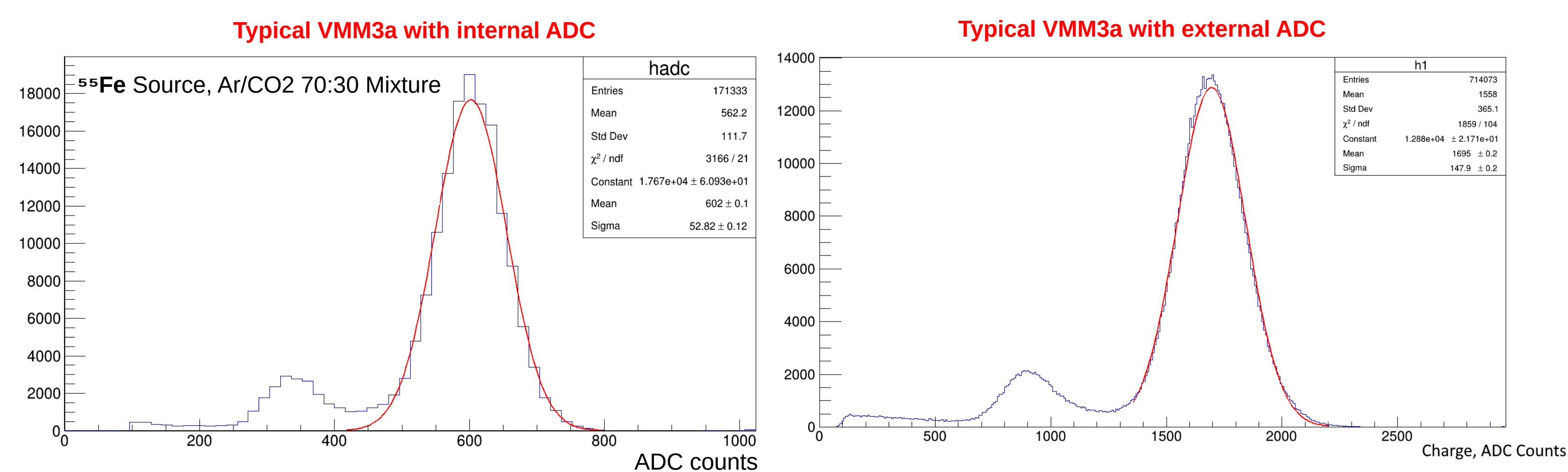
Efficiency versus radius at 400 kHz

Estimated readout efficiency of a 64-channel VMM3a-based straw tracker board at Stage-I.

NICA interaction rate: 400 kHz + 100 Hz of noise on every tube

- 87.9% at 270 mm, rising to 94.7% at 760 mm
- Inner board: mean event size 5.53, dead time 0.68 μs
- Inner board: 217 kHz events and 53.5 Mbit/s, about 5% of the 1.25 Gbit/s line
- Noise of 100 Hz per tube changes the efficiency from 88.1% to 87.9%

Readout tests



Developed readout boards have been attached to the prototype straw chambers and tested with radioactive sources in the lab. Also several test beams with 150 GeV/c muons at the CERN SPS and with 1–15 GeV/c protons at the PS have been arranged.

The external-ADC mode is flexible enough to integrate the boards into the triggerless SPD DAQ.

Significant improvement of the ADC resolution can be observed.

No channel latching has occurred during the test beams.

Conclusions

- At SPD-NICA Stage-I the Straw Tracker is used for both momentum reconstruction and particle identification.
- A new front-end electronics solution has been designed for the first stage of SPD-NICA Straw Tracker.
- In order to achieve the best performance for the straw tubes, we have developed a completely new circuit, including differential buffering and external ADCs.

- We managed to utilize the existing VMM3a ASIC originally designed for the ATLAS Micromegas detector.
- That helped us to achieve a low-cost design with a price of ~\$5 per channel and a power consumption of about 30–40 mW per channel.
- The device is a complete multichannel solution for collection, amplification and digitization of incoming signals.