

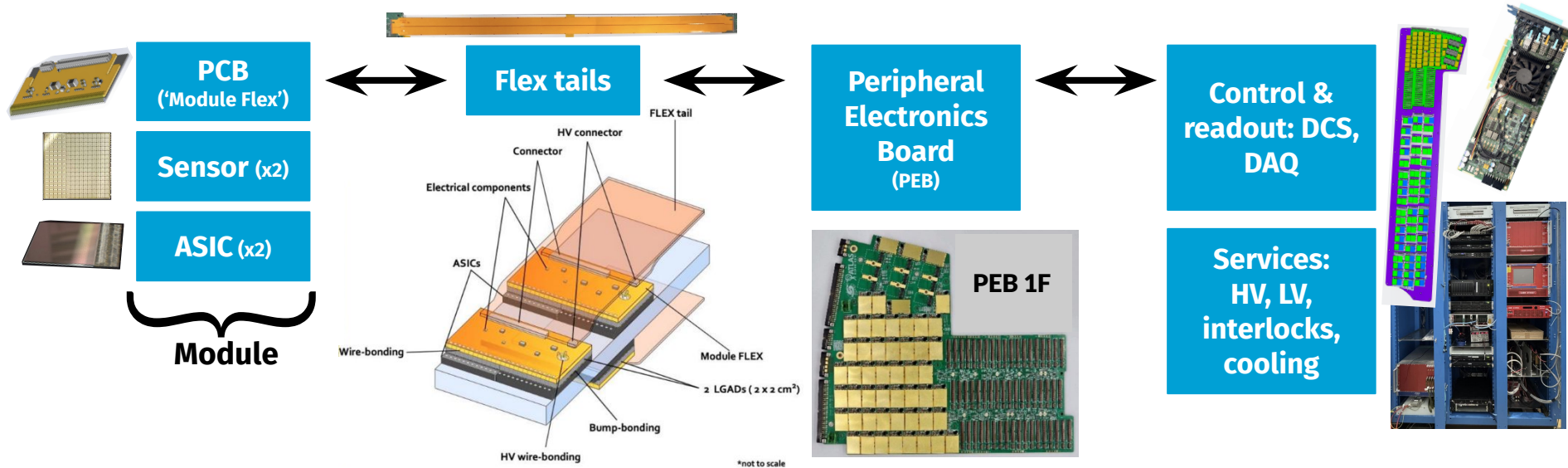
International Conference on Instrumentation for Colliding Beam Physics, Hefei, China (INSTR2026)

Development and Characterisation of Sensors and Electronics for the ATLAS High-Granularity Timing Detector

Steffie Ann Thayil (CERN, Switzerland), on behalf of the ATLAS HGTD Group

13 October, 2026

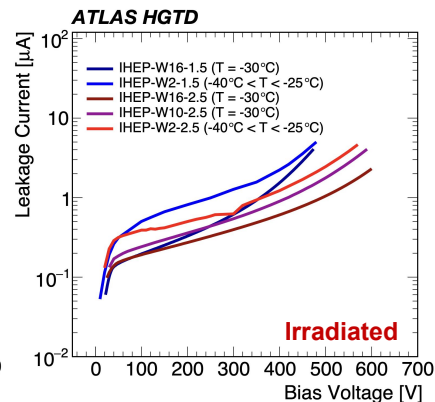
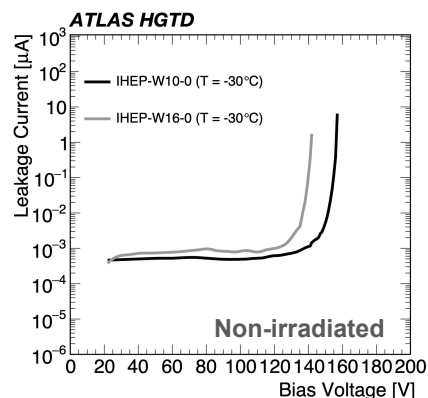
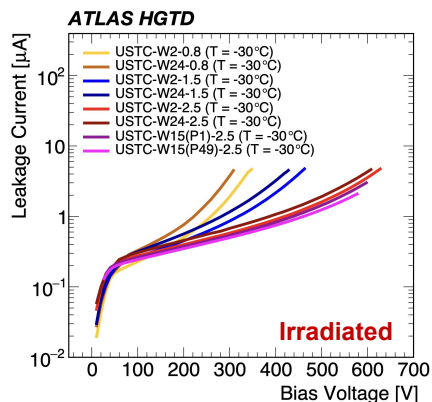
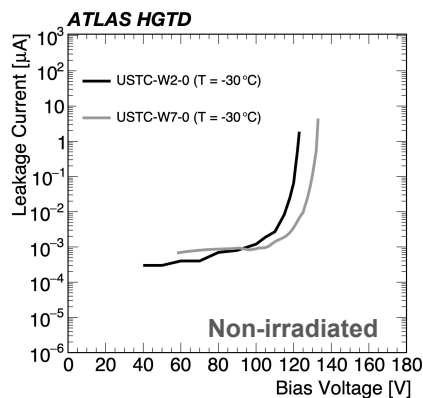
The ATLAS High Granularity Timing Detector



- ❖ **ATLAS HGTD:** Phase-II upgrade designed to provide **precision timing** in the forward region + **luminosity** measurement ([Tao's talk](#))
- ❖ **HGTD Modules:**
 - 15 x 15 grid of **LGAD sensors** providing **excellent time resolution** ($< 40 \text{ ps}$ pre-irradiation, $< 50 \text{ ps}$ at End of Life)
 - Bump-bonded to the **ALTIROC** front-end ASIC, also with 15 x 15 channels, to form a 'hybrid'
 - Modules are made of 2x hybrids + **Module Flex** PCB
- ❖ 6 types of **Peripheral Electronics Board (PEB)** supply power to, get data from multiple modules via '**flex tails**' + send data off-detector

Sensors: Low Gain Avalanche Detectors

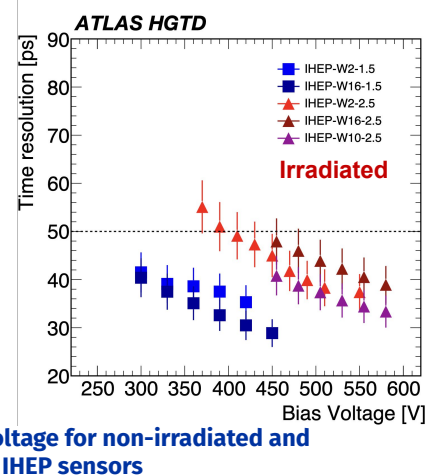
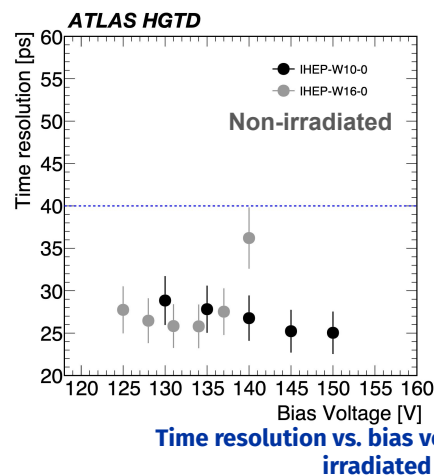
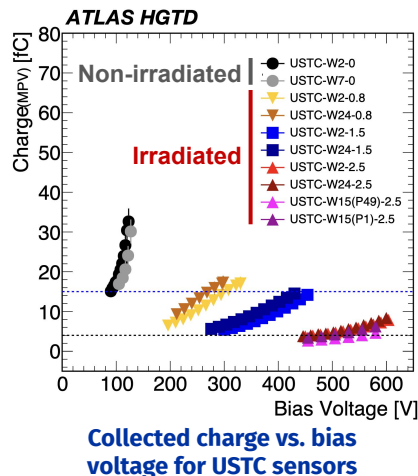
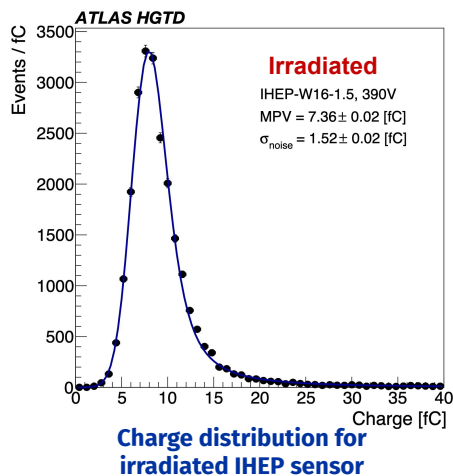
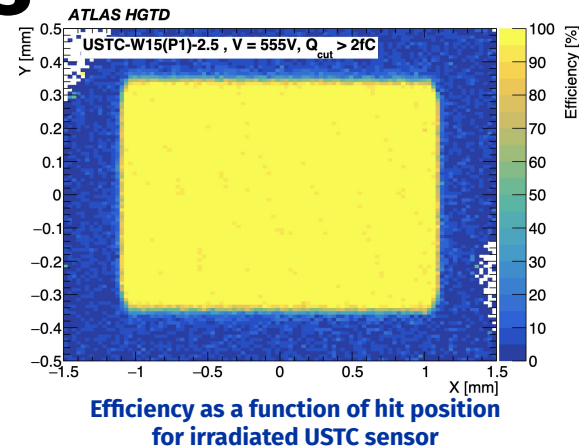
- ❖ **n-in-p diode** with an **additional p⁺ gain layer**; high E field produces **avalanche gain** through impact ionisation
- ❖ 50 μm active thickness: **fast charge collection** + **low Landau fluctuations** → Fast **rise time**, high **S/N**, excellent **time resolution**
- ❖ HGTD end-of-life requirement: fluence up to $2.5 \times 10^{15} \text{ n}_{\text{eq}}/\text{cm}^2$ at R = 12 cm
- ❖ p⁺ gain layer is doped with B, irradiation causes acceptor removal; **extra C implantation** protects dopants and makes sensor more radiation-hard. **Increasing bias voltage** also partially recovers the electric field and gain **after irradiation**.
- ❖ Bias voltage limited to **~550 V**; at higher fields, irradiated 50 μm sensors become susceptible to **single-event burnout**



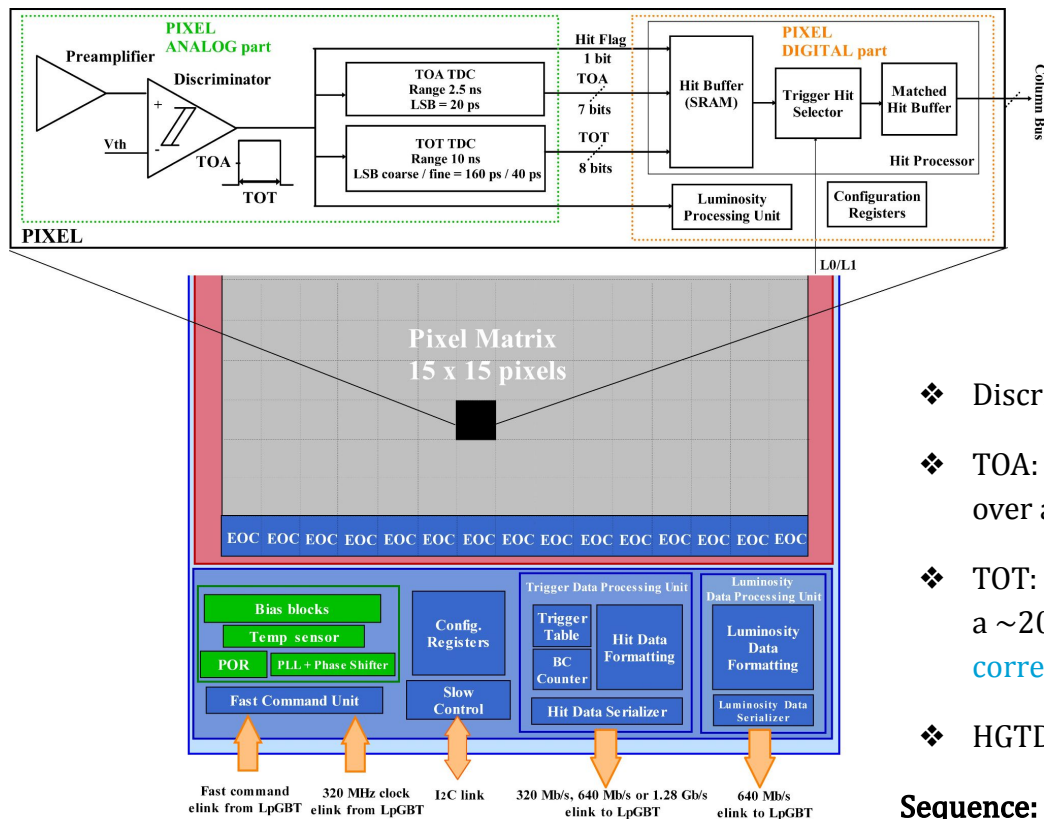
USTC and IHEP sensor leakage currents vs. bias voltage, at various irradiation fluences

Testing the HGTD LGAD sensors

- Pre-production IHEP-IME and USTC-IME single-pad LGADs from QC test structures characterised using test beams, **before and after irradiation** at fluences up to $2.5 \times 10^{15} \text{ neq/cm}^2$
- Collected charge $>15 \text{ fC}$ and time resolution $<40 \text{ ps}$ before irradiation, $>4 \text{ fC}$ and $<50 \text{ ps}$ after irradiation at max fluence; meets HGTD requirements
- Hit efficiency $>95\%$ up to max fluence, with good spatial uniformity across the active area (USTC sensor size: $2.27 \times 0.75 \text{ mm}^2$)



ASICs: ALTIROC-A

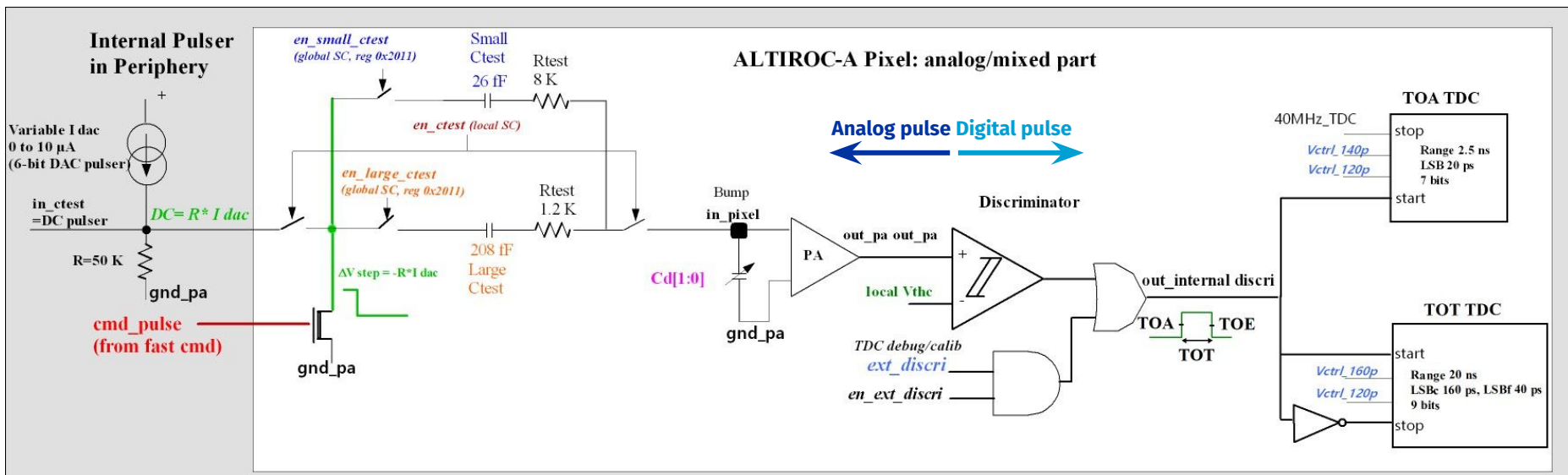


- ❖ ALTIROC development has progressed through several iterations from the 4-pixel ALTIROC-0 to the **225-pixel ALTIROC-A**, progressively **adding functionality** and **improving performance**
- ❖ ALTIROC-A: **timing ASIC** fabricated in **TSMC 130 nm CMOS** on a $2 \times 2 \text{ cm}^2$ die, matching the 15×15 LGAD matrix
- ❖ Preamplifier: ~ 1 GHz-bandwidth front-end providing **fast amplification of the LGAD signal**
- ❖ Discriminator: Fast leading-edge disc., programmable threshold
- ❖ TOA: **7-bit TDC with a 20 ps bin**, using a cycling Vernier delay line over a **2.5 ns range**
- ❖ TOT: **9-bit TDC with 40 ps binning**, measuring the pulse width over a ~ 20 ns range to provide amplitude information for **time-walk correction**
- ❖ HGTD end-of-life requirement: TID of **2 MGy / 200 MRad**

Sequence: **LGAD signal** $\rightarrow$ Analog processing $\rightarrow$ **TOA/TOT** $\rightarrow$ Digital readout (**Timing data** + hit counting for **luminosity data**)

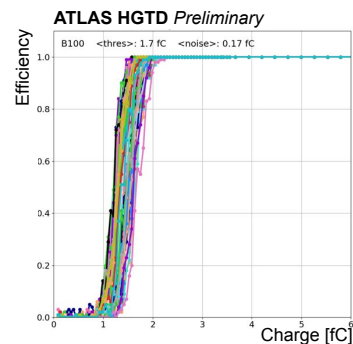
ALTIROC-A calibration pulse circuitry

- ❖ ALTIROC-A includes dedicated calibration circuitry to characterise the analog readout chain and calibrate the timing response without relying on an external LGAD signal
- ❖ The internal DAC pulser injects controlled charge pulses through the small or large calibration capacitor, allowing emulation of LGAD signals; these pulses are used to tune the chip and to measure noise, efficiency, jitter, etc.
- ❖ The ext_discri signal is generated internally from the fast CAL command, bypassing the analog path, and is used for TDC calibrations

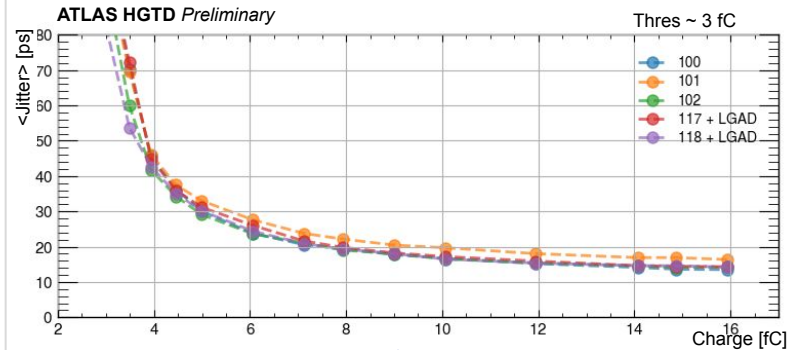


Testing the ALTIROC-A ASICs

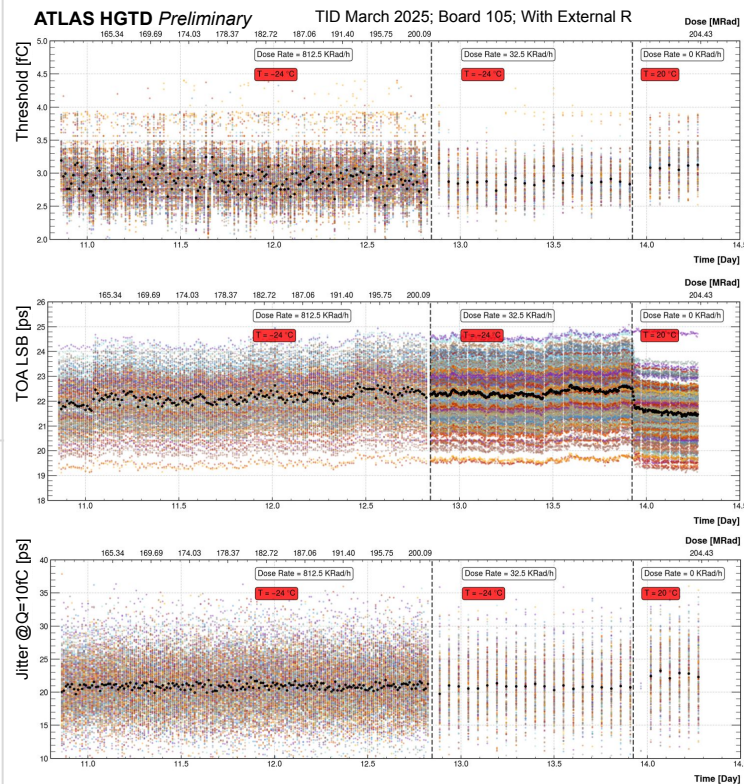
- ❖ ALTIROC-A has been extensively characterised at ASIC level, including standalone test-bench measurements and irradiation studies
- ❖ The ASIC remains stable beyond the HGTD specification of 200 MRad (2 MGy), as seen in the plots on the right
- ❖ With the ASIC alone:
 - The minimum detectable charge or Q_{min} is close to 2 fC
 - The jitter (main ASIC contribution to time resolution) is below 25 ps at 10 fC when the chip is tuned to 3 fC



Minimum detectable charge



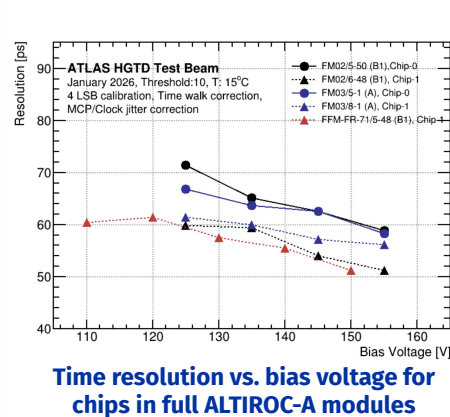
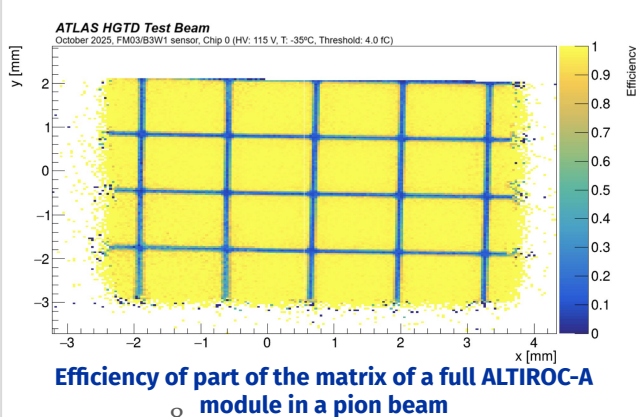
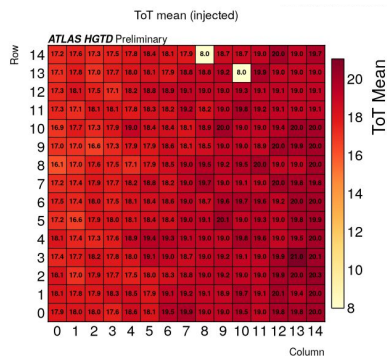
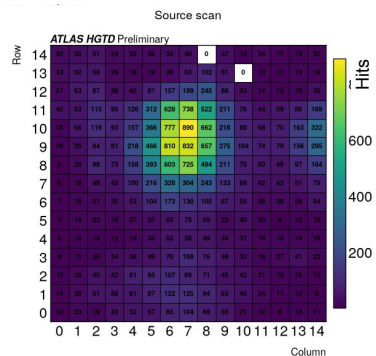
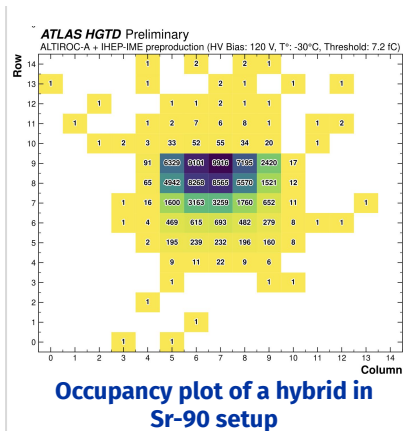
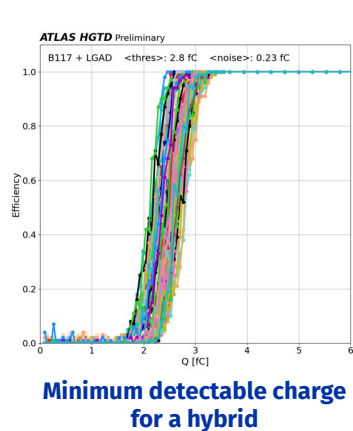
<TOA RMS> as a function of detected charge



Effect of radiation on various ALTIROC-A metrics

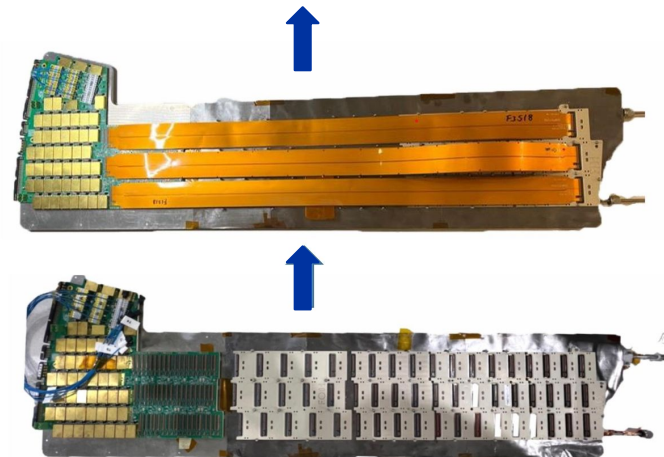
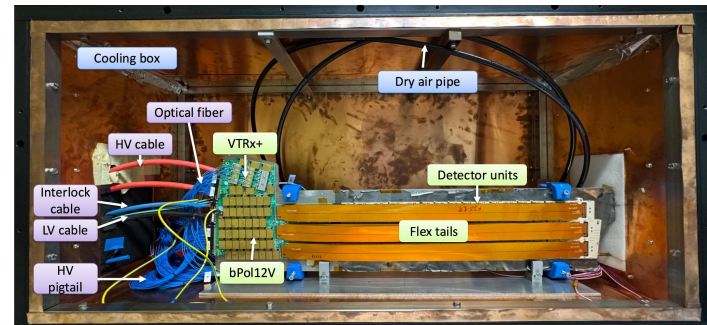
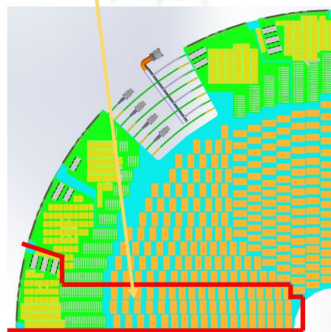
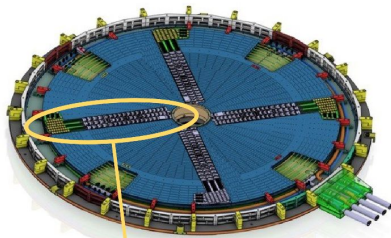
Putting things together: Hybrids & modules

- ❖ LGADs and ALTIROC-A ASICs are **bump-bonded** to form **hybrids**, pairs of which are then assembled with a module flex into **full HGTD modules**
- ❖ Both hybrids and full modules have been characterised on the **test bench**, using internal charge injection, as well as using a ^{90}Sr source and in **testbeams**
- ❖ They demonstrate **good pixel connectivity** and **high hit efficiency**
- ❖ Hybrids achieve a **Q_{min} of ~ 3 fC** and a **time resolution below 50 ps**, while full modules achieve **~ 4 fC and ~ 55 ps**, respectively



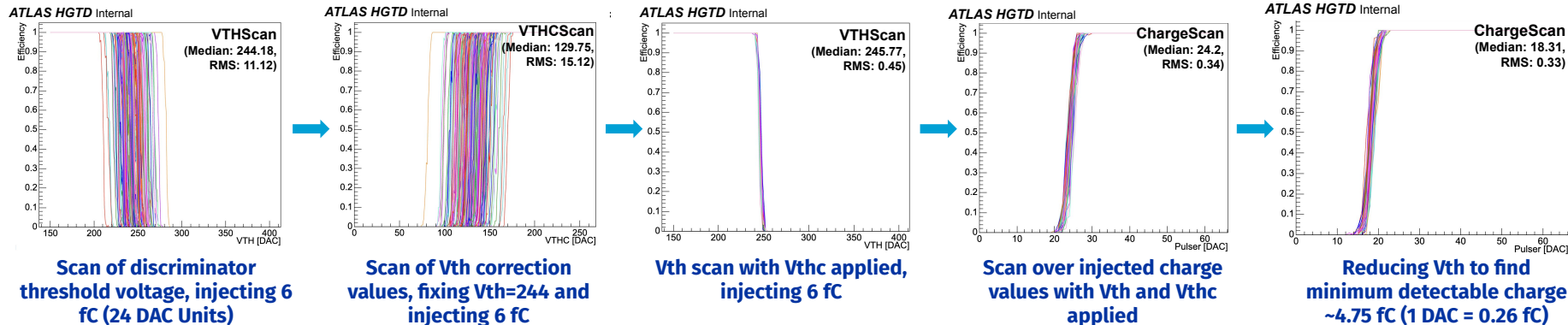
Putting things together: Demonstrator

- ❖ The demonstrator setup at CERN allows us to **exercise the full chain**, from **modules**, connected to the **PEB** via **flex tails**, up to the **DAQ server**
- ❖ Currently uses **PEB1F prototype**
- ❖ LV provided by **CAEN BRIC modules**, HV provided by **Fullde HV crate**
- ❖ Interlocks provided by **LISSY crate**, connected to **temperature sensors** on certain module flexes
- ❖ PEB and modules mounted on a **cooling plate**, inside a cooling box which can be operated at **-30°C**
- ❖ Building up **DCS** and **DAQ** to be compatible with final ATLAS specifications
- ❖ Offers the opportunity to **do sanity tests** with **realistic services and mechanics**

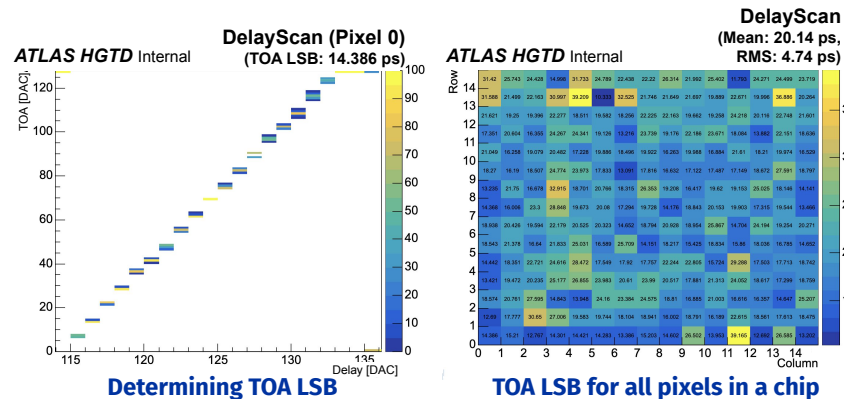


Demonstrator v1 with PEB 1F

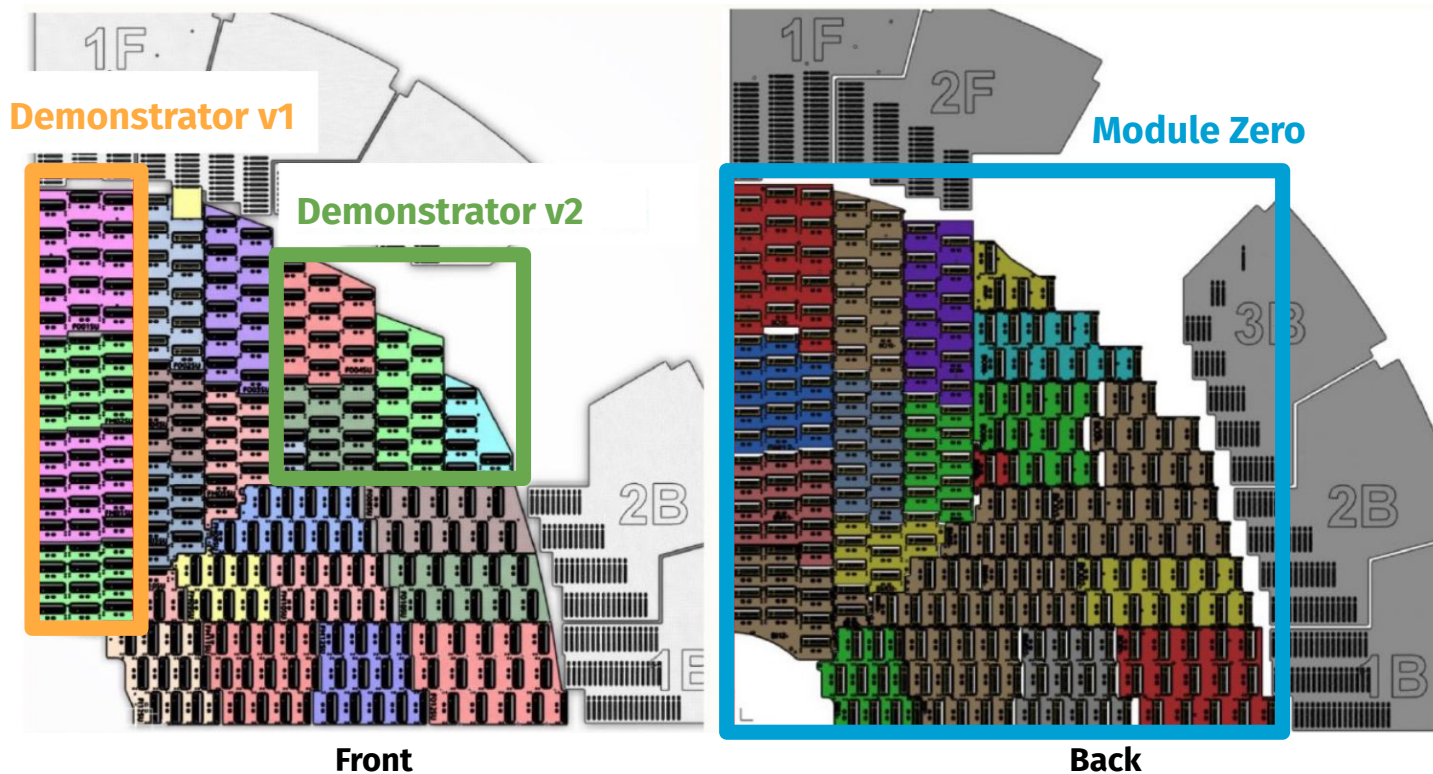
Tests with the Demonstrator



- ❖ The demonstrator is tested **without an external particle source**, representative of how the final HGTD system will be assembled. As a result, all tests need to be carried out **using the ALTIROC's calibration pulse circuitry**.
- ❖ **Qmin scans** done at the demonstrator show a **minimum detectable charge of ~4.5-5 fC** (the chip above shows ~4.75 fC as an example)
- ❖ Delay scans show a **mean TOA LSB close to 20 ps**, with an RMS spread of 5 ps. This value can be modified and the spread reduced by optimising slow control parameters.



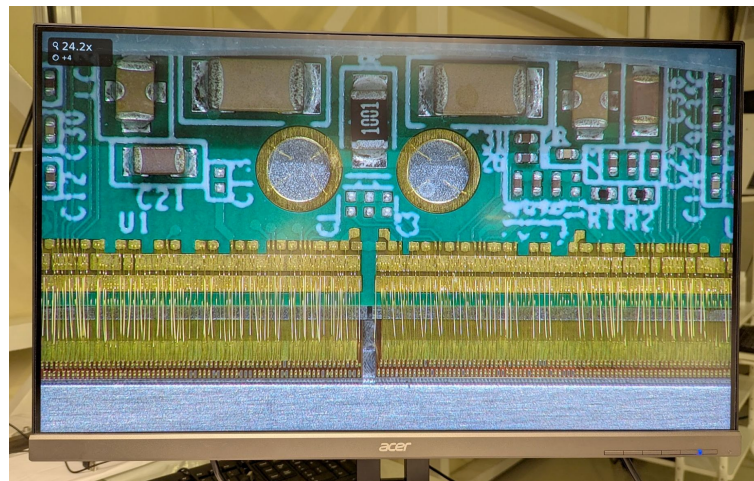
Demonstrator → Module Zero



- ❖ Lots of learnings so far with the **current demonstrator** (v1; PEB 1F with up to 55 modules)
- ❖ Up next: **demonstrator v2** (PEB 3F with 39 modules), with near-final **cooling plate** design, and 'outer ring' included
- ❖ Then: **Module Zero**
 - One **quarter** of one side of one disk ('back side')
 - 5 different PEBs
 - **251 HGTD modules**

Summary and conclusions

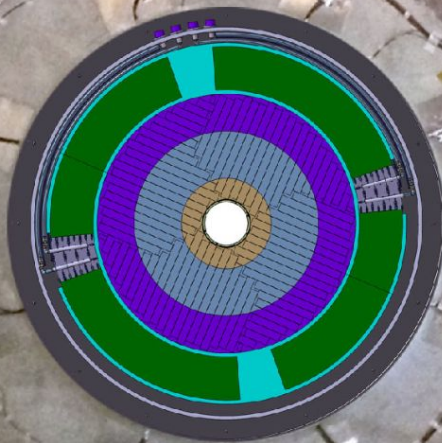
- ❖ The LGAD sensors meet the HGTD requirements for **charge**, **timing** and **efficiency**, including **after irradiation** to $2.5 \times 10^{15} \text{ neq/cm}^2$
- ❖ The ALTIROC-A ASIC provides the required **fast**, **low-noise readout**, with **acceptable jitter** and **radiation tolerance**
- ❖ Sensor-ASIC assemblies demonstrate **good pixel connectivity**, **high hit efficiency** and time resolutions of **below 50 ps** for hybrids and **around 55 ps** for full modules
- ❖ The **complete detector chain**, including modules, PEB, services and DAQ, is being **successfully exercised** with good preliminary results and **$Q_{\min}$ values are close to 5 fC**
- ❖ The sensor, ASIC and electronics are in a **mature state** with demonstrated **performance according to specifications**
- ❖ **Next steps**: add final components to build **demonstrator v2**, then build up to a **quarter disk**, and eventually the full **High Granularity Timing Detector**!



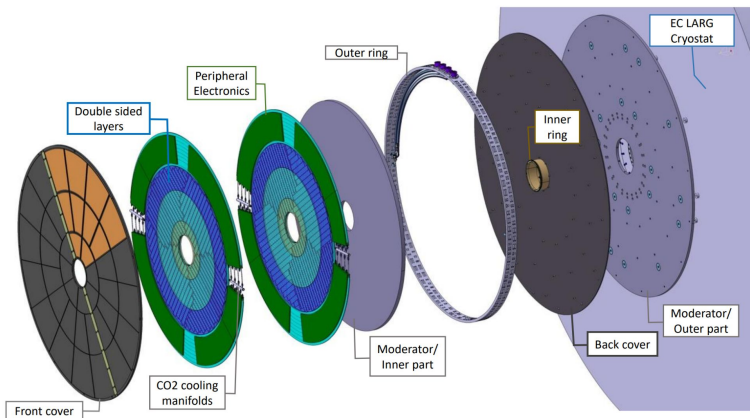
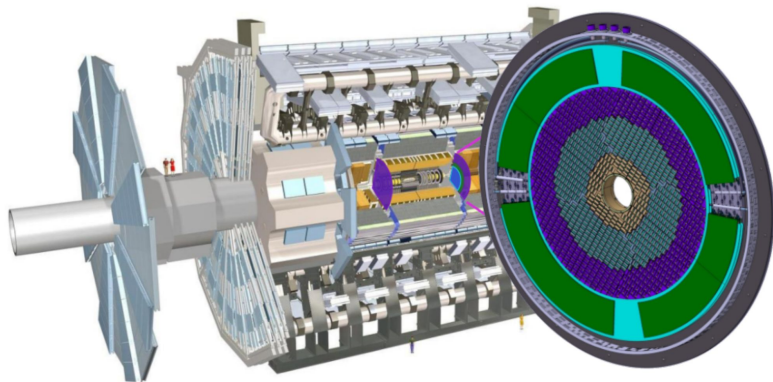
HGTD module as seen under a microscope

**Thank you
for your attention!**

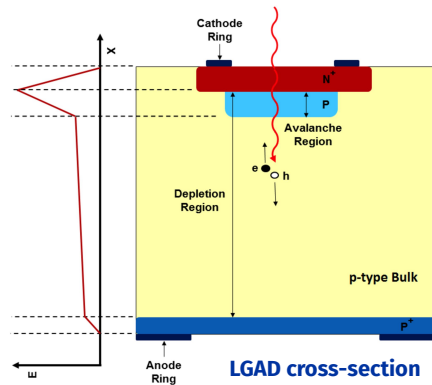
Backup



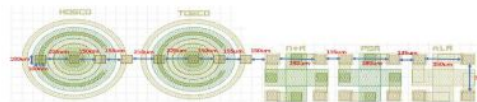
The ATLAS High Granularity Timing Detector



- ❖ The **HGTD** is a Phase-II upgrade for ATLAS experiment, designed to
 - Provide **precision timing** in the forward region (**50-70 ps/hit**, **30-50 ps/track**), helping **mitigate pileup** by adding timing information to vertex association
 - Provide a **luminosity measurement** by counting the number of hits every bunch crossing
- ❖ Located between the barrel and endcap calorimeters, with
 - **2 double-sided discs** on each endcap, inside a hermetic vessel
 - Active area coverage: $2.4 < |\eta| < 4$
 - Three rings which can be **replaced** independently as they suffer radiation damage and reach end-of-life

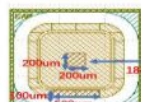


Quality Control-Test Structures (QC-TS)

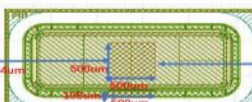


GCD

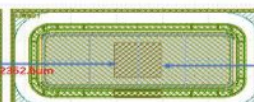
VDP



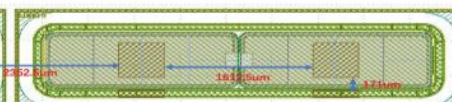
MOS



PIN



LGAD



1x2 LGAD

Gate-Control-Diodes (GCD):
measure surface currents (not
used after initial
measurements showed that
the GCD design does not
allow for meaningful
extraction of surface currents)

Van-der-Pauw (VDP)
structures: Measure
resistance of the substrates
(n+, p-stop) and aluminum

MOS capacitor:

- CV: Flat-band voltage and oxide thickness

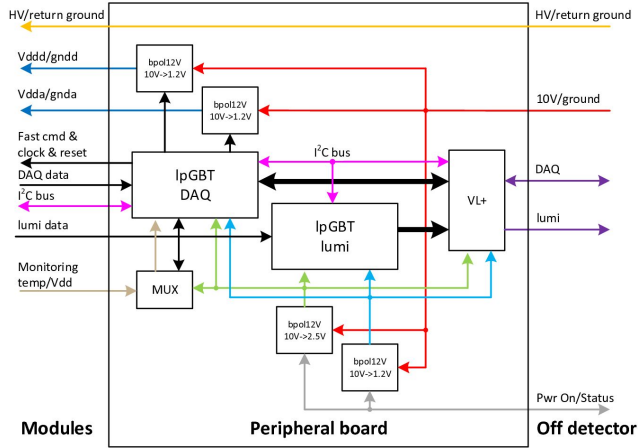
PIN diode IV: Compare PIN
IV with LGAD IV and
deduce the gain

LGAD (same area as main sensor pad, but elongated):

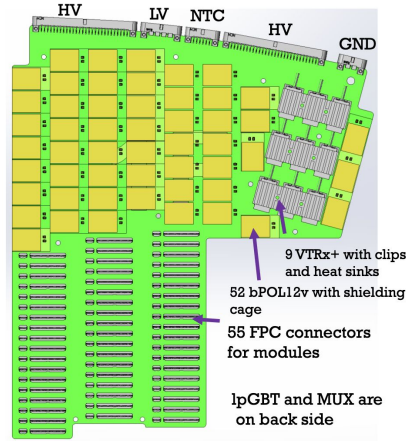
- IV: Break-down voltage and current at operation voltage
- CV: Gain-layer depletion voltage, full depletion voltage, detector capacitance

1x2 LGAD:
Measure inter-pad gap and other
inter-pad properties

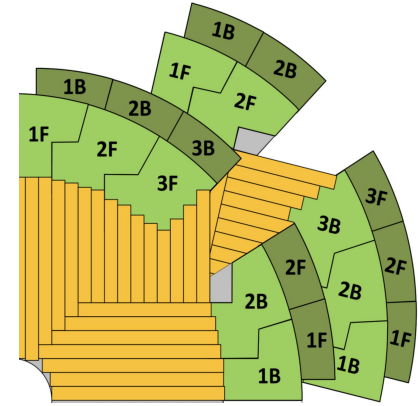
Peripheral Electronics Board



PEB architecture



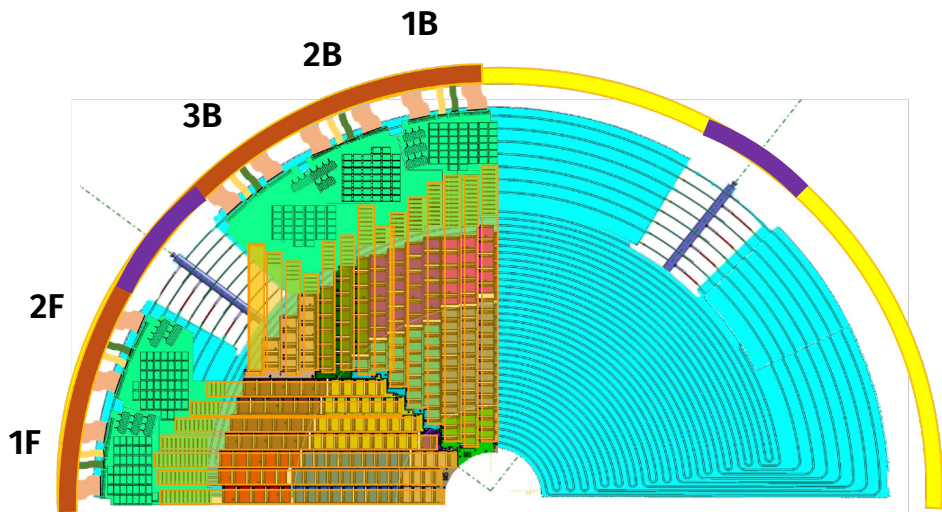
PEB1F layout



PEB quarter disk arrangement

- ❖ The **Peripheral Electronics Board (PEB)** provides the **interface** between the front-end modules and the off-detector systems
- ❖ IpGBT and VTRx+ provide the **optical links** for detector data, timing, trigger and control
- ❖ DC-DC converters supply the required **low voltages** to the front-end electronics; the **LGAD bias voltage** is distributed to each module via the flex tail

Module Zero



#HGTD modules on each PEB and HV modules needed:

1F: 55 $\rightarrow$ 4 HV modules ($55 = 14 \cdot 3 + 13$)

2F: 56 $\rightarrow$ 4 HV modules ($56 = 14 \cdot 4$)

3B: 39 $\rightarrow$ 3 HV modules ($39 = 14 \cdot 2 + 11$)

2B: 48 $\rightarrow$ 4 HV modules ($48 = 14 \cdot 3 + 6$)

1B: 53 $\rightarrow$ 4 HV modules ($53 = 14 \cdot 3 + 11$)

(Details in Backup)

- ❖ One quarter of one side of one disk ('back side')
 - 5 different PEBs
 - 251 HGTD modules
- ❖ LV:
 - 5 PEBs * 2 LV channels = Need **10 LV CH total**
 - $\Rightarrow$ **2 LV modules** (since 8 channels/module)
- ❖ HV:
 - 1 HV crate: 16 modules, 1 HV module: 14 channels
 - 251 HGTD modules $\rightarrow$ 18 modules minimally ($251 = 14 \cdot 17 + 13$)
 - Realistically: **19 modules** so that HGTD modules from different PEBs don't share HV modules
 - $\Rightarrow$ **2 HV crates**

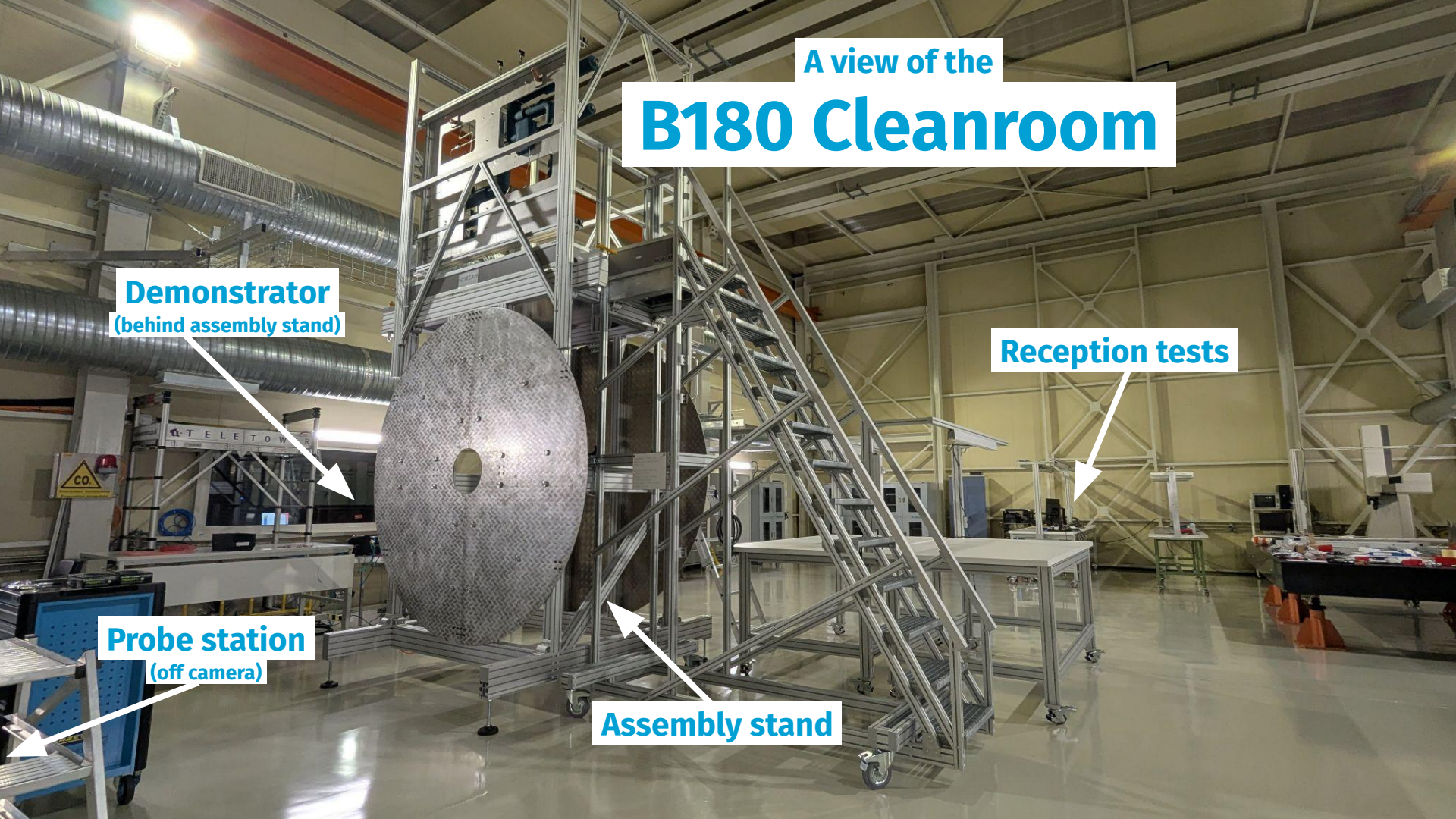
A view of the B180 Cleanroom

Demonstrator
(behind assembly stand)

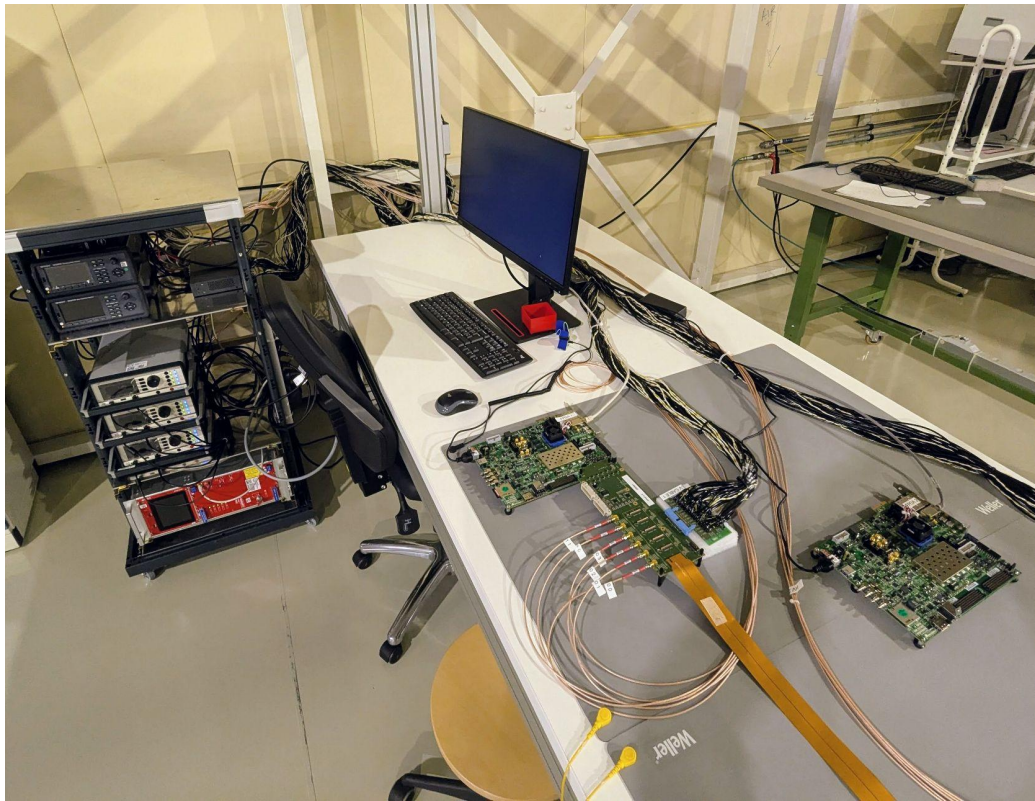
Reception tests

Probe station
(off camera)

Assembly stand



Reception testing

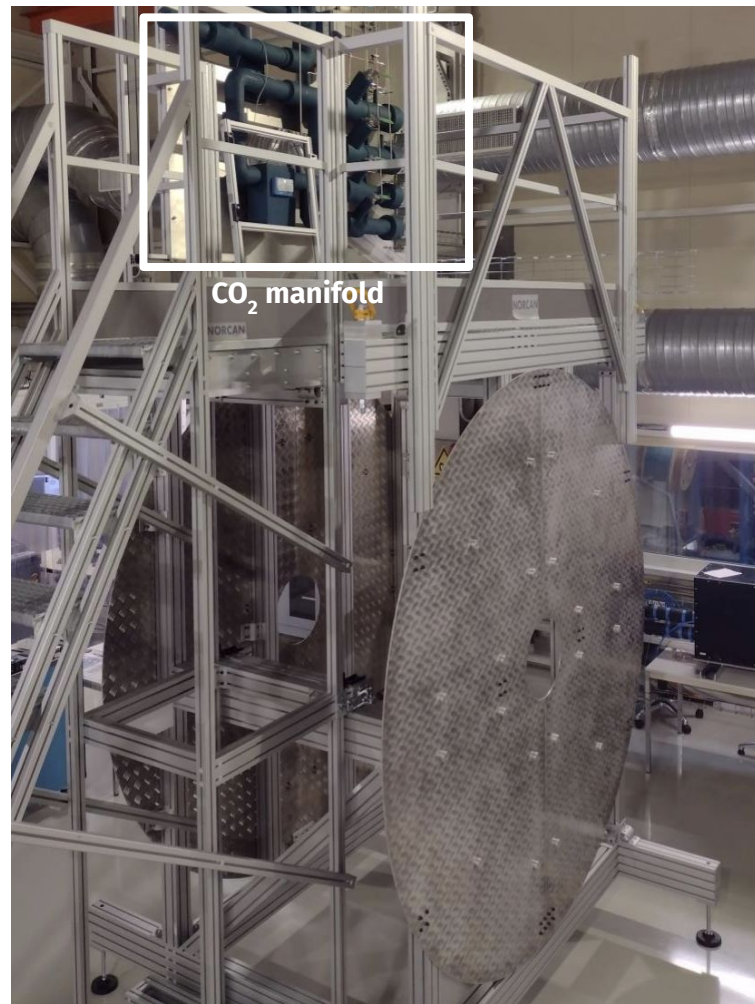


Reception test setup in B180 cleanroom

- ❖ Dedicated 'reception test' setup under development in B180 cleanroom
- ❖ Fully assembled DUs will arrive at CERN from the 6 module assembly sites; reception test setup will be used to make sure nothing was damaged in transport
- ❖ Two stations to simultaneously test up to 6 modules each
 - Perform a set of basic tests
 - Upload results to database and compare with results from previous tests
 - Clear DU for assembly

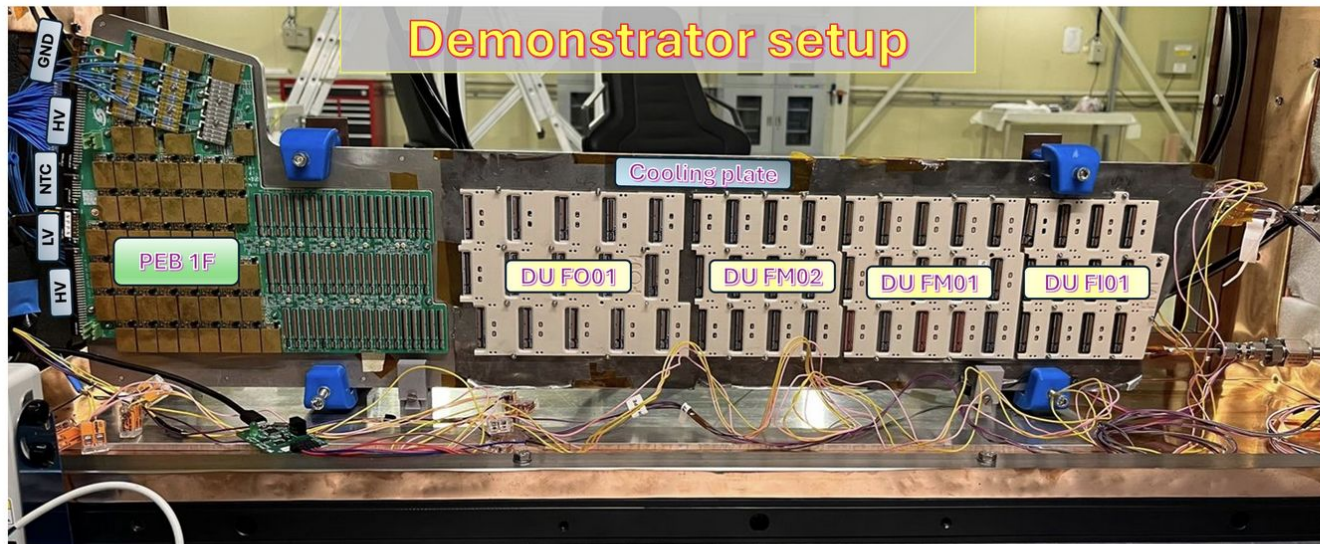
Building the HGTD

- ❖ **Assembly tooling components** have arrived at CERN
- ❖ **Front and back plates** have been machined, **cooling plate under development**
- ❖ HGTD will be assembled in **half-discs**
 - B180 cleanroom setup will provide **services** (HV, LV, interlocks, readout) for **one half-disc at a time**
 - Allows for a **final set of tests** once the half-disc has been mounted; list of tests to be done at **warm** and **cold** is in preparation
- ❖ Each vessel will contain **8 half-discs** (to form 2 double-sided discs), with **outer ring connectors along the boundary** to deliver services to, and receive information from, the electronics inside the vessel
- ❖ Once the first vessel has been assembled and tested, it is ready to move to P1, and **work begins on the second vessel**

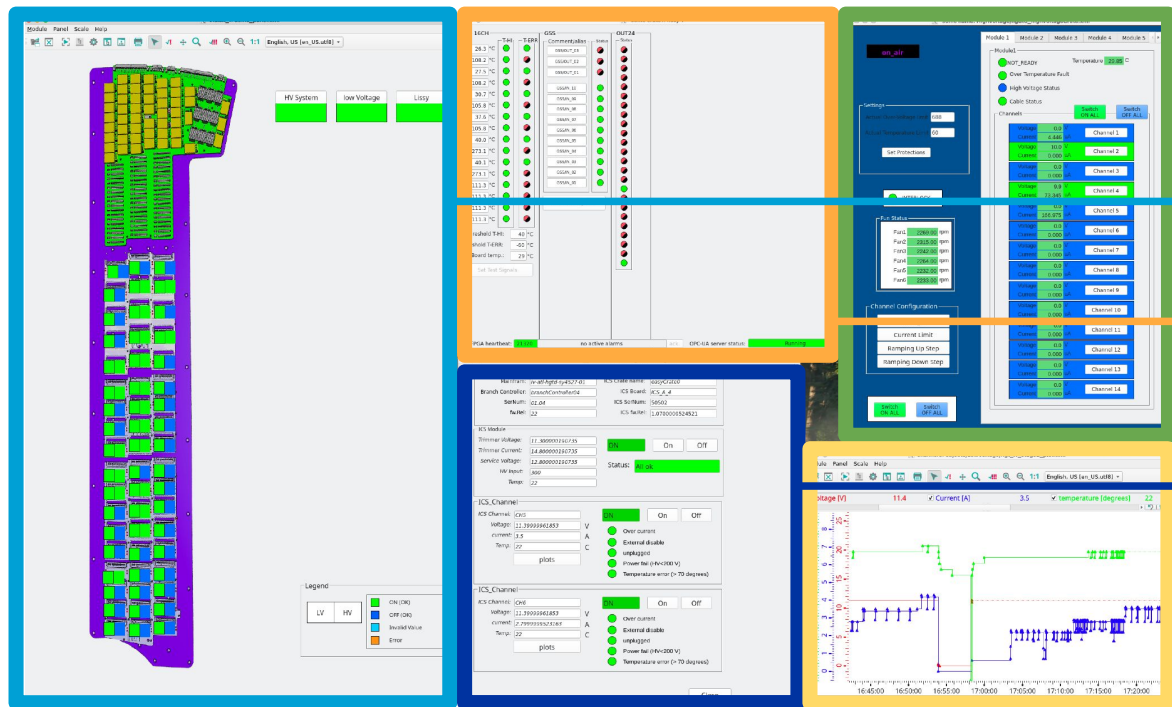


Assembly stand taking shape

Demonstrator DUs and rack



DCS at the Demonstrator



'Main' panel showing status of HV and LV for each module

LISSY panel showing status of the interlock system

HV panel

LV panel

LV plots showing V output of the PS, current in the circuit, temp of the PS