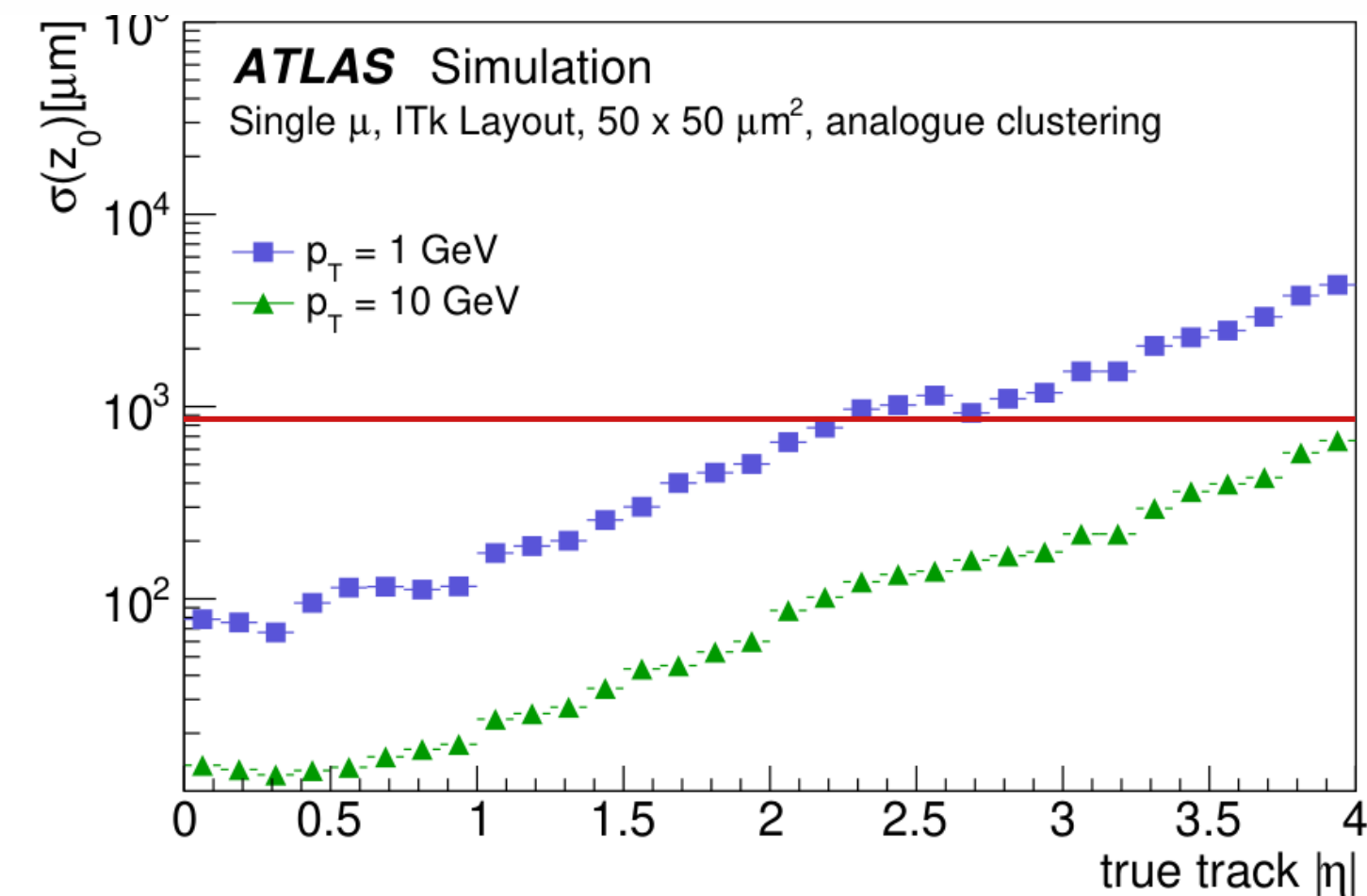
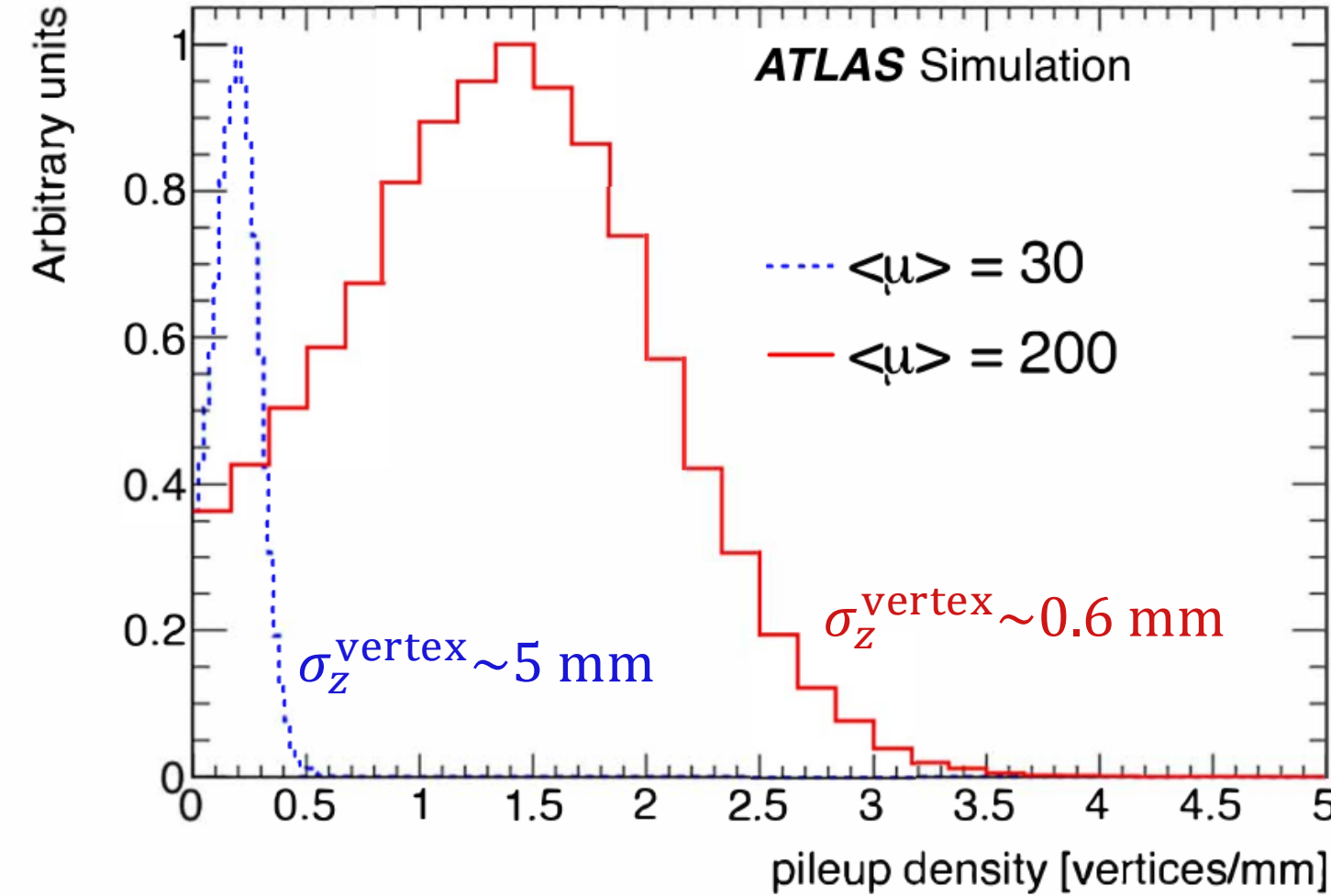
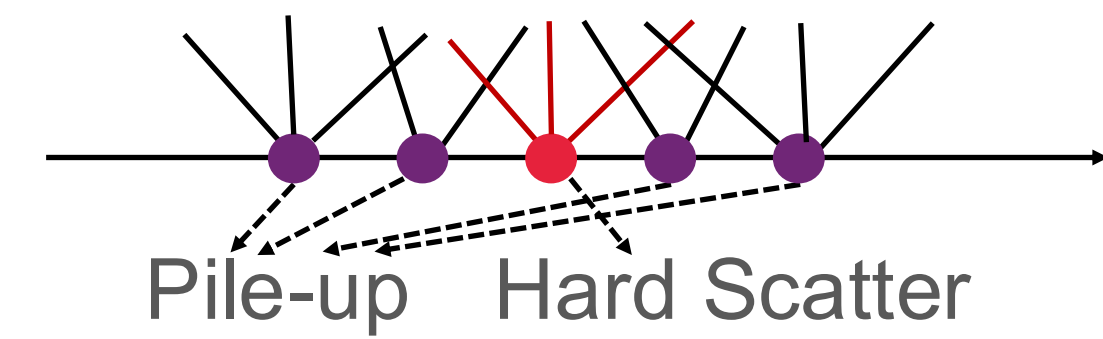


The ATLAS High-Granularity Timing Detector for the HL-LHC: project status and results

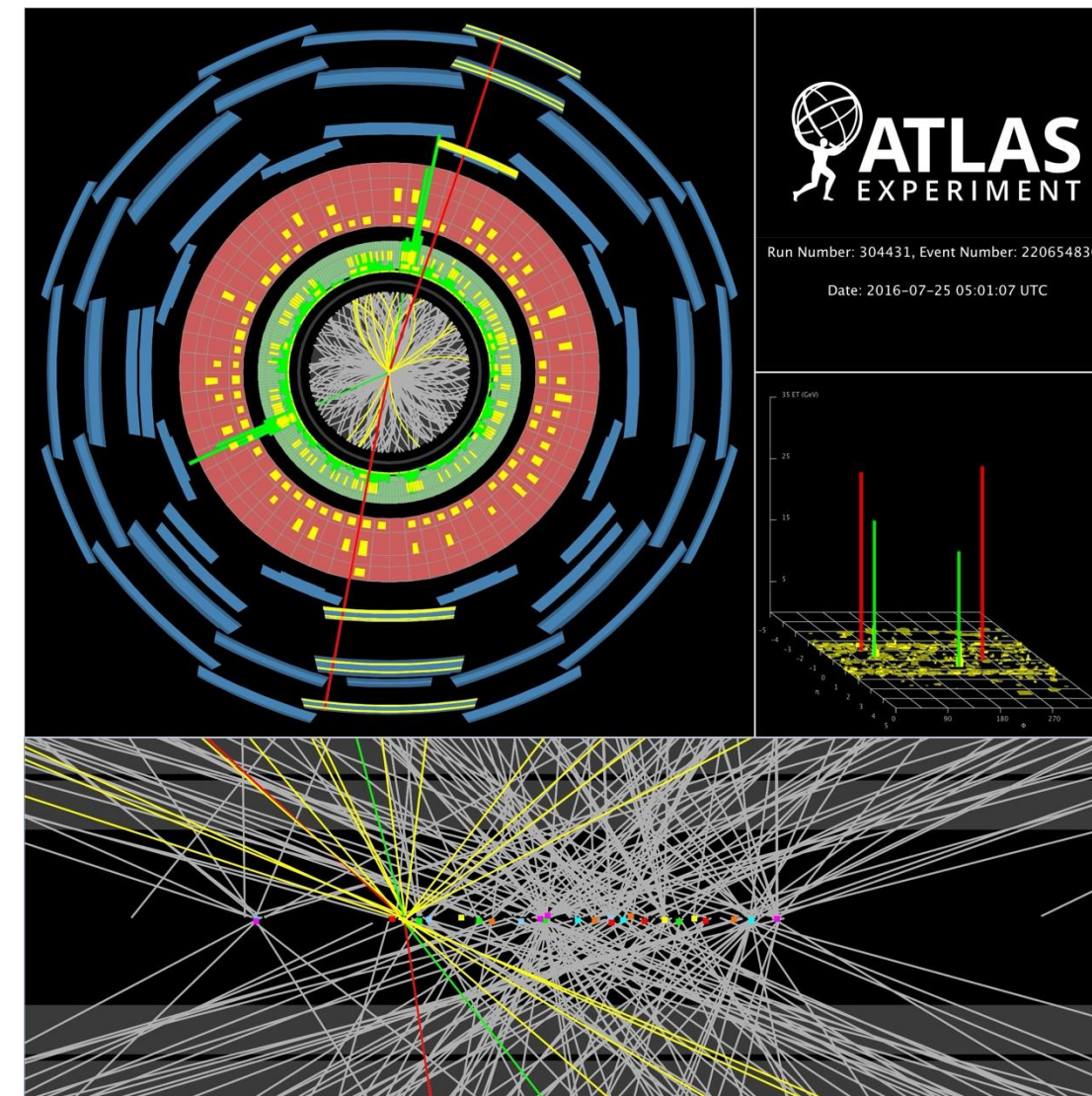
Tao Wang, Radboud University Nijmegen/Nikhef
on behalf of the ATLAS HGTD collaboration

The HL-LHC and the pile-up challenge

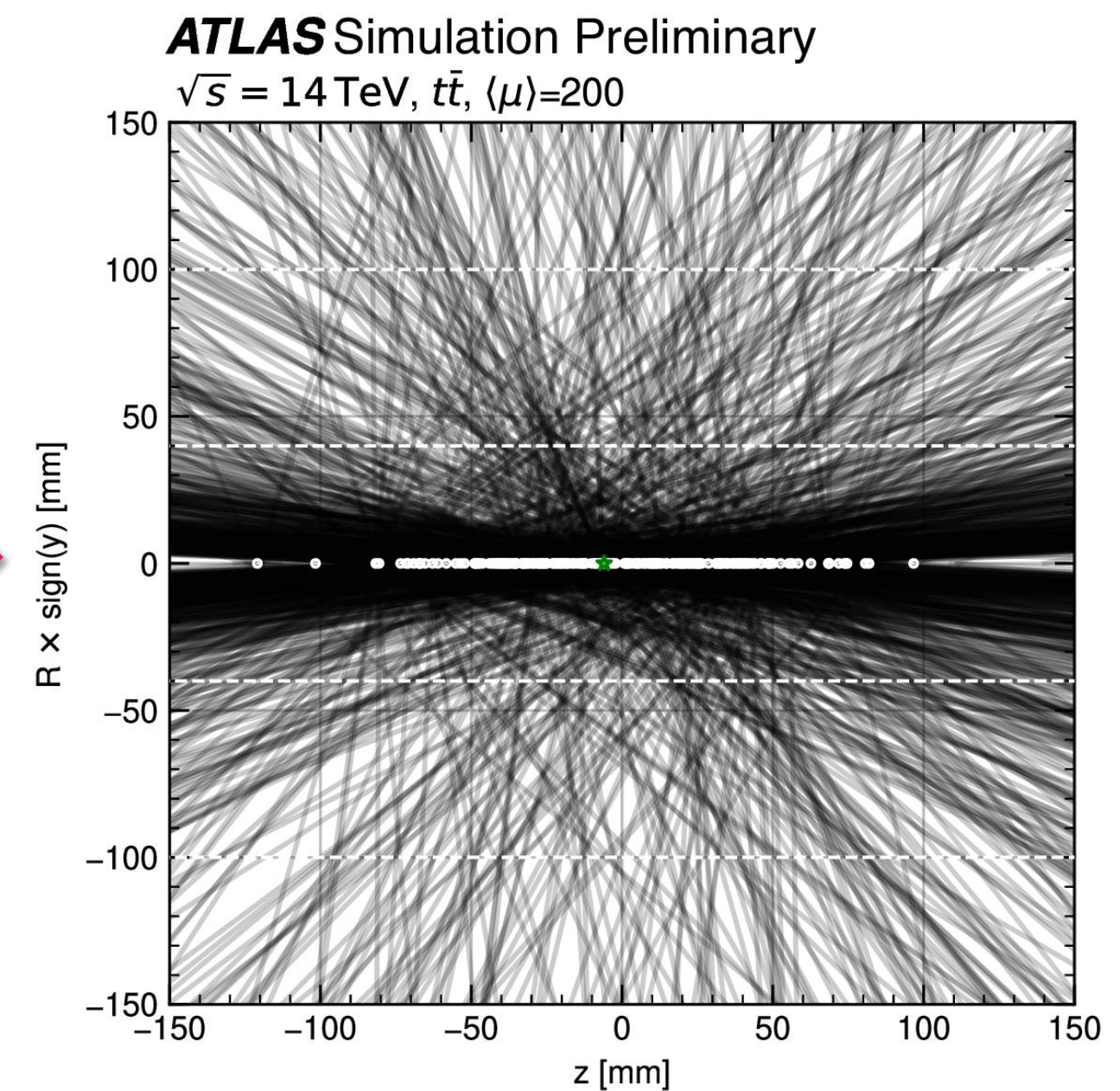


- Track z_0 resolution is vital to vertex separation
- [ATLAS-TDR-031](#), see also: M. Repik's [talk](#) from yesterday

- The HL-LHC will deliver instantaneous luminosity up to $7.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$, with up to 200 interactions per bunch crossing => **6 times more** than LHC run 2
- Collision vertex to pile-up separation will become extremely challenging, especially in the **forward region**

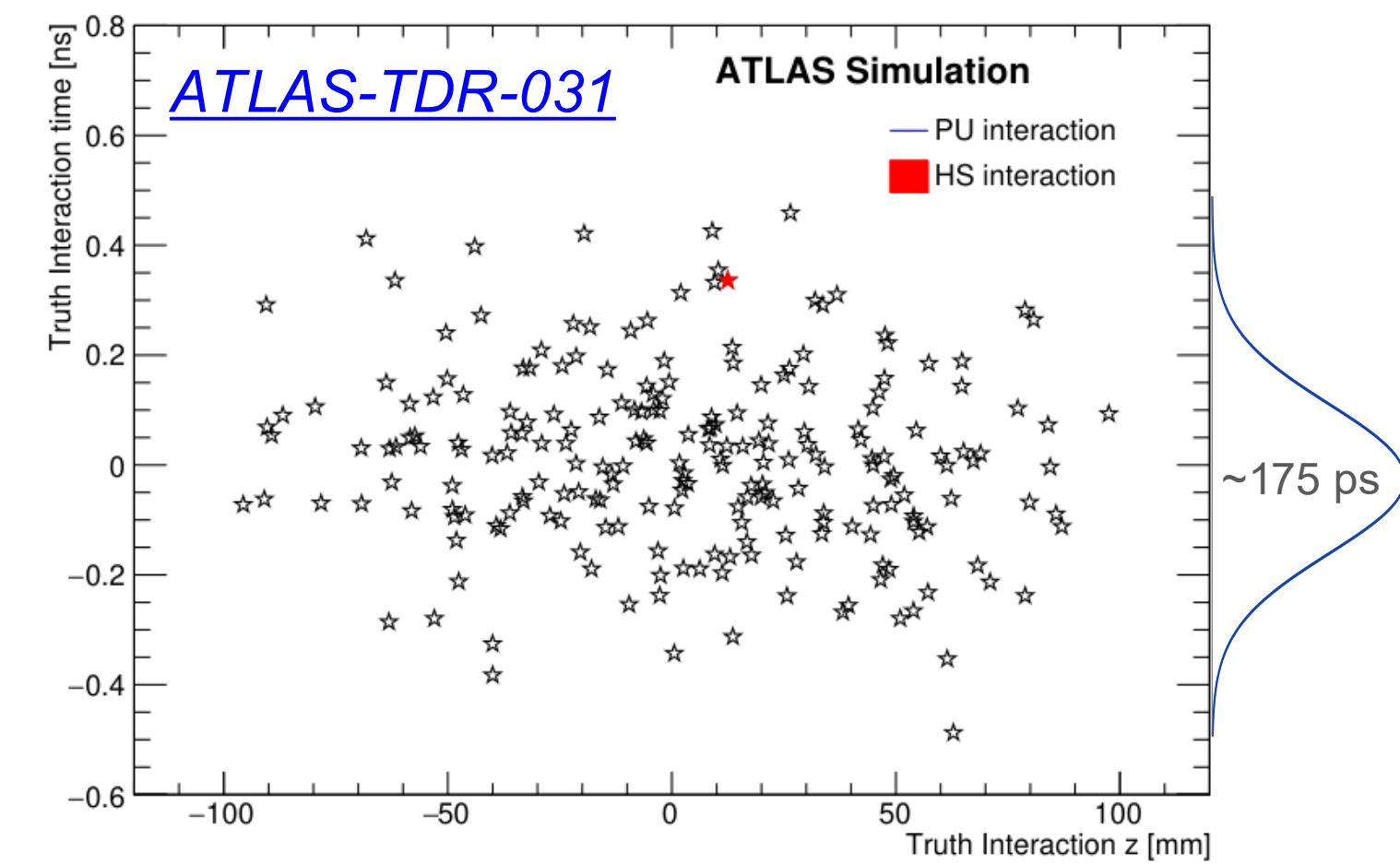


LHC Run 2, $H \rightarrow e e \mu \mu$, $\mu = 25$

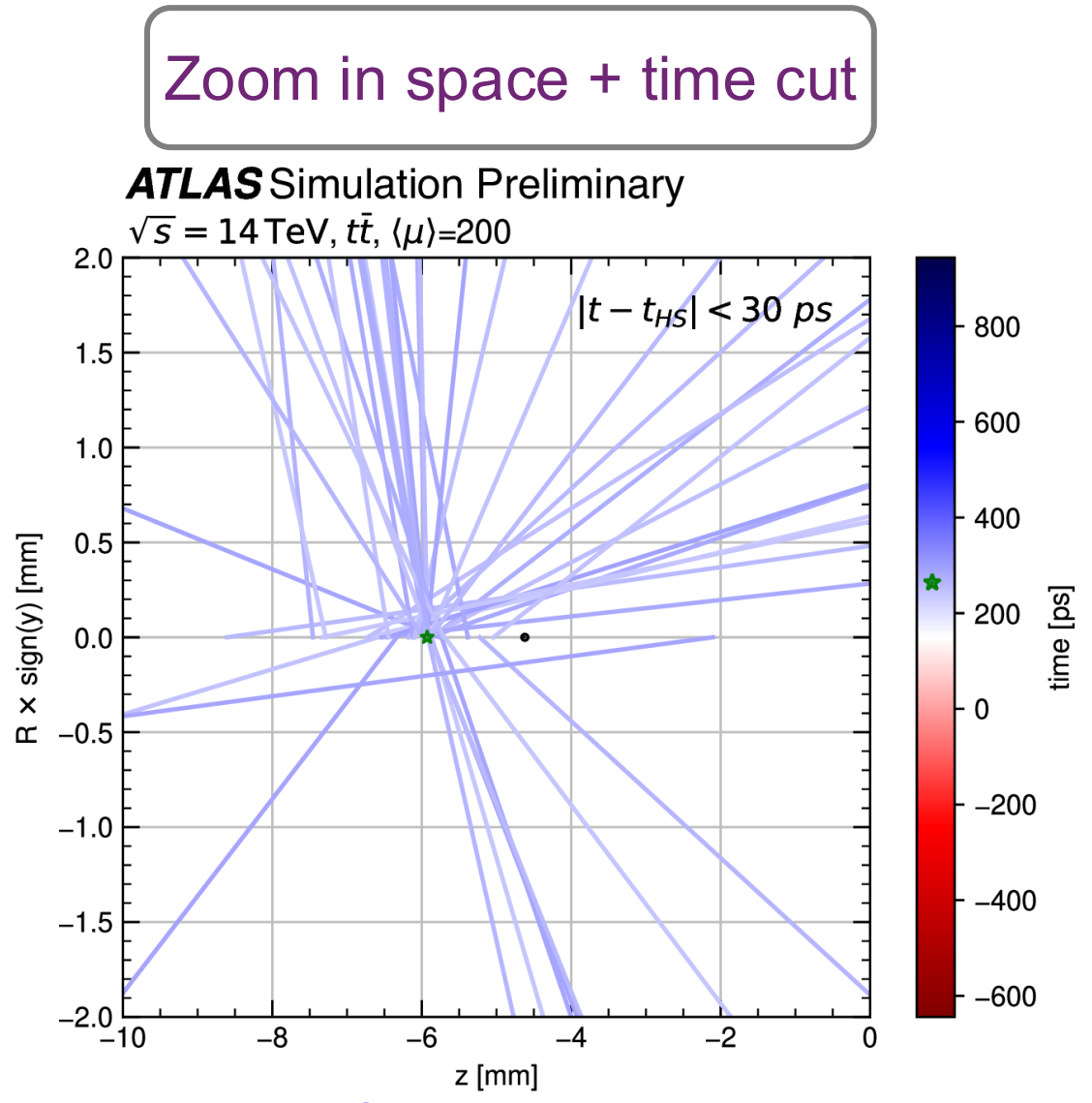
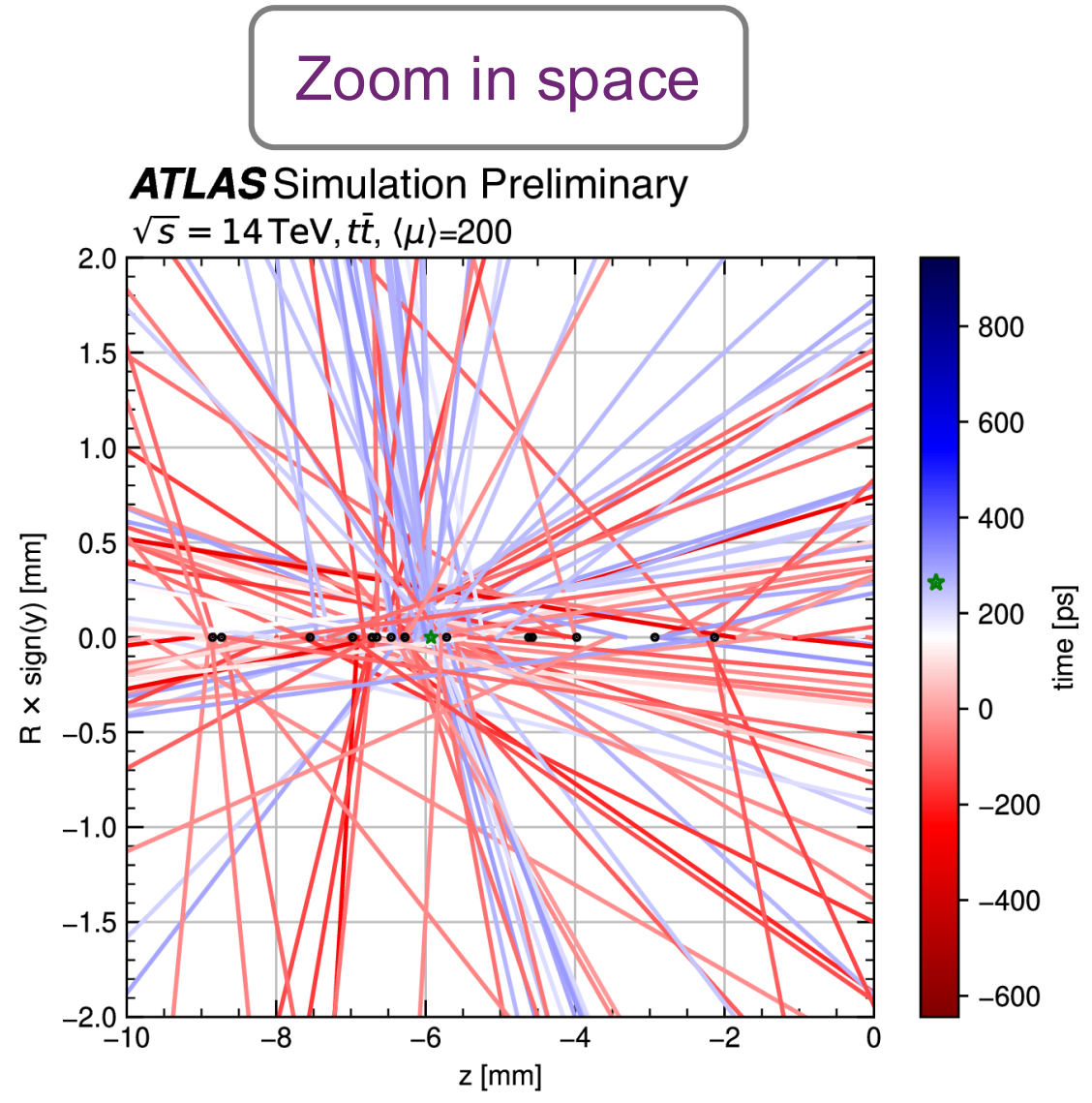
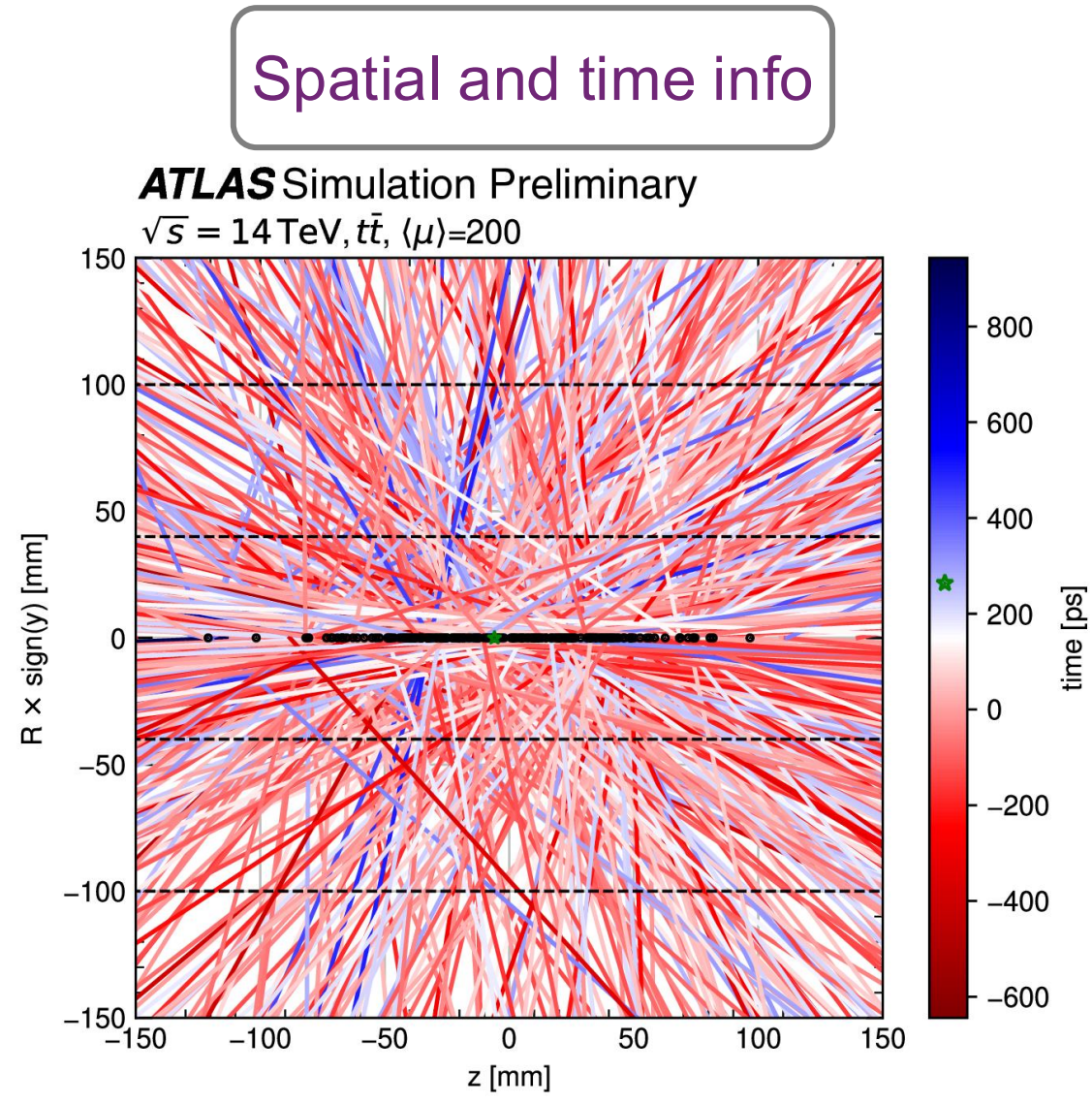
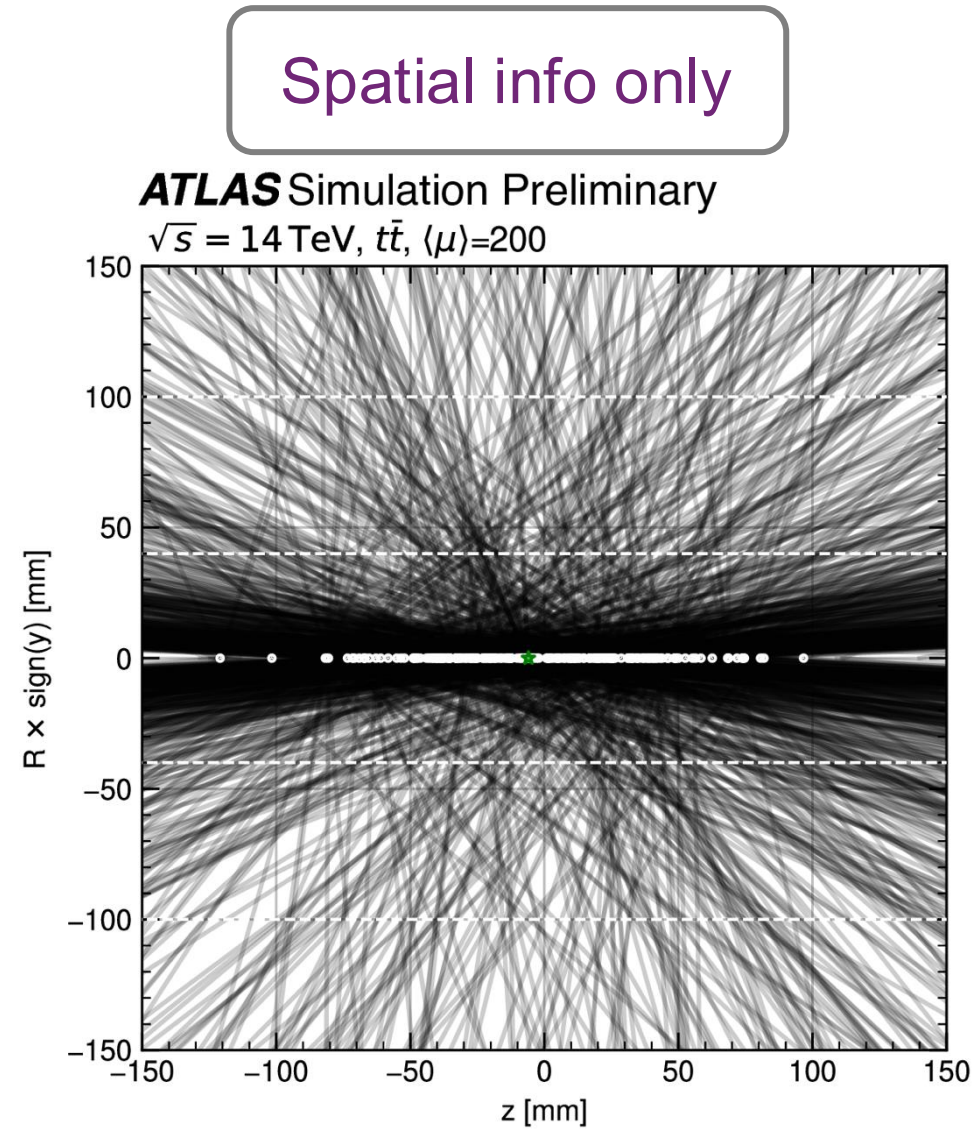


HL-LHC simulation, $t\bar{t}$, $\langle \mu \rangle = 200$

Adding timing to the ATLAS tracking

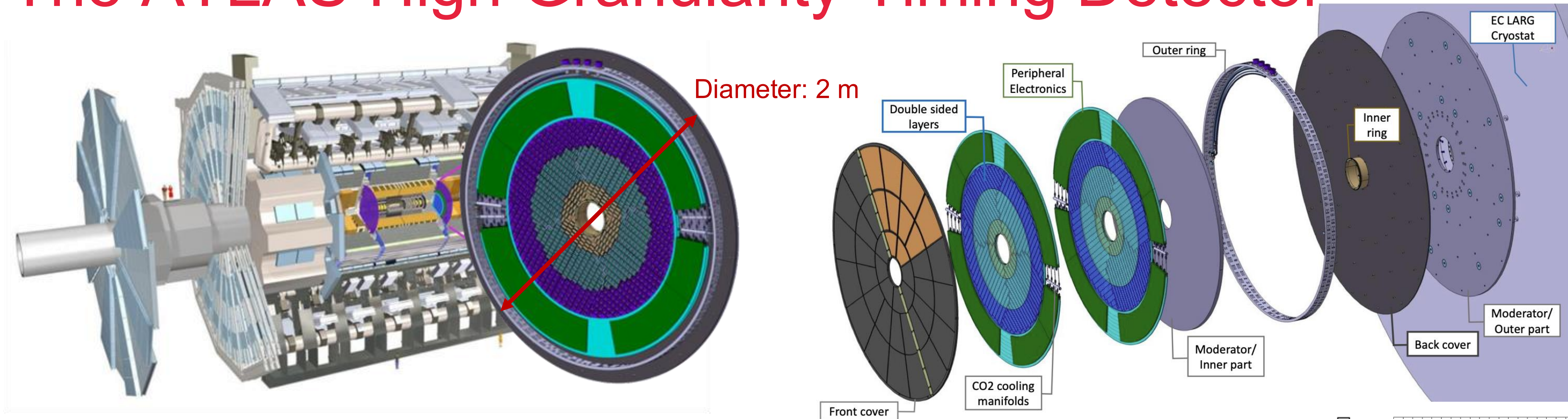


- Timing adds an additional dimension for collision-vertex and pile-up separation
- To sufficiently zoom in time, a vertex timing resolution of **O(10) ps** is required
- A timing layer at the forward region ($2.4 < |\eta| < 4.0$) with precise timing resolution could mitigate the pile-up challenge in this region
=> **The ATLAS High Granularity Timing Detector (HGTD) project**

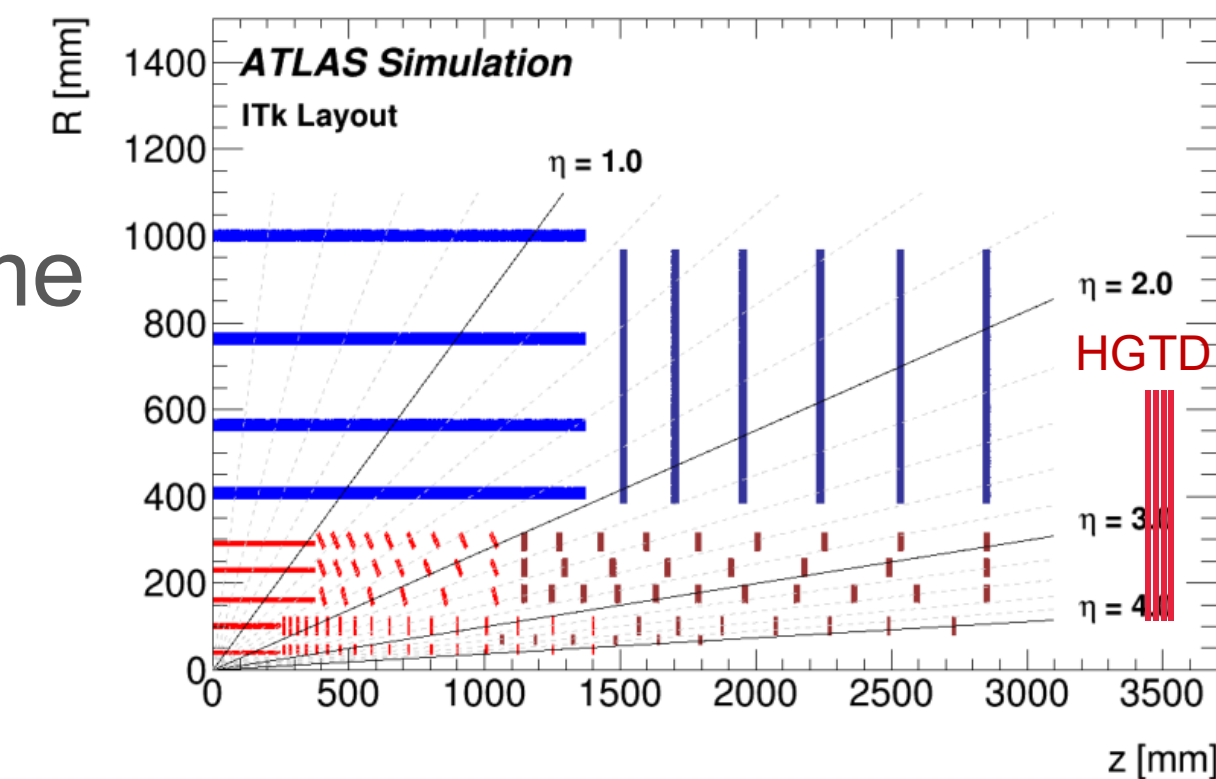


ATL-PHYS-PUB-2023-023

The ATLAS High Granularity Timing Detector

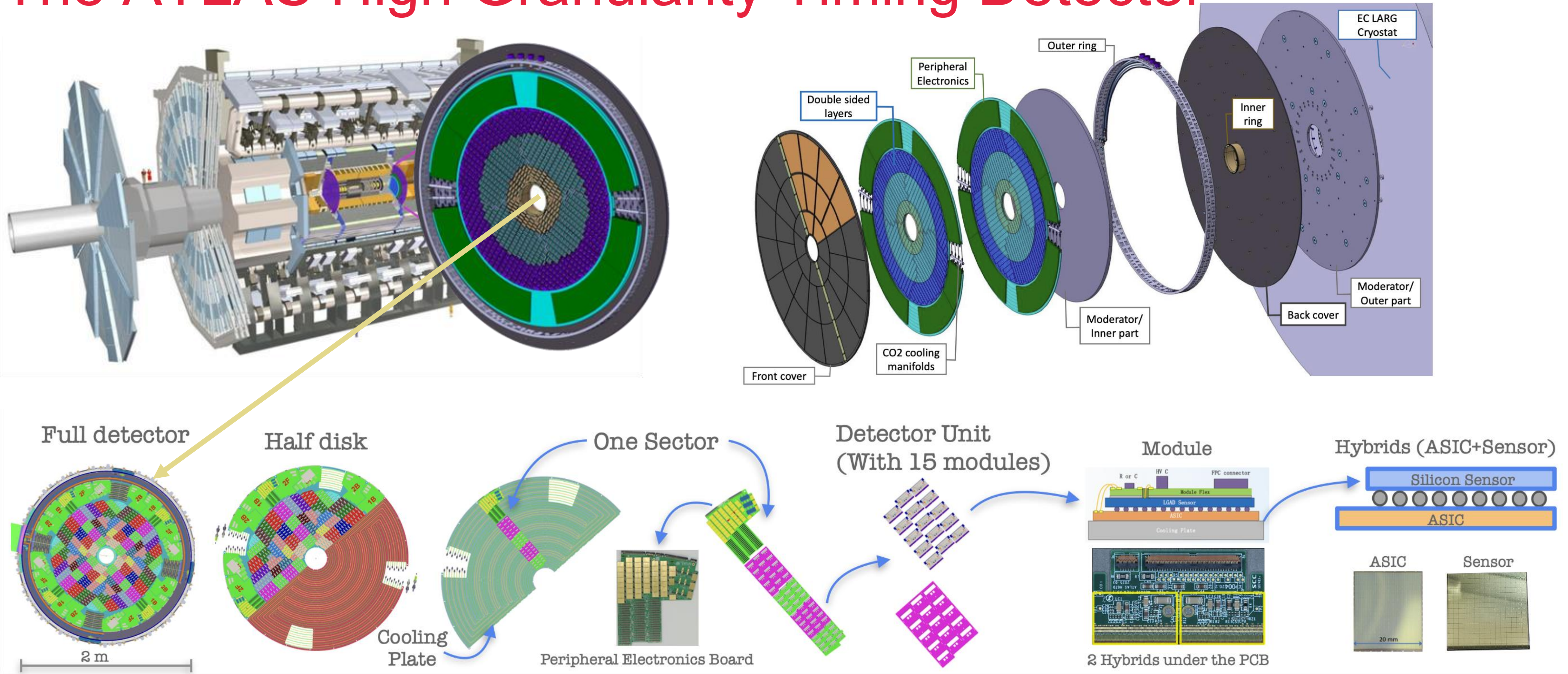


- 2 disks, each contains two layers, located at $z = \pm 3500$ mm, 12 cm thick in total
- Low Gain Avalanche Detector (LGAD) technology, deployed at this scale for the first time
- 8032 modules, and 3.6 million channels in total
- Operating temperature: -30 °C
- Per-track resolution: 30 ps–50 ps up to a fluence of 2.5×10^{15} neq/cm²
- Also allows for bunch-by-bunch luminosity measurements (ATLAS goal: <1% precision)



[ATLAS-TDR-031](#)

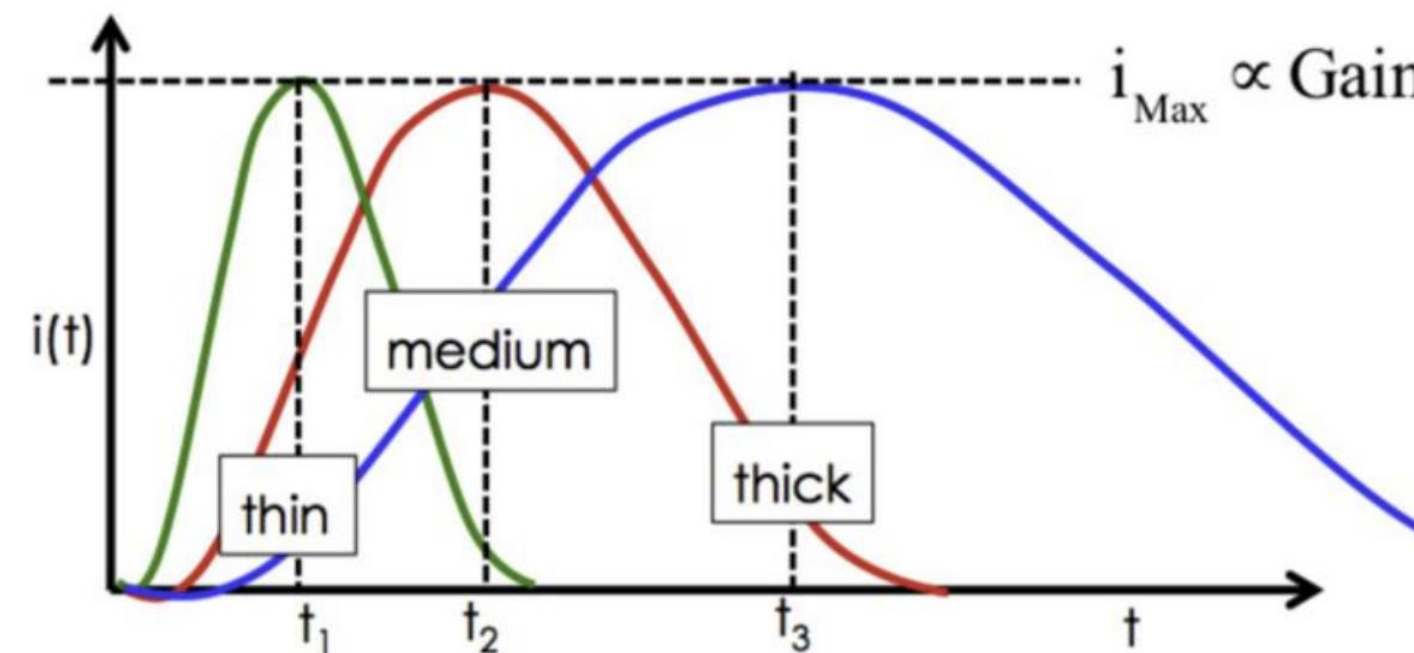
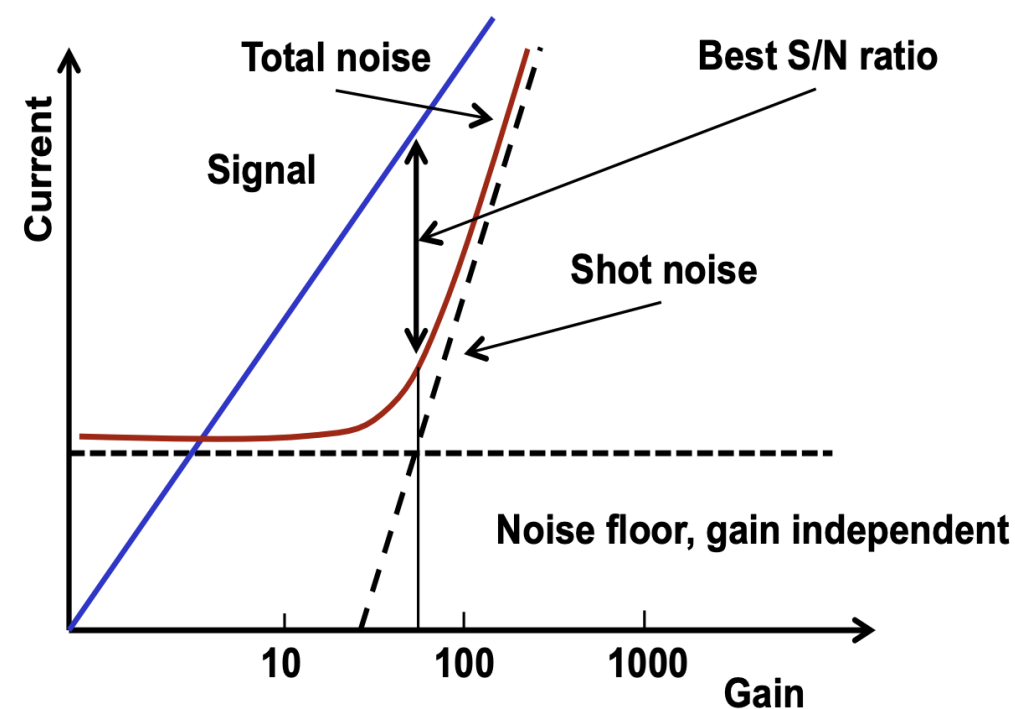
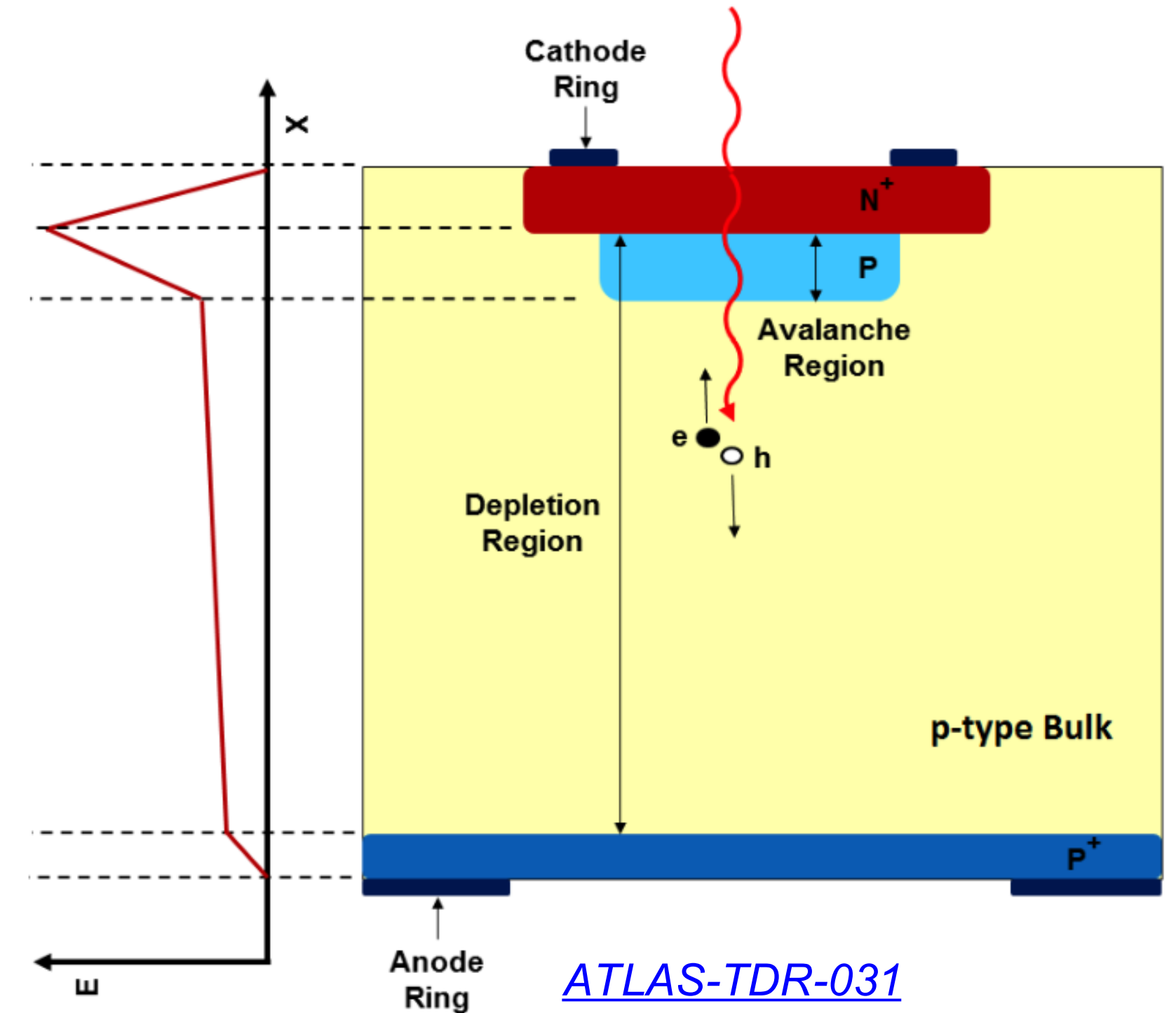
The ATLAS High Granularity Timing Detector



[HGTD breakdown](#) from M. Leite, ICHEP 2026

LGAD sensors: the technology

- Developed by CNM Barcelona ([link](#)) and CERN RD50 collaboration
- Standard segmented **N-in-P** silicon detector with built-in **p multiplication** layer
- The high electric field in the avalanche region can provide moderate gain (**10–20**) => **Good signal/noise ratio**
- Implementing the multiplication layer allows thinner detector
- **Fast** rising time (~ 400 ps) => **Low jitter**

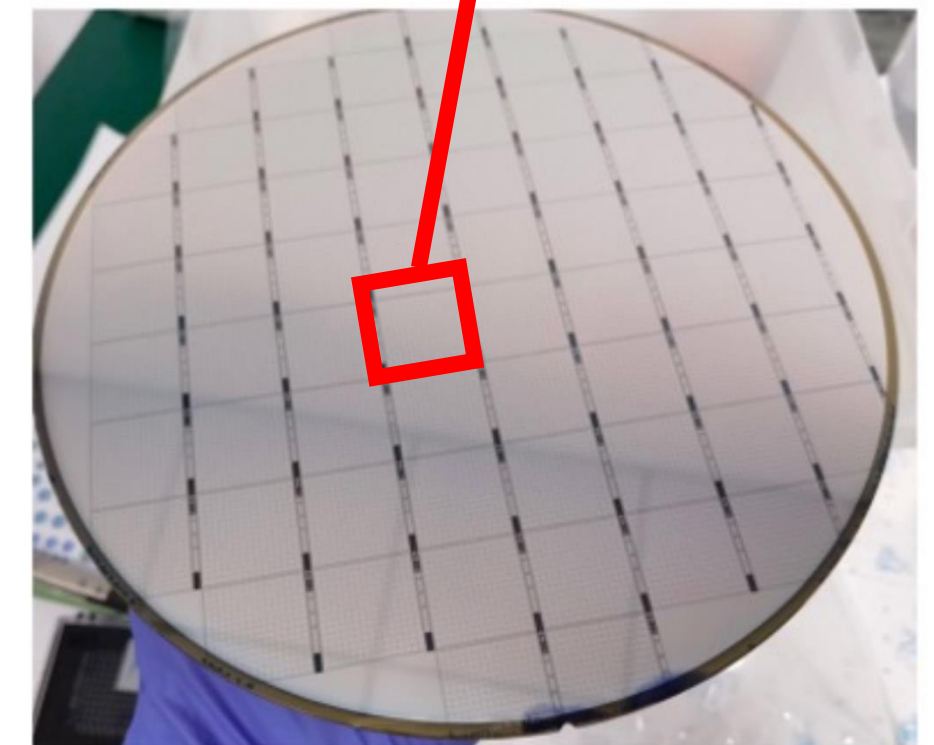
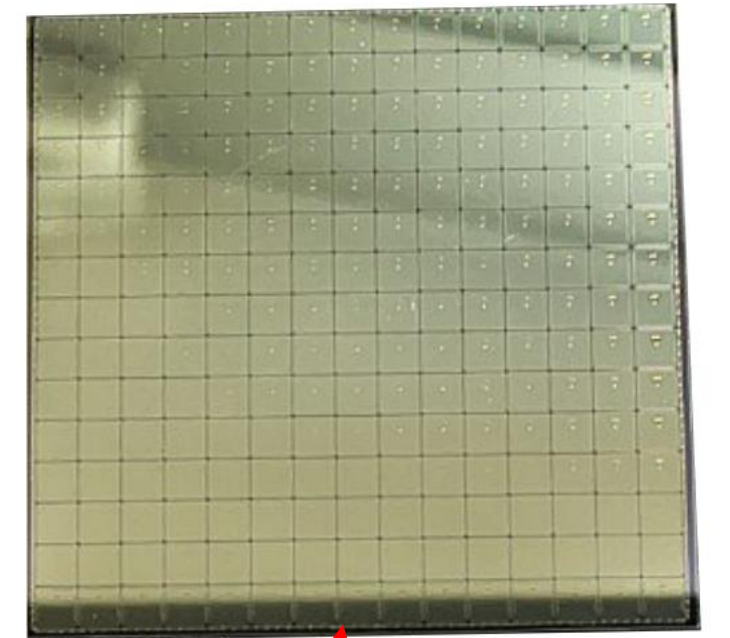


*Sadrozinski et al.,
arXiv:1704.08666 (2017)*

LGAD sensors in HGTD

- HGTD LGAD design
 - 15×15 pads, $1.3 \times 1.3 \text{ mm}^2$ pad size, thickness: **50 μm** (active)/**775 μm** (physical)
- Requirements (“end of lifetime” means after $2.5 \times 10^{15} \text{ neq/cm}^2$ irradiation):
 - Sensor time resolution: **< 40 ps** before irradiation, **< 50 ps** end of lifetime
 - Collected charge: **> 15 fC** before irradiation, **> 4 fC** end of lifetime
 - Hit efficiency: **> 97%** before irradiation, **$\geq 95\%$** end of lifetime
- **Irradiation problem:** acceptor removal reduces LGAD gain $\rightarrow$ higher bias voltage needed to compensate $\rightarrow$ increased risk of **Single Event Burnout (SEB)**
- **Solution:** Introducing a **carbon-enriched gain layer** to lower the operating voltage
- Roadmap: First prototypes (2020) $\rightarrow$ Carbon-enriched design (2021) $\rightarrow$ Design optimization (2022) $\rightarrow$ Pre-production (2023) $\rightarrow$ Production (since 2024)
- **~10000** LGAD sensor fabricated so far; tests and further production ongoing

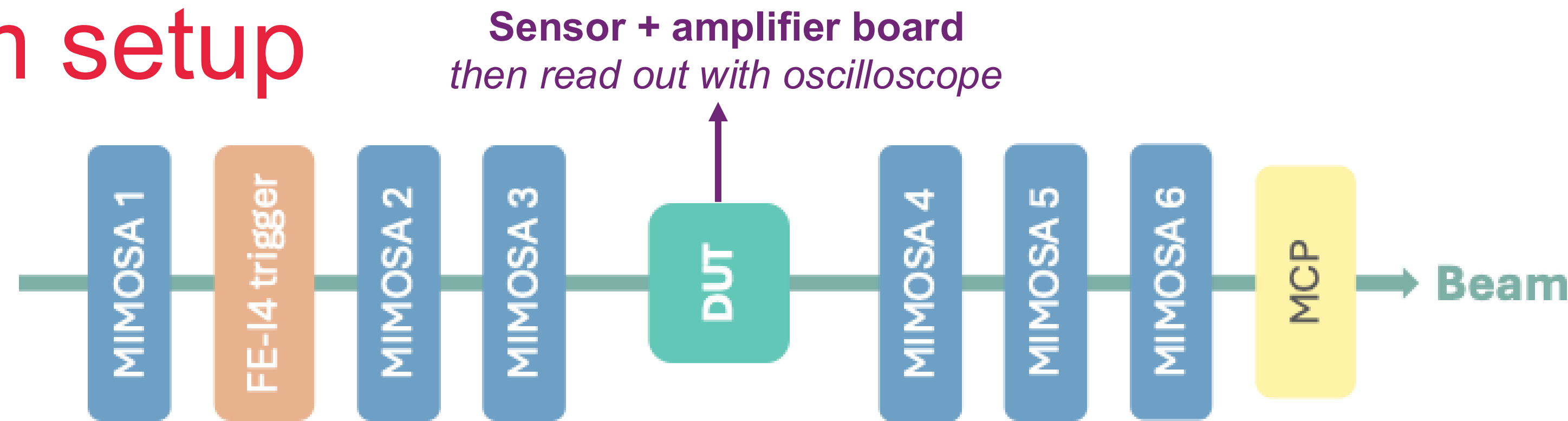
15×15 pad array



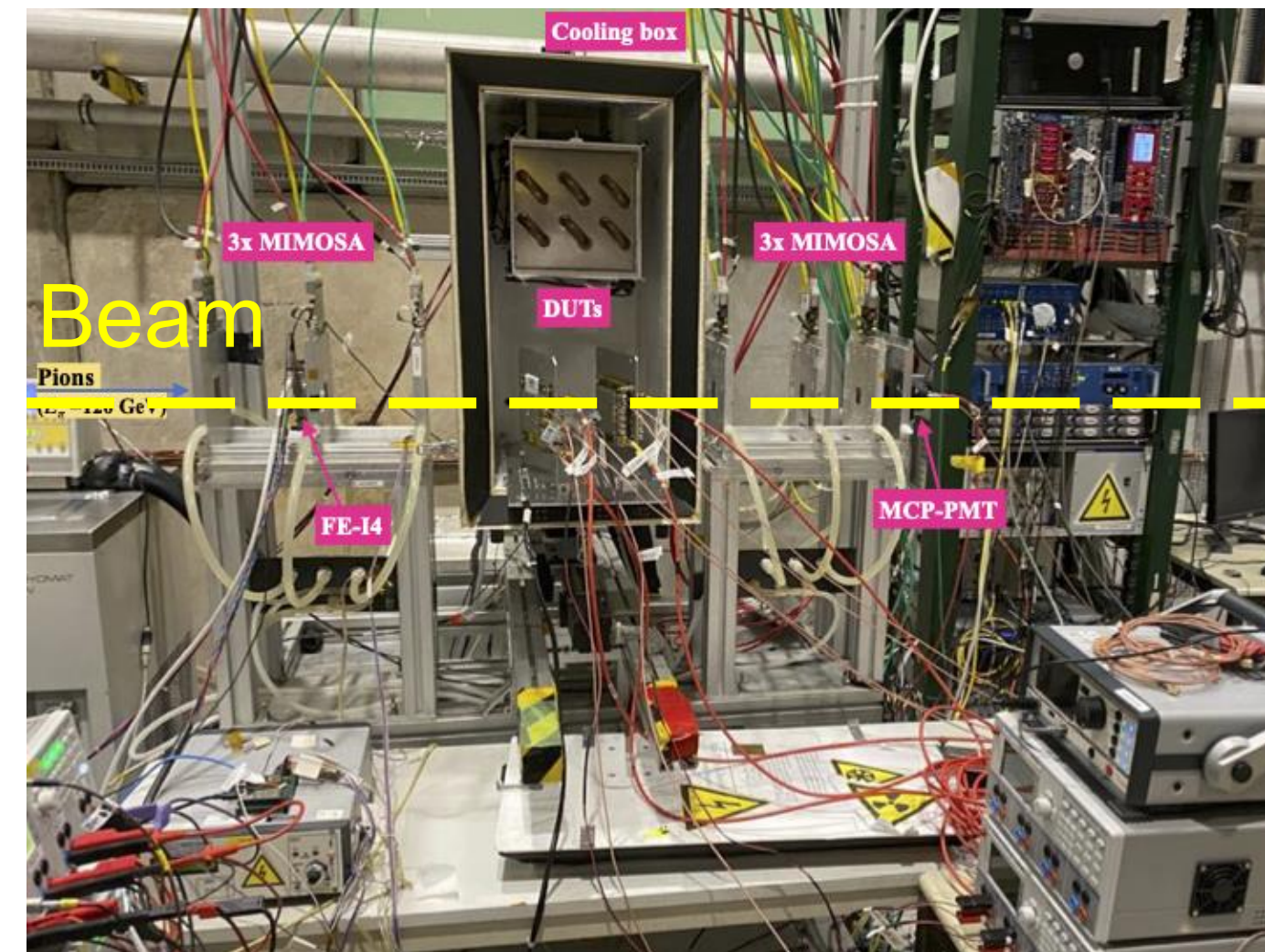
8" wafer with 52 LGADs and test structures

LGAD sensors: test beam setup

- Several test beam campaigns has been conducted at SPS and DESY
- Sensors are mounted in a telescope (**Mimosa** sensors) setup for recording the particle **hit position** and extract the **efficiency**
- An **FE-I4** that provides a fast, region-of-interest (ROI) selective HitOR trigger, with **25 ns** hit-timestamp granularity
- A fast (**<10 ps**) and **low jitter** timing reference (**microchannel plate, MCP**) is used to extract the **timing resolution**, read out using oscilloscope
- **AIDA-TLU** (Trigger Logic Unit) is used for trigger generation, synchronization and distribution



SPS (120 GeV π)



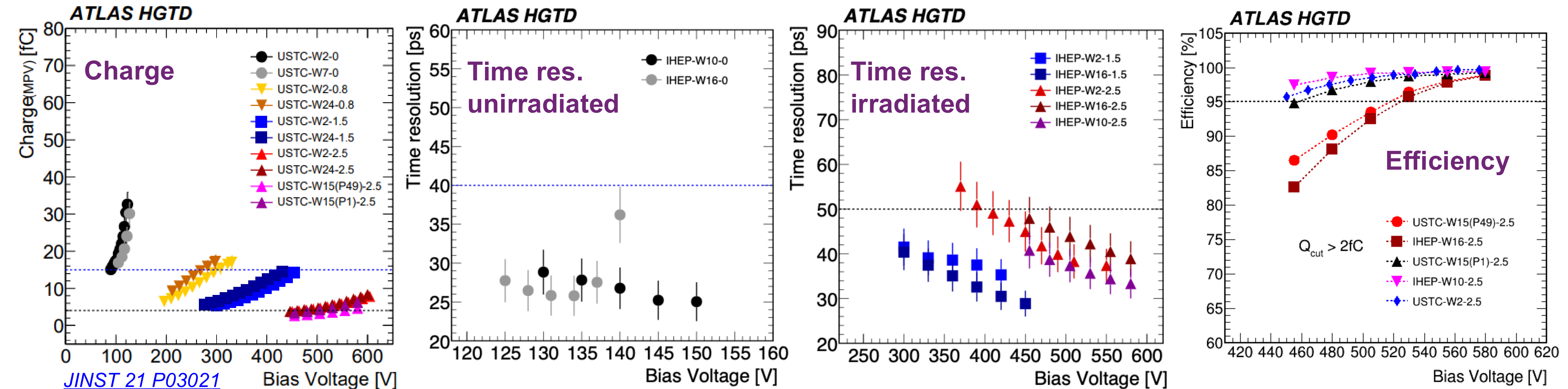
[HGTDTTestBeamPublicPlots](#)

DESY (5 GeV e^-)



LGAD sensors: test beam results

- **Charge collection, timing resolution, and efficiency** are measured for unirradiated and irradiated sensors
- **Unirradiated:** Satisfy the > 15 fC charge and < 40 ps time resolution requirements at low bias, $> 99\%$ efficiency
- **Irradiated:** Maintain > 4 fC collected charge and < 50 ps time resolution, $\geq 95\%$ efficiency up to 2.5×10^{15} neq/cm² and show **strong radiation tolerance**



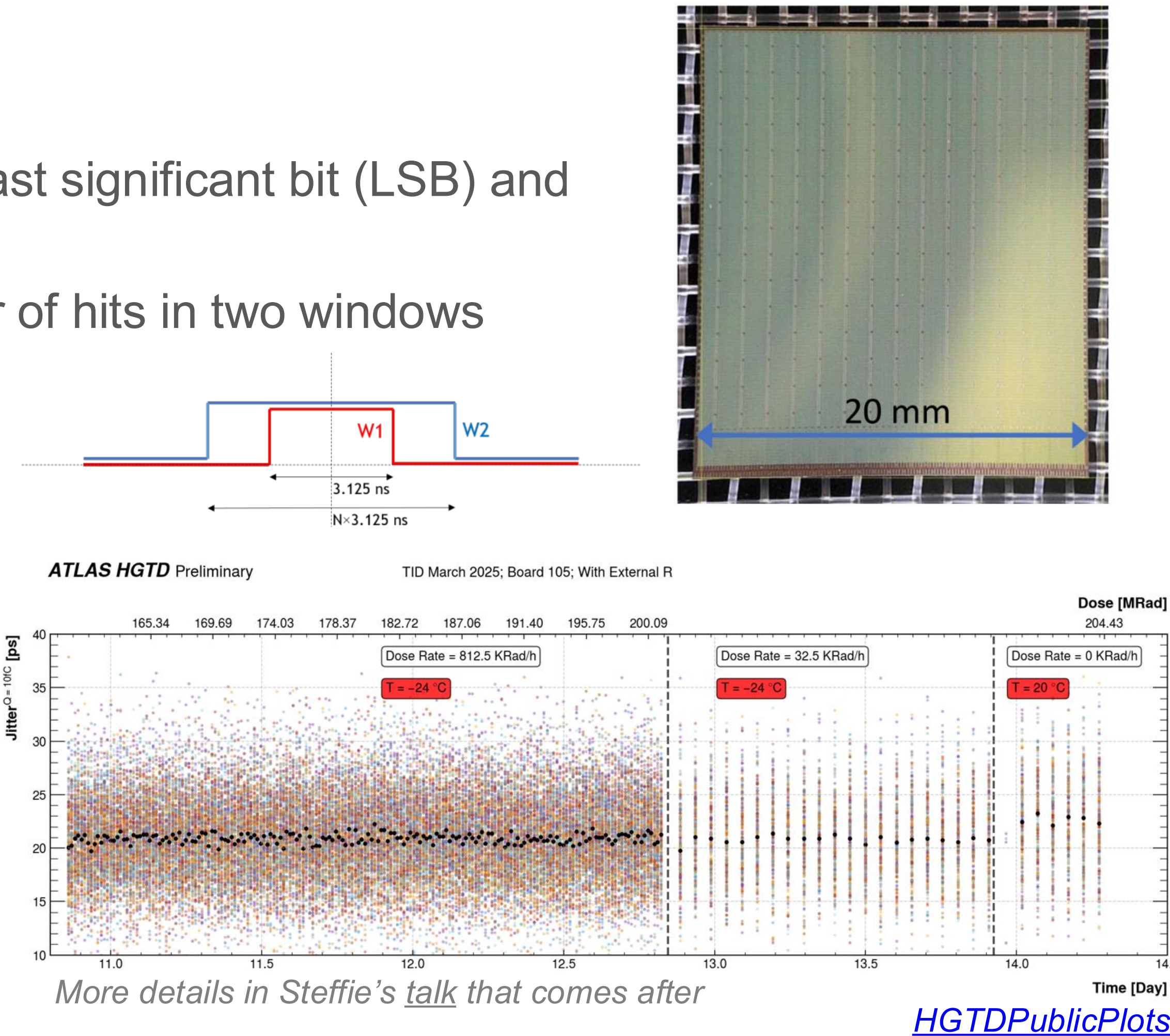
[JINST 21 P03021](#)

More details in Steffie's [talk](#) that comes after

ATLAS LGAD Timing Integrated Read-Out Chip (ALTIROC)

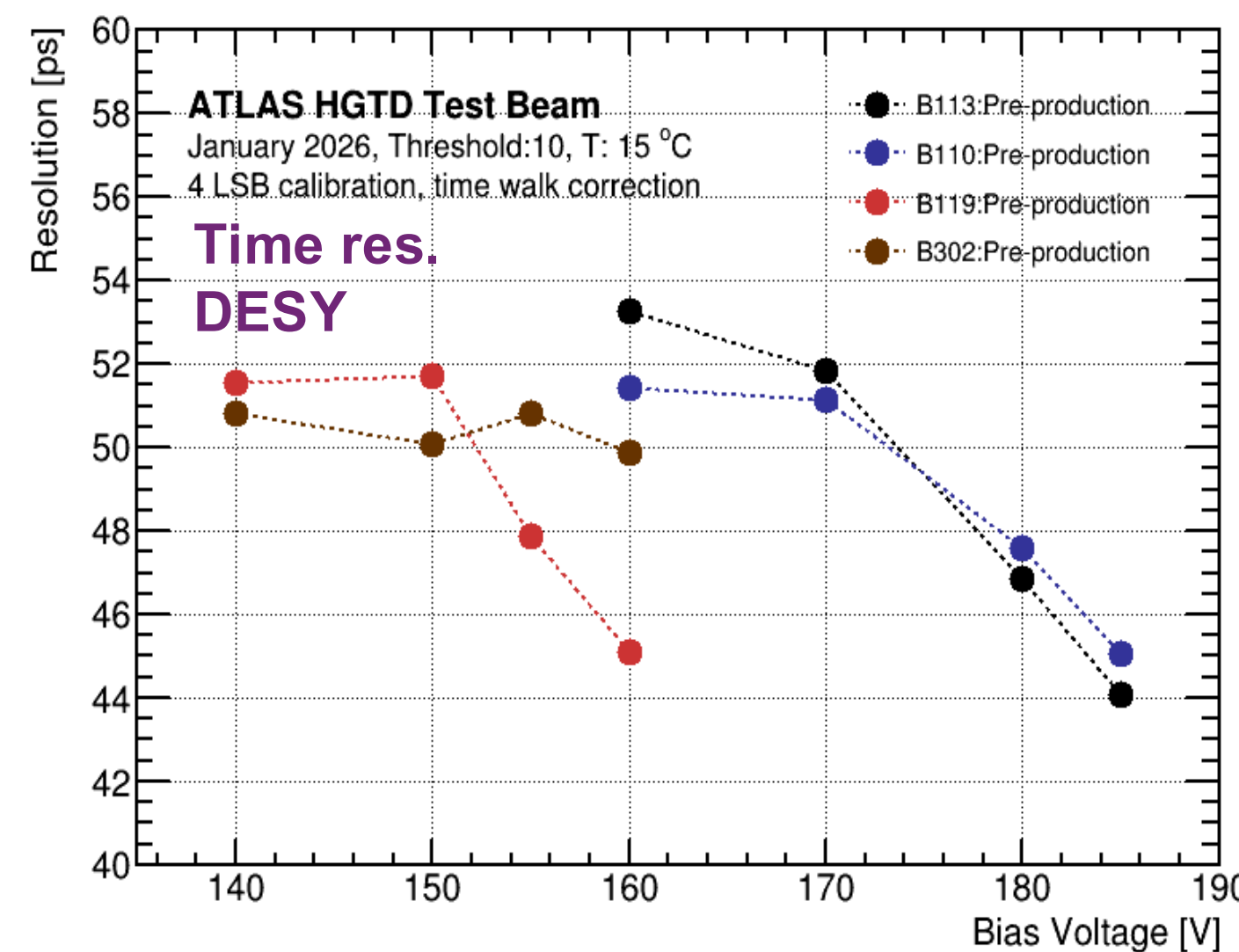
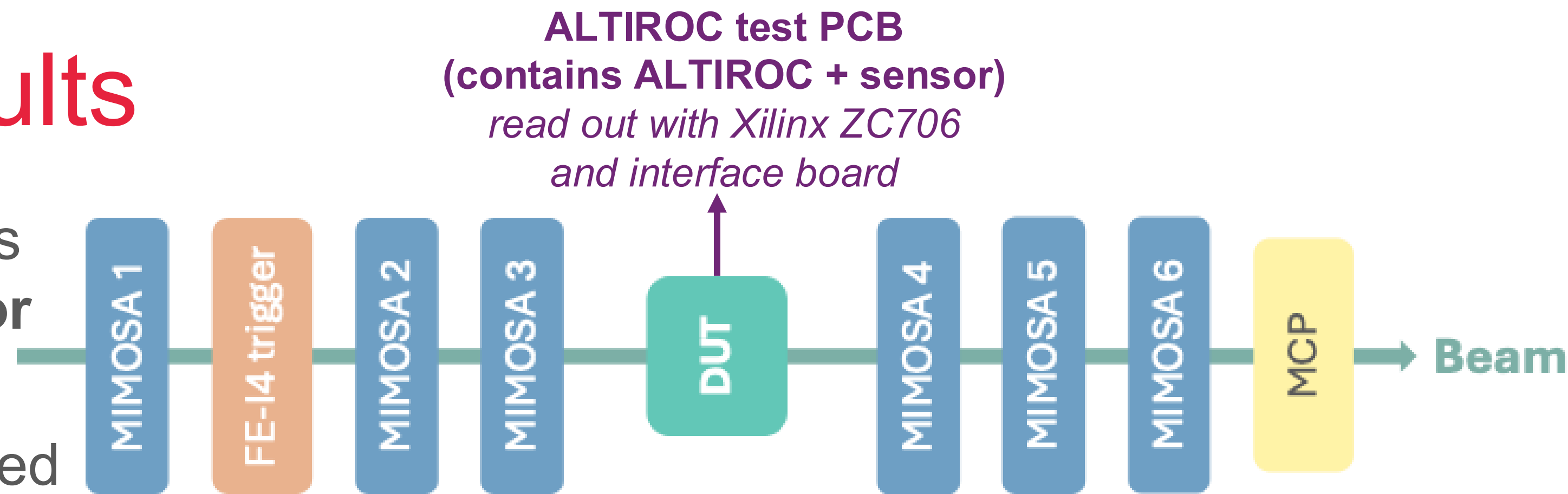
- 130 nm CMOS technology from TSMC
- 15×15 matrix matched to the LGAD pixel matrix
 - **Timing measurement: Time of Arrival (ToA)** with **20 ps** least significant bit (LSB) and **Time over Threshold (ToT)** with **40 ps** LSB
 - **Luminosity measurement:** per-bunch luminosity as number of hits in two windows
- Requirements
 - Power dissipation < **1.2 W**
 - Jitter < **25 (65) ps** for **10 (4) fC**
 - Minimal detectable charge of **2 fC** with > **95% eff. @ 4 fC**
 - Radiation hard up to **2 MGy**
- Roadmap: ALTIROC 0 (R&D, 2016) $\rightarrow$ 1 $\rightarrow$ 2 $\rightarrow$ 3 $\rightarrow$ A (Production, 2025)
- Extensive efforts in characterization, around **2000** ALTIROC-A ASICs probed

ALTIROC-A



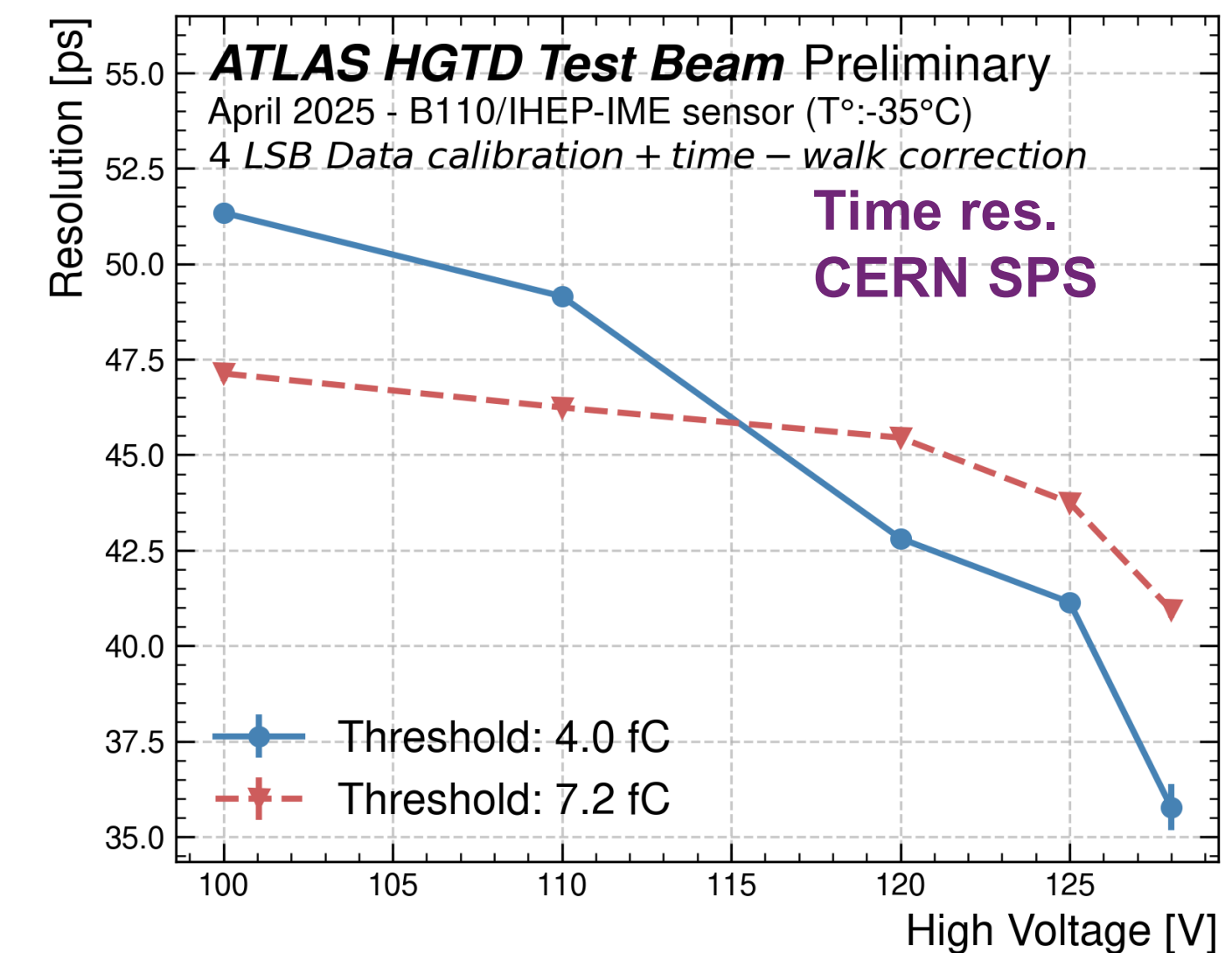
ALTIROC: test beam results

- The DUT consists of an **ALTIROC-A** that's bump-bonded to a **pre-production sensor** and wire-bonded to a **test PCB**
- Xilinx ZC706 FPGA board** with a dedicated interface board is used for DUT readout
- Results:
 - CERN SPS (-35°C):** Best time resolution of ~ 36 ps (unirradiated) with B110 compared to ~ 30 ps from sensor only test beam results
 - DESY (15°C , ambient):** Best time resolution of ~ 44 – 45 ps across the tested DUTs
 - ALTIROC-A demonstrates **excellent** timing performance



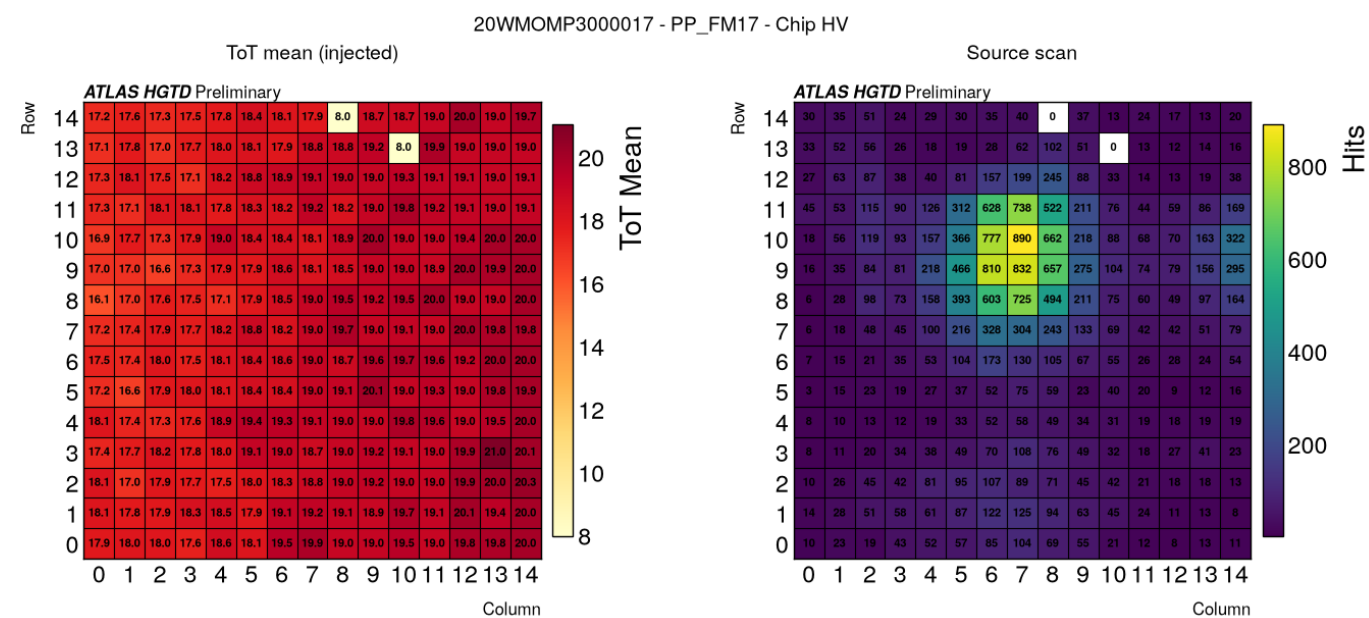
[HGTDTestBeamALTIROCA](#)

More details in Steffie's [talk](#) that comes after



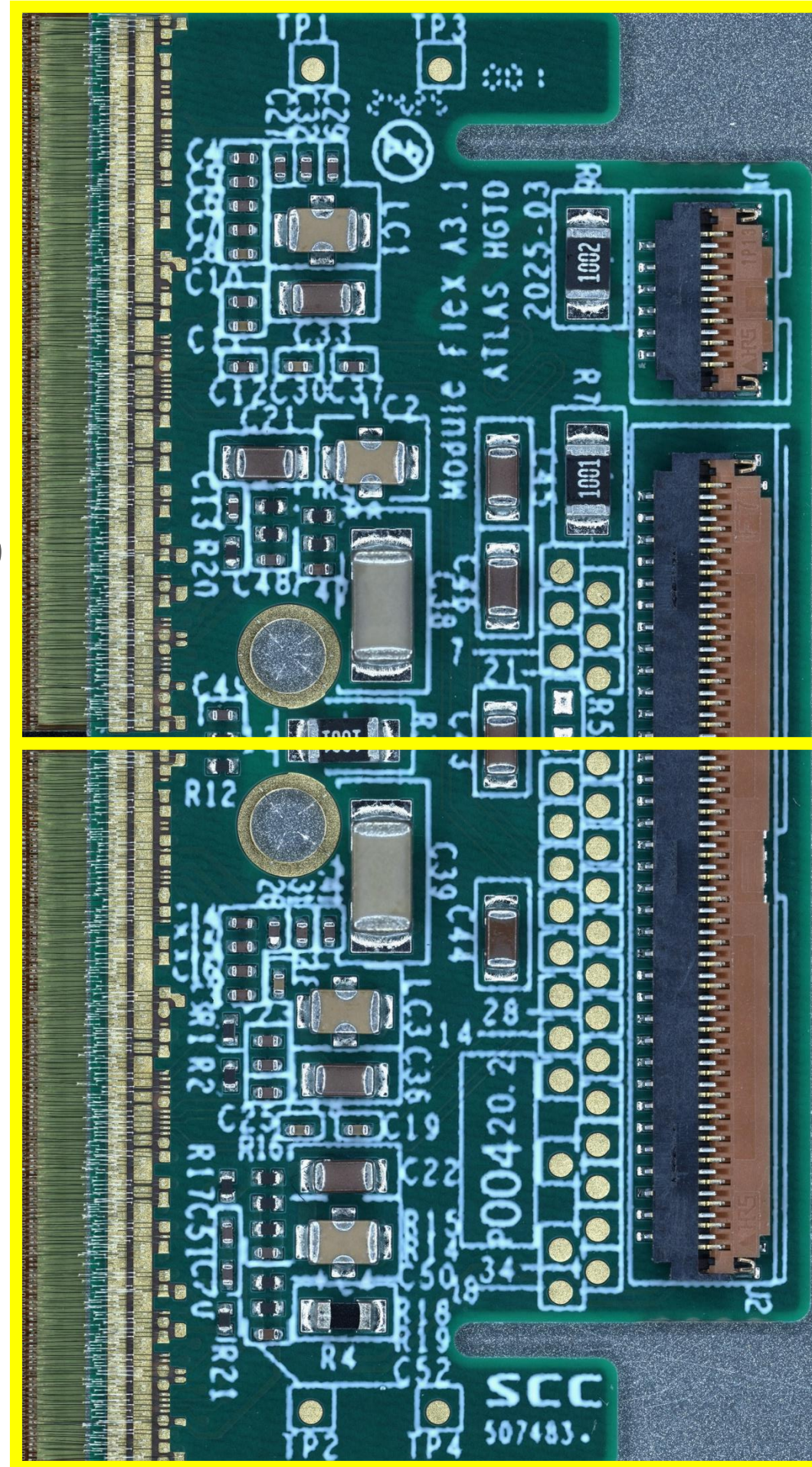
LGAD modules

- Module assembly:
 - An **LGAD** is **bump-bonded** to an **ALTIROC** to form a **hybrid**
 - **Two hybrids** are glued onto a module flex to form a **module**
 - Both LGADs and ASICs are **wire-bonded** to the flex, with FPC connector linking to peripheral electronics
- Assembly tolerance: **~100 μm**
- Entering production phase, with **>120 of 8032** modules assembled and tested



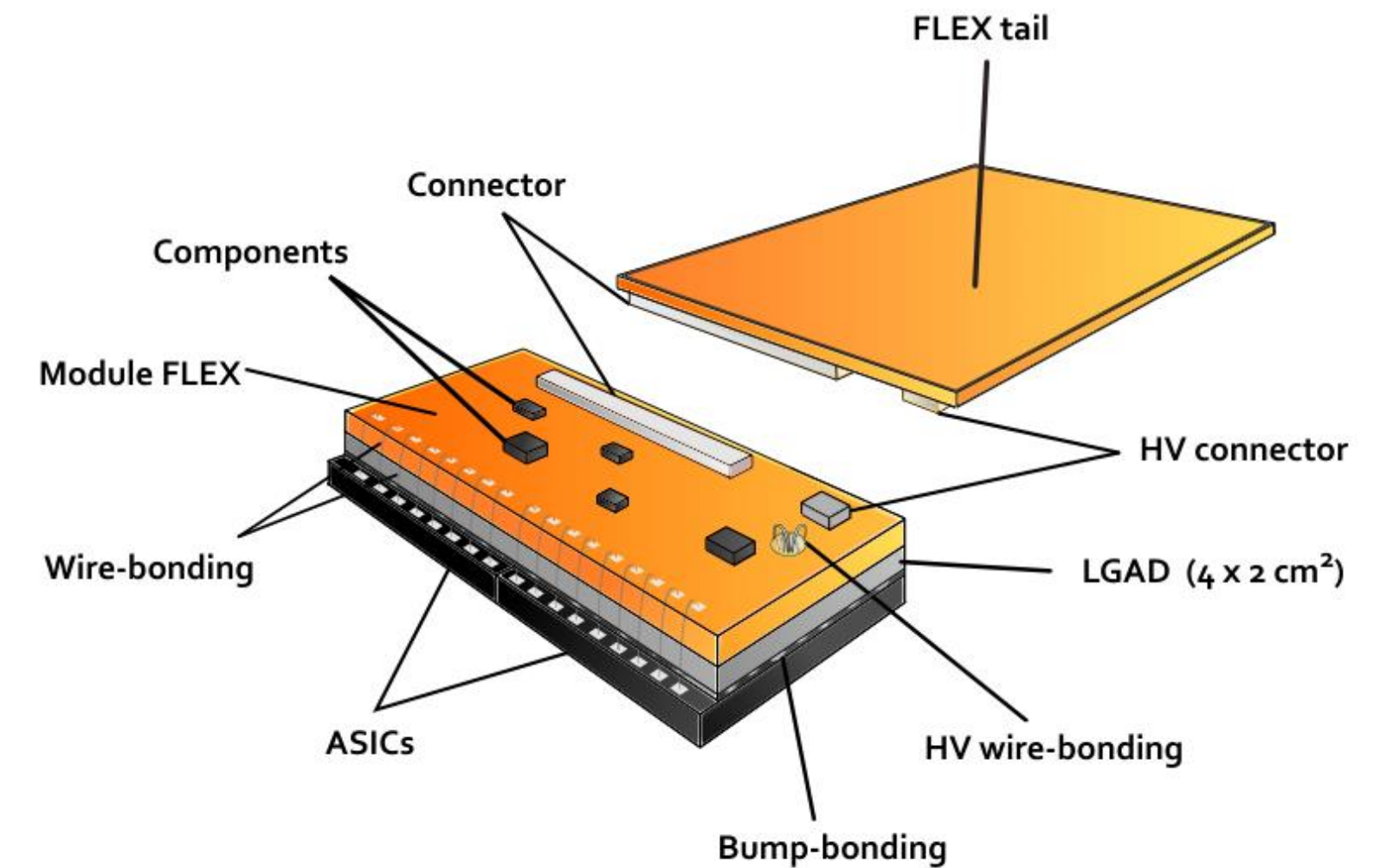
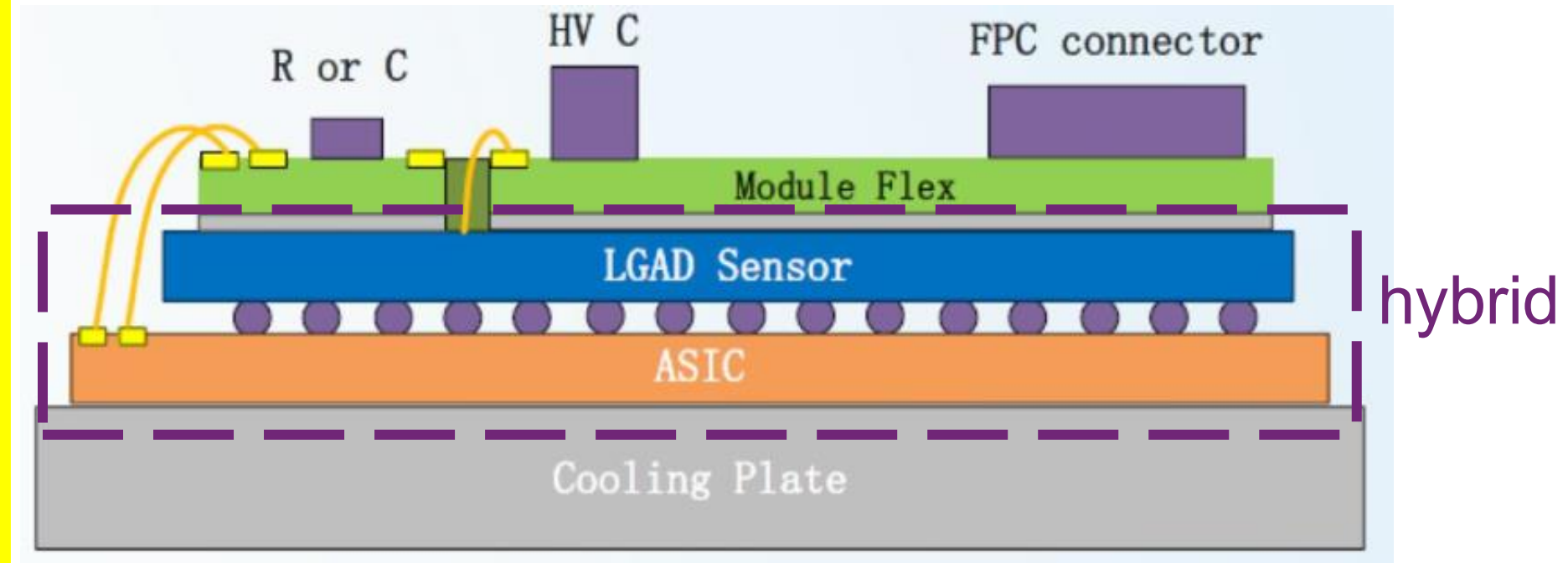
Tests to check bump connection

Module (2 hybrids)



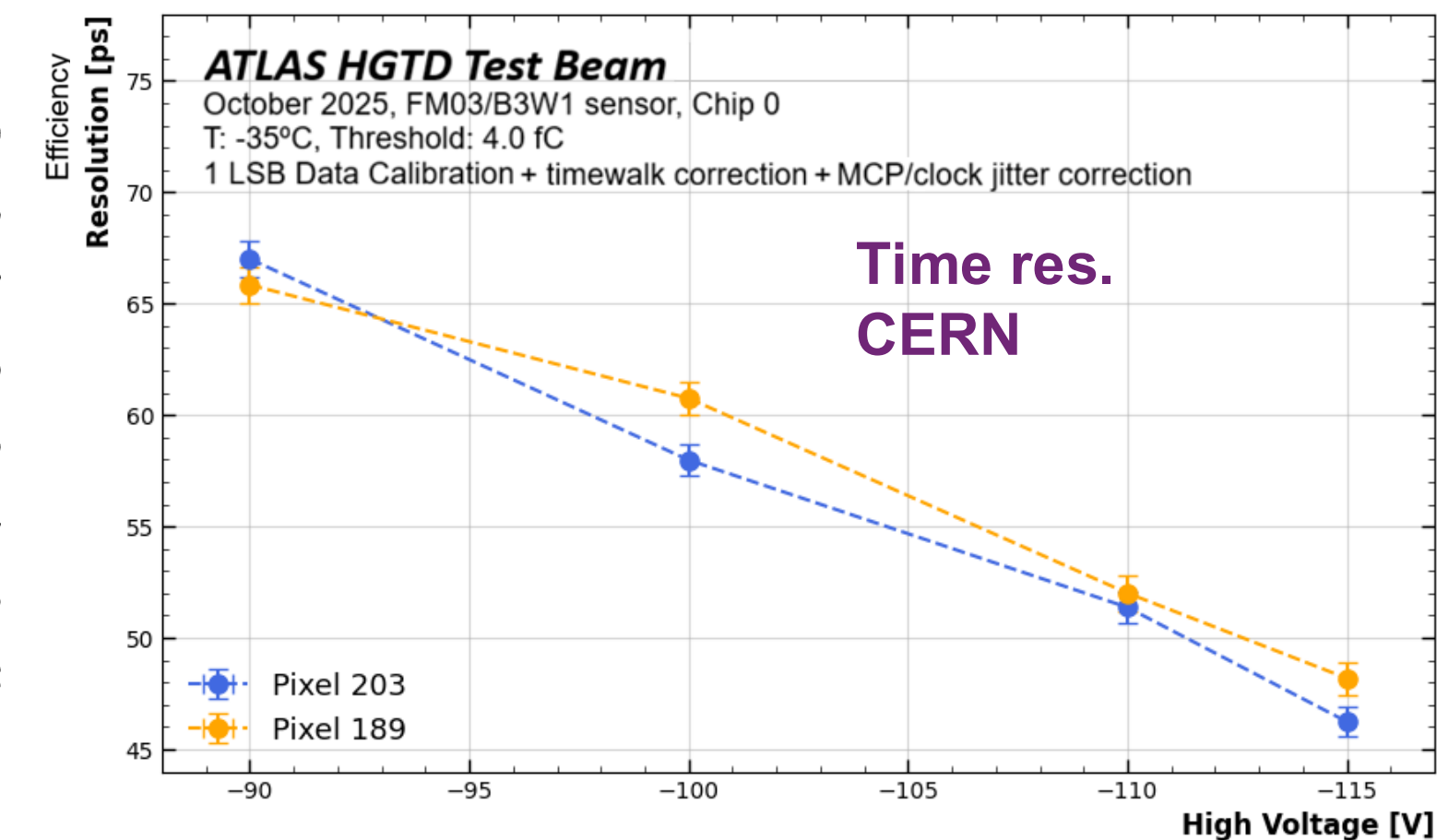
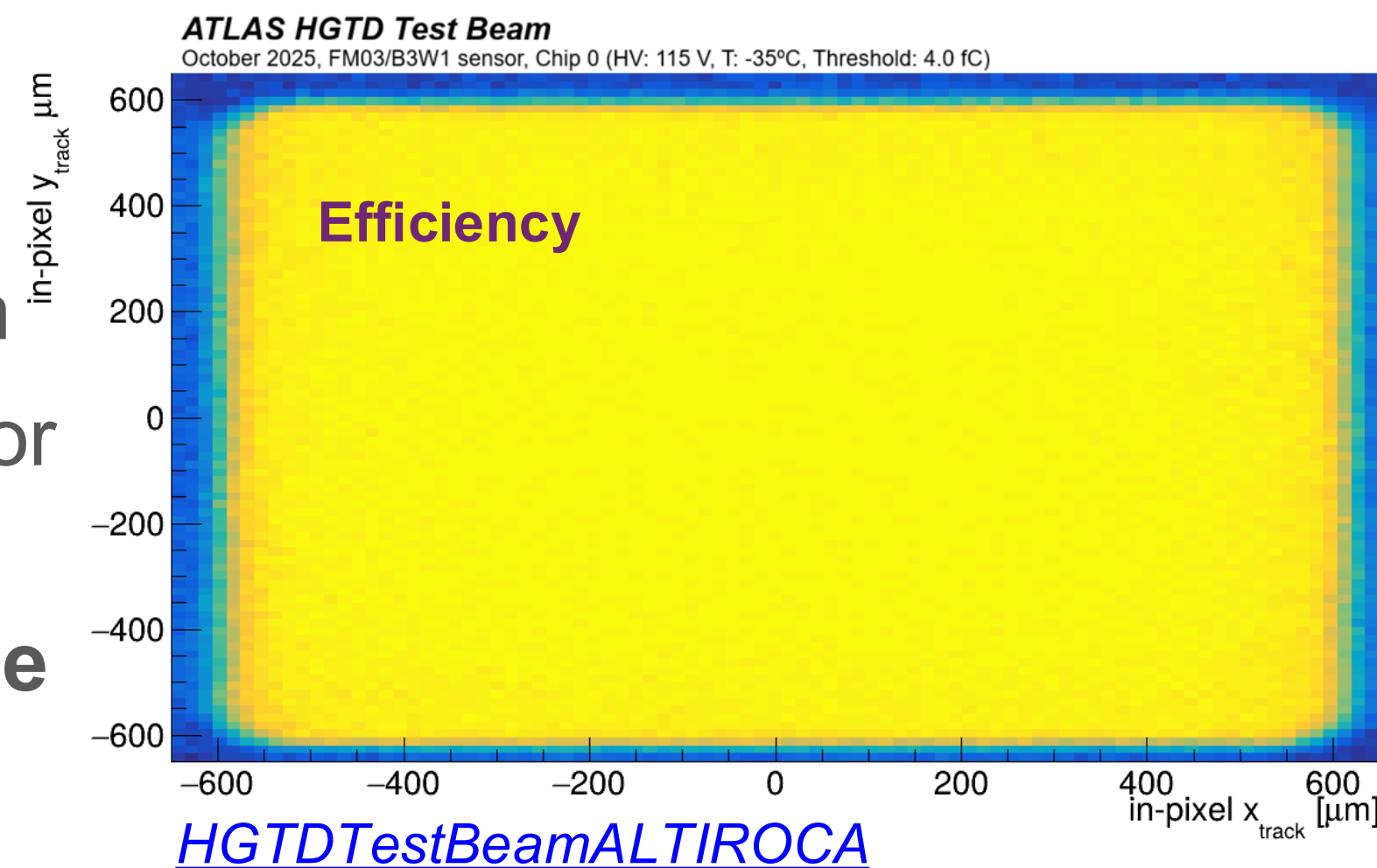
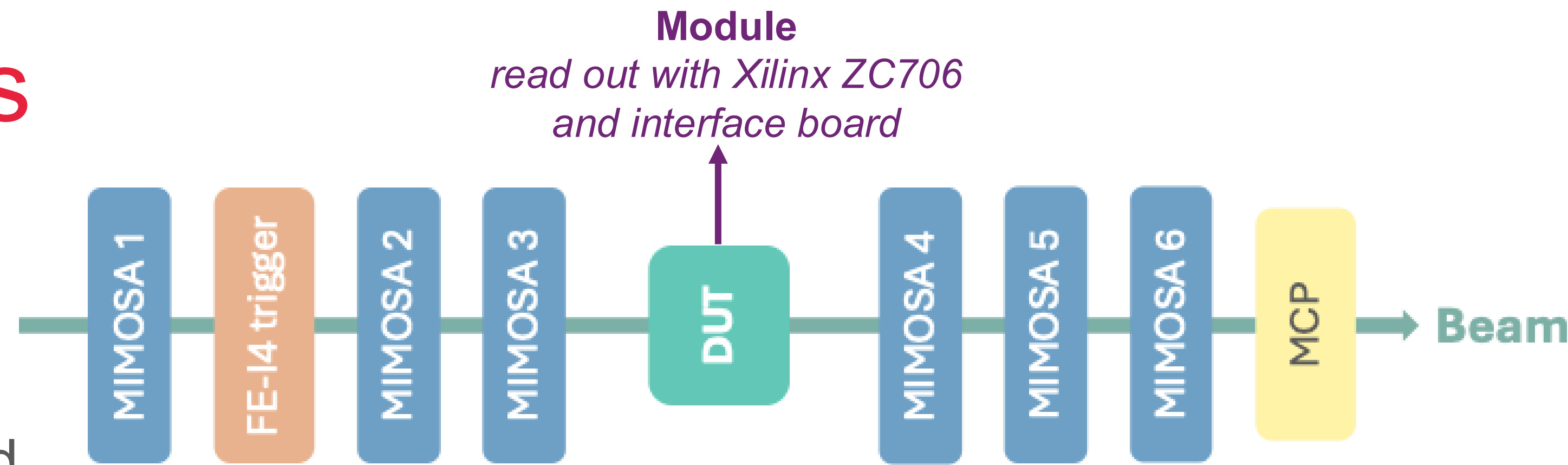
HGTDPublicPlots

Side view



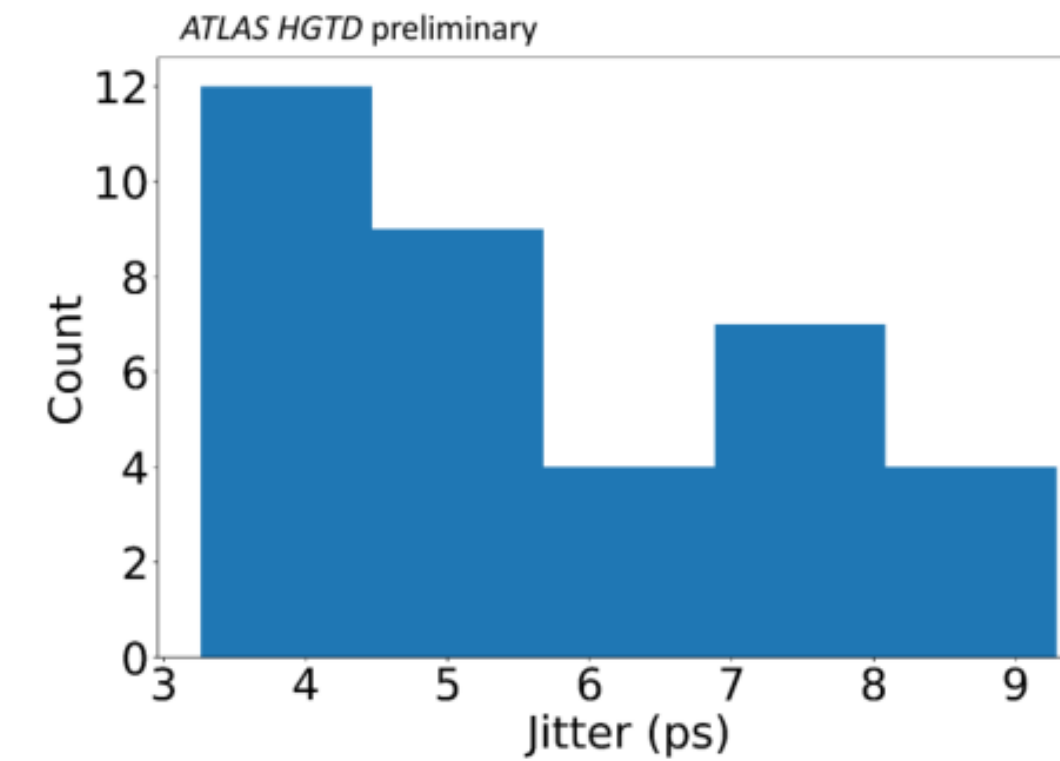
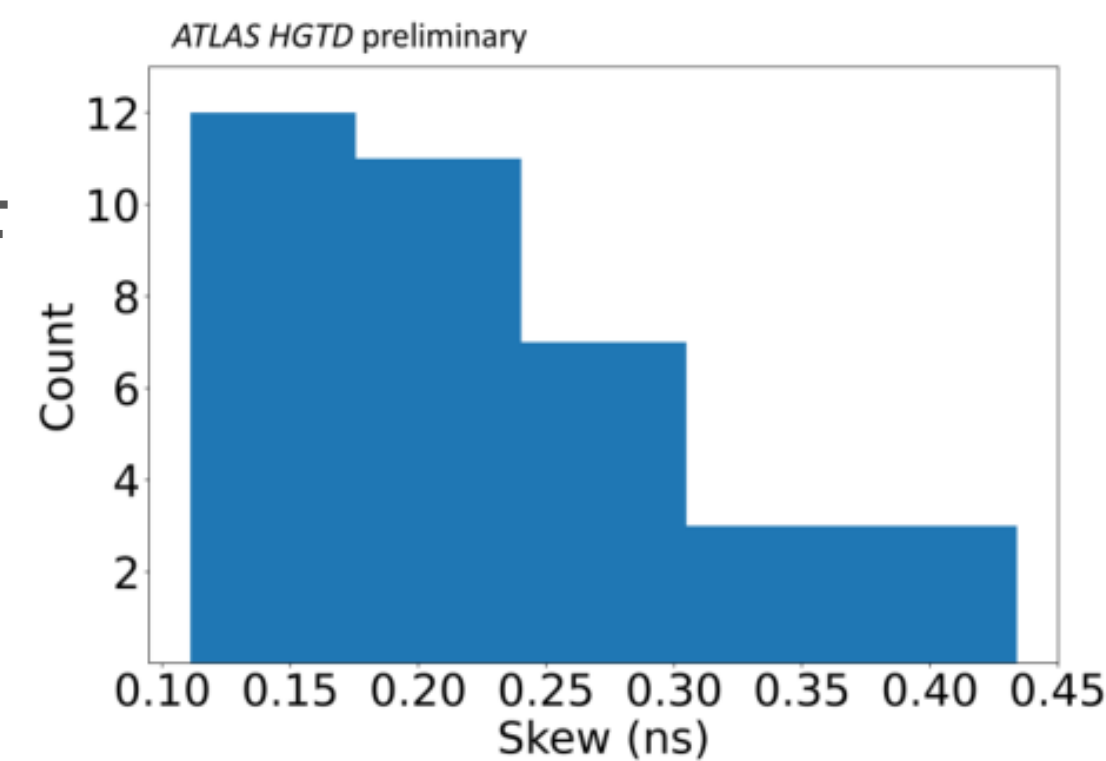
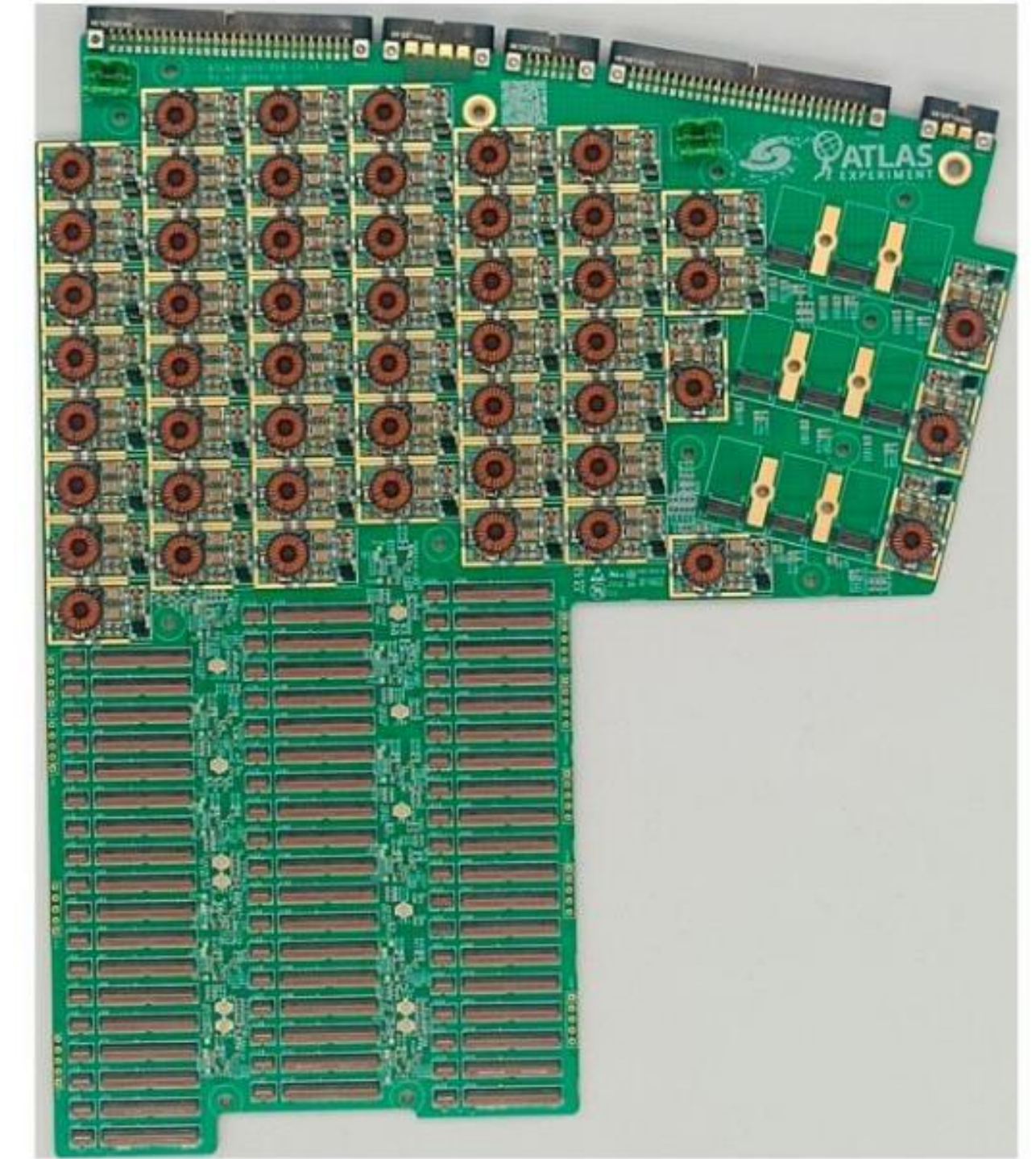
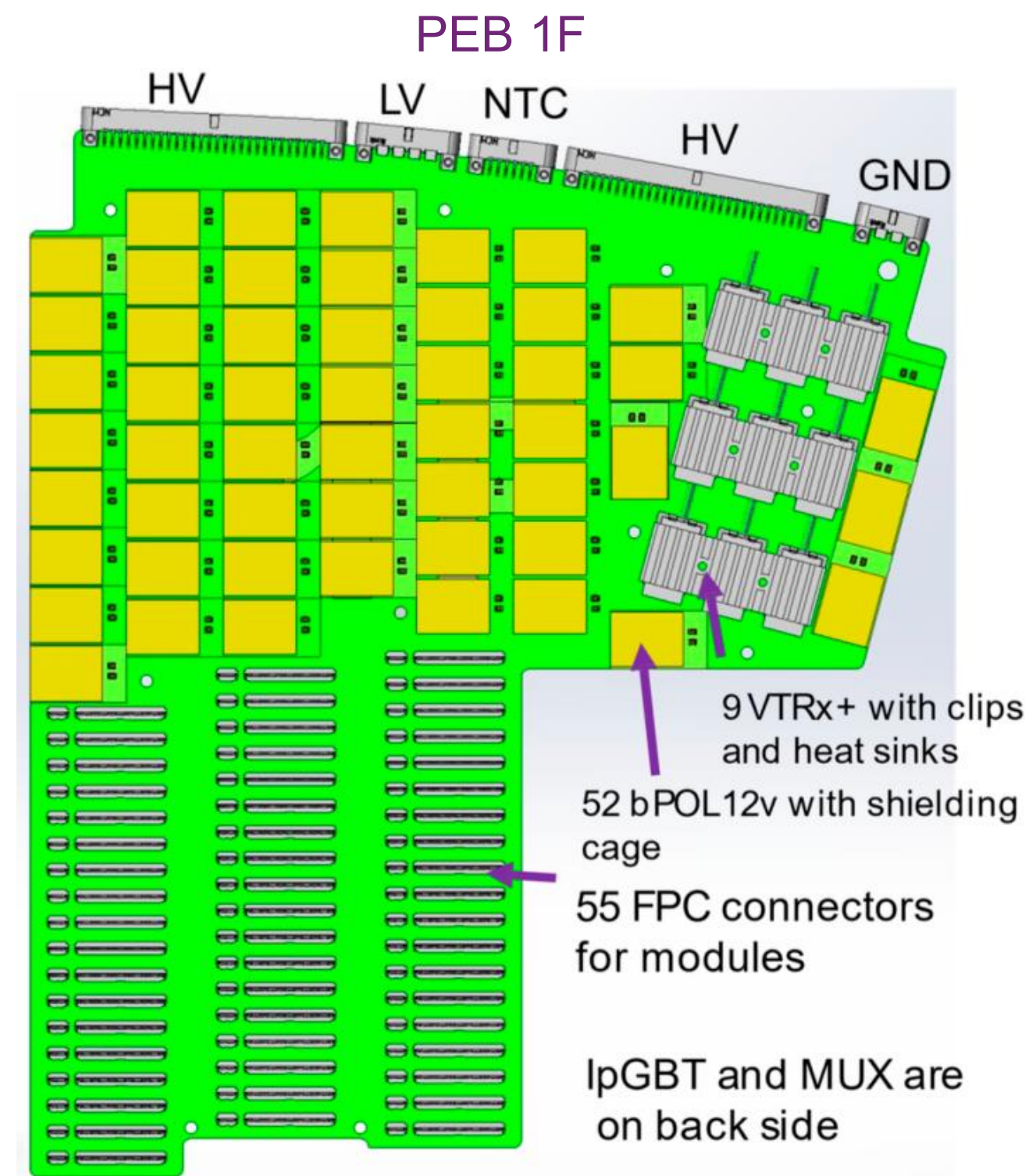
Module: test beam results

- **DUT: ALTIROC-A** full module with pre-production LGAD sensors
- Readout done by a **Xilinx ZC706 FPGA board** through a dedicated interface board
- **HGTD-designed flex tails** connect the module to the interface board
- Results:
 - **Efficiency:** $> 98\%$ in the gain region
 - **Time resolution (-35°C):** $< 50\text{ ps}$ for highest bias voltage point
 - **Both meet the HGTD performance requirements**



Peripheral Electronics

- **Peripheral Electronics Board (PEB)** locates at the rim of HGTD disk
 - 22-layer High-Density Interconnect (HDI) PCB with **radiation-tolerant** design
 - 6 different designs to cover the geometry, total required PEBs: **160**
 - Built with **IpGBT chip** (data aggregation) and **VTRx+** (optical link), both developed by CERN
 - Provides **power** and interconnect the **HV**, **control**, **monitoring**, **clock** and **data transfer** from modules to data acquisition (DAQ) system
 - **~63 Gbps** data rate per PEB
- Roadmap: Modular PEB (2022) → PEB 1F prototype (2023) → Pre-production (2025)

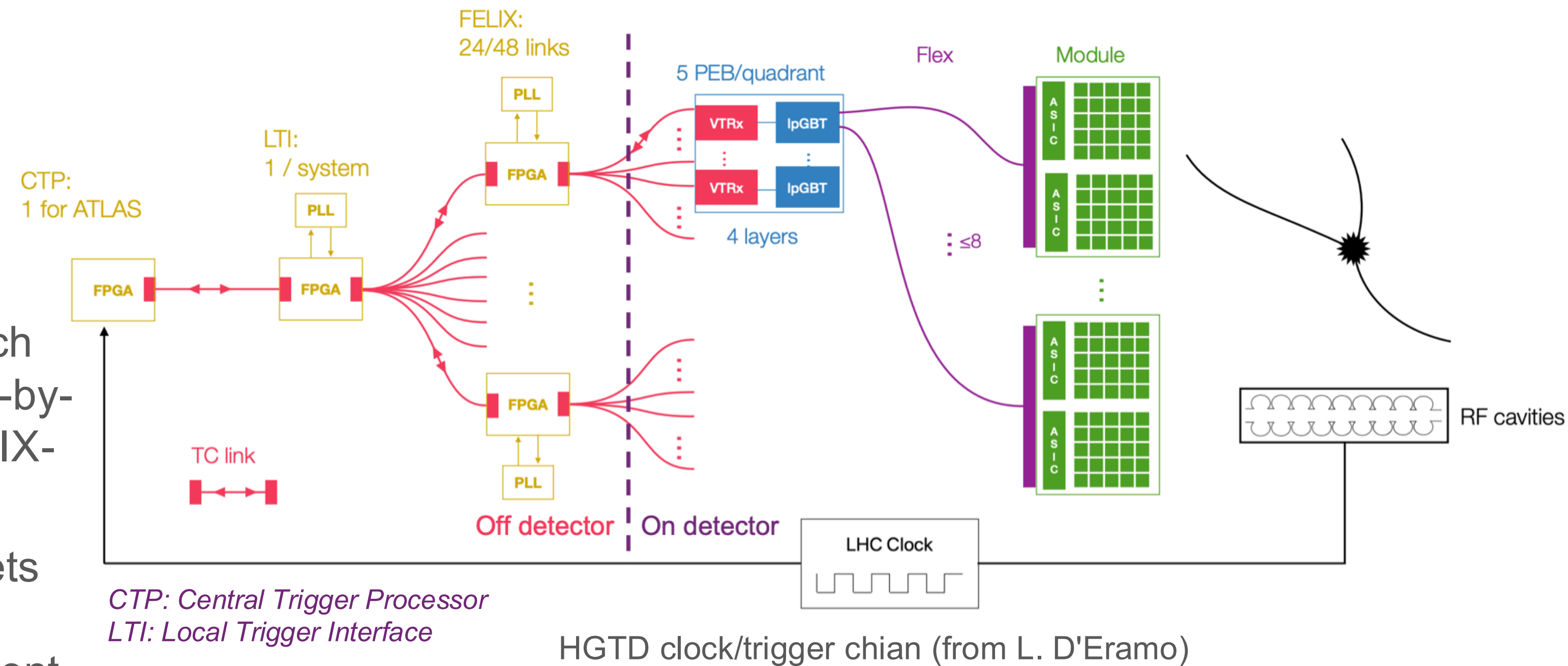


Skew and jitter for PEB clock signals connected to a module within the expected limits

[ATL-HGTD-PROC-2024-003](#)

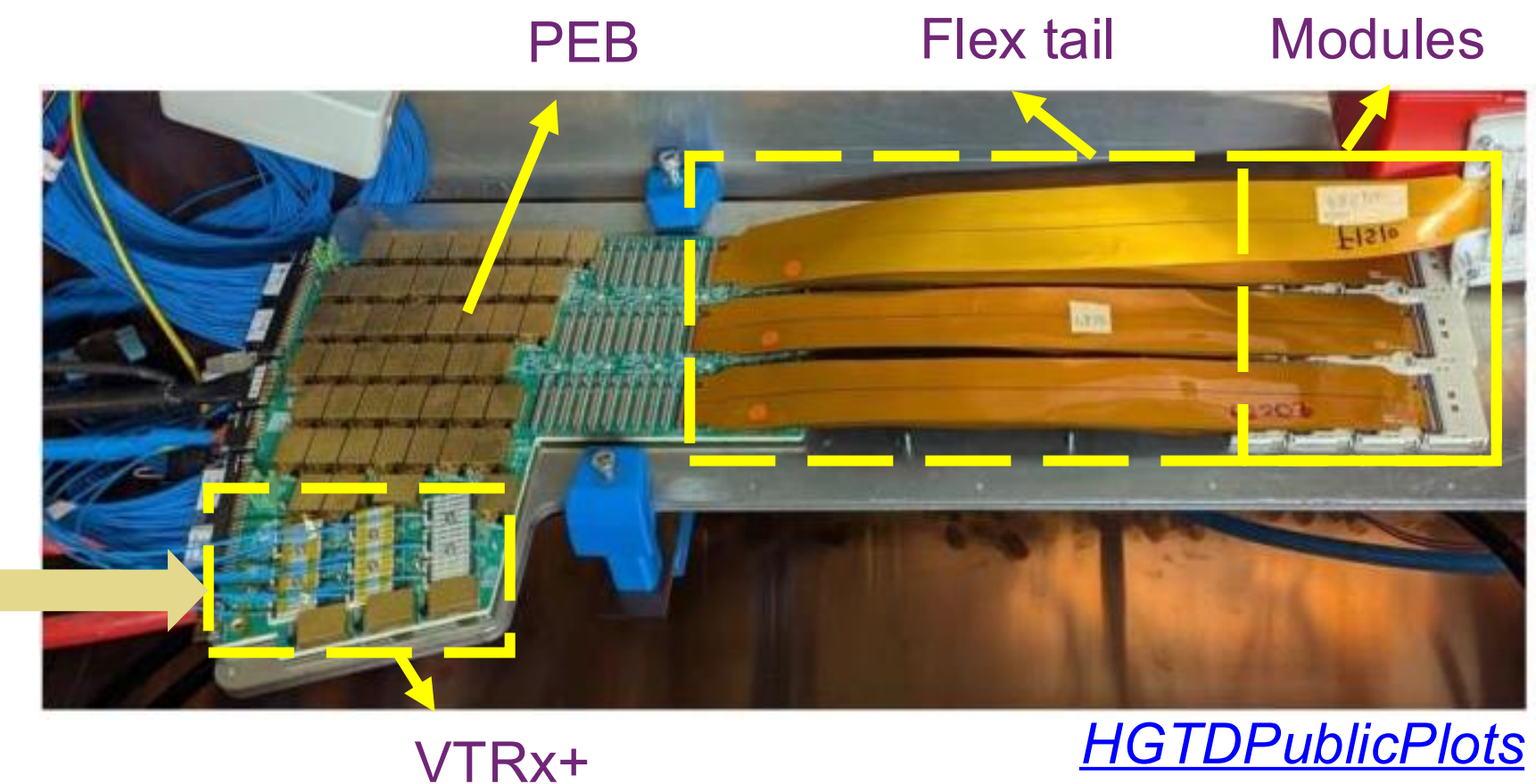
Data Acquisition (DAQ)

- Off-detector DAQ in USA15
 - The optical links from the **PEB (VTRx+)** are collected by **FELIX-155**
 - Two data streams: **timing** (TOA/TOT for each hit per triggered event) + **luminosity** (bunch-by-bunch hits). Each stream is received by FELIX-155 flashed with corresponding firmware
 - Data Handlers** aggregate FELIX data packets into detector-specific fragments and forward them to the **ATLAS Dataflow system** for event building
 - DAQ software under active development



FELIX-155

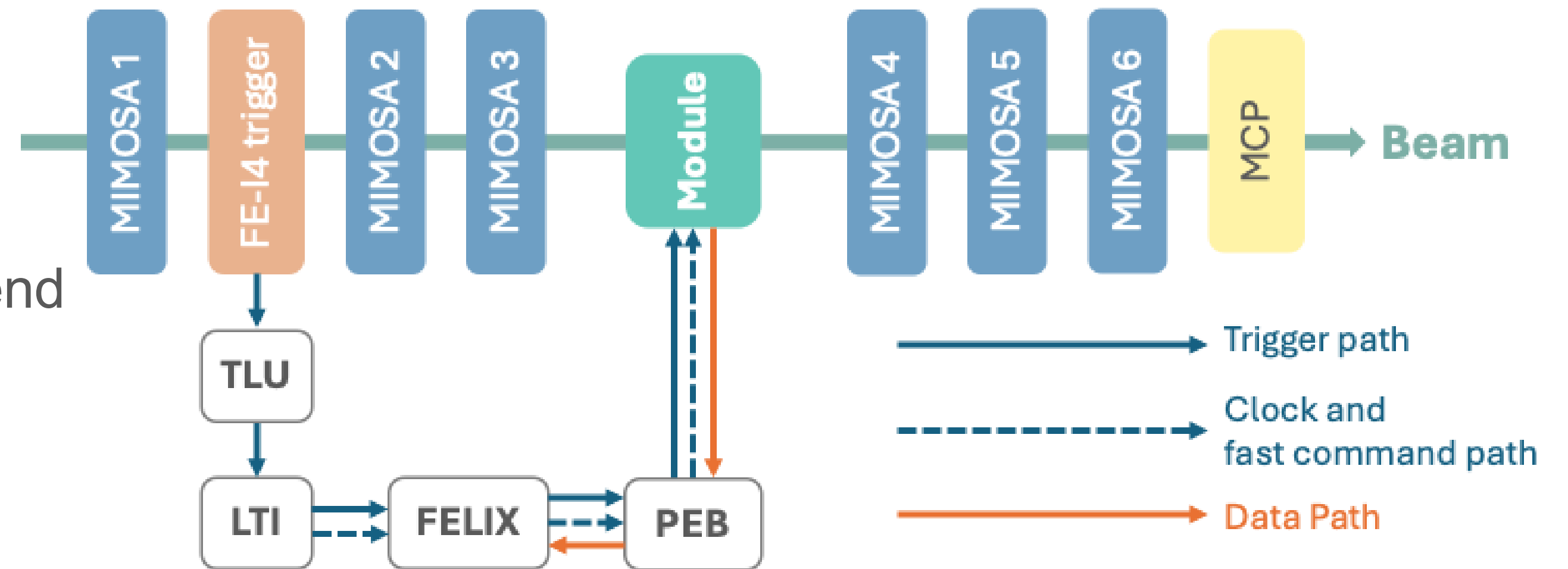
Fibers



HGTDPublicPlots

HGTD test beam on DAQ

- Test beam at SPS in July 2026:
 - First time with ATLAS phase-II equipment for trigger/clock distribution (**LTI**), chip readout and calibration with **PEB** and **FELIX**, and full end-to-end **luminosity** readout
 - Almost everything in the HGTD clock and trigger chain, with latest HGTD DAQ software
- Testing
 - DAQ software
 - Clock and trigger chain
 - **Timing performance** including effect from LTI, FELIX, PEB (compared to module test beam)
 - **Luminosity** measurement performance

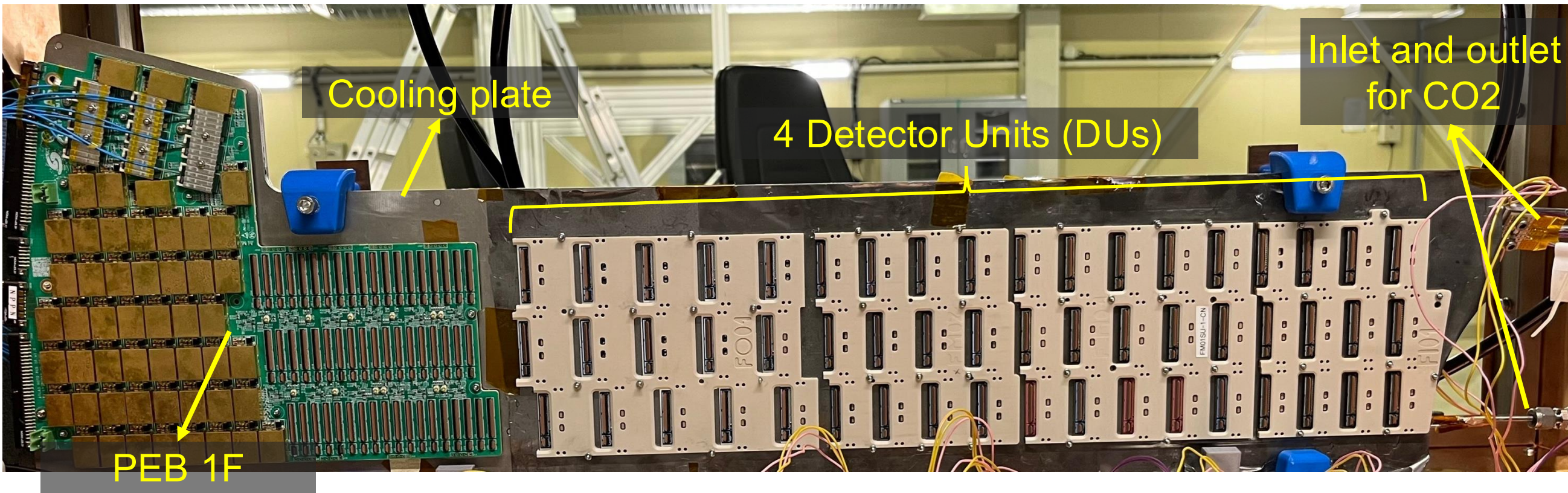


- Test-beam data analysis ongoing for both **timing performance** and **luminosity measurements**
- More test beams on DAQ planned

HGTD Demonstrator

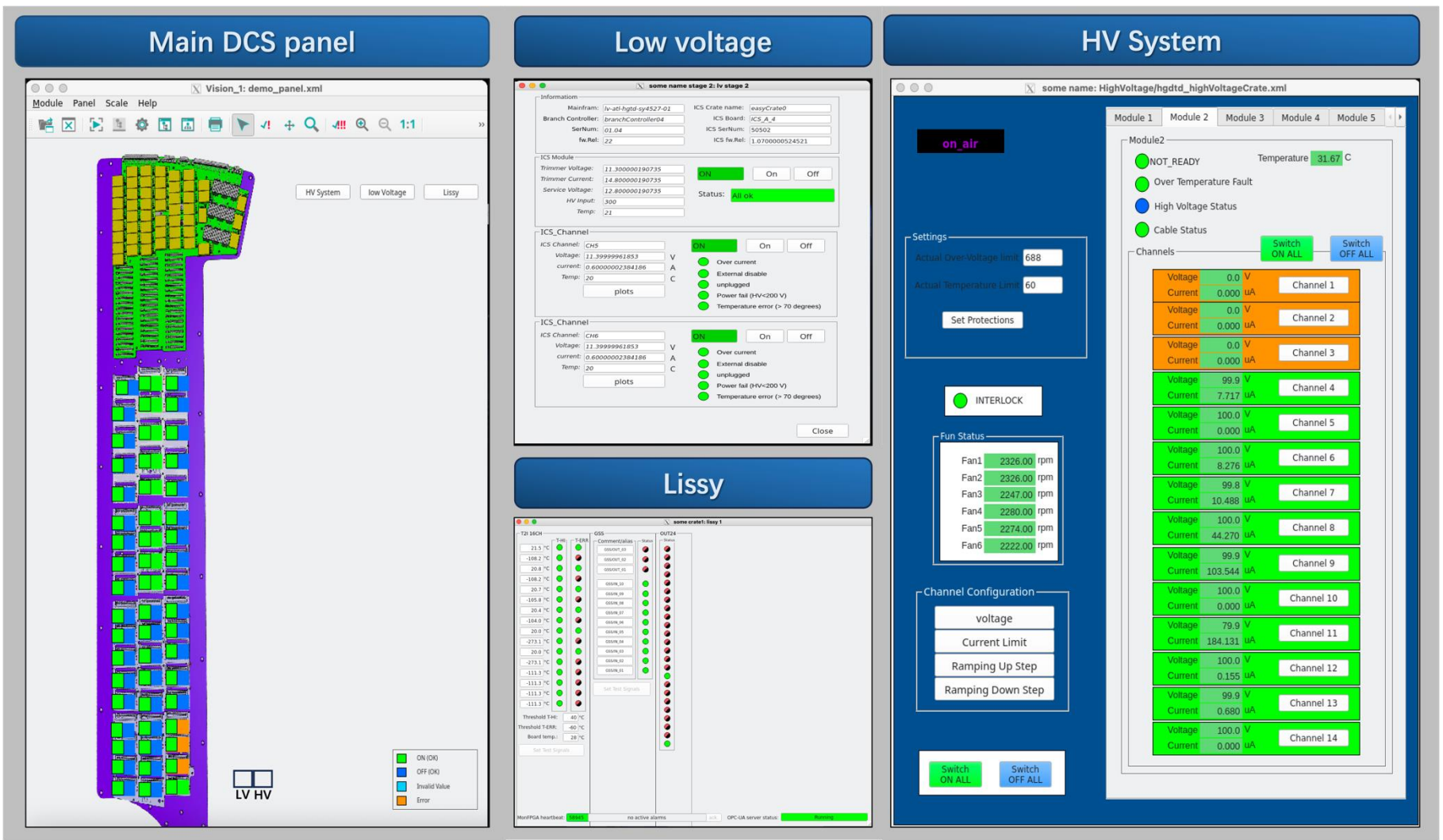
- 1st generation demonstrator assembled with R&D modules of type ALTIROC-2 and 3
- Test of the installation procedures, PEB readout ([JINST 19 \(2024\) C12012](#)), cooling, DCS (Detector Control System)
- 2nd generation demonstrator to be assembled in 2026
- **ALTIROC-A** modules: full study of the final system performance
- A one-side full quarter of HGTD (**Module-0**) will be built in 2026
- Practice full scale test and integration procedures

First generation demonstrator (ALTIROC 2 + 3)



DAQ and DCS Rack

DCS interface



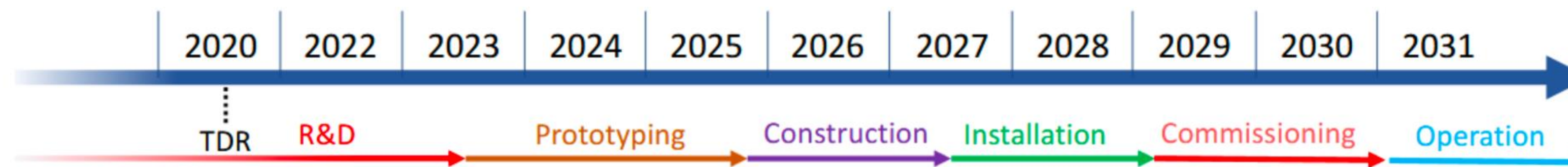
Cooling box



[HGTDPublicPlots](#)

Summary

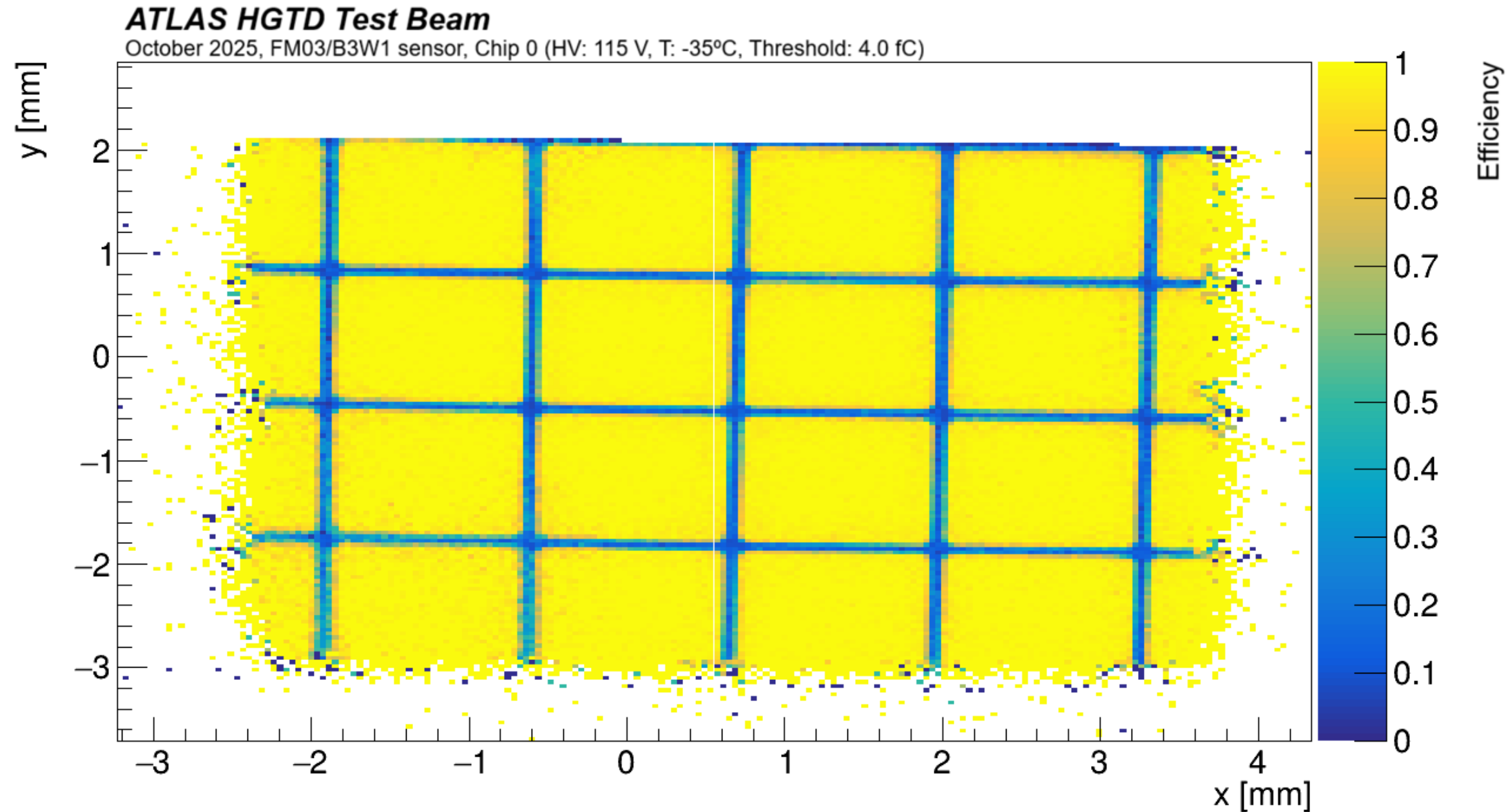
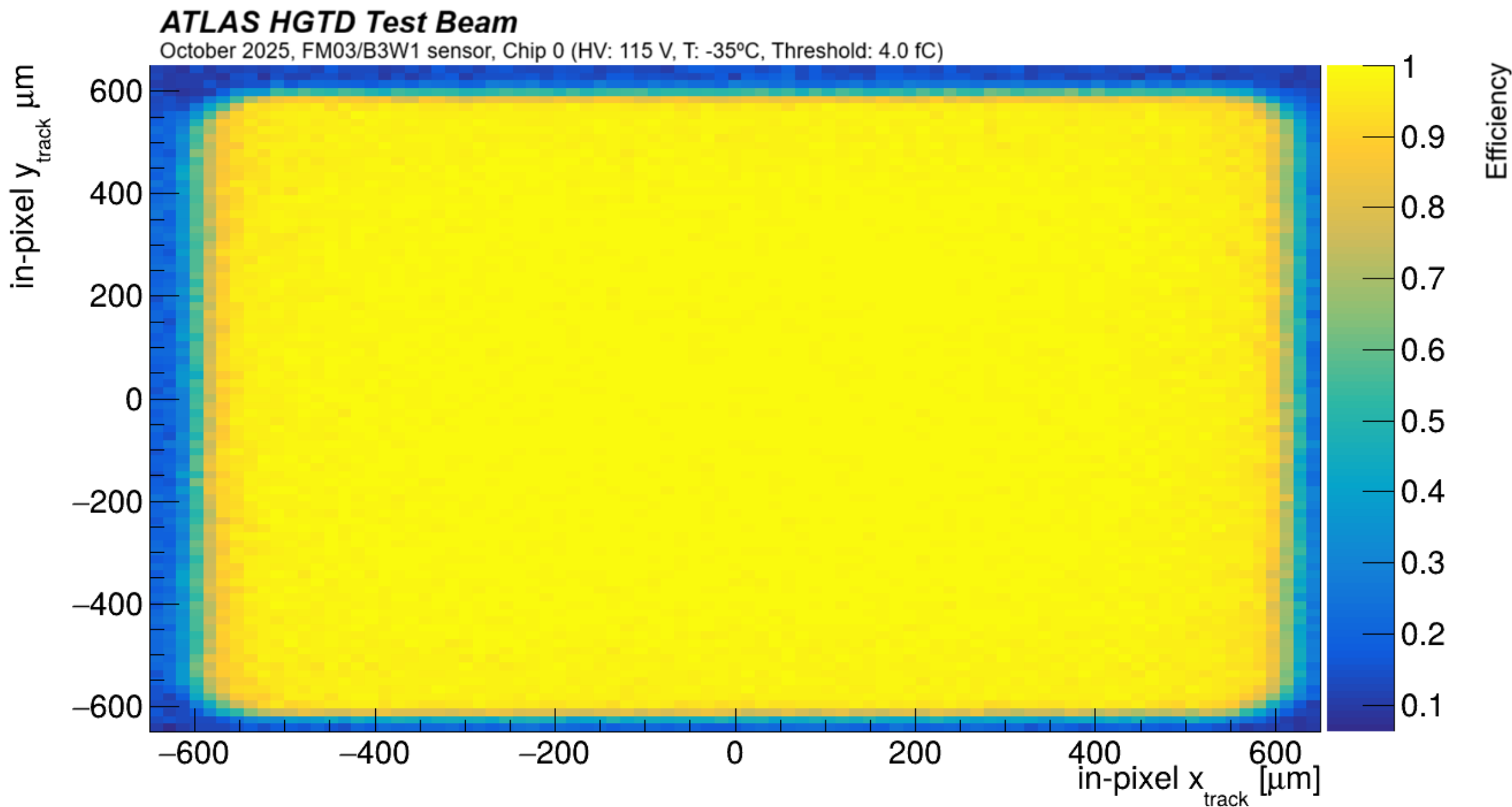
- **HGTD** provides precision timing (**30–50 ps** per track) in the forward region (**$2.4 < |\eta| < 4.0$**), primarily to mitigate pile-up at the HL-LHC
- **R&D** phase completed, with performance within specification, project now entering **(pre-)production**:
 - LGAD sensor: In **production**, **~10000** of the **~16000** has been fabricated
 - ALTIROC-A chip: In **production**, **~2000** ALTIROC-A ASICs probed
 - Module: Entering **production**, **>120** of 8032 modules assembled and tested
 - PEB: In **pre-production**, with features ready
- Complete system exercised on the demonstrator: **PEB**, **FELIX DAQ**, and **DCS** all working
- Next up: **2nd-generation demonstrator** (ALTIROC-A) and **Module-0** (one quarter disk), finish construction



Roadmap from K. Tariq, 14th Beam Telescopes and Test Beams Workshop

Backup

SPS and DESY setup



HGTD PEB design

