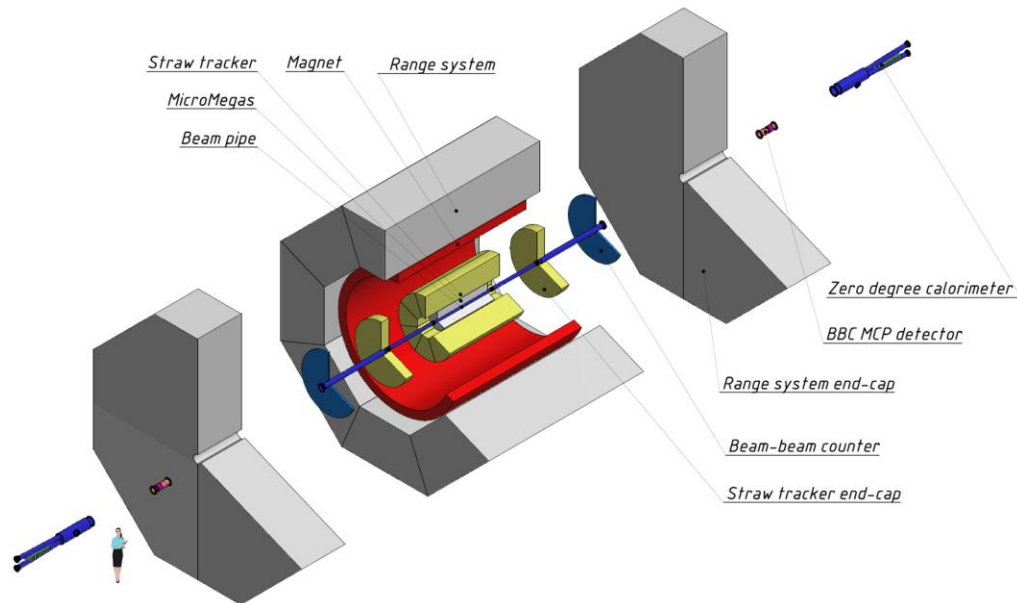


A High-Precision Time-of-Flight Detector Proposal for the SPD Experiment at the NICA Facility

Valery Chmill



Stages of Spin Physics Detector (SPD) project at NICA

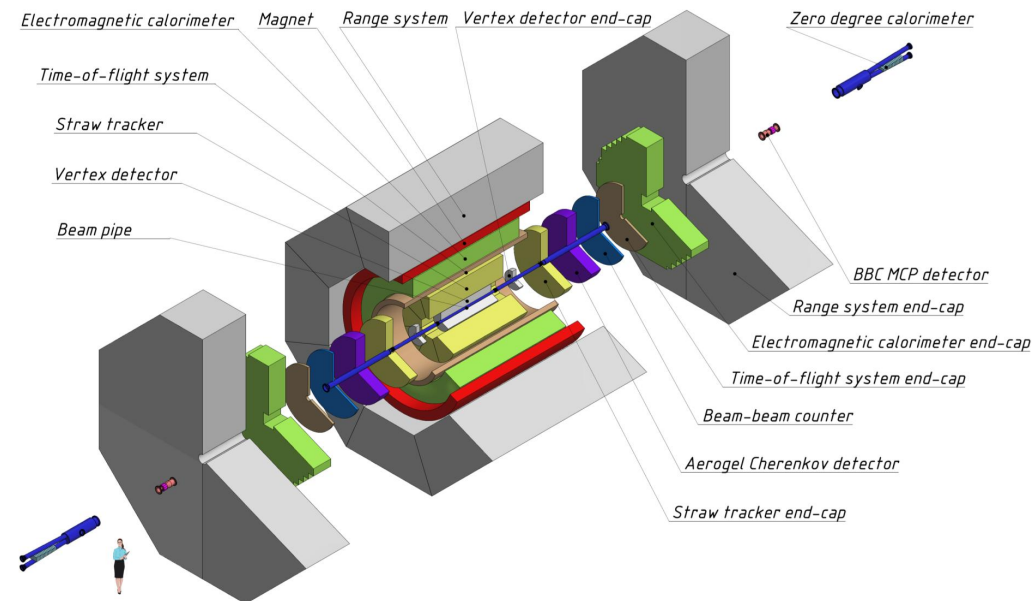


Stage I of experiment (~2031)

- Basic set of subsystems
 - Magnet, RS, Straw
 - MM, BBC, MCP, ZDC
- No PID detector (TOF, FARICH), no ECal, no SVD
- p-beam: $\sqrt{s} \lesssim 10 \text{ GeV}$, $\mathcal{L} \lesssim 10^{30} \text{ s}^{-1} \text{ cm}^{-2}$

Stage II: Fully assembled setup

- p-beam: $\sqrt{s}=27 \text{ GeV}$, $\mathcal{L}=10^{32} \text{ s}^{-1} \text{ cm}^{-2}$ with interaction rate of $\sim 4 \text{ MHz}$



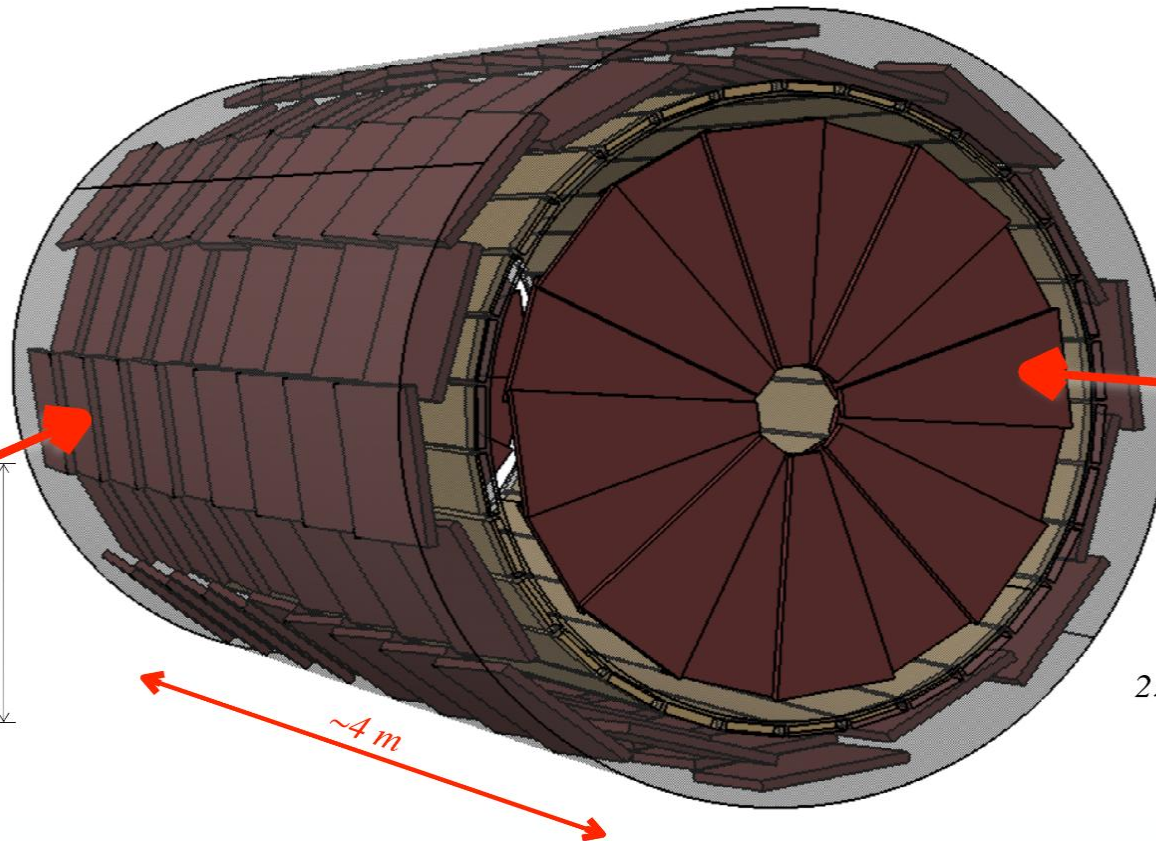
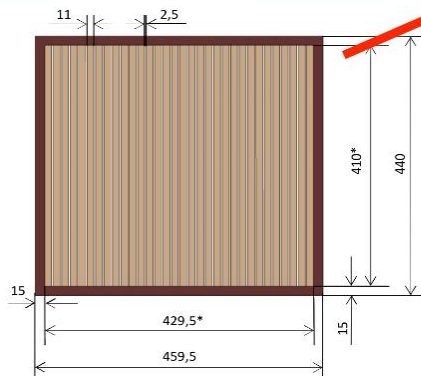
Time of Flight (TOF) detector proposal



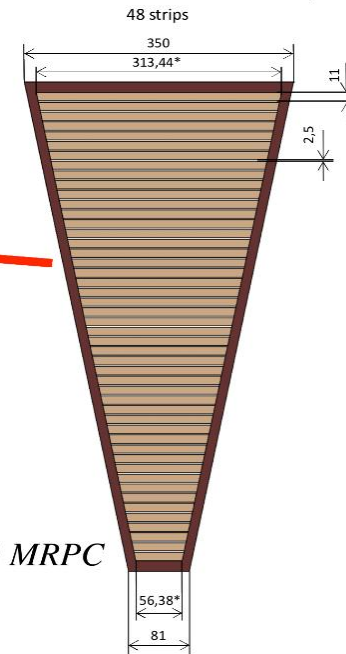
TOF Chambers for Barrel
(overlap in 2 dimensions)

$$16 \times 9 = 144 \text{ MRPC}$$

TOF Chamber
32 strips



TOF Chambers for Endcap



$$2 \times 16 = 32 \text{ MRPC}$$

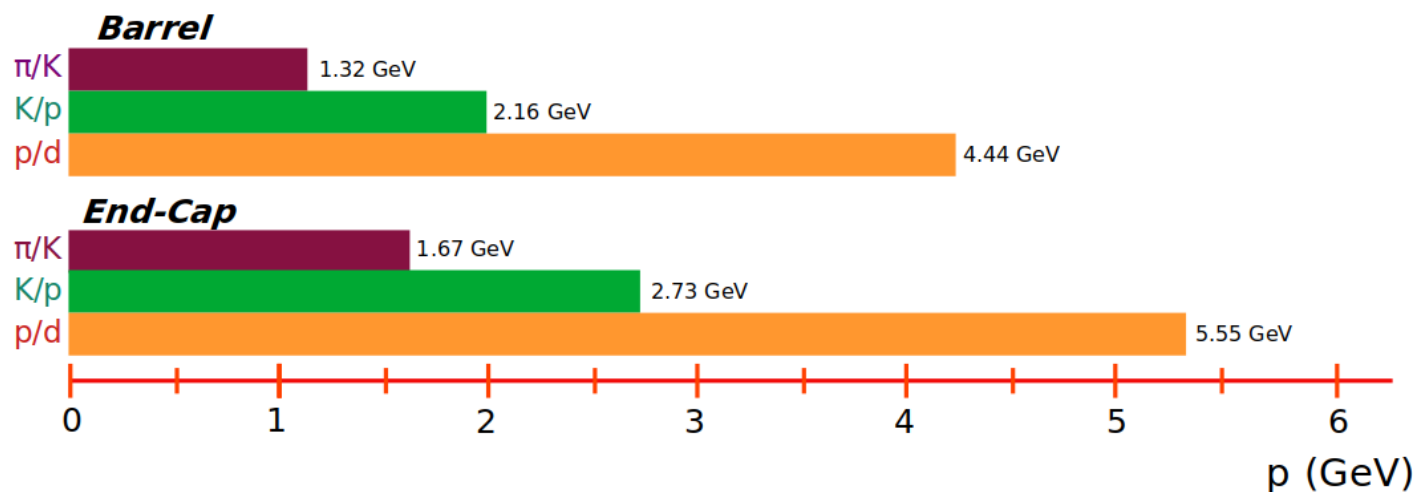
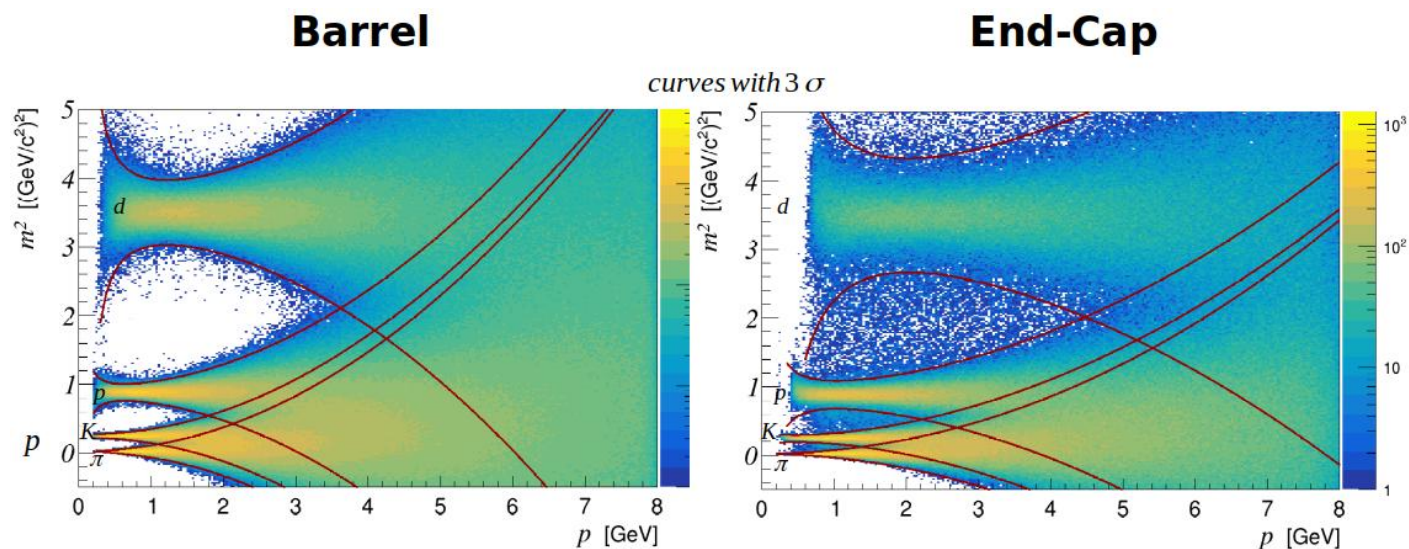
- $\pi/K/p$ discrimination for momenta $\lesssim 2 \text{ GeV}$
- Time resolution requirement $< 60 \text{ ps}$.
- Sealed (MRPC) are the base option.

- Number of readout for Barrel is $144 \times 2 \times 32 = 9216$ channels.
- Number of readout for Endcap is $32 \times 2 \times 48 = 3072$ channels.
- Total amount is **12288** channels

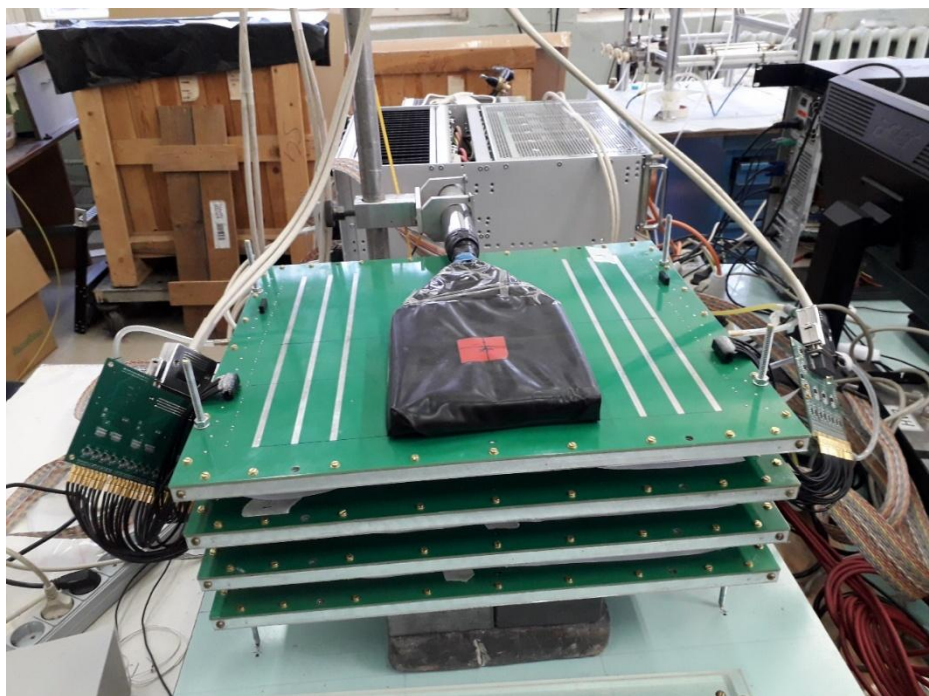
Particles ID for m^2 vs. p



- $\pi/K/p/d$ discrimination for momenta < 2 GeV
- Determination of t_0
- Time resolution requirement < 60 ps.

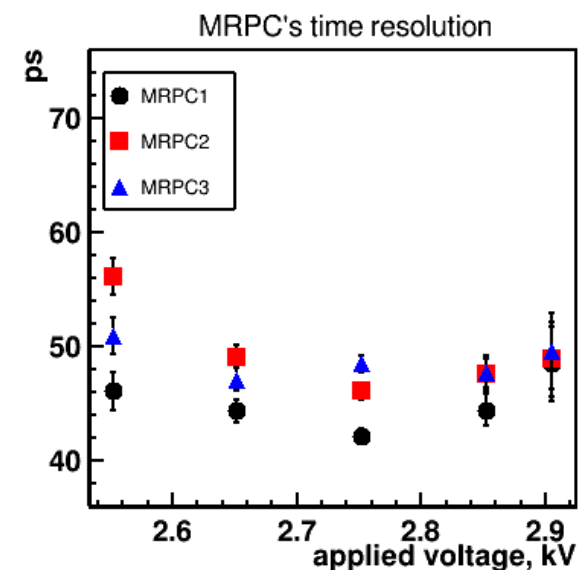
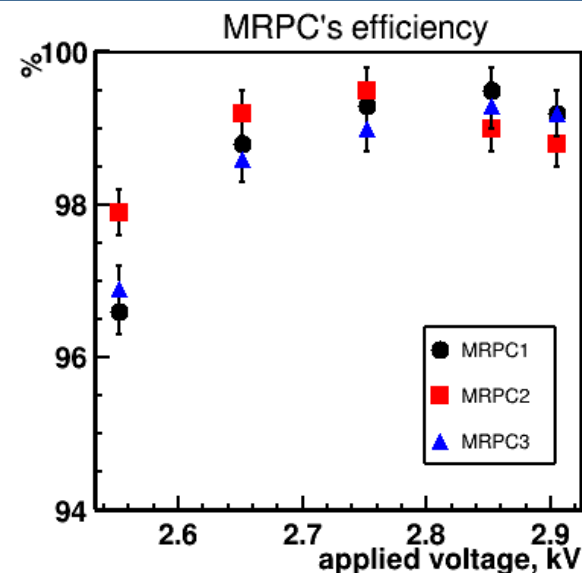


IHEP (Protvino) MRPC prototypes for the SPD



- To start MRPC and check functionality
- To obtain detection efficiency and time resolution on a new DAQ

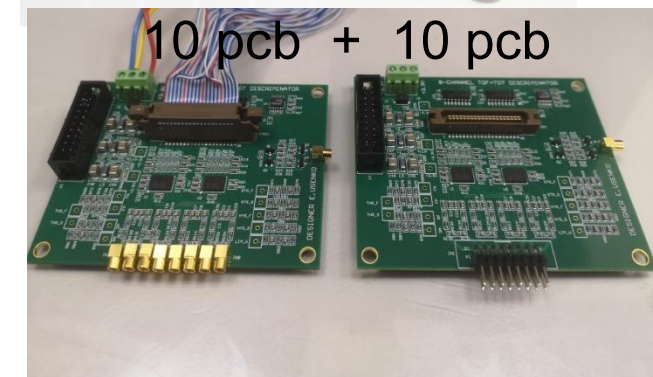
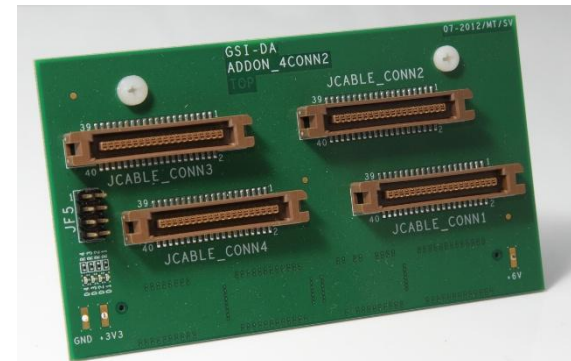
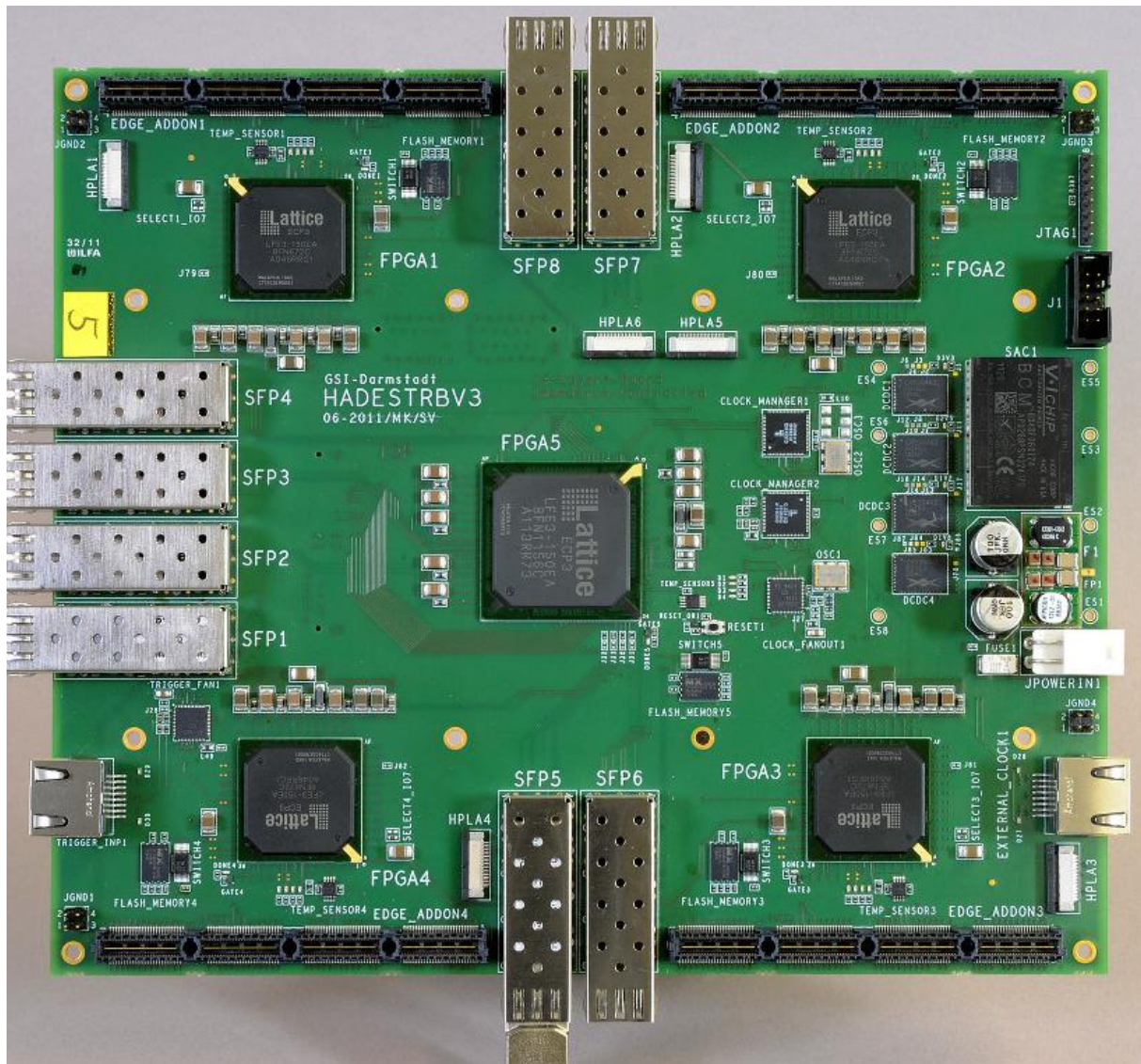
arXiv:2505.22044 Design and implementation of the constant fraction discriminator for glass MRPC timing
L.L. Kurchaninov, E.A. Ladygin, V.P. Ladygin, A.A. Semak



DAQ TRBv3 based

Valery Chmill





TDC-Readout-Board, Triggered/Triggerless-Readout-Board

Item		Value
Supply Voltage		48 V (40-50V), galvanically isolated on board
Power Supply Current		0.5A minimum without AddOns
GbE-connectivity		max. 95 MBytes/s transfer per link
GbE-slow-control		up to 400 registers/transfer, speed depends on GbE latency
Connectivity		Max. 8 SFPs, each 2GBit/s on board. With hub-addon: max. 32 SFP
		4 AddONs on top (208 pin), 1 AddOn on bottom
Max Readout Trigger Rate		about 300 kHz (depending on configuration and network size)
Max Hit Rate		50 MHz (burst of 63 hits)
TDC Channels		260 (Single edge detection)
Time Precision		<20 ps
Minimum pulse width		<500 ps

TRBv3 FPGA-TDC Based Platforms 128ch in TDC mode

WEB CTS

TDC Registers
X
TDC Registers
X
TDC Registers
X
Central Trigger System
X



Central Trigger System

- Status overview

Counter	Counts	Rate
Trigger asserted	34969050 clks.	30.00 Kcnt/s
Trigger rising edges	34969050 edges	30.00 KHz
Trigger accepted	34969050 events	30.00 KHz

Last Idle Time	30860 ns	
Last Dead Time	2470 ns	404.86 KHz
Total Dead Time	74100242 ns	7.4%

Plot will be available in a few moments

Throttle ☐ Limit Trigger Rate to KHz
 Full Stop ☐ Ignore all events

Click on the image to switch between short and long plotting intervals

Export CTS Configuration [as TrbCmd script](#) [as shell script](#)

- Trigger Channels

#	Enable	Trg. Cond.	Assignment	TrbNet Type	Asserted	Edges
0	☐	R. Edge	Periodical Pulser 0	0x1_physics_trigger	0.00 cnt/s	0.00 Hz
1	☐	R. Edge	Periodical Pulser 1	0x1_physics_trigger	25.00 Mcnt/s	25.00 MHz
2	☐	R. Edge	Random Pulser 0	0x1_physics_trigger	0.00 cnt/s	0.00 Hz
3	☐	R. Edge	Input Multiplexer 0	0x1_physics_trigger	100.00 Mcnt/s	0.00 Hz
4	☐	R. Edge	Input Multiplexer 1	0x1_physics_trigger	2365.45 cnt/s	2365.45 Hz
5	☐	R. Edge	Input Multiplexer 2	0x1_physics_trigger	100.00 Mcnt/s	0.00 Hz
6	☒	R. Edge	Input Multiplexer 3	0x1_physics_trigger	6.40 Mcnt/s	30.00 KHz
7	☐	R. Edge	Input Multiplexer 4	0x1_physics_trigger	0.00 cnt/s	0.00 Hz
8	☐	R. Edge	Input Multiplexer 5	0x1_physics_trigger	0.00 cnt/s	0.00 Hz
9	☐	R. Edge	Periph. FPGA Inputs 0	0x1_physics_trigger	0.00 cnt/s	0.00 Hz
10	☐	R. Edge	Periph. FPGA Inputs 1	0x1_physics_trigger	0.00 cnt/s	0.00 Hz
11	☐	R. Edge	Coincidence Module 0	0x1_physics_trigger	100.00 Mcnt/s	0.00 Hz
12	☐	R. Edge	Coincidence Module 1	0x1_physics_trigger	100.00 Mcnt/s	0.00 Hz
13	☐	R. Edge	Coincidence Module 2	0x1_physics_trigger	100.00 Mcnt/s	0.00 Hz
14	☐	R. Edge	Coincidence Module 3	0x1_physics_trigger	100.00 Mcnt/s	0.00 Hz

- Trigger Inputs

#	Source	Inp. Rate	Invert	Delay	Spike Rej.	Override	Downscale
0	extclk[0]	0.00 Hz	☐	0 ns	0 ns	bypass	
1	extclk[1]	2365.45 Hz	☐	0 ns	0 ns	bypass	
2	trgext[2]	0.00 Hz	☐	0 ns	0 ns	bypass	
3	trgext[3]	30.00 KHz	☒	0 ns	0 ns	bypass	
4	jeclin[0]	0.00 Hz	☐	0 ns	0 ns	bypass	
5	jeclin[1]	0.00 Hz	☐	0 ns	0 ns	bypass	

- Peripheral Trigger Inputs

#	from FPGA 1				from FPGA 2				from FPGA 3				from FPGA 4			
	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0
0	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐
1	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐

- Pulsers and Coincidence Detectors

Periodical Pulsers
Coincidence Detectors

ZOO on SUSE Tumbleweed:

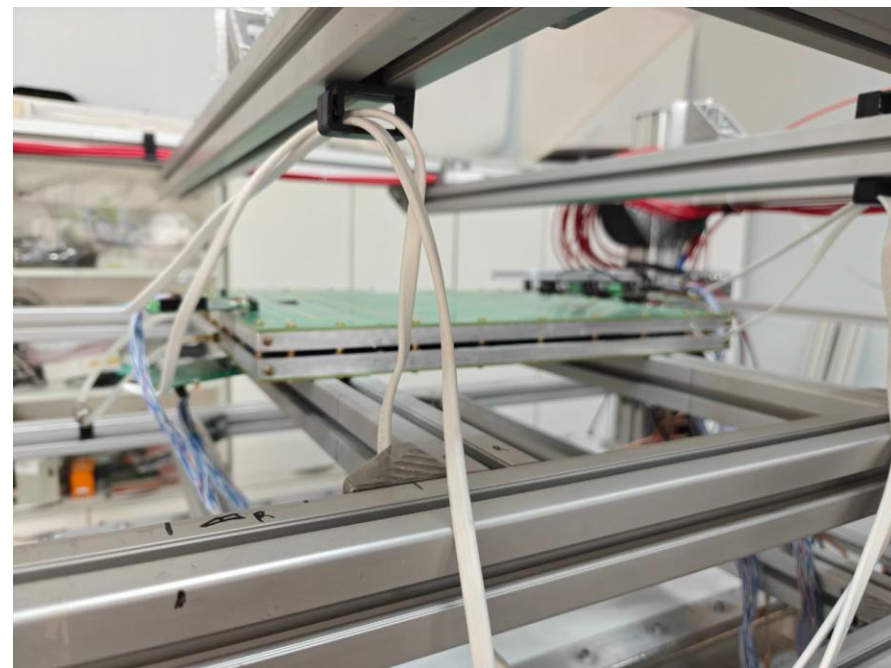
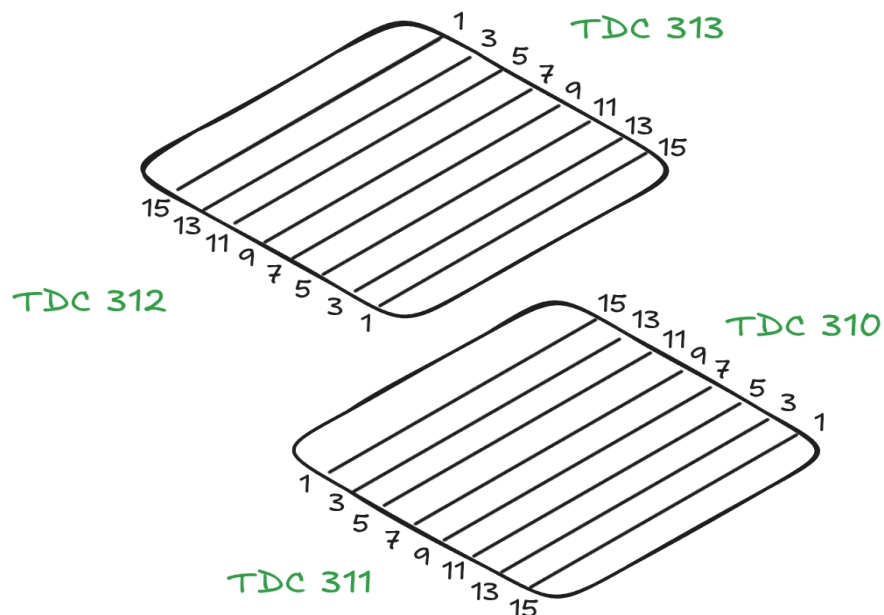
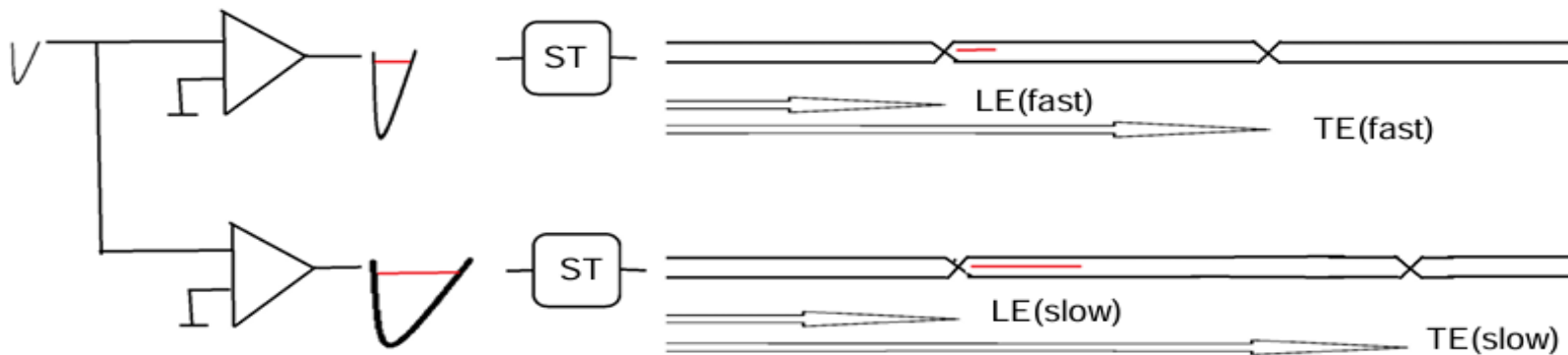
- **VHDL** is ranging from the system level down to that of logic gates, for design entry, documentation, and verification purposes.
- **Perl** Practical Extraction and Report Language.
- **XML** ExtensibleMarkupLanguage for storing, transmitting, and reconstructing arbitrary data.
- **C++** (ROOT etc.)

Status of DATA analysis

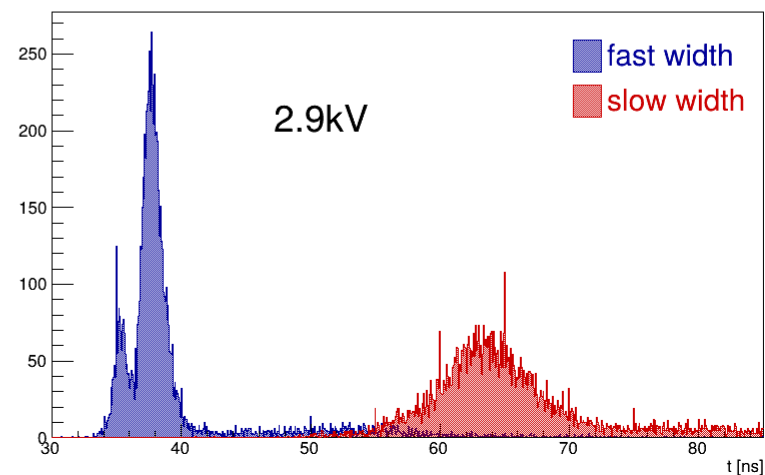
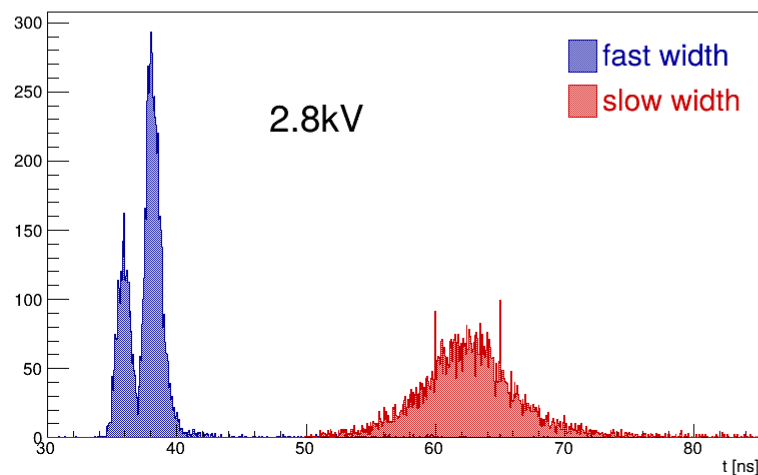
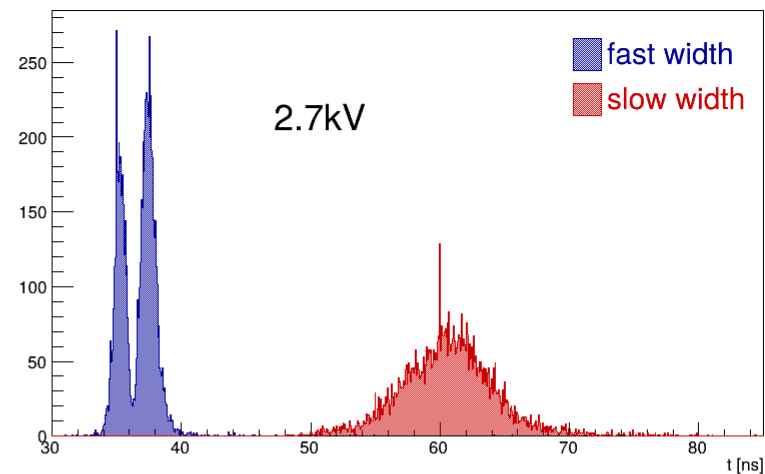
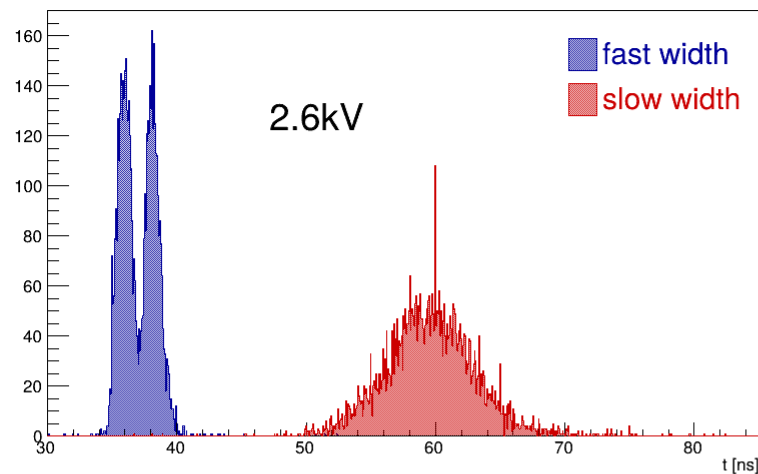
Valery Chmill



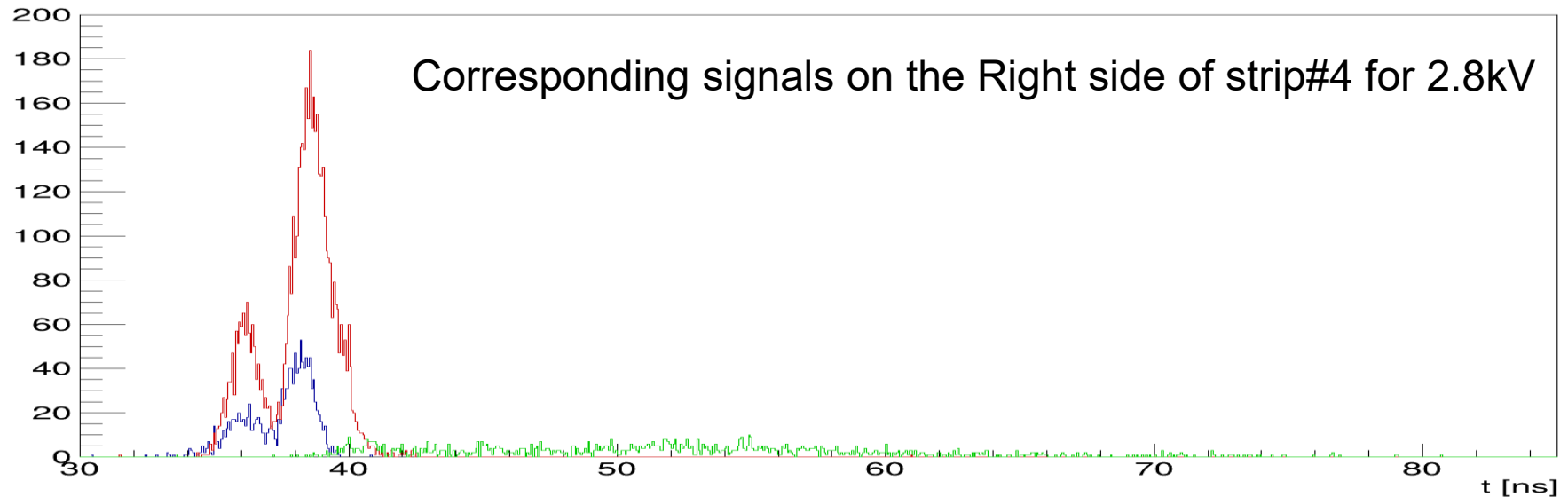
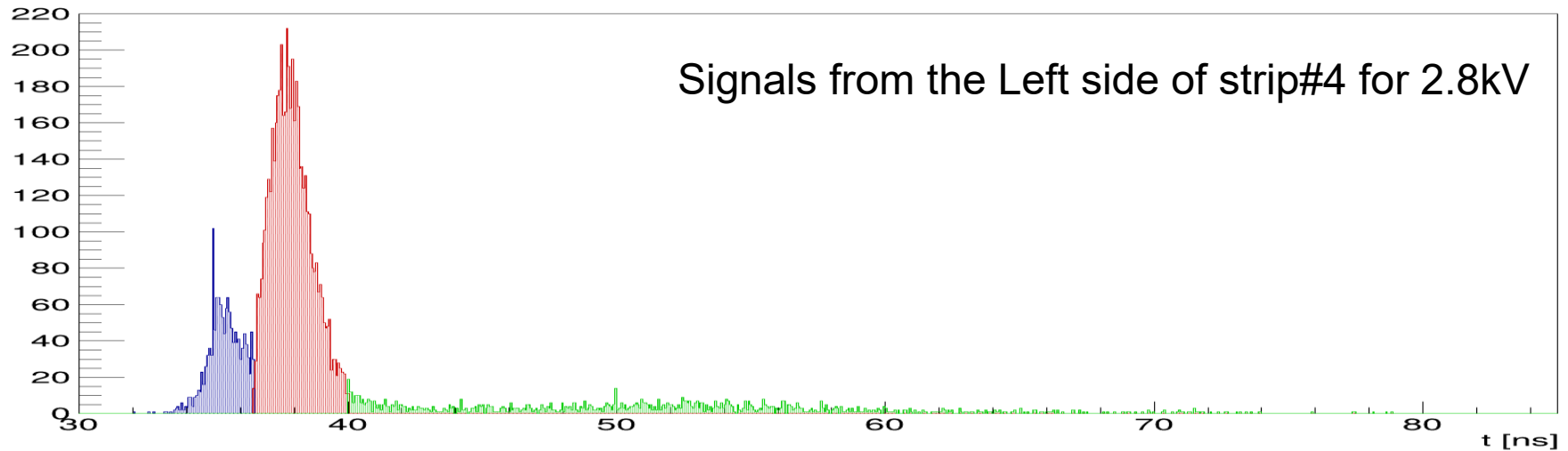
Schematic view of the experimental setup



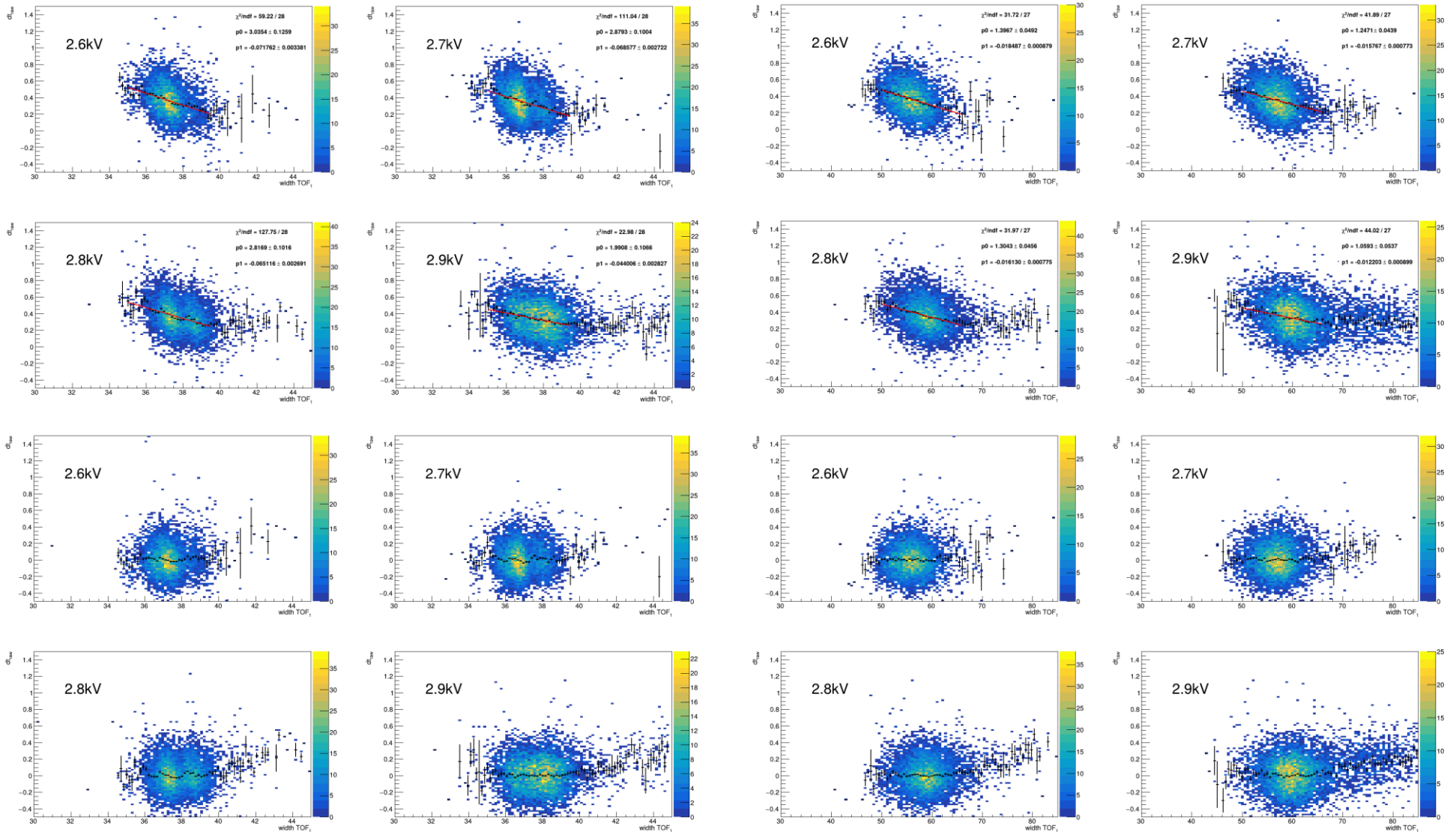
Width spectra for the fast and slow channels



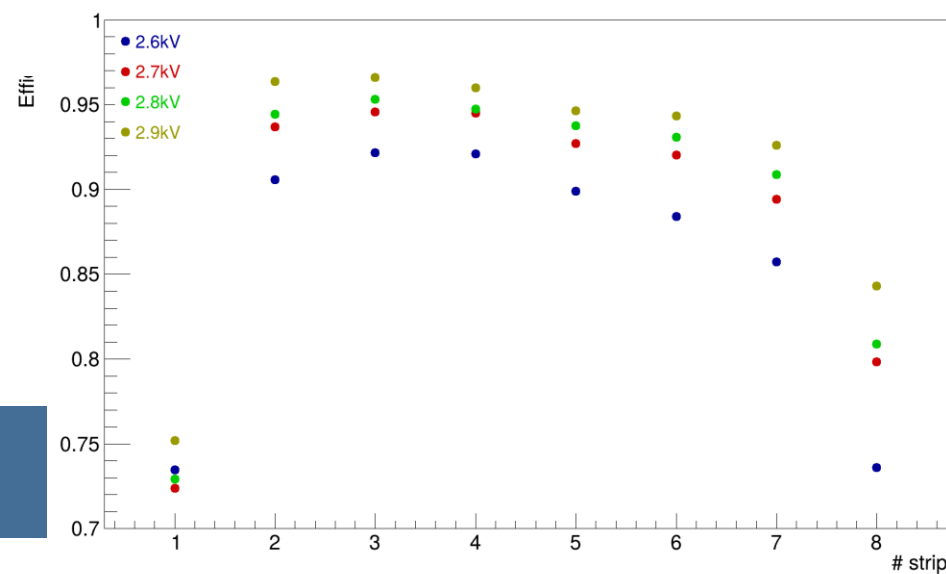
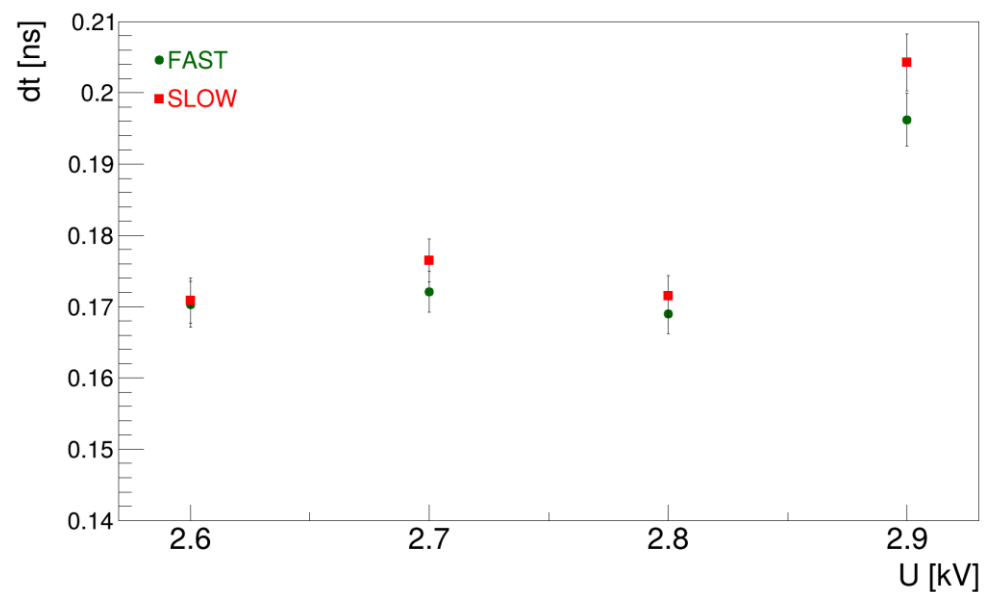
Timing cuts for signal redistribution in the fast channel



Walk through correction for Fast & Slow branches



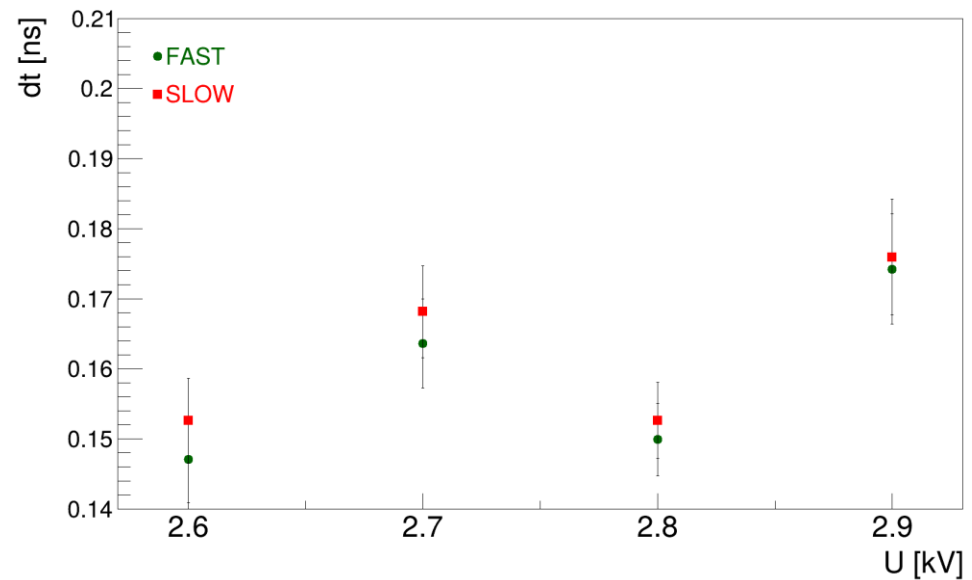
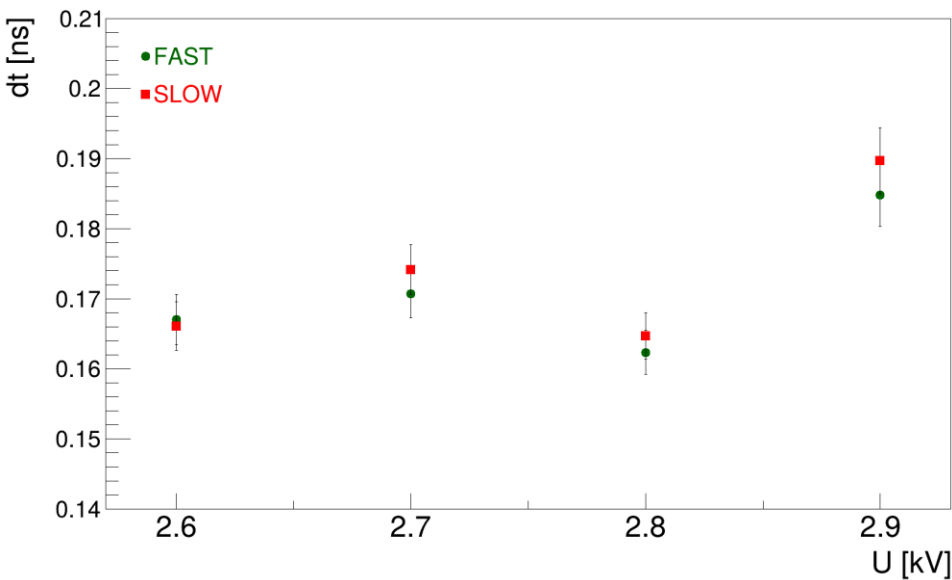
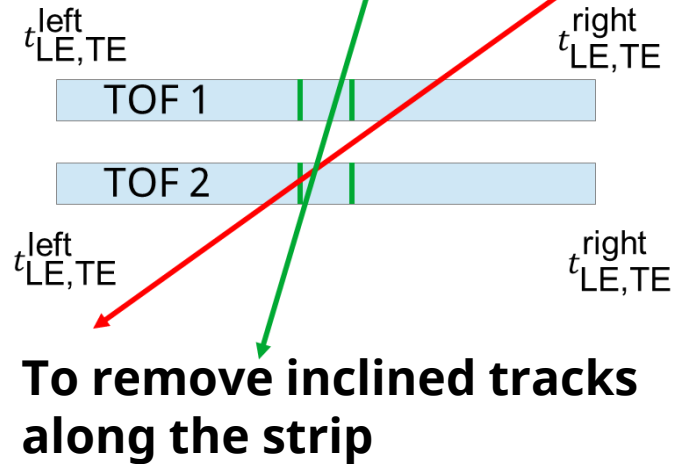
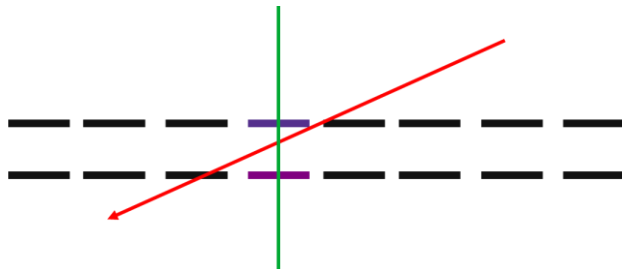
Time resolution after Walk through correction



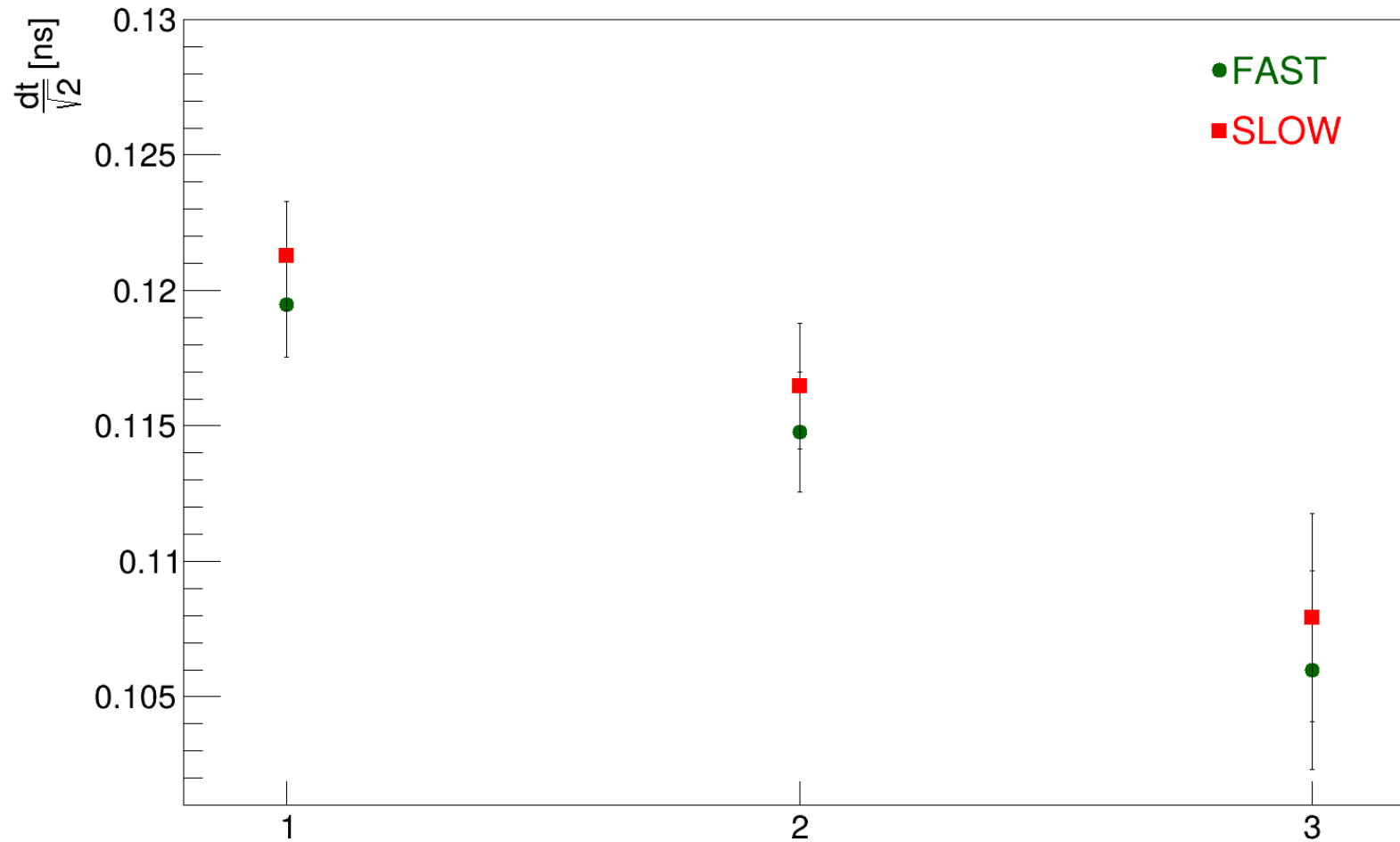
Detection efficiency

Track selection to improve the time resolution

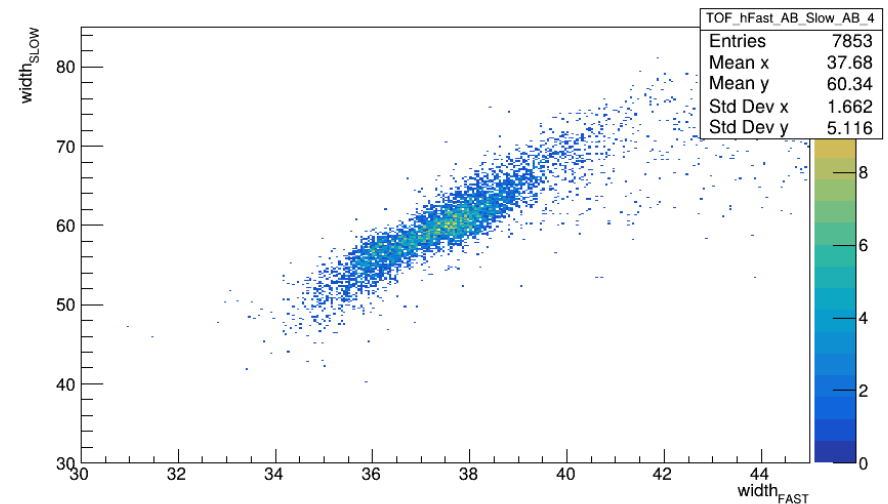
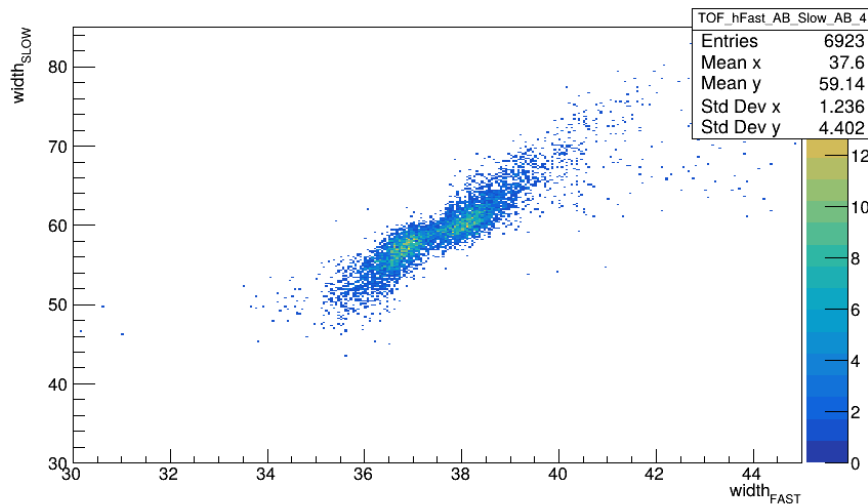
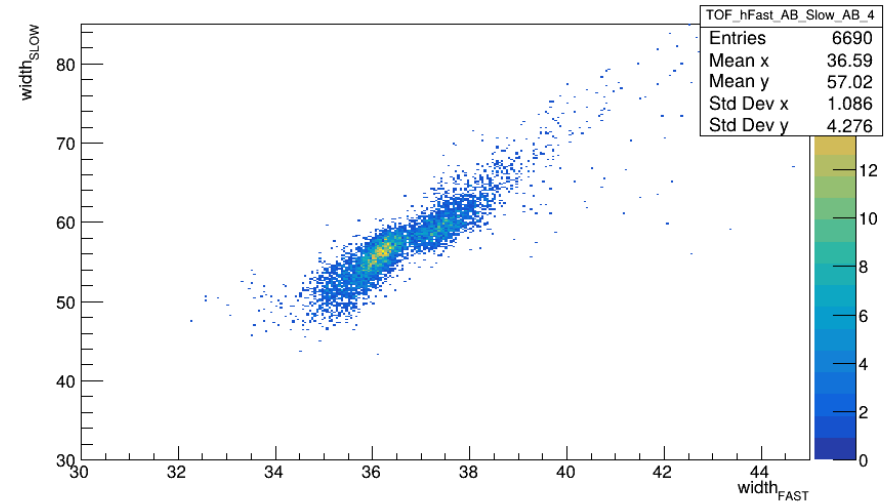
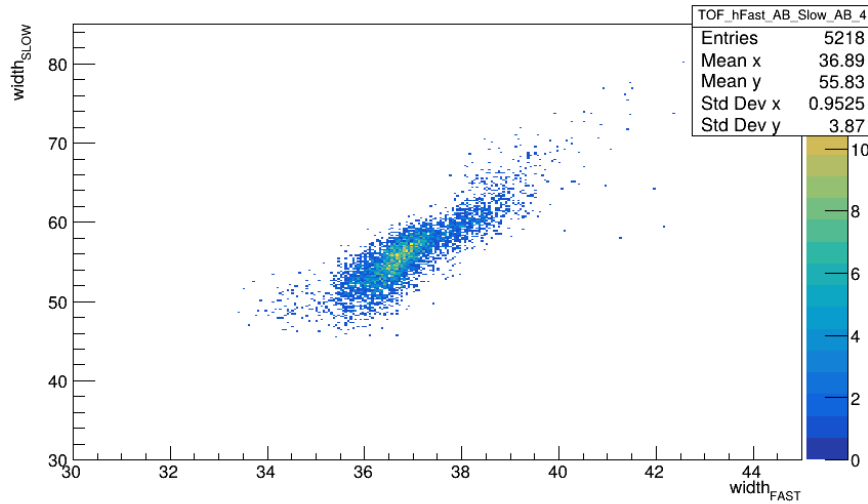
To remove inclined tracks



Time resolution after three correction steps at 2.8kV



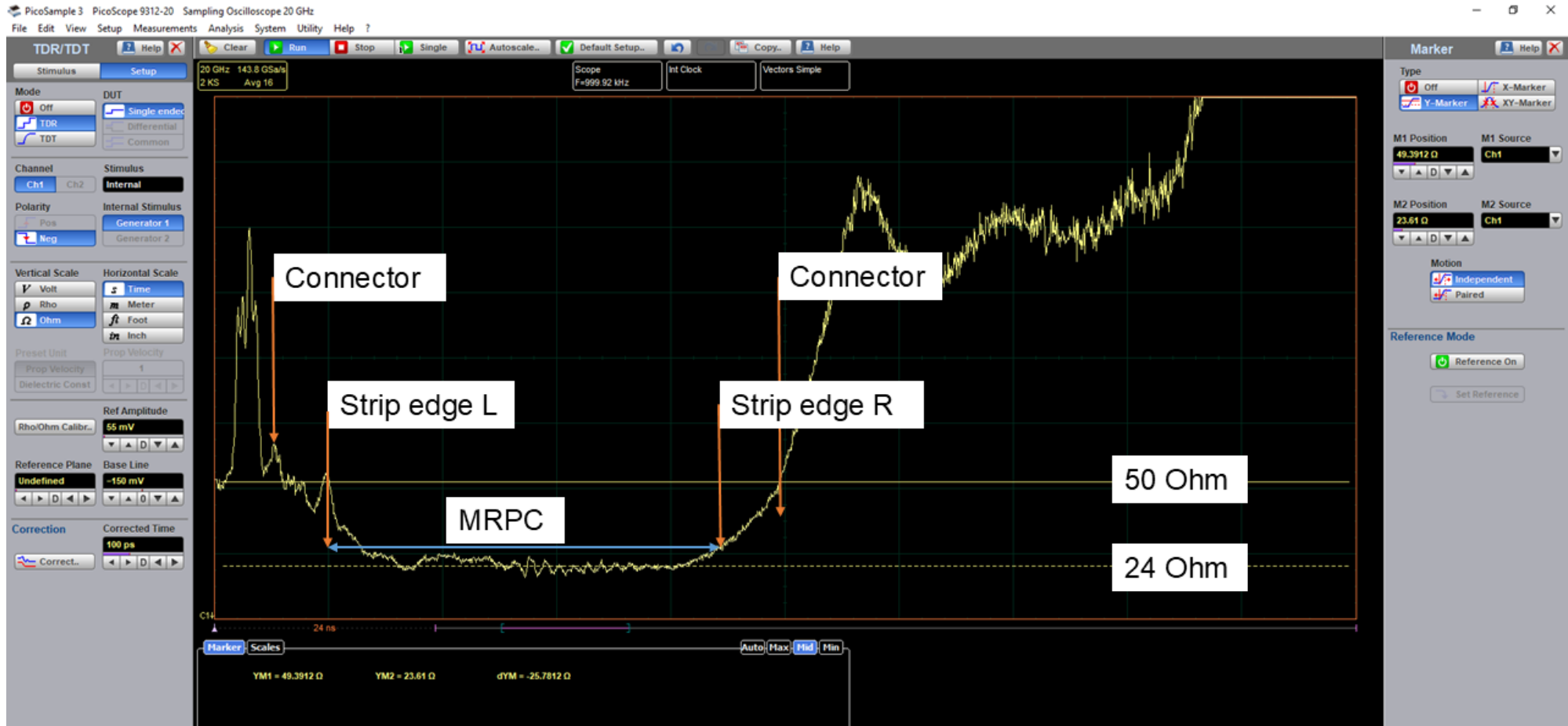
Slow vs. Fast: explaining absence of improvement



Impedance measurements for Protvino MRPC

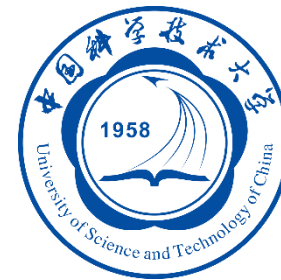


Unipolar readout mode

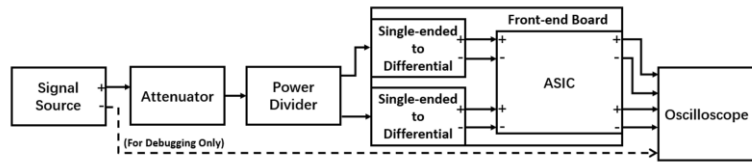


Status of **DISA** Differential current(I) Saturation **A**mplifier development

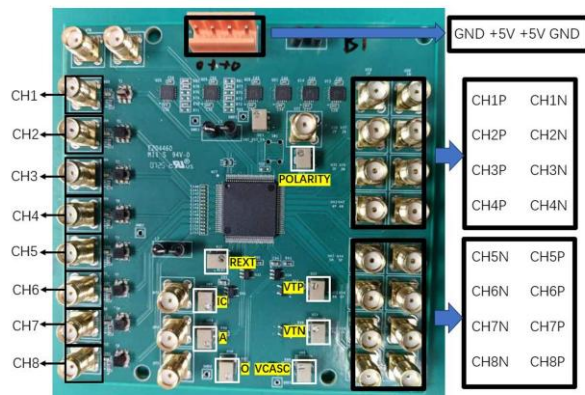
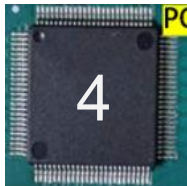
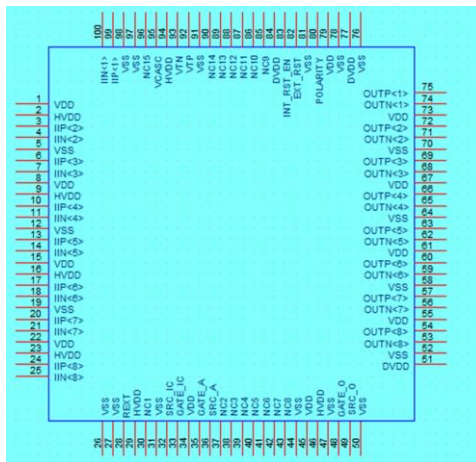
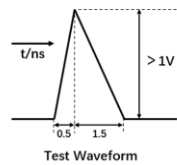
Valery Chmill



DISA evaluation Board description and test parameters

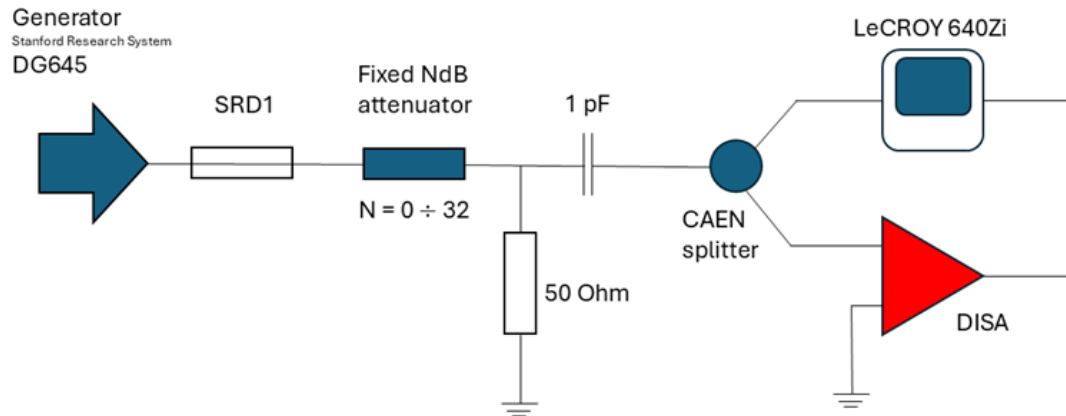


Test System Block Diagram



Bias Set	Recommend Value
REXT: External resistor for impedance matching	45Ω
VTP: Threshold Voltage at P Terminal (VTP is positive when polarity is 1, and negative otherwise)	0.697V
VTN: Threshold Voltage at N Terminal (VTP is negative when polarity is 1, and positive otherwise)	0.873V
VCASC: Input Stage MOSFET Common-Gate Voltage	1.352V
IC: Amplifier Stage Internal Current Compensation	0.806V
A: Internal Amplifier Circuit Current Setting	0.434V
O: LVDS Output Level Setting	1.092V
POLARITY: Signal Polarity Control, Set to "1" for Positive Signal on P Terminal(Output Pin), Set to "0" for Negative Signal on P Terminal. "0" Indicates High Level(1.8V).	1.8V (POLARITY=0)
Attention: Adjust VTP and VTN as needed. Note that too small differential voltage may cause noise-induced signal triggering.	Attention: The measurement of the recommended value is described in the illustration below.

Performance Characterization and Time Resolution Analysis



High-Performance Setup:

Pulse generator with <100 ps rise time.
LeCroy oscilloscope with 1.87 ps intrinsic jitter (4 GHz BW, 40 GS/s).

System Sensitivity:

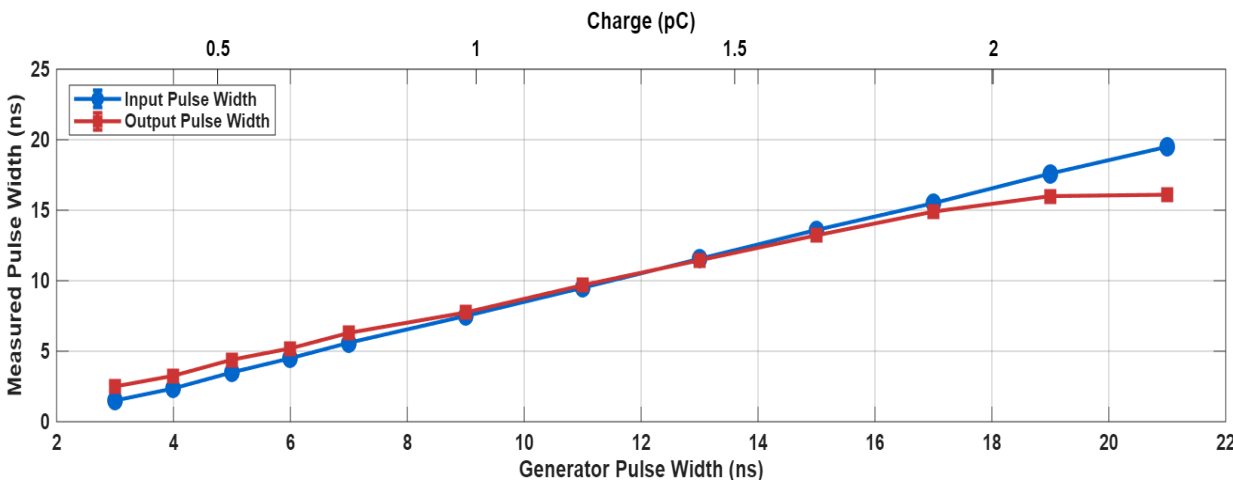
Minimum detectable charge: 6-8 fC
Stable operation confirmed down to 5.5 mV threshold.

Key Highlights:

System achieves picosecond-level timing resolution.

Linear response to injected meander shaped charge pulse

Jitter less than 5 ps on working range



DISA calibration test using a Delta function



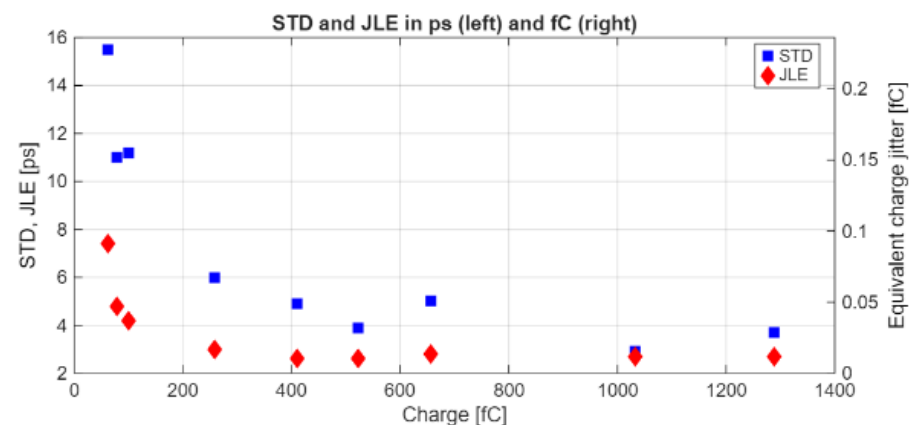
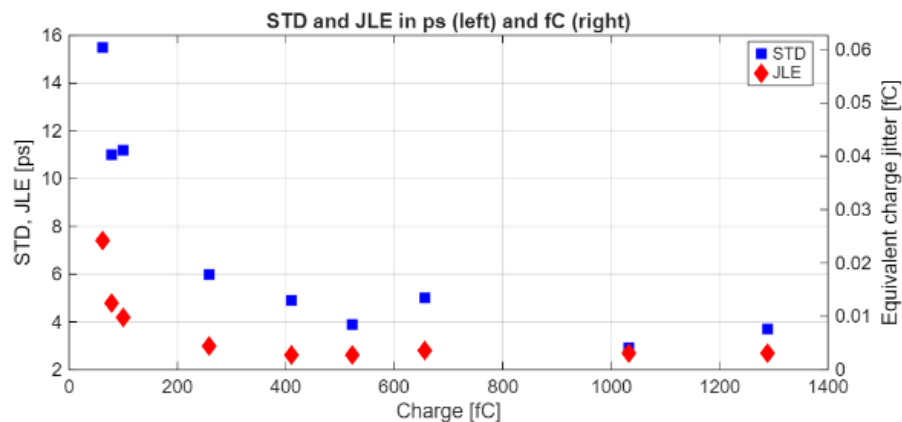
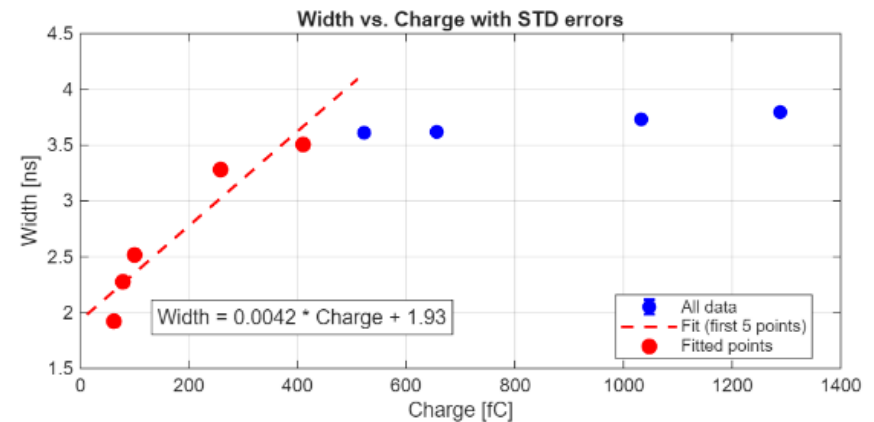
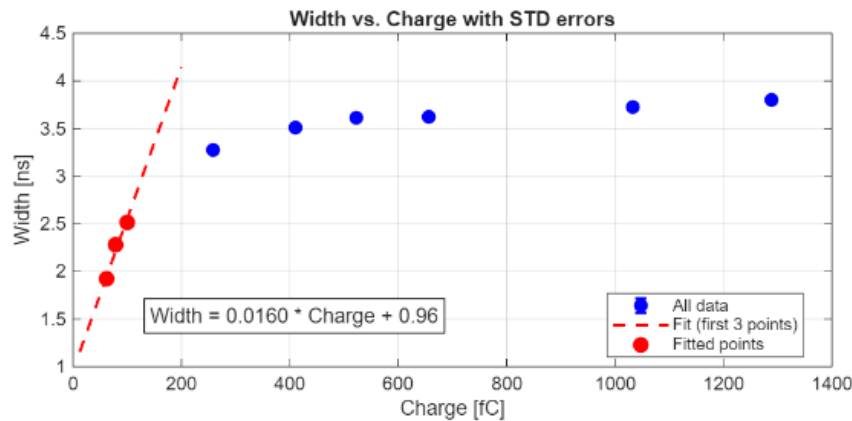
The conversion factor comes from the fit:

Width = A · Charge + b, where A is in **ns/fC**.

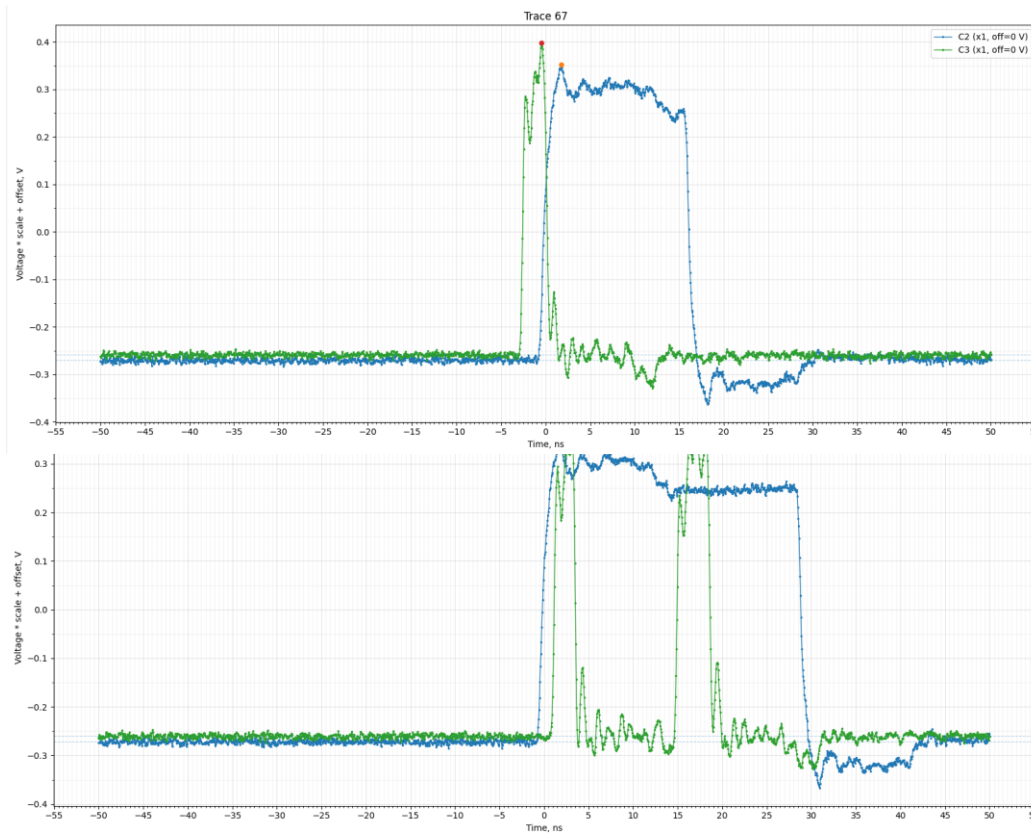
The derivative d(Charge)/d(Width) = 1/A (fC/ns).

To convert a time interval Δt in ps to an equivalent charge ΔQ in fC:

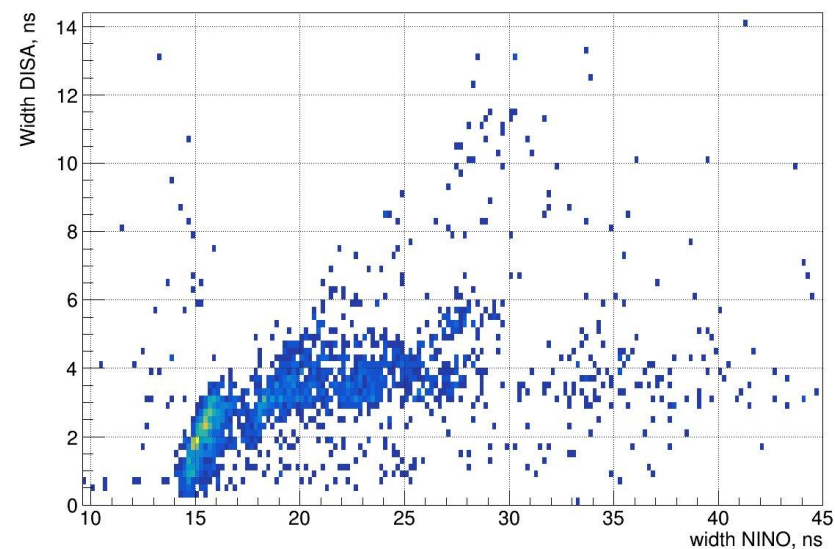
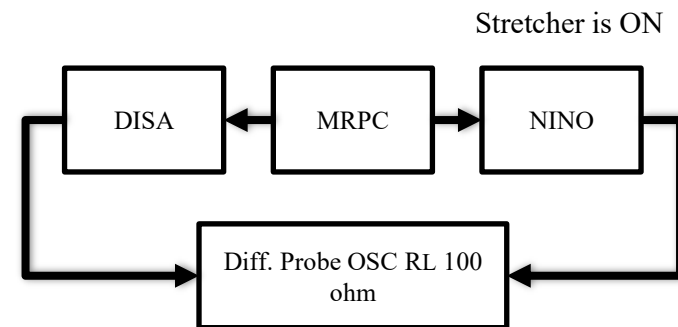
$$\Delta Q = \Delta t [ps] \times \frac{1}{A} [fC/ns] \times \frac{1 ns}{1000 ps} = \frac{\Delta t}{A \cdot 1000} [fC]$$



Comparison of DISA and NINO response to MRPC signals



Green – DISA, Blue – NINO



Pulse width distribution FEE for one same strip MRPC

To be continued (plans and dreams)



- Verification and testing of **DISAv2** functionality.
- MRPC readout using two **DISAv2**-based **FEE** cards, tested in cosmic-ray and muon-beam tests.
- Testing and modification of a stand-alone **FPGA-based** 32-channel **TDC** module.
- ***A Fully Functional MRPC Readout Module:*** *A compact, high-density, low-power PCB providing 32 channels of readout, integrating DISA ASICs and an FPGA-TDC optimized for the signal profile from MRPCs.*
- ***Strengthened Collaboration:*** *Establishment of a strong foundation for future joint projects in detector electronics for high-energy physics experiments between JINR and PRC institutions.*
- ***A Versatile Platform for Gaseous Detectors:*** *The developed system will serve as a key building block for future MRPC-based ToF systems in major experimental facilities.*

“The only way to do great work is to love what you do.” — Steve Jobs



- **Artem Ivanov, Mikhail Rumyantsev, Mikhail Buryakov**



- **Lei Zhao, Jiajun Qin, Dongdong Hu**



- **Sergei Morozov, Evgeni Usenko**



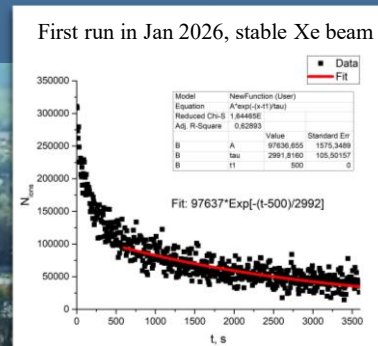
- **Andrei Snesev & Protvino team**

I'm proud to work with such amazing coworkers

Spare parts (slides)

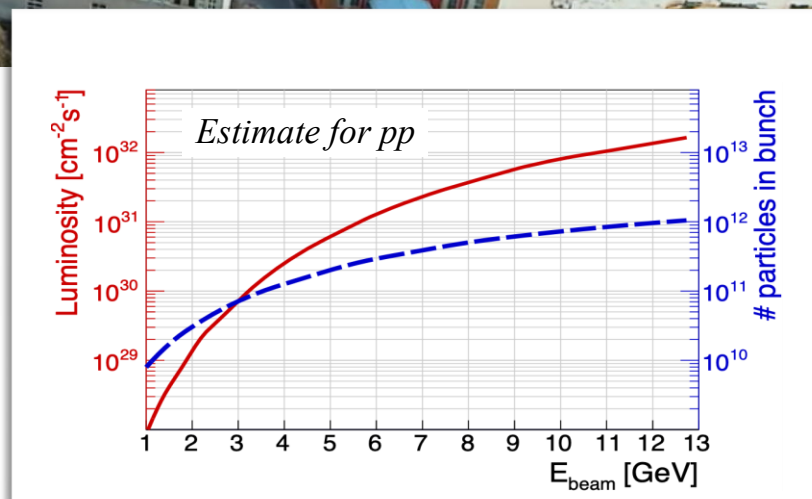


Accelerator complex **NICA** at JINR



SPD project

- SPD (Spin Physics Detector) is a universal facility with the primary goal to study *unpolarized and polarized gluon content of proton and deuteron*
- SPD project was approved in JINR and had its first proto-collaboration meeting in June 2019
- Conceptual Design Report (CDR) was released in January 2021, [arXiv:2102.00442]
- Official birthday of the SPD collaboration in June 2021
- Technical Design Report (TDR) of SPD was released in January 2023, NSR 1 (2024) 1, [arXiv:2404.08317], <http://spd.jinr.ru>



Status of RUNO development

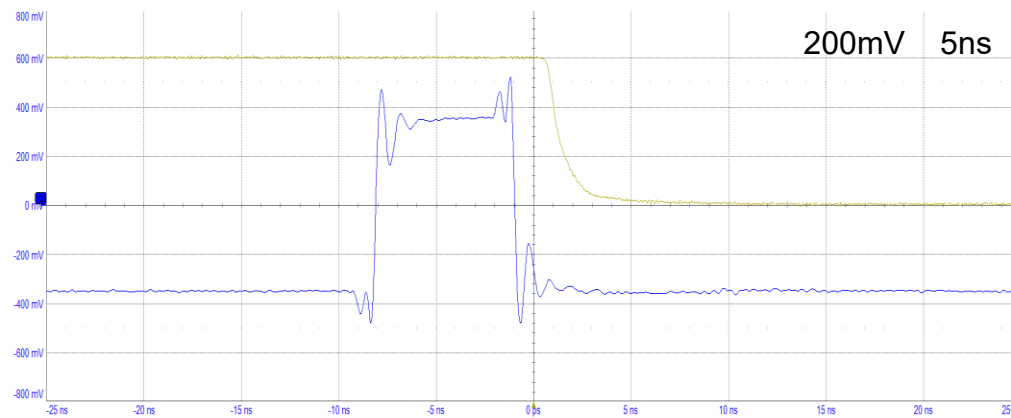
Valery Chmill



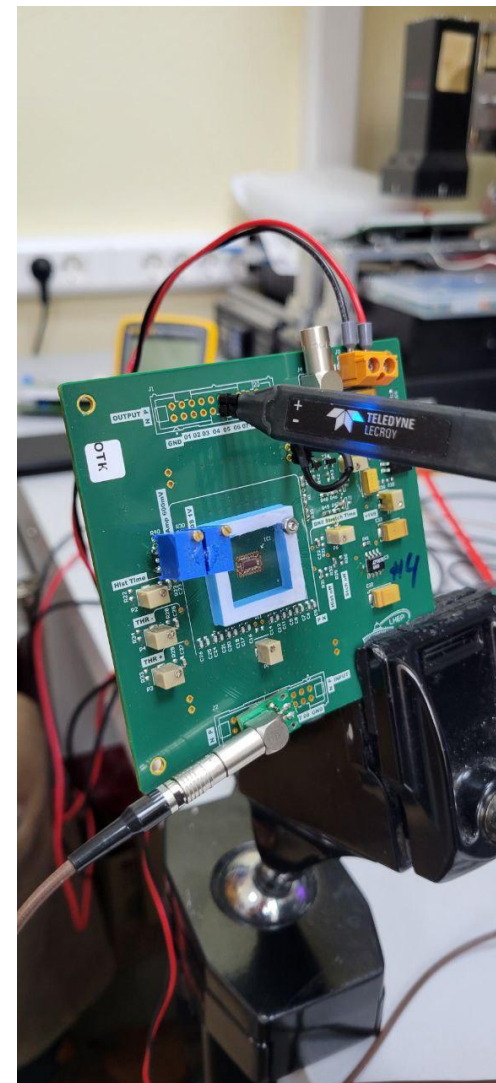
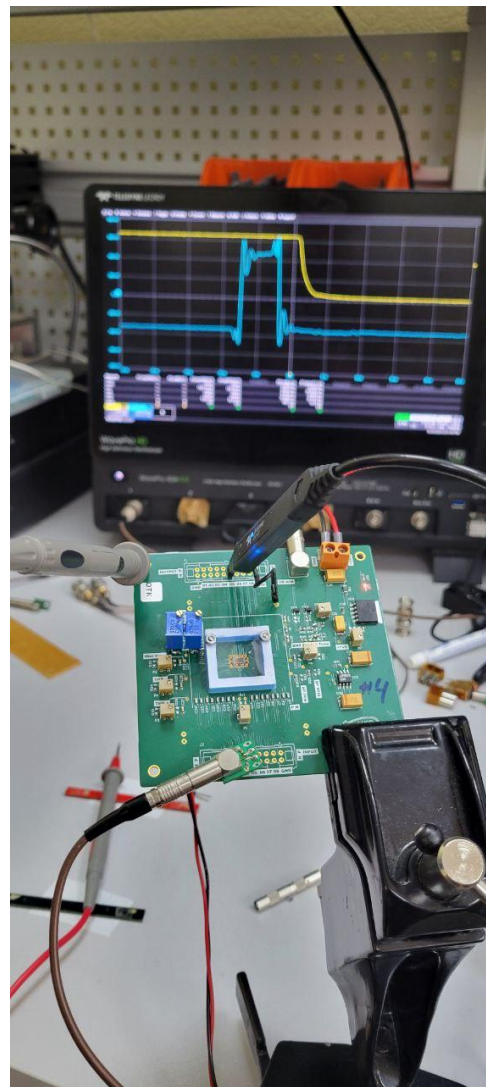
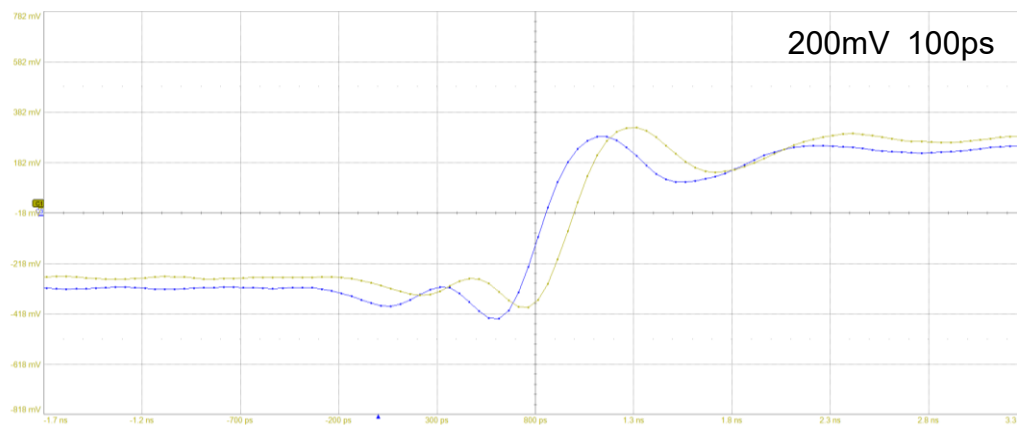
RUNO run#2 Chip ver#3

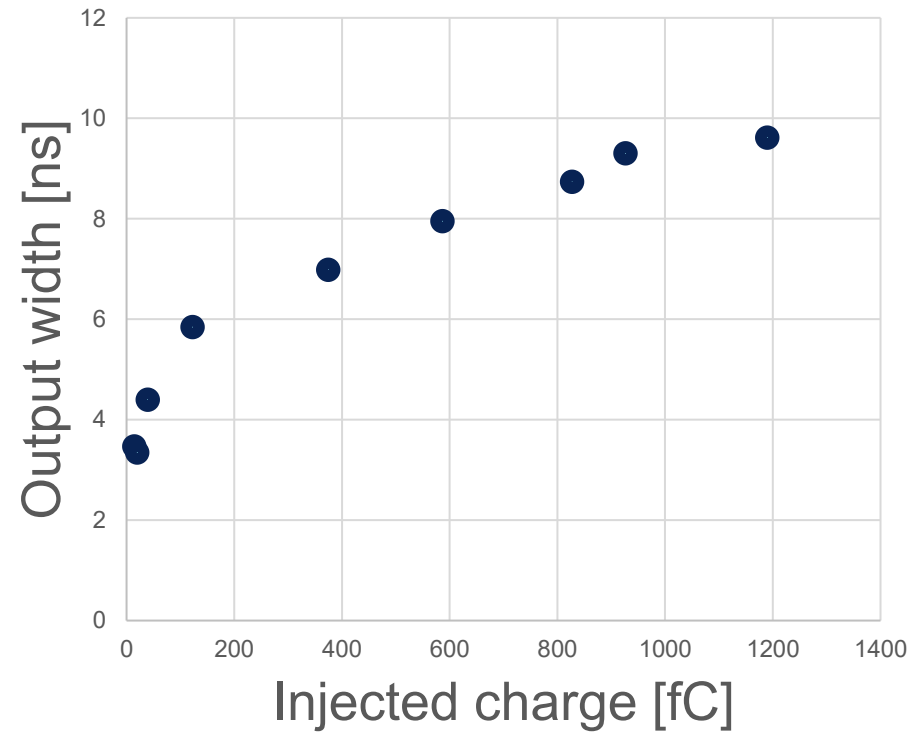
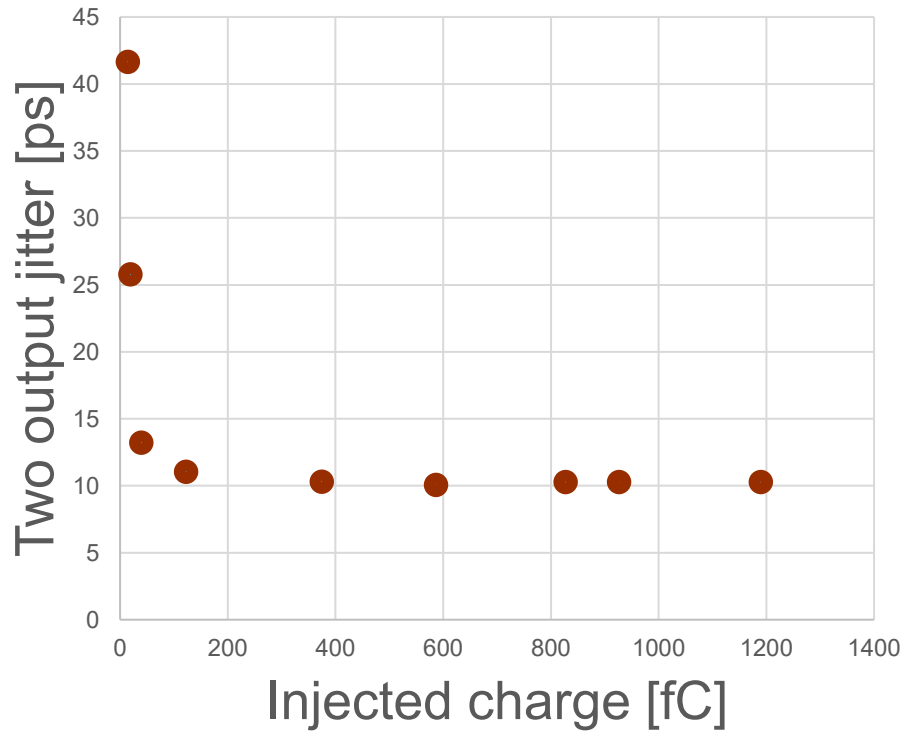


Minimum injected charge 15fC



Intrinsic jitter 10ps



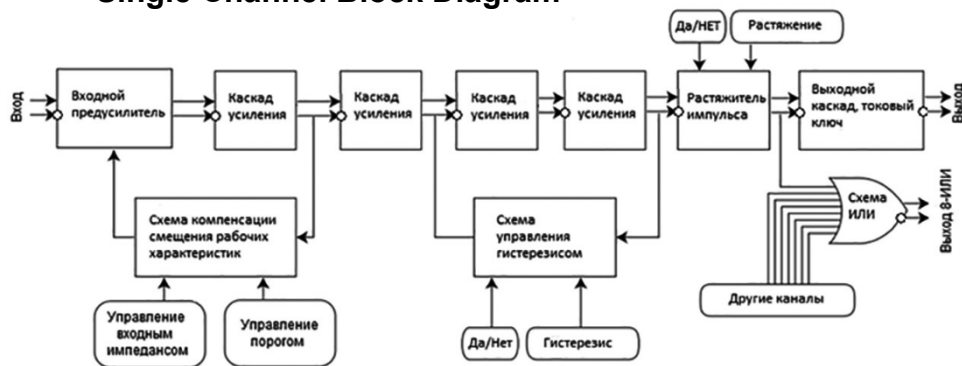


Input impedance is equal to 65Ohm, power consumption was: $1.8V \cdot (0.166A - 0.017A) / 8 = 33.5mW/ch.$

Technical proposal for RUNO run#3



Single Channel Block Diagram



ALEXANDRE SOLIN, ALIAKSANDR SOLIN, INSTITUTE FOR NUCLEAR PROBLEMS, MINSK

Objective and Purpose of the Work

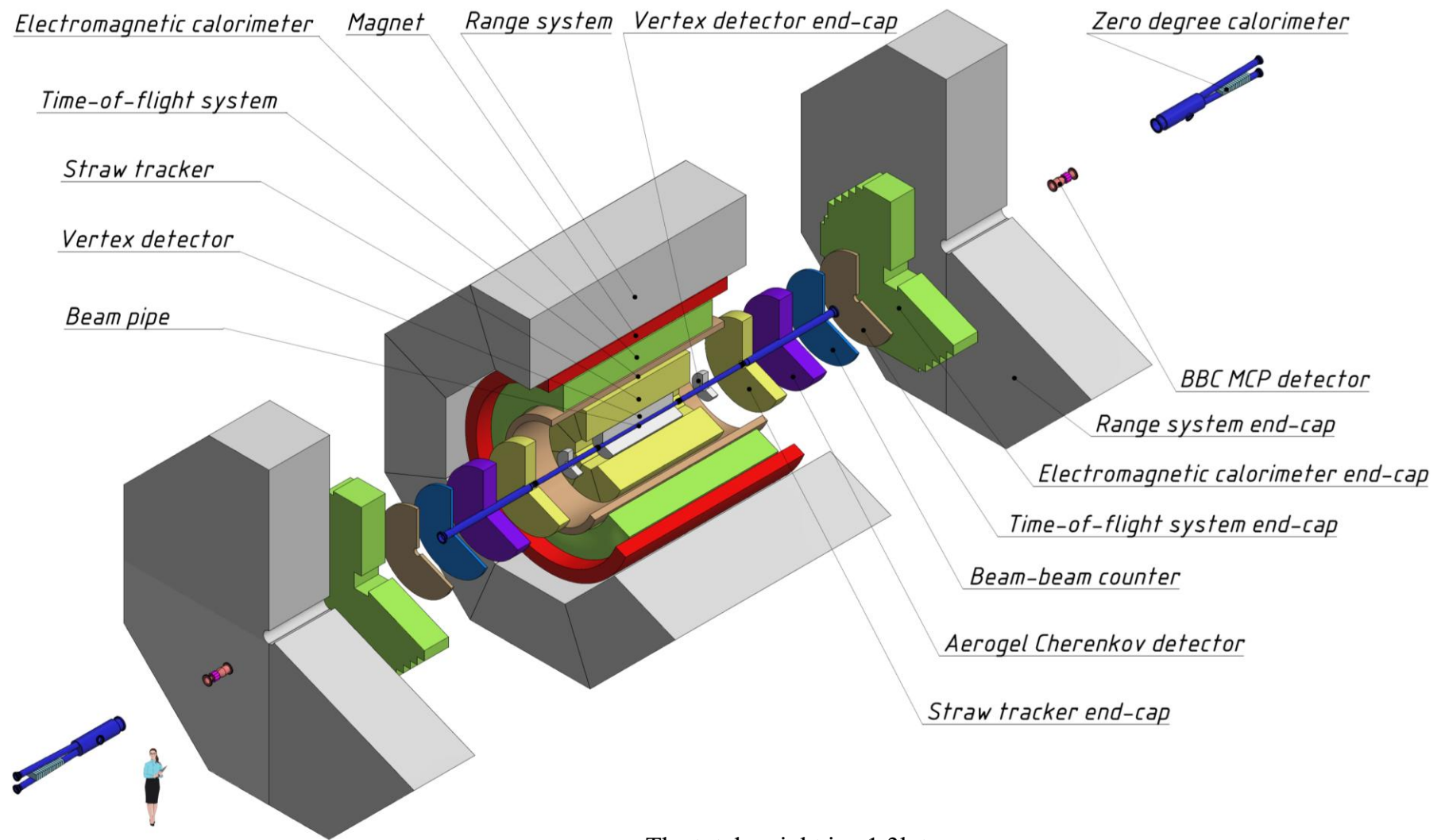
Development of the RUNOv1 IC prototype for the readout electronics of the RPC cameras of the NICA-SPD project.

Work Content:

1. Development of the IC's schematic diagram and topology.
2. IC simulation and post-simulation.
3. Preparation for transferring the IC's GDS file to the semi-conductor foundry.

Параметры детектора и линии передачи	
Емкость детектора, пФ	10
Максимальный сигнал, пК	1.5
Фронт сигнала, пс	<200
Сопротивление линии передачи, Ом	55
Две 110-омные параллельные линии	
Длина линии передачи, см	<20
Загрузка канала, МГц	<10
Параметры ИС	
Технология	CMOS
Проектные нормы, нм	180
Напряжение питания, В	1.8
Количество каналов	8
Рассеиваемая мощность, мВт/канал	<30
3-й приоритет	
Время формирования, нс	1
1-й приоритет	
Линейный динамический диапазон предусилителя, фК	0÷100
Коэффициент преобразования для заряда, мВ/фК	>1000
Напряжение смещения по входу (дифференциальное), мВ	<3
Шум (RMS), е 2-й приоритет	<2500
Гистерезис, В	0÷0.9
Порог дискриминатора, фК	10÷100
Внешняя установка	
Коэффициент преобразования для порога, мВ/фК	4÷5
Джиттер, ps При входном сигнале	<15
Time walk, пс	<50
Входное сопротивление (дифференциальное), Ом	55
Соответствует входному сопротивлению линии передачи	
Уровни выходных сигналов (дифференциальные)	LVDS
Задаются внешними элементами	
Диапазон выходных токов, мА	1÷6
Диапазон растяжения импульса, нс	0÷100
Типовая длительность импульса, нс	15
Разброс длительности импульса, %	<15
Кросс-ток между каналами, дБ	-50

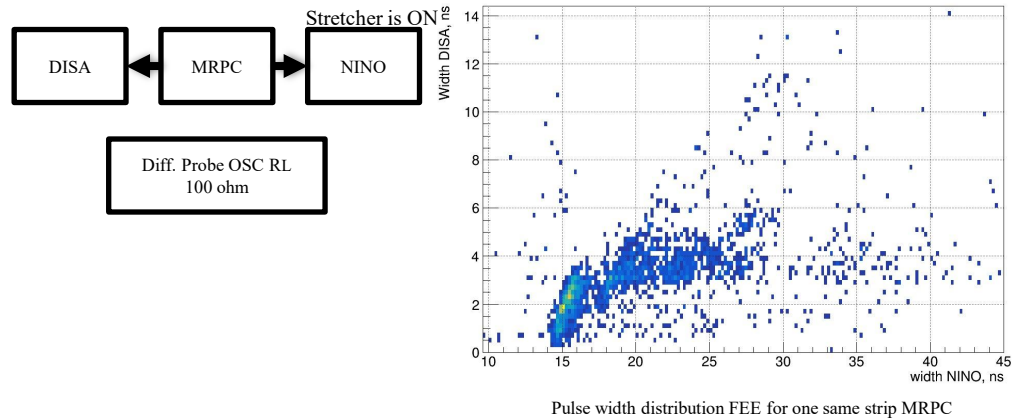
Schematic view of the SPD setup



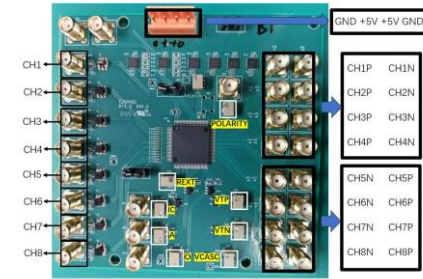
The total weight is ~1.3k tons

Time-of-flight (TOF) system

DISA to NINO comparison



DISA evaluation board



DISA calibration and jitters

$$\Delta Q = \Delta t [ps] \times \frac{1}{A} [fC/ns] \times \frac{1 ns}{1000 ps} = \frac{\Delta t}{A \cdot 1000} [fC]$$

Impedance measurement for Protvino MRPC

