

MAPS sensor using 55nm HV-CMOS for tracking systems of LHCb upgrade and future Higgs factory

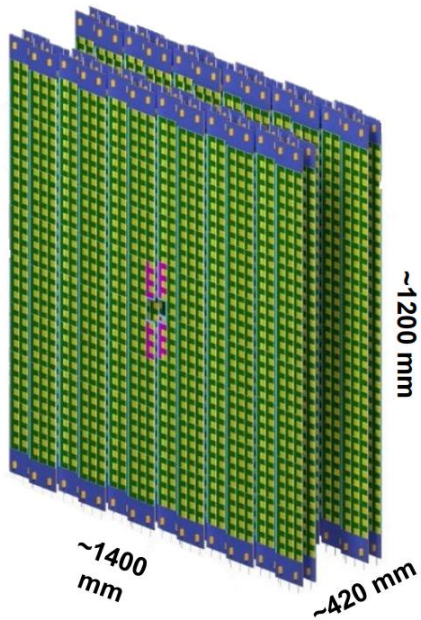


CMOS SENSOR IN
FIFTY-FIVE NM PROCESS

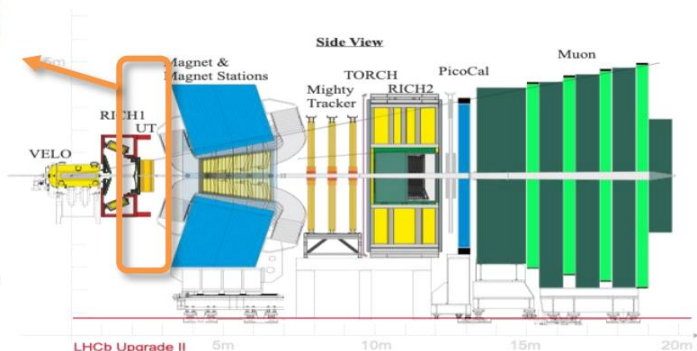
徐子骏 Zijun Xu (IHEP, CAS)
on behalf of COFFEE collaboration
INSTR, 2026-Oct-12, Hefei

Tracking detectors

- LHCb Upgrade Tracker @ Upgrade II
- Inner Tracker of CEPC Reference detector / AGORA concept for FCCee

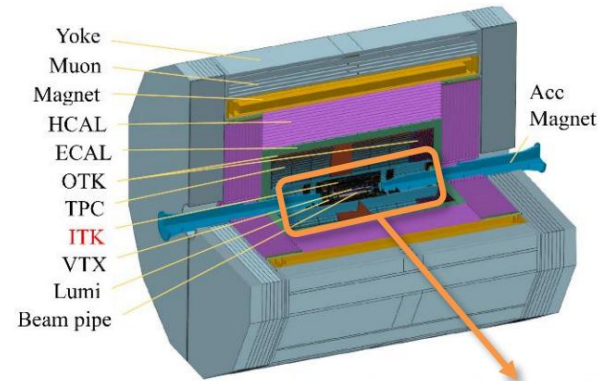


LHCb Upgrade II
 $1.0 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$



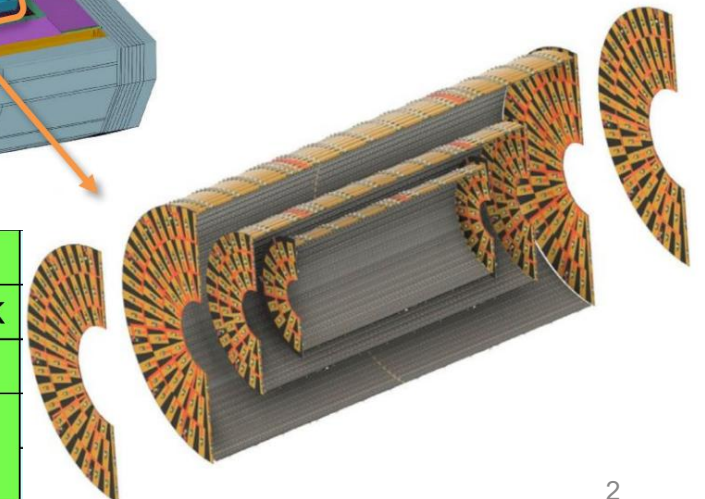
[LHCb Upgrade2 frame-TDR](#)

Key parameter	Requirement
Sensor size	2 cm x 2 cm
Spatial resolution	< 10 μm
Time resolution	3~5 ns
NIEL	$3 \times 10^{15} \text{ n}_{\text{eq}}/\text{cm}^2$
Max hit rate	80 MHz/cm ²
Power consumption	< 200 mW/cm ²



CEPC Ref-Detector
 / AGORA concept

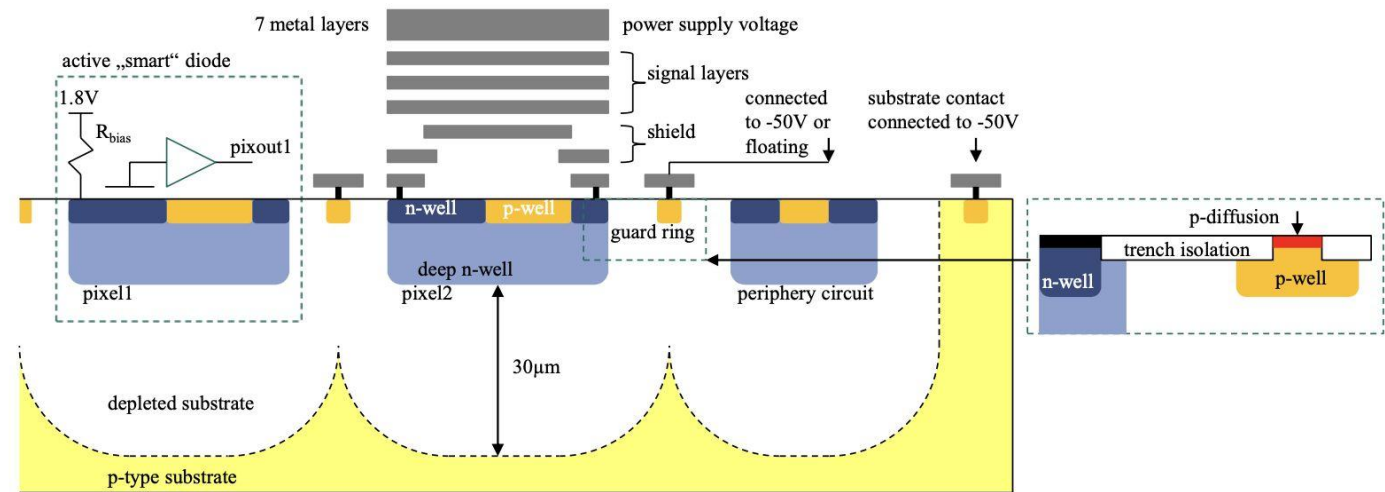
Vertex	CMOS + Stitching
Tracker	CMOS Si Pixel ITK
	Pixelated TPC
	AC-LGAD OTK



[arXiv:2510.05260](#)

HV-CMOS for Monolithic Active Pixel Sensors

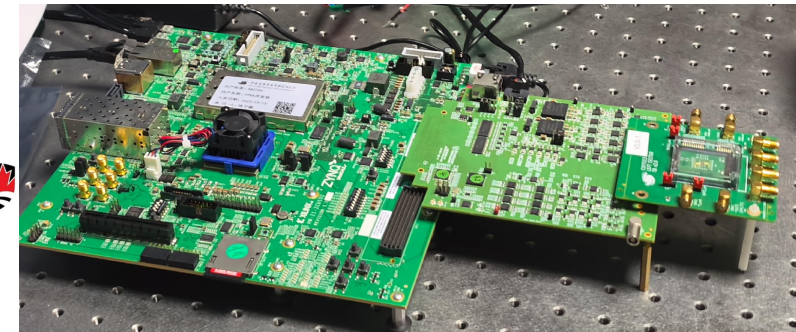
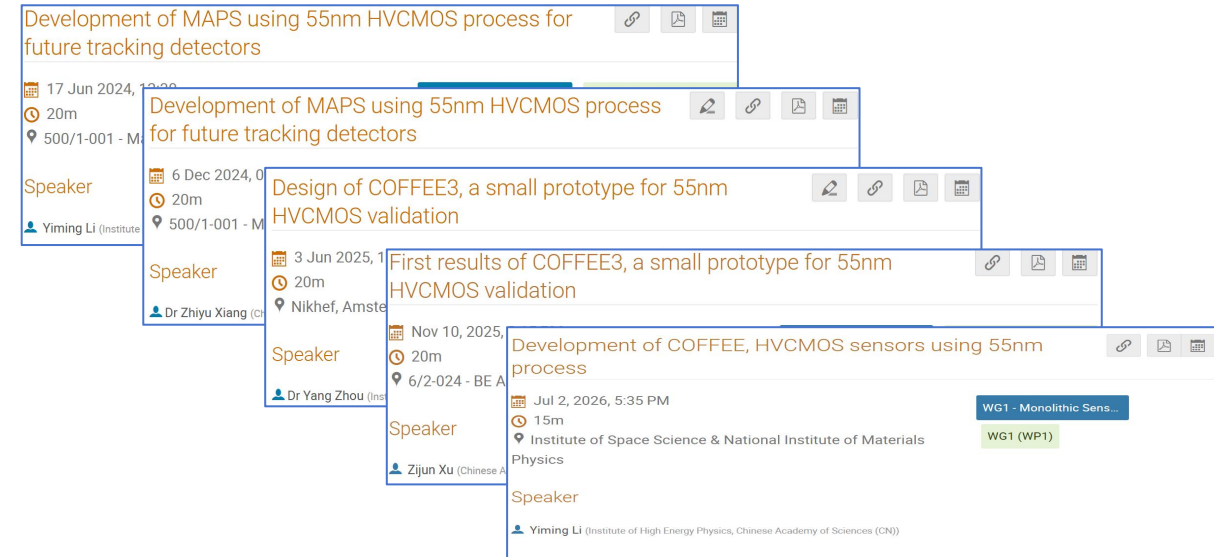
- **full depletion** possible due to large electrode
- intrinsically **radiation hard**
- **fast** charge collection
- **cost-effective**: based on commercially available process
- relatively larger capacitance noise, power



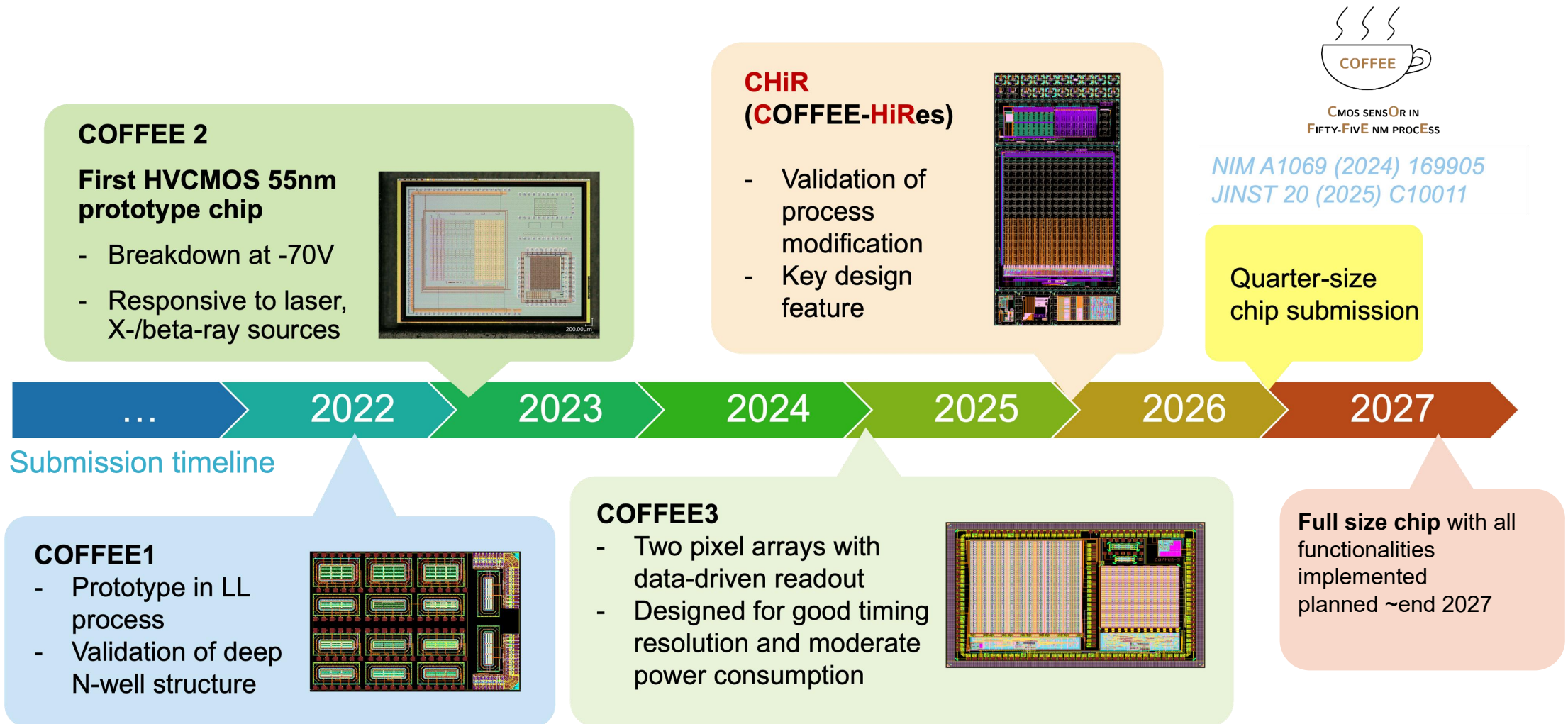
- ATLASPix3 as example, [link](#)

HV-CMOS MAPS R&D at IHEP

- IHEP actively involved in CERN DRD3
 - test-beam and irradiation facilities sharing
 - joint serial powering R&D with US/UK/Italy
 - joint aluminum flex R&D with Italy/UK
- Caribou DAQ for MAPS R&D
 - open source hardware/firmware/software
 - FE chip specific carrier board, firmware and software IP blocks by ourself
 - as a user, keep reporting bugs and solutions



CMOS sensOr in Fifty-FivE nm procEss (COFFEE)



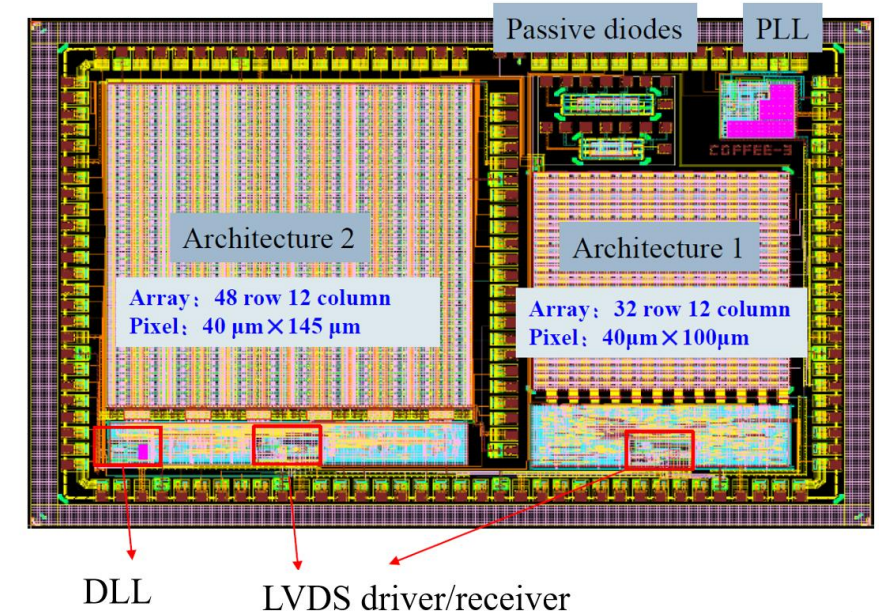
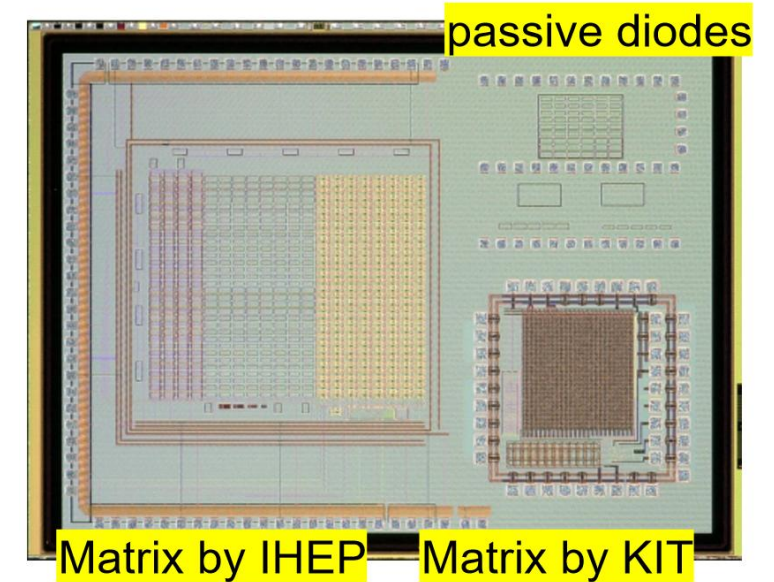
COFFEE Layout

- COFFEE2

- Passive diode for sensor characterizing
- the big pixel matrix design leaded by IHEP team
- R&D for pixel electrode structure, in-pixel Amplifier and comparator

- COFFEE3

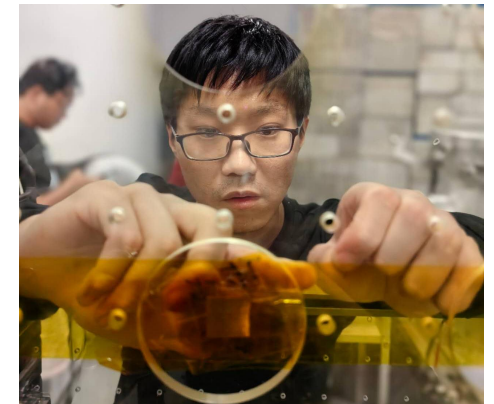
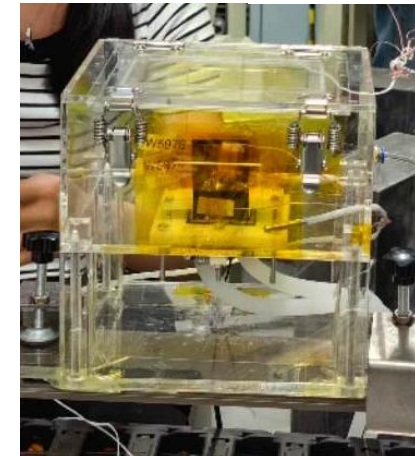
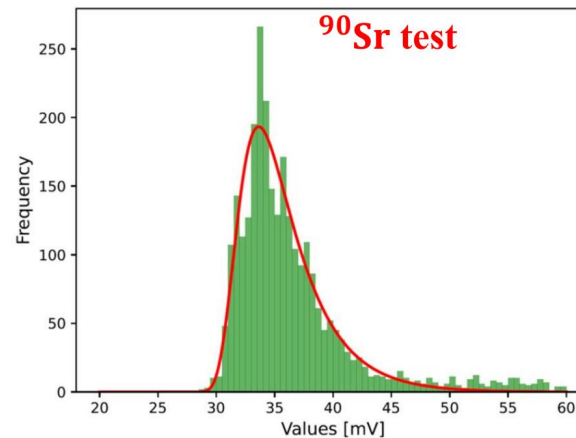
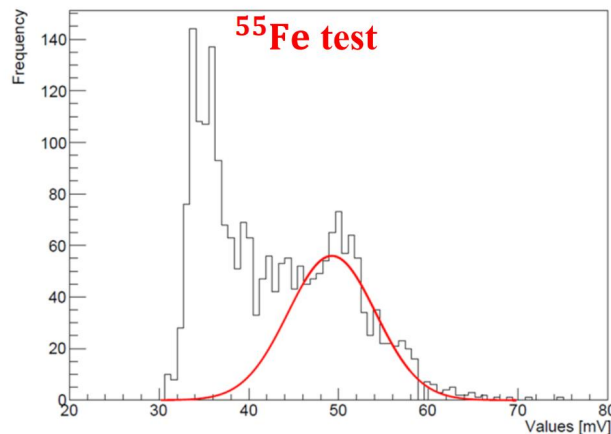
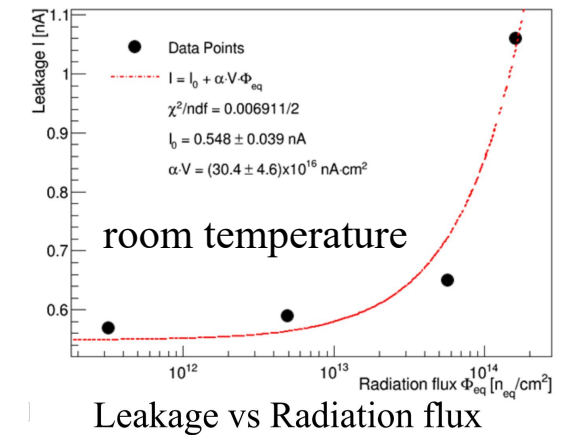
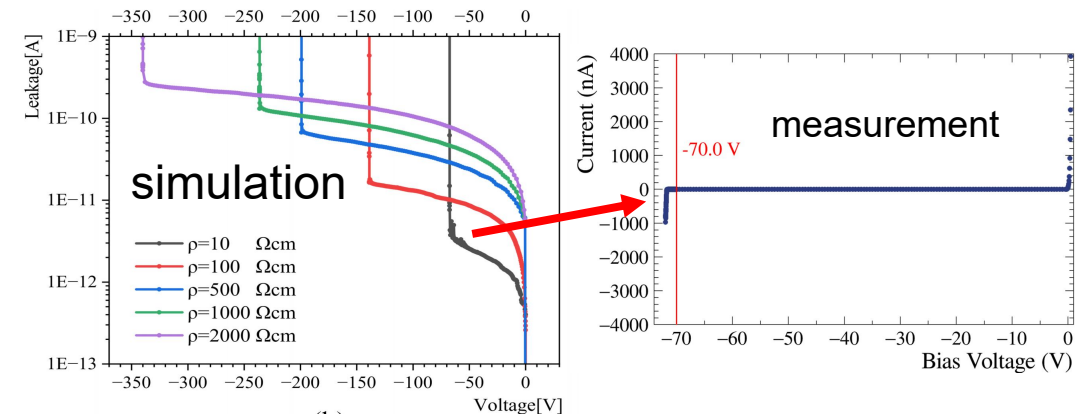
- PLL, DLL, LVDS IP accumulation
- Two pixel matrix & readout architectures:
 1. NMOS design in-pixel: for current triple-well process; Less X-talk between analog and digital circuits
 2. CMOS design in-pixel, for future quadruple-well process. Advanced readout design, more suitable for high hit density environment



MPW chip size $\sim 3 \times 4 \text{ mm}^2$

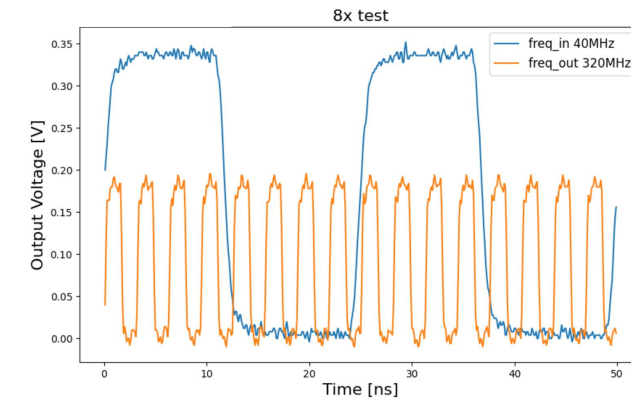
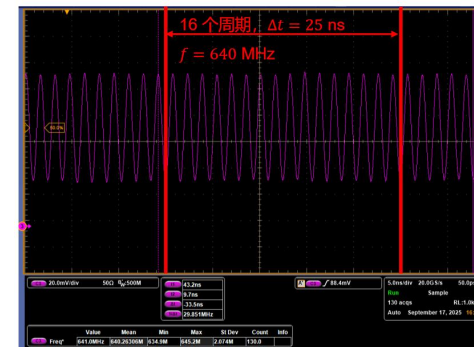
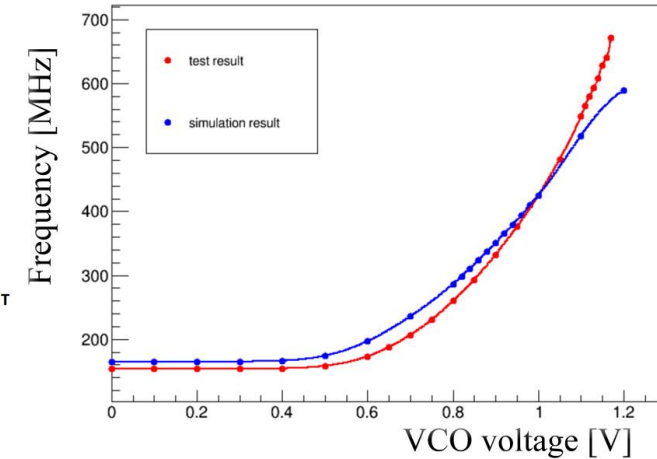
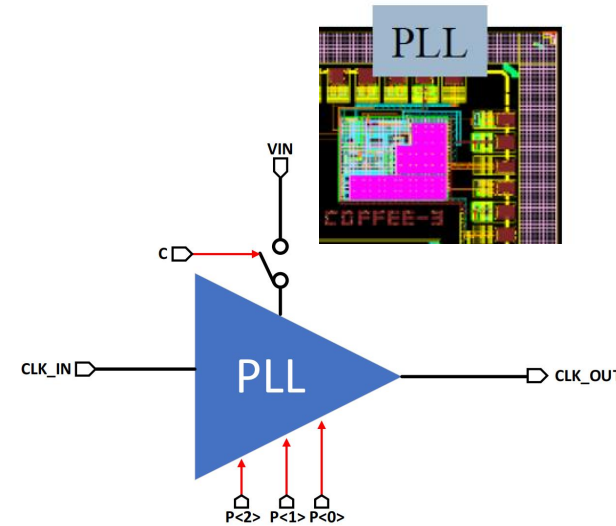
Sensor (charge sensing diode)

- COFFEE2/3 got consistent sensor IV/CV performance
 - consistent with TCAD simulation
 - $V(\text{Breakdown}) \sim 70\text{V}$ for $10\ \Omega\cdot\text{cm}$ resistivity wafer
 - irradiation @CSNS, APEP: 80MeV proton
- sensor depletion depth only $\sim 10\ \mu\text{m}$ from simulation, and inferred from radiation source (^{55}Fe vs ^{90}Sr) study of COFFEE2
 - high resistivity wafer will increase break-down voltage
 $\Rightarrow$ increase depletion zone, reducing capacitance noise



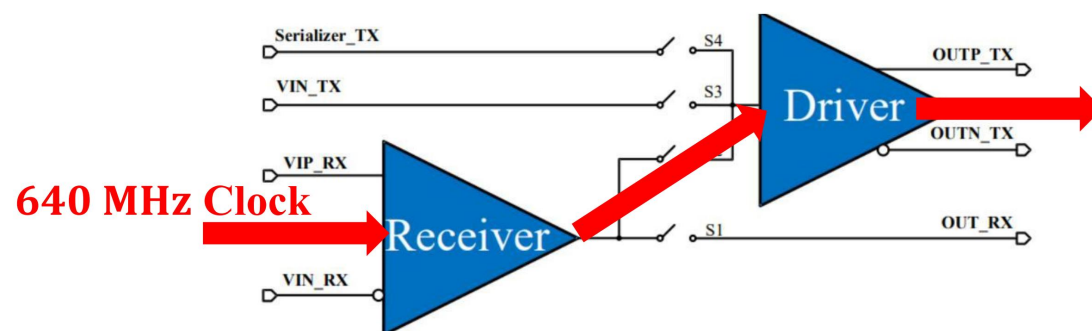
COFFEE3 PLL IP

- synchronizing the clock between FE chips and back-end DAQ
- converting input low-speed CLK to internal high-speed clock to support TDC and data transmission
- VCO control and frequency multiplication (x4, 8, 16) function works up to ~660 MHz
 - jitter noticed at highest speed, will improve in the next version
- working from room temp. to -50C

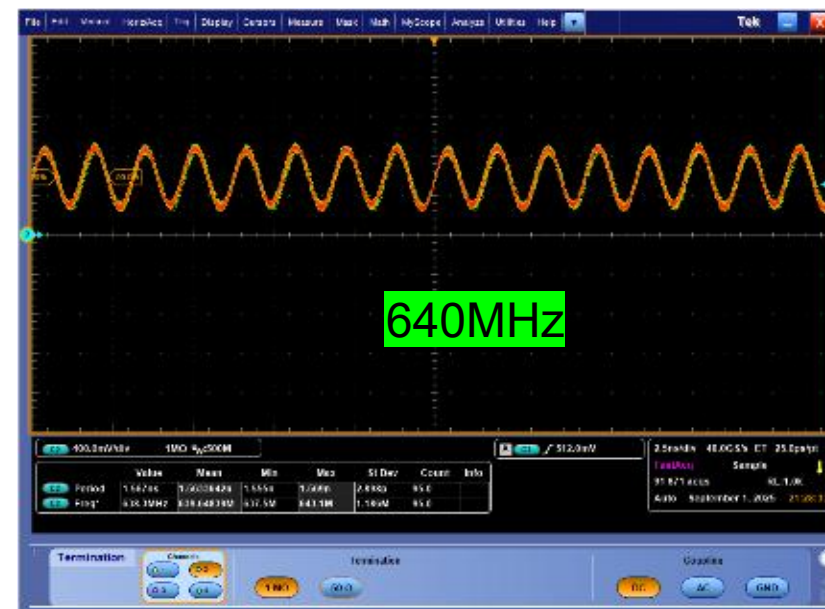
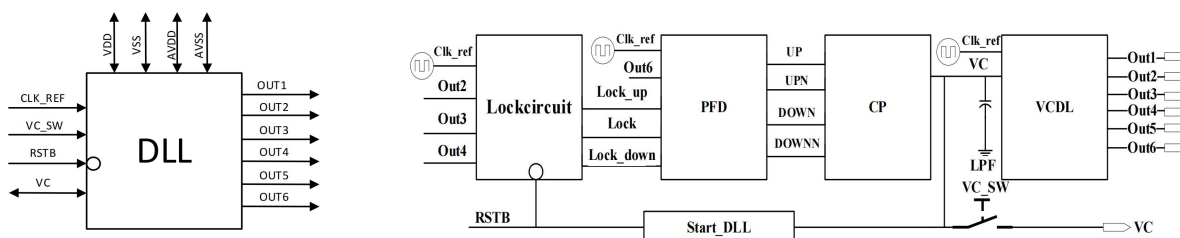


COFFEE3 LVDS and DLL IP

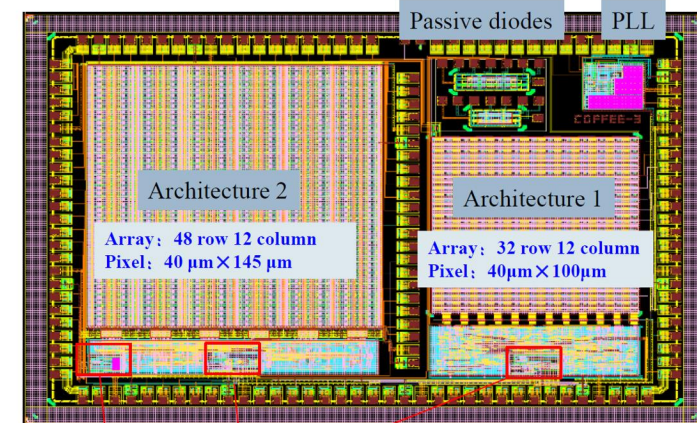
- LVDS transceiver Tx/Rx works up to 640 MHz CLK
 - high speed data transmission test in preparing (1.28 Gbps PRBS for example)



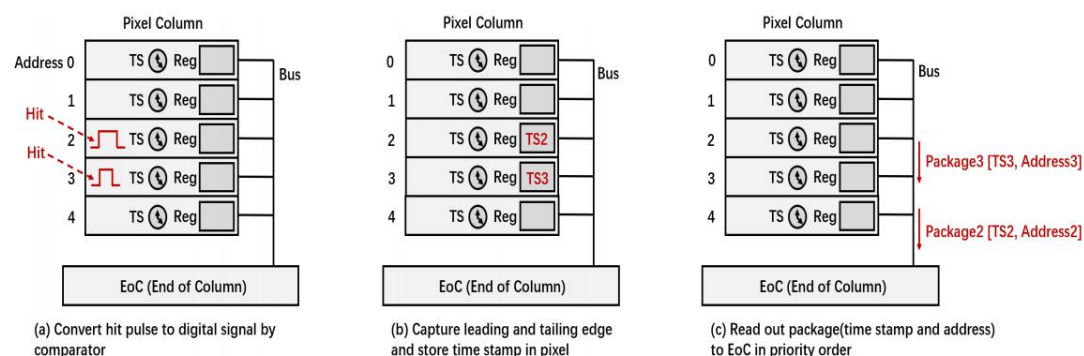
- Delay Locked Loop (DLL) delivers clock phase shifted as expected, for finer LSB of in-pixel TDC



COFFEE3 Readout Architectures



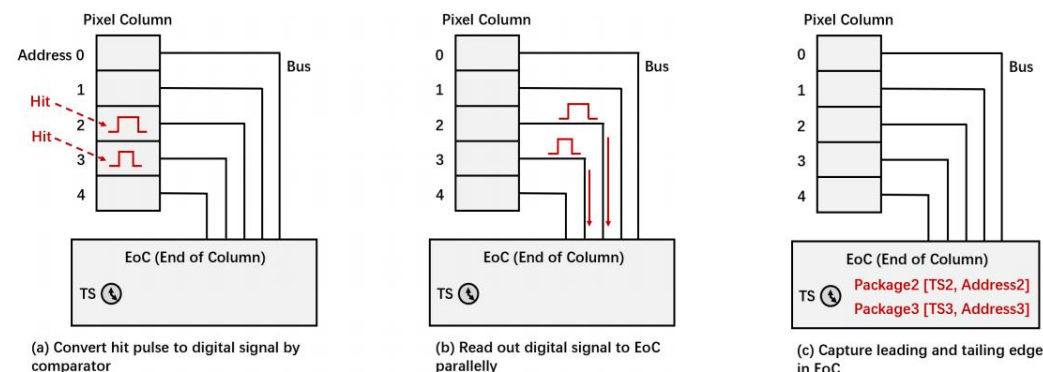
Architecture 2: employs a TDC within each pixel. Particle hit information (arrival time, end time) is recorded locally in each pixel and then read out to the bottom of the array in priority order.



Readout concept of Architecture 2, similar with Timepix, RadPix, MonoPix, etc.

- *More possibilities & High hit density processing capability*

Architecture 1: In-pixel NMOS design, after digitization, each pixel data is transmitted in parallel to the bottom of the array, where time stamps are added.



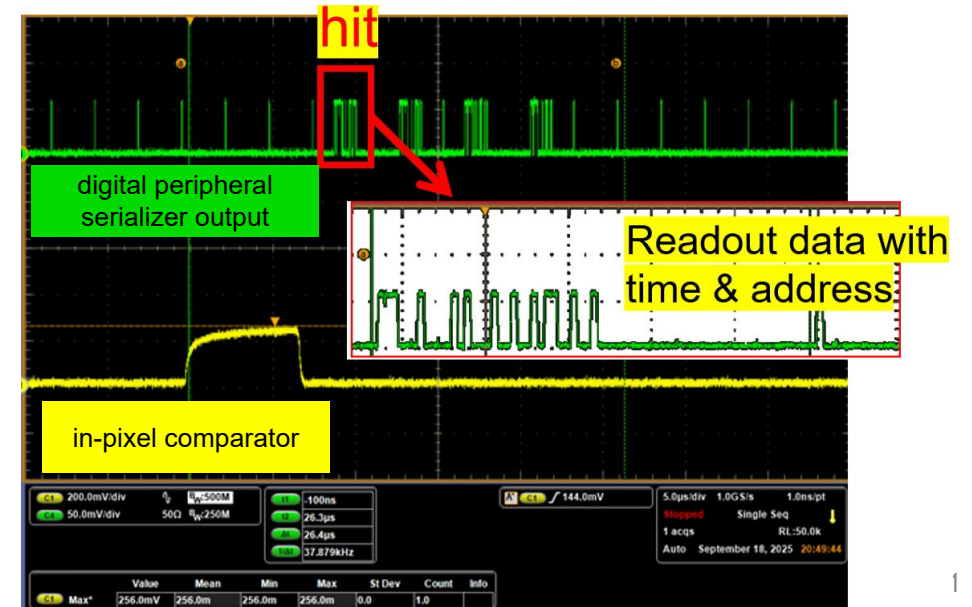
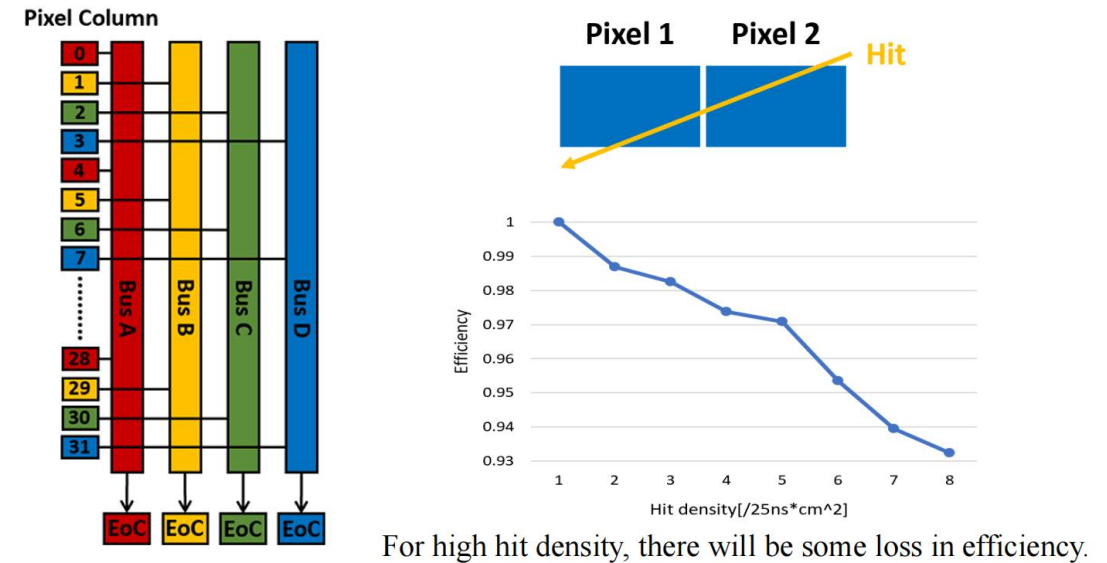
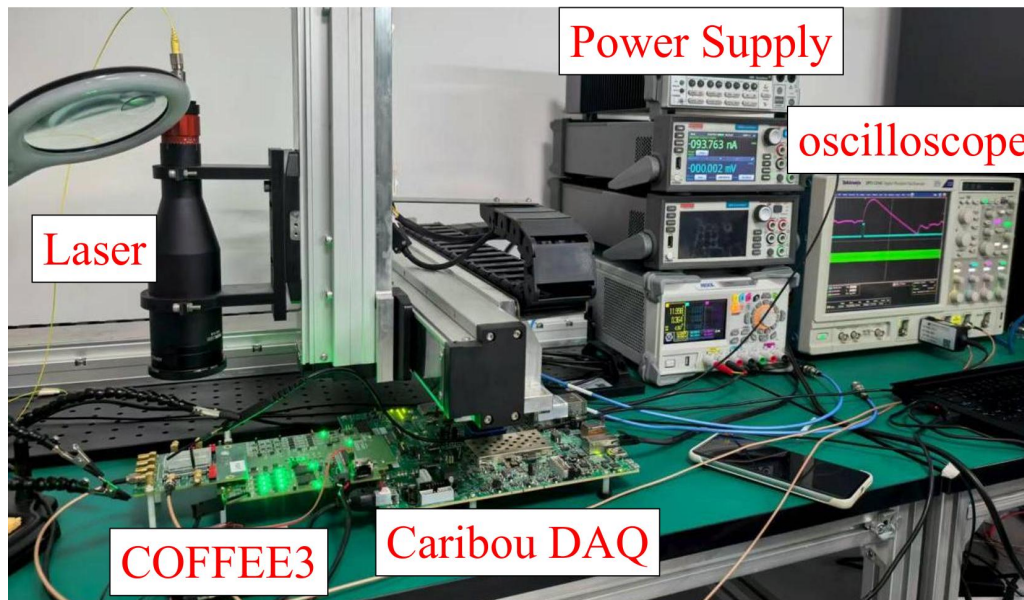
Readout concept of Architecture 1, similar with ATLASPix, MightyPix, MuPix, etc

Targets:

- *Potential for Low power consumption and high position accuracy*

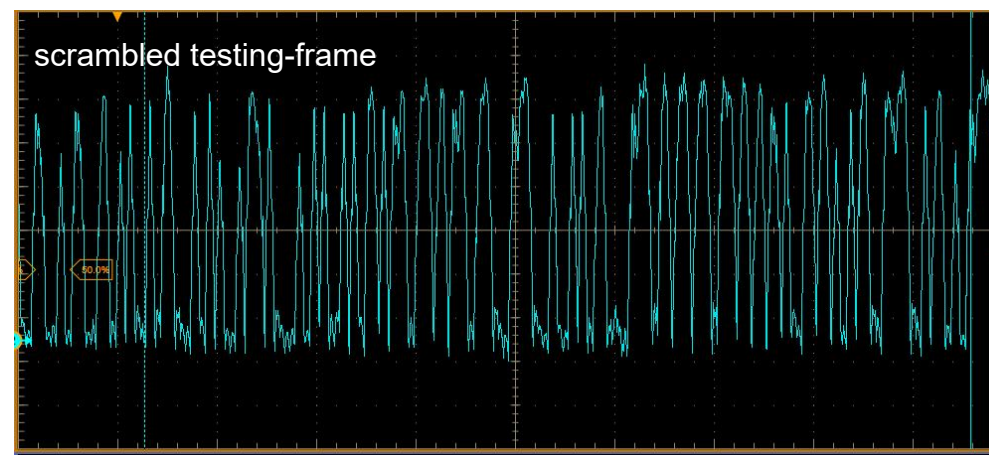
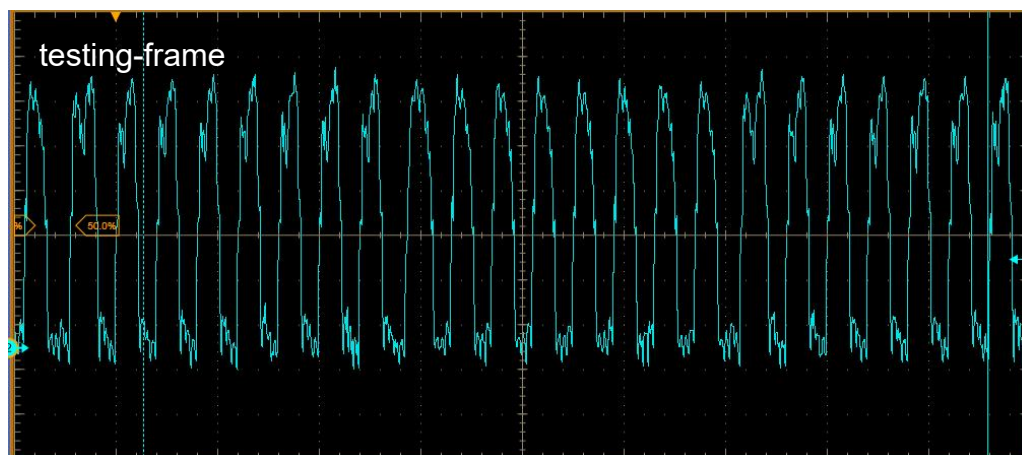
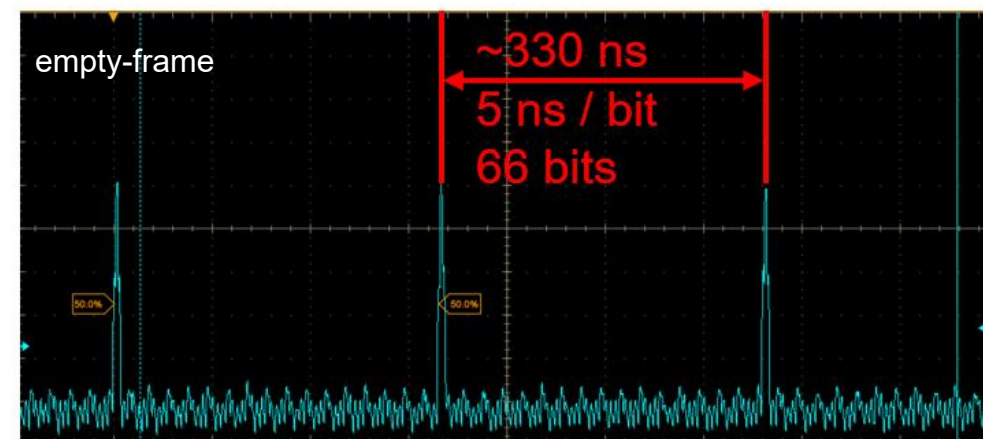
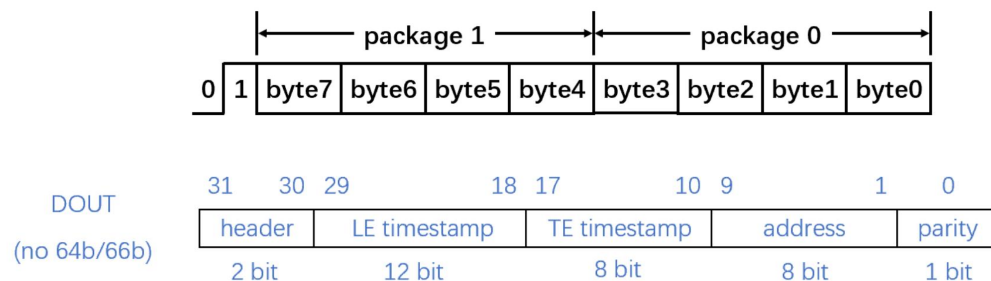
COFFEE3 Pixel-matrix-1

- in-pixel circuit + digital peripheral responding to global charge injection and laser injection
 - digital readout schemes optimized for high hit density
- *irradiation study in progress



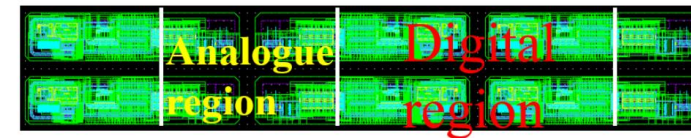
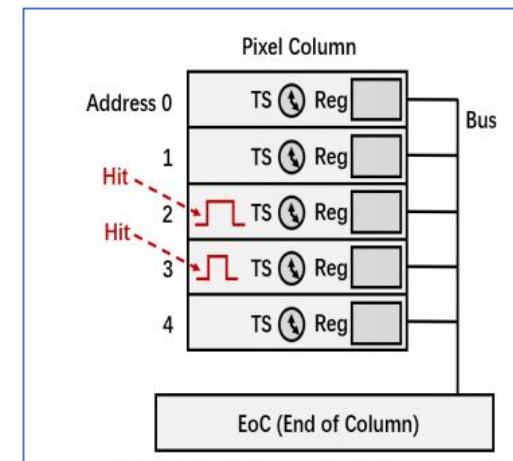
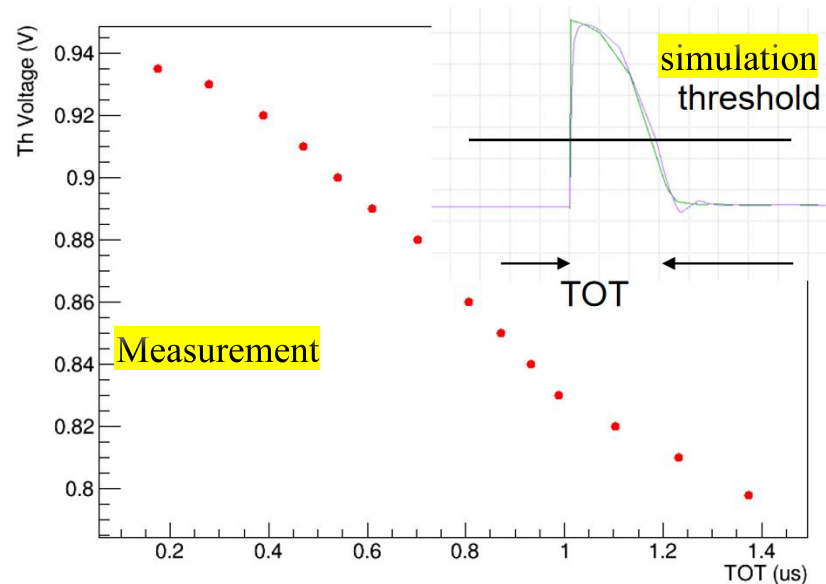
COFFEE3 Pixel-matrix-1: digital peripheral

- 64/66 encoder, scramble, testing/empty frame functions verified



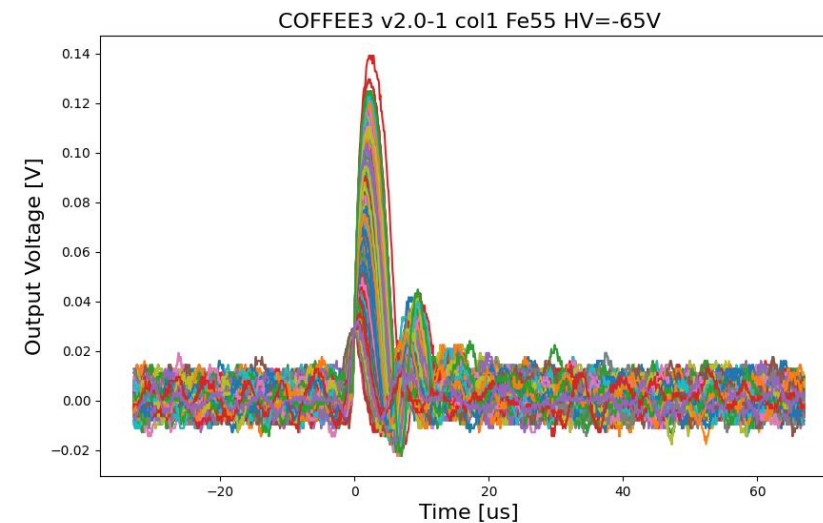
COFFEE3 Pixel-matrix-2

- In-pixel CSA and comparator output for laser signal and ^{55}Fe source (6 keV X-ray)
 - time-over-threshold (TOT) ~ 1 us, agree with simulation



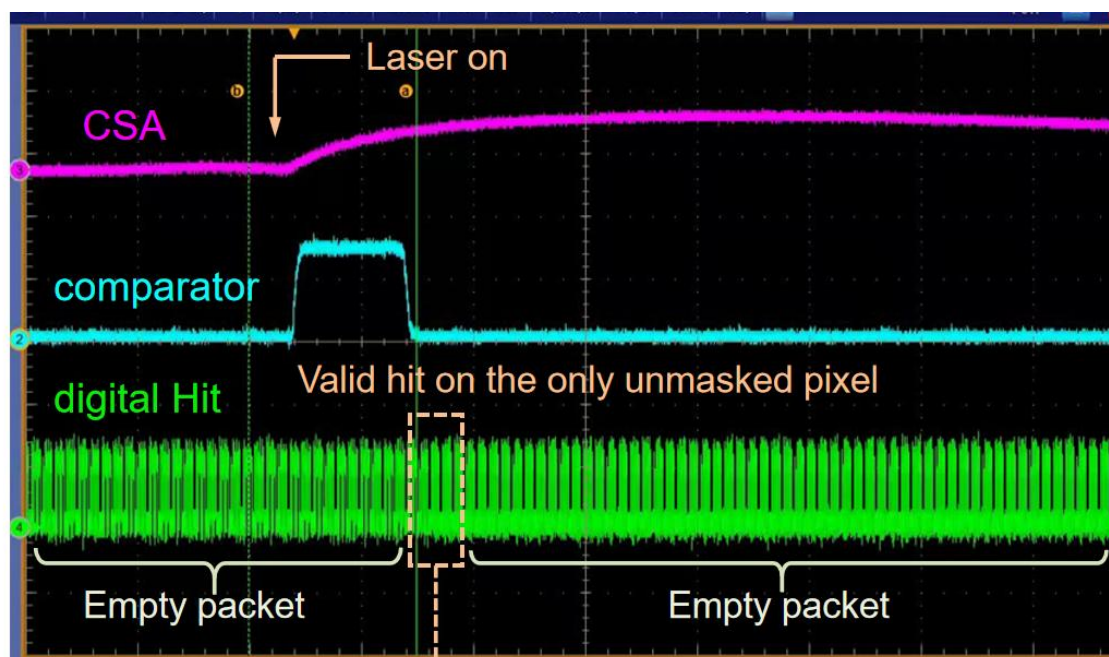
Layout of 2×3 pixels, signal pixel size is $40 \times 145 \mu\text{m}^2$

**The actual manufacturing size will be scaled down to 0.9 times the layout size.*



COFFEE3 Pixel-matrix-2

- charge sensing diode → in-pixel (CSA\comparator\TDC) → digital peripheral serializer
- Full-readout-chain with laser injection

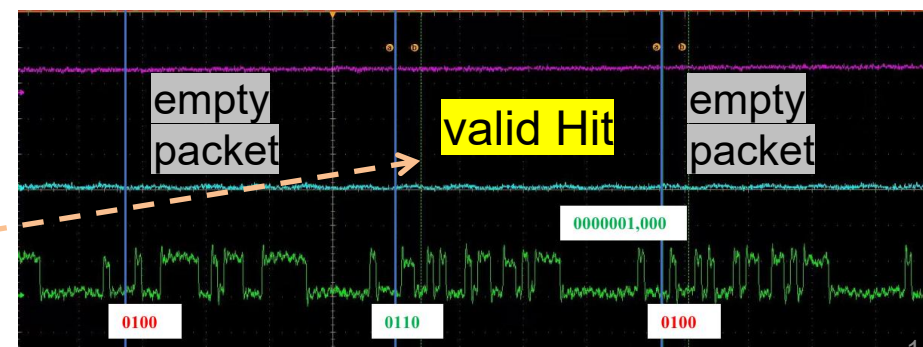
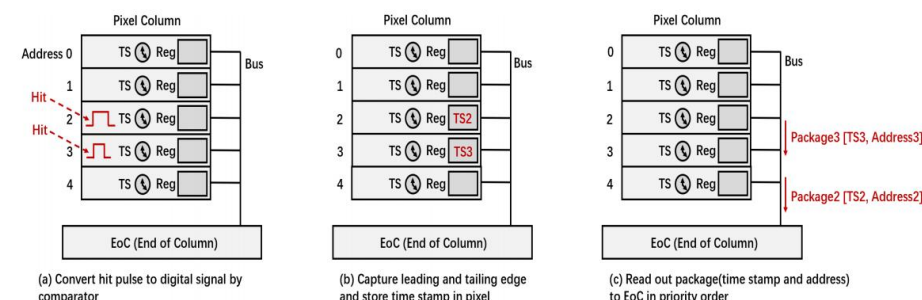


4 bit header	4 bit CHIP_TS	8 bit LE_coarse	8 bit TE_coarse	6 bit LE_fine	2 bit TE_fine	7 bit Addr_Row	3 bit Add_Col
0 1 1 0	0 1 0 1	0 0 0 1 0 1 1 0	0 1 1 0 1 0 1 1	1 1 0 0 0 0	0 0	0 0 0 0 0 0 1	0 0 0

A valid transmission packet corresponding to a hit

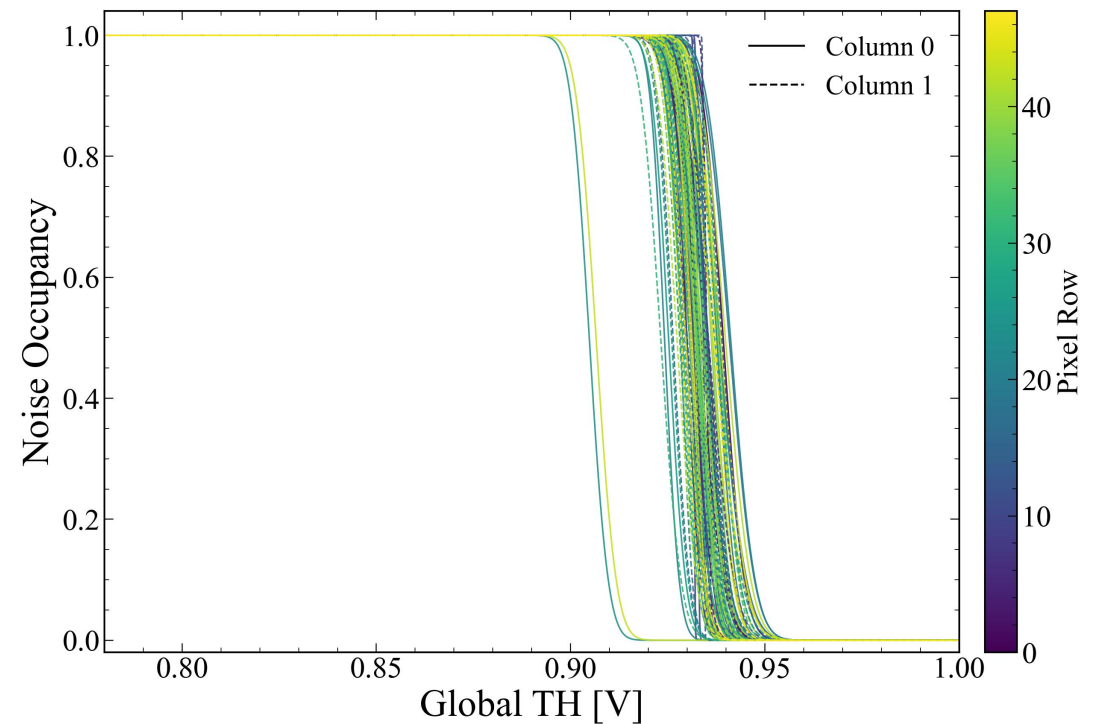
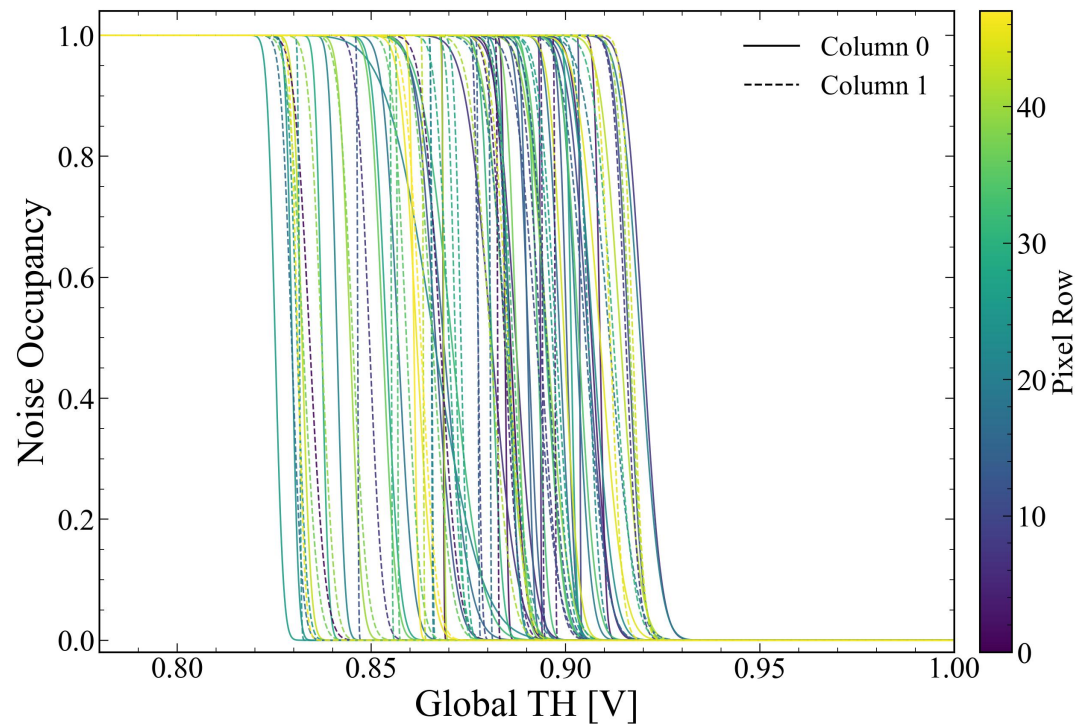
Correct row & column address

Architecture 2: employs a TDC within each pixel. Particle hit information (arrival time, end time) is recorded locally in each pixel and then read out to the bottom of the array in priority order.



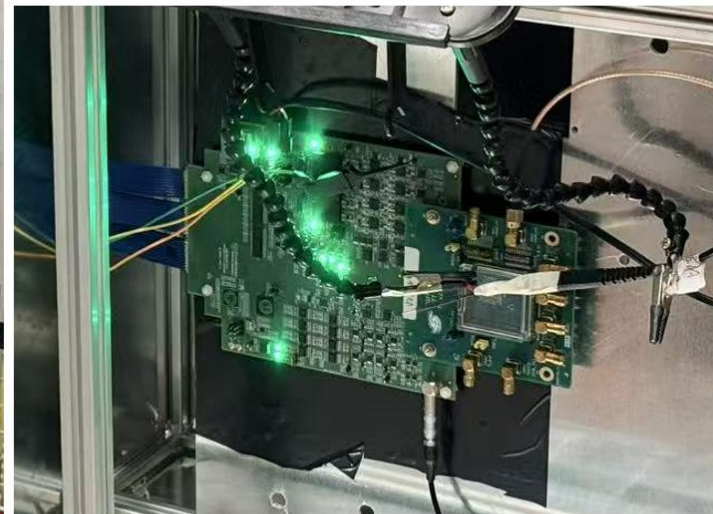
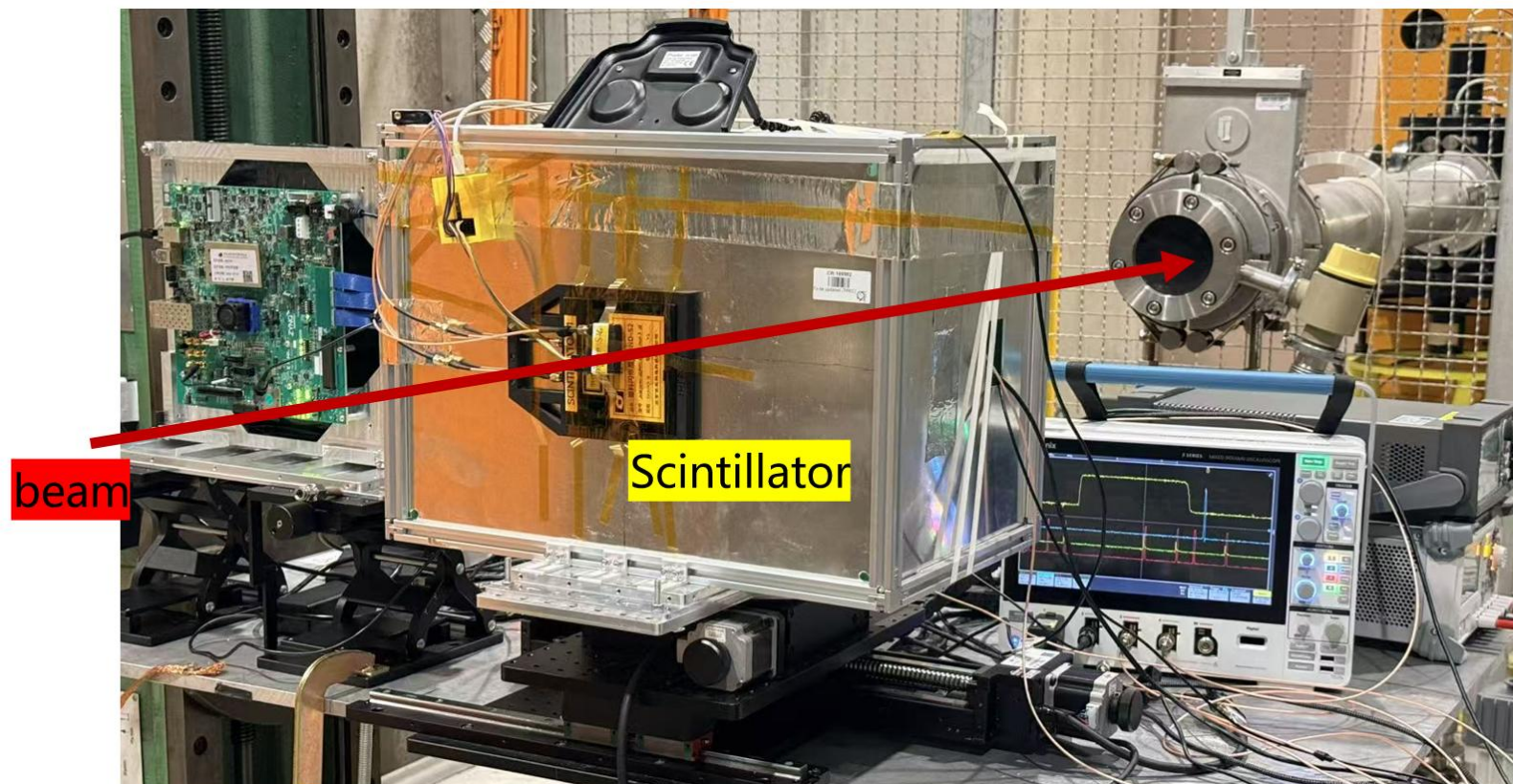
COFFEE3 Pixel-matrix-2

- Global Threshold for all pixels
- in-pixel 4-bit TDAC: tuning local Threshold to compensate individual differences



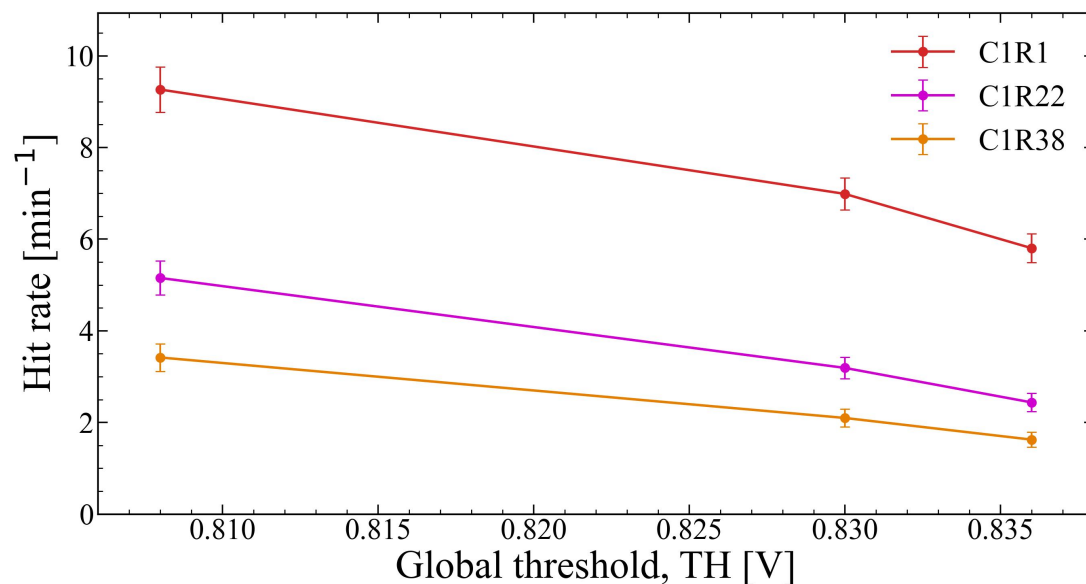
COFFEE3 testbeam

- 2026, CERN SPS, mix hadron, ~ 180 GeV/c

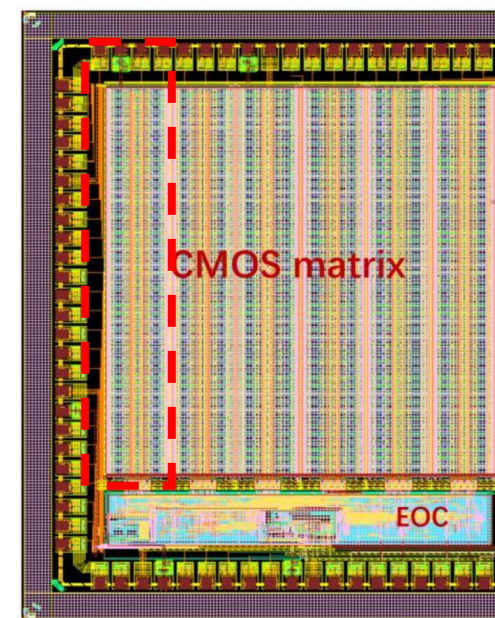


COFFEE3 testbeam: preliminary results

- 2026, CERN SPS, mix hadron, 180GeV/c
- all pixels alive, a few are noisy
- readout architecture is verified
- Global Threshold function is verified
- sensor performance will be improved with high-R wafer

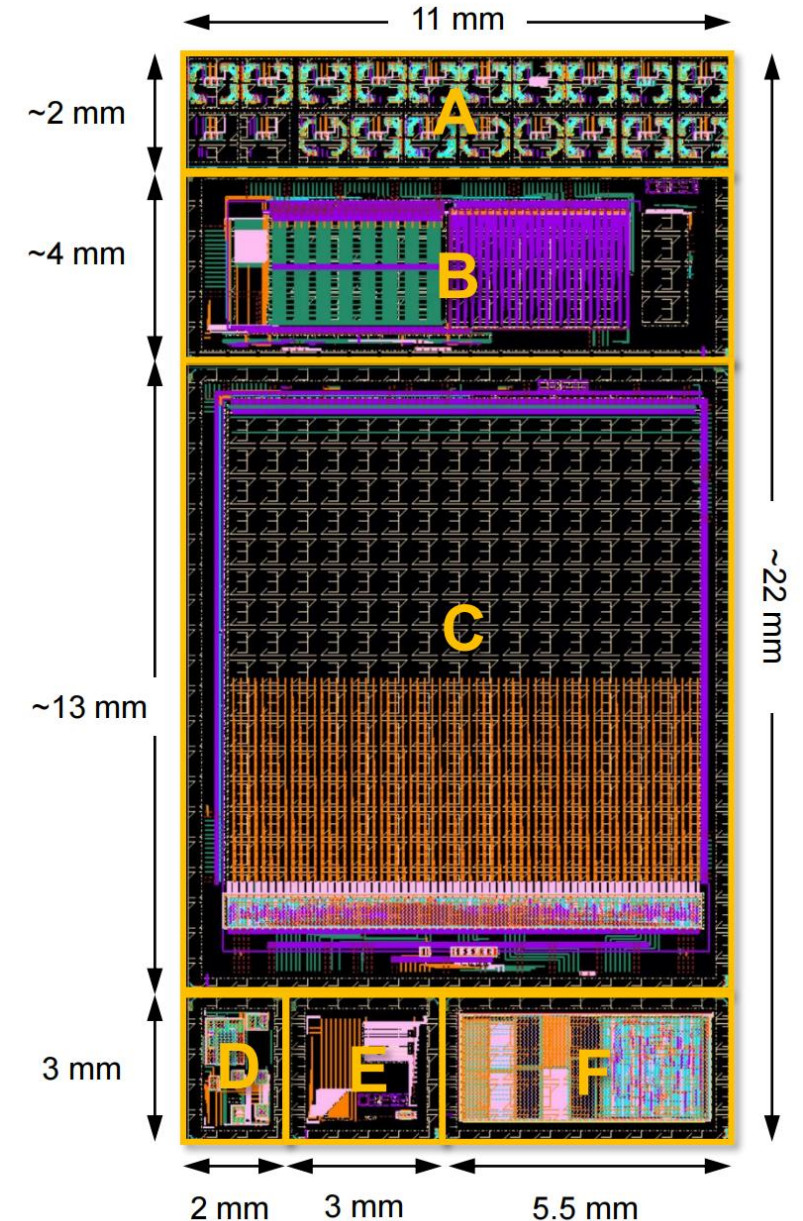


- 2 columns 96 pixels tested



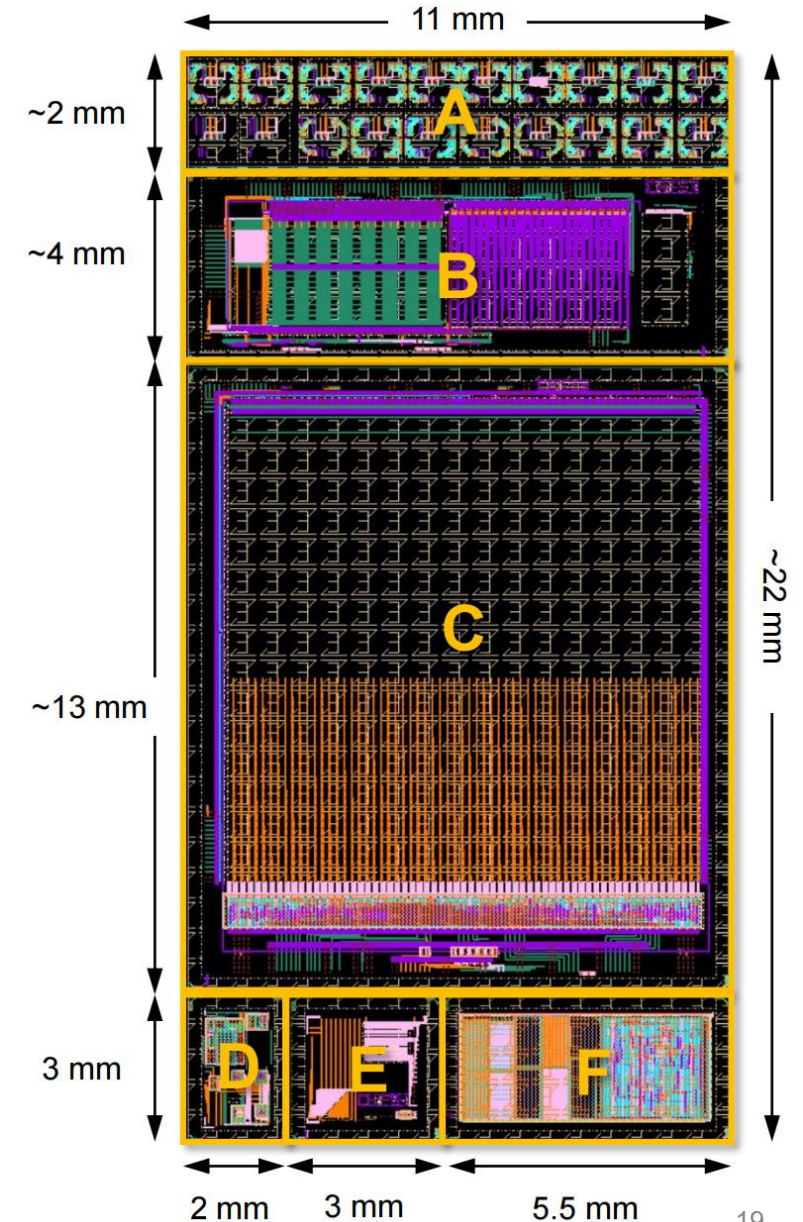
Process improvement: CHiR

- Encouraging testing results from COFFEE2/3
 - but sensor breakdown voltage, cross-talk are not ideal
- process modification + high-R wafer is needed
- **CHiR** (COFFEE-**HiR**es) design goal
 - Priority: to validate the process with high-res wafers
 - 1k/2k/4k Ohm cm wafers available from two manufactures
 - Radiation effects of simple components (eg. MOS) with or w/o radiation hardening
 - Implementation of “Five-well process”: to validate basic IP not affected by process modification



CHiR1 chip(s)

- Passive sensor validation:
 - A: 20 arrays of 3x4 passive pixels with diff guard ring designs
 - Pixel size: 38 μm x 175 μm
- Pixel array design
 - B: 9 variations of in-pixel frontend designs
 - C: main pixel array of 256 x 64 pixels;
 - E: alternative small pixel arrays
- IP validations
 - D/E: shuntLDO, PLL, DLL, LVDS, ...
 - F: digital modules and transistors for TID and SEE studies
- Submitted in early 2026, testing results is on-the-way



COFFEE Teams

➤ Chip design:

- **COFFEE2:** Weiguo LU, Mei ZHAO, Kunyu Xie, Leyi Li, Ruoshi DONG, Yang CHEN, Xuekang LI, Xinyang GUO, Zhuojun CHEN, Yang ZHOU;

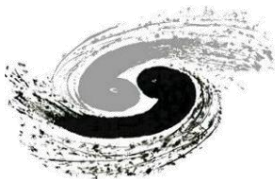
& **Independent KIT design:** Hui ZHANG, Ruoshi DONG, Ivan PERIC;

- **COFFEE3:** Leyi Li, Xiaoxu ZHANG, XiaoMin WEI, Weiguo LU, Pengxu LI, Mei ZHAO, Yang CHEN, Yujie WANG, Huimin Wu, Zexuan ZHAO, Yu ZHAO, Yang YU, Xia CHEN, Jia SHI, Yang ZHANG

➤ Chip test and validation:

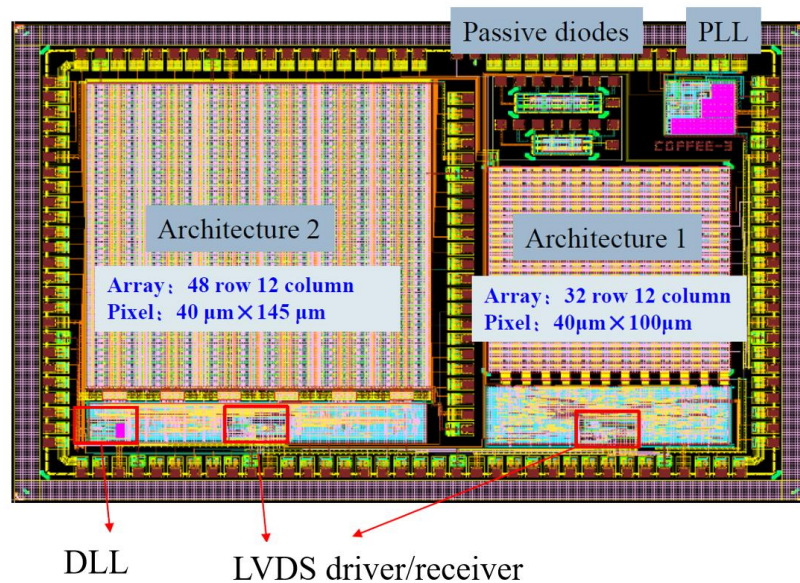
- Zhiyu Xiang, Zijun Xu, Zeng CHENG, Menke Cai, Boxing Wang, Yuman Cai, Weiguo LU, Mingjie FENG, Hui ZHANG, Jianpeng DENG, Pengxu LI, Hongbo ZHU, Yiming Li

More collaboration and experts are desired for the chip development.....

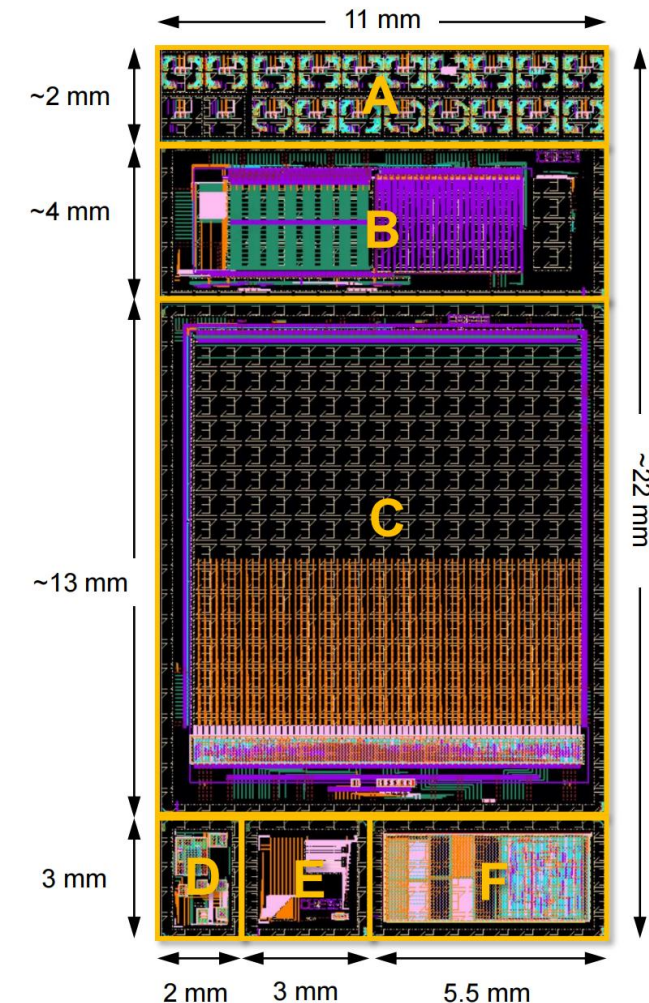


Summary

- Encouraging results from COFFEE2/3:
 - V(Breakdown)~70V. High-Resistivity wafer will significantly improve
 - most analog/digital, in-pixel/EOC circuits verified
 - irradiation and testbeam on-going

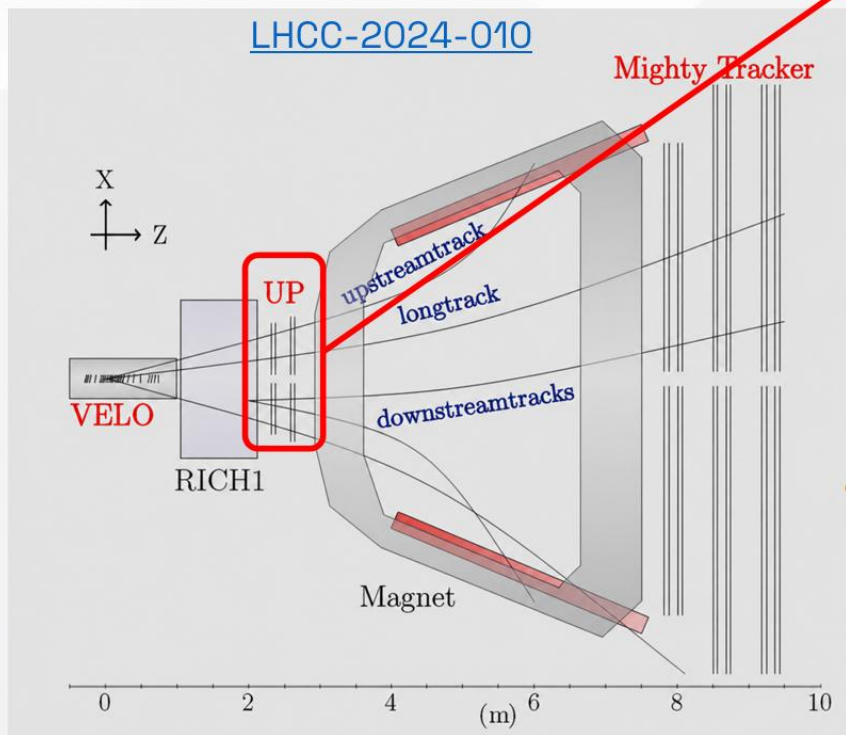


- ChiR: process modi. + high-R wafer



Backup

What Should UP Deliver?



- What should UP deliver?

- ⇒ Maintaining (ideally enhancing) the track momentum resolution
- ⇒ Suppressing ghost tracks
- ⇒ Accelerating real-time track reconstruction
- ⇒ Efficiently reconstructing long-lived particle decays



- Requirements for the UP to handle the $\times 5$ luminosity increase:

- Higher granularity than UT
- Full geometric coverage, matching the tracking system
- Sufficient layers to reconstruct UP segments-based track
- Radiation-hard and low-material design

- Upstream tracks:

- Hits in the VELO and UP, without MT

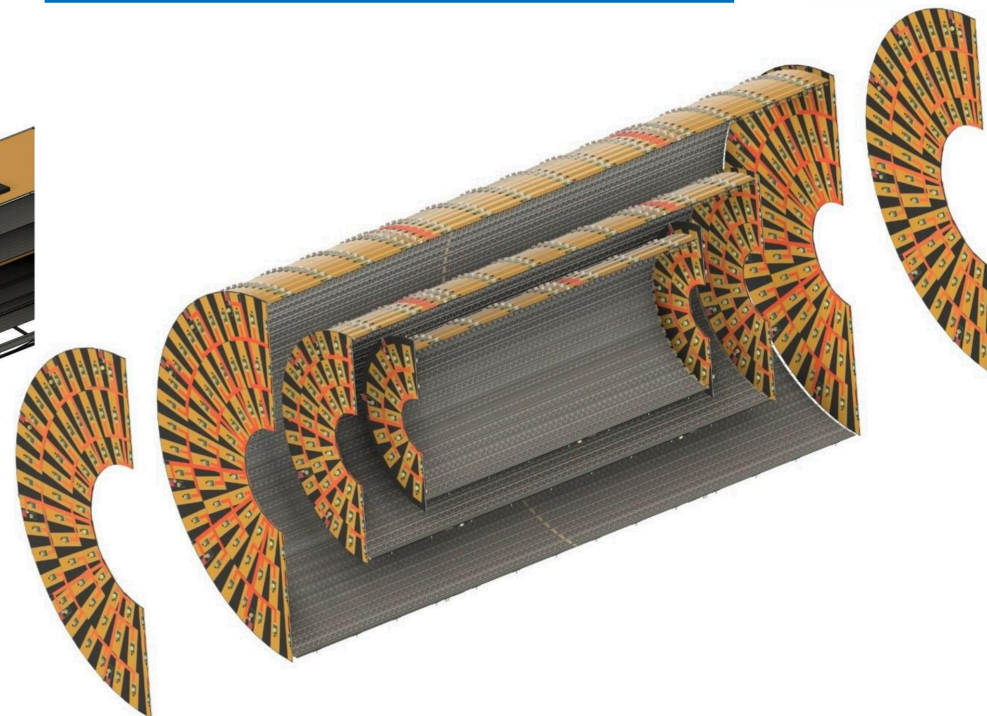
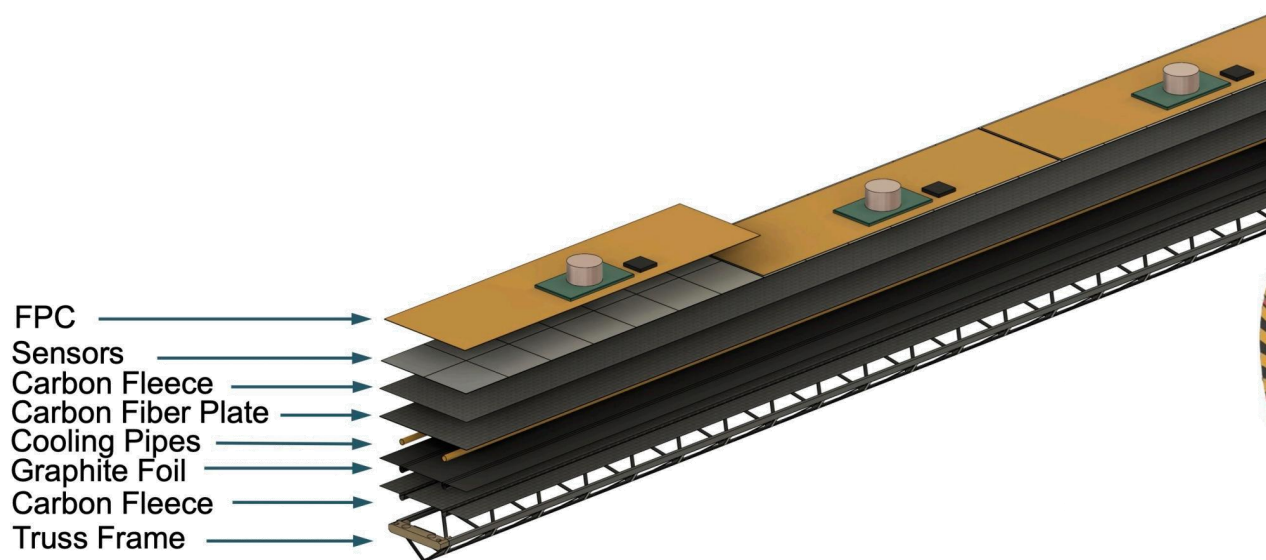
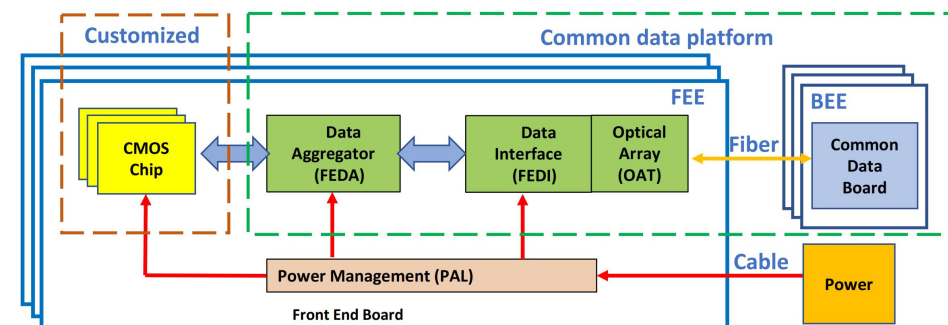
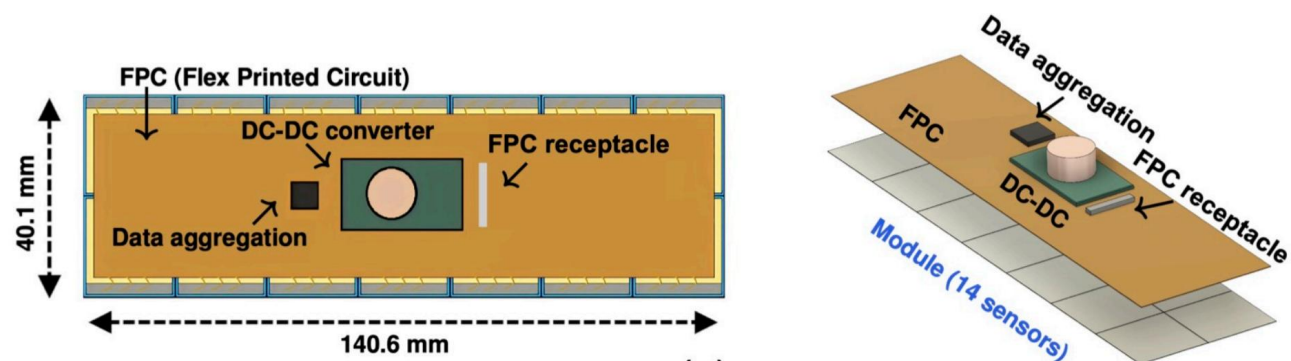
- Downstream tracks:

- Hits in the UP and MT, without VELO

- Long tracks:

- Across the full tracking system, combining VELO + UP + Mighty Tracker

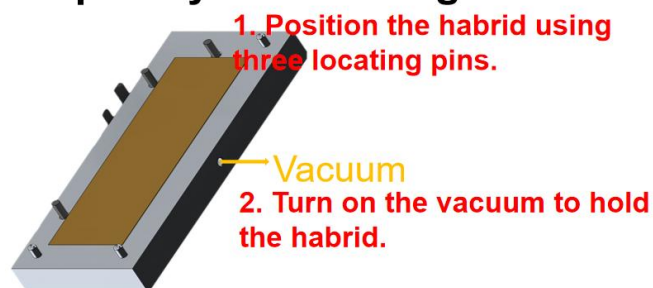
Pixel ASICs for CEPC Silicon Inner Tracker



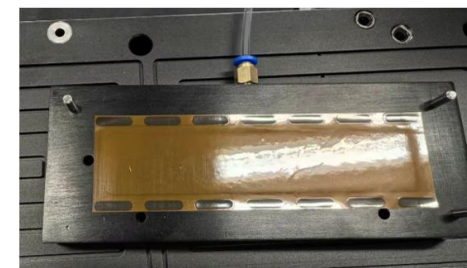
CEPC Silicon Inner Tracker: dummy module

Assembly Procedure

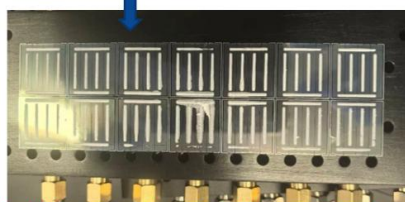
Step 3. Hybrid Loading



3. Remove the pins once the habrid is secured.

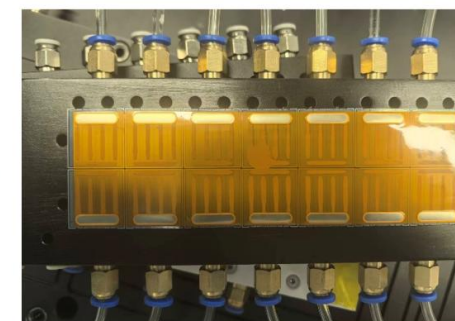
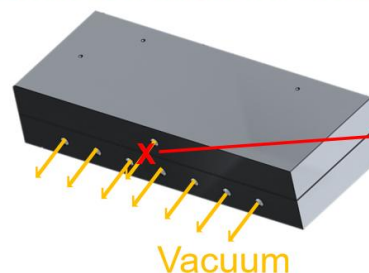


Step 4. Module Assembly



1. Align and mate the adhesive-applied sensors and hybrid using locating pins and holes, with spacers between the two jigs.

2. Wait 30 minutes for the adhesive to cure.



CEPC Ref-Detector

Table 2.1: Physics objects and key observables used as benchmarks for setting the requirements and the optimization of the CEPC detector.

Physics objects	Measurands	Detector subsystem	Performance requirement
Tracking	Coverage Recon. efficiency Resolution in barrel Resolution in endcap	Tracker	$ \cos \theta \leq 0.99$ $\geq 99\%$ ($p_T > 1 \text{ GeV}/c$) $\sigma_{p_T}/p_T < 0.3\%$ ($ \cos \theta \leq 0.85$) $\sigma_{p_T}/p_T < 3\%$ ($ \cos \theta > 0.85$)
Leptons (e, μ)	PID efficiency Mis-ID rate	Tracker, ECAL HCAL, Muon	$\geq 99\%$ ($p > 5 \text{ GeV}/c$, isolated) $\leq 2\%$ ($p > 5 \text{ GeV}/c$, isolated)
Photons	PID efficiency Mis-ID rate Energy resolution	ECAL, HCAL	$\geq 95\%$ ($E > 3 \text{ GeV}$, isolated) $\leq 5\%$ ($E > 3 \text{ GeV}$, isolated) $\sigma_E/E \leq 3\%/\sqrt{E(\text{GeV})} \oplus 1\%$
Vertex	Position resolution	Vertex	$\sigma_{r\phi} = 5 \oplus \frac{10}{p(\text{GeV}) \times \sin^{3/2} \theta} (\mu\text{m})$
Hadronic jets	Energy resolution Mass resolution	Tracker ECAL, HCAL	$\sigma_E/E \sim 30\%/\sqrt{E(\text{GeV})} \oplus 4\%$ $\text{BMR} \leq 4\%$
Jet flavor tagging	b-tagging efficiency c-tagging efficiency	Full detector	$\sim 80\%$, mis-ID of uds $< 0.3\%$ $\sim 50\%$, mis-ID of uds $< 1\%$
Charged kaon	PID efficiency, purity	Tracker, TOF	$\geq 90\%$ (inclusive Z sample)

CEPC Ref-Detector

Table 2.3: Parameters and layout of the CEPC tracker including VTX, ITK, TPC, and OTK. The column labeled $\pm z$ shows the half-length of the barrel layers, and the z position of the endcap disks. The column labeled σ_ϕ and σ_t represent the spatial resolution in the bending direction and time resolution, respectively.

Components		Radius R [mm]	$\pm z$ [mm]	Material [X_0]	σ_ϕ [μm]	σ_t [ns]	
Beam pipe		10.55	85.0	0.454%	—	—	
VTX	Layer 1	11.1	80.7	0.067%	5	100	
	Layer 2	16.6	121.1	0.059%	5	100	
	Layer 3	22.1	161.5	0.058%	5	100	
	Layer 4	27.6	201.9	0.061%	5	100	
	Layer 5	39.5	341.0	0.280%	5	100	
	Layer 6	47.9	341.0	0.280%	5	100	
Beam pipe protective cylinder		66.3	462.0	0.19%	—	—	
ITK Barrel	Layer 1 (ITKB1)	235.0	493.3	0.68%	8	3–5	
	Layer 2 (ITKB2)	345.0	704.8	0.68%	8	3–5	
	Layer 3 (ITKB3)	555.6	986.6	0.68%	8	3–5	
OTK Barrel	Layer 4 (OTKB)	1,800.0	2,840.0	1.58%	10	0.05	
TPC	Inner wall	600.0	2,900.0	0.45%	—	—	
	Gas	605.4–1,779.6	2,750.0	1.00%	110–144	—	
	Outer wall	1,800.0	2,900.0	0.69%	—	—	
		R_{in}	R_{out}				
ITK Endcap	Disk 1 (ITKE1)	82.5	244.7	505.0	0.76%	8	3–5
	Disk 2 (ITKE2)	110.5	353.7	718.5	0.76%	8	3–5
	Disk 3 (ITKE3)	160.5	564.0	1,000.0	0.76%	8	3–5
	Disk 4 (ITKE4)	220.3	564.0	1,489.0	0.76%	8	3–5
OTK Endcap	Disk 5 (OTKE)	406.0	1,816.0	2,910.0	1.37%	10	0.05

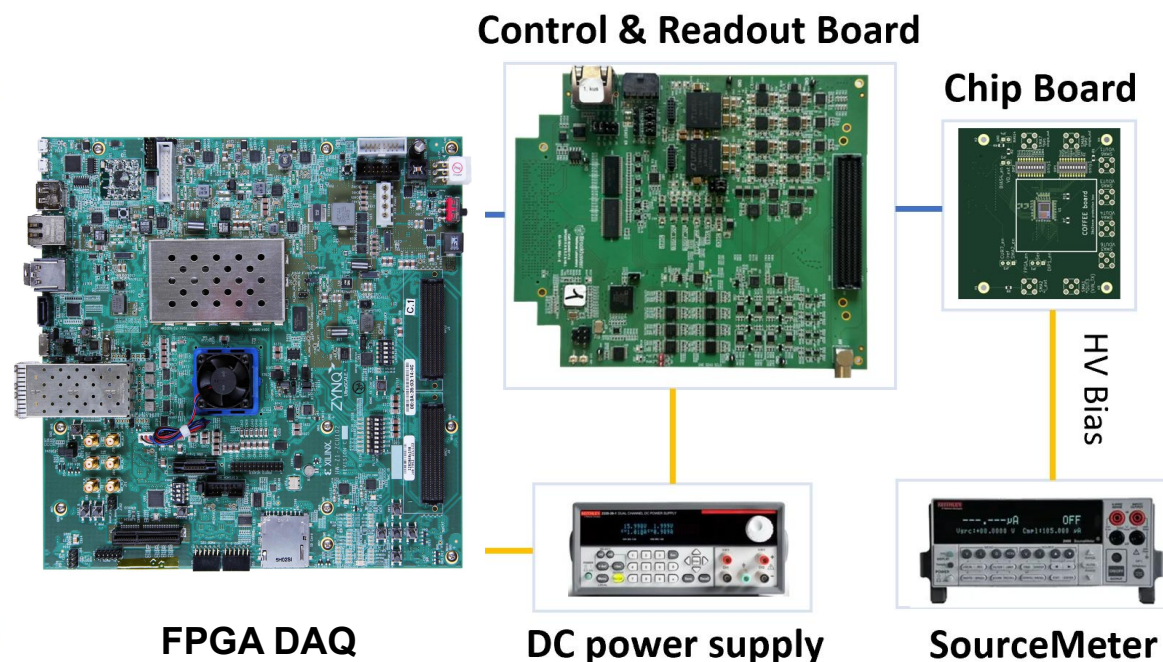
Bench-top DAQ Setup

- Caribou DAQ from DRD3: power, clk, DAC, slow-ctrl, fast readout, ...
- FE chip specific carrier board, firmware IP, and software by ourself

Control and Readout (CaR) board

Feature	Description
Adjustable Power Supplies	8 units, 0.8 – 3.6 V, 3 A
Adjustable Voltage References	32 units, 0 – 4 V
Adjustable Current References	8 units, 0 – 1 mA
Voltage Inputs to Slow ADC	8 channels, 50 kSPS, 12-bit, 0 – 4 V
Analog Inputs to Fast ADC	16 channels, 65 MSPS, 14-bit, 0 – 1 V
Programmable Injection Pulsers	4 units
Full-Duplex High-Speed GTx Links	8 links, <12 Gbps
LVDS Links	17 bidirectional links
Input/Output Links	10 output links, 14 input links, 0.8 – 3.6 V
Programmable Clock Generator	Included
External TLU Clock Reference	Included
External High-Voltage (HV) Input	Included
FEAST Module Compatibility	Supported
FMC Interface to FPGA	Included
SEARAY Interface to Detector Chip	320-pin connector

Resources for various target applications



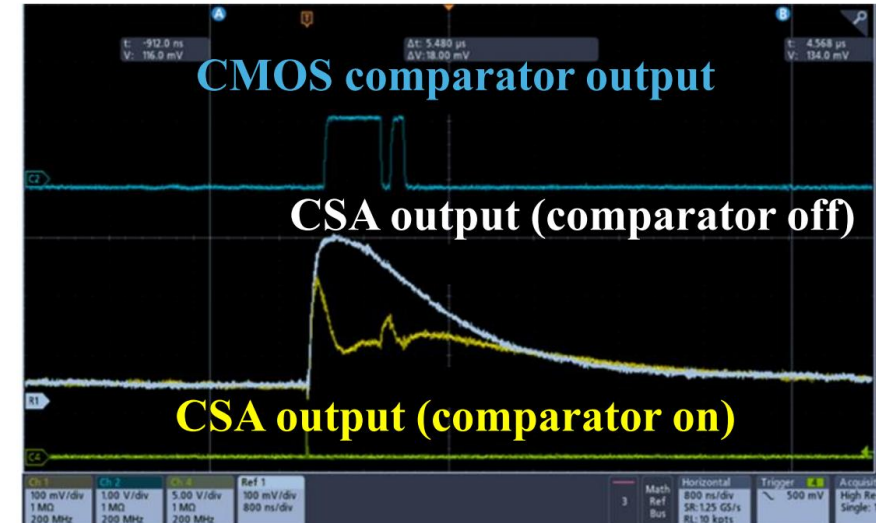
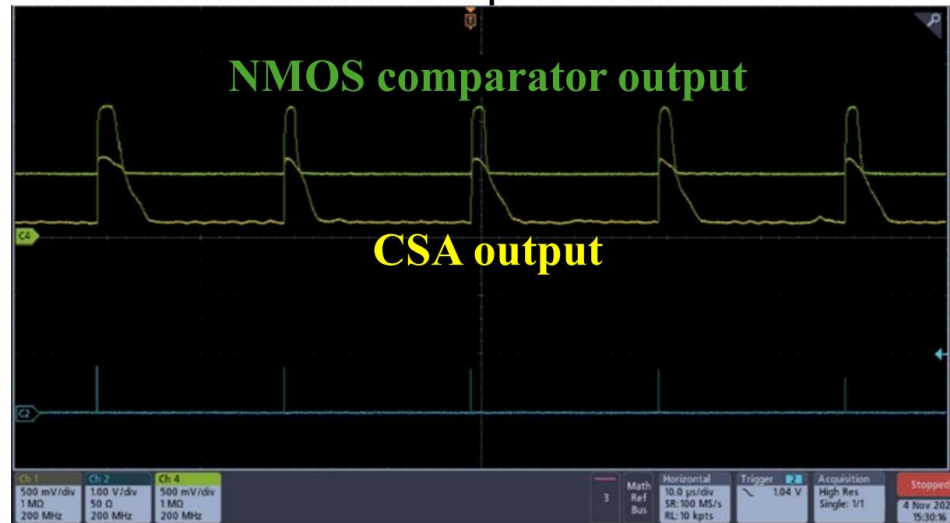
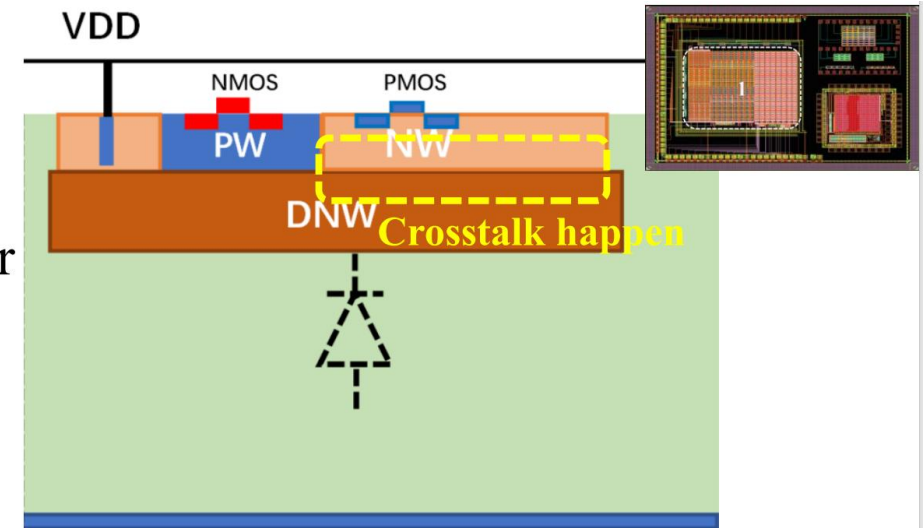
HV-CMOS

Table 5.3: The HV-CMOS sensor key parameters

Parameter	Value
Sensor size	2 cm $\times$ 2 cm (active area: 1.74 cm $\times$ 1.92 cm)
Sensor thickness	150 μm
Array size	512 $\times$ 128
Pixel size	34 μm $\times$ 150 μm
Spatial resolution	8 μm $\times$ 40 μm
Time resolution	3–5 ns
Power consumption	200 mW/cm ²
Technology node	55 nm

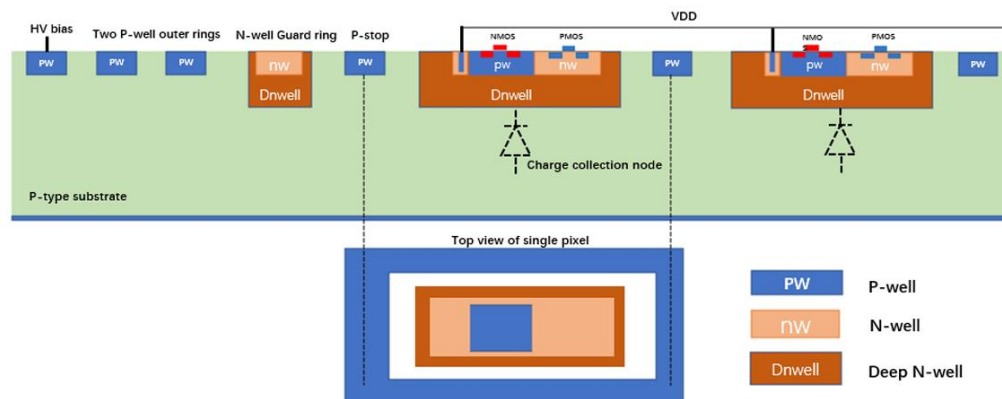
COFFEE2: in-pixel Ana/Digi-circuit X-talk

- Laser test : **JINST 20 (2025) C10011**
 - NMOS comparator work well
 - Crosstalk issue seen among CMOS comparator and CSA.
 - Potential flip in digital circuitry cause the disturbance between N-well of PMOS bulk terminal and deep N-well



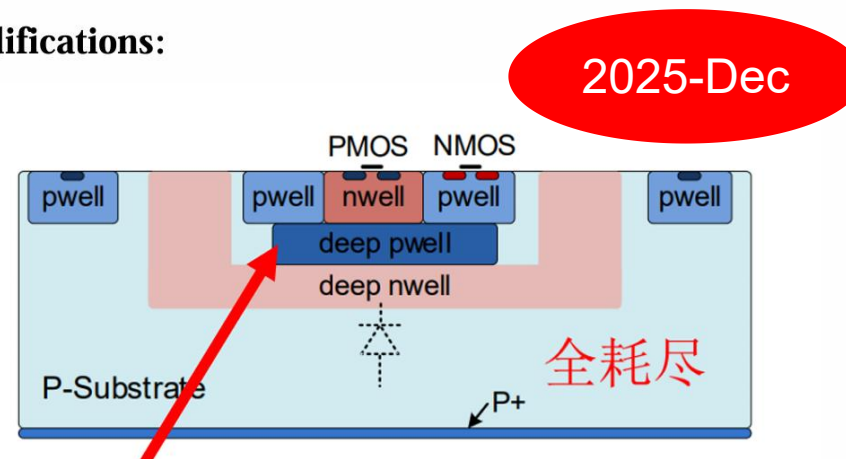
COFFEE Design: Now and Next

Current condition of the used 55nm commercial process:



- **Triple-well:** transistors are enfolded by Drwell
- **Wafer resistivity:** **10 $\Omega\cdot\text{cm}$;**
- **Metal layers:** **9 (1 top metal);** **benefit for routing**
- The charge sensing diode formed by DNW & PSUB could be biased > **70V** before breakdown;
Depletion depth about 10 — 20 μm ;
 (corresponding to 1k – 2k e^- total signal charges)

Process modifications:



Several modifications are desired:

1. **Replace the wafer for a higher resistivity substrate:** significantly increase the depletion depth, enhancing the total signal charge (2k – 20k e^-) and reducing the front-end equivalent capacitance -> resulting in a higher SNR (signal-to-noise ratio);
2. **Fine-tuning the well structure:** Adding an isolation layer between the Nwell and DNW allows for the integration of complex digital circuits within the pixel -> greatly increasing design flexibility and improving overall performance.

..... Efforts are still on going