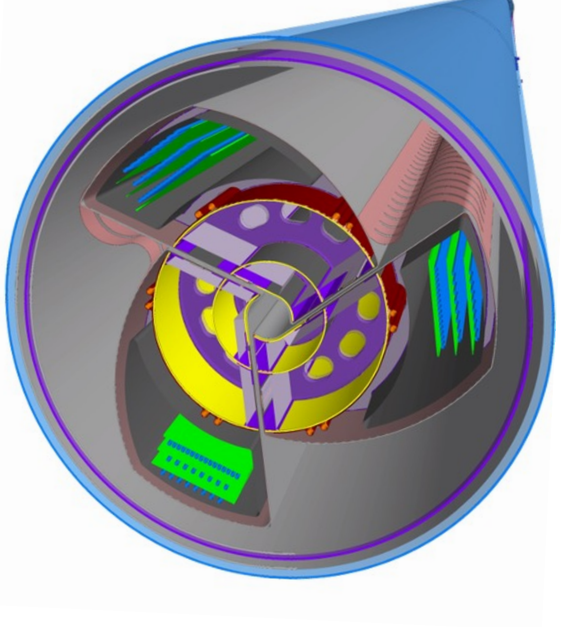


Characterisation of Pixel Chip Prototypes for the ALICE 3 Inner Tracker

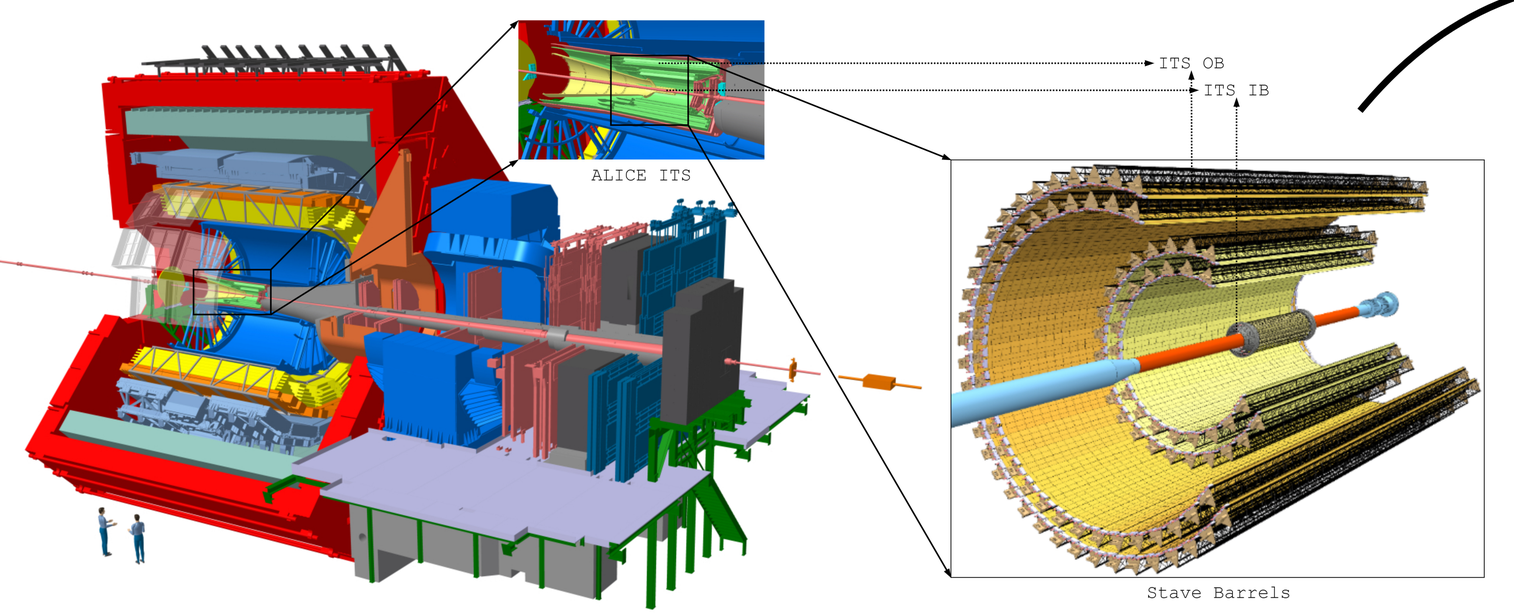
International Conference on Instrumentation for Colliding Beam Physics 2026
Hefei, China

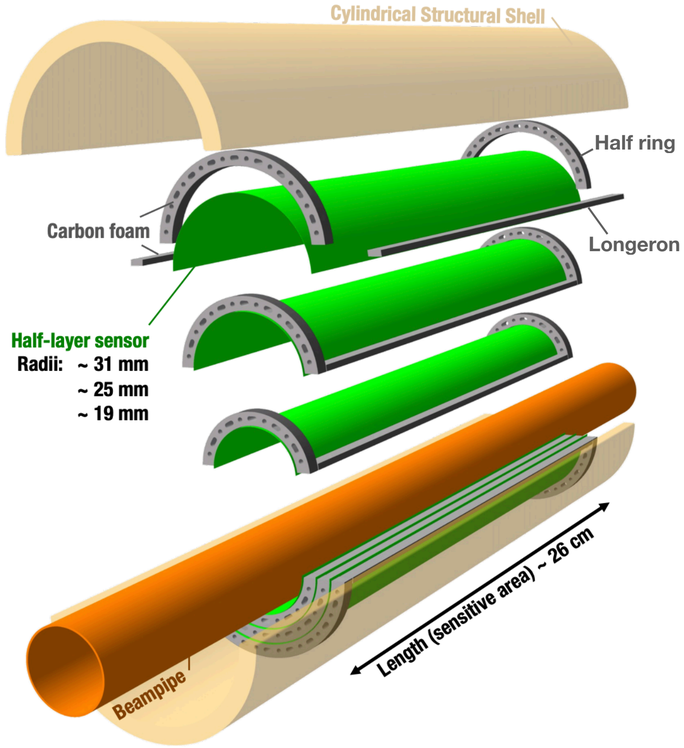
Naseem Bouchhar (Sejong University)
On behalf of the ALICE Collaboration

12/10/2026

ALICE EXPERIMENT

ITS2 inner 3 layers: 432 flat sensors → **ITS3: 6 bent sensors**





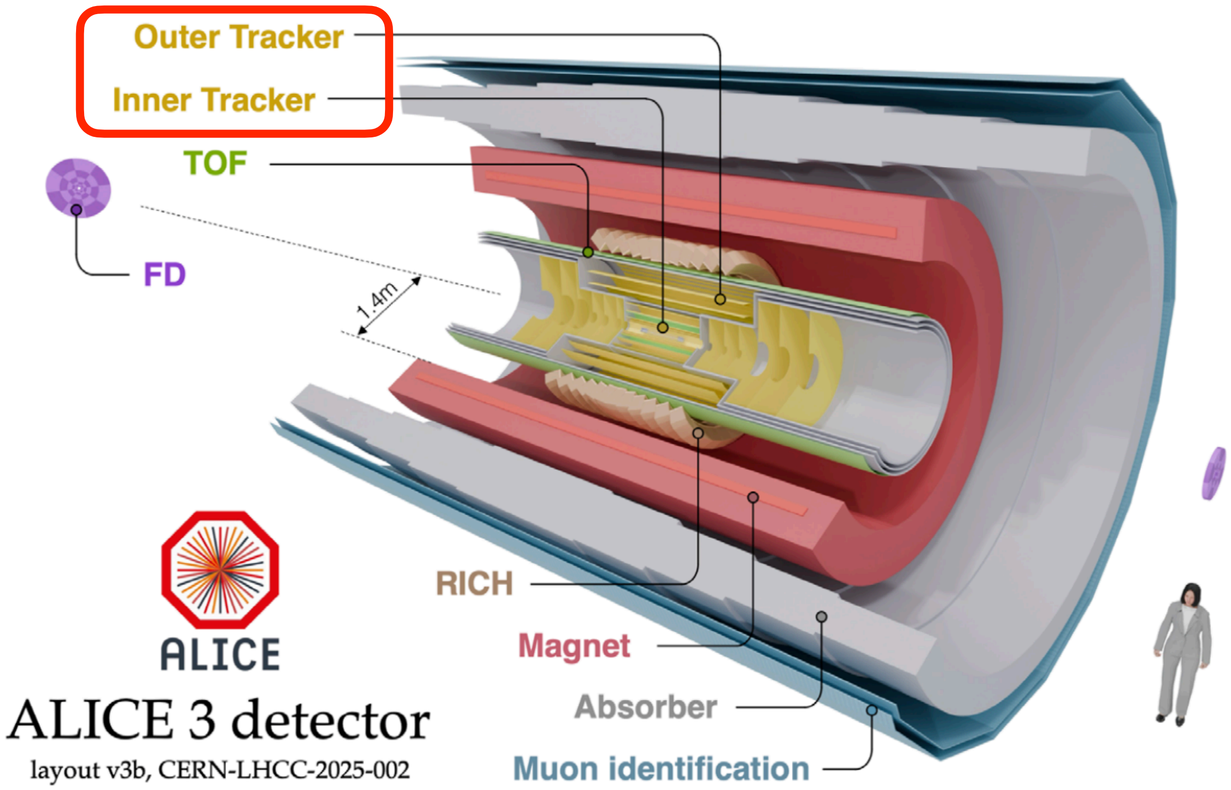
ALICE 2				ALICE 2.1							ALICE 3				
2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036	2037	…
Run 3 2022 – 2026				**LS3** 2026 – 2030			**Run 4** 2030 – 2034				**LS4** 2034 – 2036		**Run 5** from 2036		

Today

ALICE 3 UPGRADE

More on this in talk by J. Klein

- ALICE 3 trackers + vertex detector
  - 46 m^2 coverage
- Must handle high luminosity
  - ~ 100 kHz (Pb—Pb) ← x2 operational Run 3 interaction rate
  - ~ 24 MHz (pp) ← ~ x50 operational Run 3 interaction rate
- Large tracker η range: $|\eta| < 2.5$
- Wide transverse momentum range: p_T > 0.05 GeV/c extending to 10 GeV/c





ALICE 3 TRACKER UPGRADE

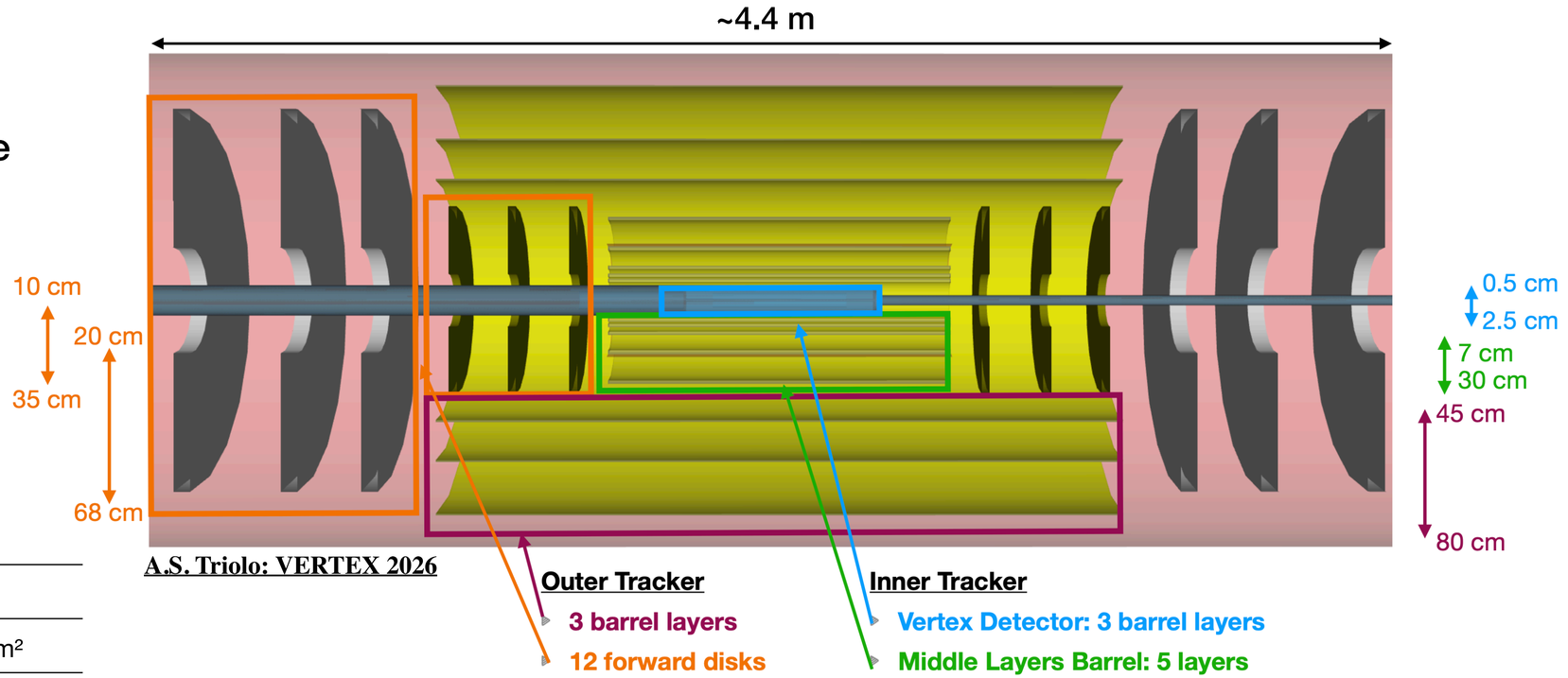
More on this in talk by J. Klein

Inner tracker (IT)

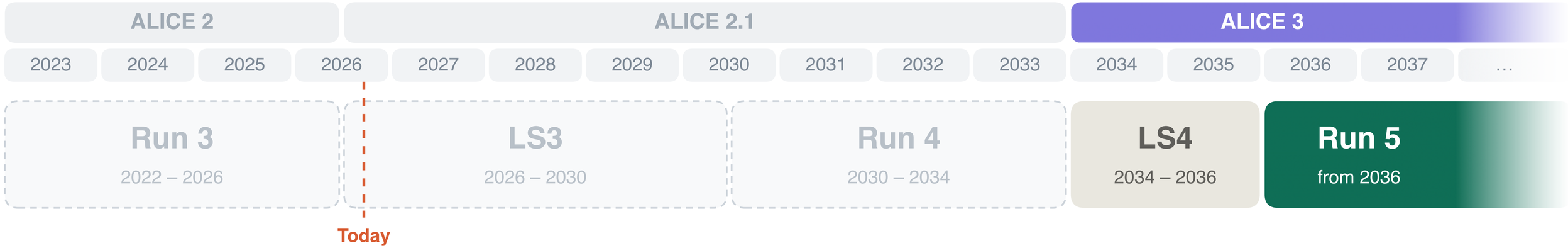
- Vertex Detector (VD): 3 layers inside the beam pipe, retractable
- Middle Layers (ML): 5 Layers outside the beam pipe

Outer tracker (OT)

- Barrel: 3 layers
- Small disks: 6 layers (10-35 cm radius)
- Large disks: 6 layers (20-68 cm radius)



	VD	ML/OT
Spatial resolution	2.5 μm	10 μm
Power density	70 mW/cm^2	20-30 mW/cm^2
Particle hit-rate	100 MHz/cm^2	1 - 0.1 MHz/cm^2



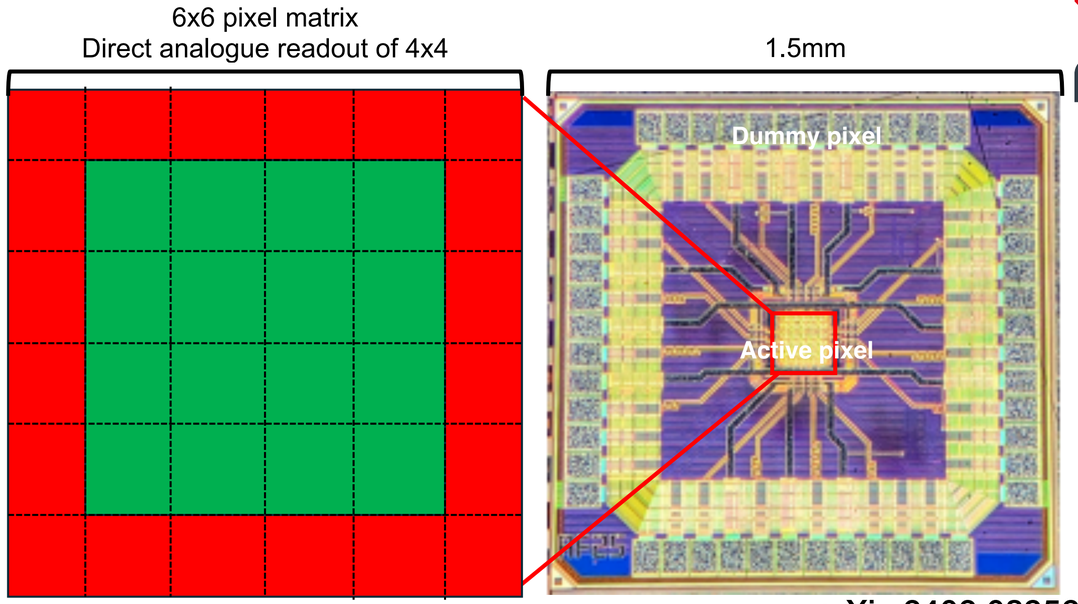
ALICE 3 PIXEL TESTING

Analogue Pixel Test Structure (APTS) - used for exploration of different sensor designs

Validation of different design approaches required: pixel pitches, split processes, and pixel architecture

→ Towards nominal choice for ALICE 3 tracker sensors

Originally used for validation of 65nm technology by ITS3



arXiv:2403.08952

Pixel pitches:
10,12,15μm VD
20.8x22.8, 30, 40, 50μm ML/OT

ALICE 3 PIXEL TESTING

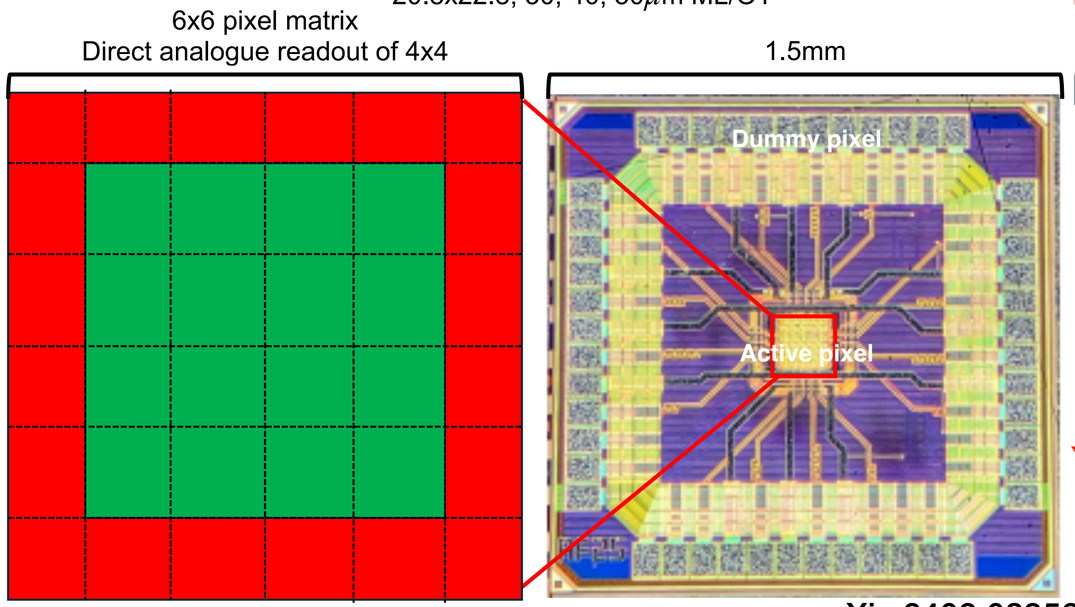
Analogue Pixel Test Structure (APTS) - used for exploration of different sensor designs

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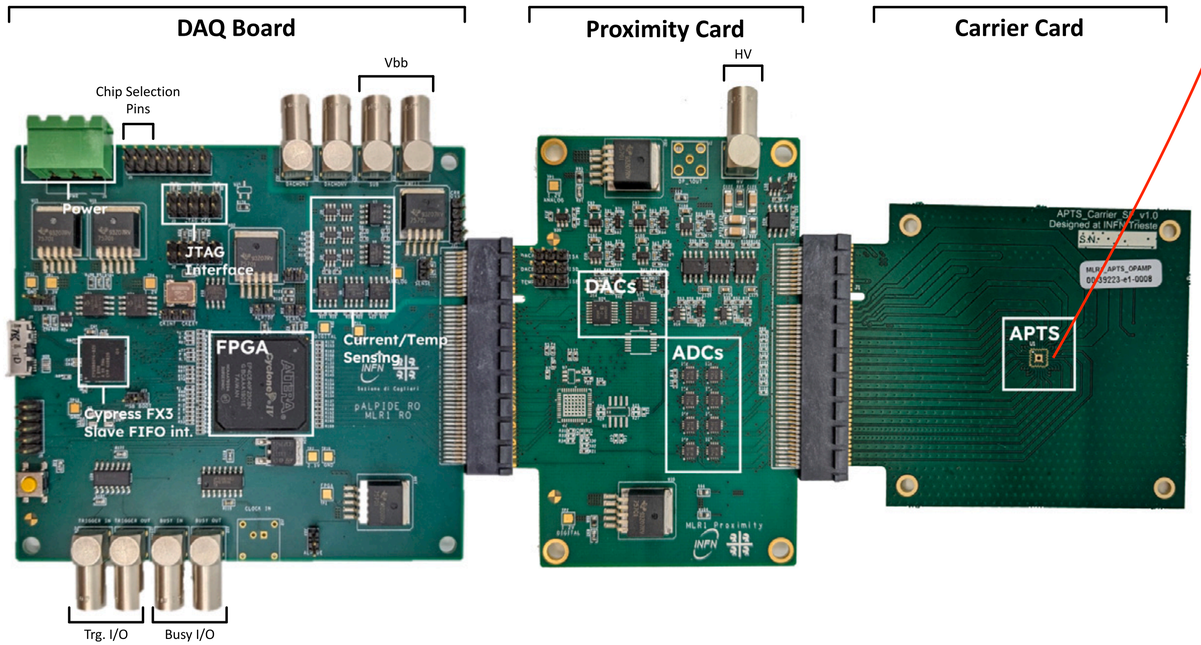
Pixel pitches:
10,12,15μm VD
20.8x22.8, 30, 40, 50μm ML/OT



arXiv:2403.08952

- Testbeam and in-lab measurements can provide information on a number of things
  - Pixel capacitance
  - Charge collection efficiency
  - Noise comparisons
  - NIEL radiation effects

Neutron irradiation at JSI from $10^{13} - 10^{16}$ MeV n_{eq} cm^{-2}



PROCESS OPTIMISATION

APTS campaign with various doping variants and pixel pitches optimised for VD and ML/OT

Splits refer to different sensor implants

- **Split 4: Baseline**

- Relatively low capacitance, reasonable radiation tolerance

- **ALICE 3 ML/OT**

- Lower capacitance → improved signal-to-noise ratio

- Large pitch ($\geq$ 20 μm), low reverse bias

- **Utilisation of split 5/6**

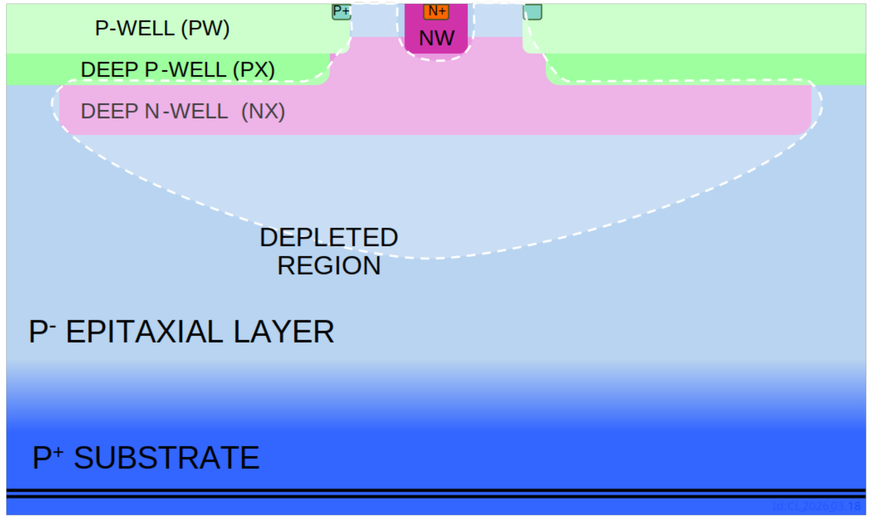
- **ALICE 3 VD**

- Faster charge collection → improved radiation tolerance

- Small pitch (~10 μm) high reverse bias, high radiation tolerance

- **Development of split 7**

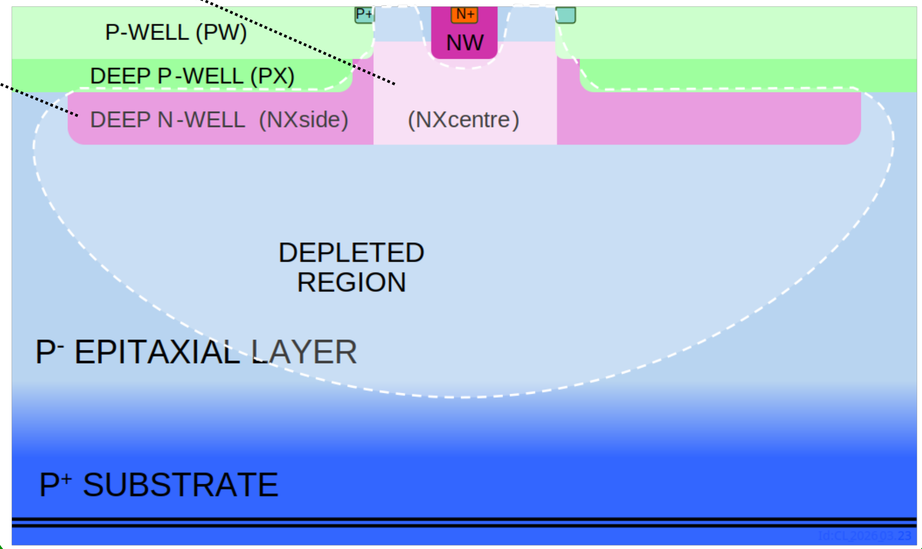
Split 4



Mainly drives pixel capacitance

Mainly drives charge collection

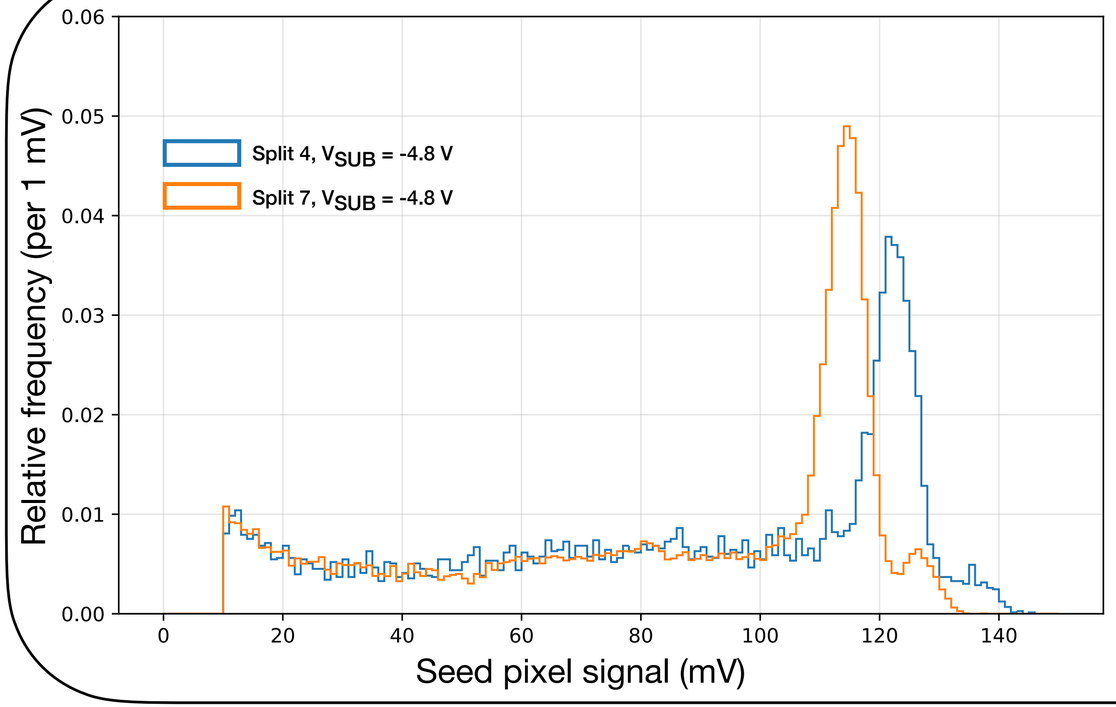
Split 5,6,7



New splits designed to partially decouple capacitance and charge collection properties

G. Borghello et al. JINST 20 (2025) C07053

SOURCE MEASUREMENTS

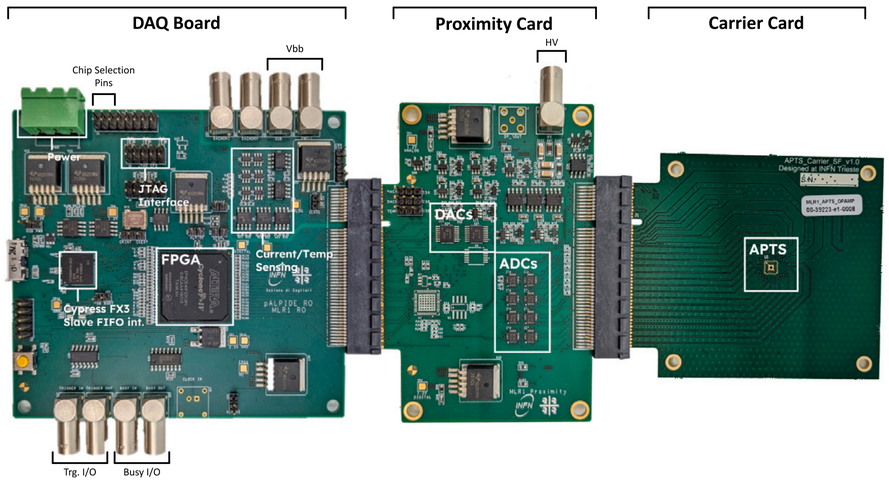


ALICE 3 IT *WIP*
Fe55 source measurements
Plotted on 21 Jul 2026

Non-irradiated
Type: G
17 °C
Pitch 10x10 µm^2

- ^{55}Fe source over APTS to study charge collection
  - Comparison of split 4 and split 7 chips
  - As expected from design split 4 sees higher amplitude due to lower capacitance

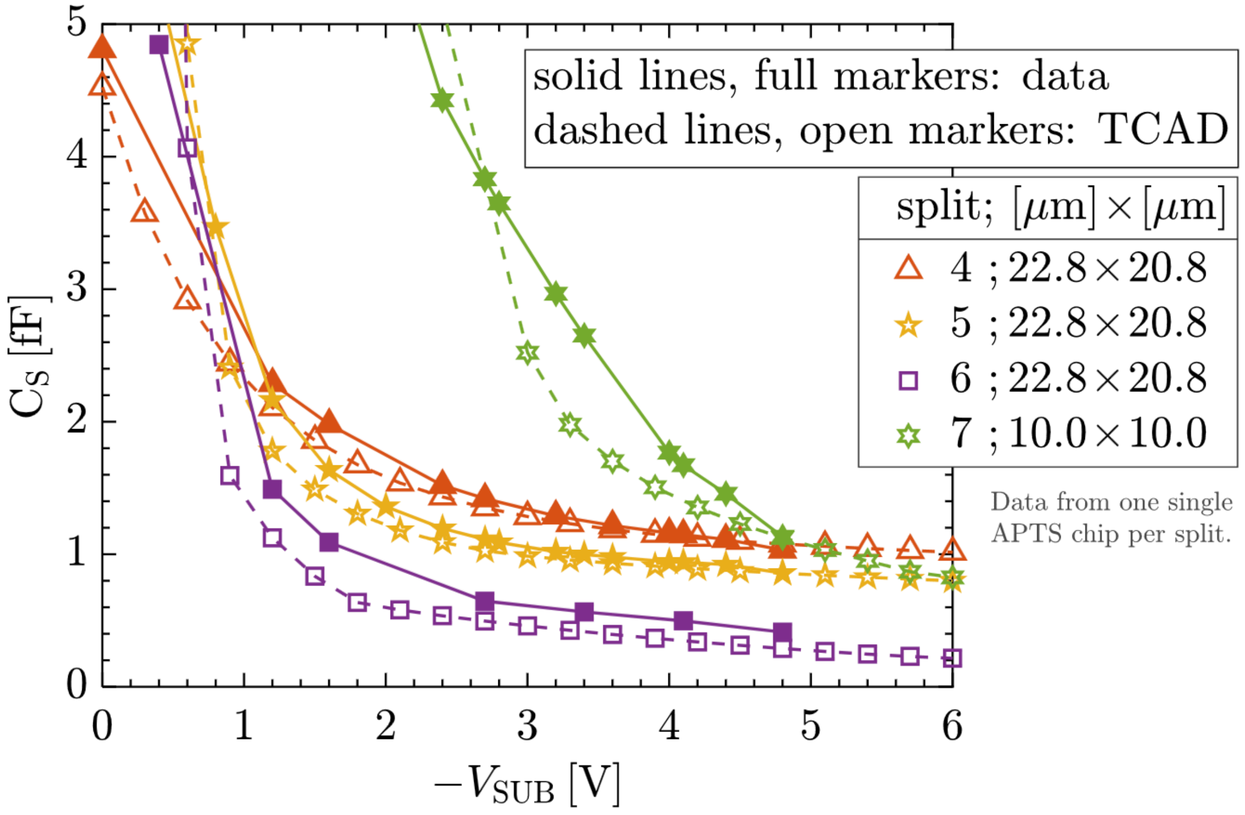
- **Well defined K_α peak signal peak**
  - **Known charge (1640 e^-)**
  - **Can extract pixel capacitance with V = Q/C**



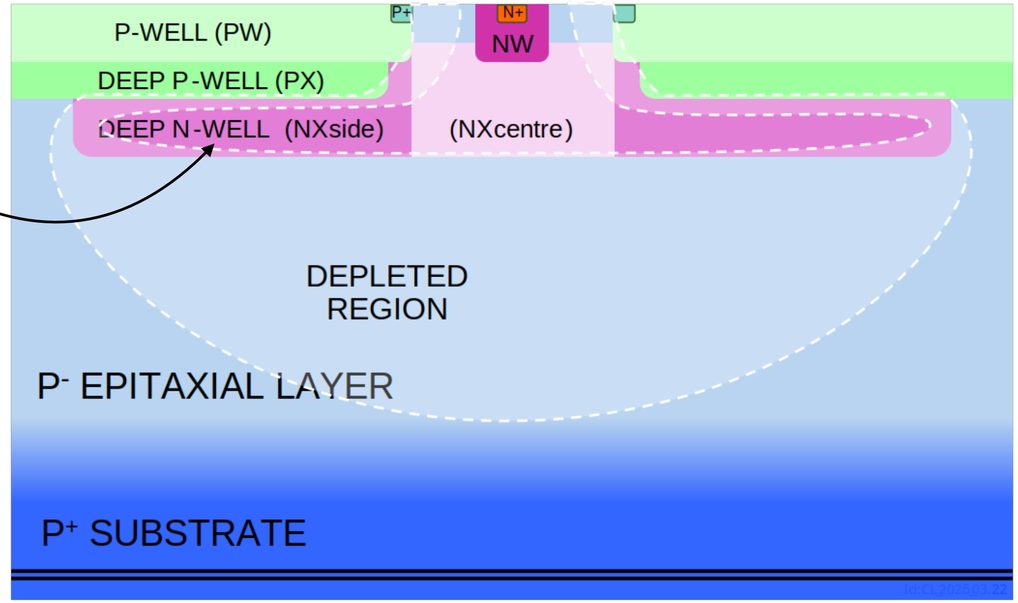
CAPACITANCE COMPARISONS

Low reverse bias

Undepleted deep n-well

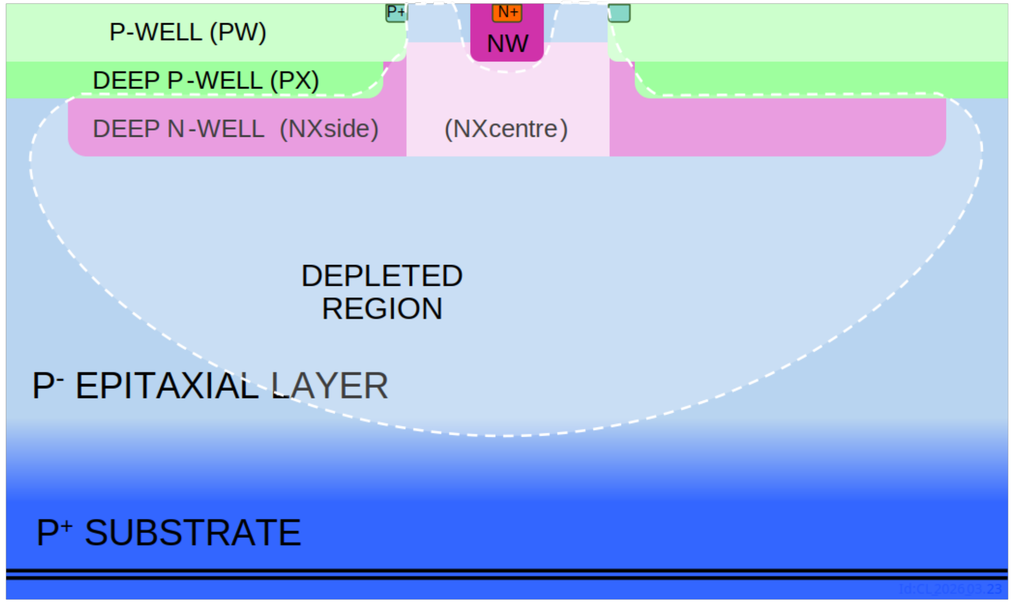


First measurements confirm trends from simulations



High reverse bias

Depleted deep n-well

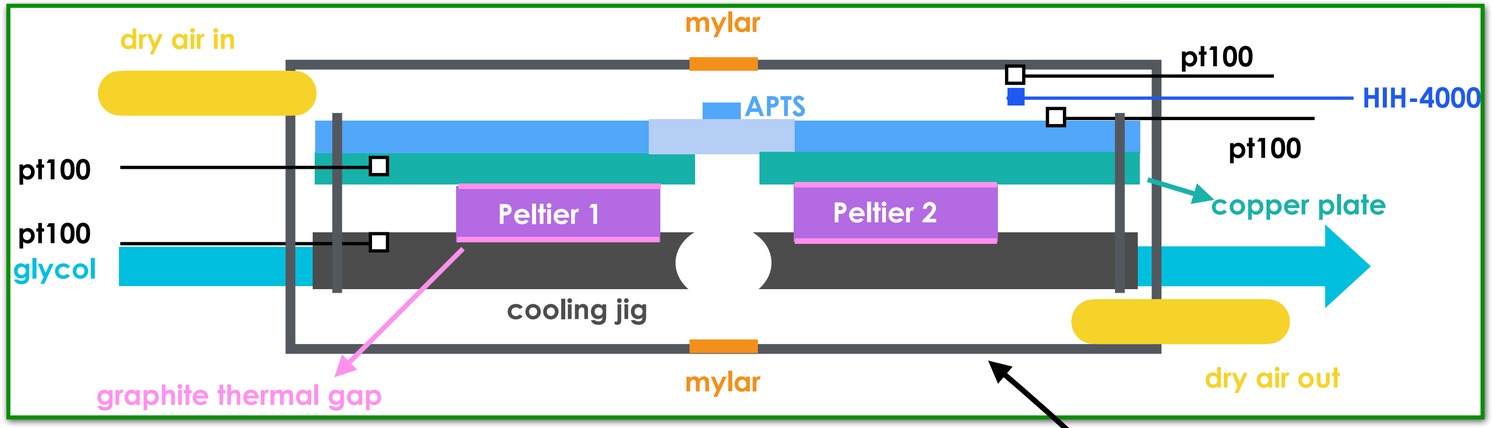


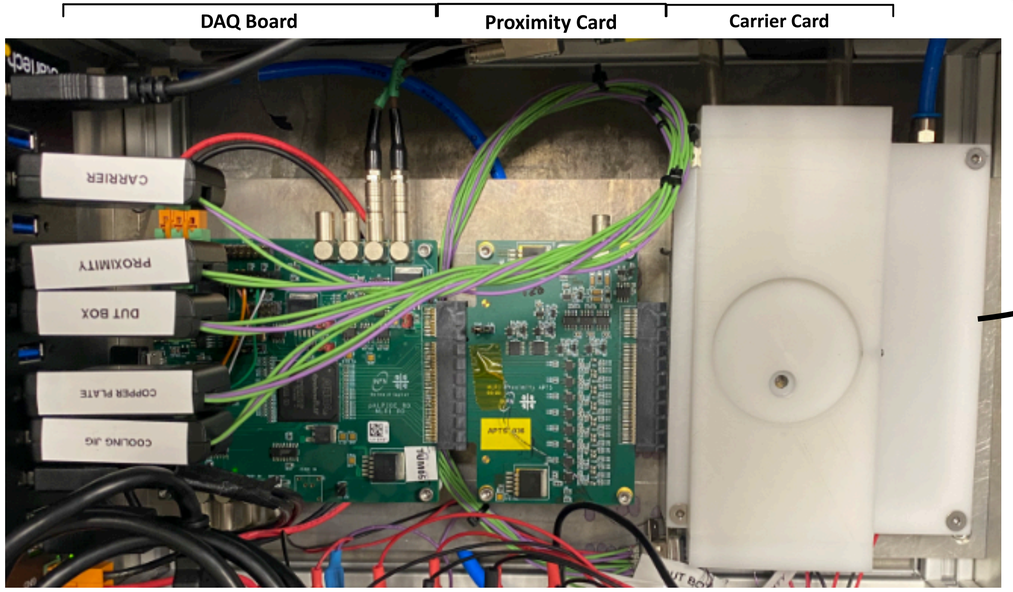
COOLING SETUP

- **Can compensate effects of radiation damage with lower temperatures for VD**
  - **Temperature dependence measurements needed**

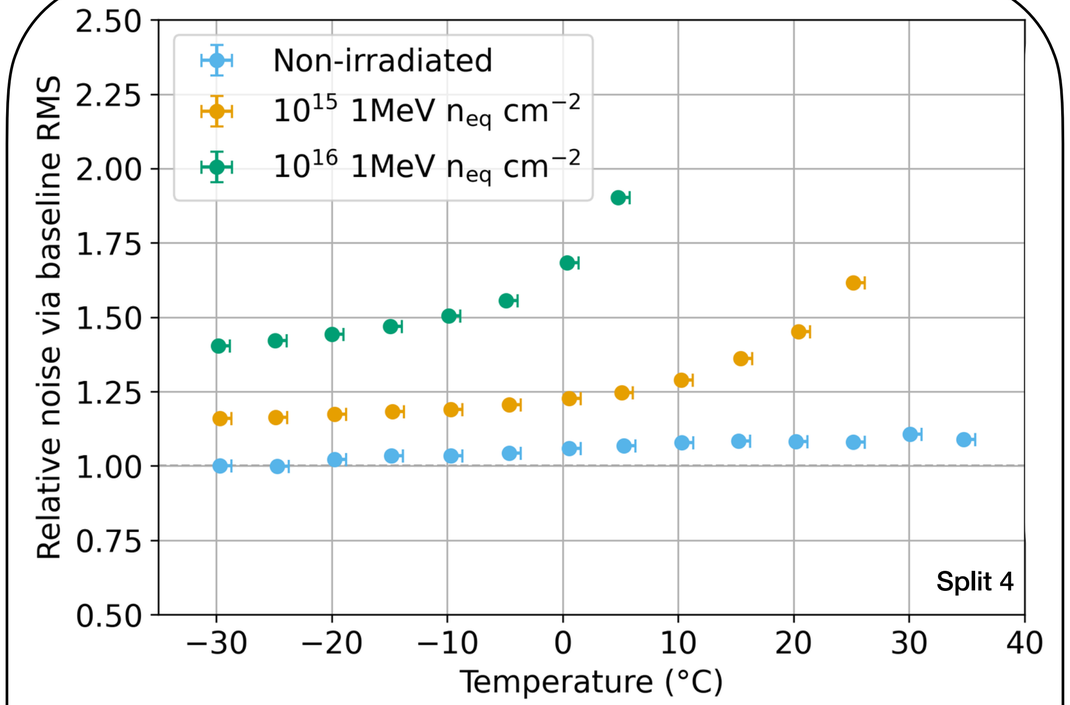
- Cooling box setup:
  - Tight box flushed with dry air
  - APTS on a copper plate, cooled by 2 peltier elements on a chiller-cooled jig
  - PT100 and a humidity sensors monitor conditions inside
  - Mylar windows allow use with testbeam/source measurements
- Temperatures down to -30˚C

E. Dall'Occo: VERTEX 2026





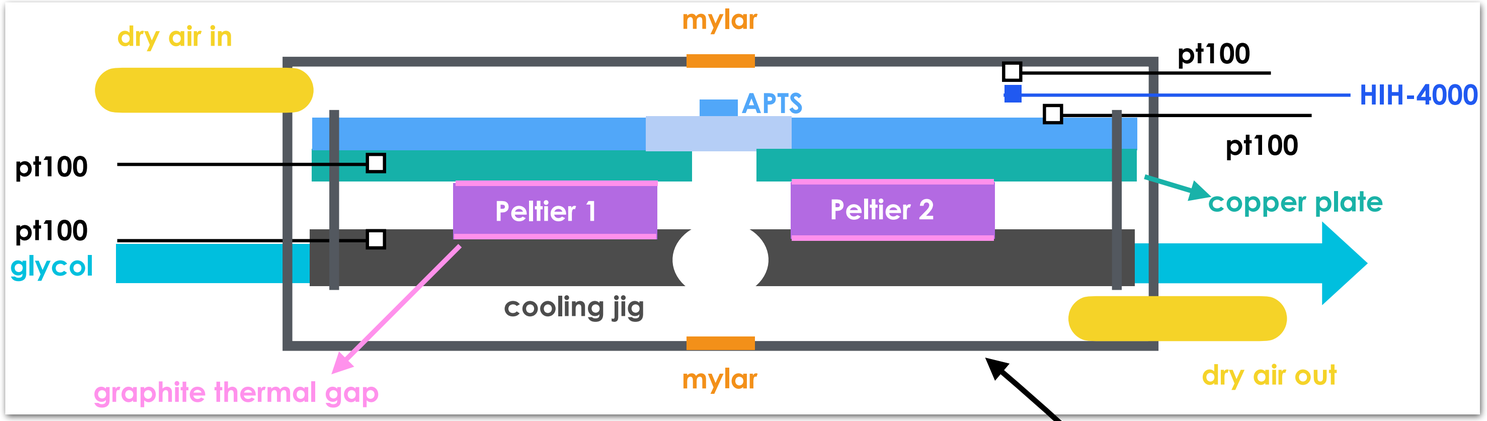
IRRADIATION EFFECTS

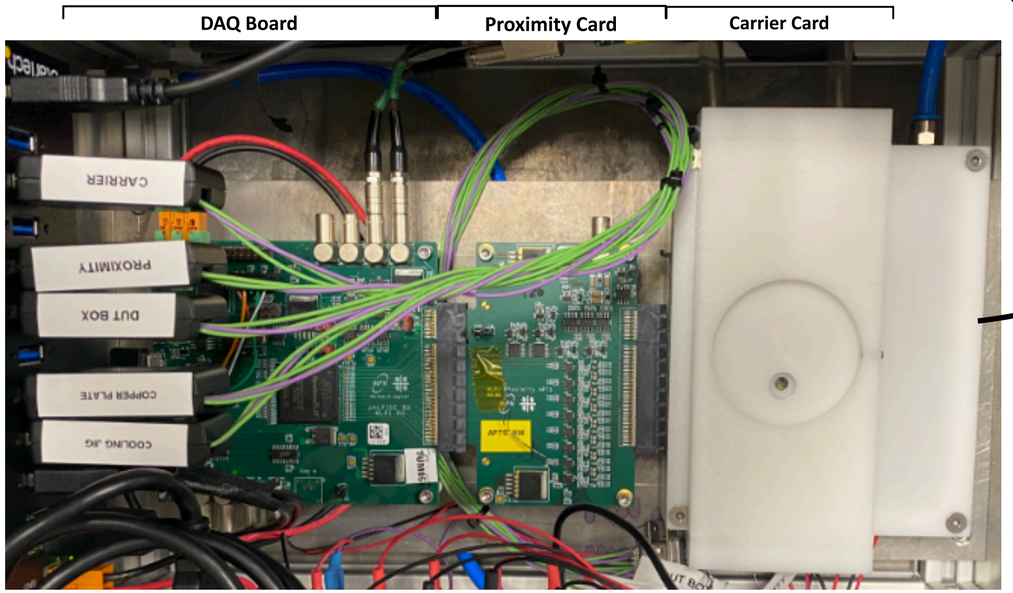


- Sensor operable at high fluence
  - Chips only operable below a certain temperature
  - Cutoff lower with higher irradiation levels
- Noise increases with temperature
  - Sharper increase with higher irradiation levels

➡ **Suggests lower temperatures needed for higher radiation tolerance**

Comparisons with split 7 required and needs to be tested with front-end for full confirmation





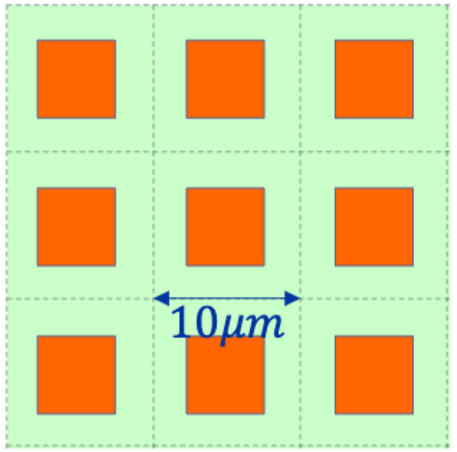
SENSOR DESIGN

APTS campaign with various doping variants and pixel pitches optimised for VD and ML/OT

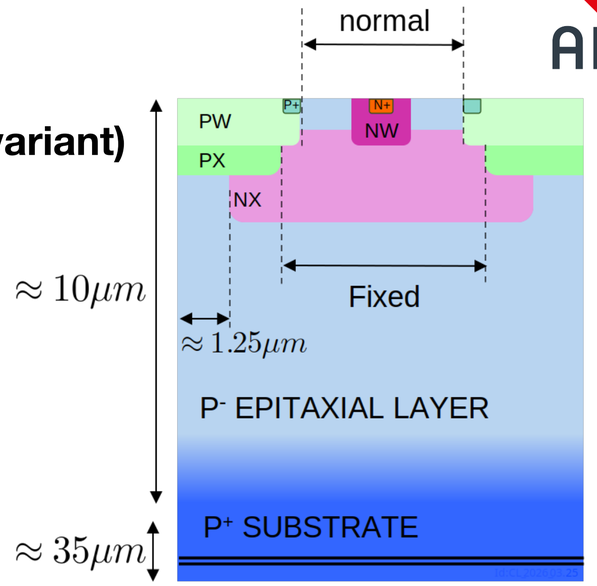
- VD requires 10 μm pitch
  - In baseline layout, the sensor footprint is ~5x5 μm^2 (1/4 of 10 μm pixel area)
  - Smaller footprint required to accommodate needed circuitry

- P5 variant leaves smaller opening around the electrode
  - More room allowed for in-pixel circuitry

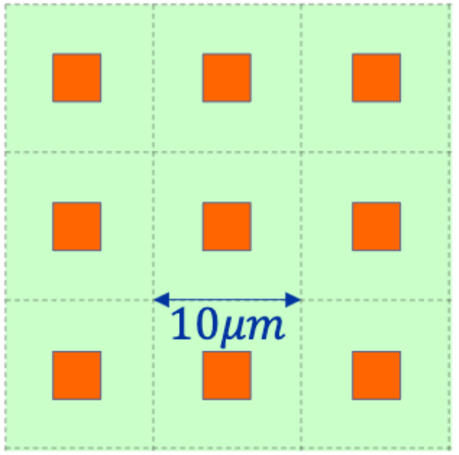
Matrix top view



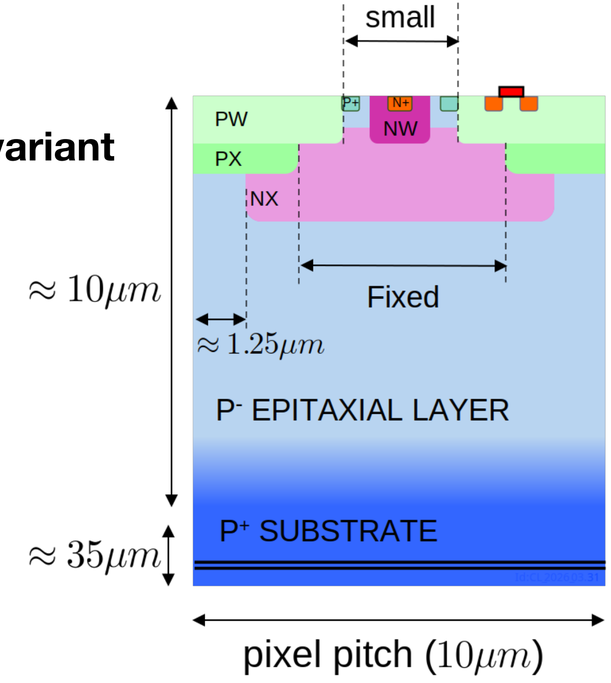
Baseline (G variant)



Matrix top view



P5 variant



Sensor area

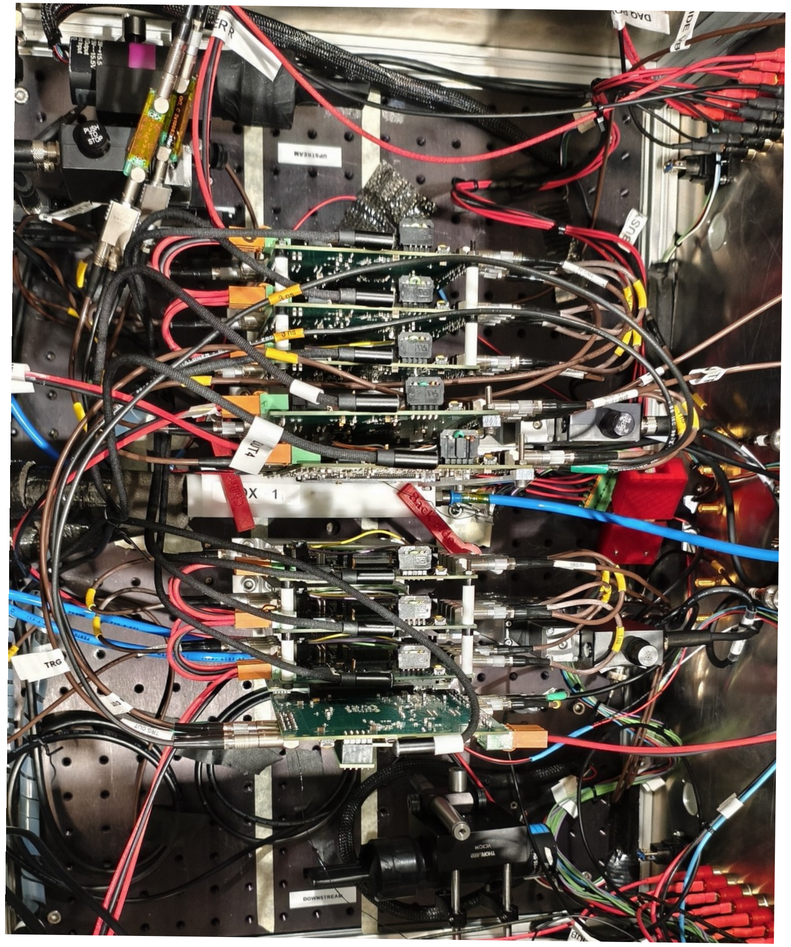
Circuit area

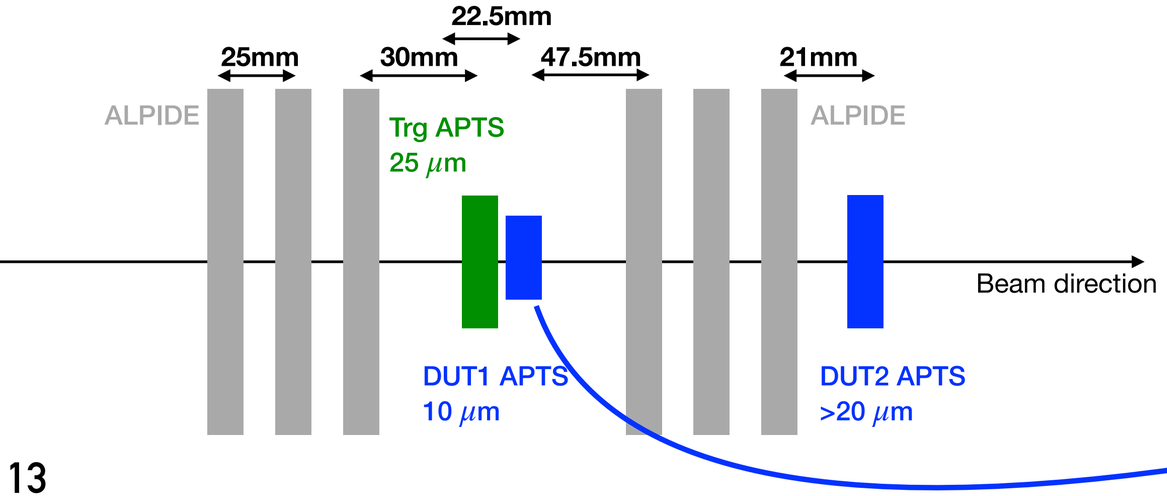
TESTBEAM SETUP

- Results from testbeams at SPS
  - 120 GeV proton beams

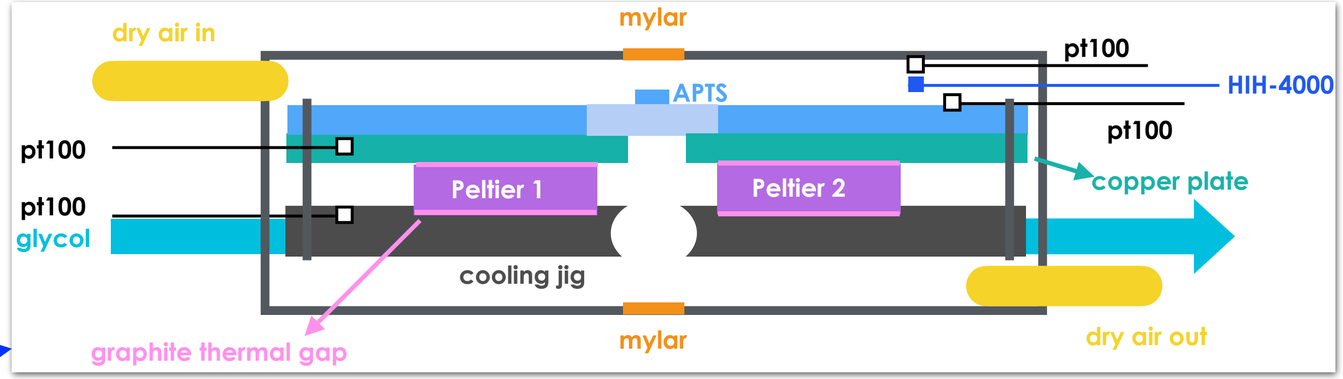
ALPIDE telescope - 3 APTS

- Plane 3 - Trigger APTS
  - On moving stages
  - MLR1 25 μm
- Plane 4 - DUT 1
  - In cold box ranging between -30˚C and 15˚C
  - ER2 10 μm (VD)
- Plane 8 - DUT 2
  - Temperature controlled by chiller
  - ER2 $\geq$20 μm (ML/OT)

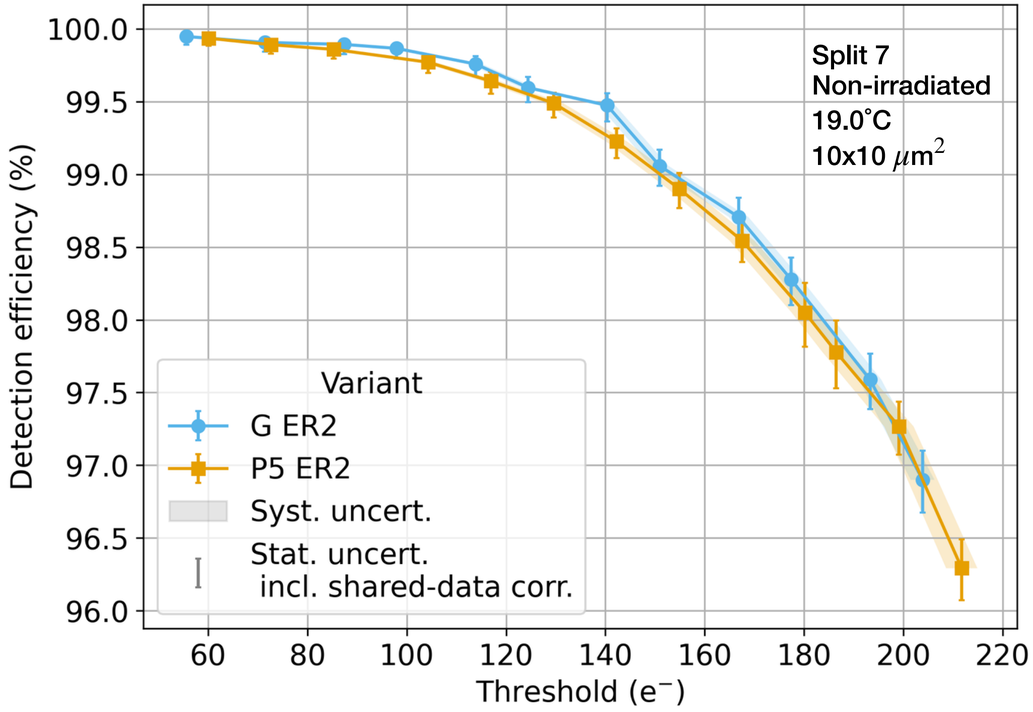


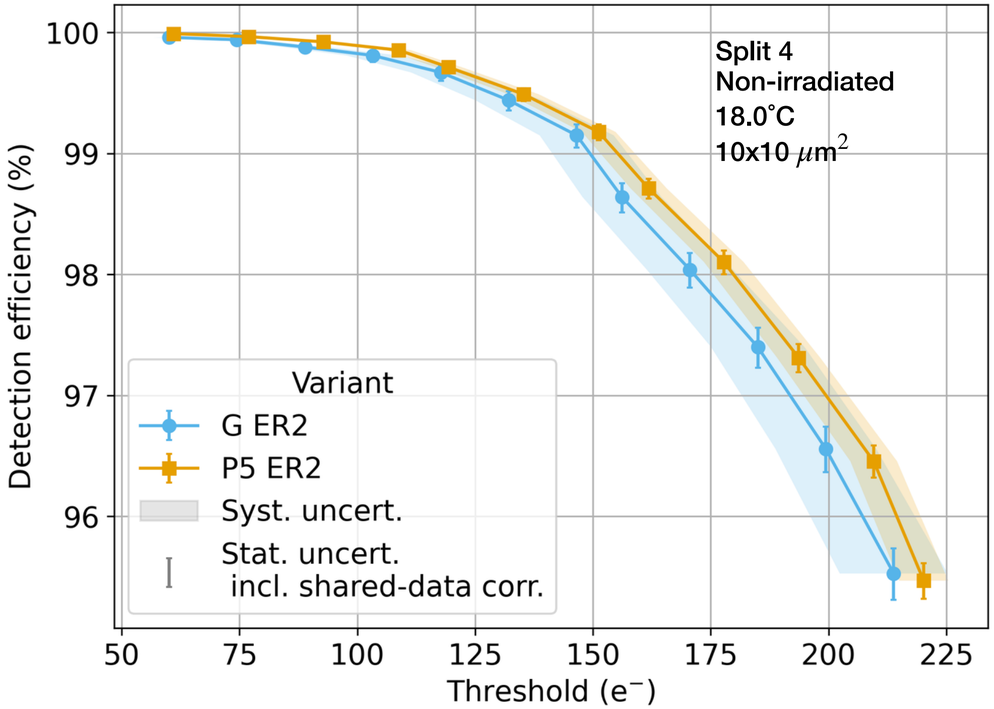


Very compact for use in test beam



SENSOR VARIANT EFFECTS





- **No signs of degradation due to decreasing of electrode opening**
- **Both variants in good agreement for both split 4 and 7**
  - **Comparison underway with irradiated chips**

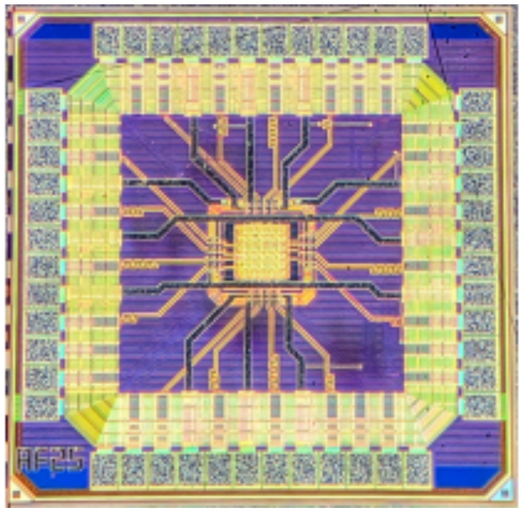
Feasibility of 10μm pitch with space for needed in-pixel circuitry

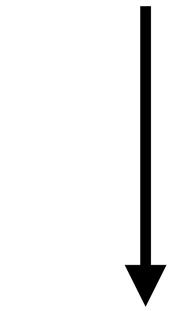
TOWARDS A FULL SENSOR

- Where APTS excels
  - Designed to find optimal pixel design
  - Ideal for single-pixel characterisation
- Where APTS falls short
  - Too few pixels for matrix-level studies
  - No in-pixel front-end
  - No fake-hit rate measurements

- Necessity for larger pixel matrix sensors including in-pixel front-end

  ➡ **Preliminary ALMIRA tapeout first half of 2027**



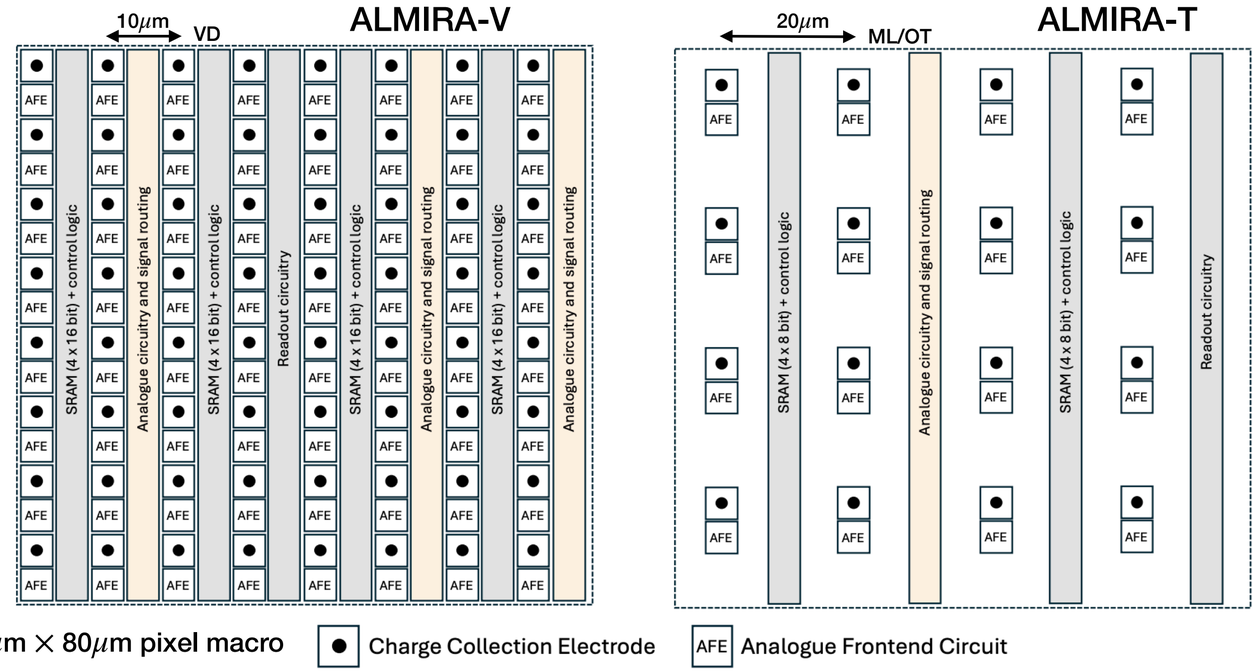


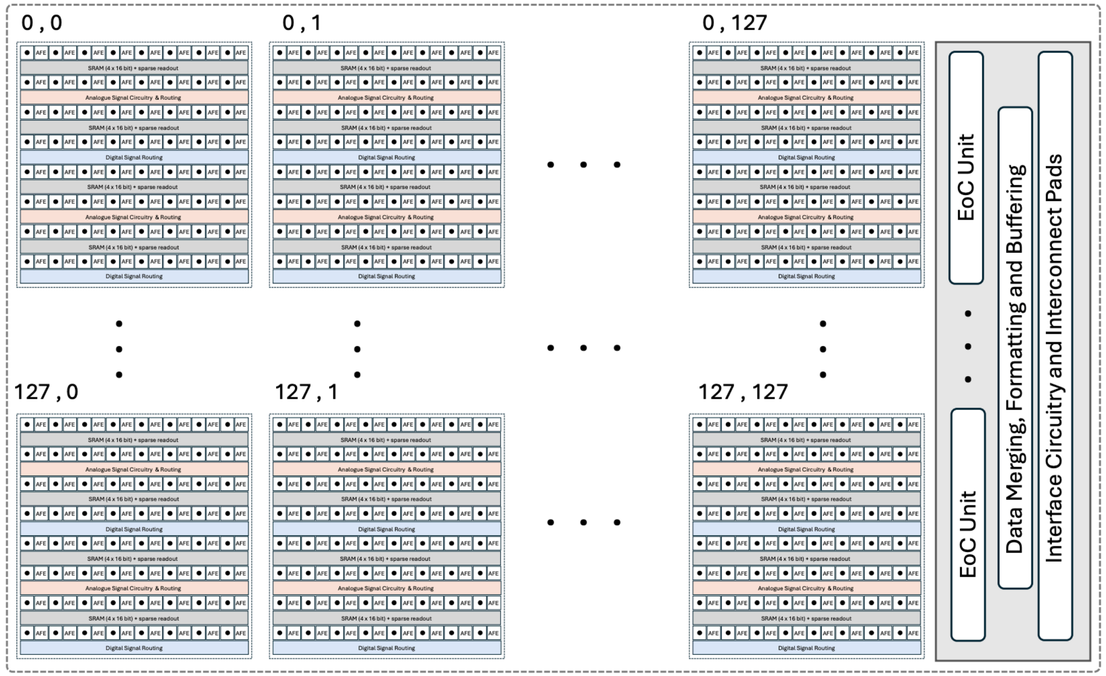


ALMIRA

ALMIRA (ALICE 3 Monolithic Integrated Tracker ASICs) project focused on sensor design, characterisation, production and qualification

- Using MAPS sensors with 65 nm CMOS technology, profiting from ITS3 development
- Common building blocks across ALMIRA-V and -T variants: modular pixel-macro design to have systematic layout and integration
- Matrix cores use unified periphery interface for readout, control, timing



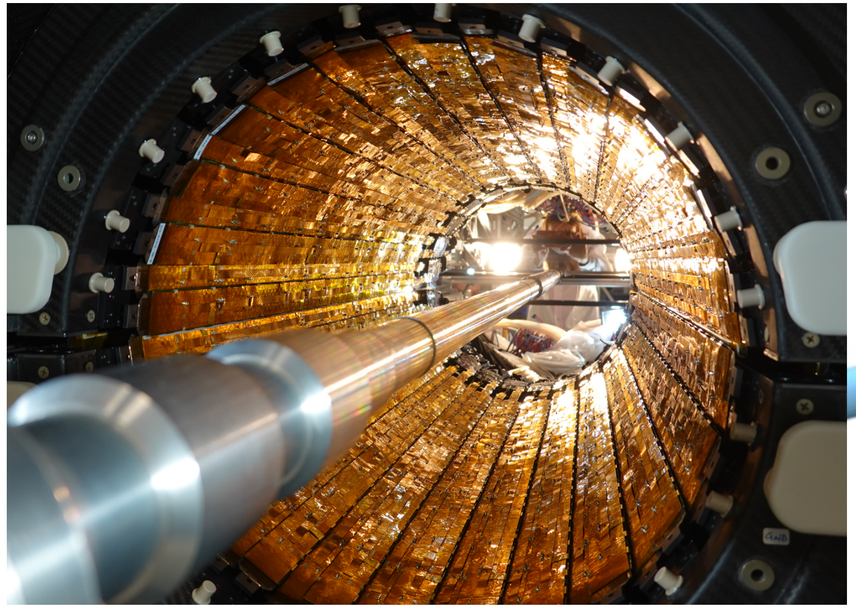


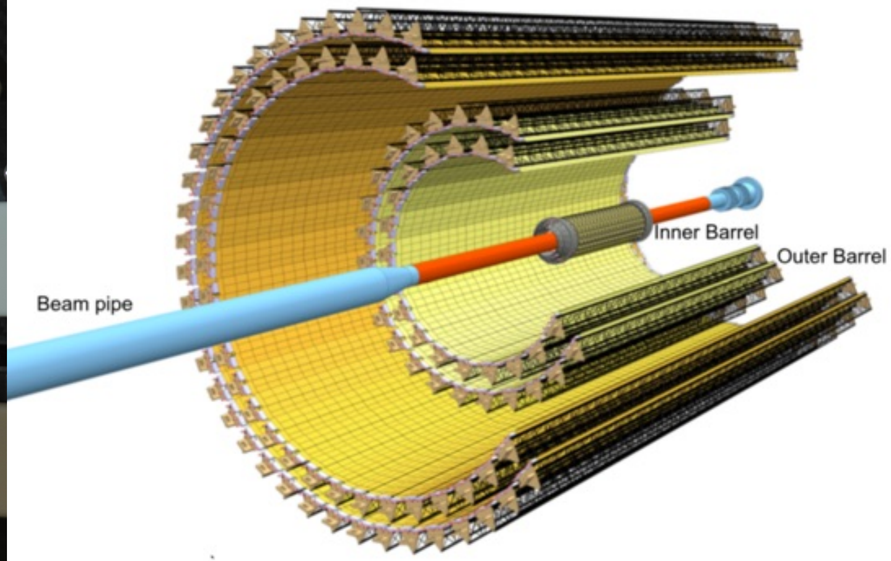
SUMMARY AND OUTLOOK

- ALICE 3 expected to be installed during LHC Long Shutdown 4 (2034-2036)
  - Design and characterisation is already ongoing towards the future ALICE 3 inner & outer tracker sensors
  - ALICE 3 technical design report in the works
- Optimisation for the sensor design is currently ongoing
  - Irradiated chips being tested in-lab and in-beam for the needs of the ALICE 3 vertex detector
  - Efficiency above 99% for both sensor variants
    - Comparison of variants suggest possibility to use 10μm sensors with space for in-pixel circuitry
  - Initial split comparisons show good agreement with design simulation
- Currently in the analysis phase for the tested ALICE 3 design APTS chips with more results to come
- Tapeout of first ALMIRA front-end chips expected first half of 2027

EVOLUTION OF THE ALICE TRACKER

- Currently installed inner tracker in ALICE
- 7 layers of ALPIDE Monolithic Active Pixel Sensors
- 180 nm CMOS fabrication
- Inner three layers
  - 432 sensors: 6 m^2 area



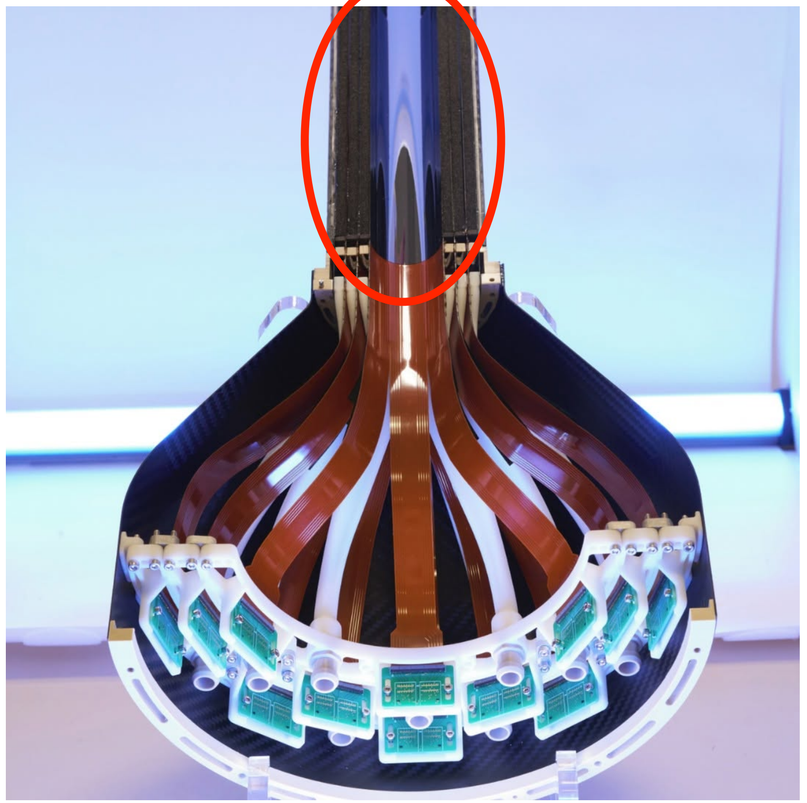


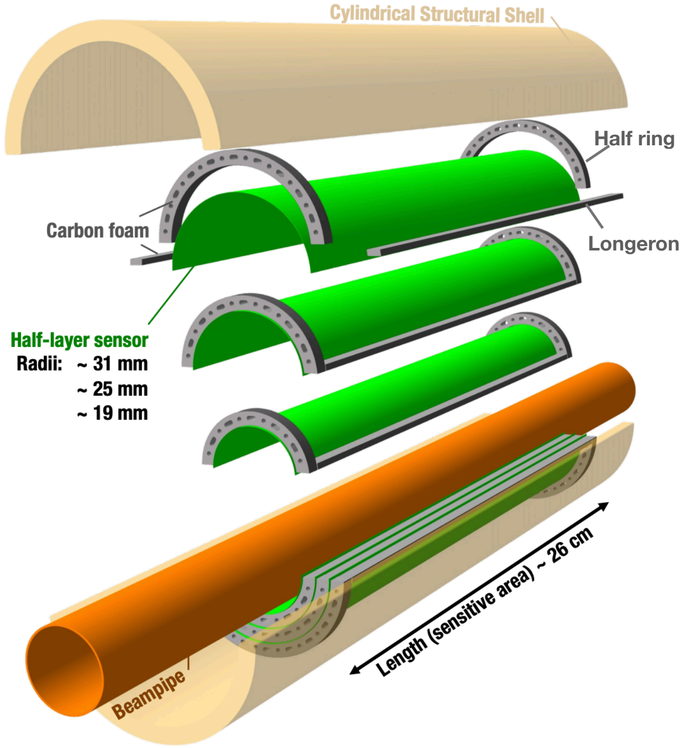


EVOLUTION OF THE ALICE TRACKER

- Inner three barrels of ITS2 to be upgraded to ITS3
- Six self-supporting bent sensors
  - Ultra-thin (50 μm)
  - Air cooling
- 65 nm CMOS fabrication
- Reduction of material budget by ~4x from ITS2

Full motivation, design specifications, and R&D plan found in ITS3 TDR: ALICE-TDR-021





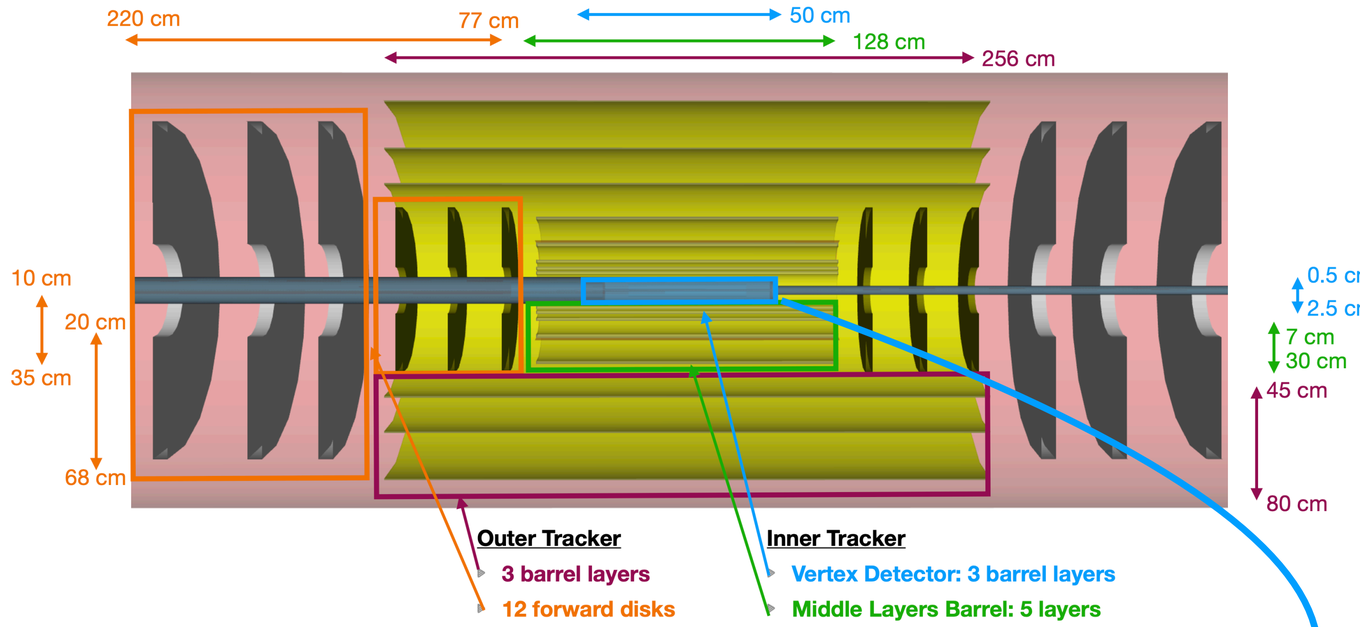


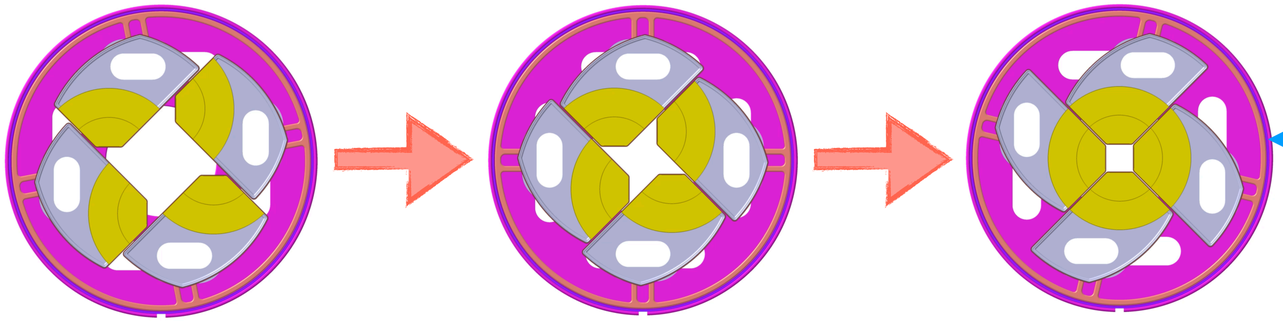
ALICE 3 VERTEX DETECTOR

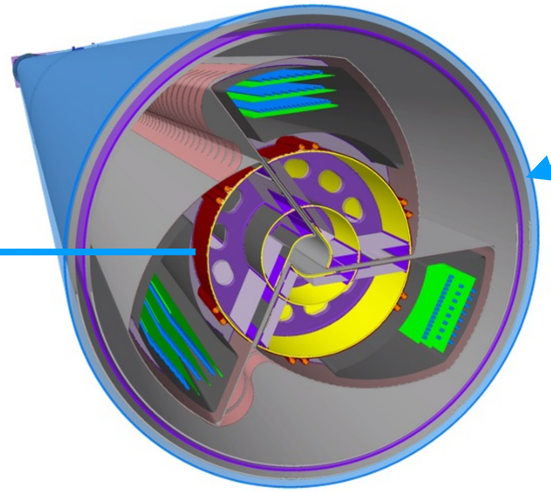
More on this in talk by J. Klein

Vertex Detector IRIS system

- 3 retractable layers of bent sensors on four petals inside the beampipe
  - During LHC beam, layer 0 is at 5mm from interaction point
  - During beam injection, the layers are retracted, layer 0 at 15 mm from interaction point
- 0.1% material budget with 2.5 μm position resolution → 10 μm pixel pitch
- Cooling of negative temperature expected → CO_2 cooling







ALICE 3 MIDDLE LAYERS

More on this in talk by J. Klein

Middle layer barrel

- 5 layers outside the beam pipe
- Current design ITS2-like staves
- 1% material budget with 10 μm position resolution → 50 μm pixel pitch
- Water cooling

