



# 重离子碰撞实验中的硅像素探测器

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- 背景介绍
- CMOS单片有源像素传感器（MAPS）
- MAPS在重离子碰撞实验中的应用
  - ✓ STAR PXL
  - ✓ ALICE ITS2
  - ✓ ALICE ITS3
- MAPS探测器研发进展
- 总结

# 背景介绍 -- 高能重离子碰撞

Pb-Pb 5.36 TeV LHC22s period

- 单次碰撞产生大量粒子 ( $\sim 10^4$ 个)
- 绝大部分为低动量 ( $\sim 0.1 \sim 1$  GeV/c) 的粒子
- 物理上对短寿命粒子感兴趣 ( $\sim 100$ 微米)

→ 要求探测器具备：高分辨率、低物质质量

→ CMOS像素传感器技术!

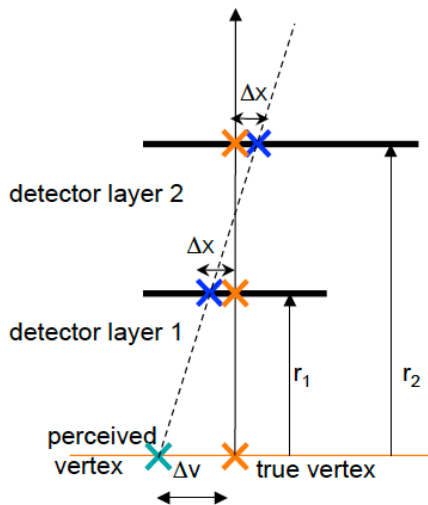
# 背景介绍 -- 像素探测器关键参数

像素探测器的性能参数：

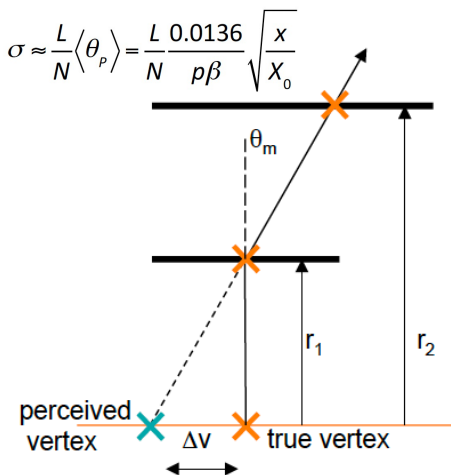
1. 碰撞参数分辨率
2. 动量分辨率
3. 寻迹效率



- 质量
- 固有位分辨率
- 到碰撞点的距离



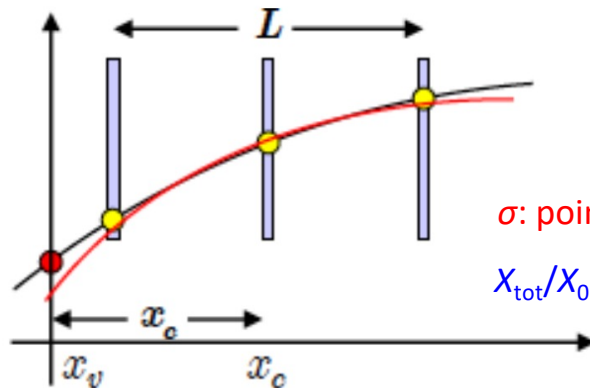
$$\Delta v = \Delta x \cdot \sqrt{\frac{r_2^2 + r_1^2}{(r_2 - r_1)^2}}$$



$$\Delta v = \theta_m \cdot r_1$$

$$\sigma \approx \frac{L}{N} \langle \theta_p \rangle = \frac{L}{N} \frac{0.0136}{p\beta} \sqrt{\frac{x}{X_0}}$$

Ref.: Luciano Musa@HP2023



$\sigma$ : pointing resolution/plane

$X_{tot}/X_0$ : total material budget

Ref.: R.L. Gluckstern, NIMA 24 (1963), 381-389

$$\frac{\Delta p_t}{p_t} = \frac{\sigma [m] p [\text{GeV}/c]}{0.3 B [T] L^2 [m^2]} \sqrt{\frac{720 (N-1)^3}{(N-2) N (N+1) (N+2)}}$$

$$\approx \frac{\sigma [m] p [\text{GeV}/c]}{0.3 B [T] L^2 [m^2]} \sqrt{\frac{720}{N+4}}$$

$$\frac{\Delta p_t}{p_t} = \frac{0.0136}{0.3\beta B [T] L [m]} \sqrt{\frac{X_{tot}}{X_0}} \sqrt{\frac{10}{7} \frac{12 + (N-1)N^2(N+1)}{(N-2)N(N+1)(N+2)}}$$

$$\approx \frac{0.0136}{0.3\beta B [T] L [m]} \sqrt{\frac{X_{tot}}{X_0}} \sqrt{\frac{10}{7}}$$

$$\approx \frac{0.0542}{\beta B [T] L [m]} \sqrt{\frac{X_{tot}}{X_0}}$$

# 背景介绍 -- 像素探测器发展历史

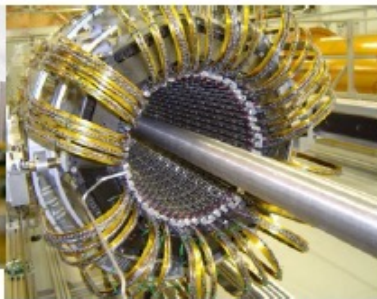
- 1995 – First Hybrid Pixel detector installed in WA97 (CERN, Omega facility)
- 1996/97 – First Collider Hybrid Pixel Detector installed in DELPHI (CERN, LEP)
- Complex systems operated in a challenging high track density environment
- Silicon pixel detectors were installed at the heart of LHC experiments since 2005



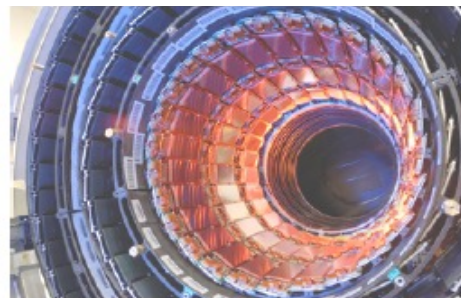
ALICE **Pixel** Detector



LHCb VELO



ATLAS **Pixel** Detector



CMS Strip Tracker IB



CMS **Pixel** Detector



ALICE Drift Detector

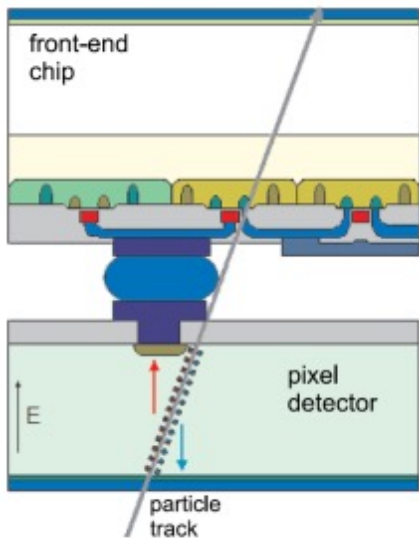


ALICE Strip Detector

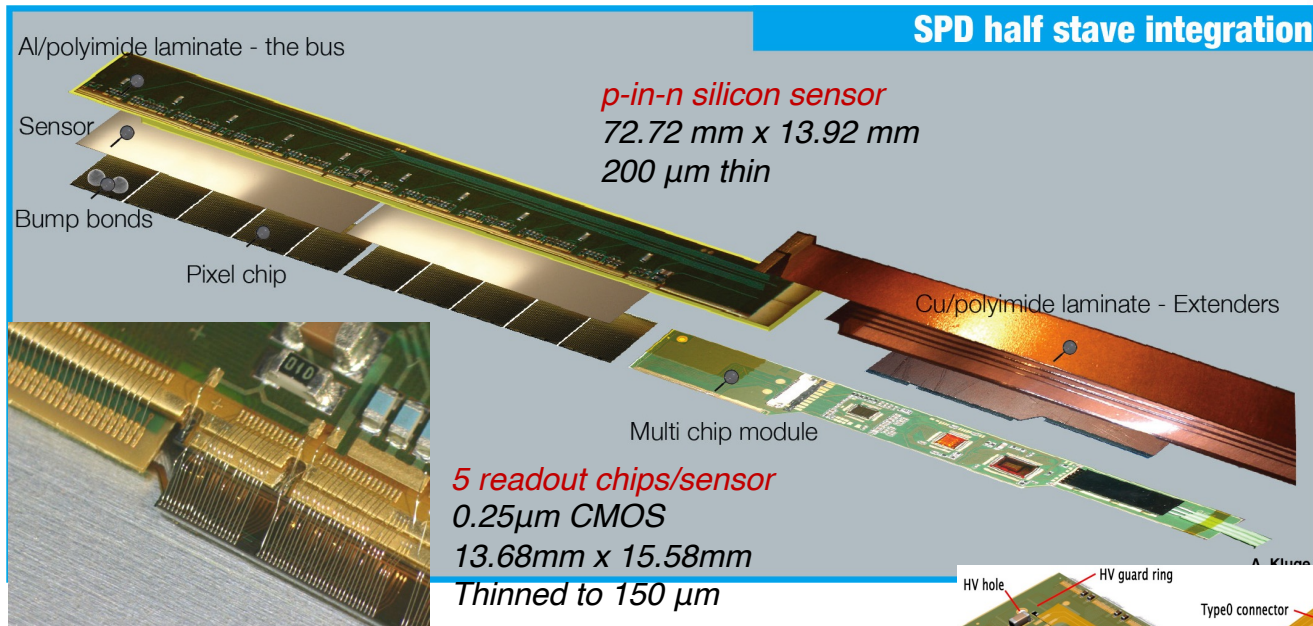


ATLAS SCT Barrel

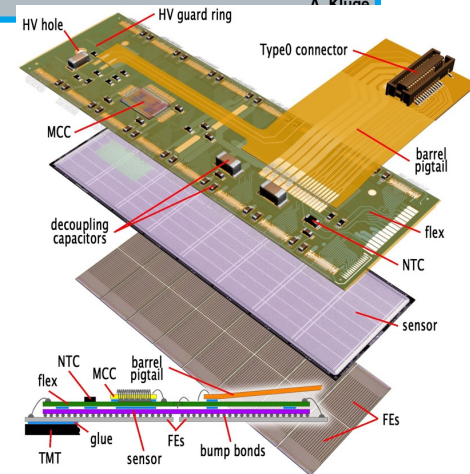
# 背景介绍 -- 像素探测器发展历史



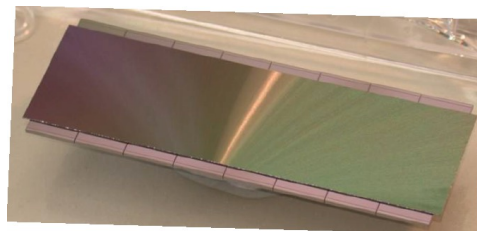
混合式像素传感器 (Hybrid)



ALICE Silicon Pixel Detecor (SPD)



ATLAS Pixel Module



# CMOS单片有源像素传感器 (MAPS)

- Only in the early 2000s proposed for charged particle tracking in HEP
  - Need larger fill factor and better charge collection (higher resistivity substrate)



ELSEVIER

Nuclear Instruments and Methods in Physics Research A 458 (2001) 677–689

NUCLEAR  
INSTRUMENTS  
& METHODS  
IN PHYSICS  
RESEARCH  
Section A

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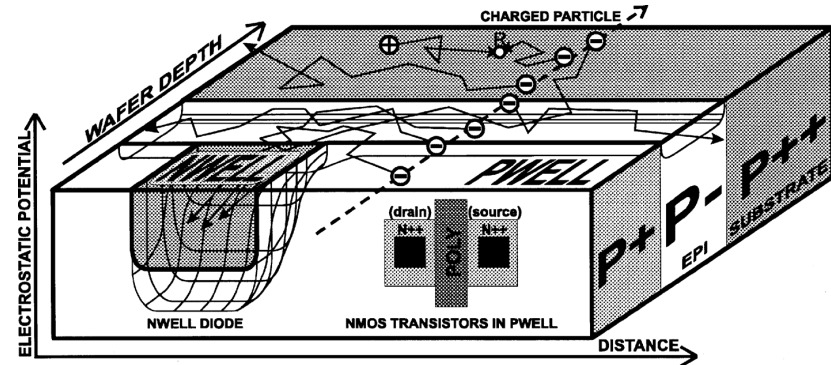
A monolithic active pixel sensor for charged particle tracking and imaging using standard VLSI CMOS technology

R. Turchetta<sup>a,\*</sup>, J.D. Berst<sup>a</sup>, B. Casadei<sup>a</sup>, G. Claus<sup>a</sup>, C. Colledani<sup>a</sup>, W. Dulinski<sup>a</sup>, Y. Hu<sup>a</sup>, D. Husson<sup>a</sup>, J.P. Le Normand<sup>a</sup>, J.L. Riester<sup>a</sup>, G. Deptuch<sup>b,1</sup>, U. Goerlach<sup>b</sup>, S. Higuere<sup>b</sup>, M. Winter<sup>b</sup>

<sup>a</sup>LEPSI, IN2P3/ULP, 23 rue du Loess, BP20, F-67037 Strasbourg, France

<sup>b</sup>IReS, IN2P3/ULP, 23 rue du Loess, BP20, F-67037 Strasbourg, France

doi:10.1016/S0168-9002(00)00893-7



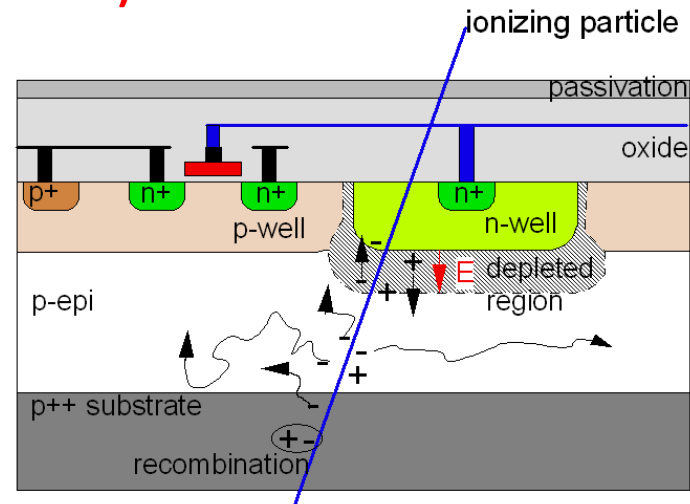
Integration of a sensor in 0.6  $\mu\text{m}$  process

- Twin (P and N) wells
- Implanted in lightly doped (P-) epitaxial layer
- Grown on top of the highly doped (P<sup>++</sup>) substrate

Charge collection diode is made of the junction between the NWELL and P-type epitaxial layer

## MIMOSA-family sensor developed for STAR/HFT (First application in HEP!)

- AMS 0.35  $\mu\text{m}$  CMOS, Twin-well process
- ‘High’ resistivity ( $\geq 400 \Omega \cdot \text{cm}$ ) p-epi layer ( $\sim 15 \mu\text{m}$ )
  - Reduced **charge collection time**
  - Improved **radiation hardness** (up to  $10^{12} \text{ 1MeV N}_{\text{eq}}/\text{cm}^2$ )
- Charge collection by diffusion (mostly) and drift
  - **Shallow depletion** region formed between n-well and p-epi
  - High-potential difference between lightly-doped epi and substrate



- NMOS only in pixel array
- **Rolling-shutter** readout architecture
- Clock distributed across the matrix, in-pixel amplifier



### Key Features:

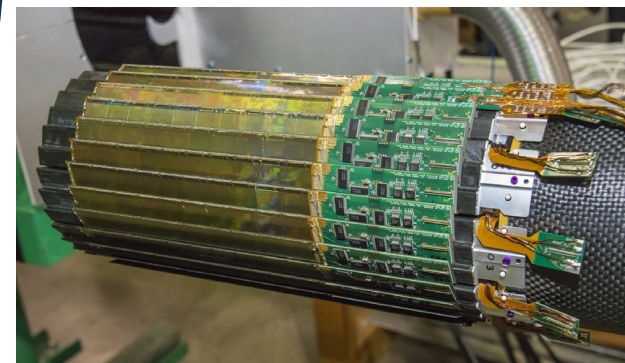
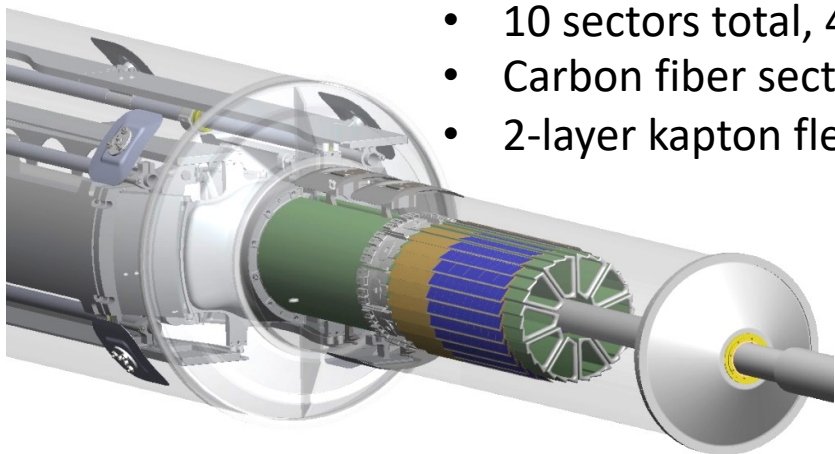
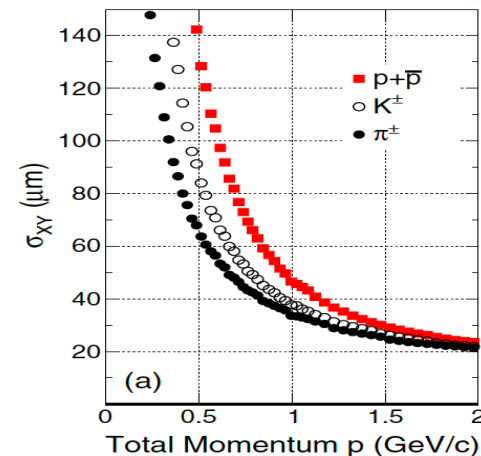
- ⊙ Dimensions: **20mm x 22.7mm x 50 $\mu\text{m}$**
- ⊙ Pixel pitch: **20.7 $\mu\text{m}$  x 20.7 $\mu\text{m}$**
- ⊙ Spatial resolution:  **$\sim 3.7 \mu\text{m}$  (3D)**
- ⊙ Integration time:  **$\sim 185.6 \mu\text{s}$**
- ⊙ Ultra-low power (entire chip):  **$< 170\text{mW}/\text{cm}^2$**
- ⊙ Sensor efficiency:  **$\geq 99\%$  with accidental rate  $\leq 10^{-4}$**



Ladder with 10 MAPS sensors ( $\sim 2 \times 2 \text{ cm}^2$  each)



- 400 sensors (356M pixels,  $0.16 \text{ m}^2$ )
- 2 layers (2.8 cm and 8 cm)
- $0.4\% X_0$  per layer
- 10 sectors total, 4 ladders/sector
- Carbon fiber sector tubes ( $\sim 200 \mu\text{m}$  thick)
- 2-layer kapton flex cable with AL traces



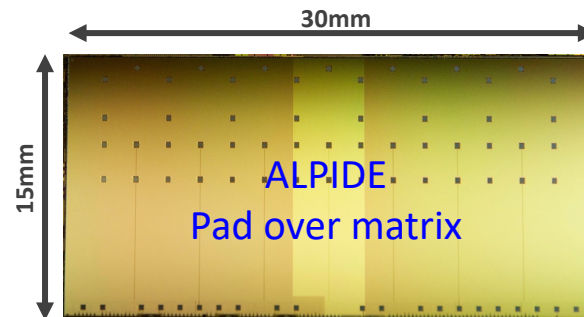
Mechanical support with kinematic mounts (insertion side)

[doi:10.1016/j.nima.2018.03.003](https://doi.org/10.1016/j.nima.2018.03.003)

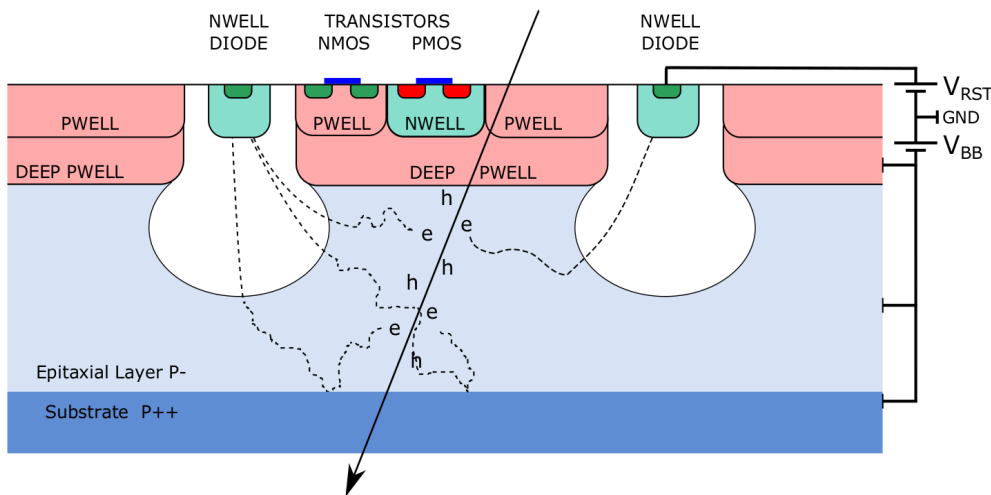
Ref.: L. Greiner (LBL) / CPIX-2014

## ALPIDE produced using TowerJazz 180nm CMOS Imaging Sensor process

- ✓ Quadruple-well process
- ✓ High-resistivity ( $>1 \text{ k}\Omega\cdot\text{cm}$ ) p-type epi-layer ( $\sim 25 \mu\text{m}$ )
- ✓ Small n-well diode ( $2 \mu\text{m}$  diameter)
- ✓ Deep PWELL shields NWELL of PMOS transistors, allowing for full CMOS circuitry within active area
- ✓ Reverse bias voltage to substrate to increase the NIEL tolerance beyond  $10^{13} \text{ 1MeV N}_{\text{eq}}/\text{cm}^2$
- ✓ Low-power hit-driven read-out

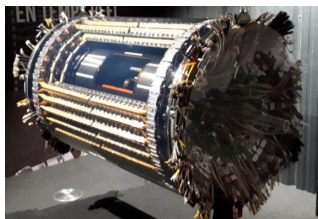


1024×512 pixels

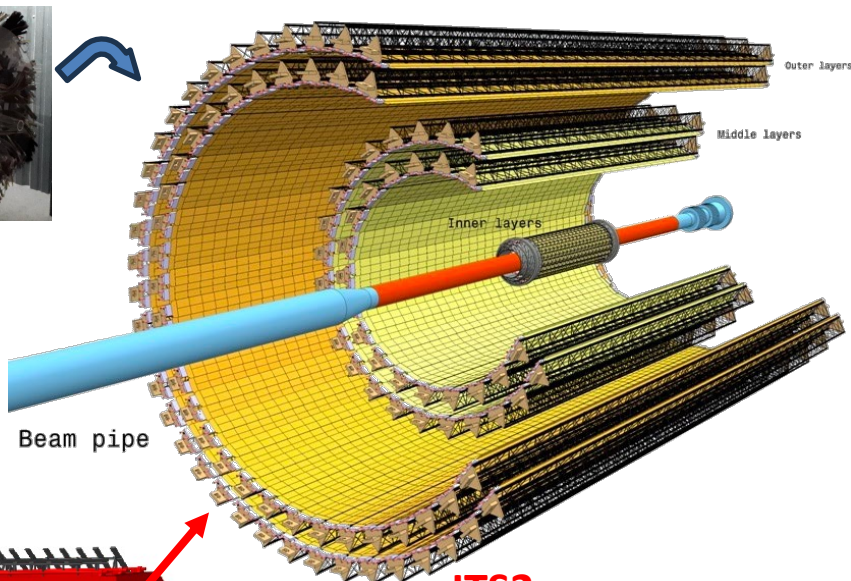


## Key Features:

- ⊙ Dimensions: **30mm x 15mm x 50 (100)  $\mu\text{m}$**
- ⊙ Pixel pitch:  **$29\mu\text{m} \times 27\mu\text{m}$**
- ⊙ Spatial resolution:  **$\sim 5 \mu\text{m}$  (3-D)**
- ⊙ Fake-hit rate:  **$\sim 10^{-10}$  pixel/event**
- ⊙ Ultra-low power (entire chip):  **$< 40\text{mW}/\text{cm}^2$**
- ⊙ Global shutter: **triggered acquisition (200 kHz) or continuous (integration time  $< 4\mu\text{s}$ )**



ITS1



ITS2

7 layers of MAPS  
12.5G pixels  
10 m<sup>2</sup> active area

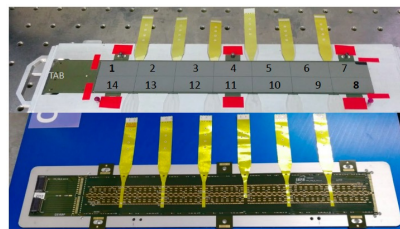
- Monolithic Active Pixel Sensor (MAPS), ALPIDE (~24k chips)
- 5  $\mu\text{m}$  impact parameter resolution
- 7 cylinders covering ~10 m<sup>2</sup> area
- Innermost radius: 23 mm
- Inner Barrel (IB)
  - 3 Inner Layers (48x 9-chip Staves)
  - ~0.35%  $X_0$  material budget
- Outer Barrel (OB)
  - 2 Outer Layers (90x 14-HIC Staves)
  - 2 Middle Layers (54x 8-HIC Staves)
  - ~0.8%  $X_0$  material budget
- 100 kHz trigger rate

**Inner Barrel (IB)**  
 Material thickness:  $\sim 0.35\% X_0$   
 Readout speed: 1200 Mbps  
 $\langle \text{radius} \rangle$  (mm): 23, 31, 39  
 Nr. staves: 12, 16, 20  
 Nr. chips: 432  
**Assembled and validated at CERN**

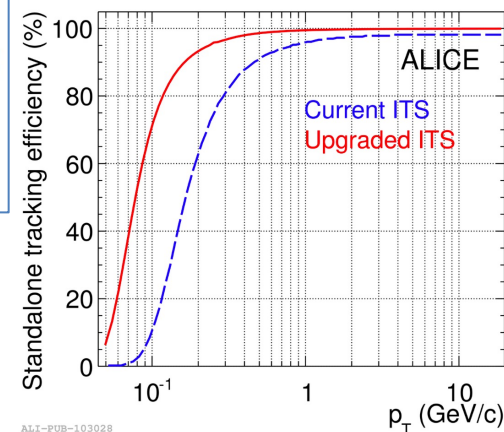
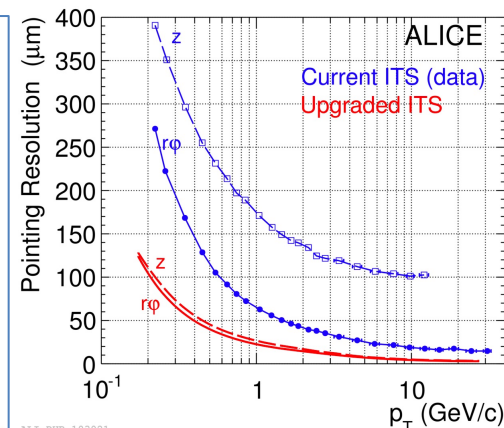


IB HIC模块

**Outer Barrel (OB) – Middle Layers and Outer Layers**  
 Nr. modules/stave: 4 (ML), 7 (OL)     $\langle \text{radius} \rangle$  (mm): 194, 247, 353, 405  
 Material thickness:  $\sim 1\% X_0$     Readout speed: 400 Mbps  
 Power density  $\sim 40\text{mW}/\text{cm}^2$     Length (mm): 844 (ML), 1478 (OL)  
 Nr. staves: 24, 30, 42, 48    Nr. Chips: 6048 (ML), 17740(OL)  
**Assembled at Berkeley, Daresbury, Frascati, Nikhef, Torino, Bari, Liverpool, Pusan, Strasbourg and Wuhan**



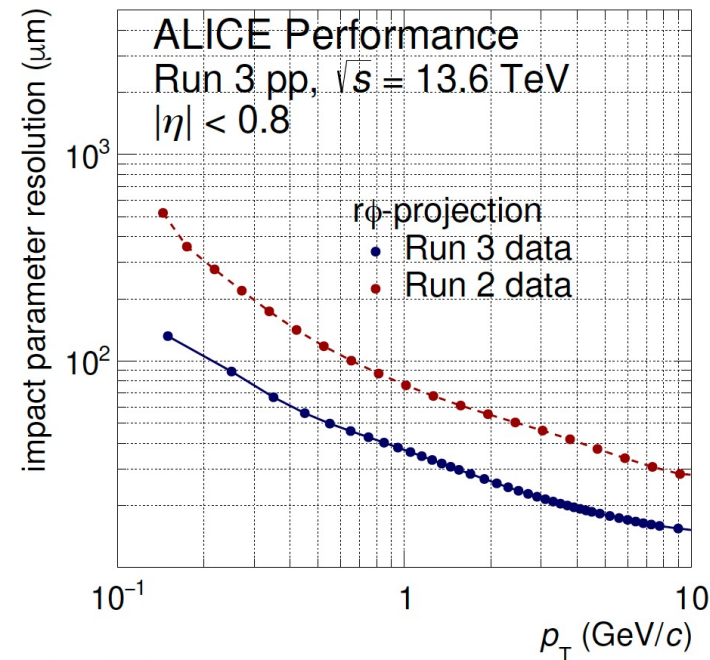
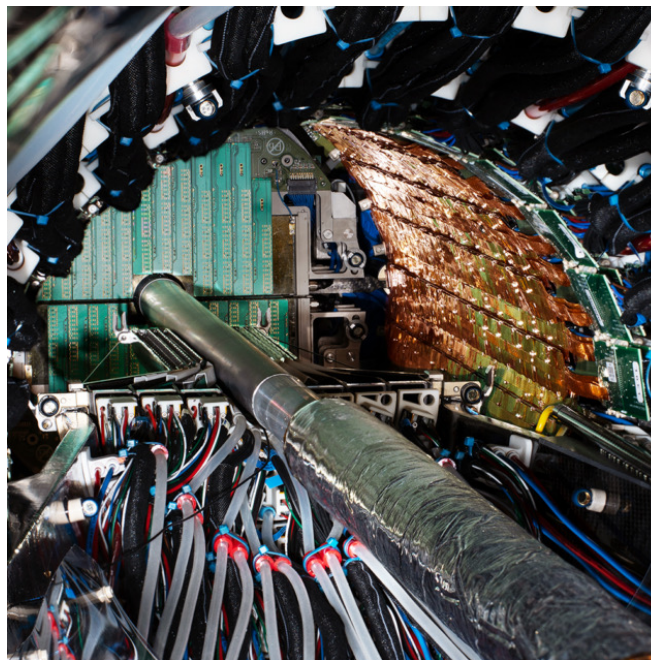
OB HIC模块





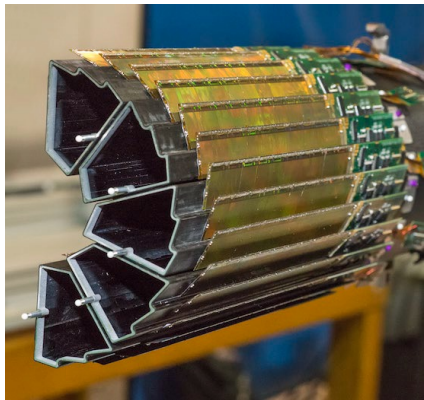
The outer barrel of ALICE ITS2 installed in March, 2021

Ref.: Magnus Mager@QM2025



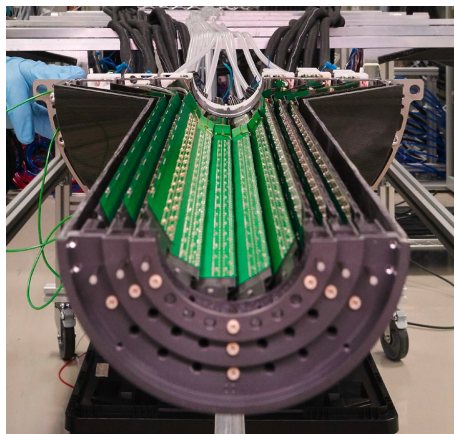
- ✓ Introducing the MAPS tracker, ALICE significantly improved its tracking performance
- ✓ improved several measurements and access new channels

# Next development of MAPS pixel detector



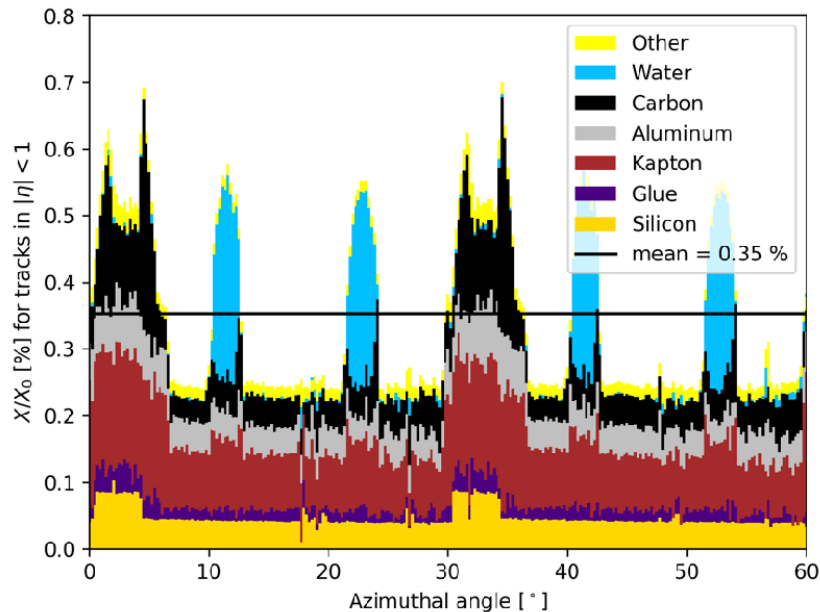
## ALICE ITS2 (2021 -2025)

Material: 0.35%  $X_0$   
 Minimum radius: 2.3 cm  
 Pixel pitch:  $\sim 30 \mu\text{m}$



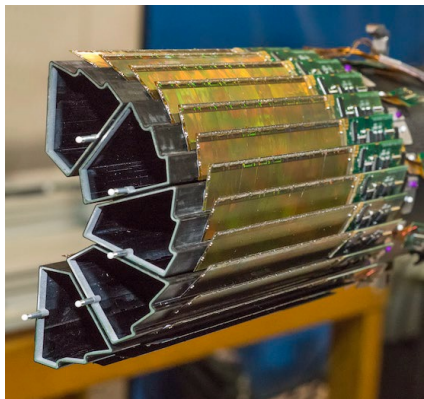
## STAR HFT (2014-2016)

Material: 0.4%  $X_0$   
 Minimum radius: 2.8 cm  
 Pixel pitch:  $\sim 21 \mu\text{m}$



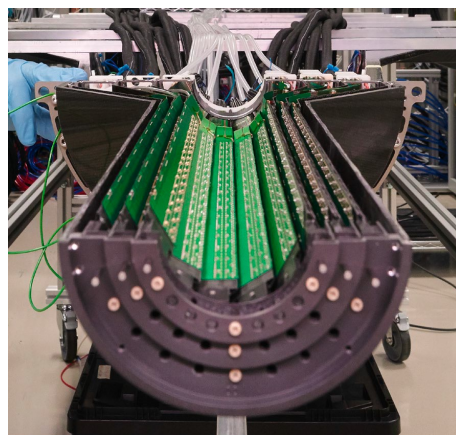
- Can the material be further reduced?
- Can we get closer to the interaction point?

# ALICE ITS3: Stitching MAPS



## ALICE ITS2 (2021 -2025)

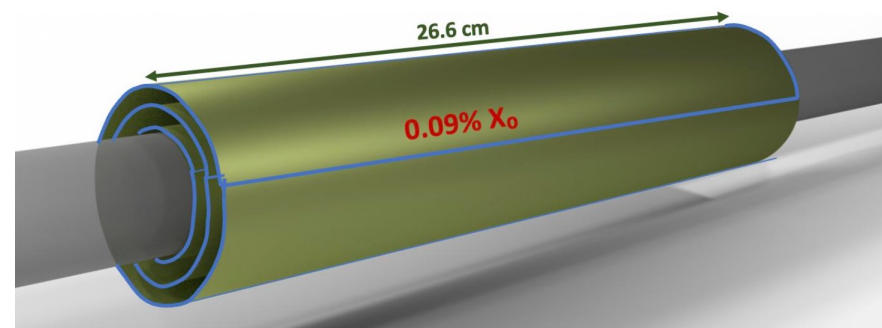
Material: 0.35%  $X_0$   
Minimum radius: 2.3 cm  
Pixel pitch:  $\sim 30 \mu\text{m}$



## STAR HFT (2014-2016)

Material: 0.4%  $X_0$   
Minimum radius: 2.8 cm  
Pixel pitch:  $\sim 21 \mu\text{m}$

A truly-cylindrical, 'silicon-only' detector to achieve unprecedented tracking performance at low  $p_T$

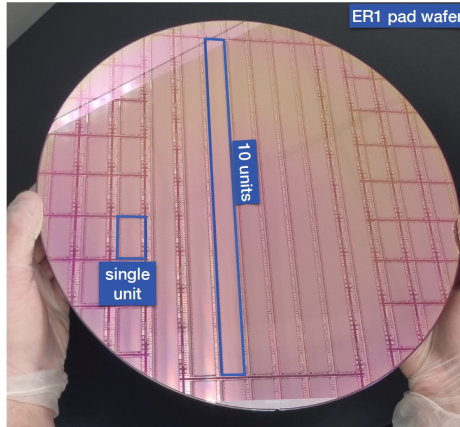
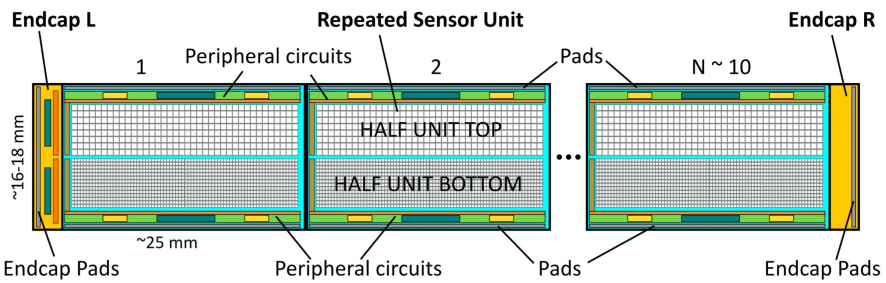


## ALICE ITS3 (2027 - ?)

Material: 0.09%  $X_0$   
Minimum radius: 1.9 cm  
Pixel pitch:  $< 25 \mu\text{m}$

# ALICE ITS3: Stitching MAPS

65nm CMOS Imaging process  
MOSAIX

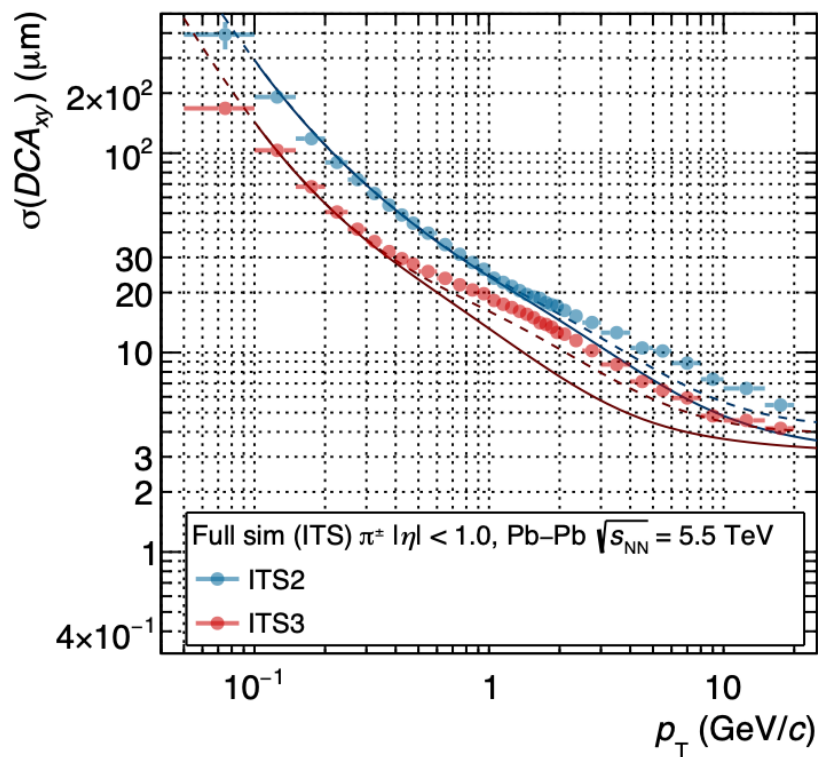


- Large wafer-scale ultra-thin sensor – 6 sensors
- Truly cylindrical – bent sensor
- No FPC for data, power – everything on silicon
- 0.09%  $X/X_0$

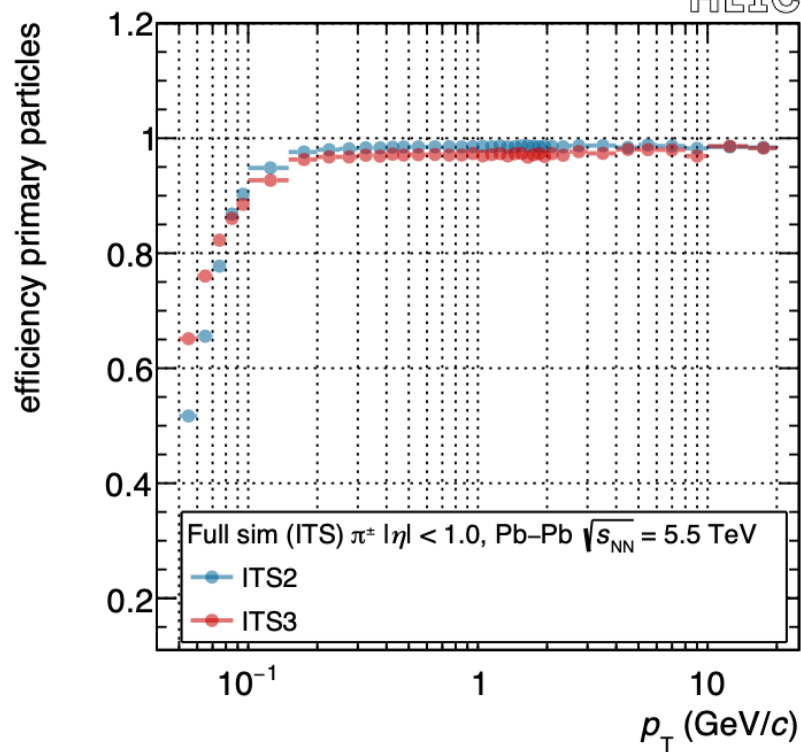
- Ultra-light self supporting mechanics
- No stave
- Air cooling

**First time in a High Energy Physics experiment!**

Ref. S. Siddhanta @ SQM 2026



✓ improvement of factor 2 over all momenta

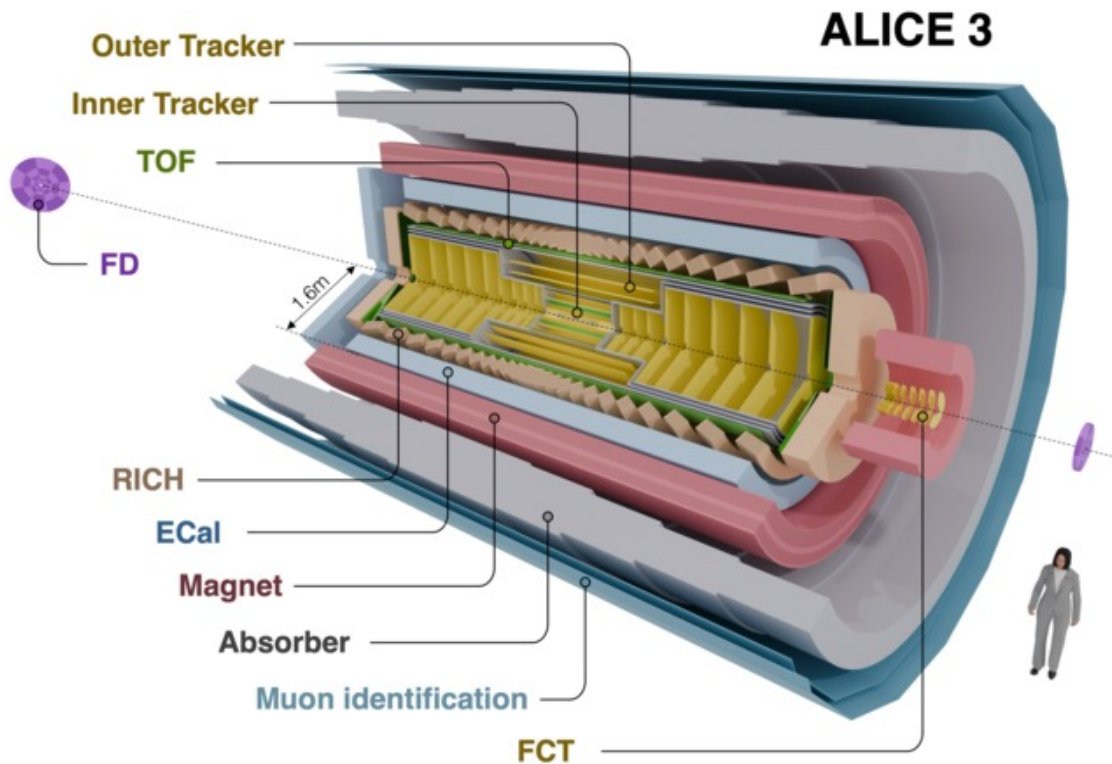
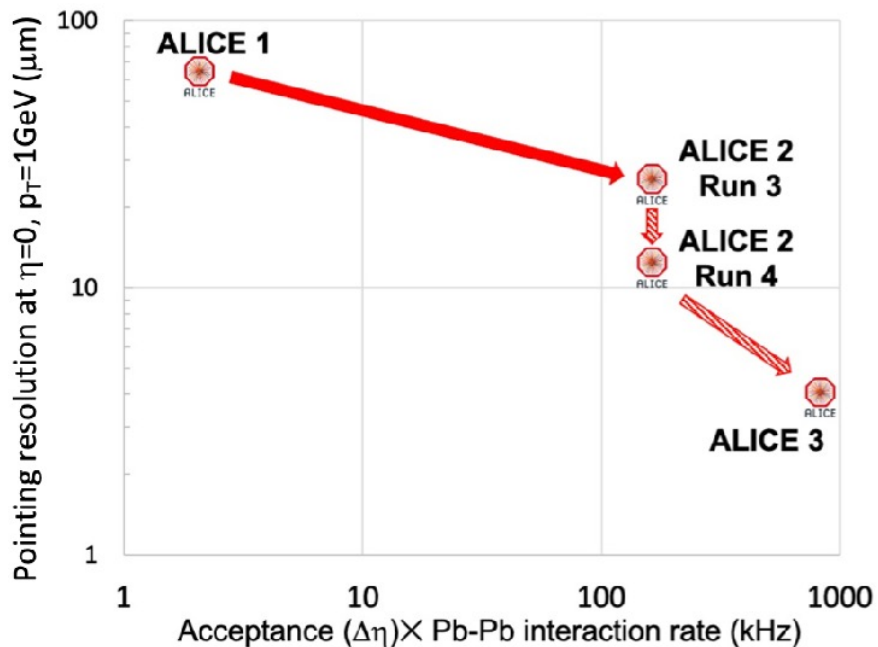


✓ large improvement for low transverse momenta

# 全硅探测器谱仪 -- ALICE 3 实验

- Compact, **low mass, all-silicon detector**, retractable vertex detector
- Super-conducting magnet system (2T)
- Extensive particle identification
- Continuous readout + online processing

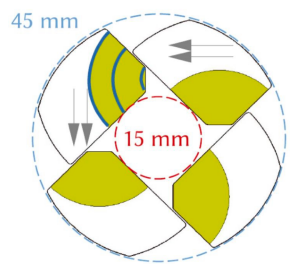
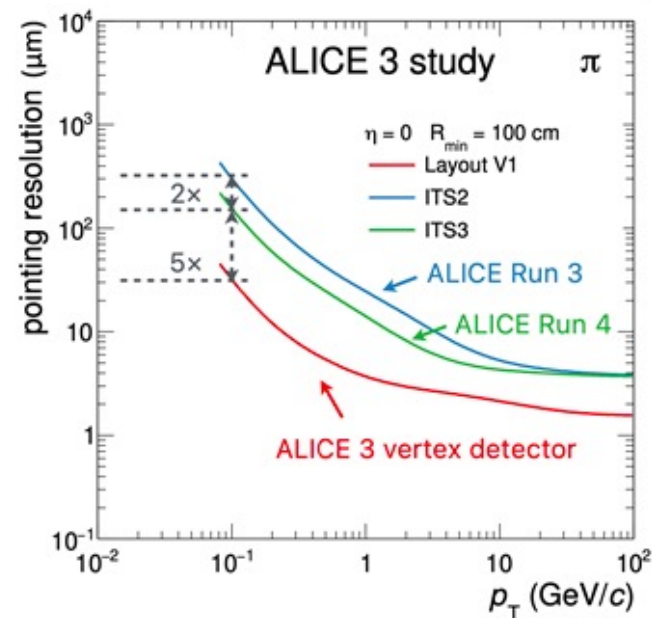
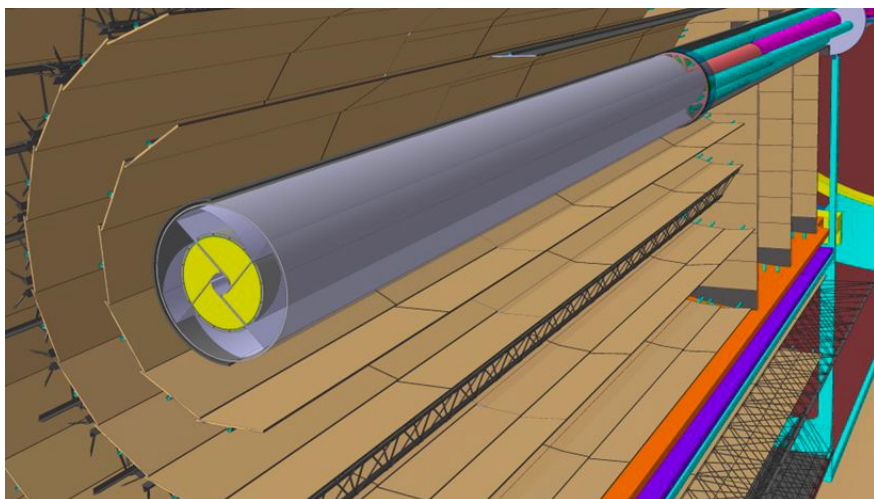
## 下一代全硅实验



# ALICE 3: Vertex Detector

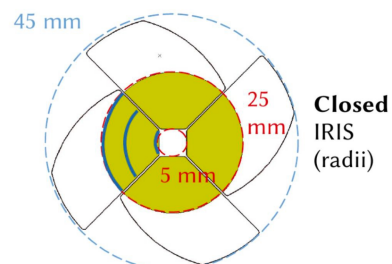
## Retractable vertex detector:

- ✓ Three layers within the beam pipe in secondary vacuum
- ✓ **Stitching**: Wafer-scale bent sensor (relying on ITS3 R&D)
- ✓ IRIS service system being developed
- ✓ Resolution:  $\sigma_{\text{pos}} \sim 2.5 \mu\text{m} \rightarrow 10 \mu\text{m}$  pixel pitch
- ✓ Material:  $\sim 0.1\%$   $X/X_0$  per layer
- ✓ 100 ns time resolution



Open  
IRIS  
(radii)

Beam injection



Closed  
IRIS  
(radii)

Beam stable

# ALICE 3: Middle & Outer tracker

## Requirements

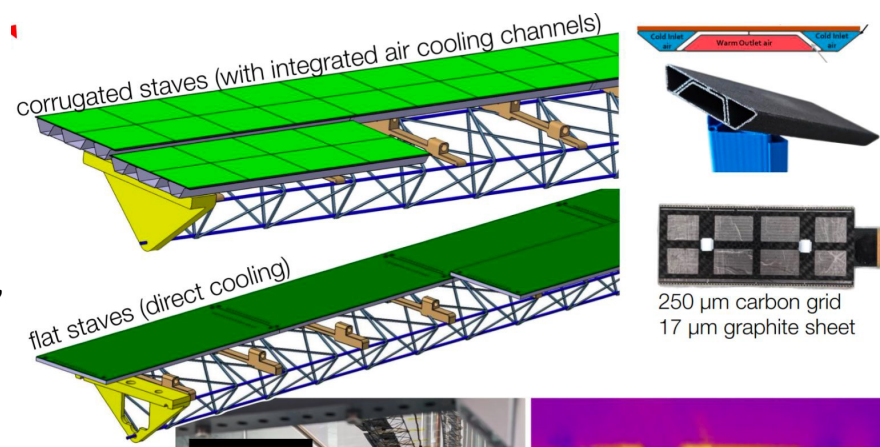
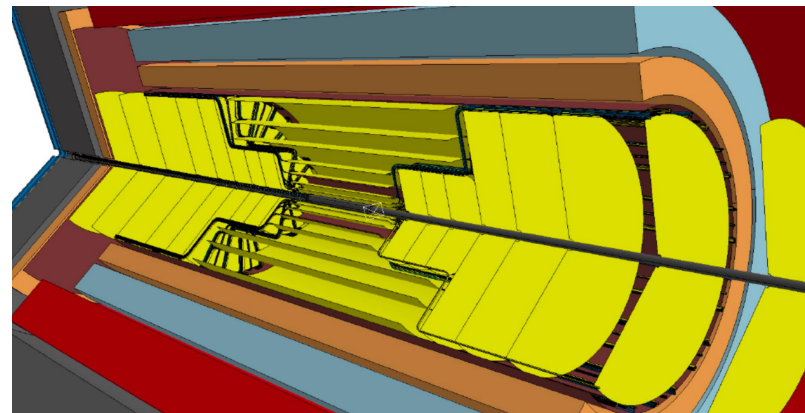
Material:  $\sim 1\% X/X_0$  per layer

Spatial resolution:  $\sim 10 \mu\text{m} \rightarrow$  pixel pitch  $< 50 \mu\text{m}$

Power consumption  $\leq 20 \text{ mW/cm}^2$

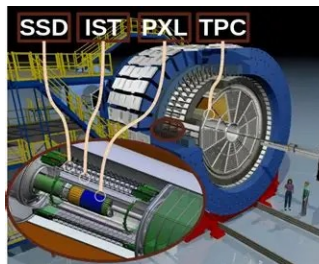
## Implementation

- Four (middle) layers at 7-20 cm + 3x2 endcap disks
- Four (outer) layers at 30-80 cm+ 6x2 disk layers
  - **60 m<sup>2</sup> active detection area**
  - CMOS MAPS are foreseen as the sensor technology.
  - The integration scheme is based on ITS 2 experience, with sensors assembled into modules and then into staves.



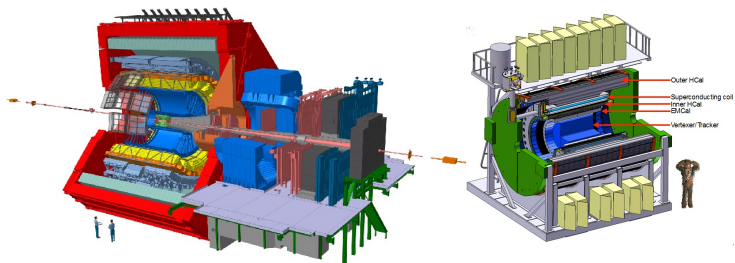
# MAPS探测器研究进展

## 1<sup>st</sup> generation MAPS



STAR PXL

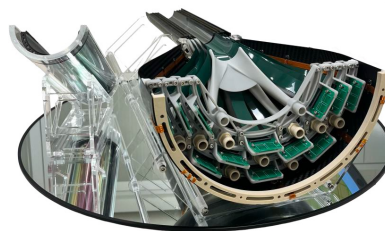
## 2<sup>nd</sup> generation MAPS



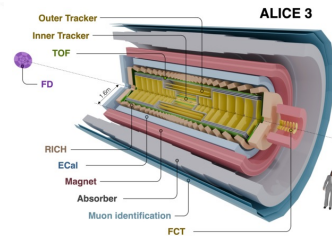
ALICE ITS2

SPHENIX MVTX

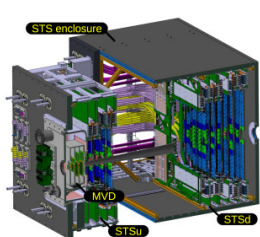
## 2<sup>nd</sup> + 3<sup>rd</sup> generation MAPS



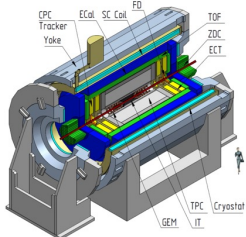
ALICE ITS3



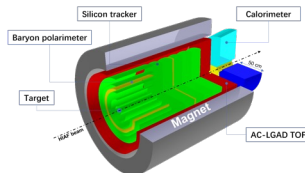
ALICE 3 Tracker



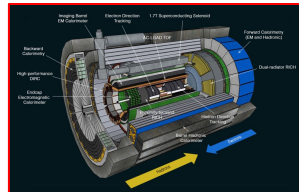
CBM STS



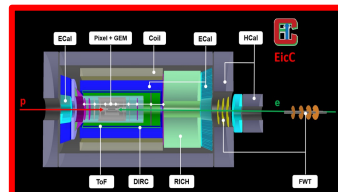
MPD IT



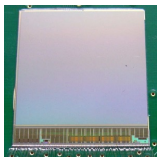
H-NS Tracker



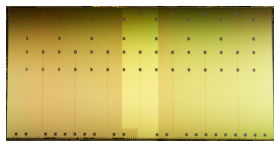
EIC/ePIC SVT



EicC Tracker



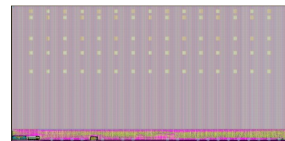
MIMOSA



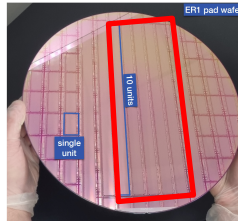
ALPIDE



MIMOSIS

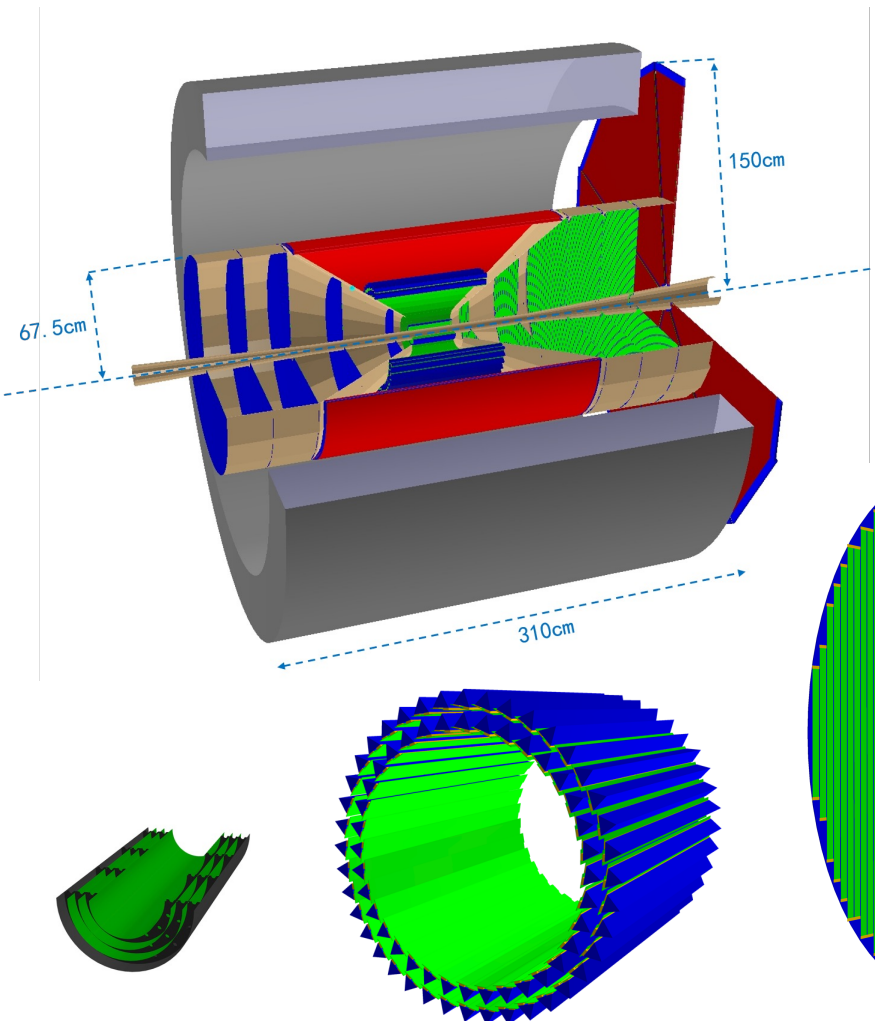


MIC6

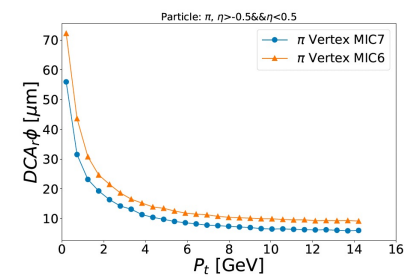
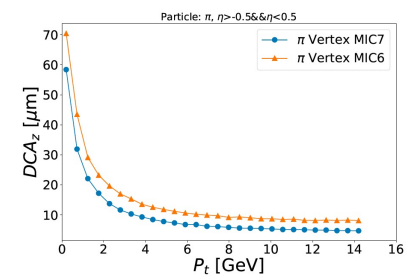
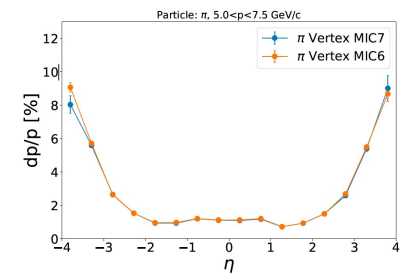
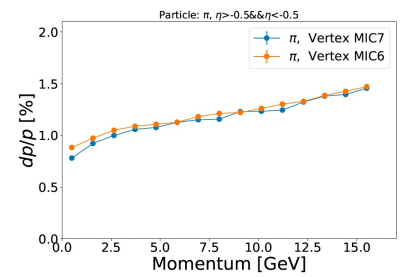
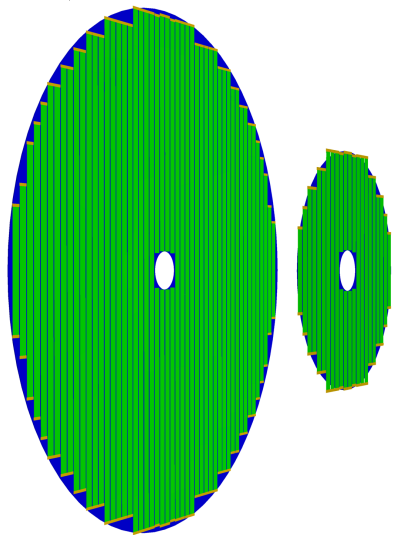


Stitching-based MOSAIX

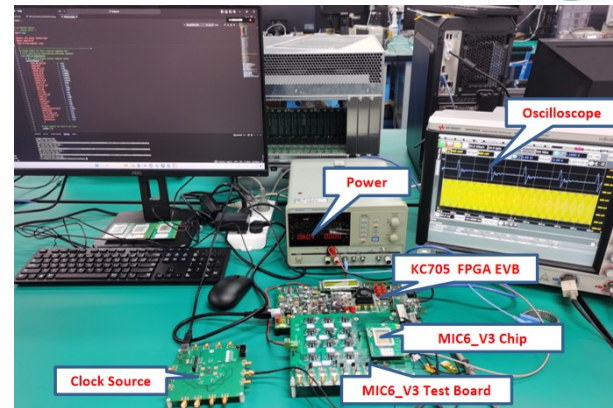
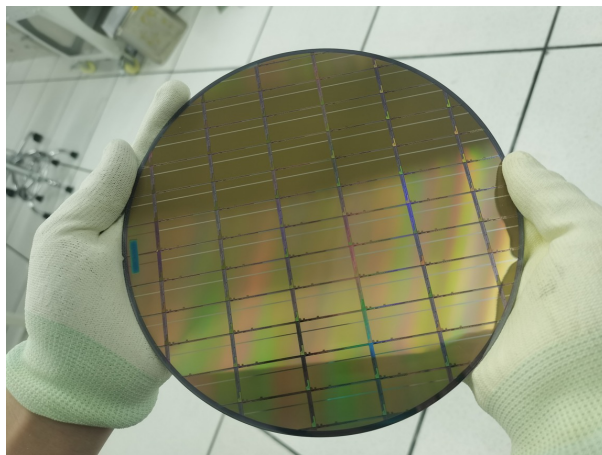
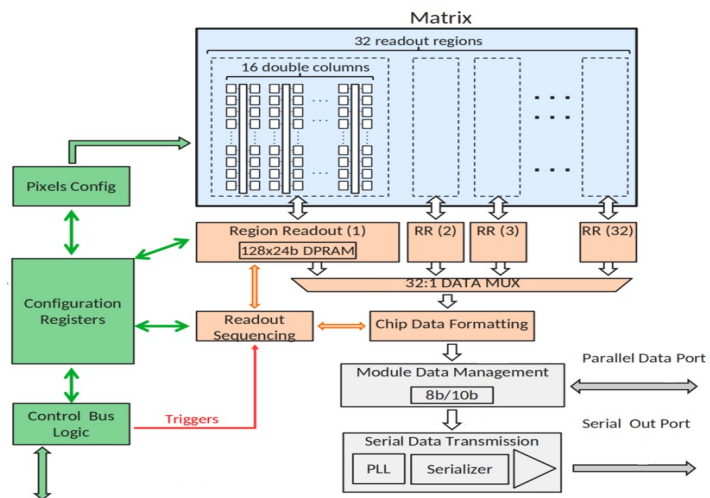
# EicC径迹系统



R(cm)	Length(cm)	Pitch Size( $\mu\text{m}$ )	X/ $X_0$ %	Tech.
3.3	28.0	20	0.09	MIC7
4.4	28.0	20	0.09	ITS3-like MIC7
5.5	28.0	20	0.09	MIC7
27.5	73.42	30	0.85	ITS2-like MIC6
30.0	80.01	30	0.85	MIC6
65.5	174.88	$150(r-\phi)\times 150(z)$	1.50	MPGD
67.5	174.88	$150(r-\phi)\times 150(z)$	1.50	MPGD

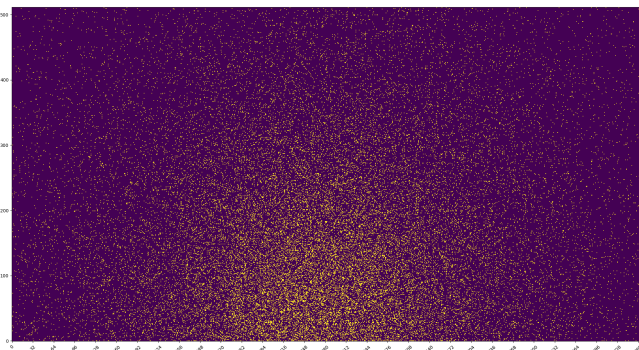


## MIC6\_V3 block diagram

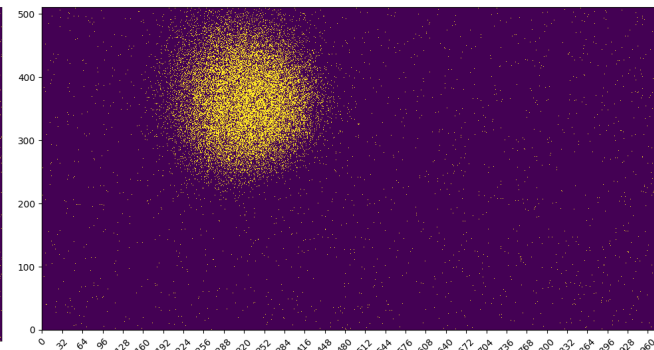


## MIC6\_V3芯片及测试系统

参数	ALPIDE	MIC6 原型
工艺	TowerJazz 180nm	GSMC 130nm
核心电压	1.8V	1.2V
芯片尺寸	30 mm × 15 mm	30 mm × 15.48 mm
像素阵列	1024 × 512	980 × 512
像素尺寸	29.24 um × 26.88 um	30.53 um × 26.8 um
像素达峰时间	2 us	1 us
积分时间	5~10 us	5~10 us
数据压缩读出	采用 AERD 方式读出	采用 AERD 方式读出
高速串行输出	1.2Gbps (8B10B 编码)	1.1Gbps (8B10B 编码)
功耗	40 mW/cm <sup>2</sup>	32 mW/cm <sup>2</sup>



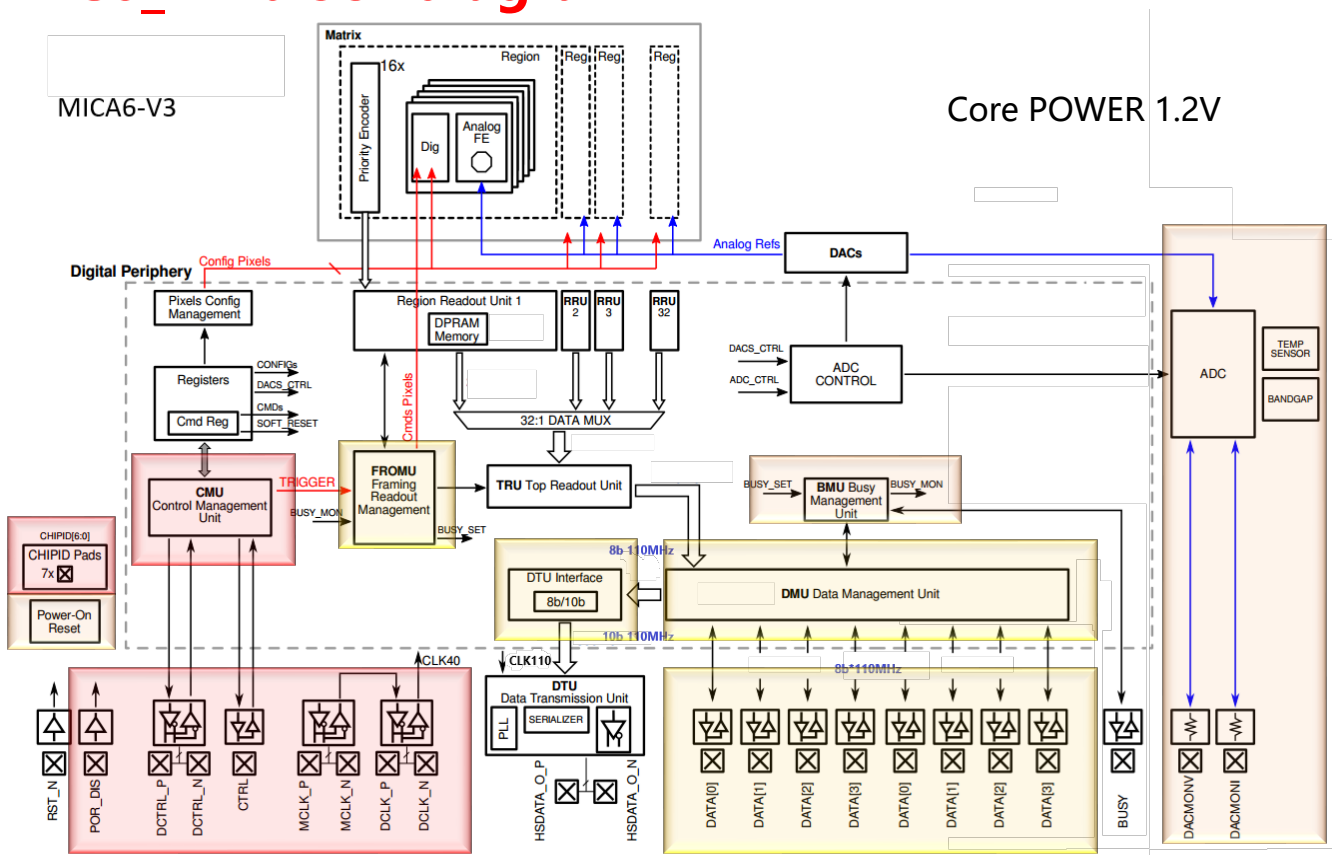
<sup>90</sup>Sr测试



<sup>241</sup>Am测试

# EicC径迹系统 – 像素芯片研发

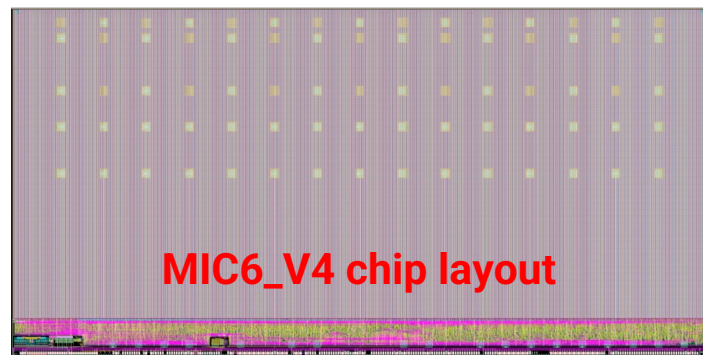
## MIC6\_V4 block diagram



Add Red Parts

Modify Yellow Parts

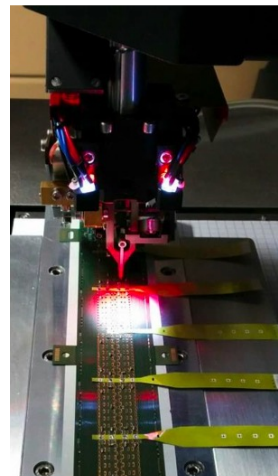
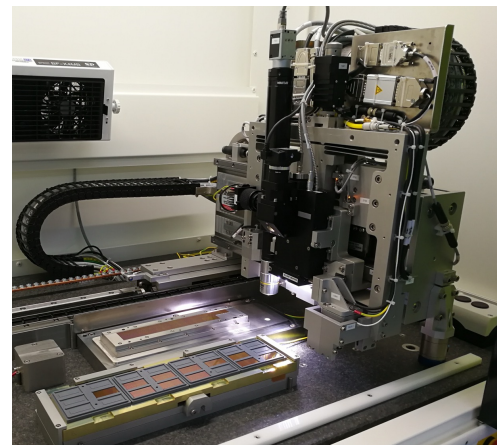
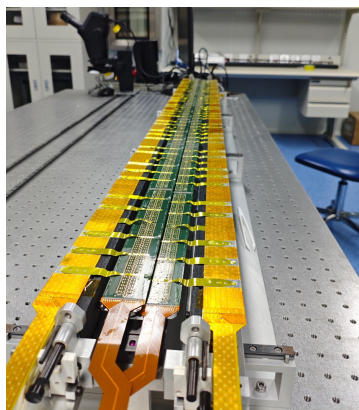
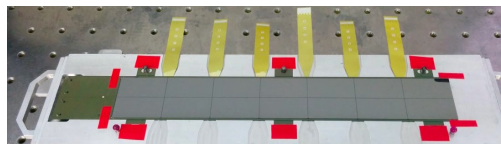
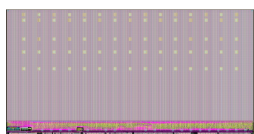
Features	MIC6_V4
Process Technology	GSMC-130 nm
Core Voltage	1.2V
Chip Size	30 mm × 15 mm
Pixel Array	980 × 497
Pixel Size	30.53 um × 26.8 um
Zero Suppression Readout	AERD
High-Speed Serial Output	1.2Gbps
Encoder	8B10B
Slow Control	MLVDS Control Bus
Parallel Data Interface	master-slave data aggregation and transmission



MIC6\_V4 chip layout

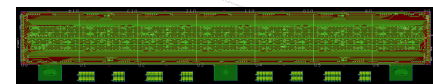
# EicC径迹系统 – 探测器组装与集成

- 掌握从芯片集成到探测器模块组装的关键技术，建立组装与测试产线
- 围绕硅像素探测器研制，开展低质量碳纤维复合材料结构设计与联合制备

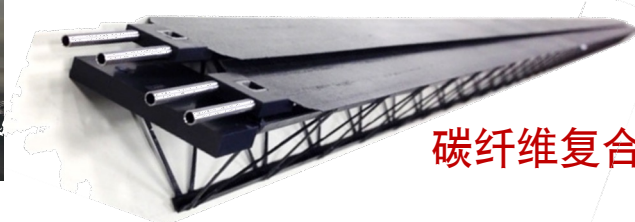


芯片集成千级净室

探测器模块组装万级净室



柔性PCB板



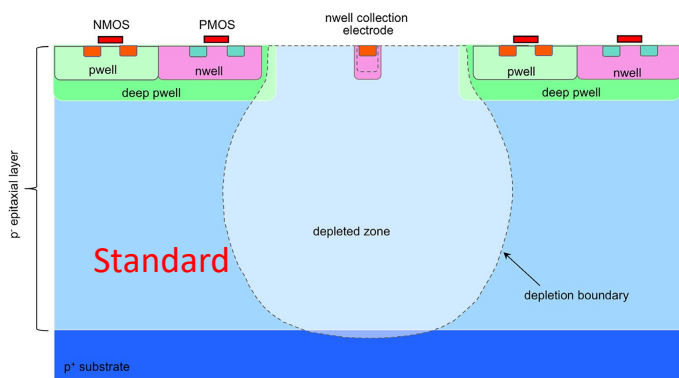
碳纤维复合材料结构

- 自2001年提出CMOS MAPS概念以来，已先后成功应用于RHIC/STAR、LHC/ALICE和RHIC/sPHENIX等重离子碰撞实验；
- 在建和拟推动建设的国内外大科学装置实验（NICA/MPD、EIC/ePIC、ALICE 3、H-NS和EicC、CEPC和STCF等）均将硅像素探测器作为其核心径迹探测器；
- 近年来，硅探测器技术在国内发展非常迅速，中国研究团队积极参与并推动硅像素探测器在等国内外核物理和粒子物理实验的应用；
  - ✓ MAPS: JadePix (IHEP&CCNU), MIC6 (CCNU), SuPix (SDU), STCF pix (USTC), TaiChuPix (IHEP), ...
  - ✓ 读出电子学: USTC, IHEP, CCNU, SDU, ...
  - ✓ 探测器组装与集成: CCNU, IHEP, IMP, CIAE, ...
- 国内团队已完成EicC实验硅像素探测器系统的概念设计！

## 谢谢大家！

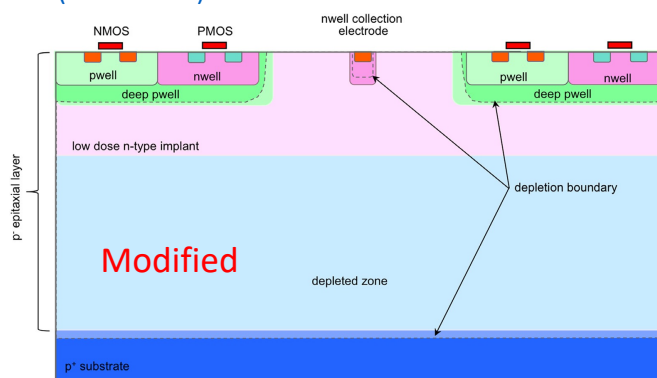
# Full depleted MAPS

- A process modification developed as side activity of ALICE R&D
- Doping profiles of MAPS have been repeatedly improved to reach full depletion



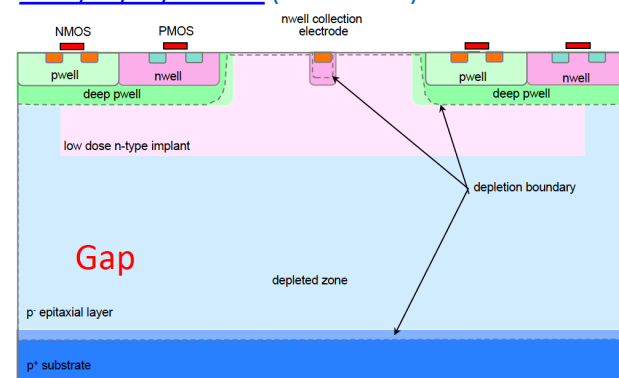
<https://doi.org/10.1016/j.nima.2017.07.046>

(ALICE R&D)



<https://iopscience.iop.org/article/10.1088/1748-0221/14/05/C05013>

(ALICE R&D)



- Partially depleted epitaxial layer
- Charge collection time < 30 ns
- Operational up to  $10^{14}$   $1 \text{ MeV}$   $n_{\text{eq}}/\text{cm}^2$

- Fully depleted epitaxial layer
- Charge collection time < 1 ns
- Operational up to  $10^{15}$   $1 \text{ MeV}$   $n_{\text{eq}}/\text{cm}^2$