



# 大型实验DAQ系统的挑战与技术发展

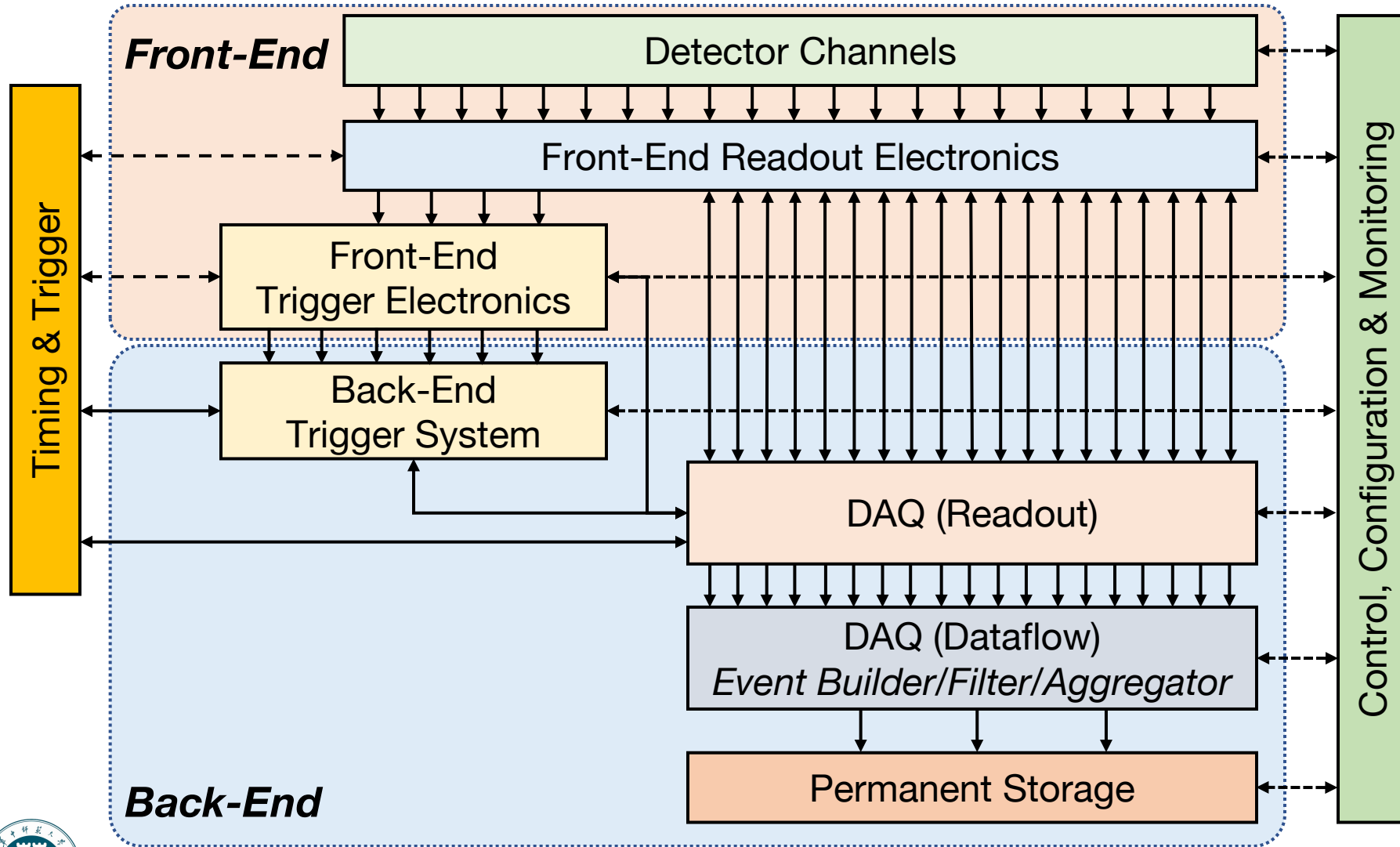
陈凯

华中师范大学

第一届中国电子离子对撞机相关物理年会（山东青岛）

2026-04-20

# 读出与数据获取整体框架

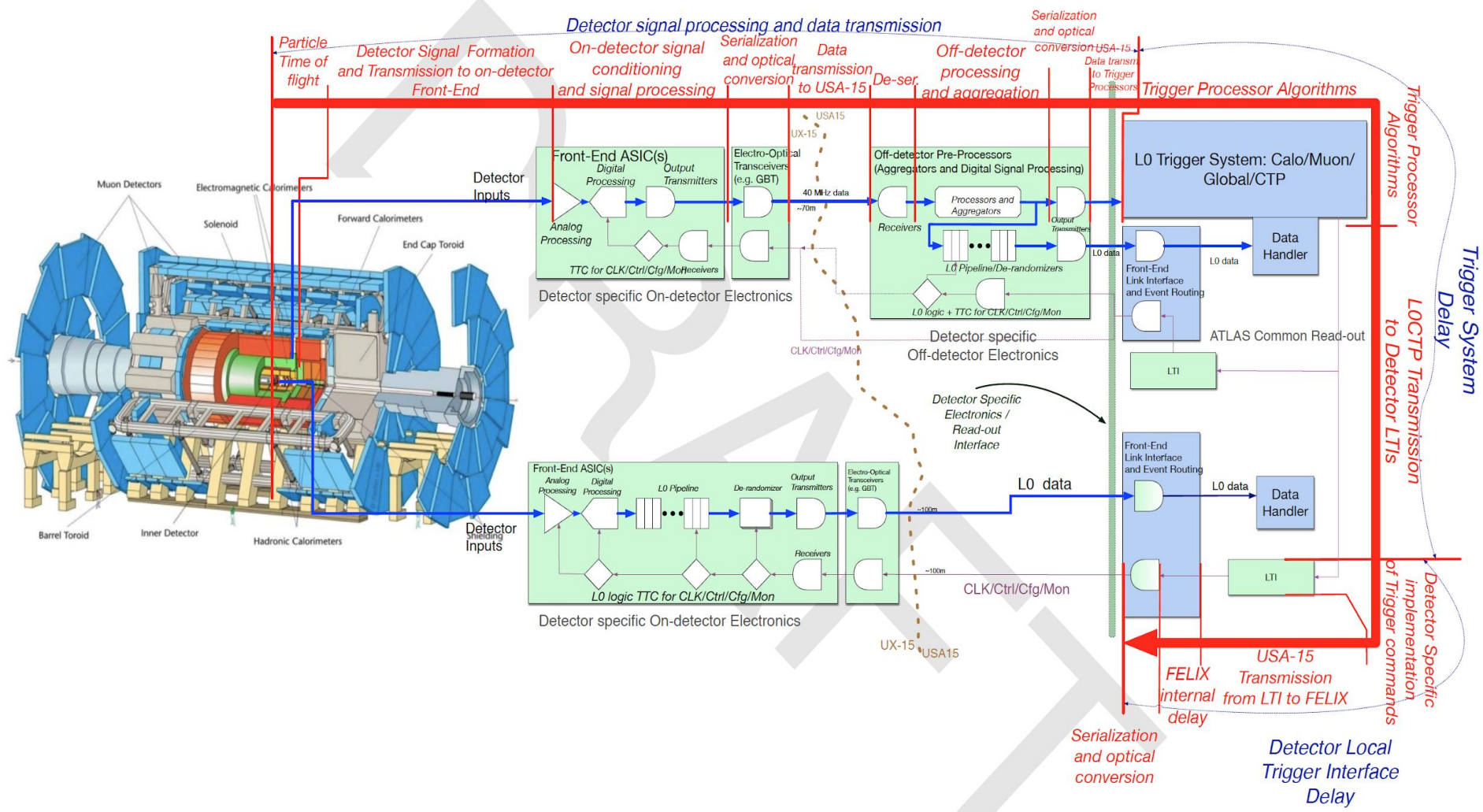


后端的触发与数据获取系统

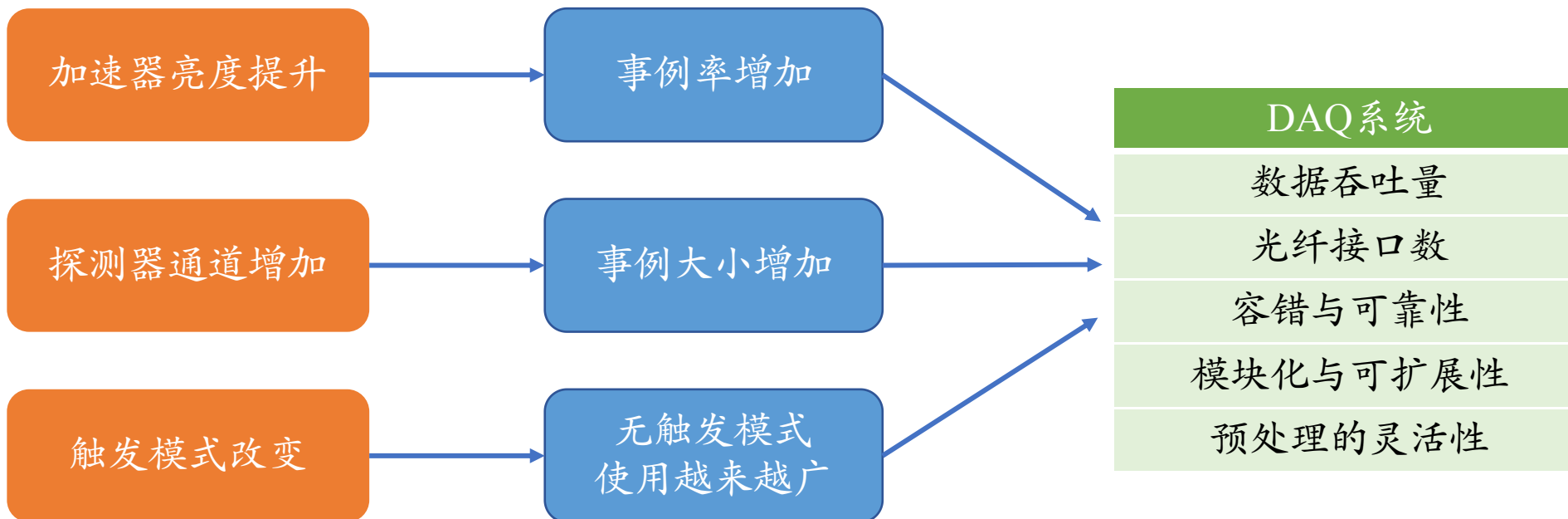
- 读出
  - 数据读出
  - 低延时触发/无触发
  - 集成时钟分发、同步命令发送
  - 慢控数据通道
- 数据处理
  - 事例组装
  - 事例过滤
  - 存储



# ATLAS @ HL-LHC (Run-4)



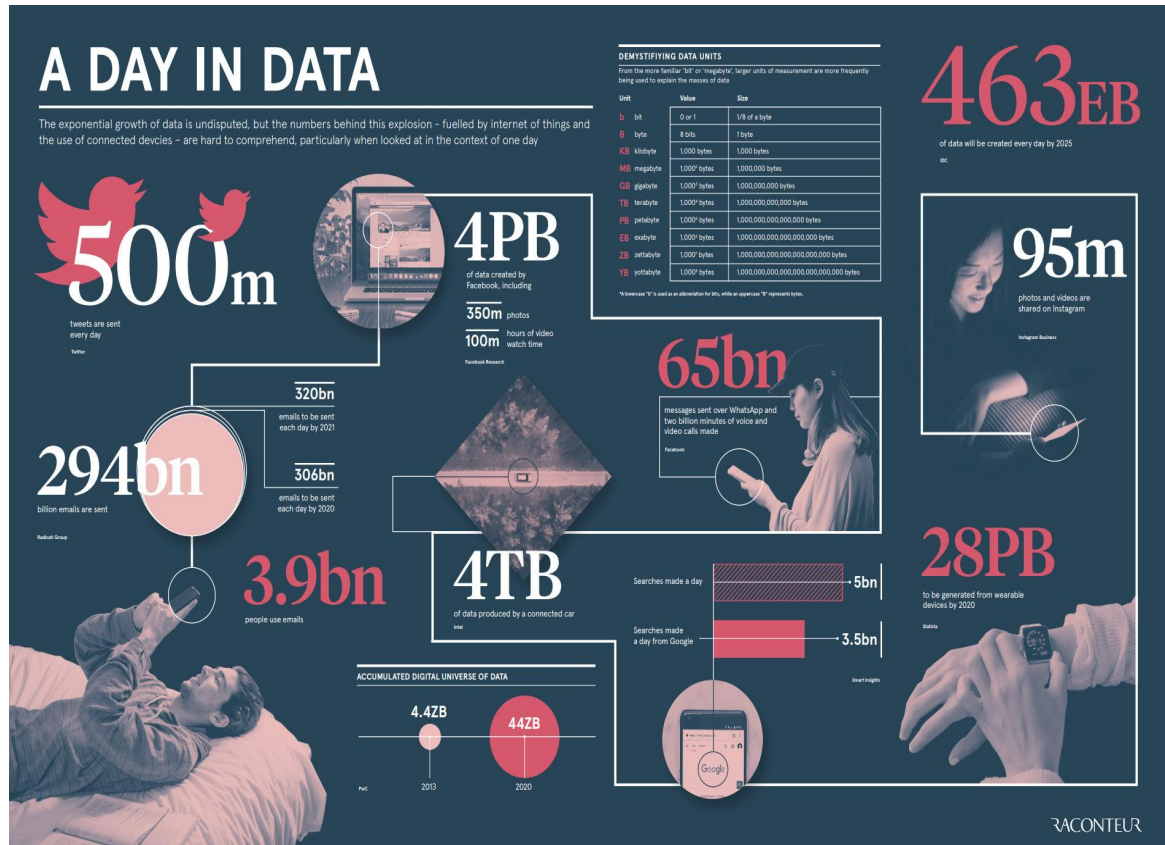
# 实验需求



				Readout	Storage		
	Rate	Size	Bandwidth	fiber	Rate	Bandwidth	
ATLAS	Run-2	100 kHz	1.6 MB	160 GB/s	~2000	<2 kHz	<3 GB/s
	Run-3	100 kHz	2.9 MB	290 GB/s	(+100 FLX712)	<2 kHz	<6 GB/s
	Run-4	1 MHz	4.6 MB	4.6 TB/s	~14000 (678 FLX155)	10 kHz	51 GB/s

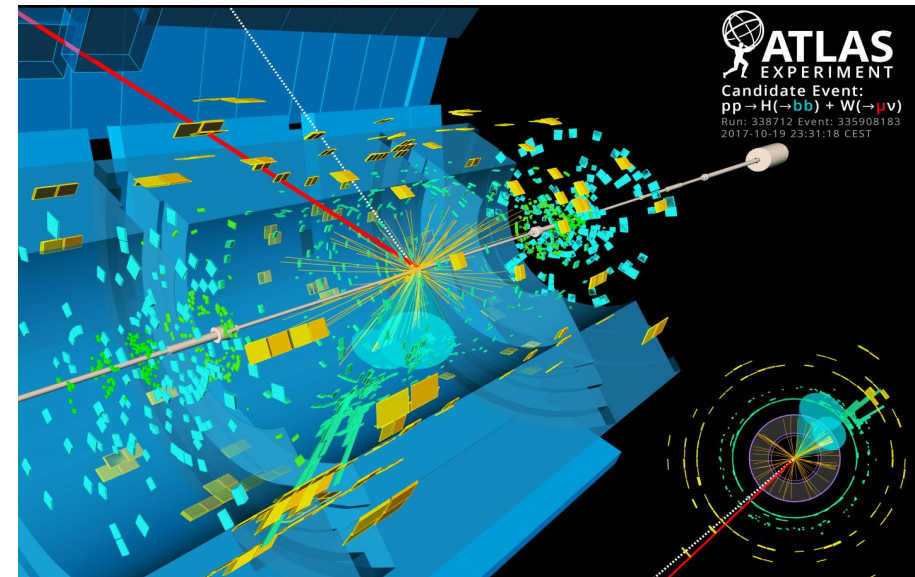


# 核心挑战：数据量、时钟分发



□ 2019年，Facebook：4PB每天

□ 2025年，463EB每年（15TB/s）



ATLAS: < 1Pb/s

FCC-hh: ~10Pb/s

事例率：100kHz ~ 10MHz

时钟同步：syntonization → synchronization: ns到ps级别



# 相关核心技术

## □ 硬件

- 工业标准的机箱
- 高密度高带宽光通信收发模块
- 高带宽总线
- 对接高性能网络
- 高性能硬件资源：数据处理

## □ 时钟与慢控

- 高精度时钟分发
- 灵活的探测器控制通路

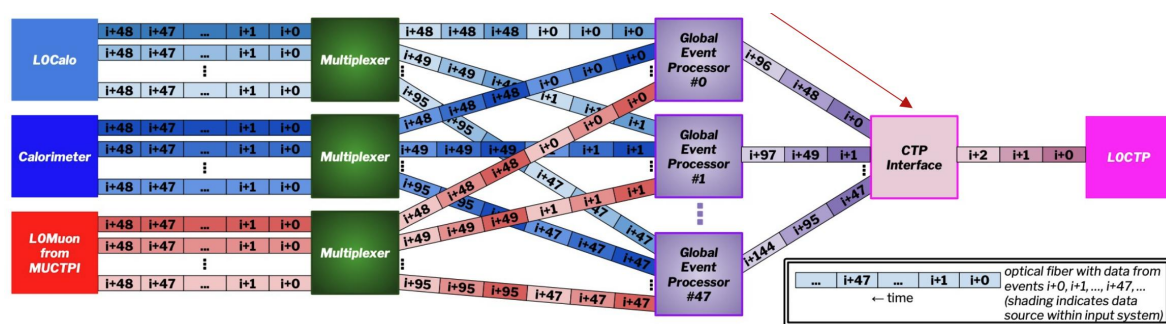
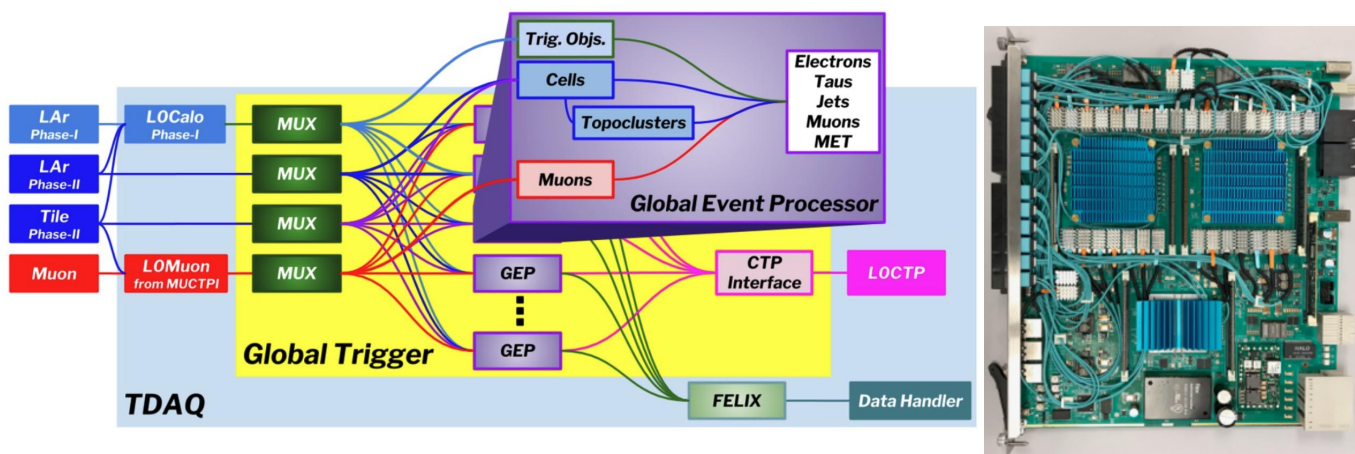


# 硬件平台的选择

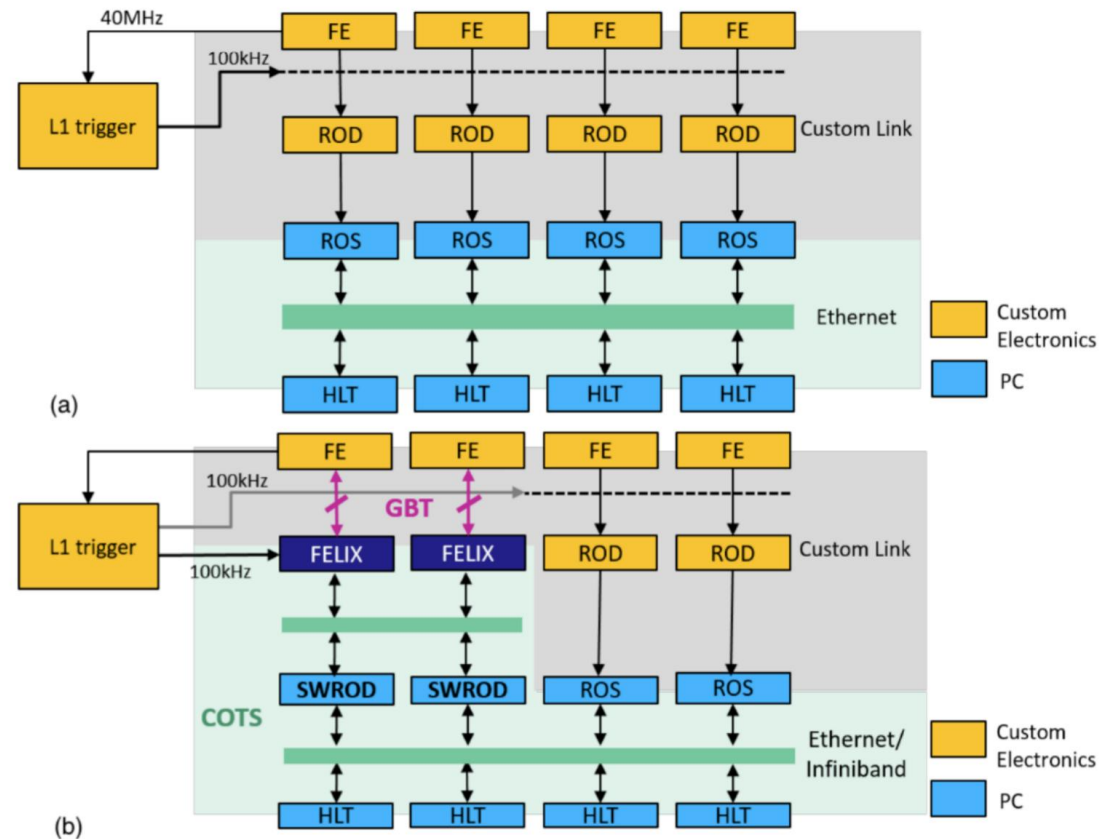
- 紧随工业界发展趋势，系统层面往模块化、通用化、标准化方向发展
  - **VME**: LHC、BES等，带宽与性能远低于当前主流的高速总线
  - **PXI/PXIe**: HIRFL-CSR外靶实验等，高可靠性，更适合前端，后端应用较少，机箱成本较高
  - **PCIe**: LHC/RHIC/Belle2/CBM等，应用广泛，对服务器要求较低
  - **ATCA**: 触发系统应用较多；CMS实验DAQ系统
  - **MicroTCA**: 更适合前端，但在后端应用也越来越多
  - **网络**: DUNE等，UDP、TCP、RDMA，如IPbus、SiTCP
  - **自定义机箱**: 需要多单位、多实验协作推进



# 后端系统的通用化



ATLAS@HL-LHC: 触发硬件的统一化: GCM



ATLAS实验DAQ系统的进化

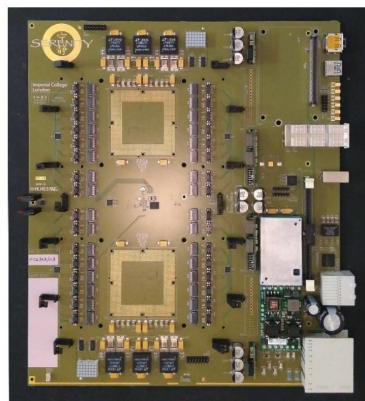


# ATCA的大量使用



SRS

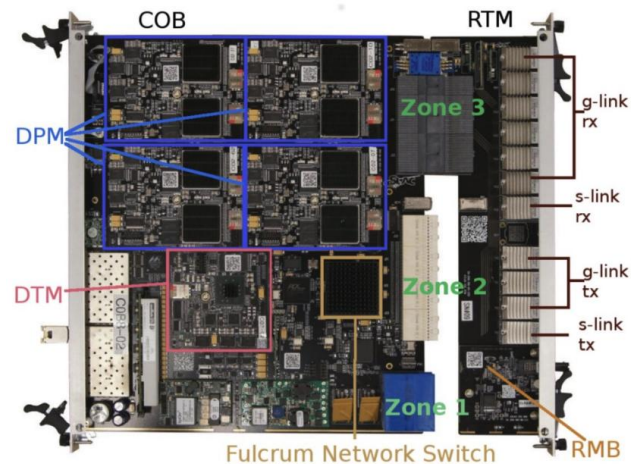
- ❑ 读出、控制、DAQ: ITER, SRS, RCE (SLAC), CMS
- ❑ 触发: ATLAS



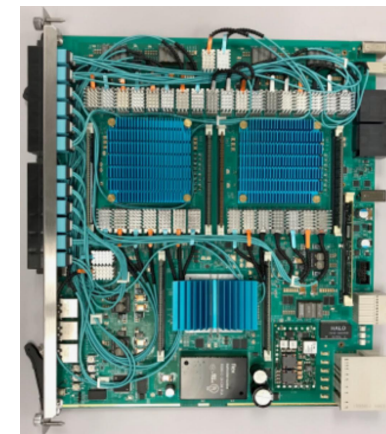
CMS Serenity



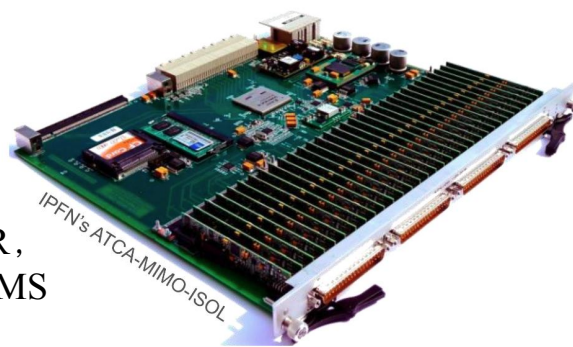
CMS DTH



RCE



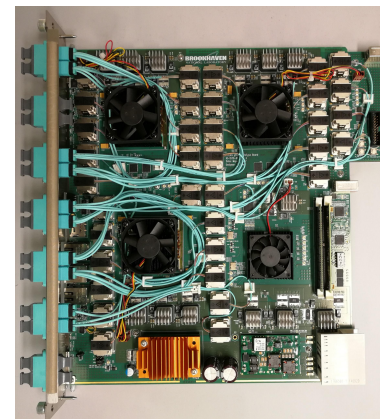
ATLAS GCM



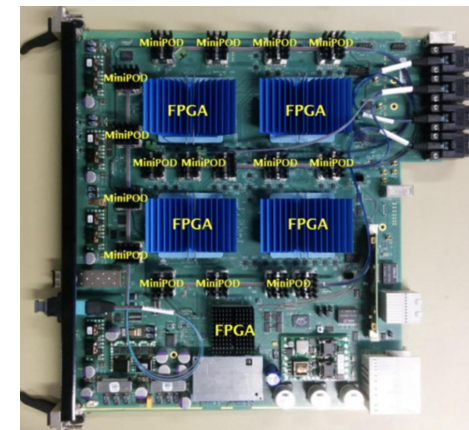
ITER



ATLAS jFEX



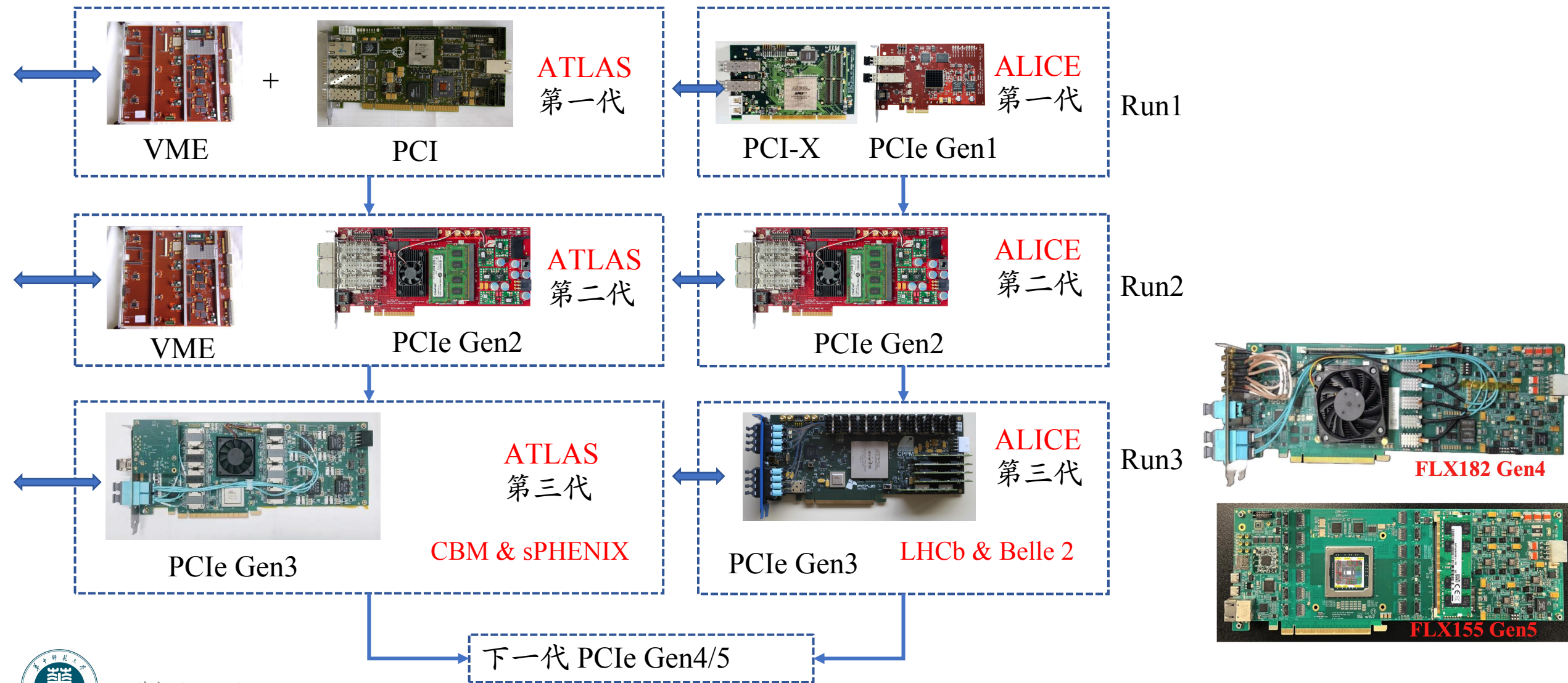
ATLAS gFEX



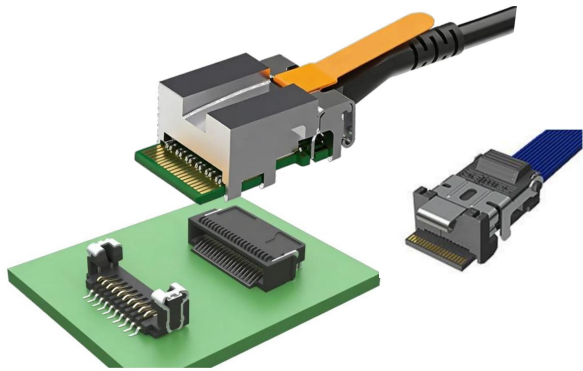
ATLAS eFEX



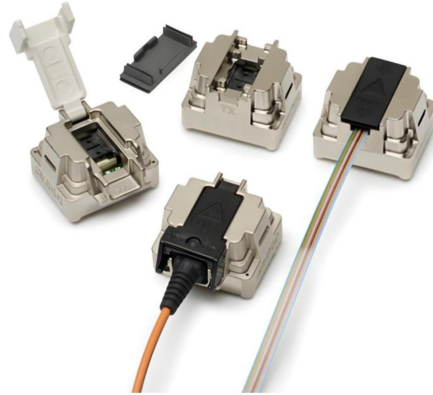
# PCIe的应用及迭代



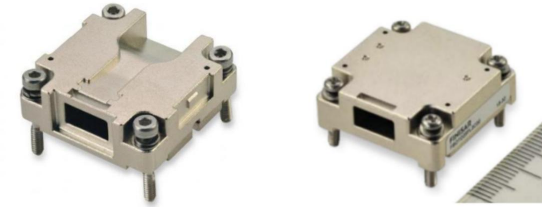
# 高密度商用模块



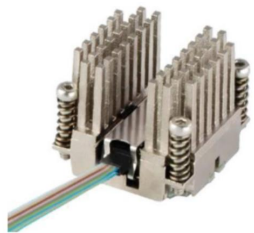
Samtec FireFly: 光缆/电缆  
4T4R/12T/12R, 可达28G



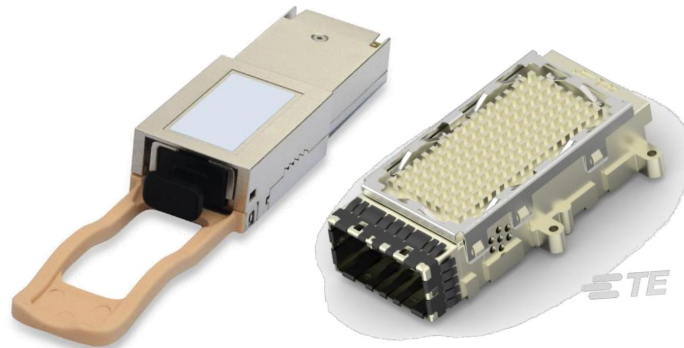
MiniPOD: 已停产  
12T/12R, 可达14G



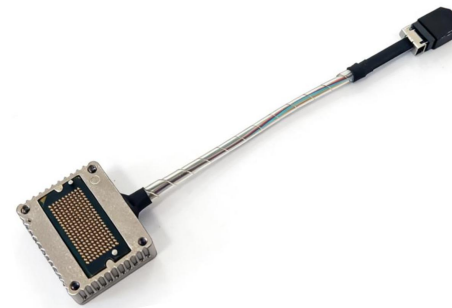
II-VI/Finisar BOA  
12T12R, 可达28G



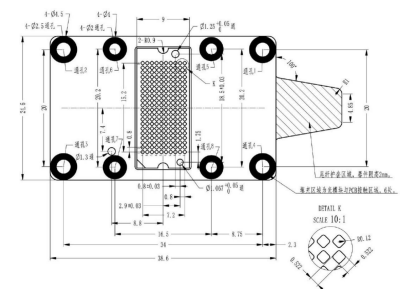
Amphenol/FCI OB  
12T12R, 可达28G



CXP 12T12R, ~ 10G



芯瑞POB 12T12R, 10G版本; 25G版本



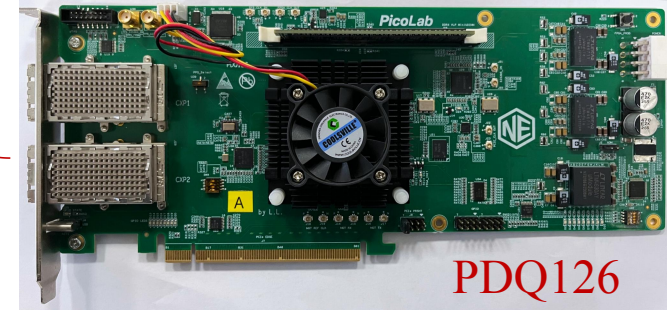
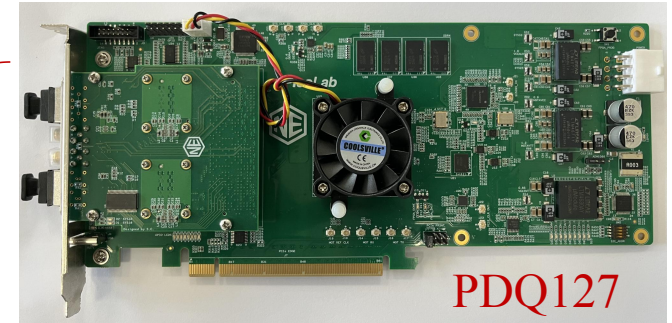
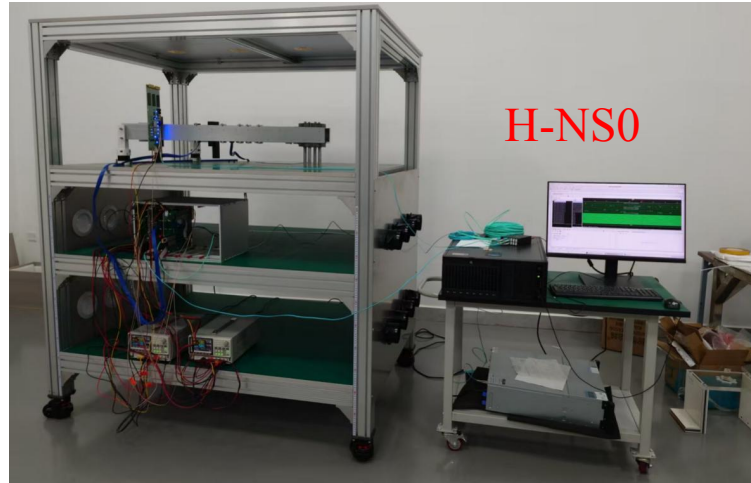
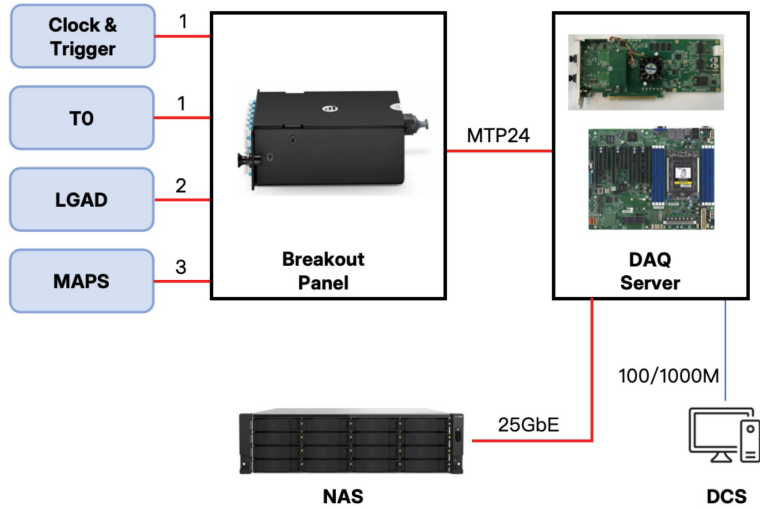
# 核心器件FPGA的禁运与国产化

- 高端FPGA的禁运
- 兼容方案：复旦微
  - 实际价格偏高
  - 仍有代差

FUDAN MICRO 复旦微电子		JFM9系列FPGA									
产品型号	JFM9RFVU2P5GF1517 JFM9RFVU2P5GF1517-AS JFM9RFVU2P5GF1517-N	JFM9RFVU3P JFM9RFVU3P-AS JFM9RFVU3P-N	JFM9RFVU3P5G JFM9RFVU3P5G-AS JFM9RFVU3P5G-N	JFM9RFVU9P JFM9RFVU9P-AS JFM9RFVU9P-N	JFM9KU6PD900 JFM9KU6PD900-AS JFM9KU6PD900-N JFM9KU6PD900-L* 为低功耗版本	JFM9KU11PE1517 JFM9KU11PE1517-AS JFM9KU11PE1517-N JFM9KU11PE1517-L* 为低功耗版本	JFM9VU3PC1517 JFM9VU3PC1517-AS JFM9VU3PC1517-N	JFM9VU9PA2104 JFM9VU9PA2104-AS JFM9VU9PA2104-N	JFM9VU9PB2104 JFM9VU9PB2104-AS JFM9VU9PB2104-N	JFM9VU13PB2104 JFM9VU13PB2104-AS JFM9VU13PB2104-N	JFM9VU13PA2577 JFM9VU13PA2577-AS JFM9VU13PA2577-N
对应国外厂家/型号	自定义架构	自定义架构	自定义架构	自定义架构	Xilinx/XCKU5P-D900	Xilinx/XCKU11P-E1517	Xilinx/XCVU3P-C1517	Xilinx/XCVU9P-A2104	Xilinx/XCVU9P-B2104	Xilinx/XCVU13P-B2104	Xilinx/XCVU13P-A2577
逻辑单元数 (K)	722	862	862	2,586	621	722	862	2,586	2,586	3,780	3,780
DSP (27x18乘法器) 个数	3,072	2,280	2,280	6,840	1,824	3,072	2,280	6,840	6,840	12,288	12,288
BRAM (36Kb) 个数	672	720	720	2160	576	672	720	2160	2160	2688	2688
URAM (288Kb) 个数	128	320	320	960	64	128	320	960	960	1280	1280
User I/O 个数	512	520	520	448	304	512	520	832	702	702	448
SERDES通道数	20	20	20	48	16	52	40	52	76	76	128
封装形式	PCB基板倒扣球栅阵列封装 FCBGA F1517	PCB基板倒扣球栅阵列封装 FCBGA F1517	PCB基板倒扣球栅阵列封装 FCBGA F1517	PCB基板倒扣球栅阵列封装 FCBGA G2577	PCB基板倒扣球栅阵列封装 FCBGA D900	PCB基板倒扣球栅阵列封装 FCBGA E1517	PCB基板倒扣球栅阵列封装 FCBGA C1517	PCB基板倒扣球栅阵列封装 FCBGA A2104	PCB基板倒扣球栅阵列封装 FCBGA B2104	PCB基板倒扣球栅阵列封装 FCBGA B2104	PCB基板倒扣球栅阵列封装 FCBGA A2577
Core工作电压	0.85V	0.85V	0.85V	0.85V	0.85V	0.85V	0.85V	0.85V	0.85V	0.85V	0.85V
I/O工作电压	HPPIO 1.0 ~ 1.8V HDIO 1.2 ~ 3.3V	HPPIO 1.0 ~ 1.8V	HPPIO 1.0 ~ 1.8V	HPPIO 1.0 ~ 1.8V	HPPIO 1.0 ~ 1.8V HDIO 1.2 ~ 3.3V	HPPIO 1.0 ~ 1.8V HDIO 1.2 ~ 3.3V	HPPIO 1.0 ~ 1.8V	HPPIO 1.0 ~ 1.8V	HPPIO 1.0 ~ 1.8V	HPPIO 1.0 ~ 1.8V	HPPIO 1.0 ~ 1.8V
质量等级	工业级 宽温级 GJB7400N	工业级 宽温级 GJB7400N	工业级 宽温级 GJB7400N	工业级 宽温级 GJB7400N	工业级 宽温级 GJB7400N	工业级 宽温级 GJB7400N	工业级 宽温级 GJB7400N	工业级 宽温级 GJB7400N	工业级 宽温级 GJB7400N	工业级 宽温级 GJB7400N	工业级 宽温级 GJB7400N



# 通用后端硬件研制@CCNU



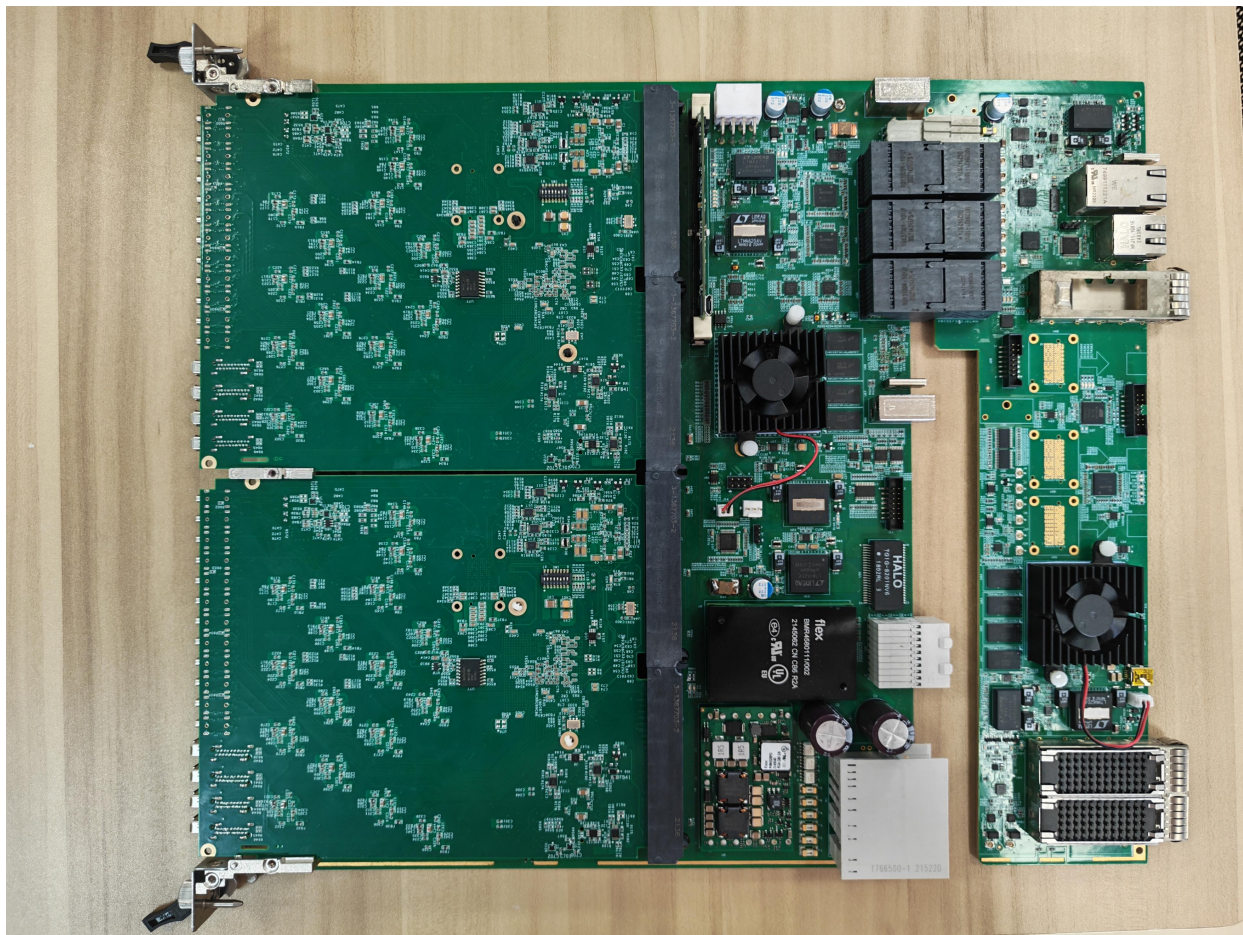
❑ NAS: QNAP TS-h1677AXU-RP

- 16 disk (16TB) RAID 6
- 854 MB/s

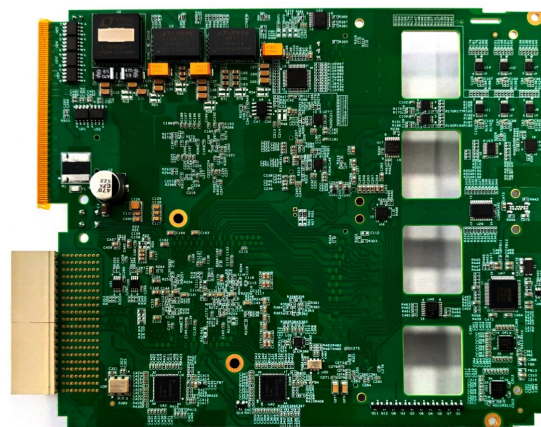
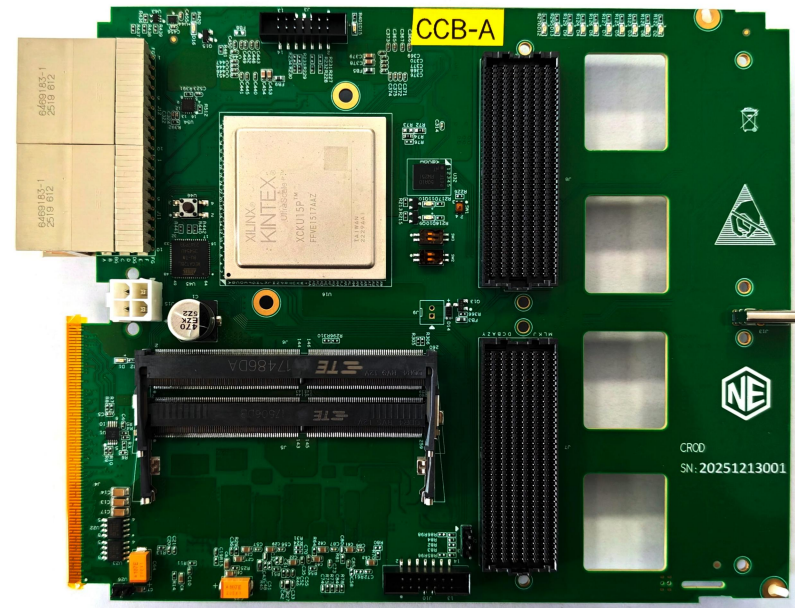
	FPGA	Fiber links	PCIe	Throughput
PDQ126/7	KU15P	24	Gen3/4	1/2×14.76 GB/s
PDQ142	VM1402	8	Gen4	1×14.76 GB/s



# 通用后端硬件研制@CCNU



模块化ATCA硬件



MicroTCA模块



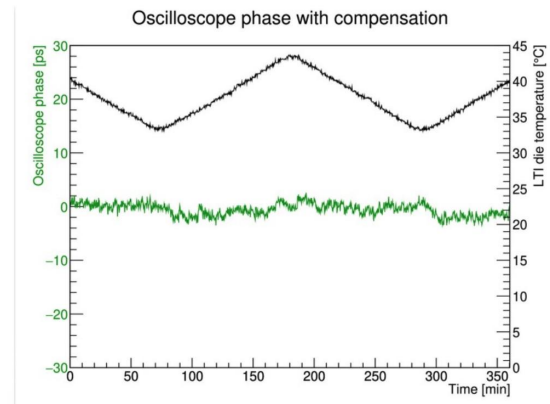
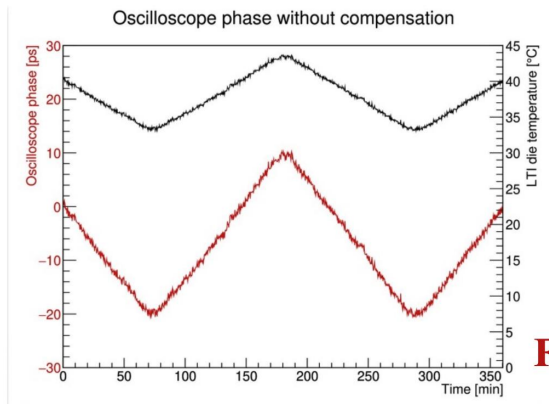
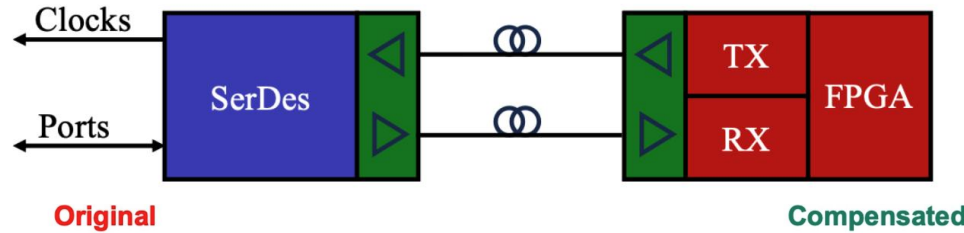
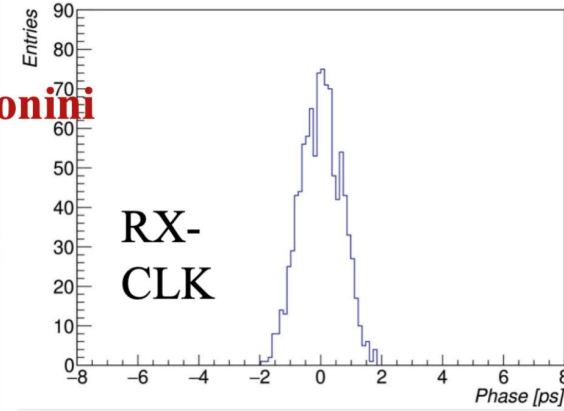
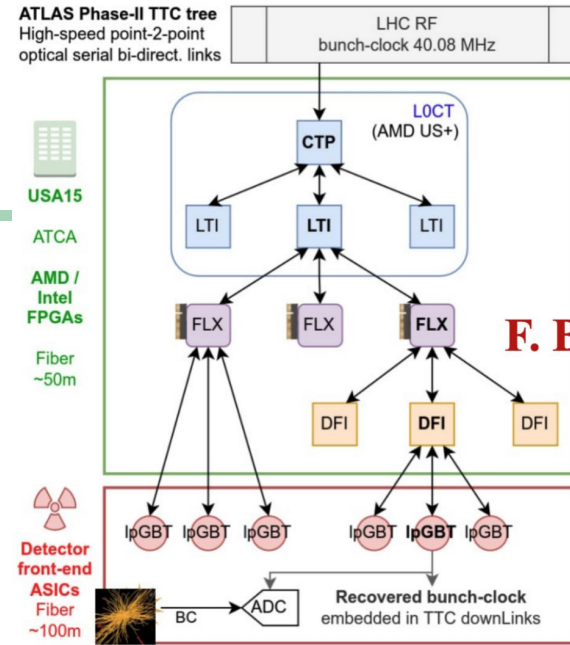
FMCP光模块子卡

2026/4/20

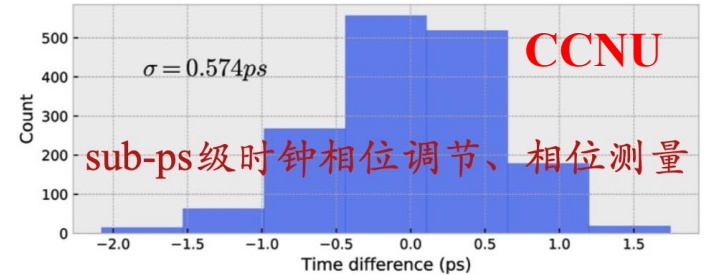
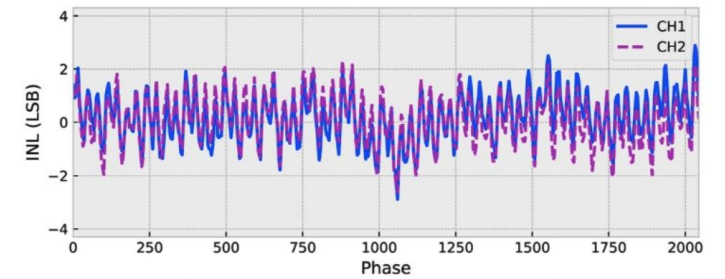


# 高精度时钟分发技术

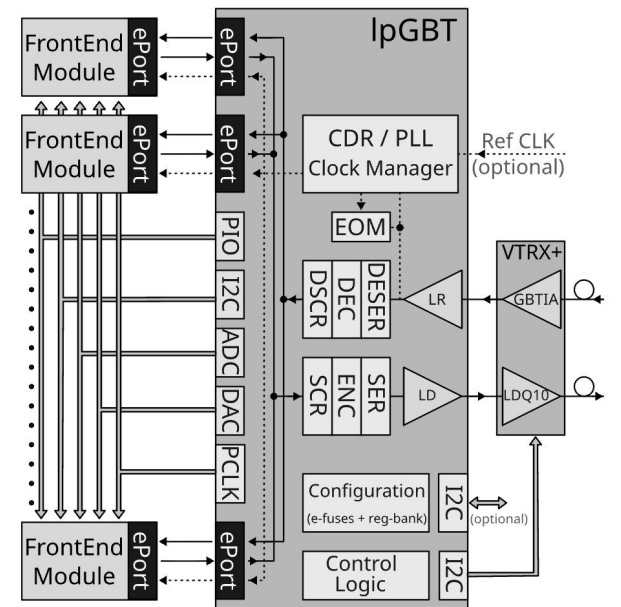
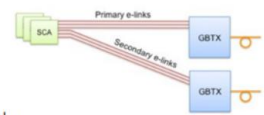
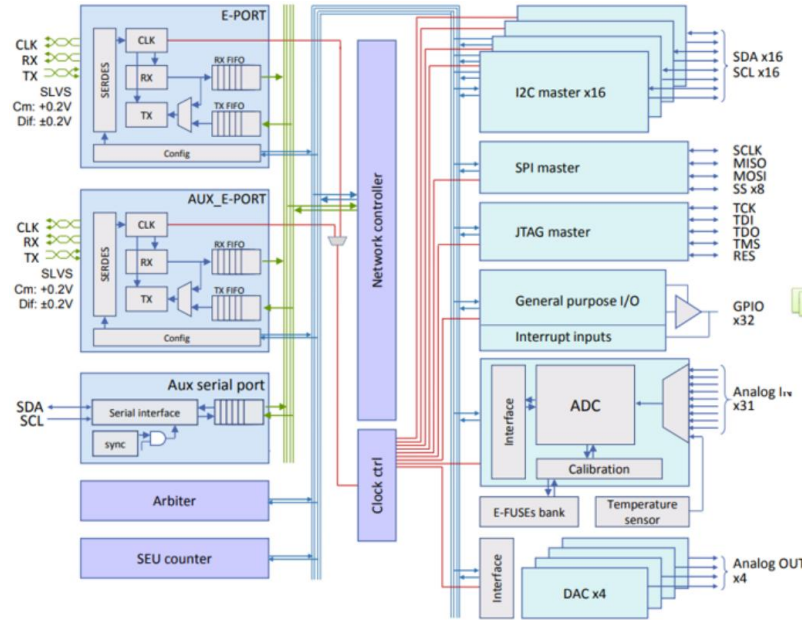
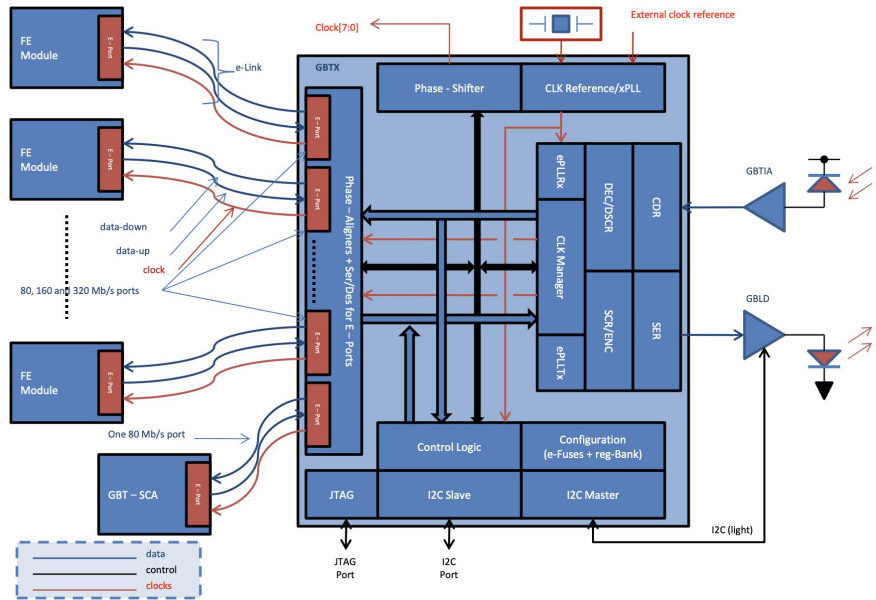
- 趋势：时钟嵌入数据链路
- CERN-HPTD：开源的针对AMD/Xilinx MGT的IP，保证相位复位后稳定性，及实现相位补偿
- CCNU：基于MGT的高精度相位测量与补偿



F. Bonini



# 慢控的集成



- ❑ DAQ与前端间单根光纤实现多个虚拟e-link并行固定延时传输
  - 数据、同步信号、慢控均以e-link形式传输
- ❑ 前端：
  - GBTx + GBT-SCA; IpGBTx
- ❑ 供电等特殊控制一般仍采用独立链路

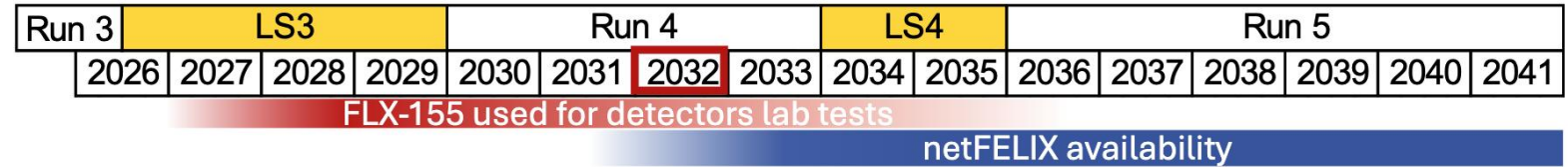


# 下一代netFELIX: (基于FPGA直接部署高性能网络)

## netFELIX Kick-Off Meeting

Welcome & Introduction  
21.01.2026

Sophie.baron@cern.ch

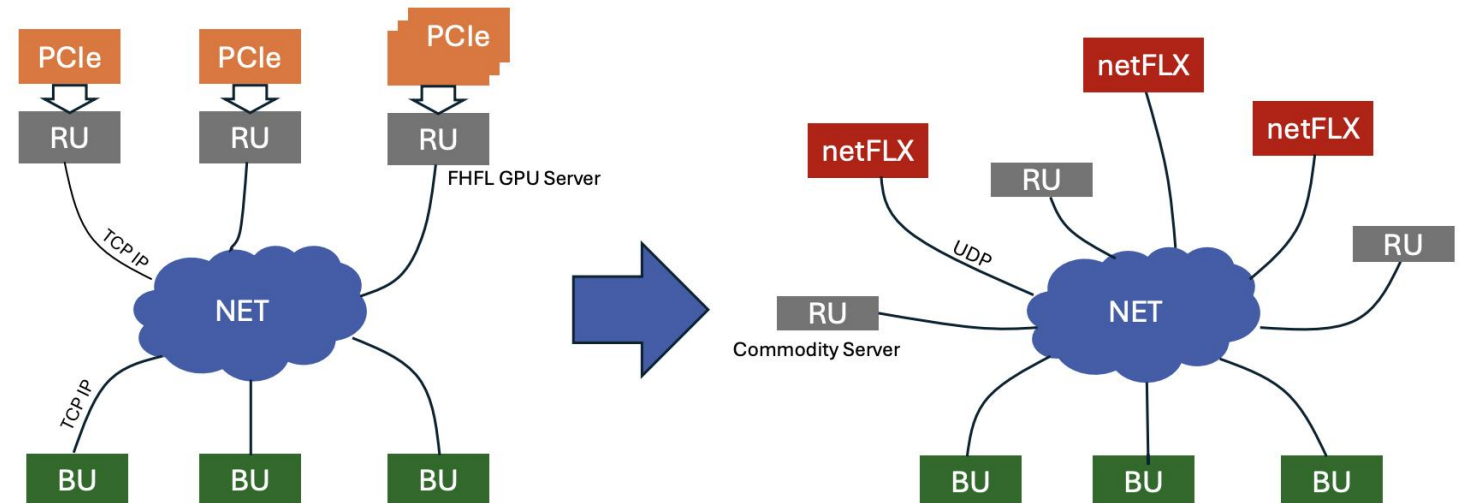


### HW TEAM PROPOSAL

- Paschalis Vichoudis/ CERN ESE / WP Lead
- Hao Xu, Shaochun Tang /BNL
- Julien Langouët, Felipe Vaccari, Franck Salomon, Kevin Arnaud,.. / IN2P3
- Mechanics\* & cooling\* TBD
- Colleagues from FW WP – Frans Schreuder, Filippo Costa, Paolo Durante

### FW TEAM PROPOSAL

- Frans Schreuder, xx/ Nikhef
- Guillaume Vouters, Frédéric Hachon, .. / IN2P3
- xxx / BNL
- Paolo Durante, Alberto Perro / CERN LHCb
- Filippo Costa, xx / CERN ALICE
- Enrico Gamberini, xx / SME
- Jose Javier Gonzalez Abascal /SHiP
- Colleagues from HW WP – Paschalis Vichoudis, ..



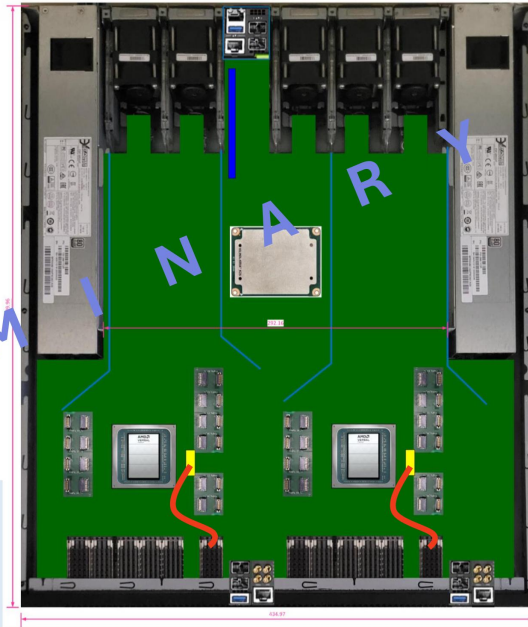
# 下一代netFELIX

how could it look like?

And how much could it cost?

hmmm, very difficult to estimate at this stage. However, we are aiming at ~20k

- assuming we can get an FPGA deal similar to the ATLAS FELIX one



02-Feb-2026

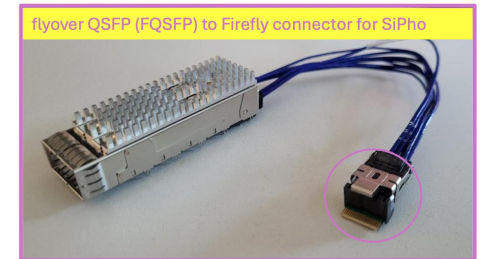
netfelix-management@cern.ch

6

## TECH optics: LpGBT & SiPho in a single design?

candidate solution: single PCB layout with FPGA connected to Samtec Firefly sockets, with two connectivity options:

1. LpGBT: CERNB-Y12 optical engine directly mounted to the two 12-way connectors (Rx12 & Tx12)
2. SiPho: Flyover QSFP cable connected to the Rx12 (compatible with F-QSFP end-connector) & CWDM QSFP module inserted in the cage



NOTE: For future applications that require standard bidirectional QSFP connectivity, FQSFP variants with two end connectors are available to interface with both the Rx and Tx Firefly sockets.

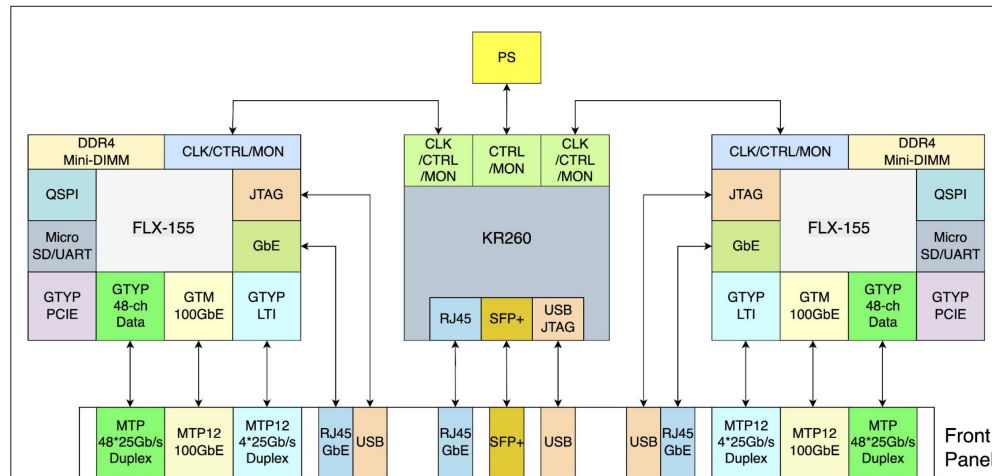
Paschalis Vichoudis (CERN)

14



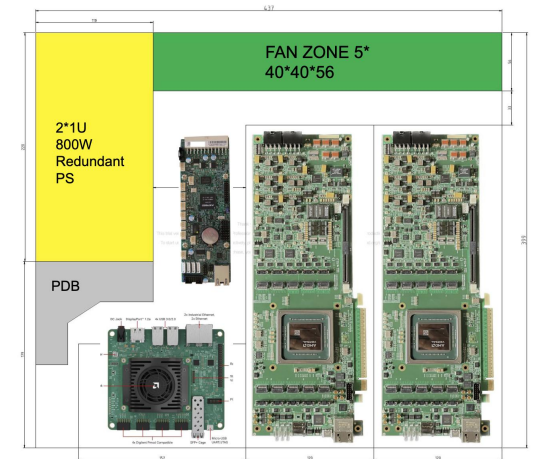
# 下一代netFELIX

## Block diagram of FELIX in 1U Chassis

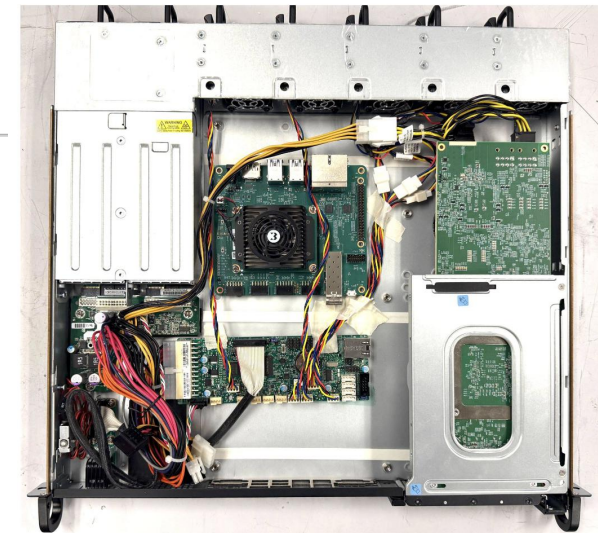


## Demonstrator

- Standard 1U commercial chassis
- 1U 800W Redundant Power Supplies with PMBUS
- Intelligent chassis management
- 1x timing/control interface and distribution card
- 1 or 2x FLX-155 for data readout

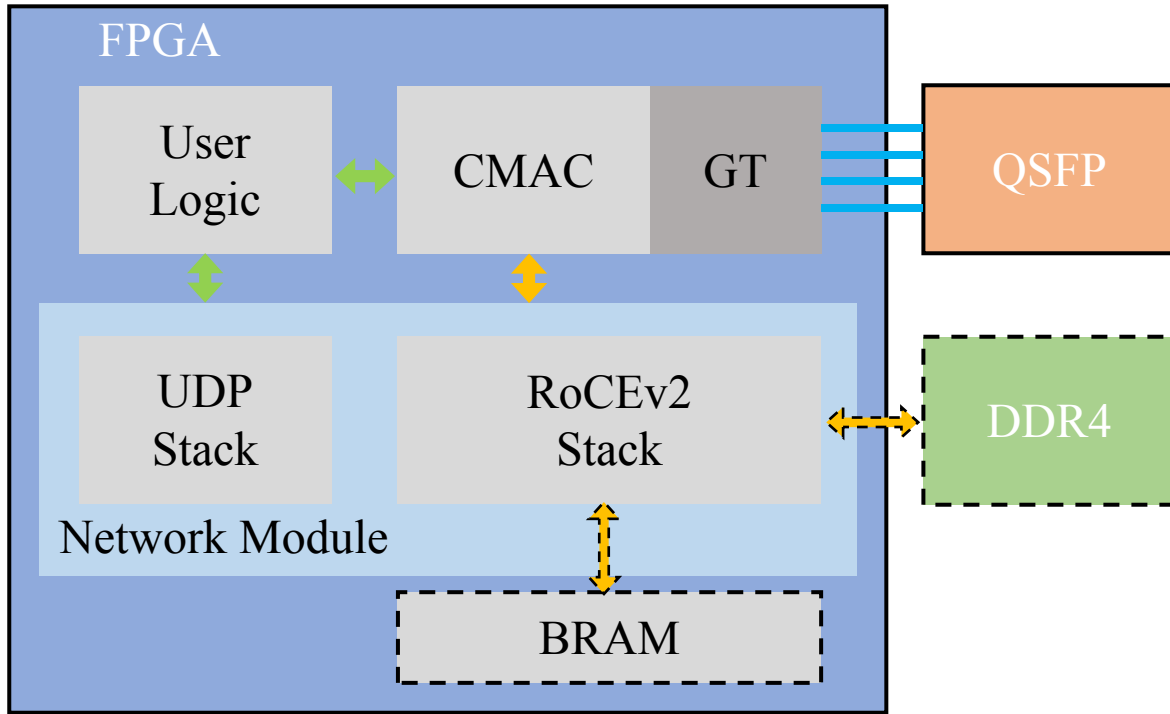


from Hao Xu (BNL)



2026/4/20

# RDMA技术的验证@CCNU



## ❑ 基于DavOS进行优化

- 支持100Gbps的TCP、UDP、RoCEv2协议
- 建链方式优化调整

## ❑ 缓存模式

### ➤ DDR4

- 单内存条（4GB）可实现数十毫秒的缓存
- 单个内存条难以支持双向同时传输
- 逻辑复杂，读写延时较高

### ➤ FPGA片内BRAM

- 带宽高且配置灵活
- AXIS协议传输，延时极低
- 占用大量内部资源



# RDMA技术的验证@CCNU

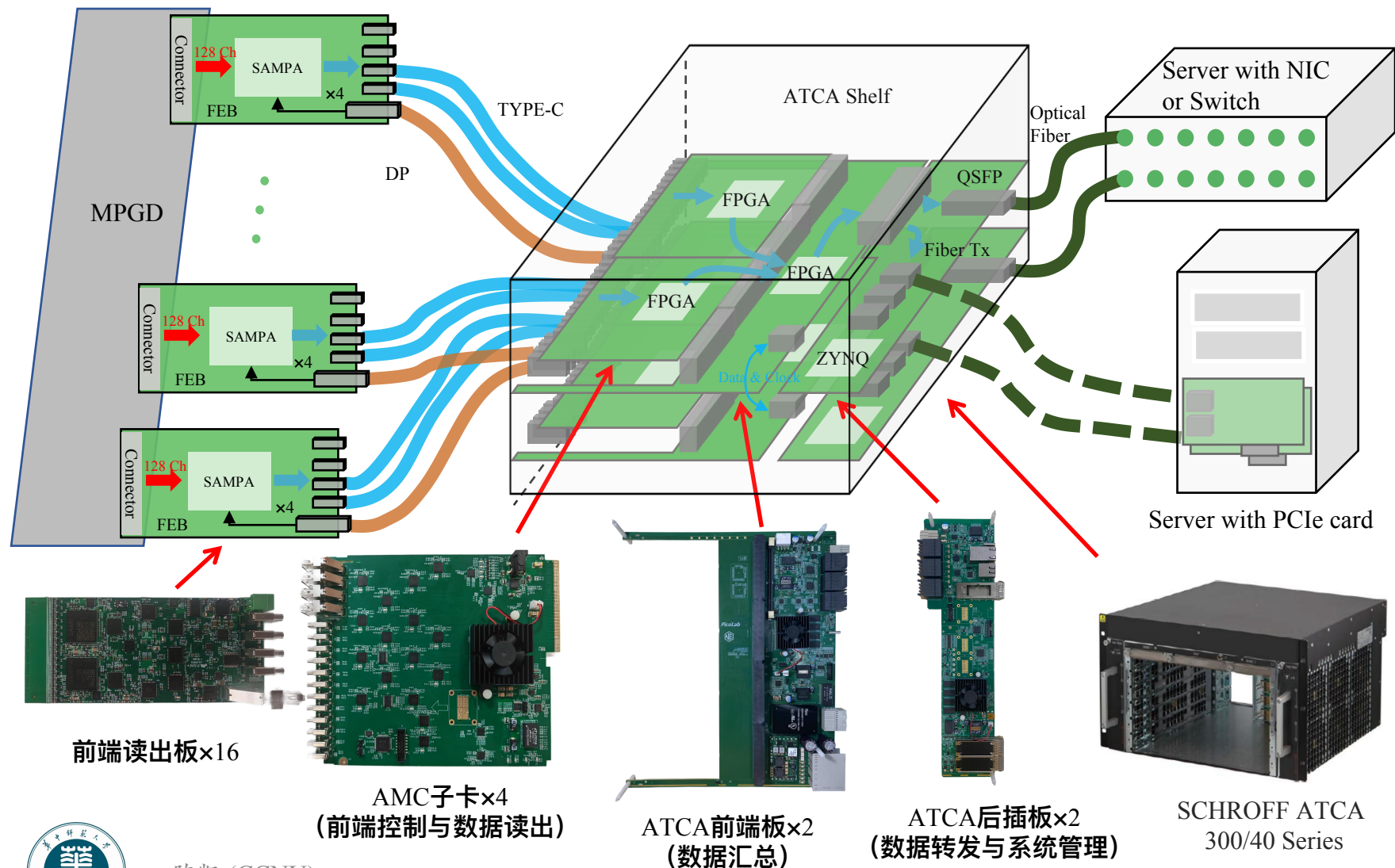
DDR4缓存			BRAM缓存		
FPGA → NIC	NIC → FPGA	双向	FPGA → NIC	NIC → FPGA	双向
97.95 Gbps	97.86 Gbps	FPGA → NIC 68.39 Gbps NIC → FPGA 39.75 Gbps	97.92 Gbps	97.48 Gbps	FPGA → NIC 96.40 Gbps NIC → FPGA 95.24 Gbps

## □ 测试平台:

- KU15P FPGA
- 单DDR4模块
- 主机端网卡: ConnectX-5
- DDR4 Module: Innodisk 16 GB DDR4 Mini-UDIMM VLP @ 2133MT/s
- 采用FPGA外部DDR4缓存时, 需优化多模块缓存结构



# RDMA应用——多通道MPGD读出



□ ~2000路MPGD读出系统原型样机

□ 后端读出方案

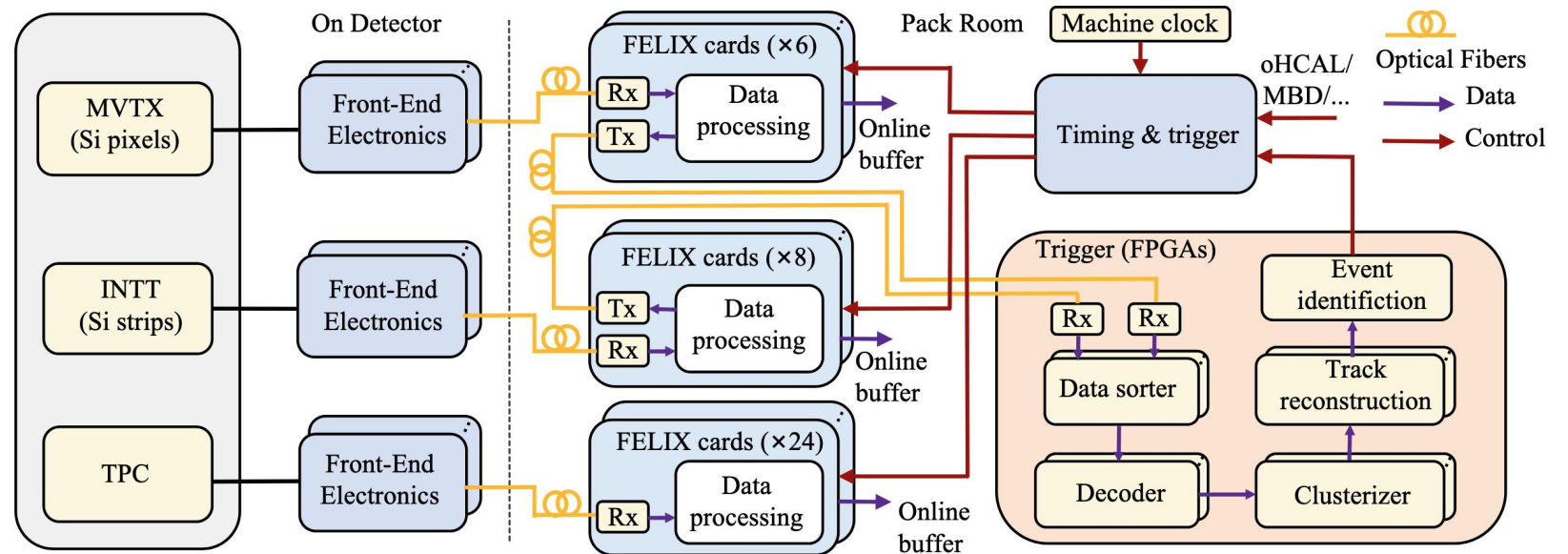
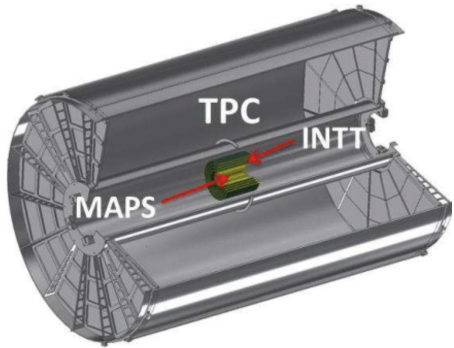
➤ 基于RDMA, 架构简单

➤ 基于PCIe, 技术成熟

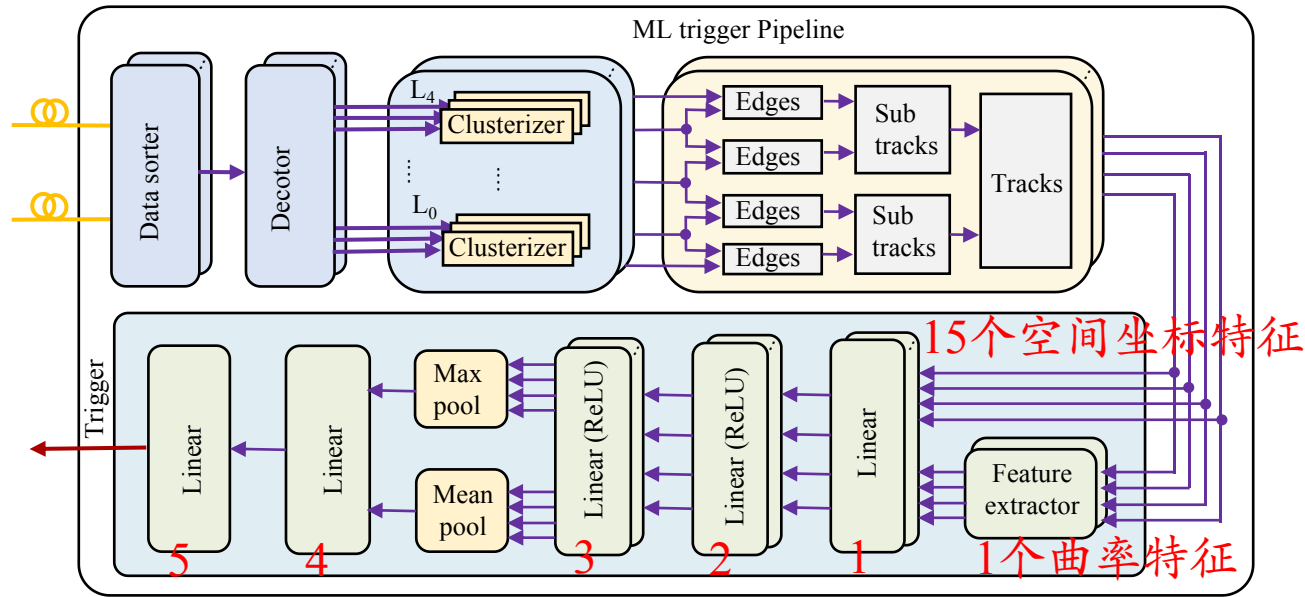


# 异构计算与AI的应用

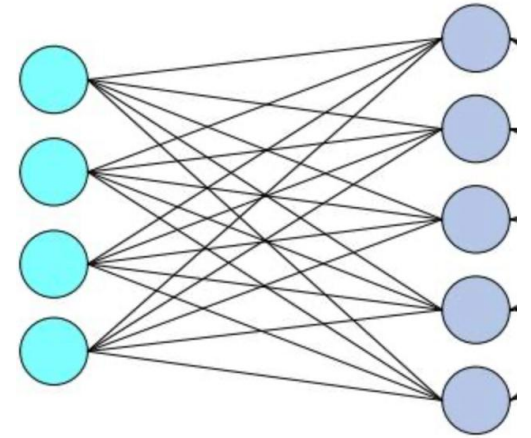
- FPGA长期以来被大量应用于第一级硬件触发与数据获取系统硬件接口
  - AI技术的发展，近年来推动了基于AI的算法在第一级硬件中FPGA的部署
  - 后级处理，早期以CPU为主，LHCb等实验开始大量应用GPU进行加速
    - Xilinx等生产的FPGA加速卡也开始在这些HLT中得到应用



# sPHENIX场景下的在线重味触发FPGA算法



输入维度

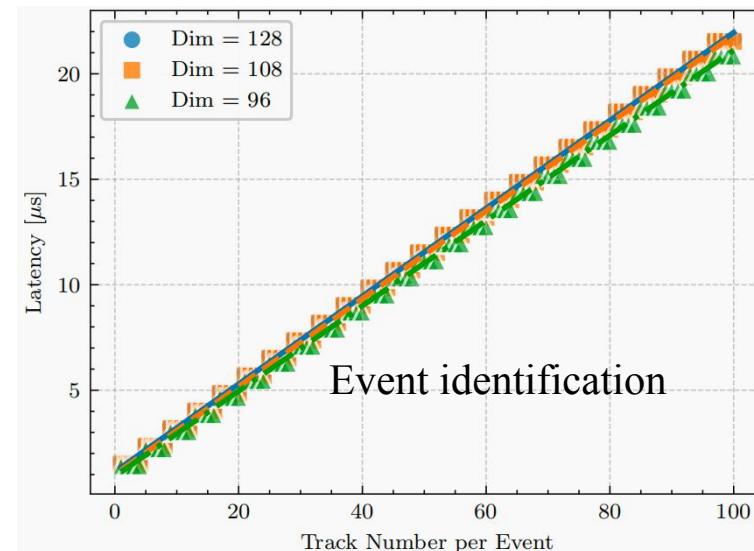
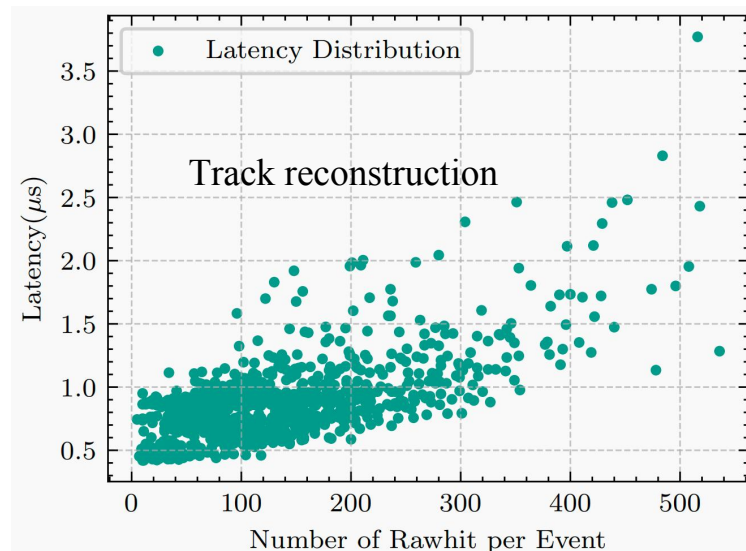
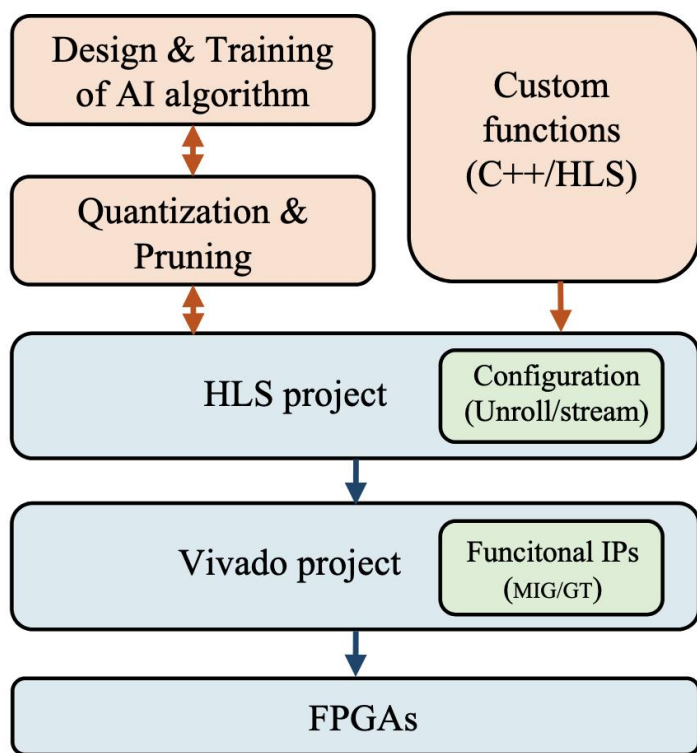


Linear结构 (全连接层)

- ❑ Linear 1:实现维度转化和特征学习，输入维度为16(15+1)，输出维度为128
- ❑ Linear 2-3:内部隐藏层，实现特征学习，输入和输出维度为128
- ❑ Linear 4-5:实现维度转化和特征学习
  - 4:输入维度256，输出维度128
  - 5:输入维度128，输出维度2



# sPHENIX场景下的在线重味触发FPGA算法



Dim.	BRAM	DSP	LUT	FF	Eff	Pur
96	1400	7,187	1,006k	945k	90.9%	98.9%
108	1400	7878	1,262k	1,023k	95.9%	98.9%
128	1400	8,971	1,646k	1,061k	98.0%	99.8%

信号事例：背景事例=1:1 **b夸克**

实际约1:100 (纯度50% / 50% / 88%)

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# 小结

- 加速器能量、亮度，探测器性能等升级持续提升对后端系统的要求：
  - 读出带宽
  - 时钟同步精度
  - 探测器控制
- 发展趋势
  - 跨实验的通用化设计
  - 工业届最前沿技术
  - 无触发模式
  - 异构计算在各级触发及数据处理中的灵活应用：FPGA/GPU/CPU

*Thank You!*

