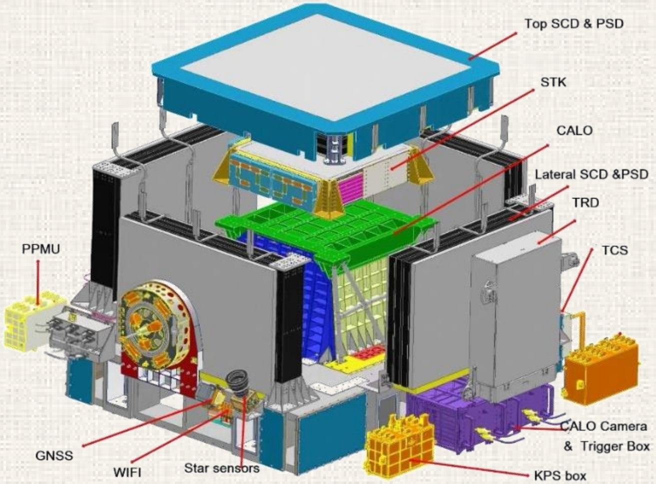
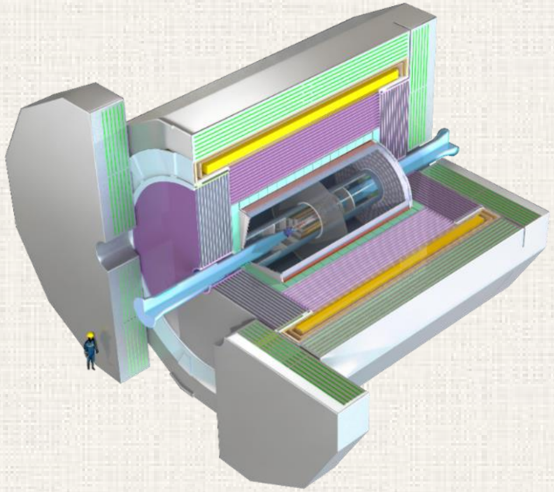
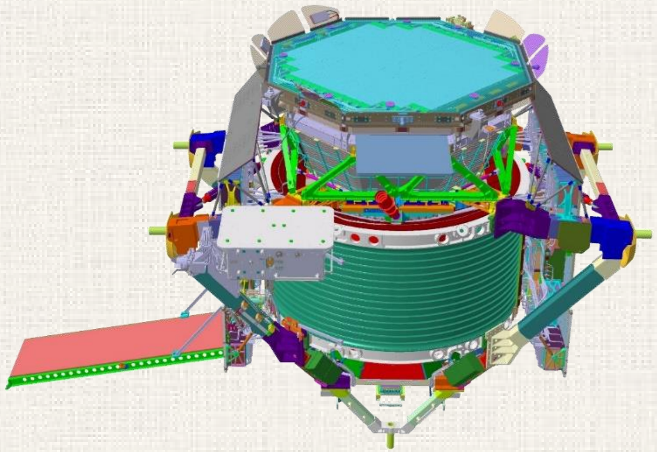




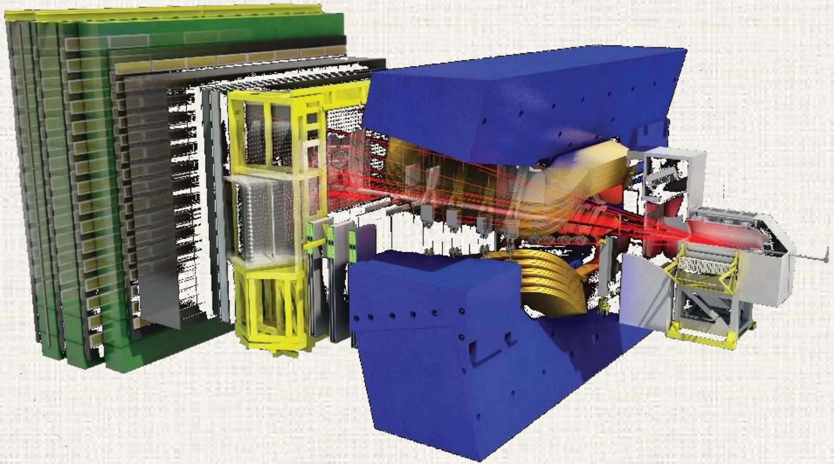


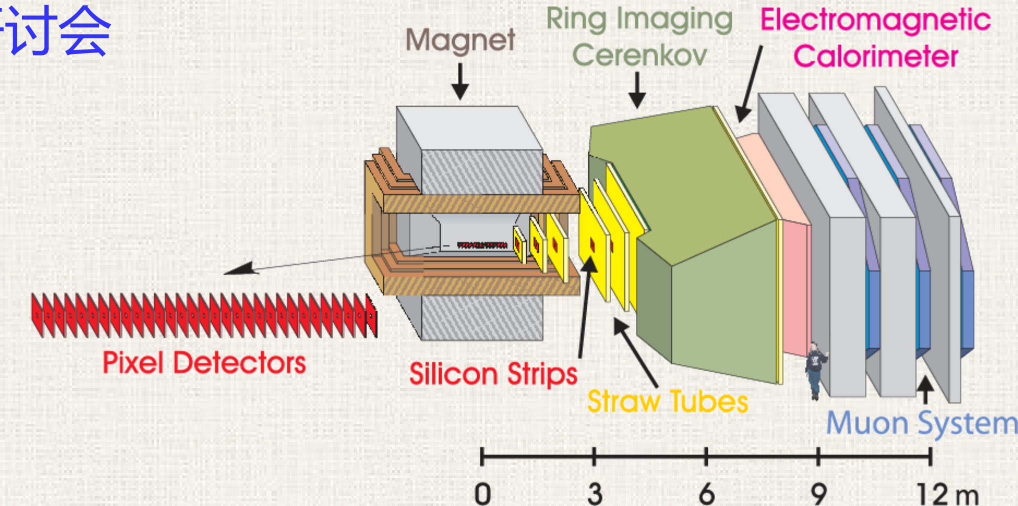
粒子物理实验中硅探测器

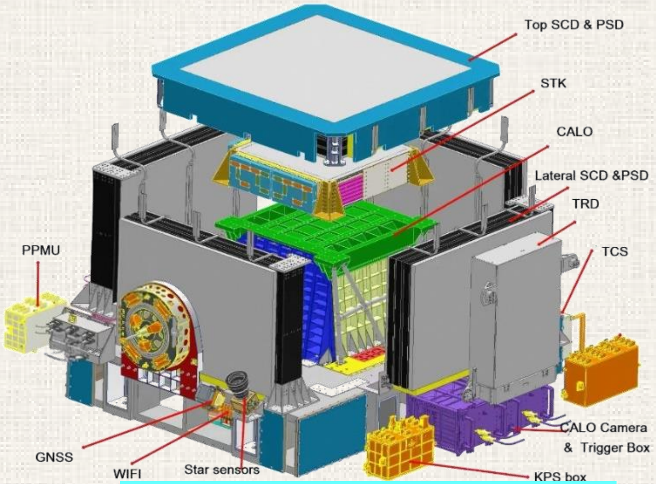
王建春 / 高能物理研究所

第六届半导体辐射探测器研讨会

2026.04.16-19, 上海

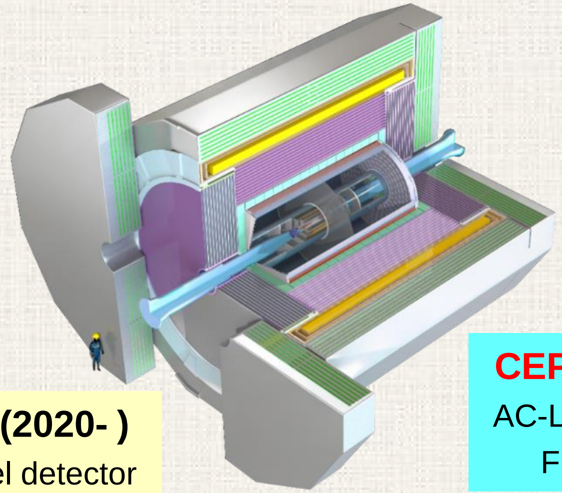






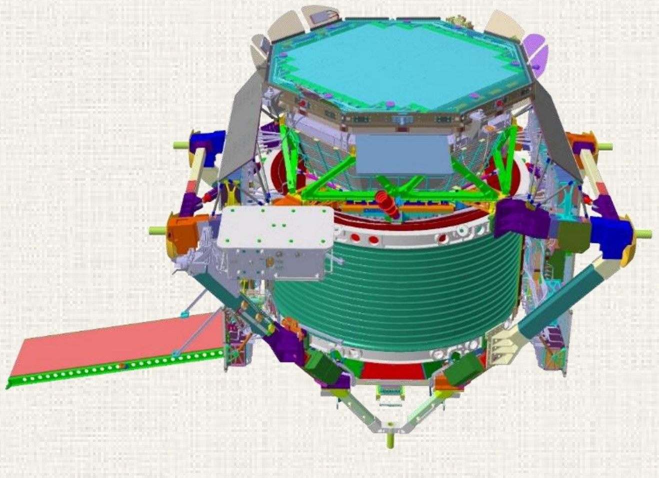
HERD SCD, STK (2025-)
Strip detector, FE ASIC readout

CEPC VTX (2020-)
Monolithic pixel detector



CEPC OTK (2024-)
AC-LGAD strip detector
FE ASIC readout

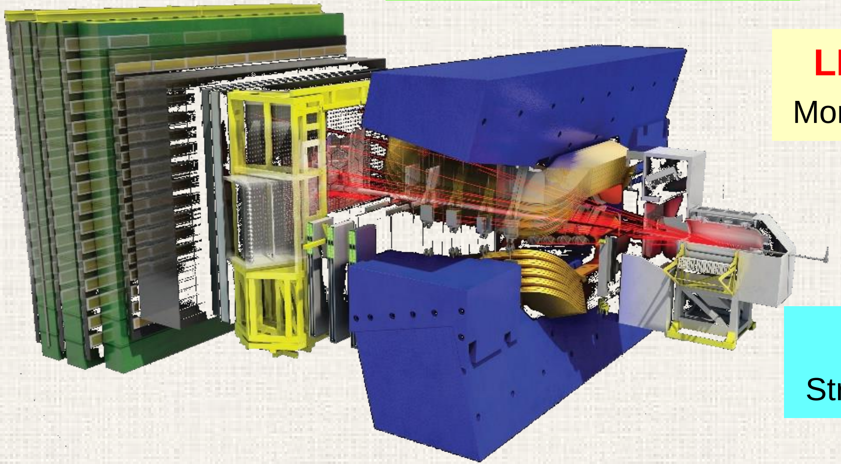
CEPC ITK (2022-)
Monolithic pixel detector



AMS L0 (2021-2027)
Strip detector, FE ASIC readout

LHCb VELO (2005-2012)
Strip detector, BE ASIC readout

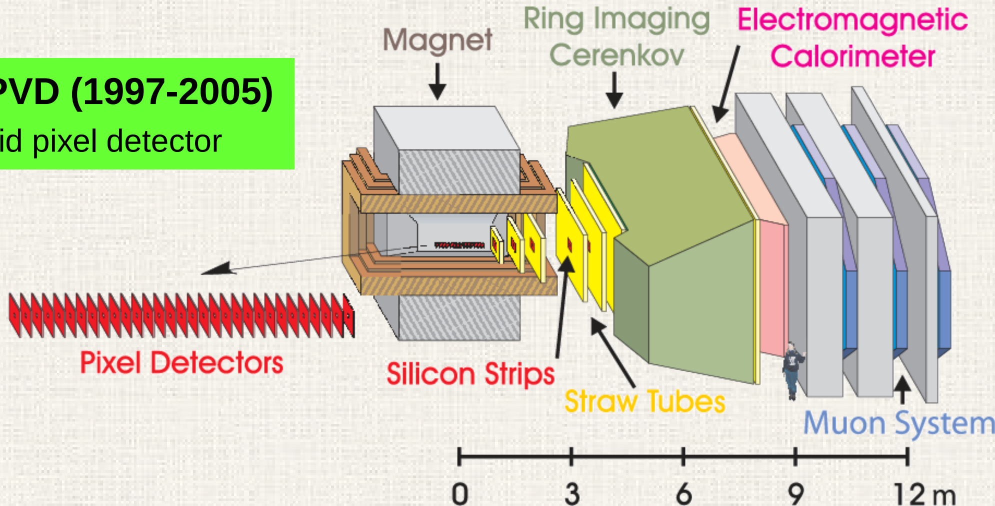
LHCb VP (2010-2012)
Hybrid pixel detector

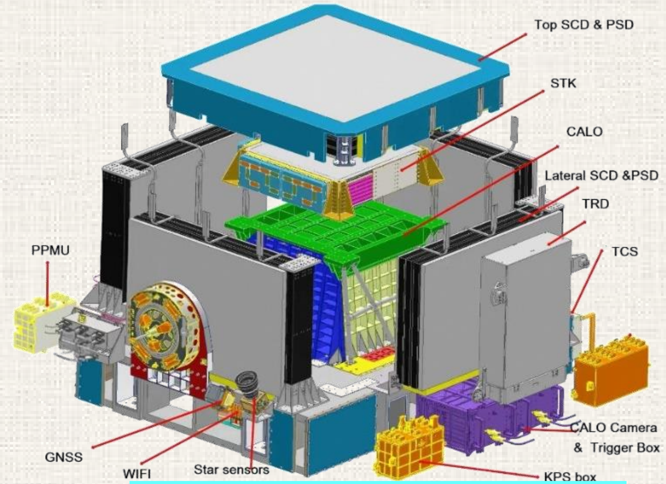


LHCb UP (2020-)
Monolithic pixel detector

LHCb UT (2010-)
Strip detector, FE ASIC readout

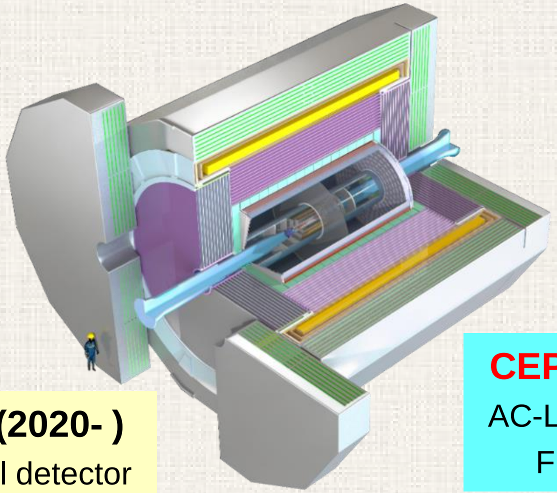
BTeV PVD (1997-2005)
Hybrid pixel detector





HERD SCD, STK (2025-)
Strip detector, FE ASIC readout

乔锐



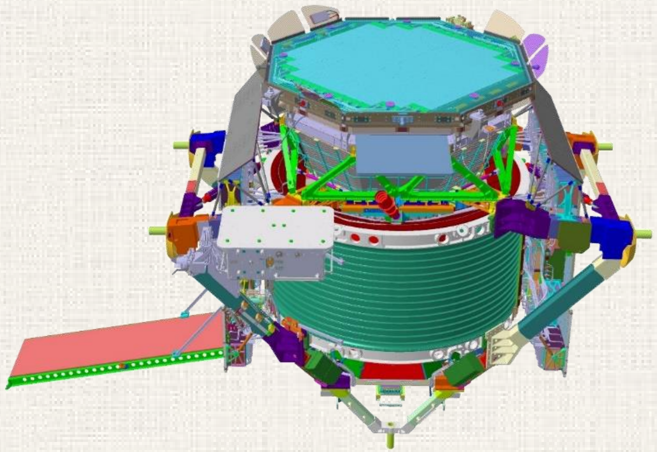
CEPC VTX (2020-)
Monolithic pixel detector

CEPC ITK (2022-)
Monolithic pixel detector

李一鸣

CEPC OTK (2024-)
AC-LGAD strip detector
FE ASIC readout

严琪、严雄波



AMS L0 (2021-2027)
Strip detector, FE ASIC readout

徐子骏

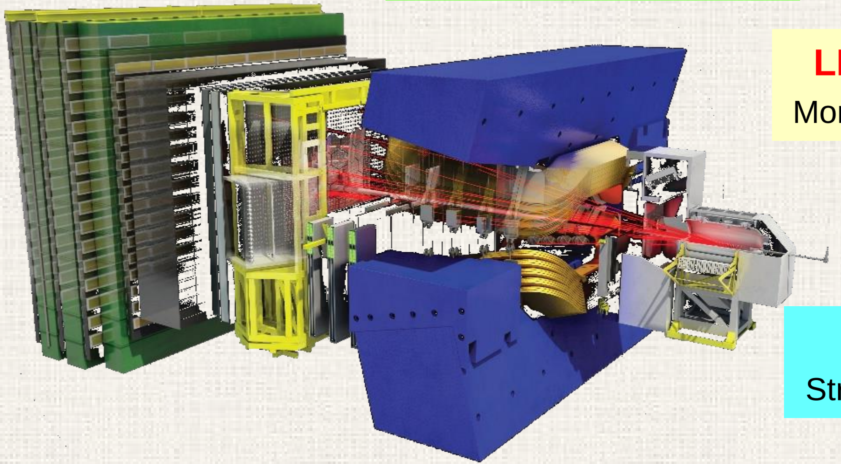
LHCb VELO (2005-2012)
Strip detector, BE ASIC readout

LHCb VP (2010-2012)
Hybrid pixel detector

周扬、张慧

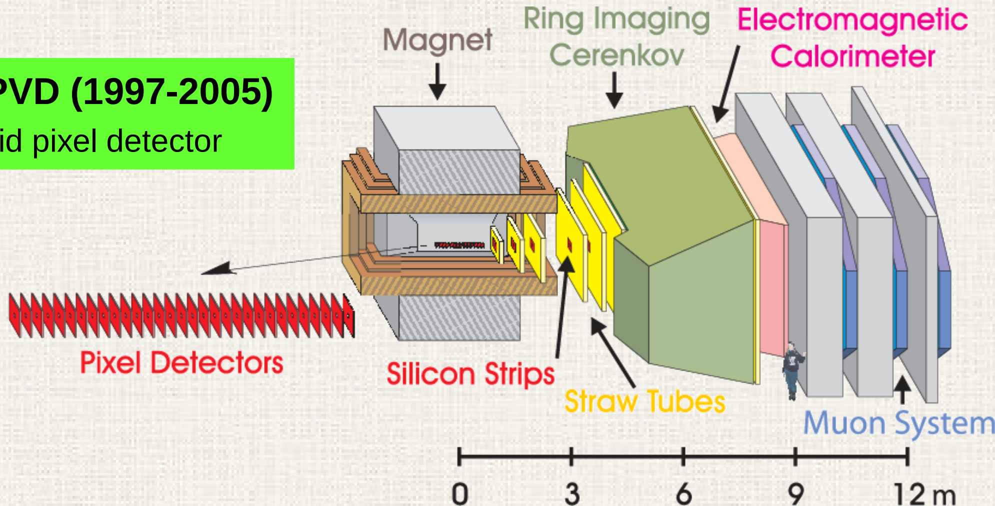
LHCb UP (2020-)
Monolithic pixel detector

袁煦昊



LHCb UT (2010-)
Strip detector, FE ASIC readout

BTeV PVD (1997-2005)
Hybrid pixel detector

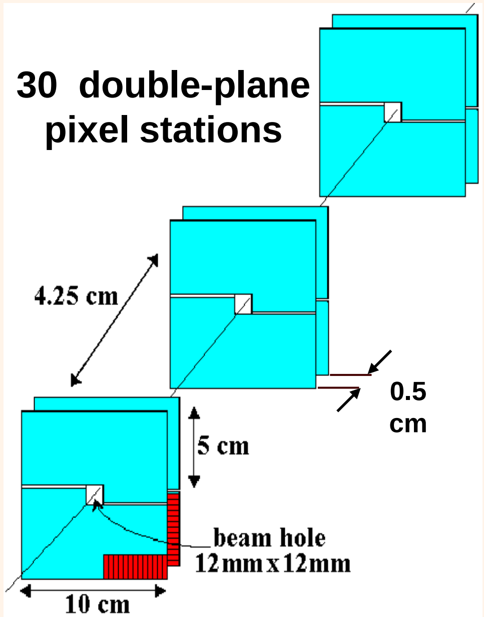


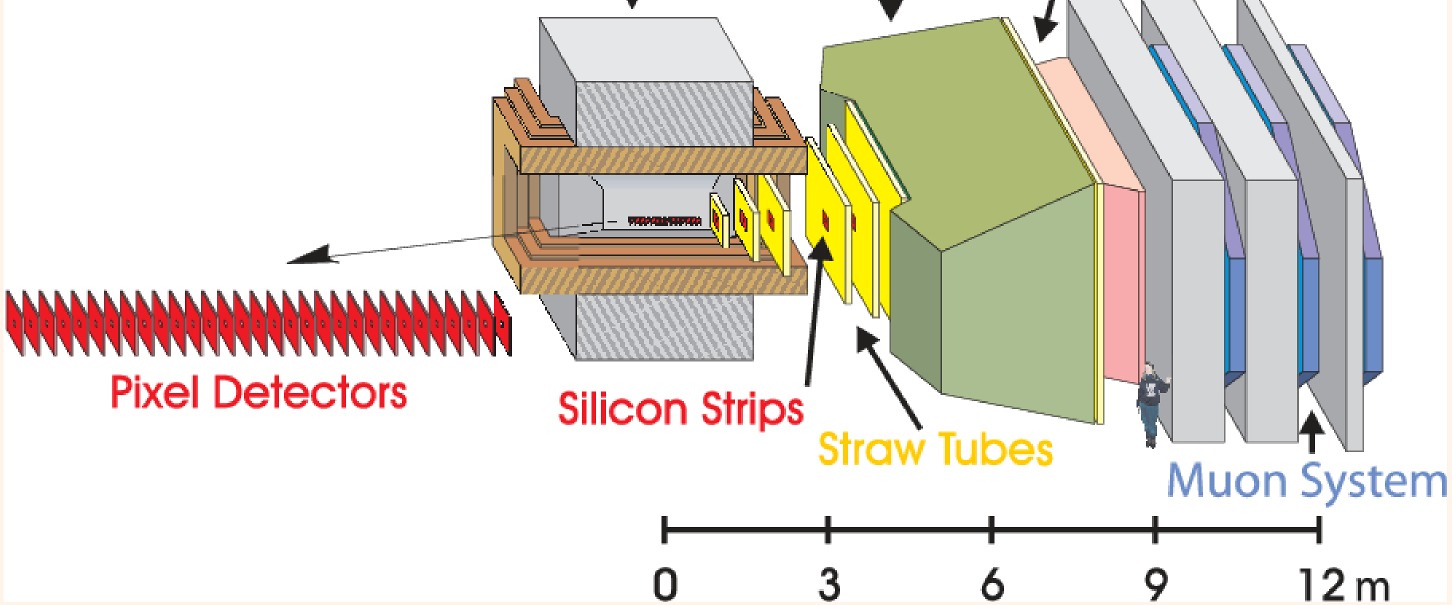
The BTeV Experiment

- Similar physics goal as the LHCb
- Key parameters
  - $p\bar{p}$ collisions @ 1.8 TeV
  - L ~ 2×10^{32} $cm^{-2}s^{-1}$
  - 132 ns bunch spacing
- Silicon pixel vertex detector in a magnetic field
- Deadtime-less trigger based on detached vertex

BTeV PVD (1997-2005)

NJU, SDU, USTC are founding members



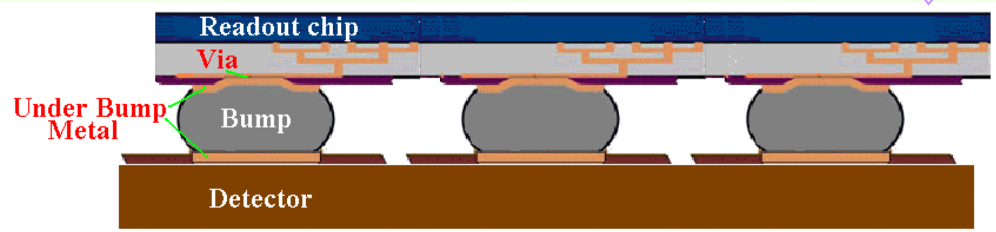


Hybrid Pixel Detector for BTeV

Readout Chip

0.25 μm CMOS process, ENC~100 e

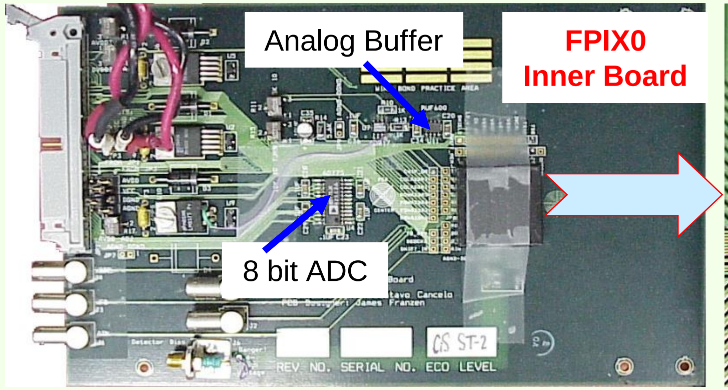
- FPIX0: 64×12 cells, 8-bit external ADC
- FPIX1: 160×18 cells, 2-bit internal FADC
- FPIX2: 128×22 cells, 3-bit internal FADC

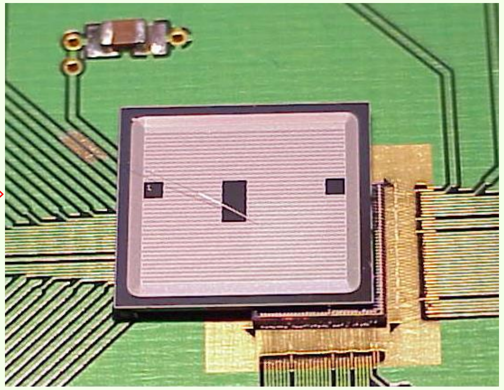


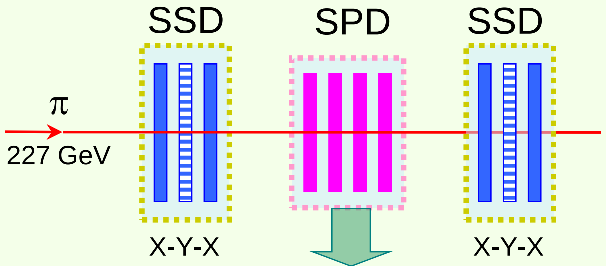
Pixel sensor (n^+np^+)

pixel size: 50×400 μm^2

- ST1-CiS p-stop
- ST2-CiS p-spray
- ST1-Seiko p-stop
- ST2-Seiko p-spray

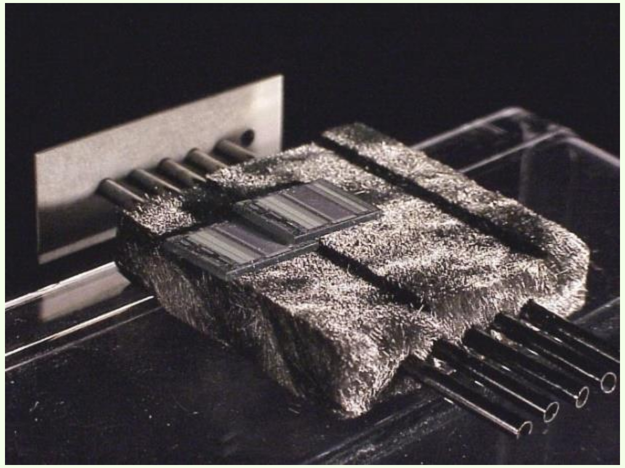


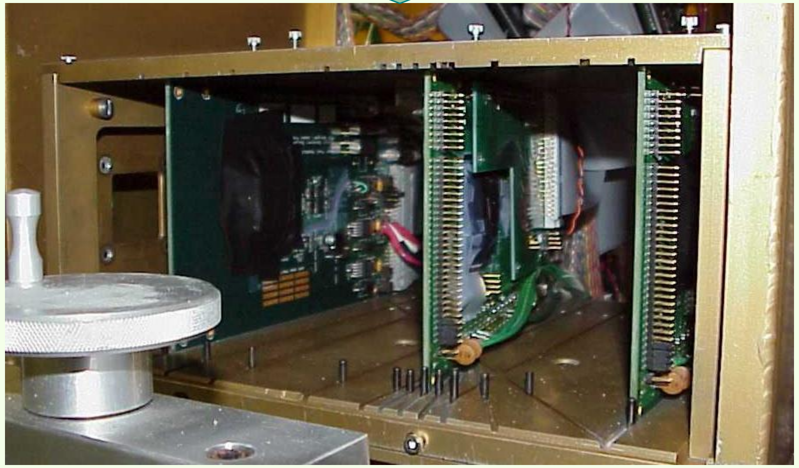




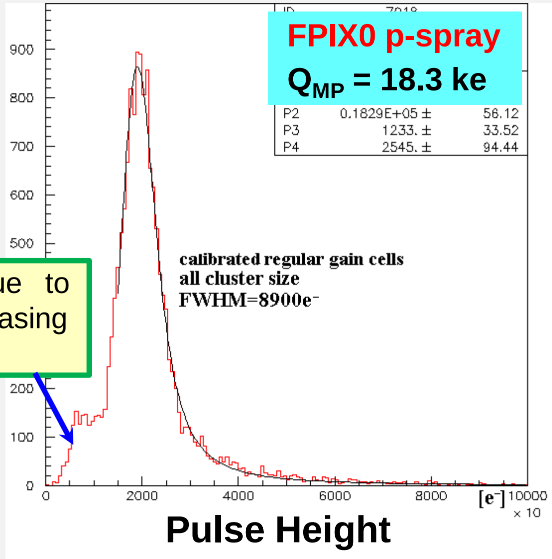
Shingled surface support for overlaps of multi-chips

Total ~ 0.9% X_0 / 2-layer

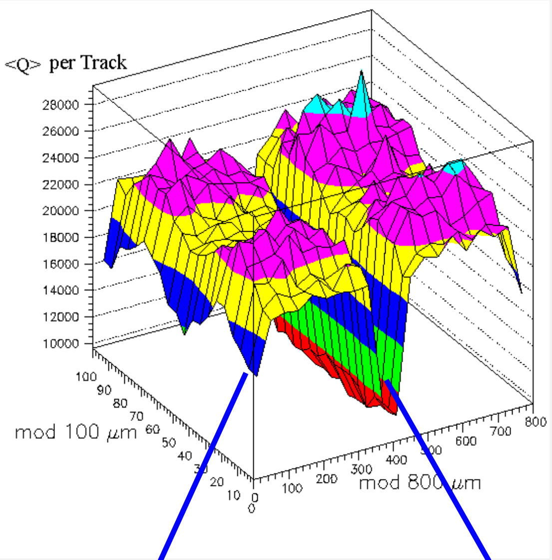


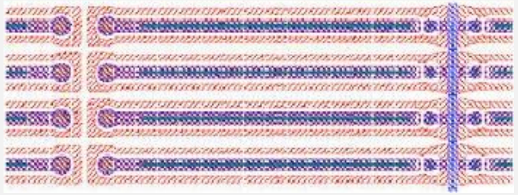


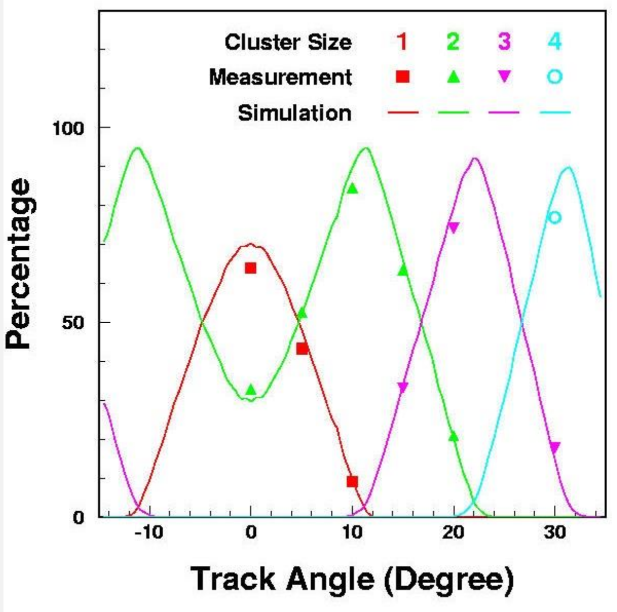
BTeV Pixel Vertex Detector R&D

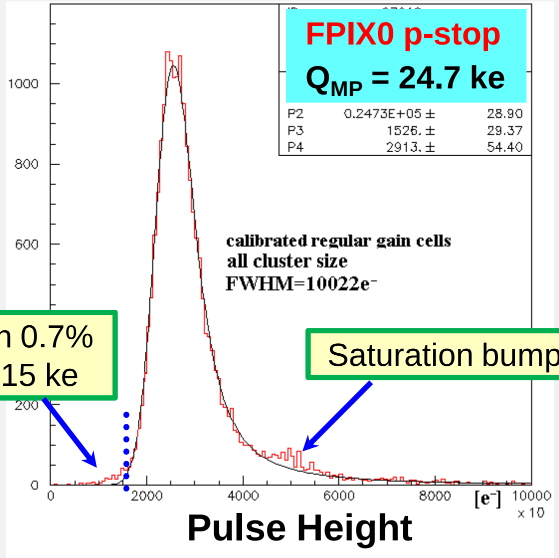


Charge loss due to punch-through biasing and floating atoll





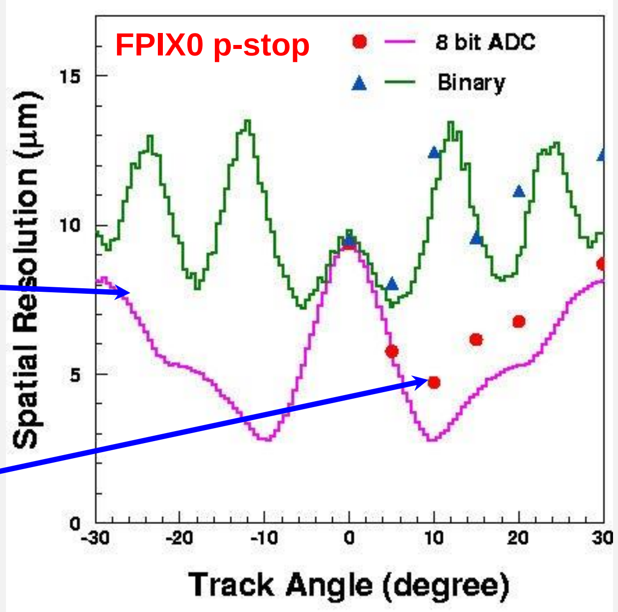




Less than 0.7% with Q < 15 ke

Saturation bump

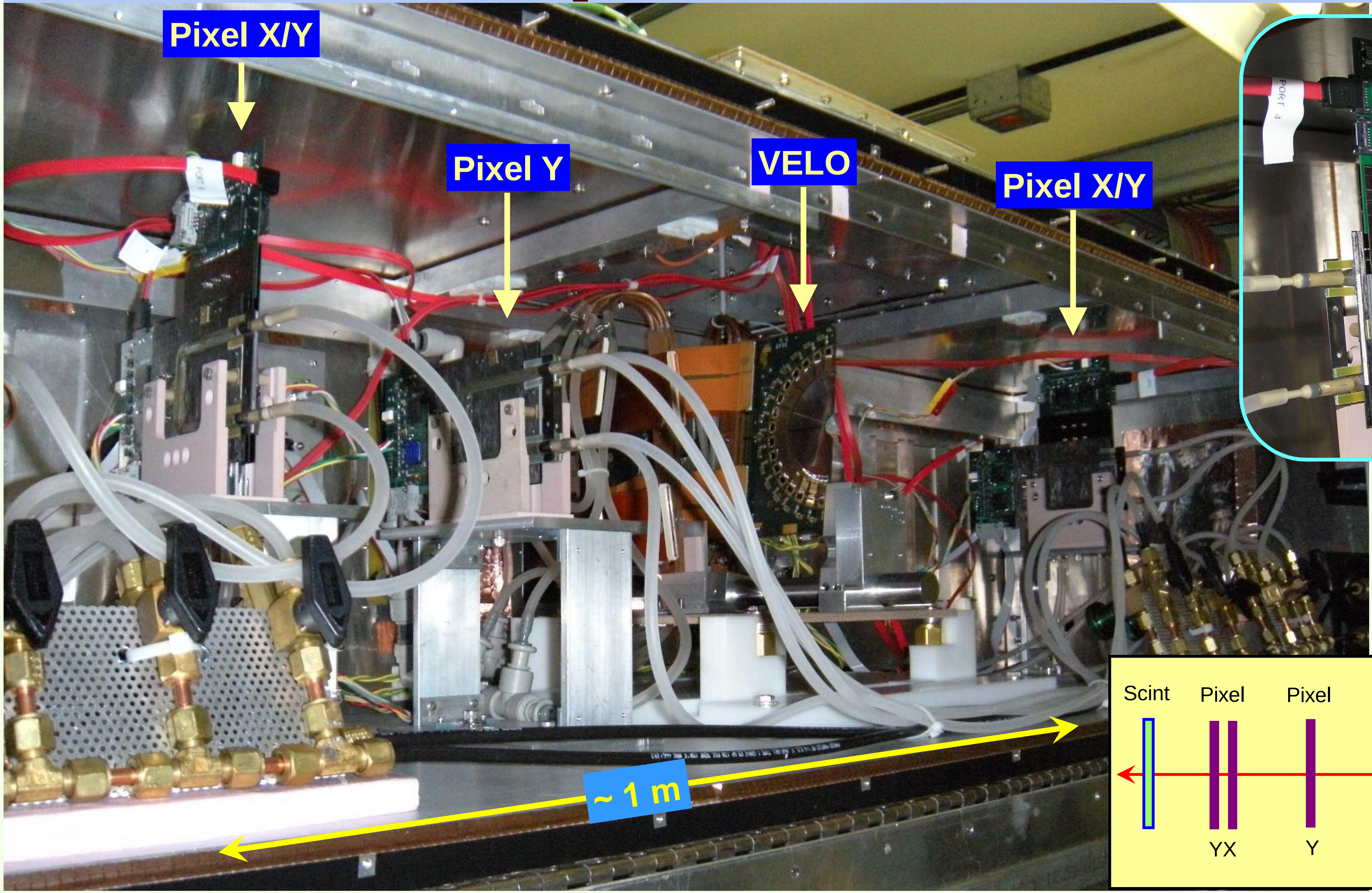
MC simulation

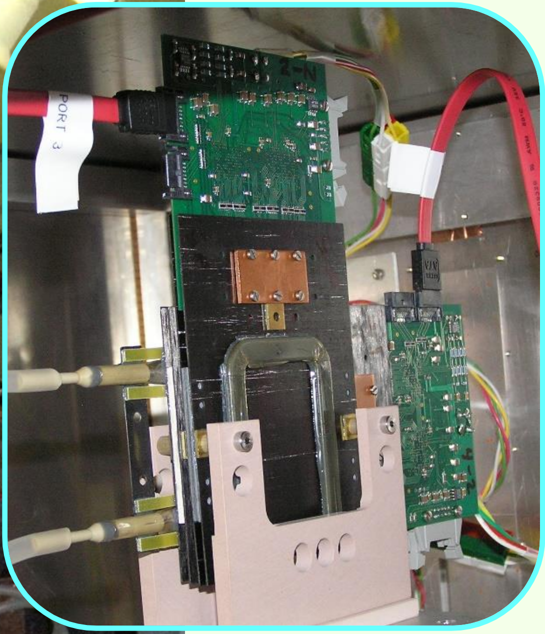


Measurement

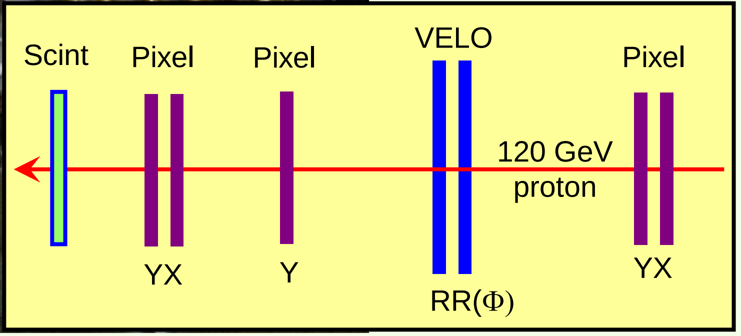
(including tracking error)

A Telescope of BTeV Pixel Stations



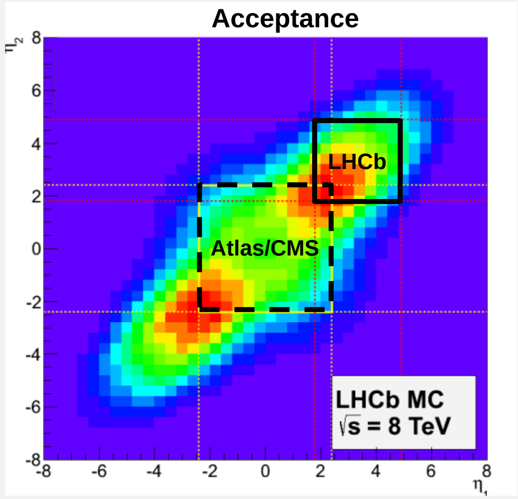


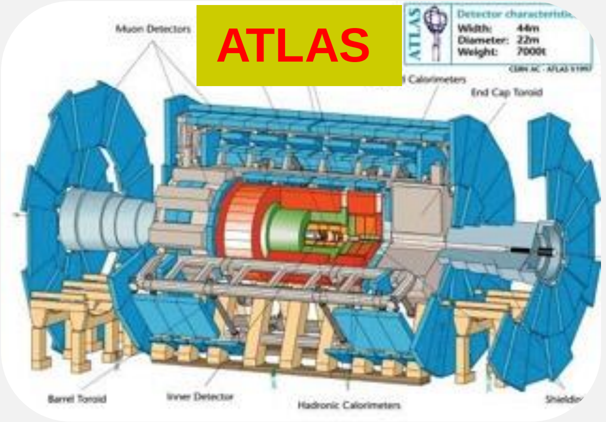
With
David Christian
and …

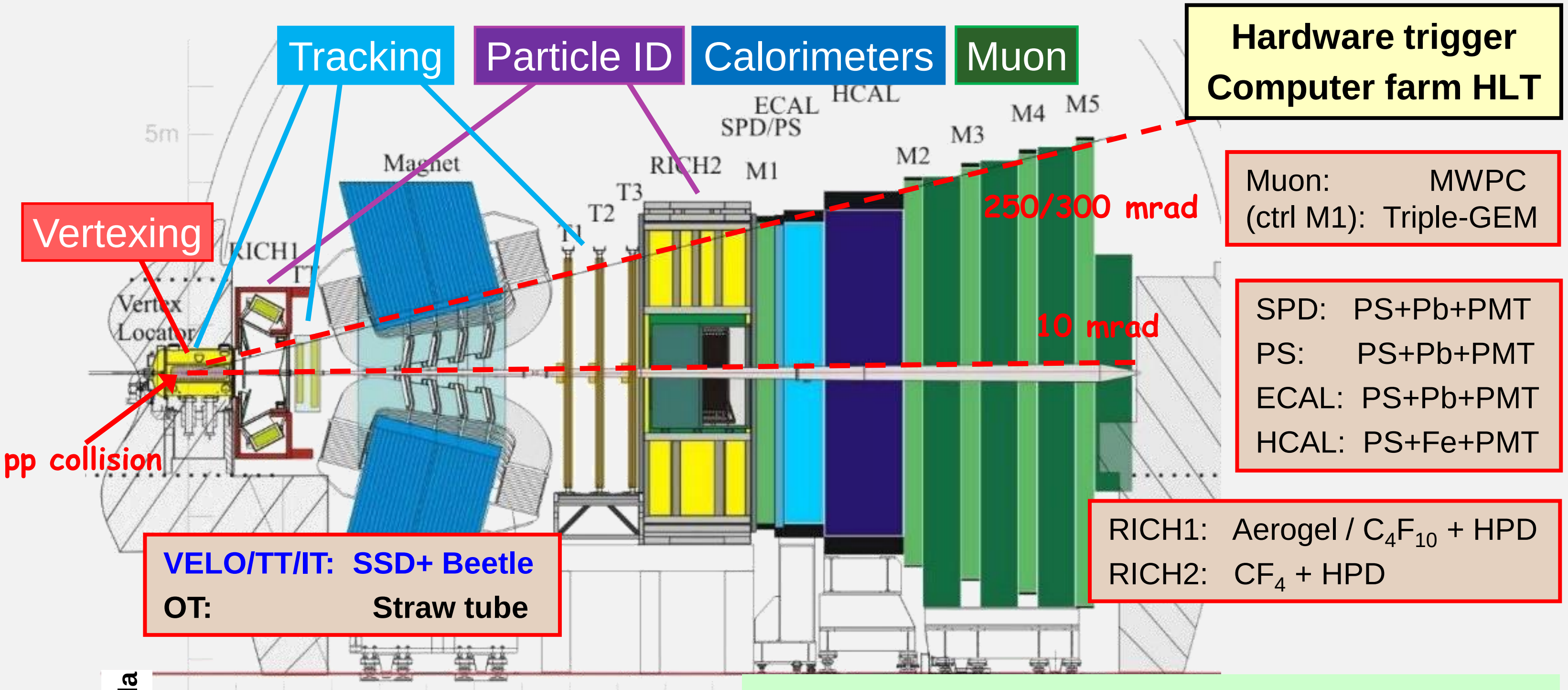


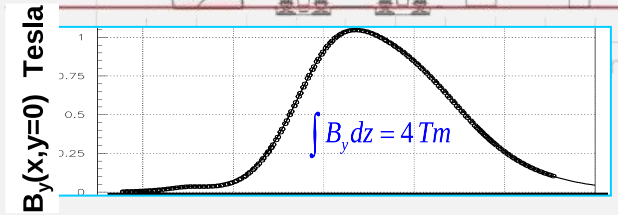
The LHCb Experiment

- The LHCb detector covers the forward region. This is driven by the physics goals: to study b & c sectors on CP-violation, rare decays, & search for new physics.
- Correlated production of $b\bar{b} \Rightarrow$ flavor tagging. Boost in Z $\Rightarrow$ decay length measurement.





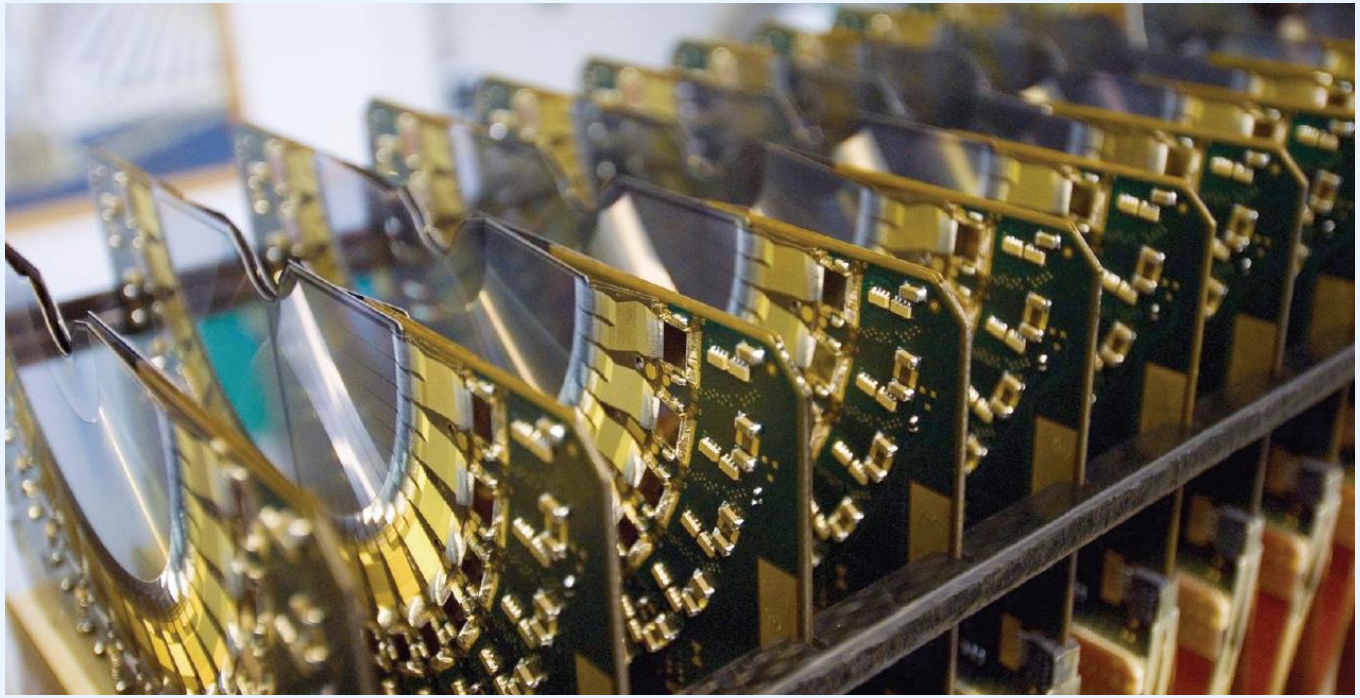




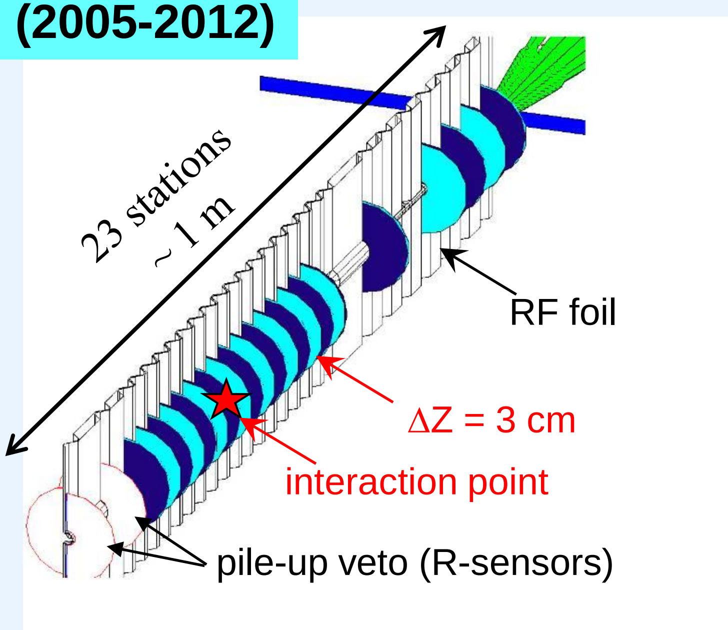
- $\Delta p/p = 0.5\%$ at <20 GeV, 1.0% at 200 GeV
- IP resolution ~ 15 + 29/p_T [GeV/c] μm
- Decay time resolution $45\ fs$ (e.g. $B_s \to J/\psi\ \phi$)
- Kaon ID ~ 95% for 5% $\pi \to K$ mis-ID probability

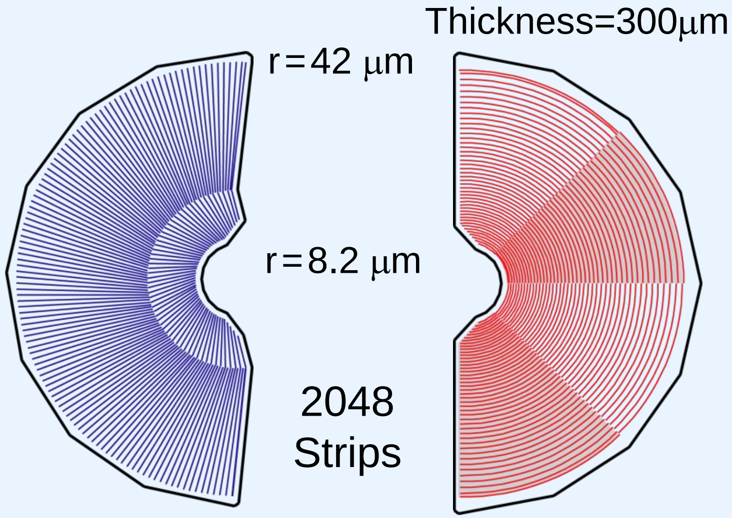
LHCb VELO Detector

- SSD n+ in n-bulk sensors, max fluence ~$7\times10^{14}\, n_{eq}\mathrm{cm}^{-2}$
- R-Φ geometry, 40–100 μm pitch.
- Serialized (×32) **differential analog output** from Beetle ASICs
- Optimized for
  - Tracks originating from beam-beam interactions
  - **Fast online 2D (R-z) tracking**
  - Fast offline 3D tracking in two steps (R-z then ϕ)

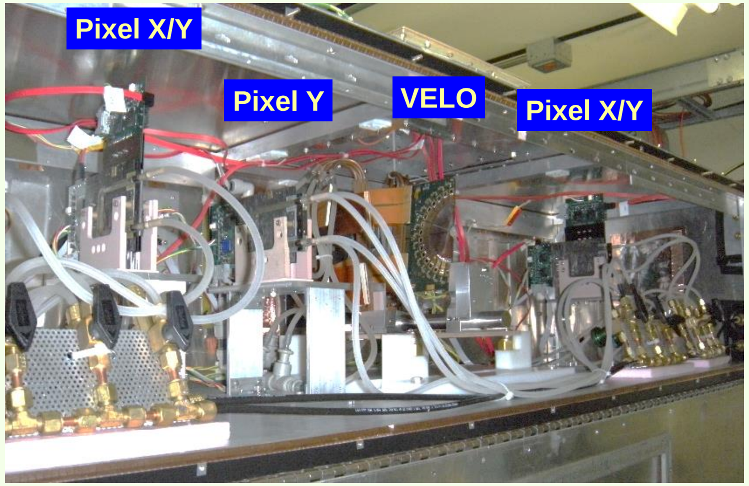


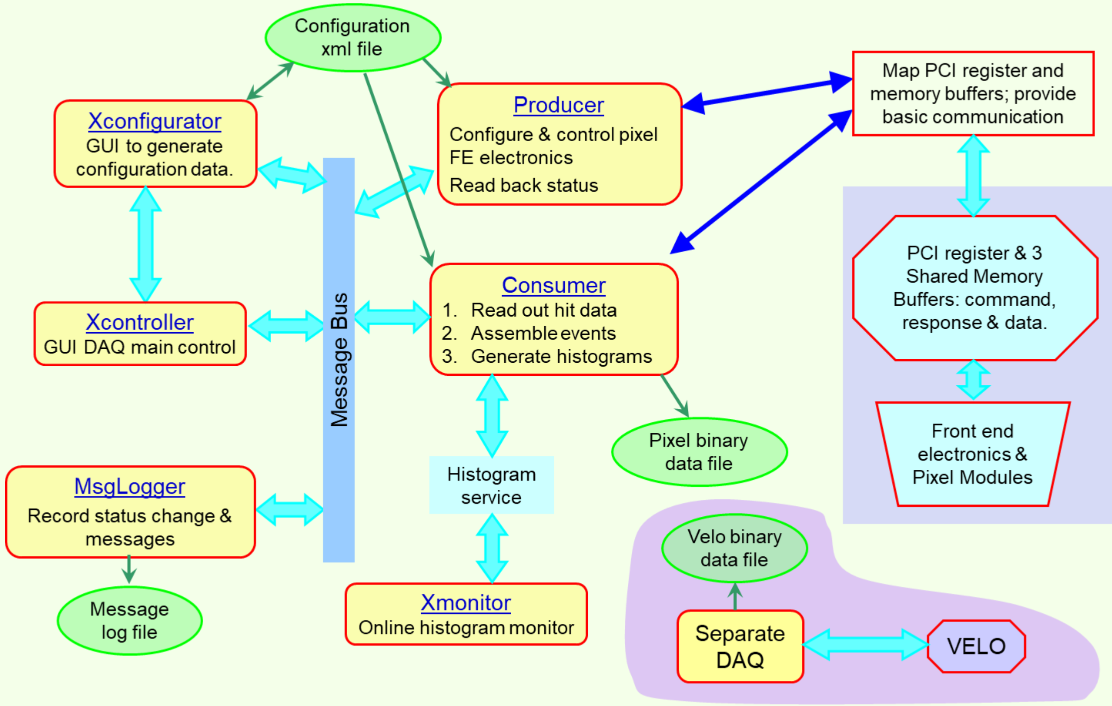
LHCb VELO (2005-2012)

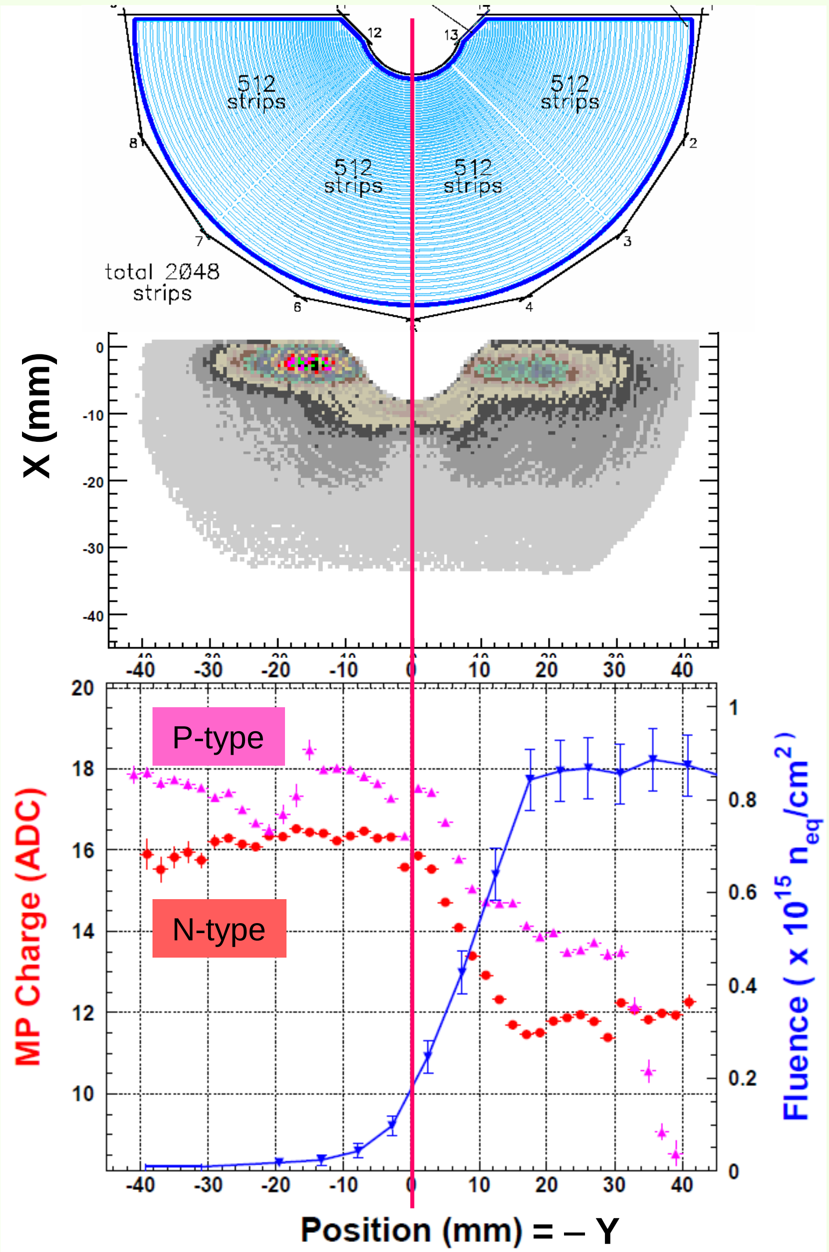




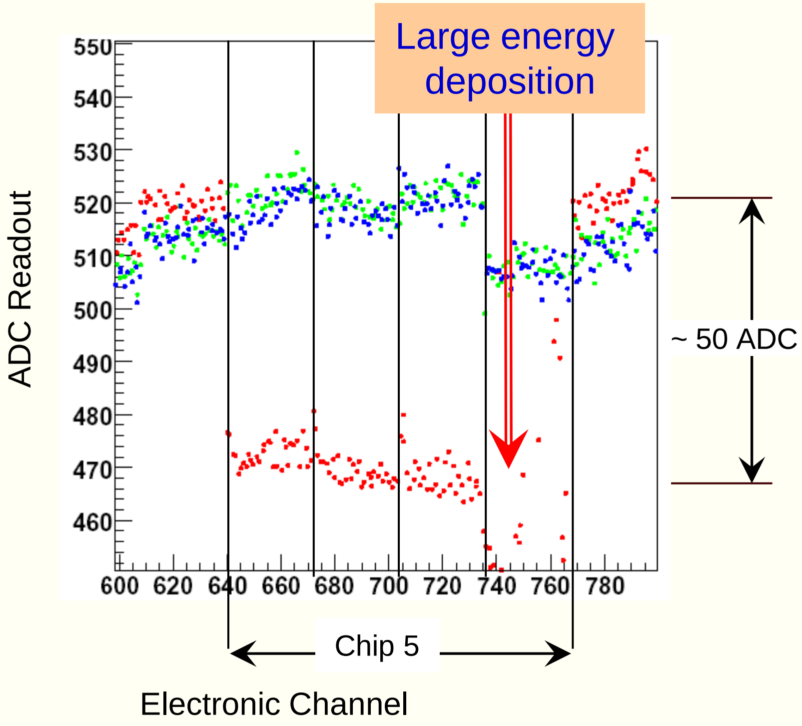
VELO Testbeam at FNAL



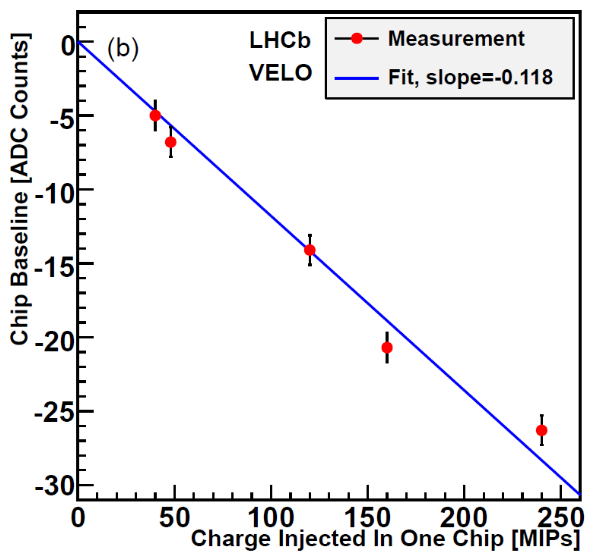


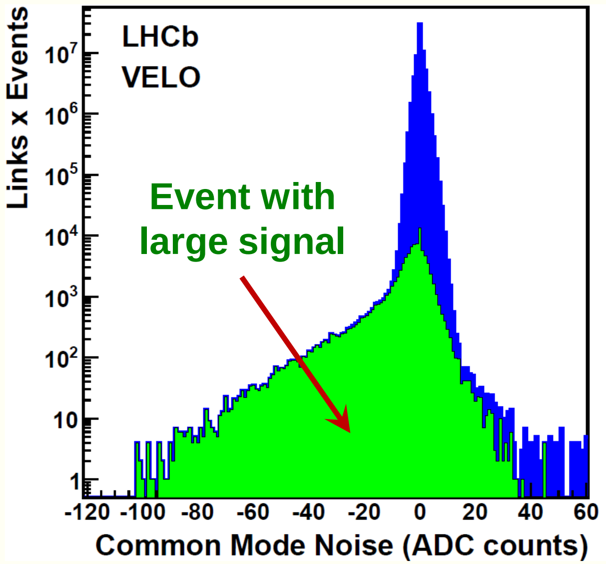


Unexpected Effects in Beetle ASICs



There large energy deposition in a few strips, resulting in the common pedestal to drop in the whole chip (**JC effect**)





Firmware Algorithm

$$sum = \sum \begin{cases} data(i) & -127 < data(i) < t1 \\ 0 & others \end{cases}$$

$$CM1 = (sum + 16) >> 5$$

$$sum = \sum \begin{cases} data(i) & |data(i) - CM1| < t2 \\ CM1 & others \end{cases}$$

$$CM2 = (sum + 16) >> 5$$

$$sum = \sum \begin{cases} data(i) & |data(i) - CM2| < t3 \\ CM2 & others \end{cases}$$

$$CM3 = (sum + 16) >> 5$$

$$N3 = N\left(|data(i) - CM2| < t3\right)$$

$$Nrec = N \begin{cases} data(i) \le ts \quad \& \\ data(i) - CM3 > ts \end{cases}$$

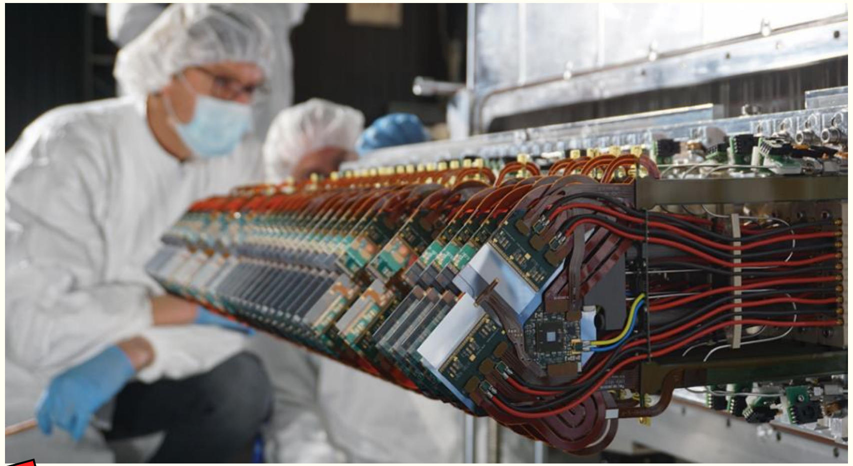
$if\ (N3 \ge ncms\ \&\ Nrec \le nrec)$

$\quad data(i) = data(i) - CM3$

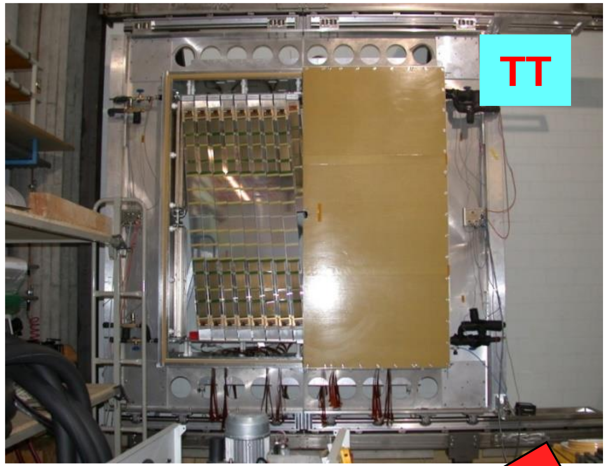
$else$

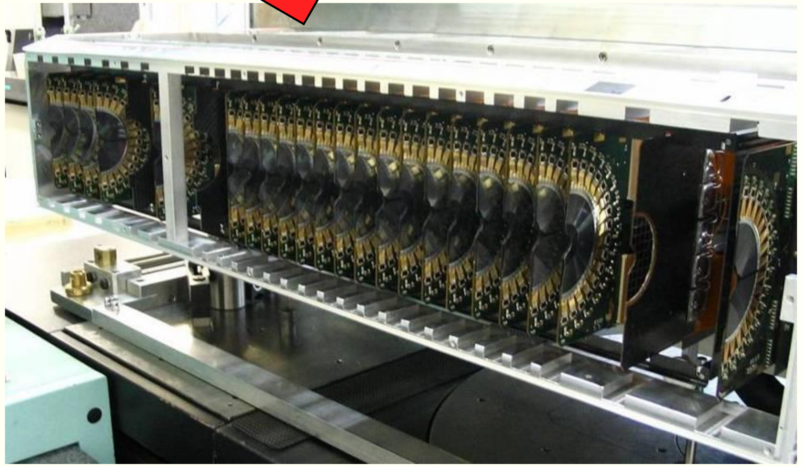
$\quad data(i) = data(i)$

LHCb Tracking & Phase-I Upgrade

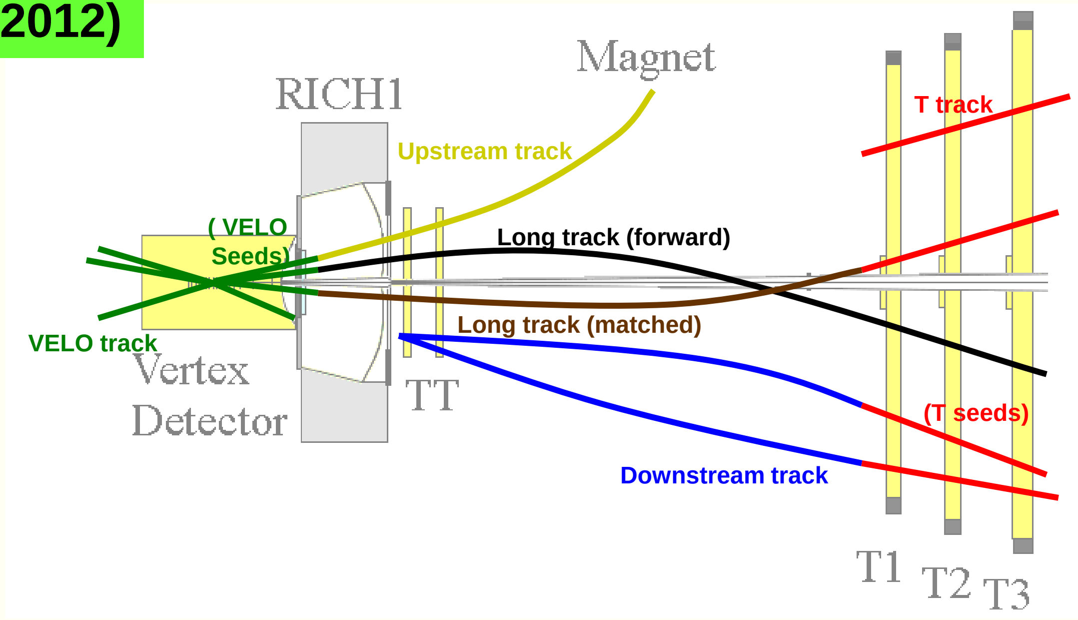


LHCb VP (2010-2012)





LHCb VELO (2005-2012)



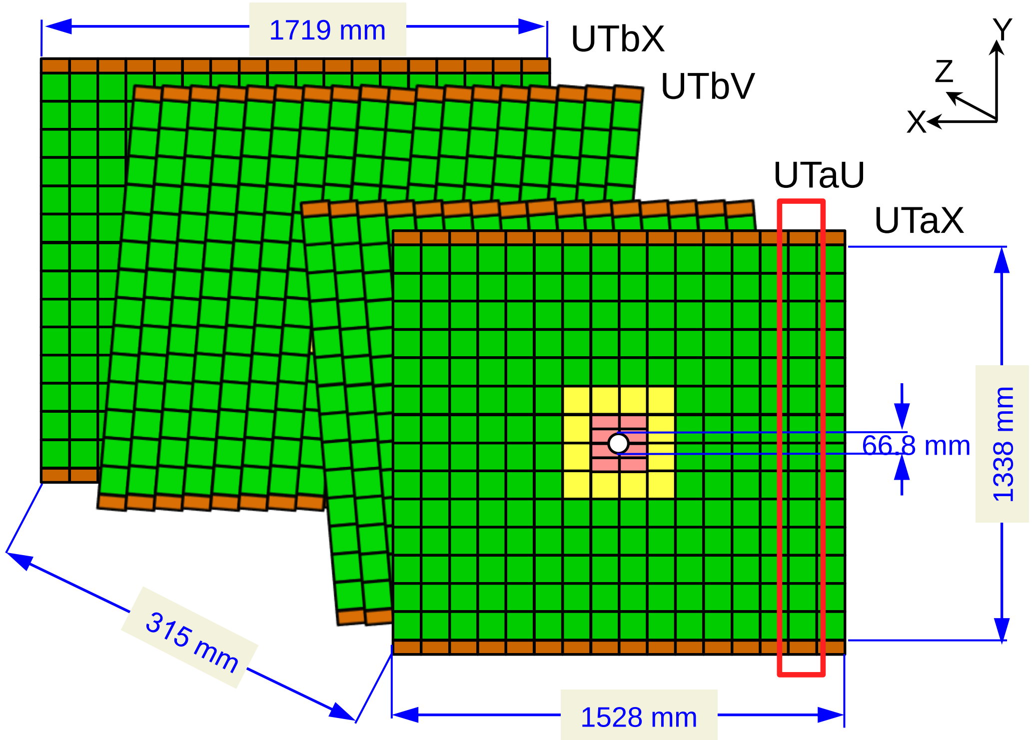
LHCb UT (2010-)

From < 1 MHz hardware trigger to
40 MHz total-software-based trigger

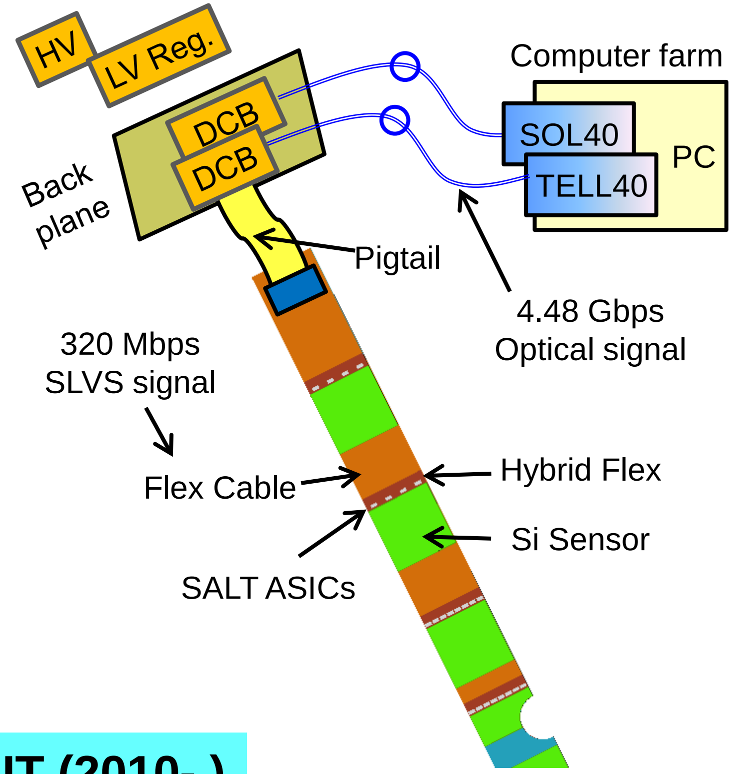
LHCb UT Design

Sensor	A	B	C	D
Pitch (μm)	187.5	93.5	93.5	93.5
Length (mm)	~100	~100	~50	~50
Strips/sensor	512	1024	1024	1024
SALTs/sensor	4	8	8	8

- Much improved coverage & segmentation
- **Read out at 40 MHz** by **custom-designed SALT ASICs** in the sensor proximity
- Digital events are packed in SALT, and sent out at the end of detector via optical fibers
- Sensor is more radiation resilience, Φ_{max} ~5×10^{14} $n_{eq}cm^{-2}$

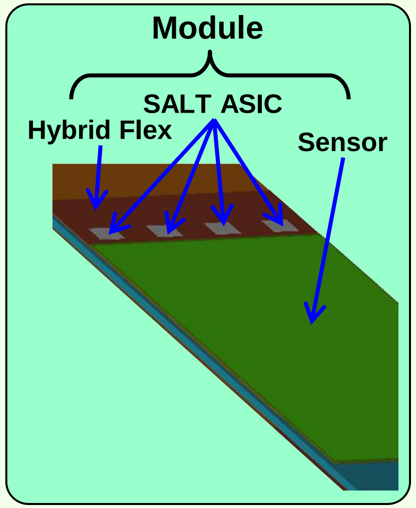


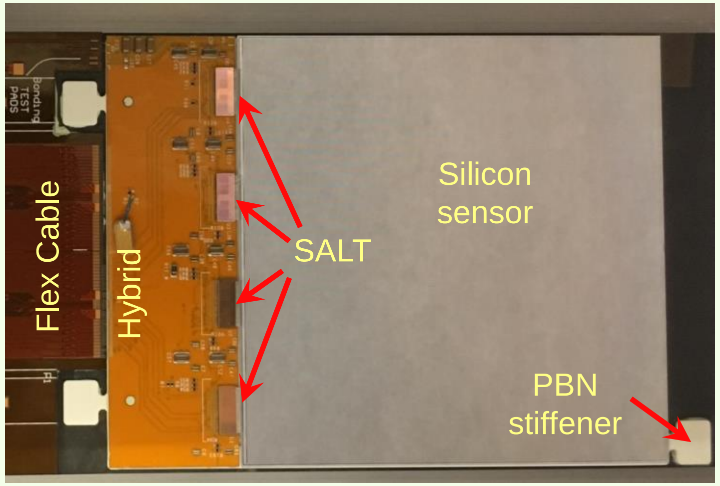
Central circular cut-out & overlapping sensors



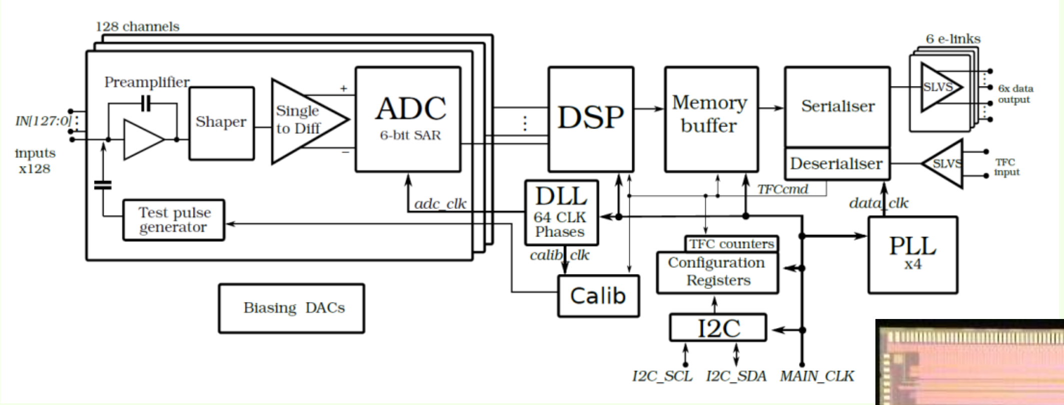
LHCb UT (2010-)

UT Module and Stave

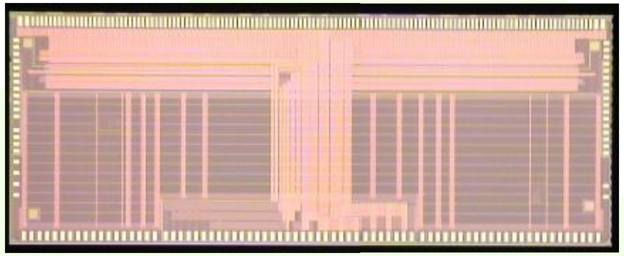


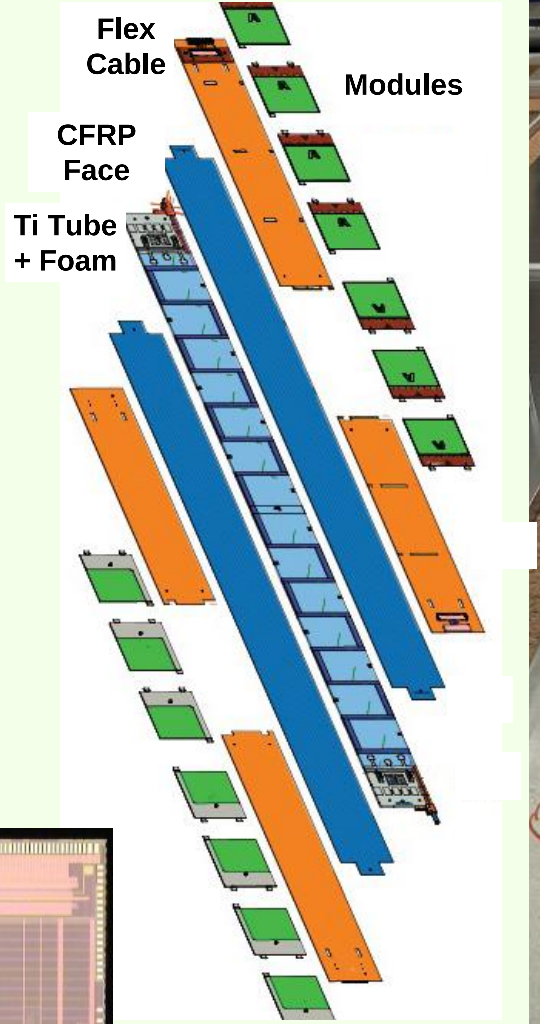


UT Module



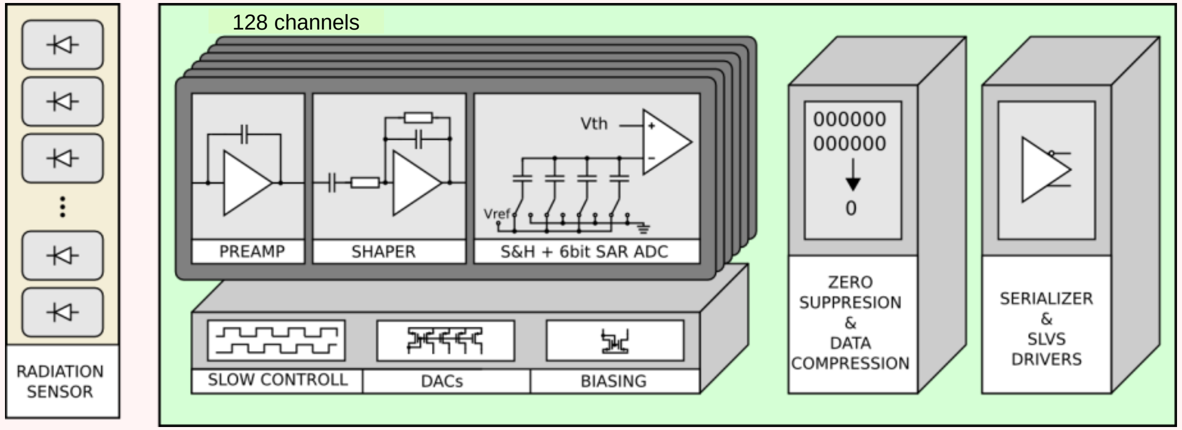
SALT ASIC



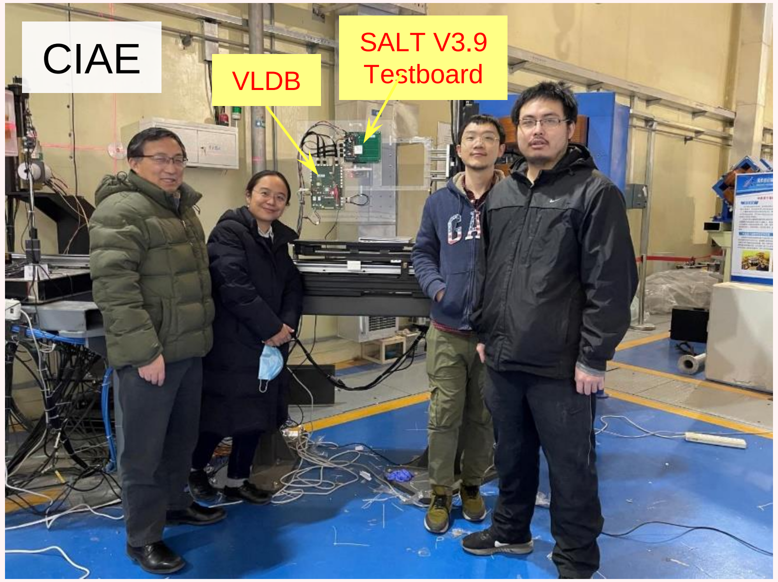


UT Stave

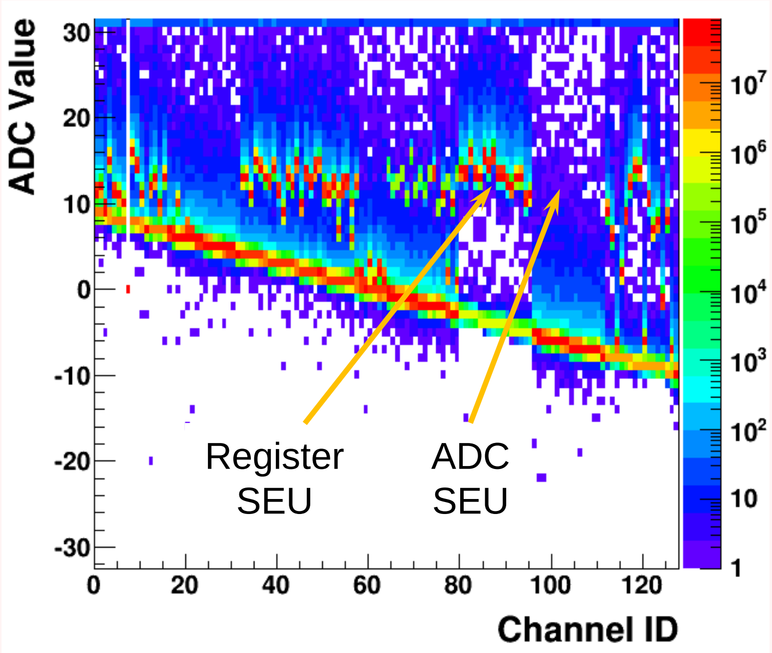
UT Front-End Readout ASIC - SALT



- CMOS 130 nm technology (IBM, TSMC)
- 40 MHz readout, digital data packet in ASIC
- 128 channels, per channel preamplifier & 6-bit ADC
- Sensor capacitance 2-12 pF, AC coupled
- Dynamic range ~ 30 ke, both input signal polarities
- Noise: ENC ~ 1000 e @ 10 pF + 50 e / pF
- T_{peak} < 25 ns, short tail ~5%@25ns+T_{peak}.
- Power consumption < 6 mW / channel.

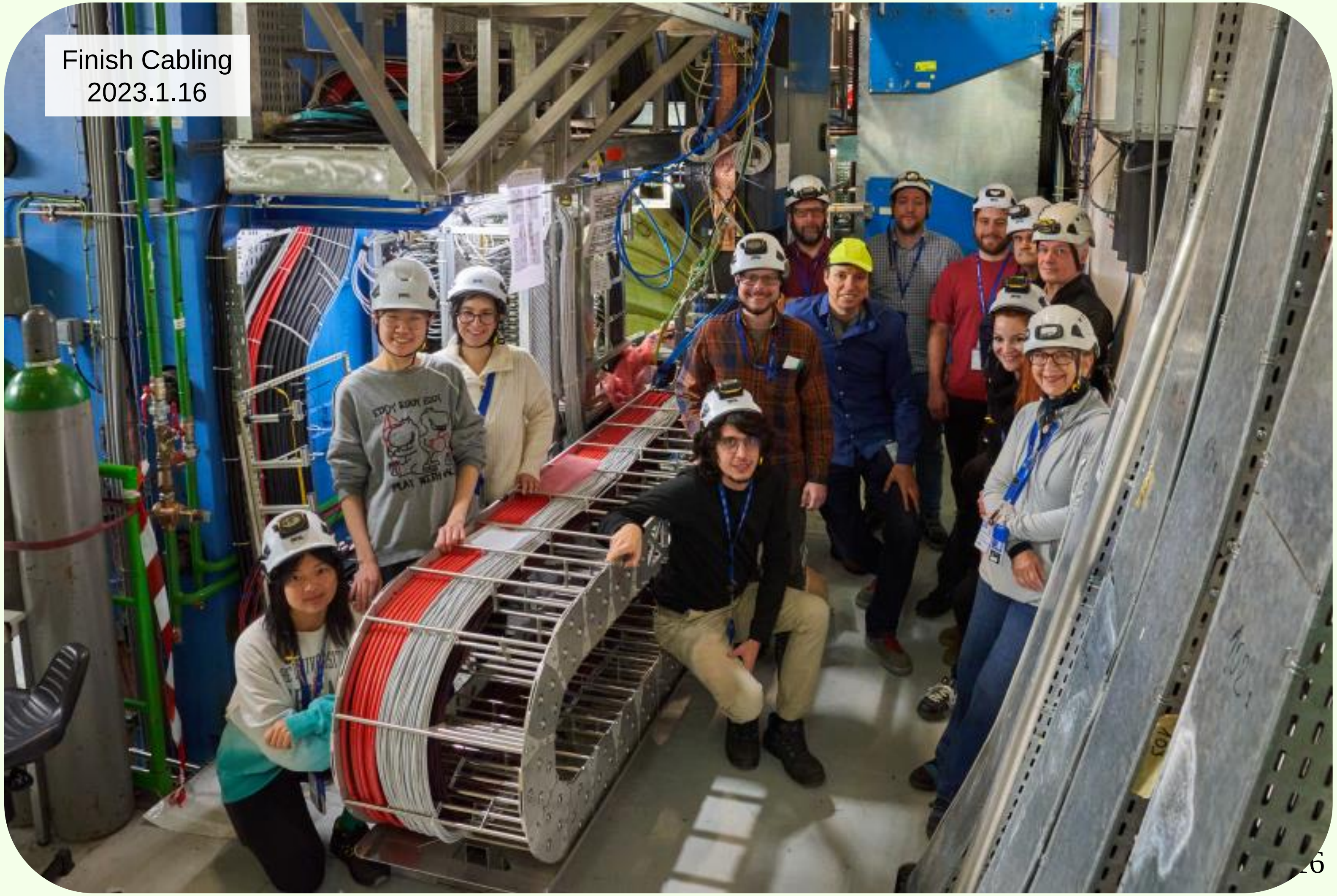


- Custom-designed SALT ASIC
- Validation of SALT functionalities by IHEP & Syracuse groups
- **Radiation hardness is very crucial,** a few studies at MGH, PSI, CIAE, and CSNS, led by IHEP group
- Few iterations for radiation hardened reinforcement, Mixed use in the final system due to tight schedule



UT Installation

- The Chinese team played key role in the UT installation.
- Maintain sufficient human resource at CERN during the difficult time (IHEP, THU, HNU, CCNU, LZU, SCNU, UCAS)



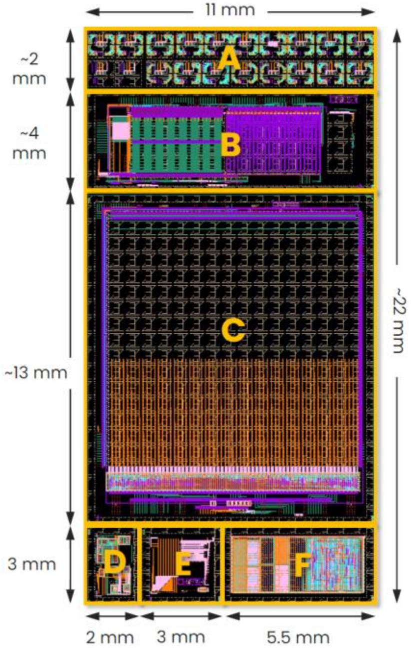
LHCb UP Detector

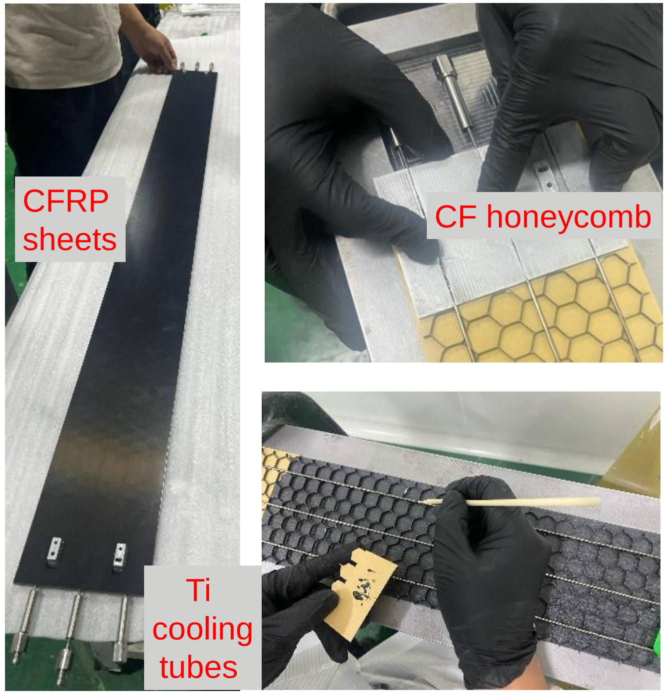
- A HV-CMOS pixel detector, total active area ~7 m^2, to be installed during LS4
- 4 chip candidates. **Pursue domestic production**

> - Spatial resolution ~ 10 μm
> - Time resolution 3-5 ns
> - Power < 200 mW/cm^2
> - Rad-hard: 3×10^{15} n_{eq}/cm^2

LHCb UP (2020-)

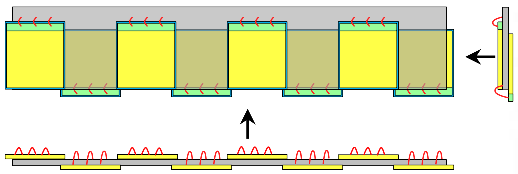
CHiR

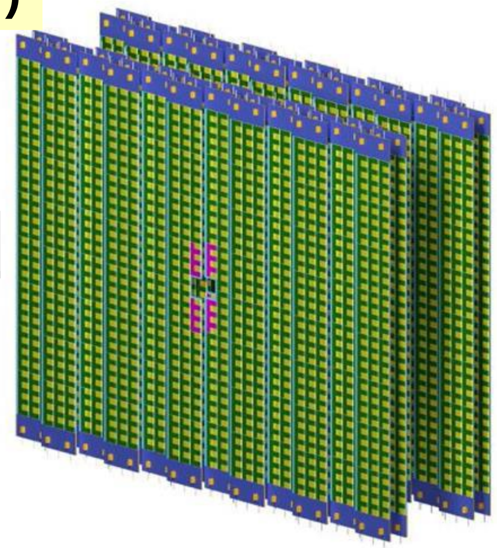




Prototype bare stave

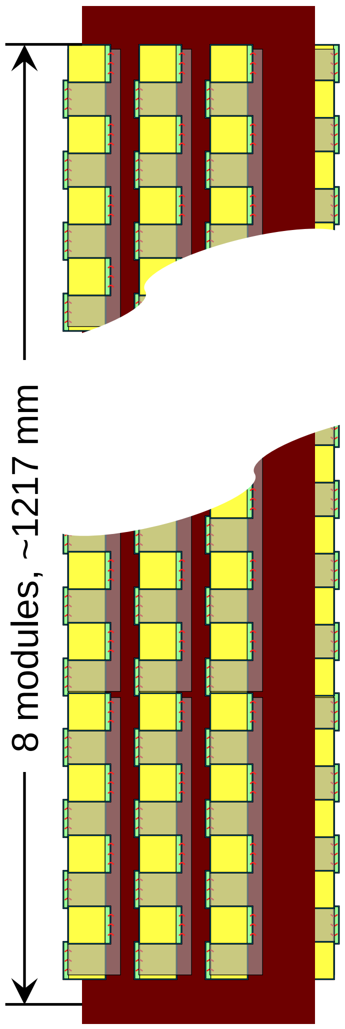
Module

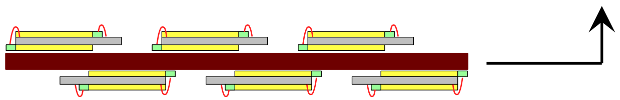




Prototype module

Stave





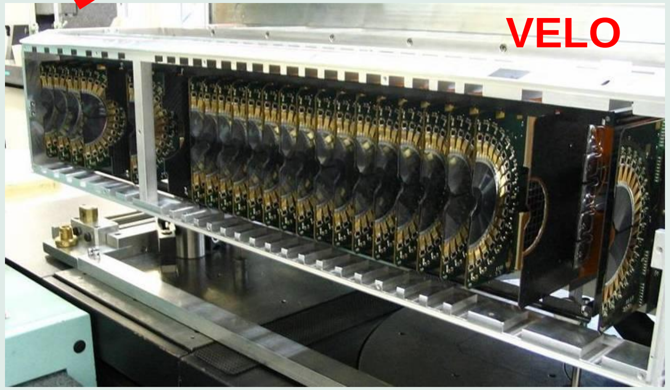
参考：袁煦昊、周扬、张慧的报告

The LHCb Operation Plan

2010–2018	2022–2033	2035–2041
$\mathcal{L}_{max}$ ~ 4×10^{32} cm^{-2}s^{-1}	$\mathcal{L}_{max}$~2×10^{33} cm^{-2}s^{-1}	$\mathcal{L}_{max}$~1.5×10^{34} cm^{-2}s^{-1}
$\mathcal{L}_{int}$ ~ 9 fb^{-1}	$\mathcal{L}_{int}$ ~ 50 fb^{-1}	$\mathcal{L}_{int}$ ~ 300 fb^{-1}
~1 Vis Interact./Xing	~5 Vis. Interact./Xing	~40 Vis. Interact./Xing

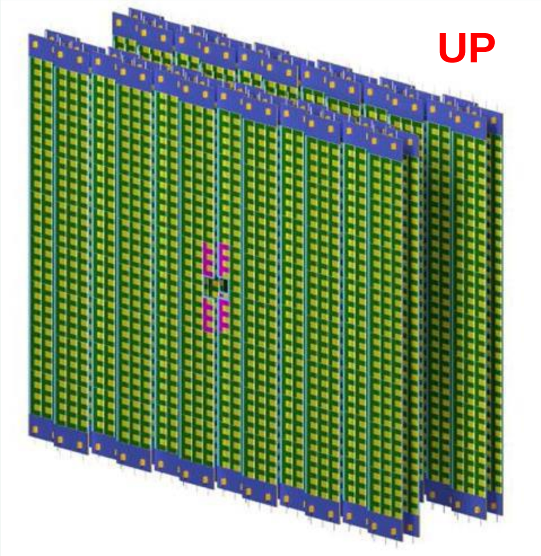
2010 2011 2012 2013 2014 2015 2016 2017 2018 2019 2020 2021 2022 2023 2024 2025 2026 2027 2028 2029 2030 2031 2032 2033 2034 2035 2036 2037 2038 2039 2040 2041

Run 1 | LS 1 | Run 2 | LS 2 | Run 3 | LS3 | Run4 | LS4 | Run 5



VeloPix

UT



Current R&D's in China for LHC Experiments

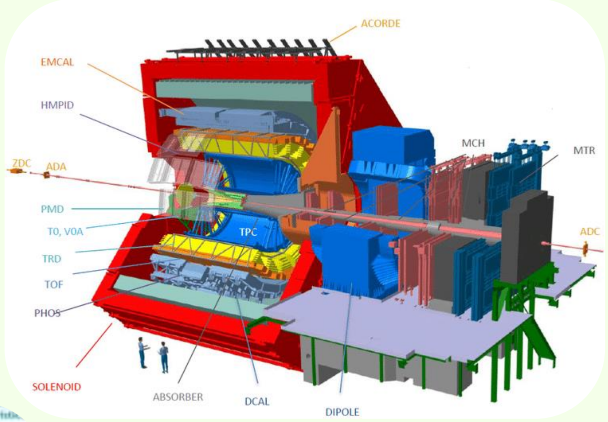
2010 2011 2012 2013 2014 2015 2016 2017 2018 2019 2020 2021 2022 2023 2024 2025 2026 2027 2028 2029 2030 2031 2032 2033 2034 2035 2036 2037 2038 2039 2040 2041

Run 1 | LS 1 | Run 2 | LS 2 | Run 3 | LS3 | Run4 | LS4 | Run 5

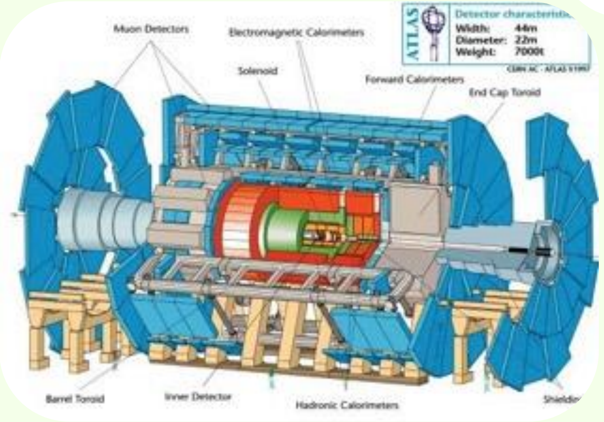
ATLAS	ITK, **HGTD**
CMS	HGCAL, MTD-ETL
ALICE	ITS3, FoCal

LHCb	**UP**
ALICE	VD, ML, TOF

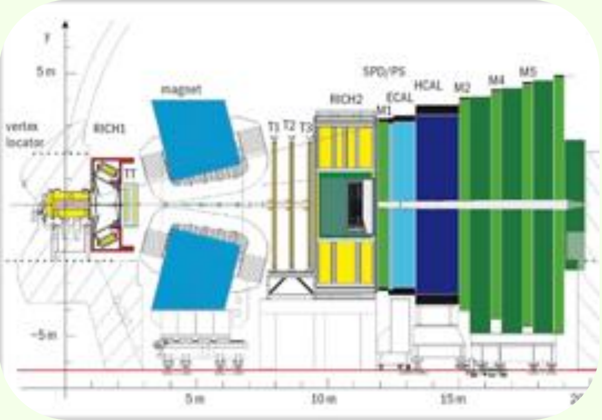
ALICE



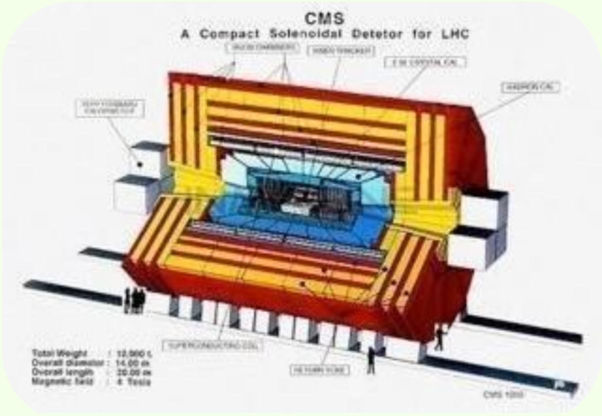
ATLAS



LHCb



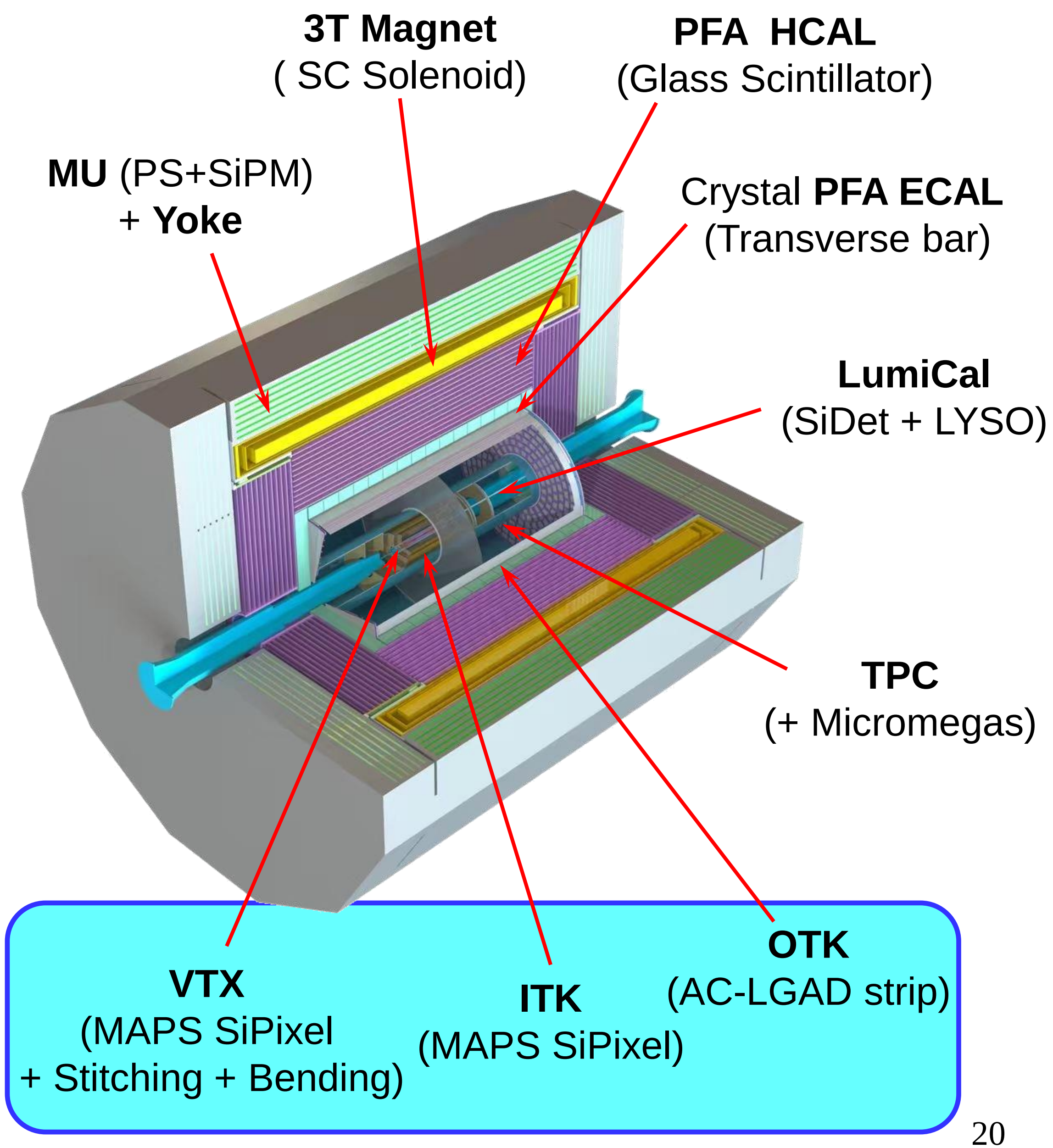
CMS



A High Energy e^+e^- Collider of Our Own

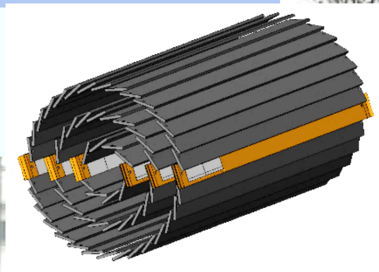
- The CEPC was proposed in 2012 as an e^+e^- Higgs / Z factory.
- To produce Higgs / W / Z / top for high precision Higgs, EW measurements, studies of flavor physics & QCD, and probes of physics BSM.
- It is possible to upgrade to a *pp* collider (SppC) of $\sqrt{s}$ ~ 100 TeV in the future.

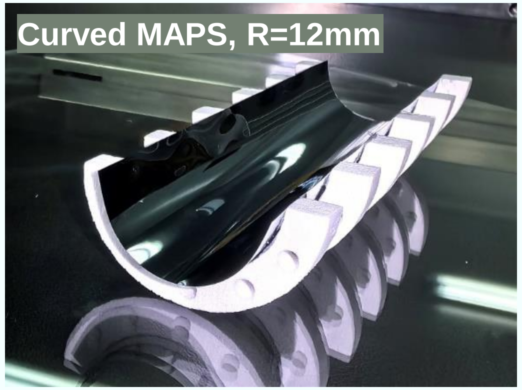
Operation mode		ZH	Z	W^+W^-	$t\bar{t}$
$\sqrt{s}$ [GeV]		~240	~91	~160	~360
Run Time [years]		10	2	1	5
30 MW	L / IP [$\times 10^{34}$ cm^{-2}s^{-1}]	**5.0**	**115**	**16**	**0.5**
	$\int L\,dt$ [ab^{-1}, 2 IPs]	13	60	4.2	0.65
	Event yields [2 IPs]	2.6×10^6	2.5×10^{12}	1.3×10^8	4×10^5
50 MW	L / IP [$\times 10^{34}$ cm^{-2}s^{-1}]	**8.3**	**192**	**26.7**	**0.8**
	$\int L\,dt$ [ab^{-1}, 2 IPs]	21.6	100	6.9	1
	Event yields [2 IPs]	4.3×10^6	4.1×10^{12}	2.1×10^8	6×10^5



CEPC Vertex Detector

Alternative design: ladder-based

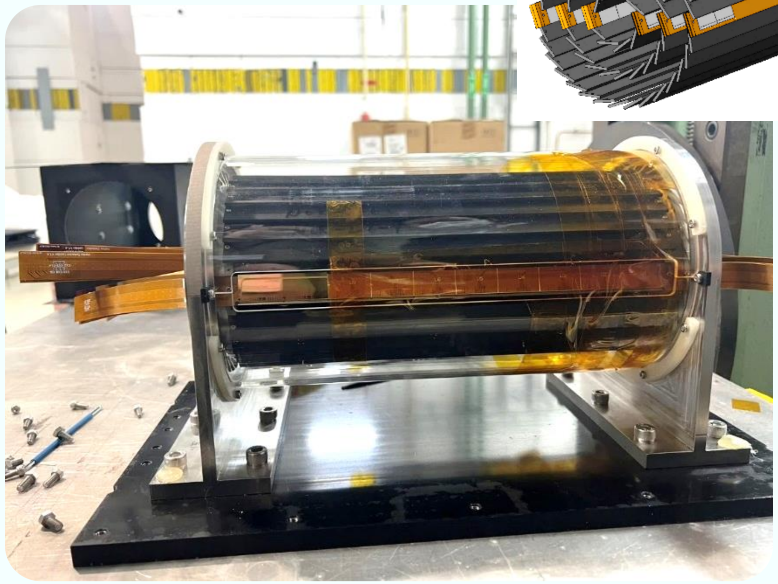




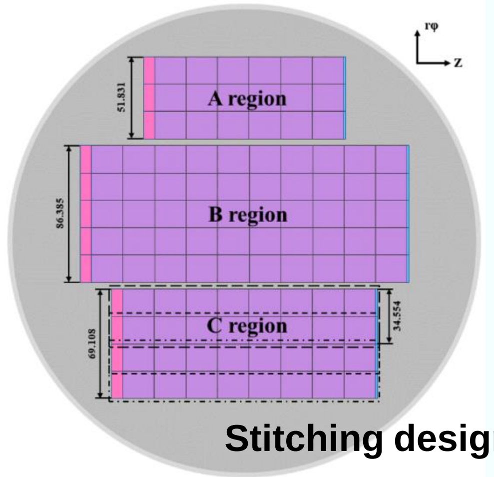
Goal: σ(IP) ~ 5 μm for high P

Key specifications:

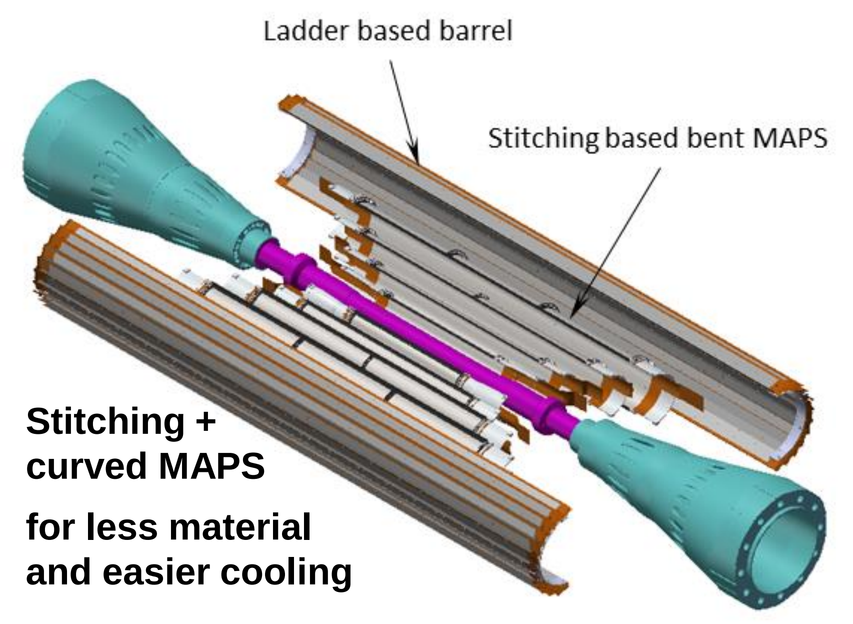
- Single point resolution ~ 5 μm
- Low material (0.15% X_0 / layer)
- Low power (< 50 mW/cm^2)



A TaichuPix-based prototype detector

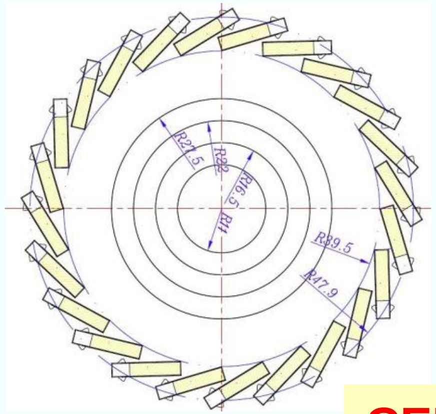


Stitching design



Stitching + curved MAPS

for less material and easier cooling



Outer: double-layer ladder
Material ~ 0.3% X_0 / layer

Inner layer: single bent MAPS
Material ~ 0.06% X_0 / layer

CEPC VTX (2020-)

CEPC Inner Tracker ITK

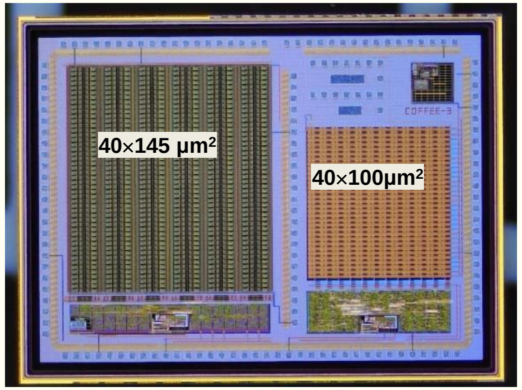
- HV-CMOS pixel detector for CEPC inner tracker ITK, area ~15-20 m^2.
- Explore 55 nm and other processes
- Same chip team as LHCb UP

CEPC ITK (2022-)

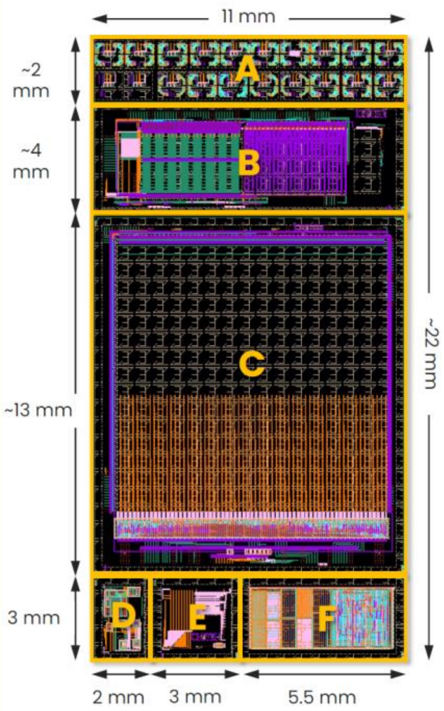
Goal
- Cost effective
- Spatial resol. < 10 μm
- Timing 3-5 ns
- Power < 200 mW/cm^2

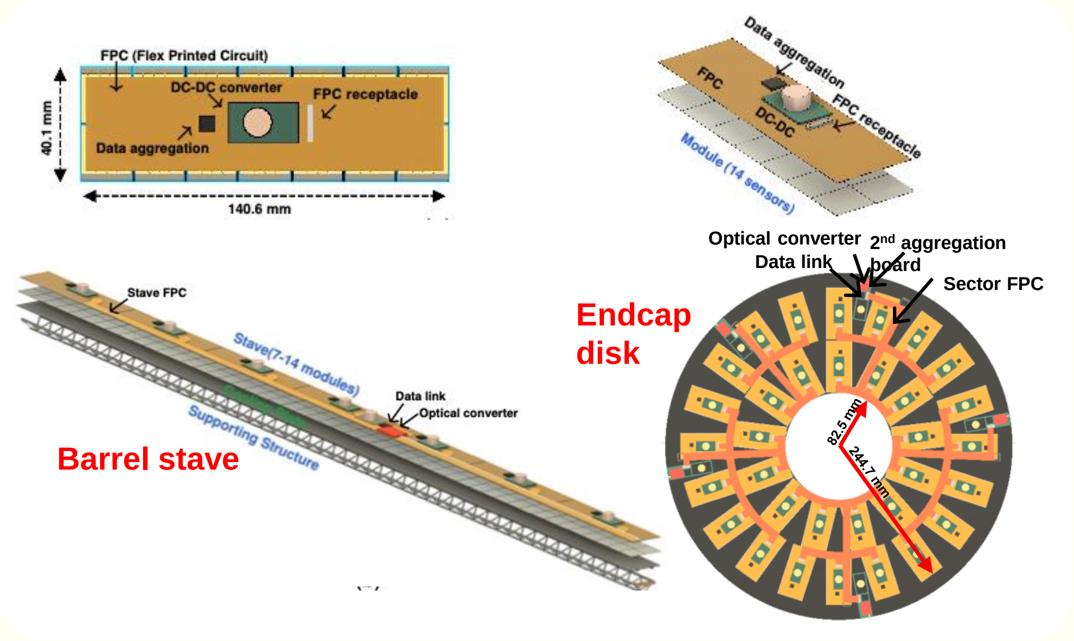
Process node: 55 nm
Chip size: 2 cm × 2 cm
Sensor thickness: 150 μm
Pixel array: 512 × 128
Pixel size: 34×150 μm^2
Spatial resolution: 8 / 40 μm
Time resolution: 3-5 ns
Power consumption: 200 mW/cm^2

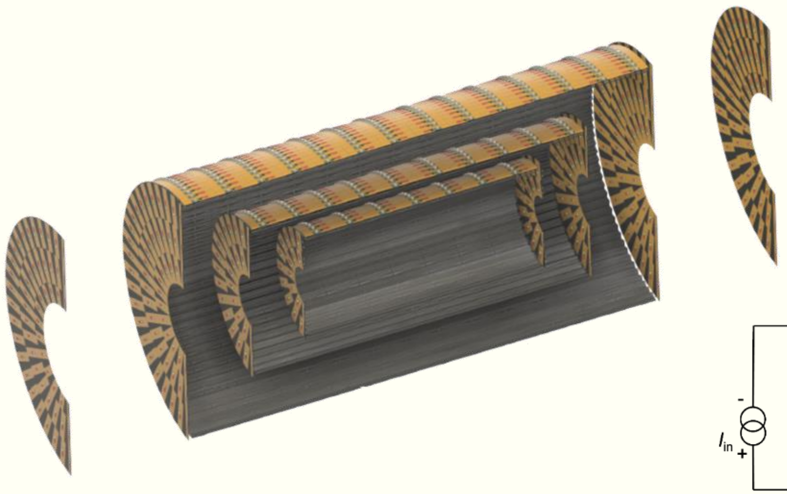
COFFEE



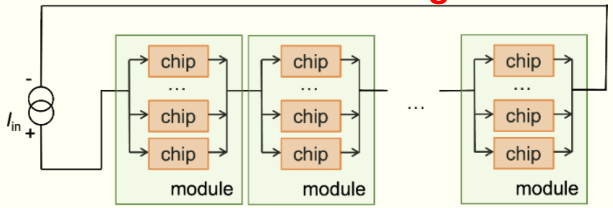
CHiR







Serial Powering



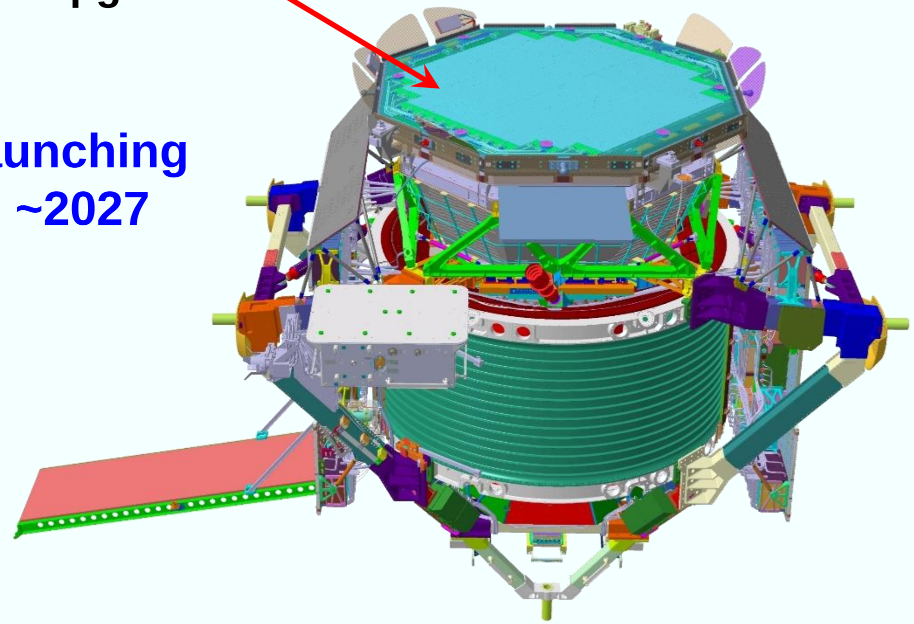
参考：李一鸣、周扬、张慧的报告

Space Station Based Experiments

L0 Tracker Upgrade

AMS-02

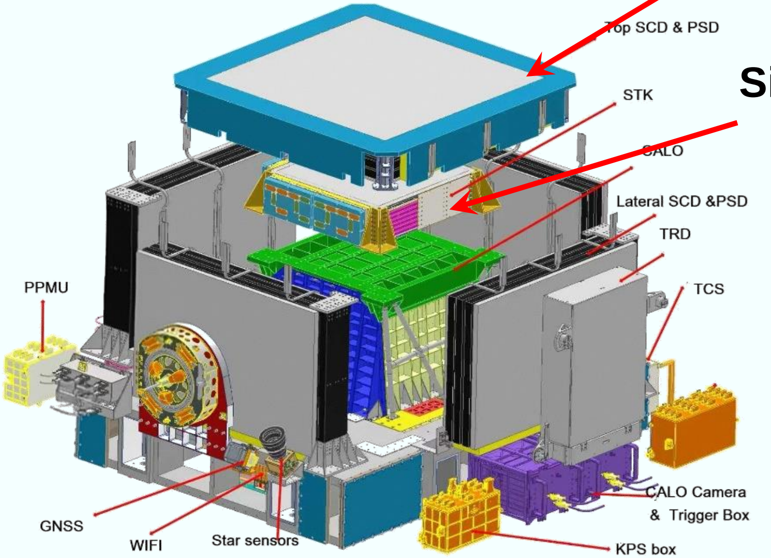
Upgrade launching expected ~2027

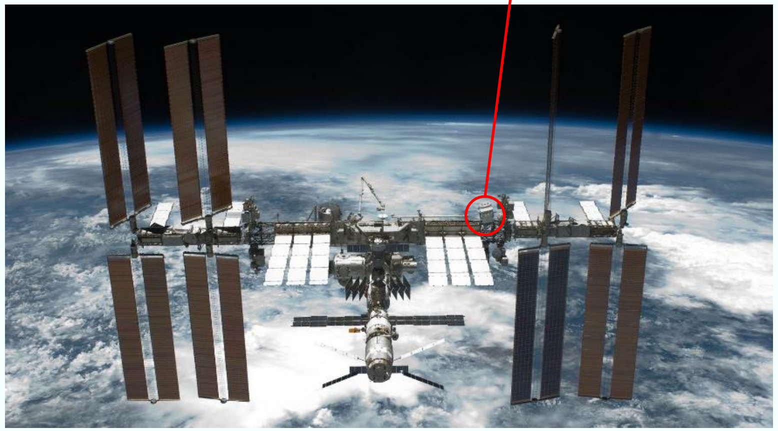


HERD

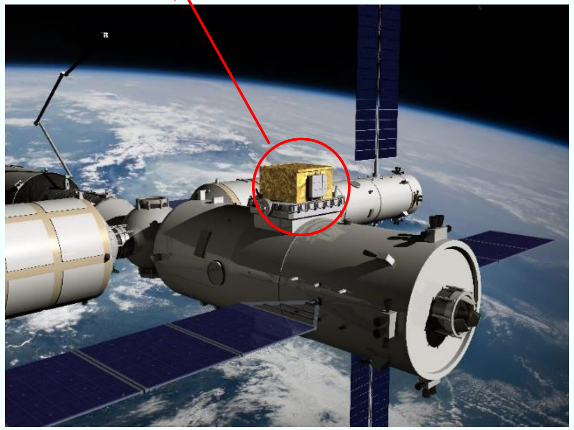
Silicon Charge Detector (SCD)

Silicon Tracker (STK)



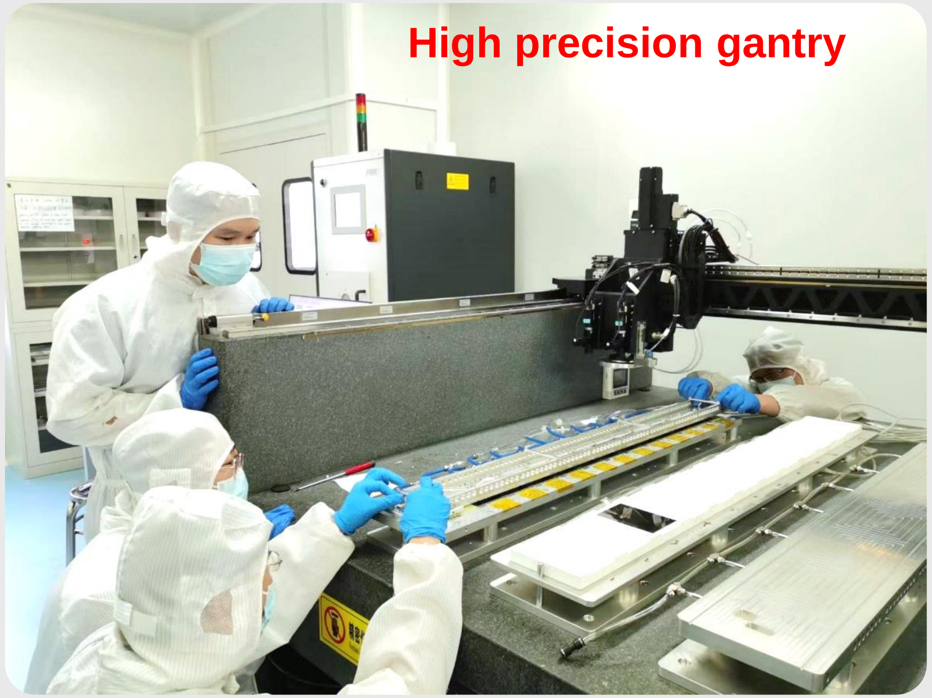


Detector launching is expected ~2028



AMS L0 Tracker

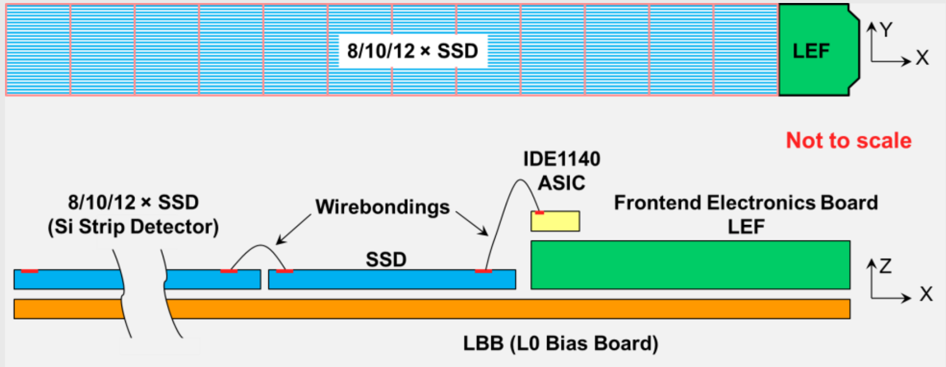
AMS L0 (2021-2027)

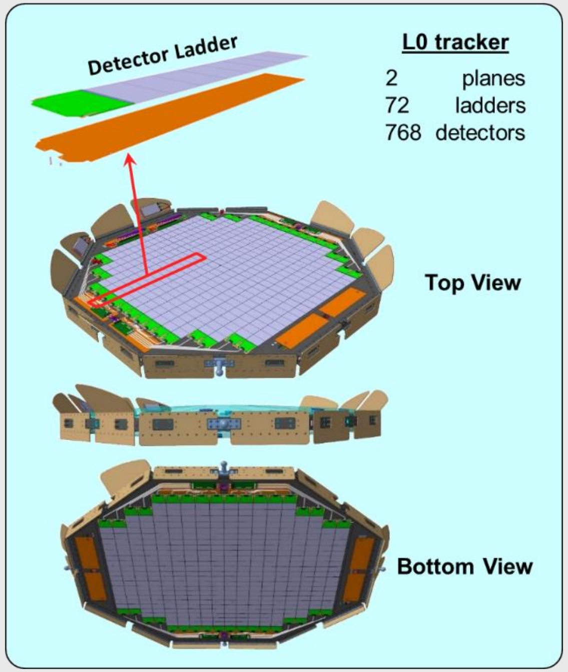


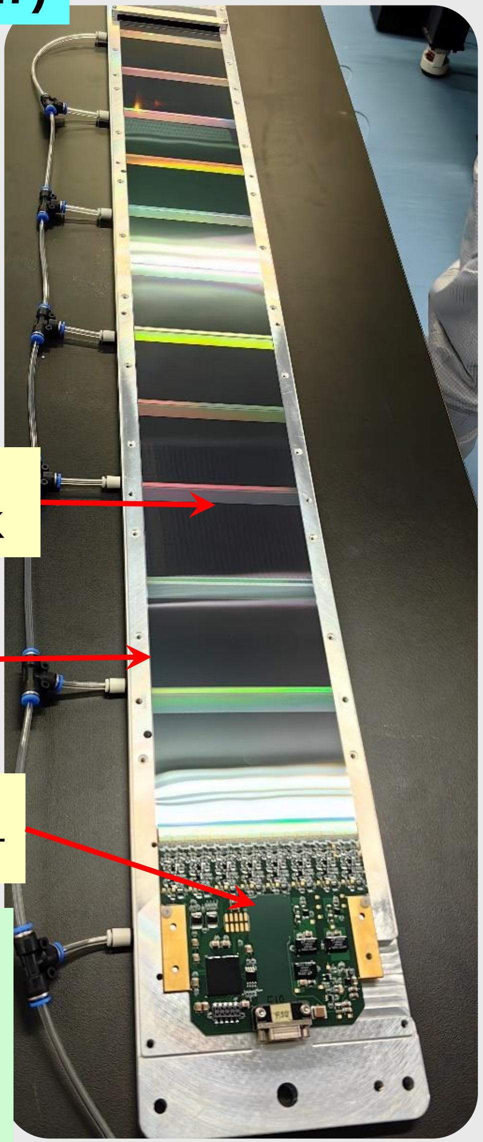
Challenges

- Coupling and noise level due to long strips impose big challenges.
- Precise placement of SSDs on a ladder. Aim for a < 5 μm precision.
- Highly reliable wire-bonding (>12K wires per ladder).

The longest SSD single unit ~ 1 m







SSD designed by IHEP+Perugia+HPK

Detector ladder produced by IHEP+SDIAT

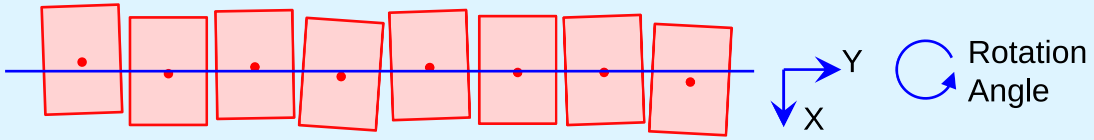
LEF produced by IPAS+NCSIST+MIT

HPK SSD
readout pitch 109 μm
readout / bias = 1:4
thickness 320 μm
AC + bias resistor

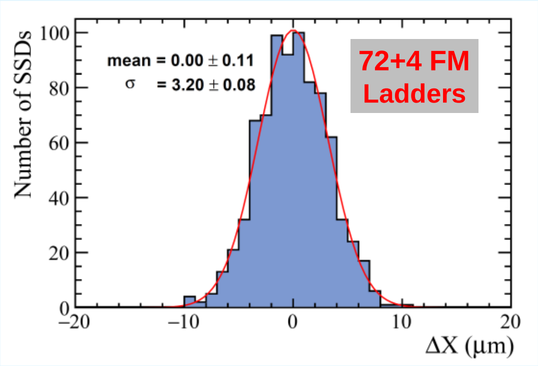
IDE1140 readout chip

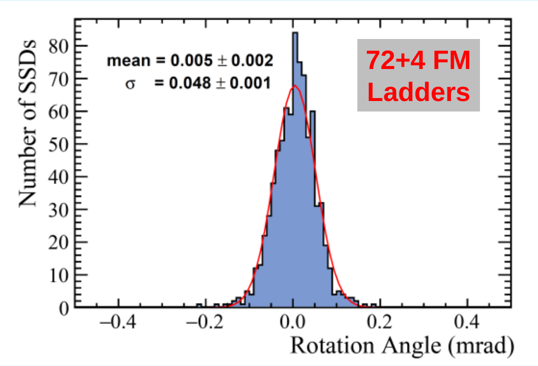
参考：徐子骏的报告

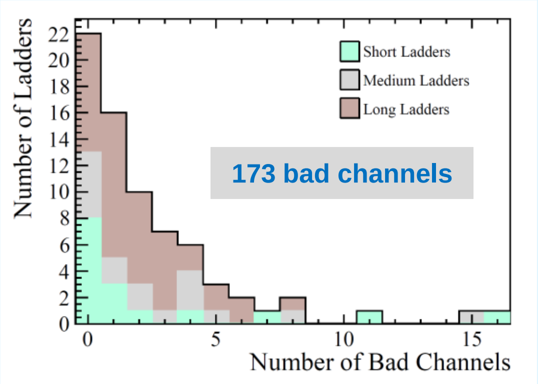
AMS L0 Tracker

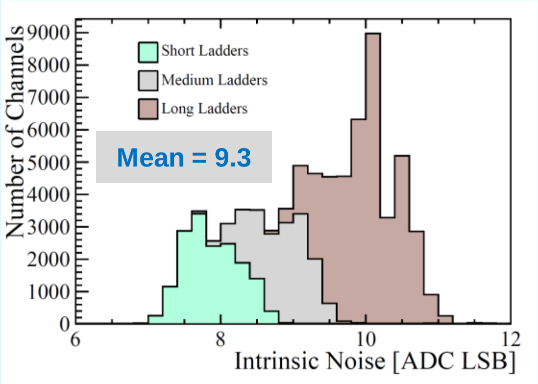


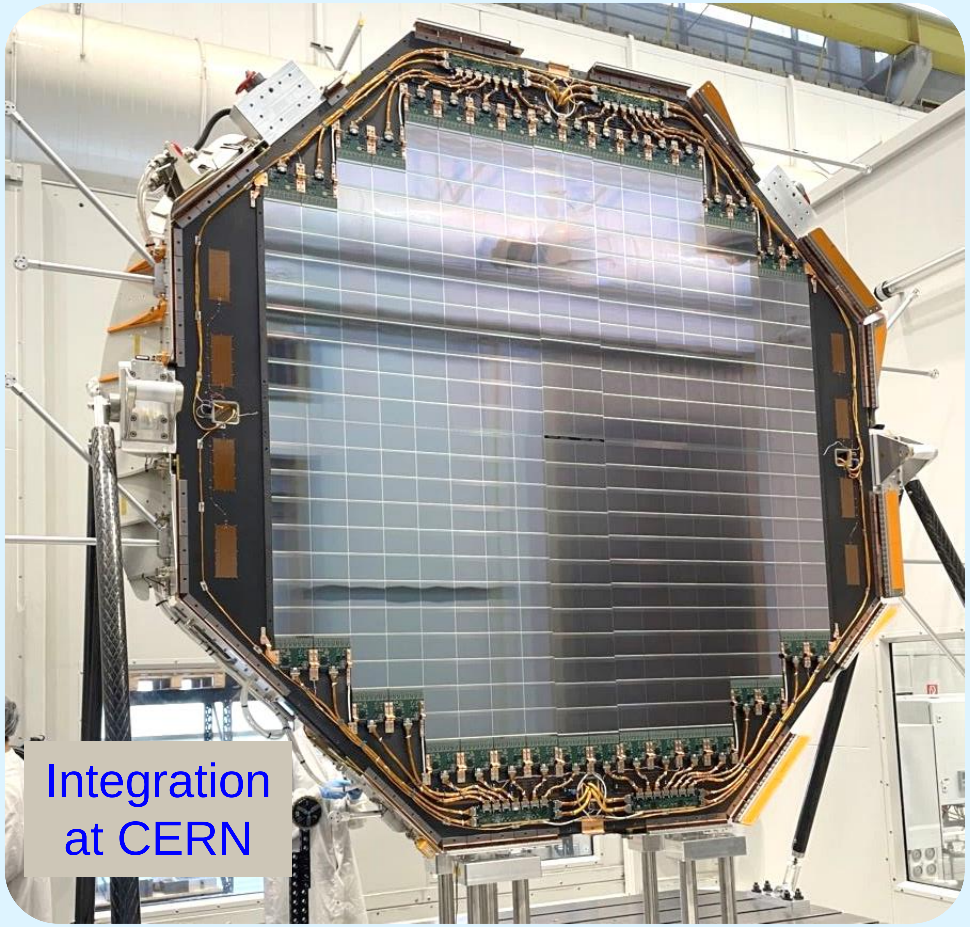
The **First** large silicon detector with major contributions from the Chinese teams





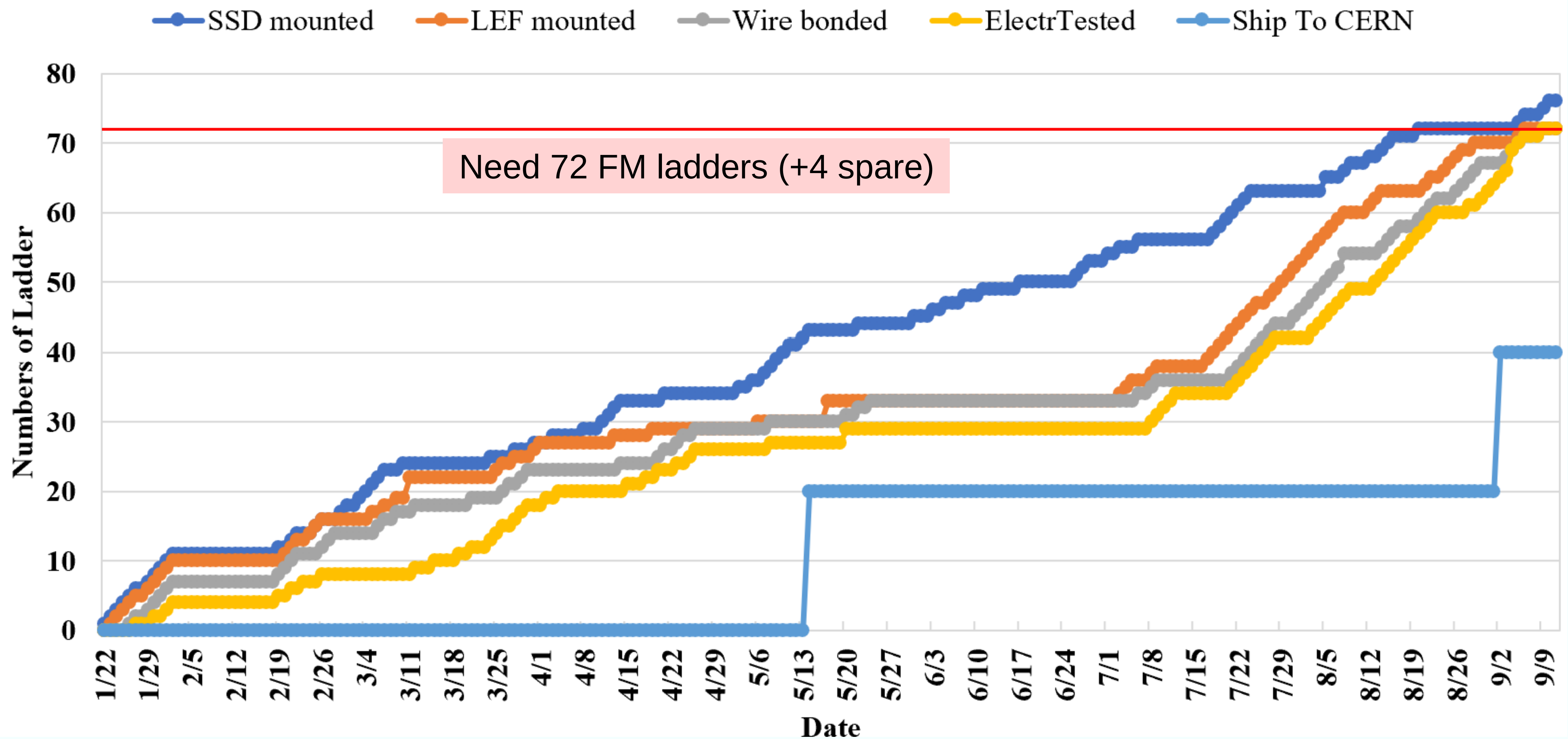






- Dark current of all ladders are < 2 μA @ 50, 80 V
- Optimized for high-Z particles; S/N for MIP ~ 6-7
- Bad channel rate **~ 0.23%**
- Non-perfect production contributes to measurement $\sigma_x = 3.4\ \mu m$, before applying correction

FM Ladder Production



Year 2024

The IHEP+SDIAT L0 Team

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Mingyi Dong	董明义	Professor
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Congcong Wang	王聪聪	Engineer (R)

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Pingcheng Liu	刘平成	Research scientist
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Haotian Yang	杨昊天
Qinze Li	李沁泽
Ji Peng	彭吉
Shuqi Sheng	盛书琪
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Tianyu Shi	史天宇
Zhijie Wang	王智颉
Yaohui Yang	杨耀晖
Yutong Li	李雨彤
Ming Dai	代铭
Yang Liu	刘洋
Danyan Huang	黄丹艳
Jiaru Wang	王佳如
Jingbo Liu	刘京博

The IHEP+SDIAT team

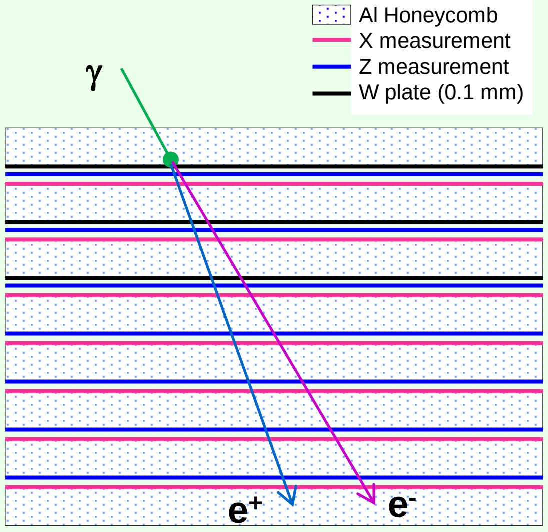
26 staff members
6 postdocs
18 graduate students
14 college students

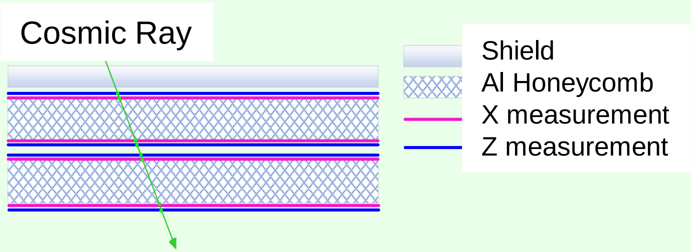
The professional title represents the date the member joined the team

HERD Silicon Detectors: SCD and STK

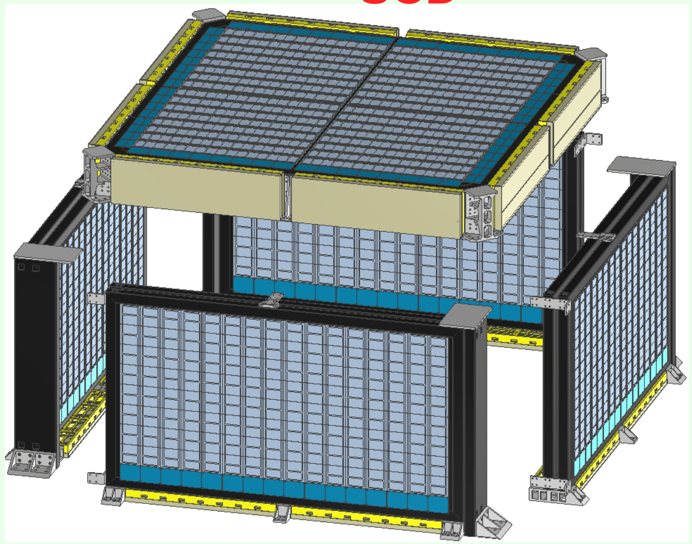
HERD SCD, STK (2025-)

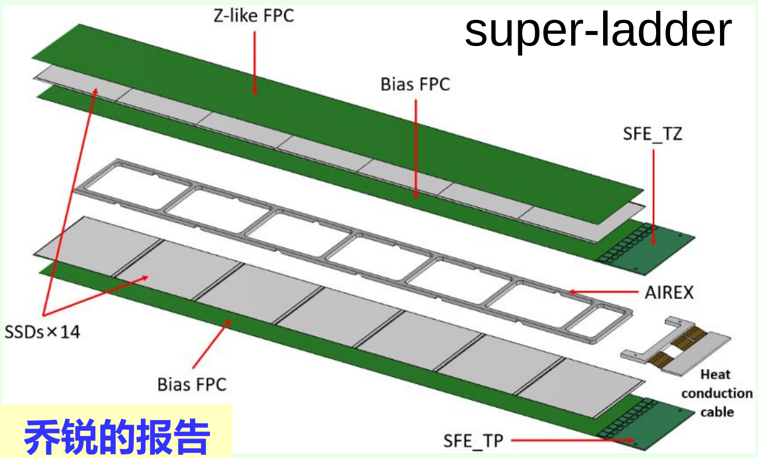
- HERD (High Energy cosmic-Radiation Detection) is to be installed on the Space Station by ~2028. The detector system has SCD, STK, +3 others
- SCD: **5-side, 8-layer** charge measurement Z=1~28, total area 38.8 m^2
- STK: **14-layer** detecting trajectories of $\gamma \rightarrow e^+e^-$ conversion in 3 W plates, angular resolution ≤ 0.1° @ 10 GeV, total active area 8.3 m^2
- HPK SSDs: 150 μm pitch, 320 μm thick, DC with bias resistor
- Front end readout chips: IDE1140, VATA450.3





SCD





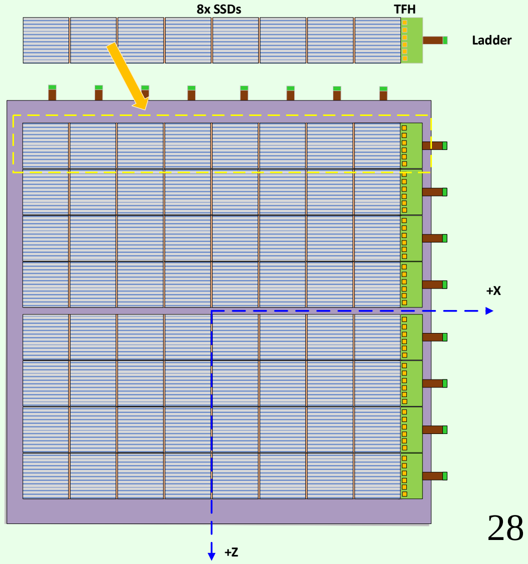
参考：乔锐的报告

Participating institutes:

IHEP, PMO, Perugia

STK

ladder and layer



Closing Remarks

Type	Detectors	Time	Comment
SSD	LHCb VELO	2005 – 2012	Special shaped strip detector for better reconstruction, trajectory measurement
	LHCb UT	2010 –	High granularity with readout ASIC in sensor proximity, trajectory measurement
	AMS L0 Tracker	2021 – 2027	Charge measurement Z=1-28 and trajectory measurement
	HERD SCD, STK	2025 –	SCD: charge measurement Z=1-28; STK: photon conversion + trajectory measurement
	CEPC OTK	2024 –	High precision timing and 1-D spatial position measurement
Hybrid SPD	BTeV PVD	1997 – 2005	Low noise, radiation-hard, long pixel
	LHCb VP	2010 – 2012	High through-put, radiation-hard
Monolithic SPD	CEPC VTX	2020 –	VTX: stitching+bent for low material and close to IP, trajectory measurement
	CEPC ITK	2022 –	Trajectory measurement, cost effective, radiation-resilient, high hit rate
	LHCb UP	2020 –	Trajectory measurement, cost effective, radiation-resilient, high hit rate

- In recent years, silicon detector technology has advanced rapidly in China
- Chinese research groups have become highly active in developing silicon detectors for major international experiments
- It is my great privilege to contribute to this exciting progress

Thank you for your attention!