



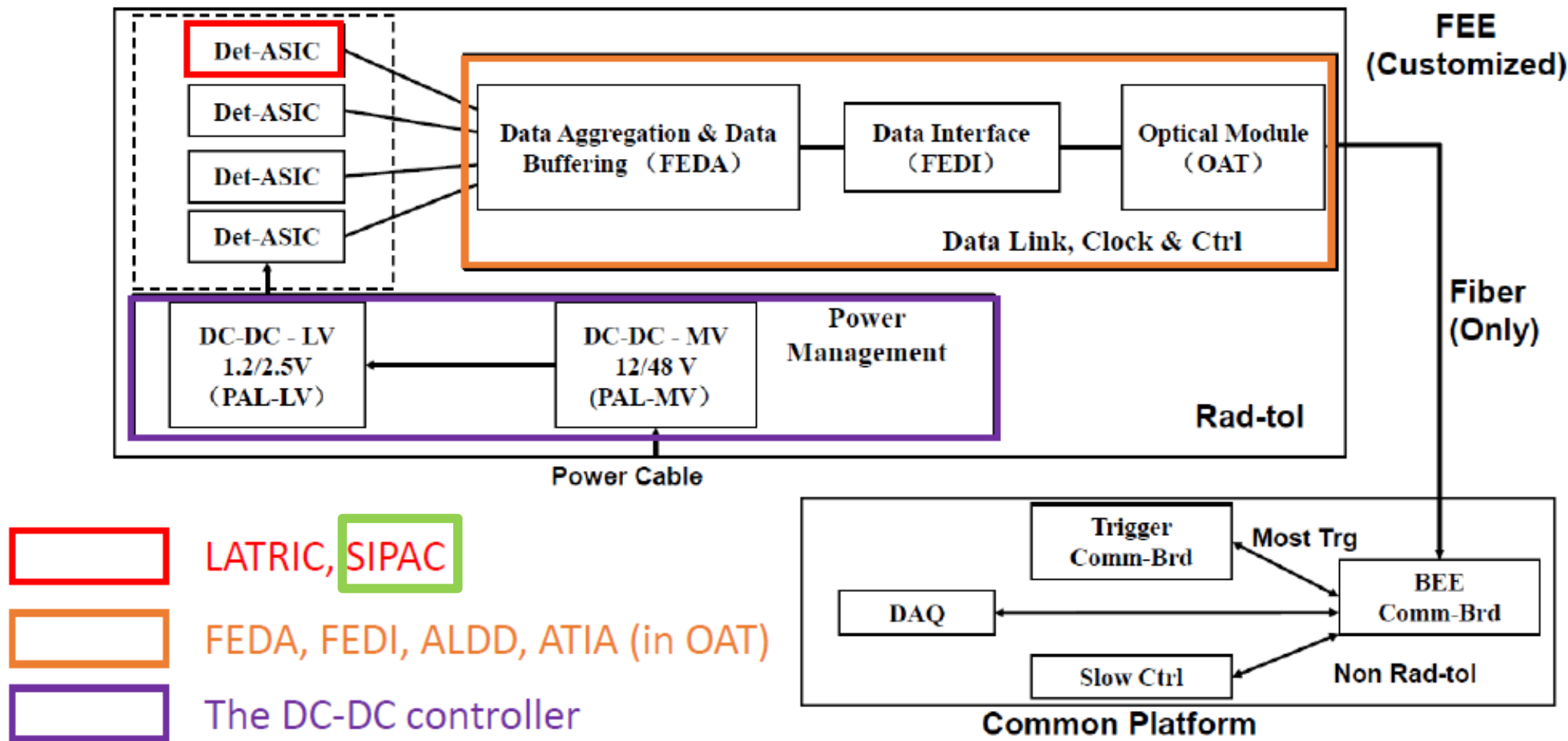
# 用于CEPC量能器SiPM读出的SIPAC芯片研究进展

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代表CEPC SIPAC芯片研发团队

# 目录

- 研究背景
- 原型芯片SIPAC0设计及改进
- 性能测试及总结

# 研究背景——CEPC基准探测器Ref.Det电子学



# 研究背景---CEPC量能器SiPM读出芯片需求

Table 7.3: Requirements of ECAL front-end electronics

Parameters	Requirements
Charge Range	0.128 pC~ 3.84 nC (0.1~3000 MIP)
Charge Resolution	10 % (1.0 MIP), 1 % (100 MIP)
Timing Resolution	200 ps (1 MIP), 100 ps (12 MIP)
Integral Non-linearity	< 1 %
Average Event Rate/channel	13 kHz
Max Event Rate/channel	230 kHz
Typical Signal Rising Edge	40 ns
Typical Signal Width	~ 1 $\mu$ s

Ref.TDR 电磁量能器电子学需求

SiPM characteristics that drive the requirements for the readout electronics design.

Item	Requirement
Charge dynamic range	0.8 pC~800 pC (0.1~100 MIPs)
Charge resolution	10% of 1.0 MIP
SiPM capacitance	$\leq 100$ pF
SiPM gain	$\geq 5 \times 10^5$
Average event rate/channel	2 kHz
Max event rate/channel	50 kHz
Typical signal	2~3 mV/p.e.

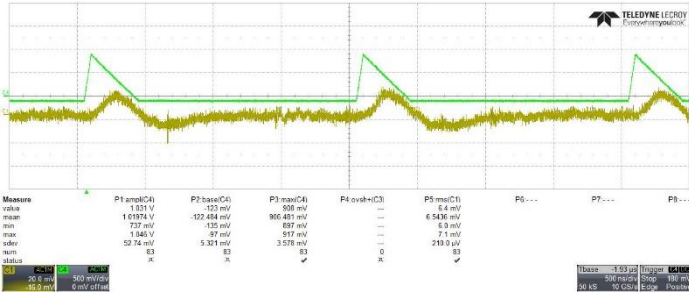
Ref.TDR 强子量能器电子学需求

## MUON requirement

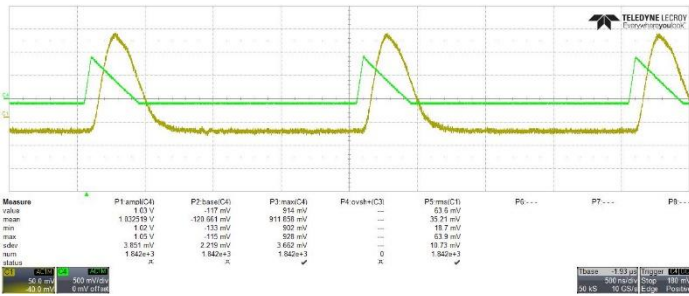
- Readout design for ECAL and HCAL covers the requirements of Muon detector  $N_{pe} < 100, \sigma_T < 0.5ns$
- Use the ASIC scheme from ECAL or HCAL, and customize the FEE based on ASIC.
- Revise according to the constraints from cooling and mechanical structure of the detector



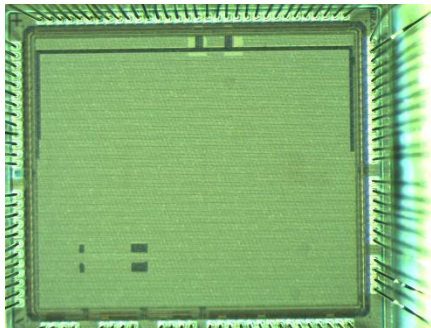
# SIPACO的测试



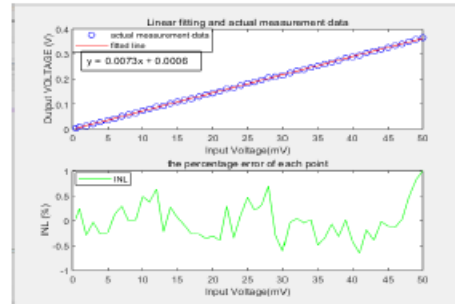
高增益支路模拟输出信号 (黄色,20mV小信号)



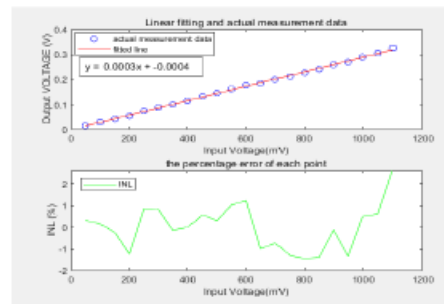
低增益支路模拟输出信号 (黄色,200mV大信号)



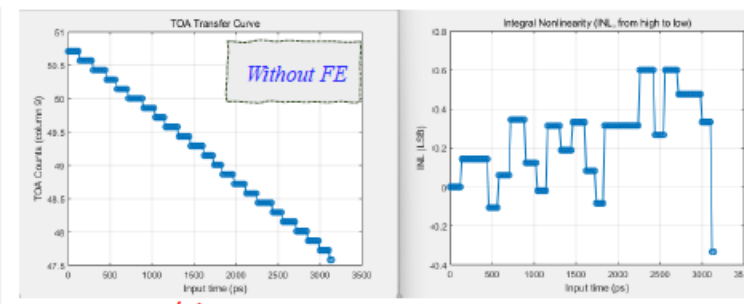
SIPACO layout 照片



1.28 pC - 128 pC  
High-gain path INL



128 pC - 2.81 nC  
Low-gain path INL



LSB=1/slope  $\approx$  142 ps  
TDC transfer curve

	Post-Simulation result	Test result
Input dynamic range	1.28 pC - 3.84 nC	1.28 pC - 2.81 nC
High gain path gain	8	7.3
Low gain path gain	0.5	0.3
SNR	5	4.3
TDC resolution	100 ps	142 ps
ADC resolution	ENOB 10bit	$\sim$ 8bit

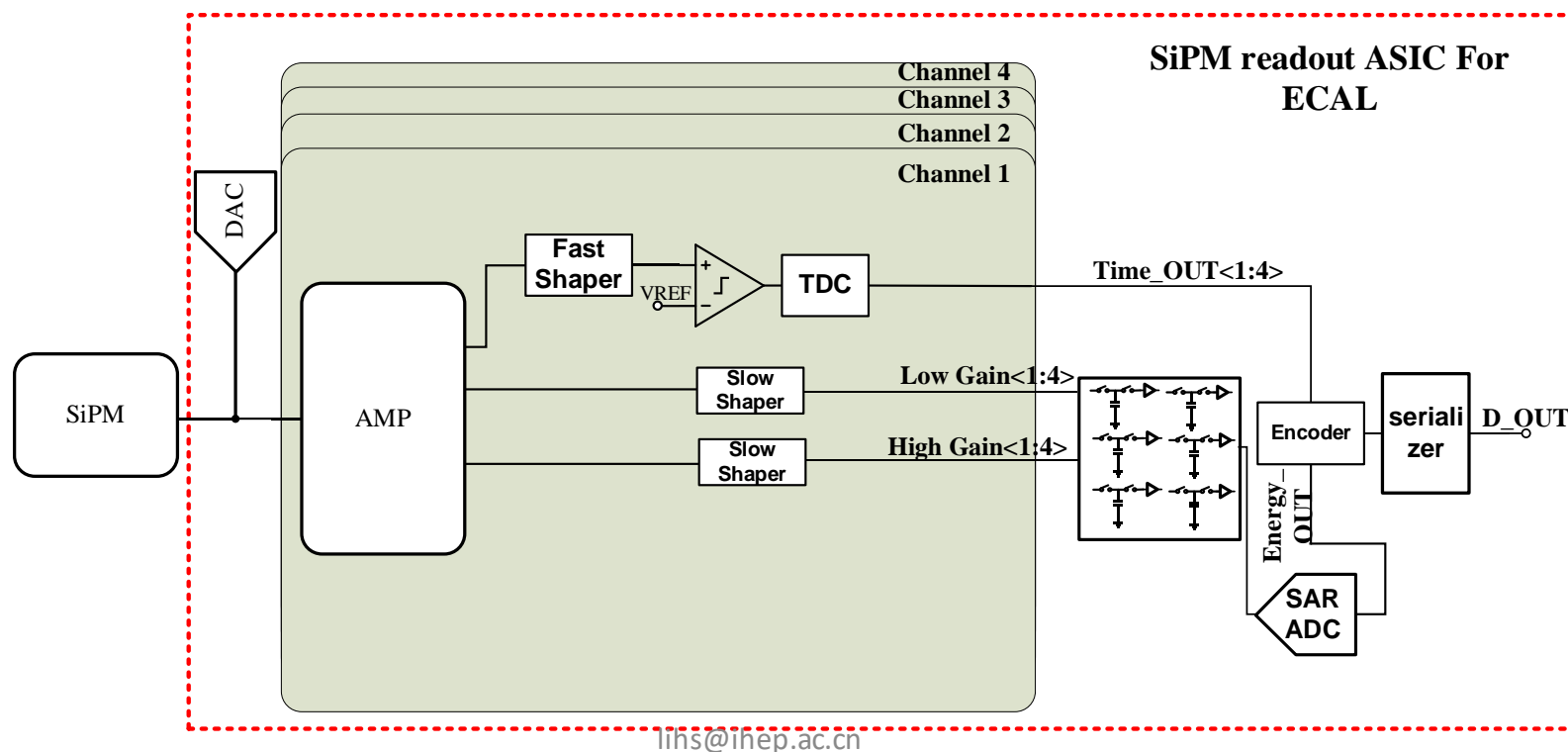
SIPACO实现目标:

- 动态范围: 1.28pc~2.81nC
- INL < 3%
- TDC: 142ps

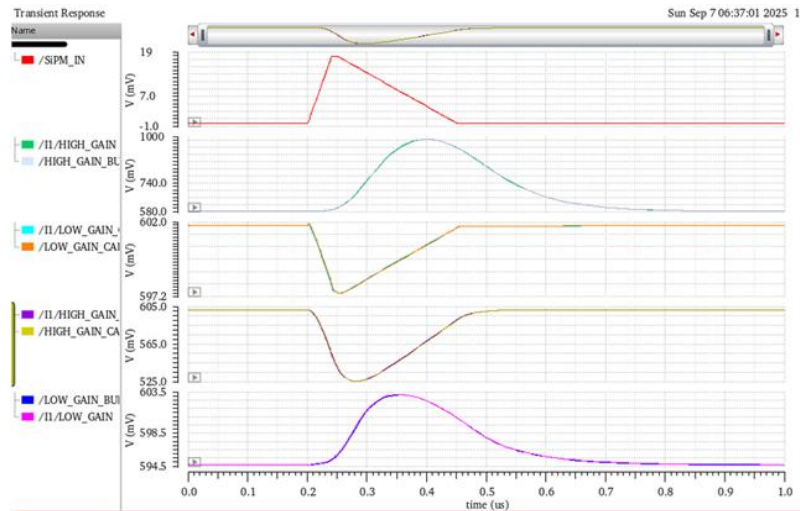
# SIPACO的改进版本--SIPAC\_E

## ■ SIPAC\_E: SIPACO的改版

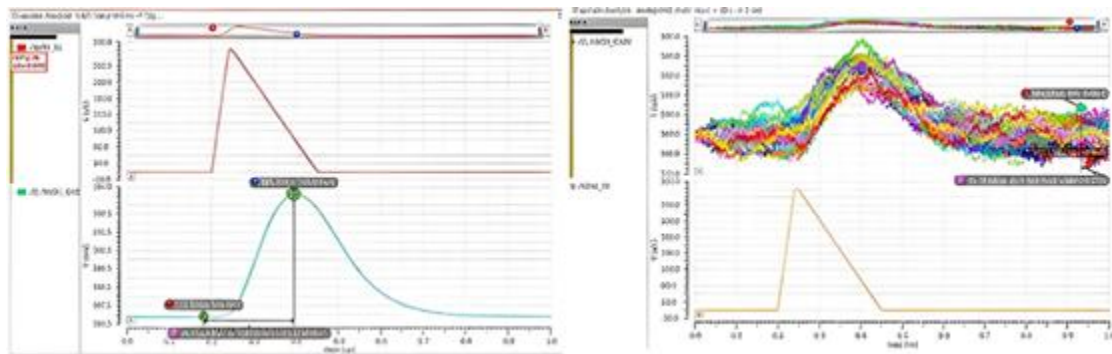
- 修正SIPACO存在的已知问题
- 优化成形电路、采样电路以及控制逻辑等
- 更小的面积: from 2.0mm x 2.3mm, to 1.3mm x 1.9mm



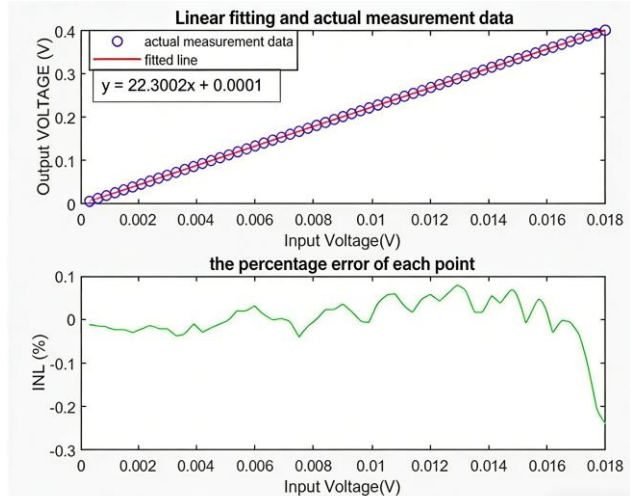
# SIPAC\_E---关键指标仿真



各个测试点的信号

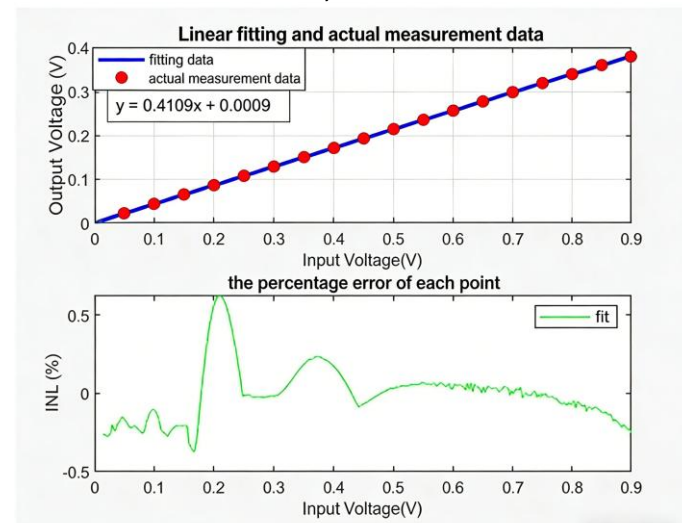


小信号输入时的噪声仿真



Linearity of Buffer Output Node in High-gain Gear

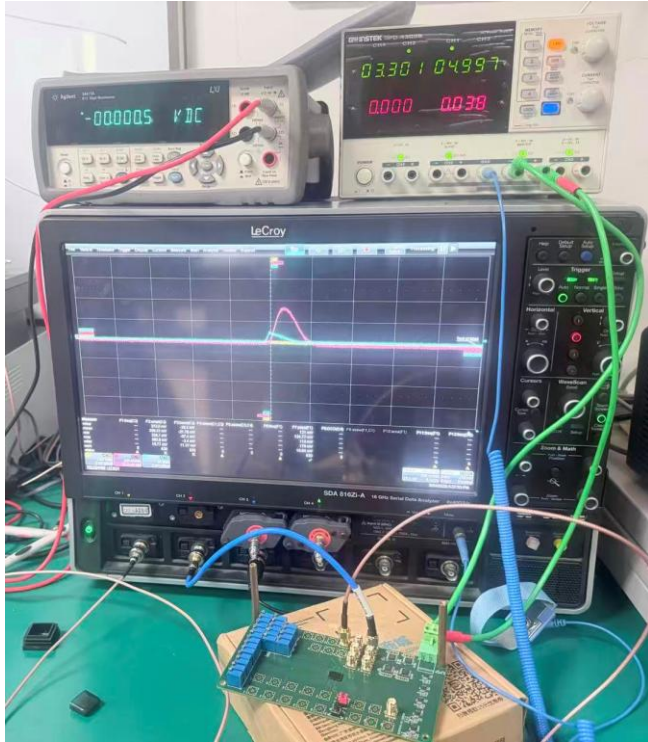
1-60MIPs, INL<0.3%



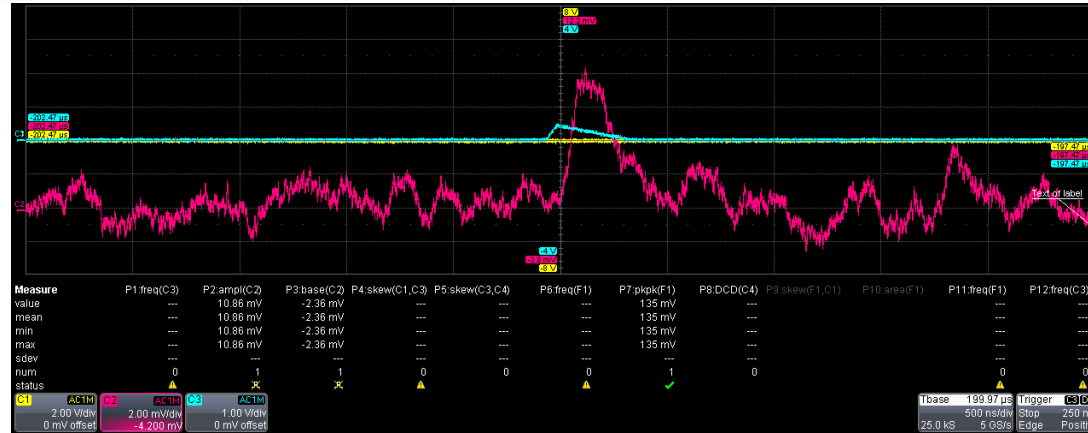
Linearity of Buffer Output Node in Low-Gain Gear

50-3000MIPs, INL<0.6%

# SIPAC\_E---噪声测试



测试环境



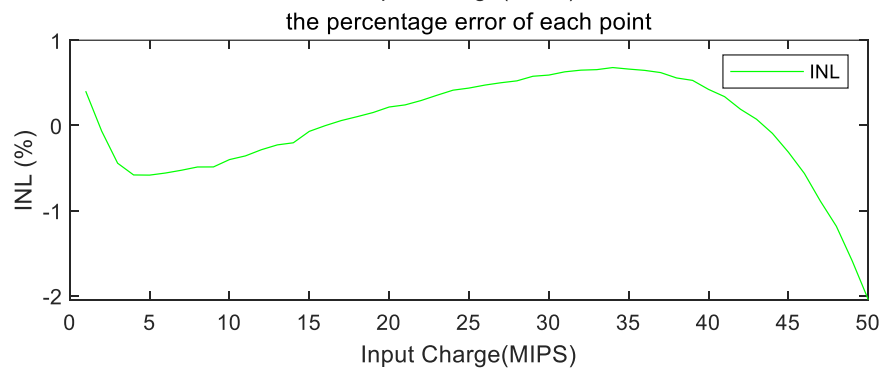
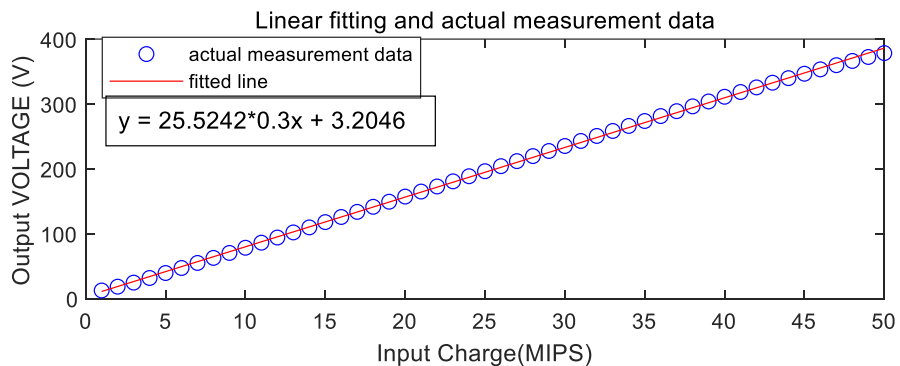
1 MIPS 输入时高增益shaper输出



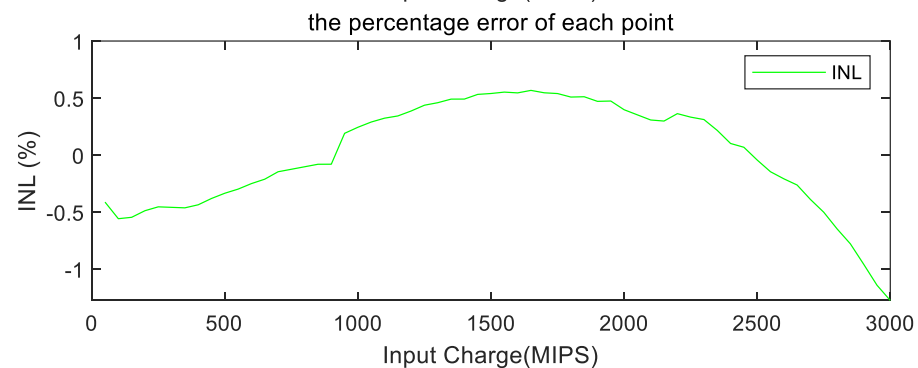
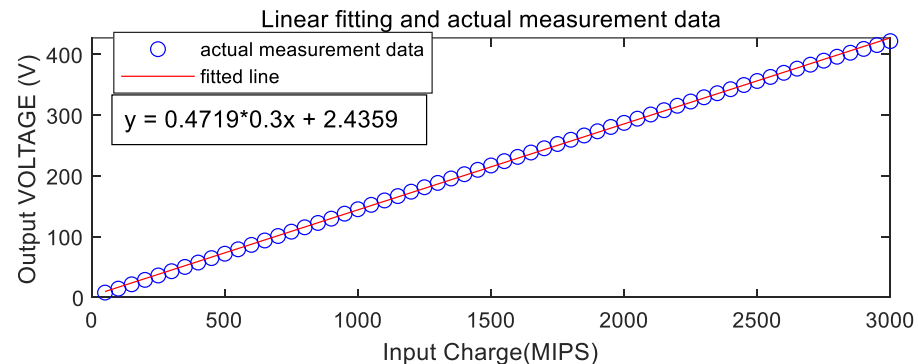
高增益shaper基线噪声

- 输入信号脉宽为400 ns，1.28 pC的电荷信号等效于300 μV峰值的三角波。
- 在1MIPS（300 μV）输入时，信号的幅值为10.86 mV。
- 在不给信号时，基线的rms噪声约为615 μV，信噪比约为17.65。

# SIPAC\_E---动态范围测试



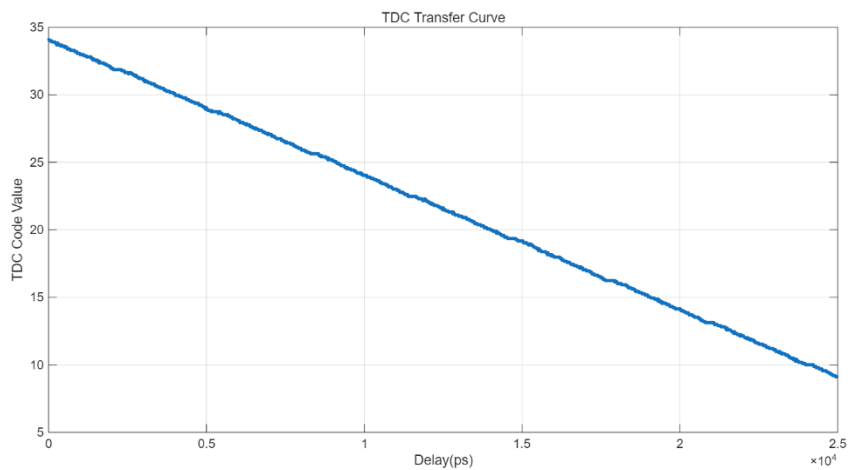
高增益档位INL<2%, Gain:25.52



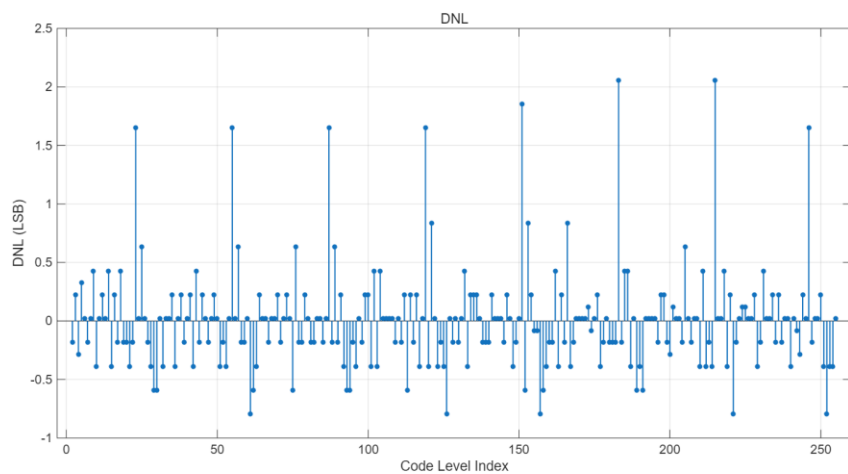
低增益档位INL<1.2%, Gain: 0.47

动态范围: 1MIP – 3000 MIP (300 $\mu$ V – 900 mV)

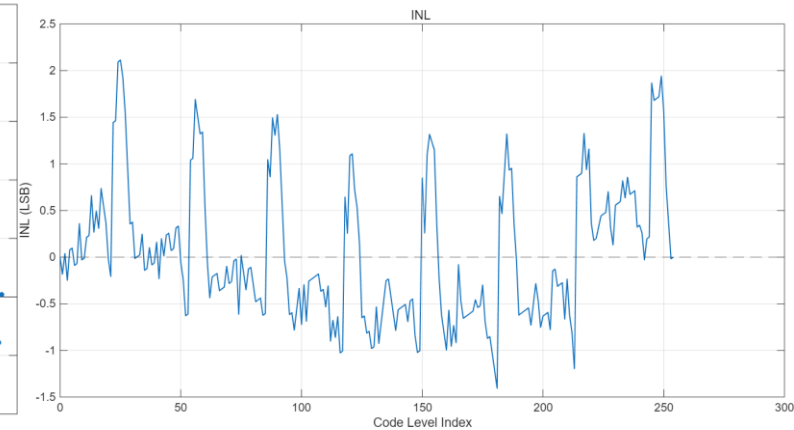
# SIPAC\_E---时间分辨测试



TDC转移曲线



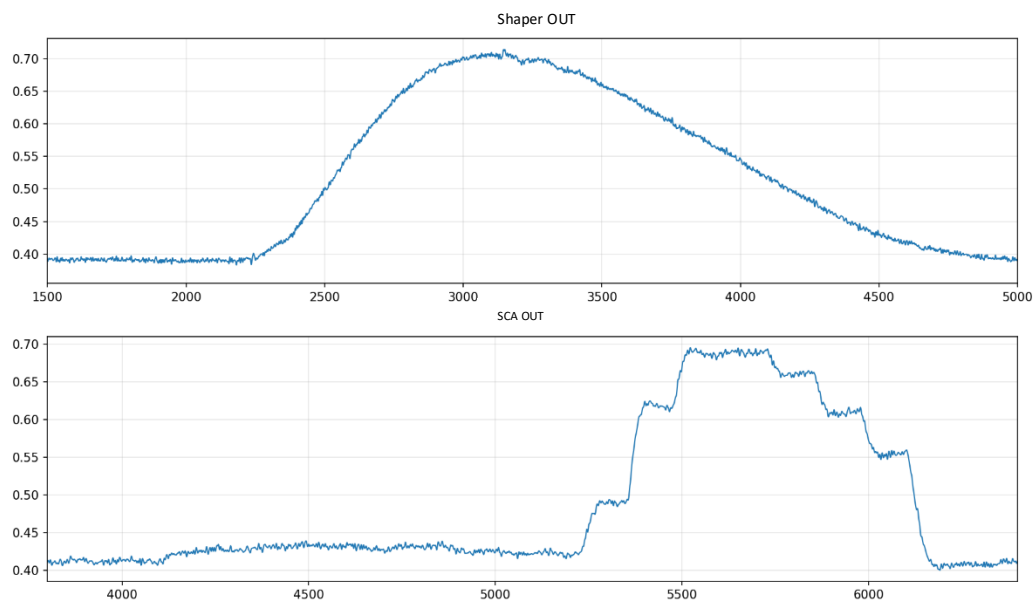
TDC DNL



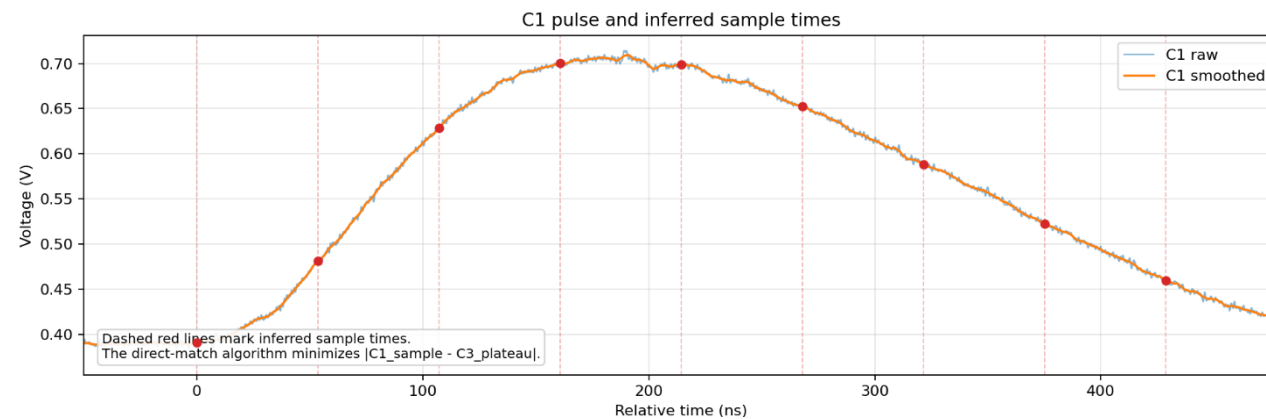
TDC INL

在前端jitter 80 ps时测试TDC的性能，TDC的LSB为102 ps，最大INL和DNL约为 2 LSB。

# SIPAC\_E---SCA测试



开关电容采样波形



波形拟合

在将采样波形拟合到原始波形，线性相关系数 $r=0.972$

# 主要指标对比、小结

## 1、主要指标对比

芯片指标对比			
设计指标		SIPACO	SIPAC_E
输入动态范围	300 $\mu$ V- 900 mV (3000倍)	0.5 mV - 1.1V (2200倍)	300 $\mu$ V- 900 mV (3000倍)
高增益档位增益	8	7.3	25.52
低增益档位增益	0.5	0.3	0.47
高增益档位线性度		1%	2%
低增益档位线性度		2.30%	1.2%
信噪比	5@300 $\mu$ V(1MIP)	4.3@1mV(0.5 MIPS)	17.65@300 $\mu$ V(1MIP)
TDC精度	100 ps	142 ps	102 ps
ADC精度	ENOB 10bit		待测

## 2、小结及计划

- 主要指标已经达到或接近设计值
- 更详细的芯片测试正在进行中

谢谢大家!