基于HVCMOS的LHCb磁场上游径迹探测器的研发

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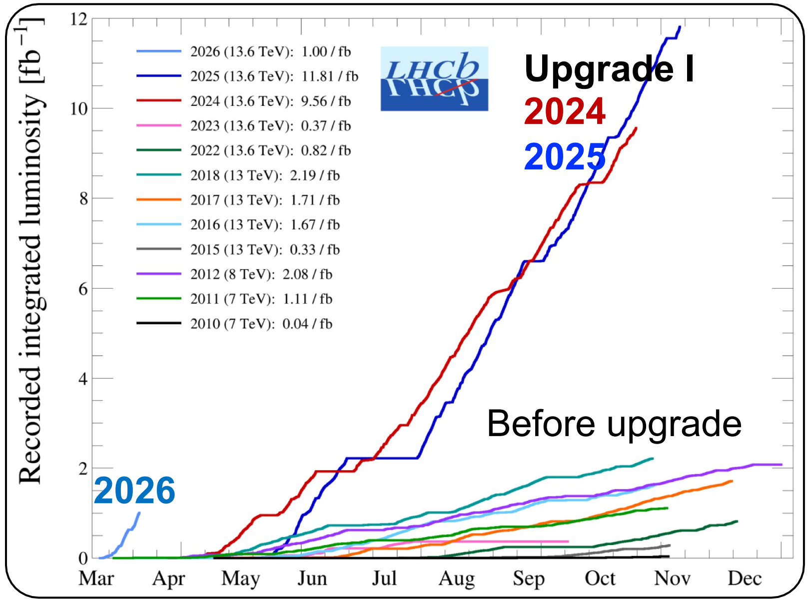
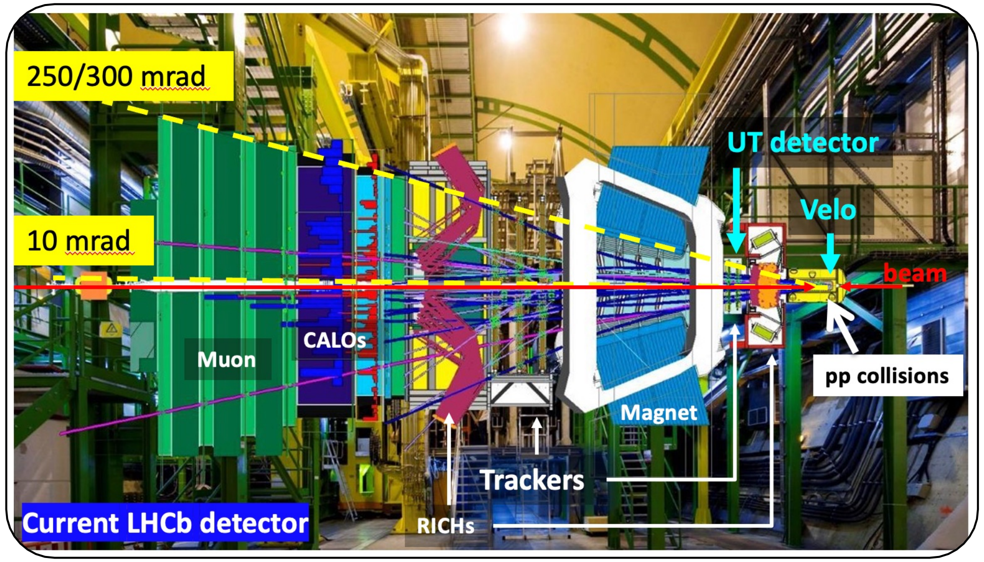
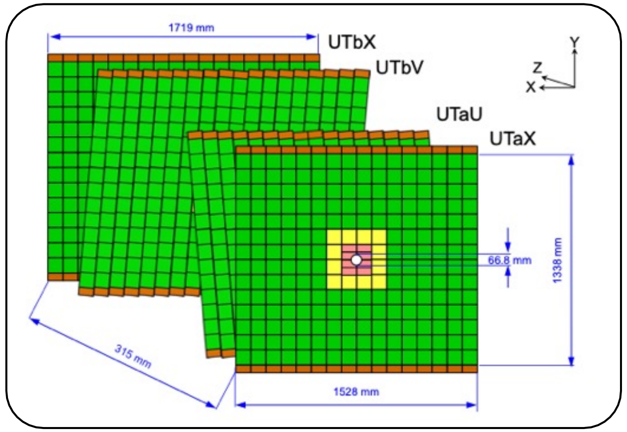
LHCb

LHCb：single-arm forward spectrometer at LHC
- ➢ Searches for NP and tests SM at the precision frontier

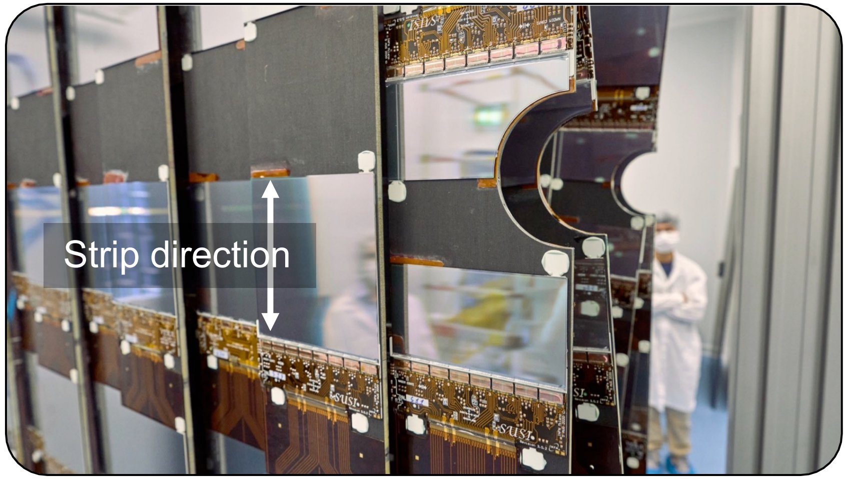
Upgrade I (2019~2023)
- ➢ No hardware trigger
- ➢ Lumi x5: $4\times10^{32}cm^{-2}s^{-1} \Rightarrow 2\times10^{33}cm^{-2}s^{-1}$
- ➢ New trackers，including UT
  - ❑ UT: 4-layer silicon strip detector







UT layout

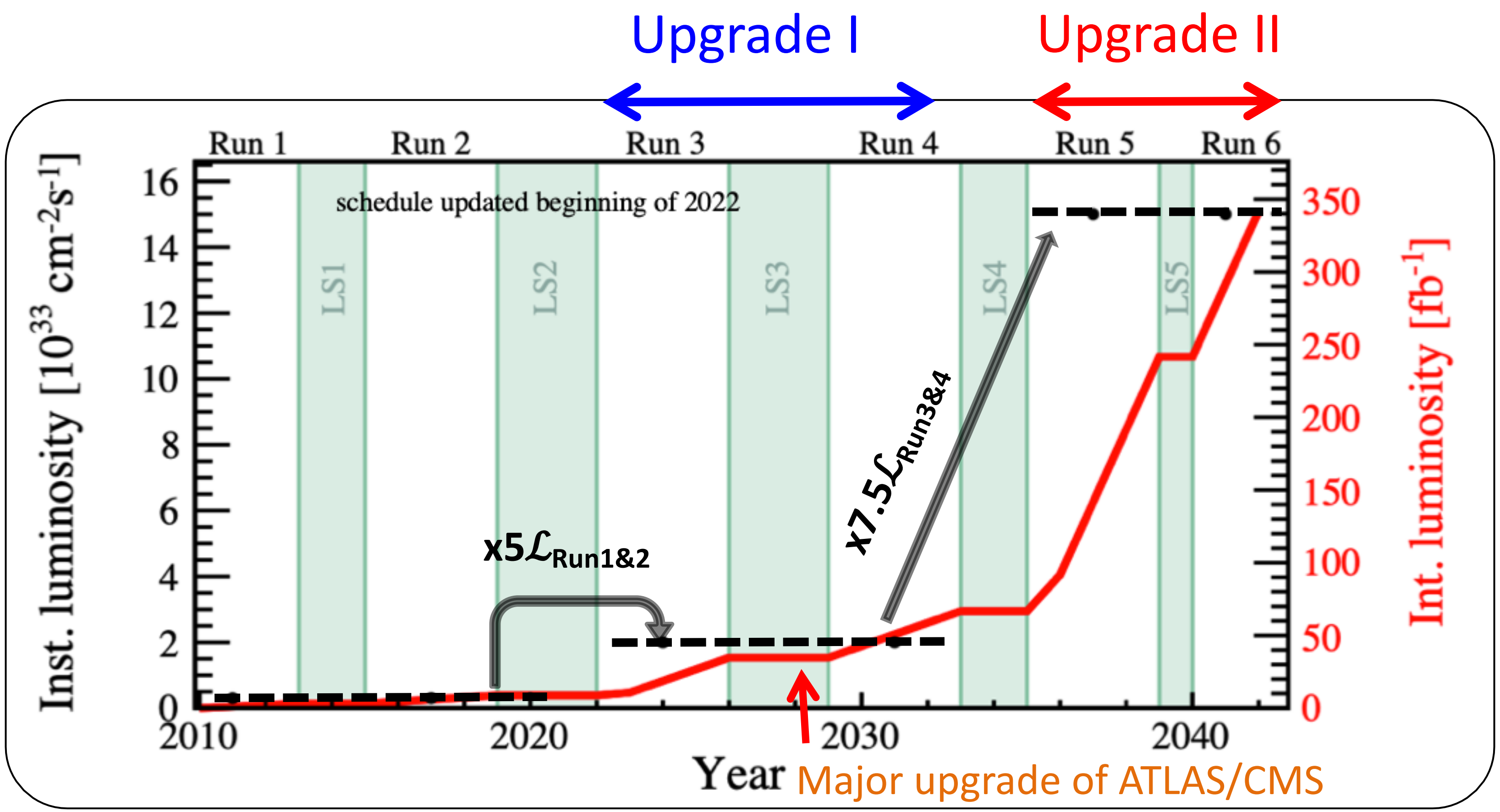


UT staves, modules and Si strip sensors

LHCb Upgrades

Upgrade I: LS2
$\mathcal{L}_{max}$~2x10^{33} cm^{-2}s^{-1}
$\mathcal{L}_{int}$~50 fb^{-1}

Upgrade II: LS4
$\mathcal{L}_{max}$~1.0-1.5x10^{34} cm^{-2}s^{-1}
$\mathcal{L}_{int}$~250-300 fb^{-1}



Major upgrade of ATLAS/CMS
LHCb also plan enhancements (U1b)

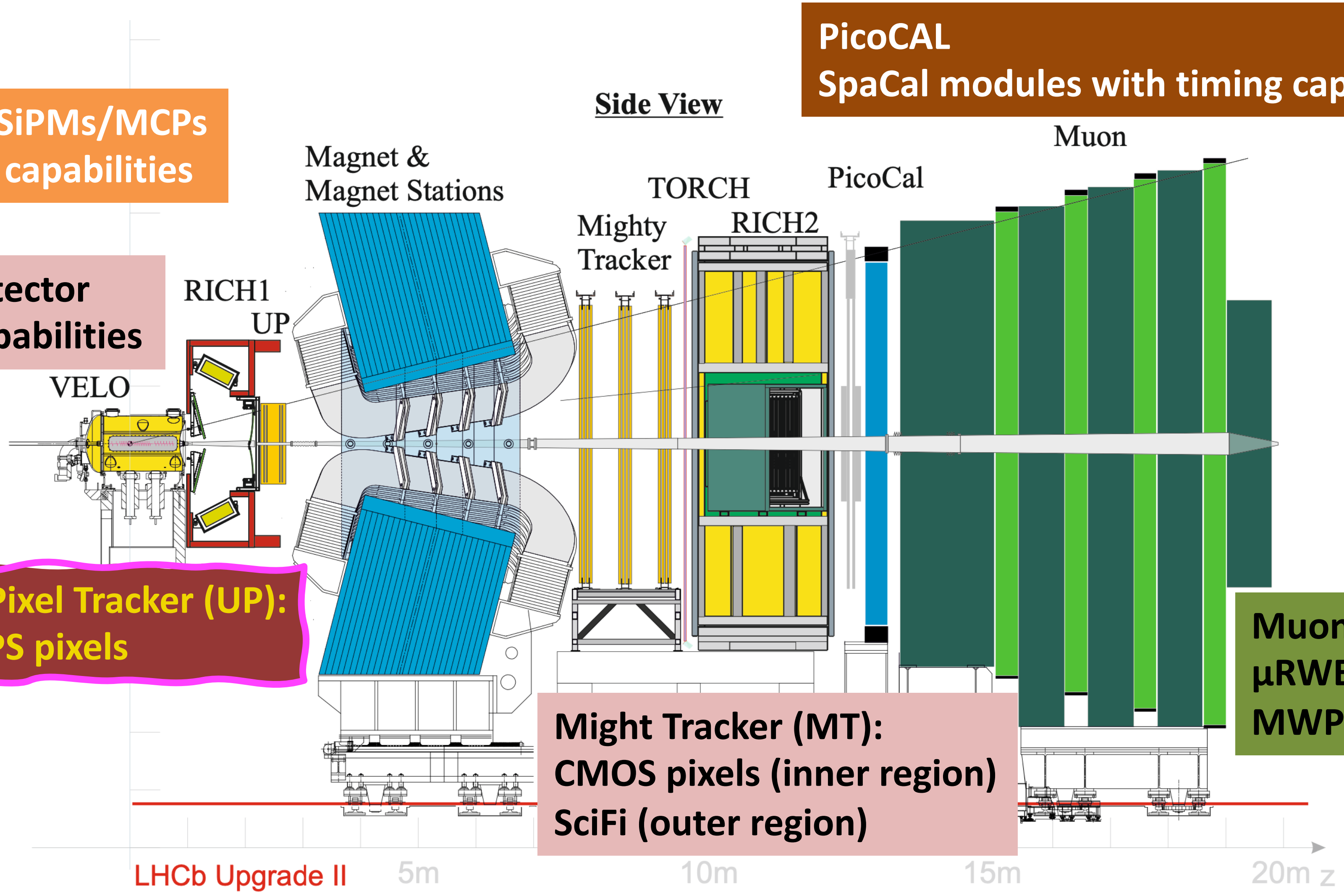
LHCb Upgrade II

RICH 1&2: SiPMs/MCPs and timing capabilities

VELO: pixel detector with timing capabilities

Upstream Pixel Tracker (UP): CMOS MAPS pixels

PicoCAL
SpaCal modules with timing capabilities



Might Tracker (MT):
CMOS pixels (inner region)
SciFi (outer region)

Muon:
μRWELL (inner region)
MWPCs (outer region)

Upstream pixel tracker (UP)

Upgrade II Lumi: 1.5x10^{34} cm^{-2}s^{-1} (**x7.5** $\mathcal{L}_{\text{Run 3\&4}}$)

- P-P collisions: ~6 hits/cm^2/BX (MAX)

Current UT not optimized for HL-LHC

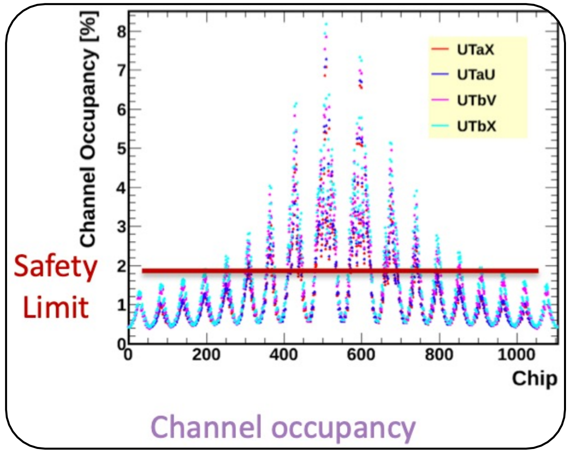
- Occupancy (max ~10%)
- Radiation does (3x10^{15}n$_{eq}$/cm^2)

UP in LHCb tracking system

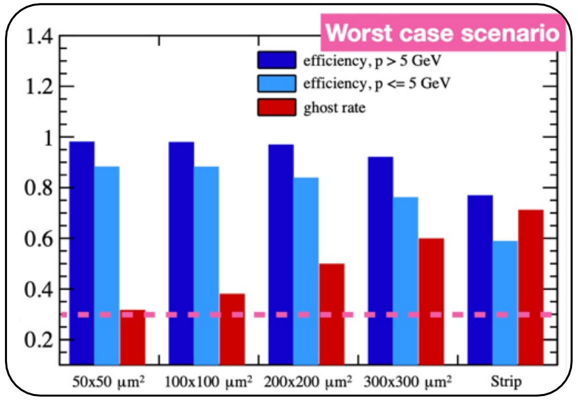
- Better σ(p)
- Lower $\mathcal{P}$(Ghost Track)
- Faster track reconstruction
- Long-lived particles (K_S or Λ^0)

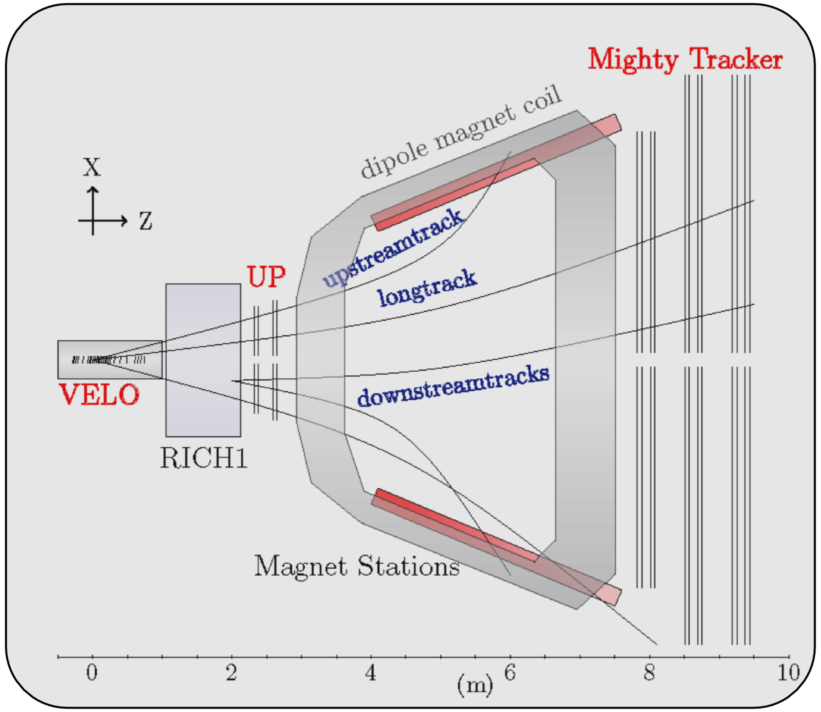
UP must satisfy

- Higher granularity than UT
- Full acceptance, according to other trackers
- Rad hardness and low material design



Channel occupancy



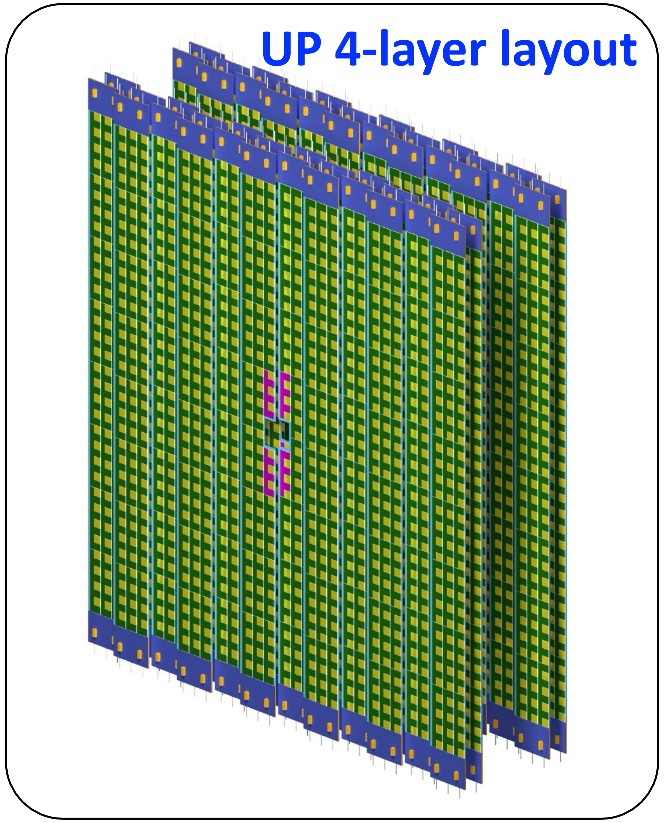


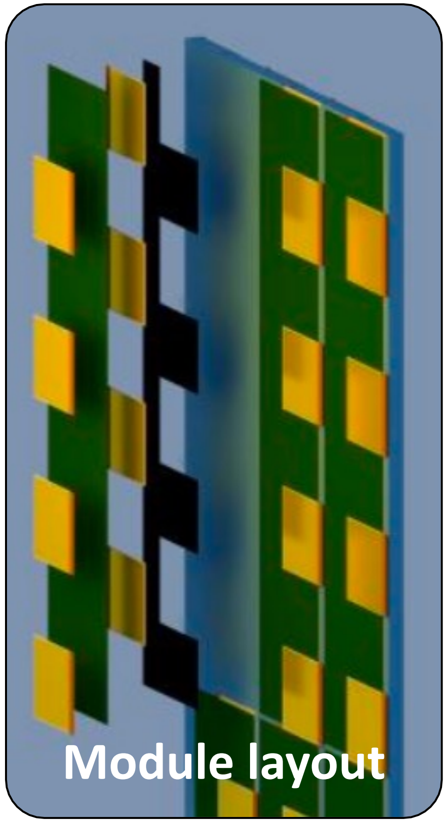
A CMOS pixelated detector, UP, will replace the current UT

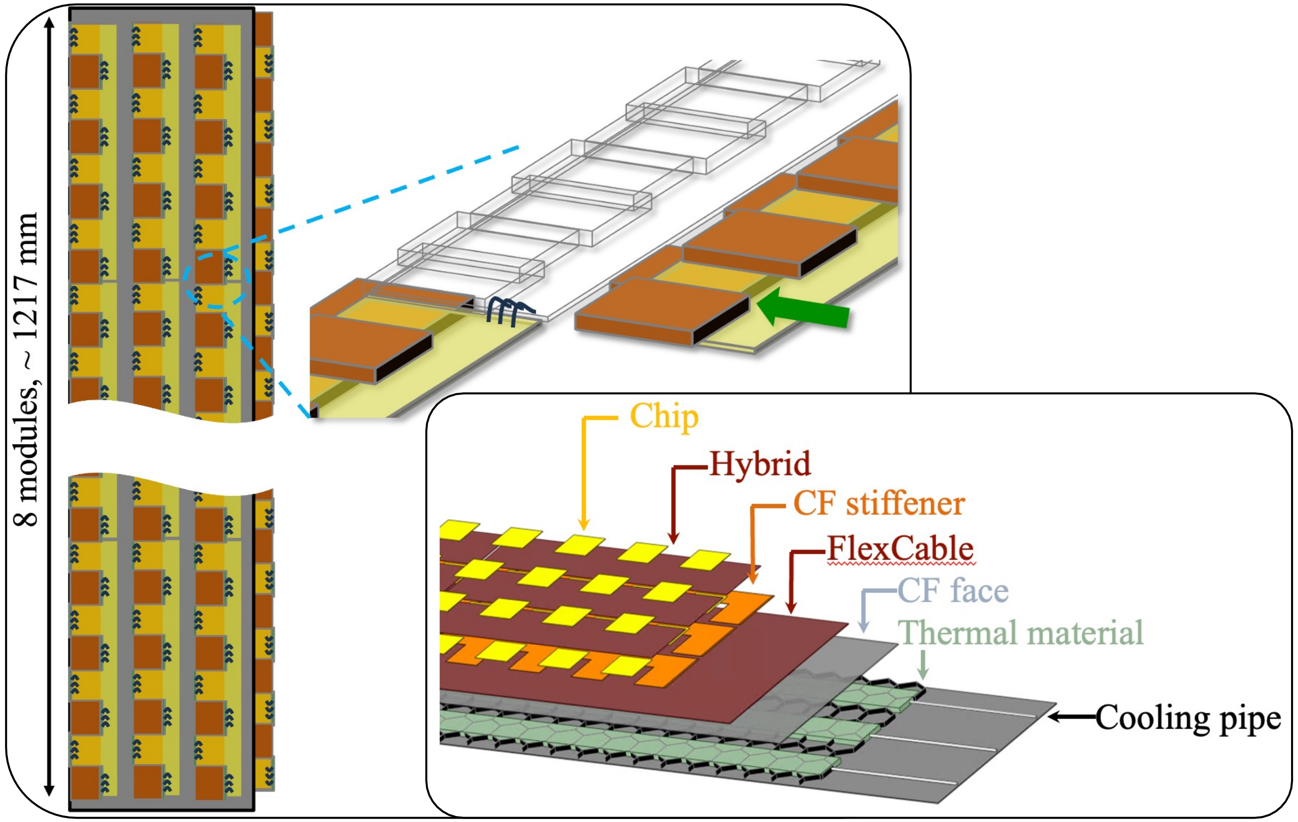
UP R&D status

- Layout design
- Development in chips, electronics
- Prototyping
- Thermal studies
- UP performance in LH-LHC tracing system

UP layout







Still 4-layer detector with stave structure to improve overlap

- Stave/module design to be decided before Upgrade II TDR

Full coverage on UP layers

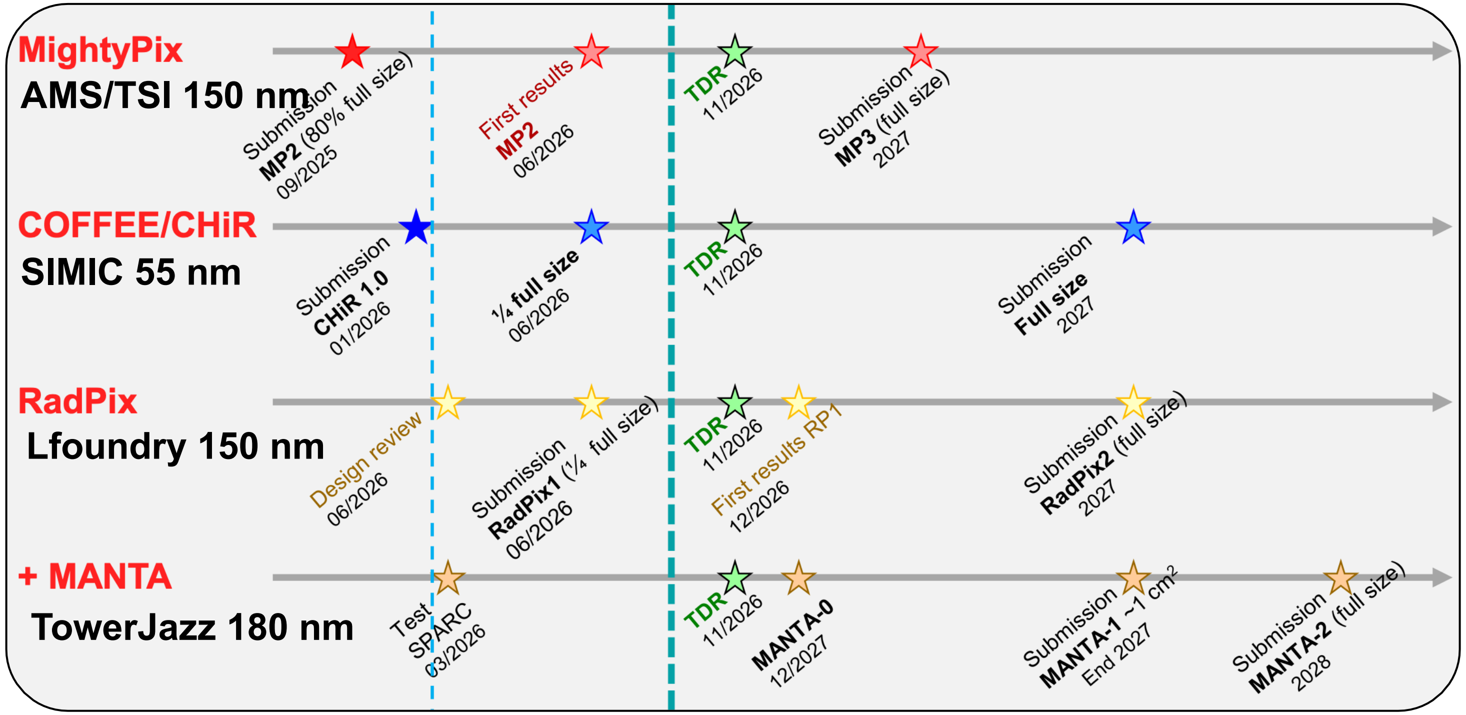
- Staggered arrangement on module/stave level

CMOS chips specifications

芯片研发细节参考
李一鸣、周扬的报告

Several chip candidates developed in parallel

- Radpix, MightyPix, Manta, COFFEE/CHiR …



Now

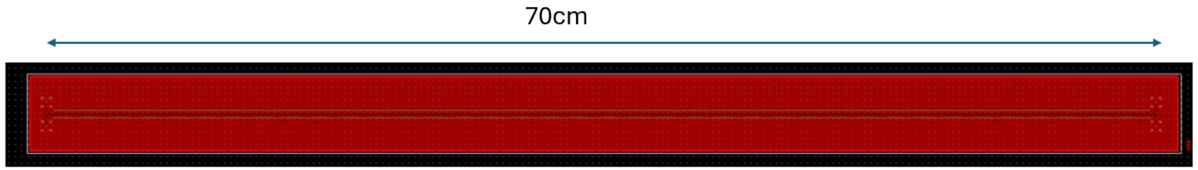
Assess the evidence of radiation hardness …

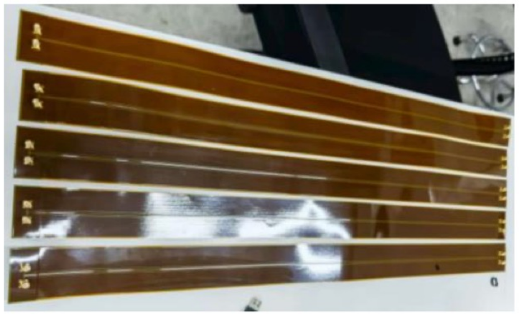
Parameter	Specification
Pixel size, square rectangular	≤ 85x85 μm² ≤ 50x200 μm²
Substrate thickness	< 200 μm
Max particle rate hit rate	50 MHz/cm² 100 MHz/cm²
Max length of data word	32 bits
Transmission rate	N x 1.28 Gbps
Overall efficiency	> 96%
In-time efficiency	> 99% within 25ns
Noise rate (end of life)	≤ 400kHz/cm²
Rad-hardness (NIEL) (TID)	4×10^{15} n_{eq}/cm^2 250 MRad
Power consumption	≤ 200 mW/cm²

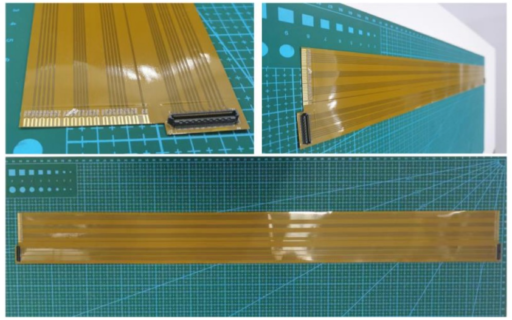
Data flow and Flex Cable

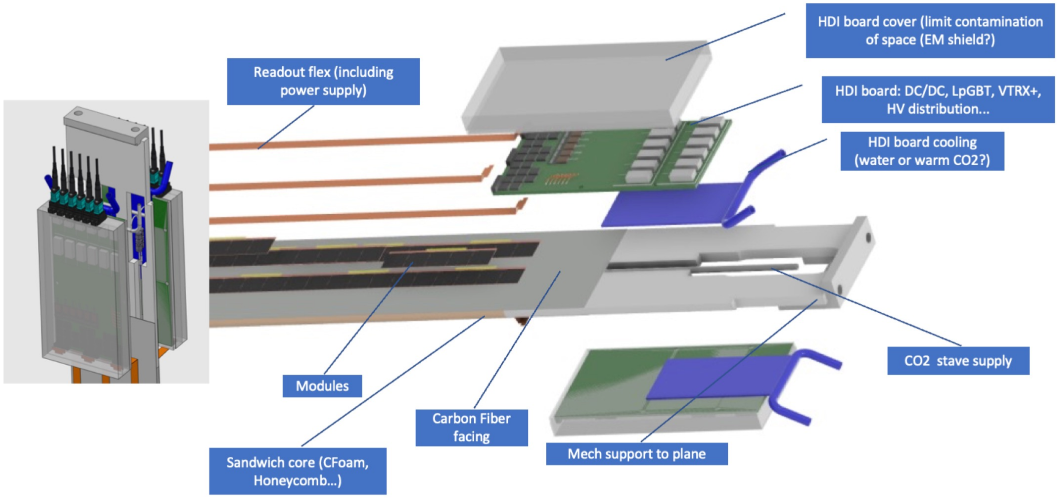
Data transmitted via FlexCable

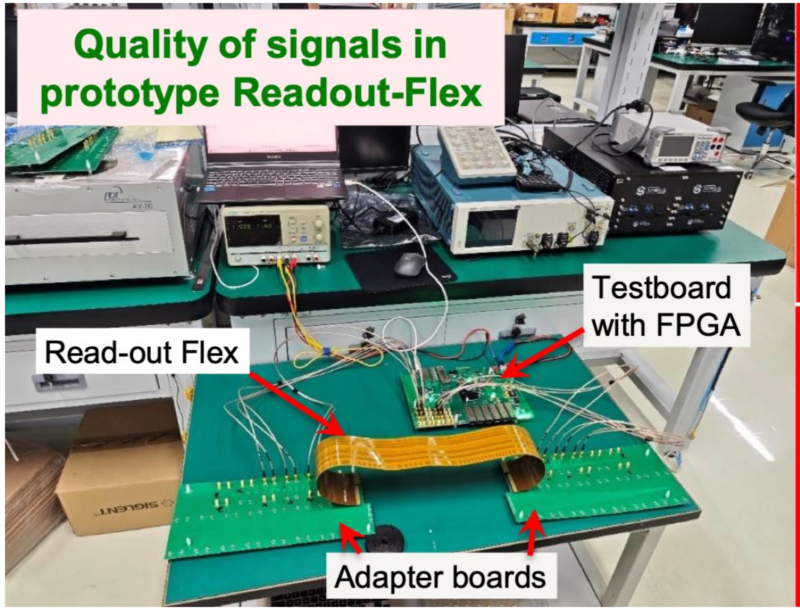
- Single differential pair with impedance 100 Ω
- Signal integrity vs material budget
- Test Max length of differential pairs

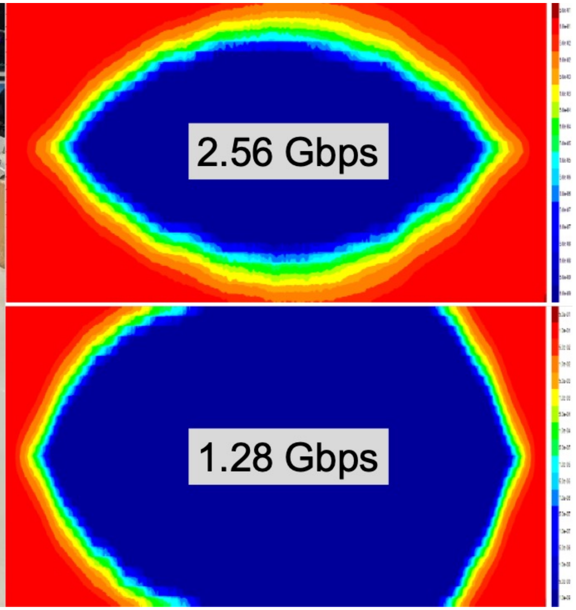








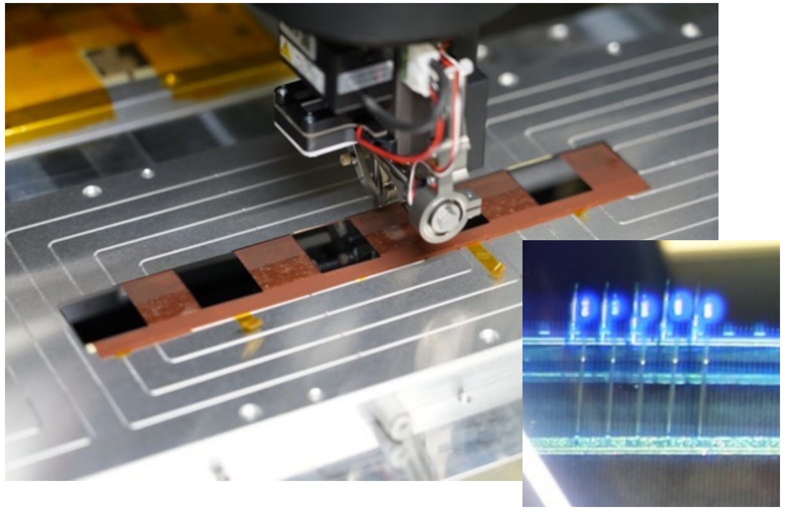




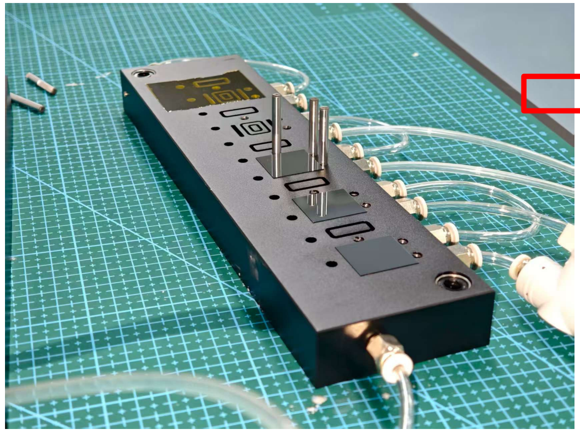
Mechanical mockup producing

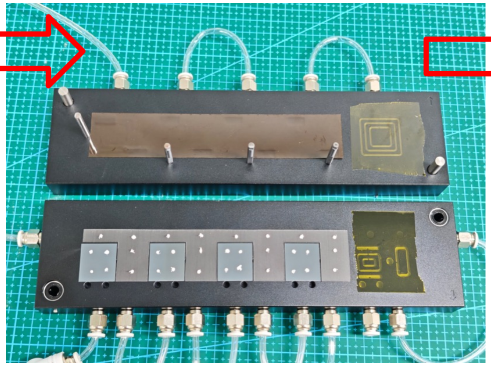
- 2025/03: V0 mechanical chips/hybrid ready
- 2025/05: 1st module assembled from IHEP + LU + HU
  - Tests on metrology/WB
- 2026/04: V1 chip ready, with heating circuit

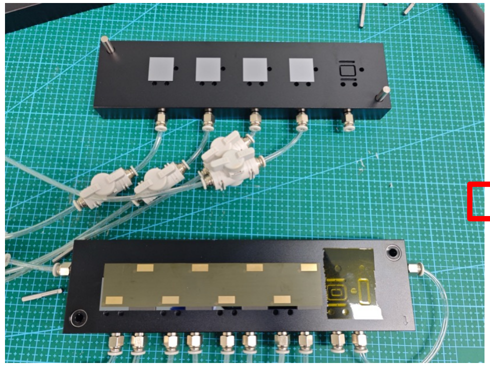
Strong supports for WB

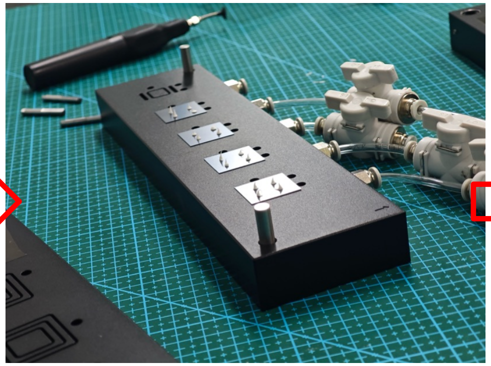


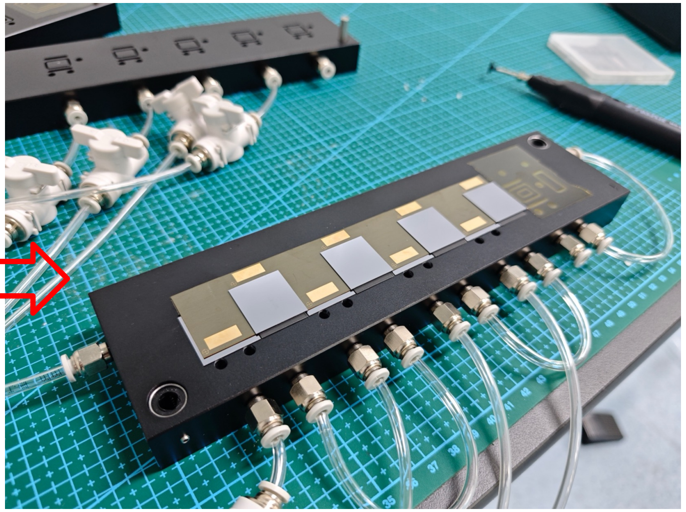
Low layer assembly







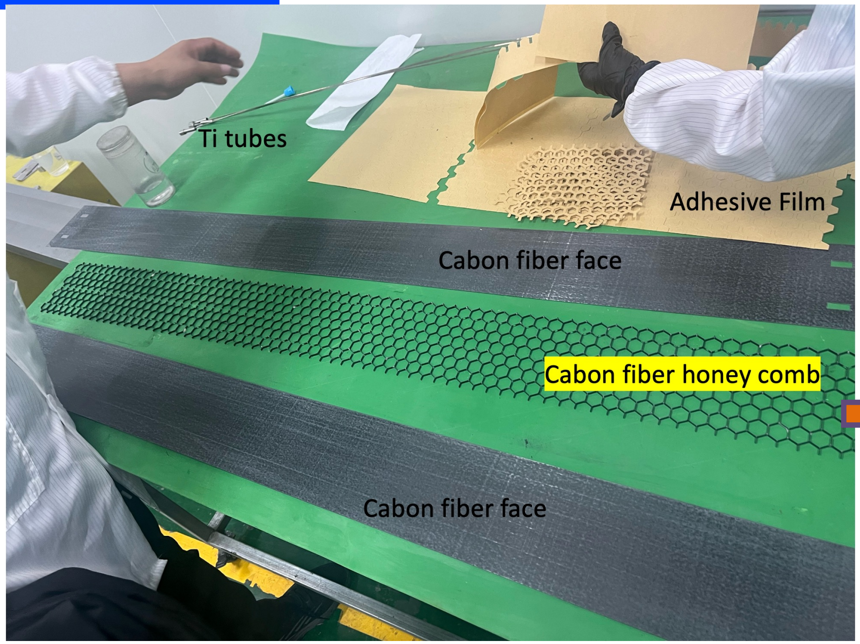


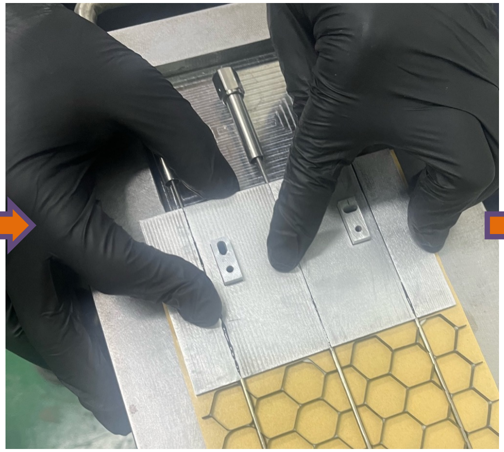


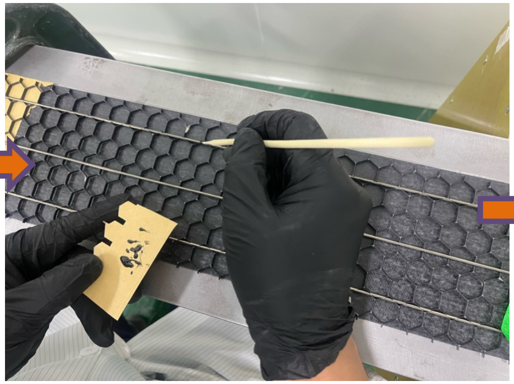
Upper layer assembly

Bare stave production

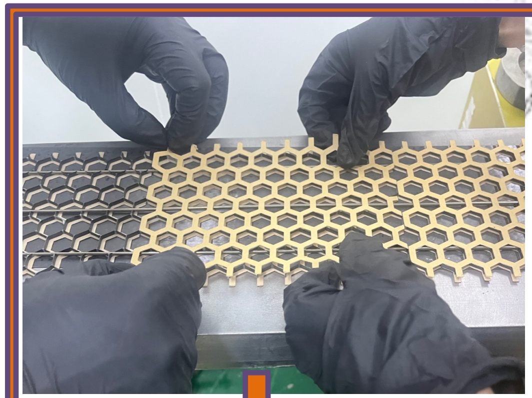
- 2025/06: V0 bare stave produced
- 2025/12: V1 stave with thermal materials
- Next step: full stave with modules

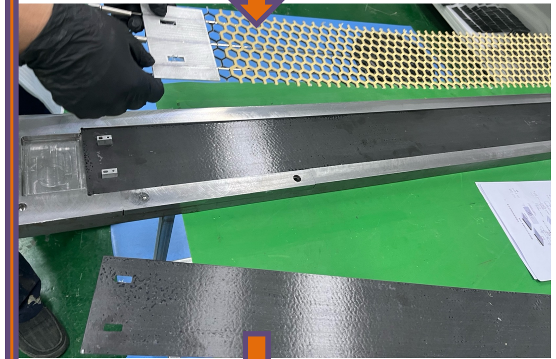


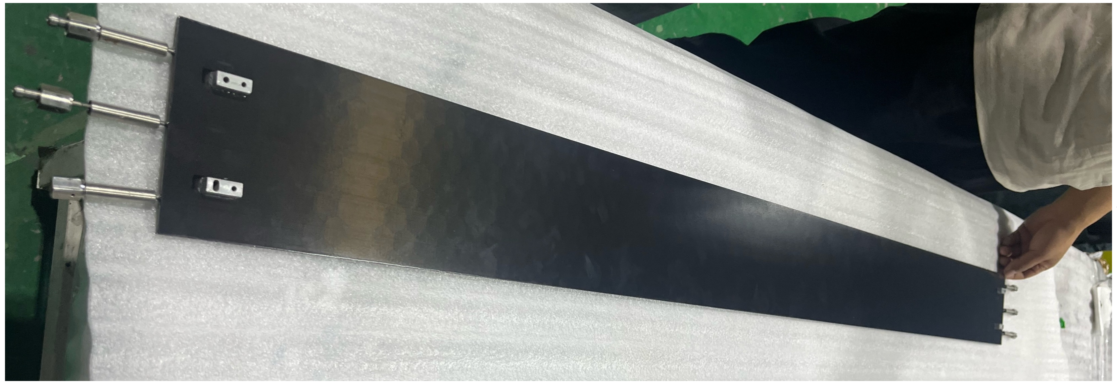




x2



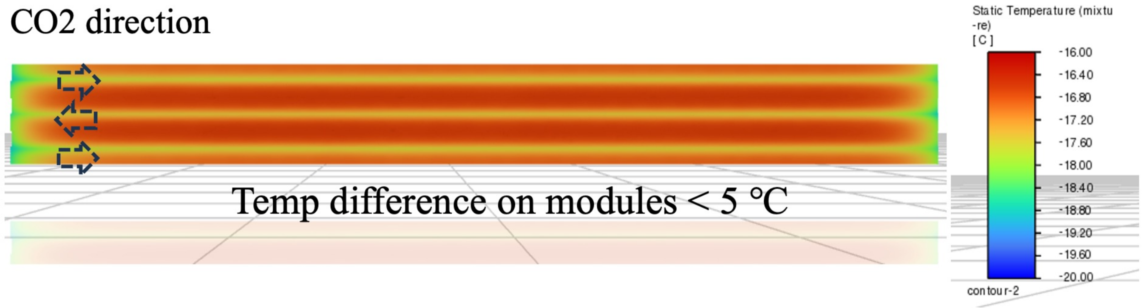


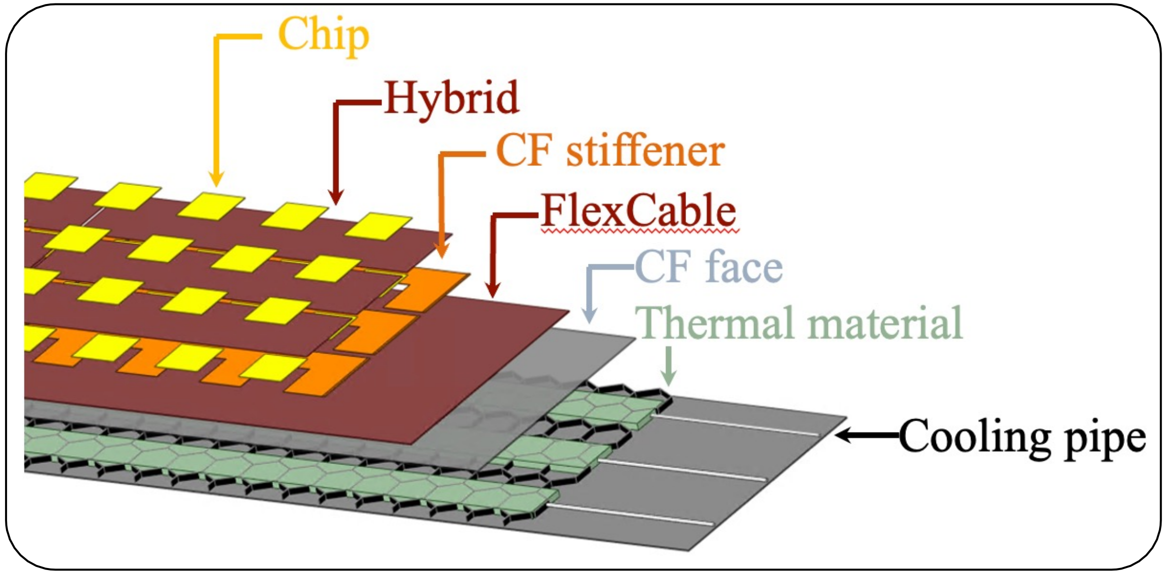


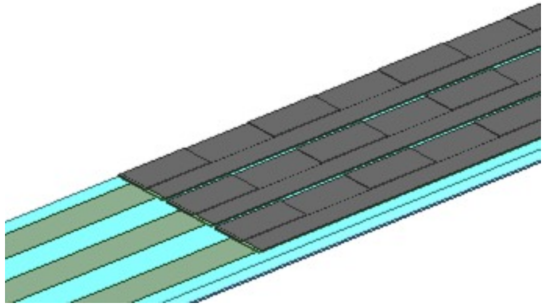
Thermal studies

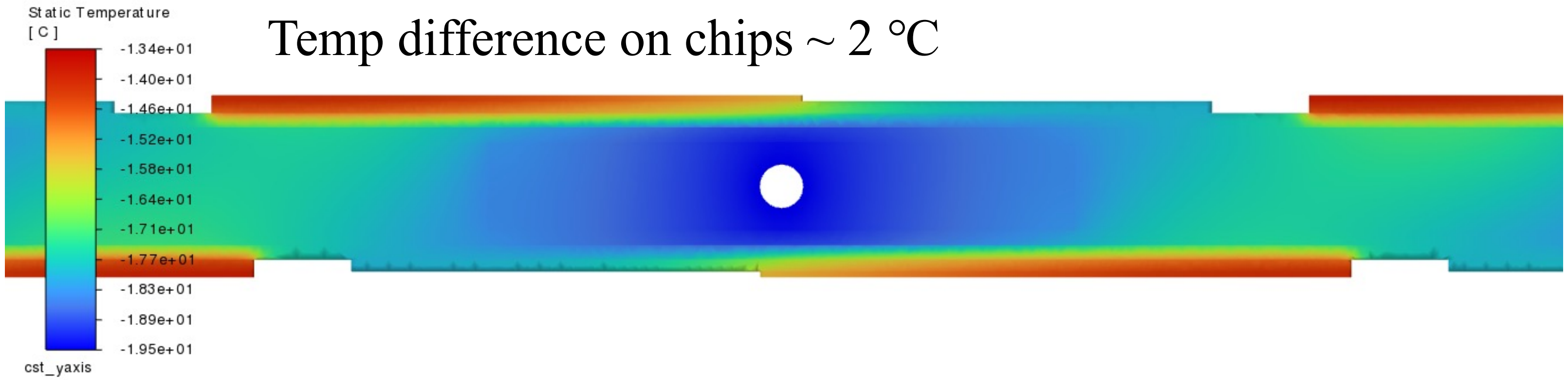
Challenge on cooling for chip heat power 200 mW/cm^2

- ➢ R&D for stave/module thermal performance ongoing
  - ❑ Material investigation
  - ❑ Thermal simulation





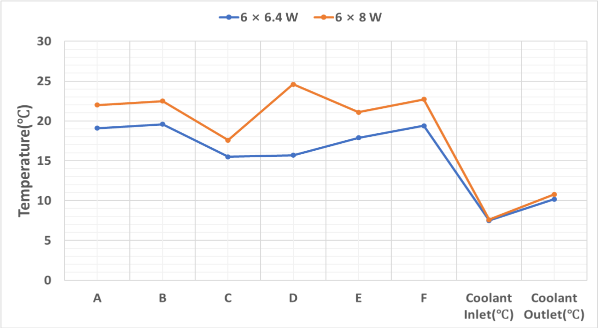


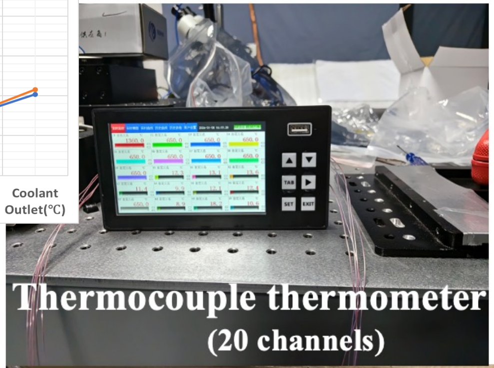


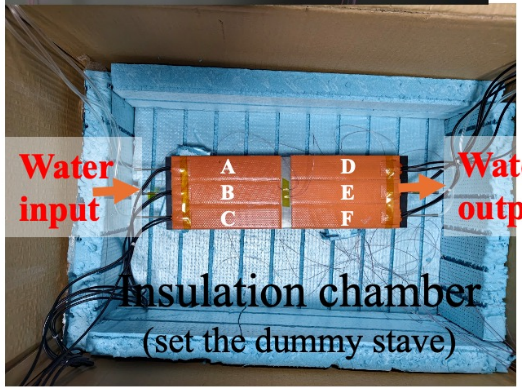
Thermal studies

Preliminary tests at bare stave level using water cooling

- ΔT~5℃ @ 200mW/cm^2







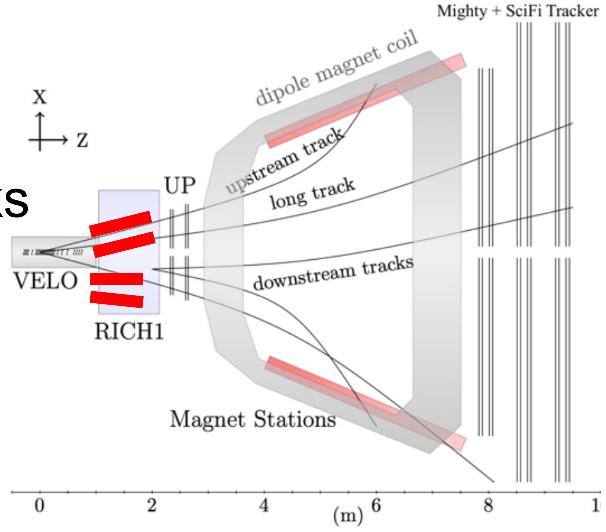
CO2 cooling system ready by 2026/03

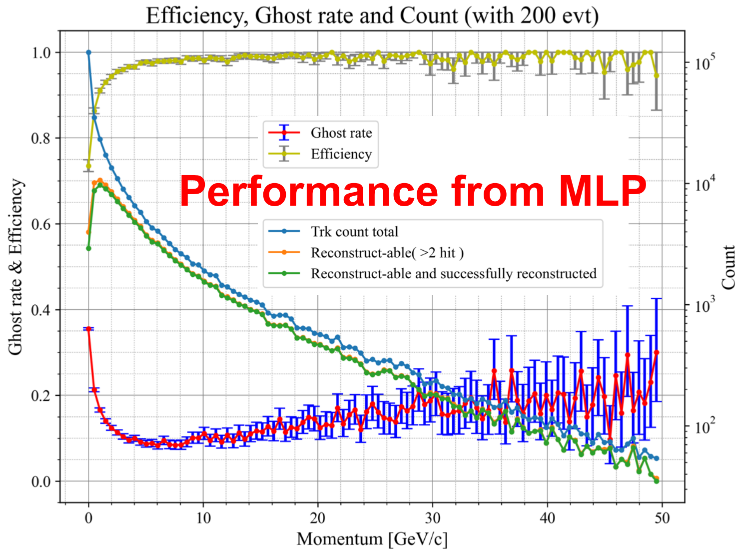
- CO2 loop + Control + thermal chamber
- Enable thermal tests for max 4 staves simultaneously

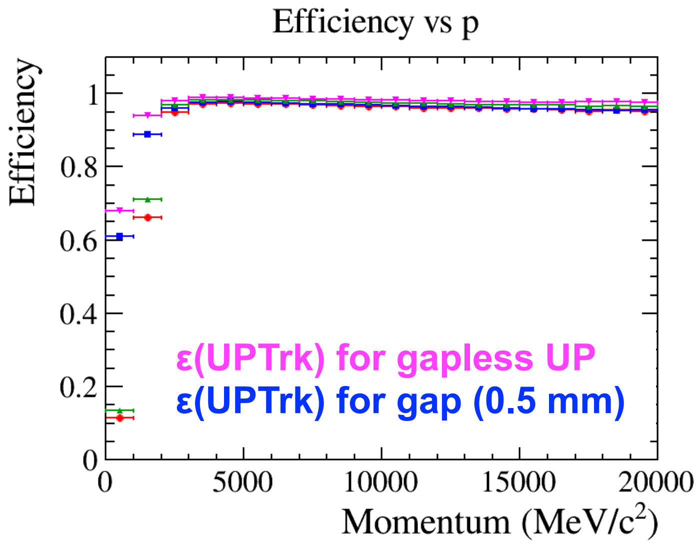
UP standalone track in HL-LHC

UP tracks reconstructed with 4-layer pixels

- ➢ Algorithm optimized for high ε & pure UP tracks
- ➢ ε & $\mathcal{P}_{GhostTrk}$ compared with gap vs gapless layout design
- ➢ New tracking technology developed
  - ❑ MLP, CAT, FPGA …





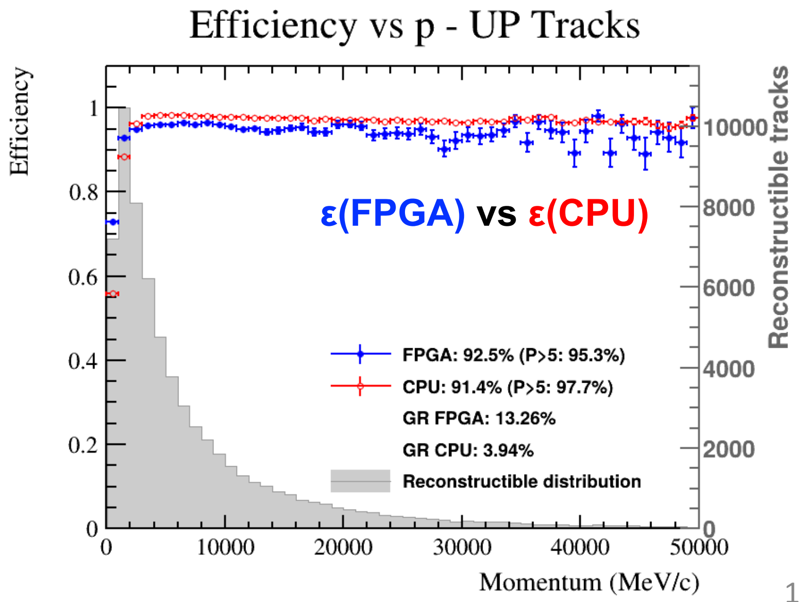


Comparison btw diff alg. and gap vs gapless

	Default Algorithm	Optimized algorithm	Default Algorithm	Optimized algorithm
UP Efficiency (All)	~82.14%	~91.53%	~84.08%	~94.26%
UP Efficiency (> 5GeV)	~96.34%	~96.58%	~97.42%	~98.11%
Ghost Rate	~10.78%	~4.07%	~12.32%	~3.47%

UP w/ gaps

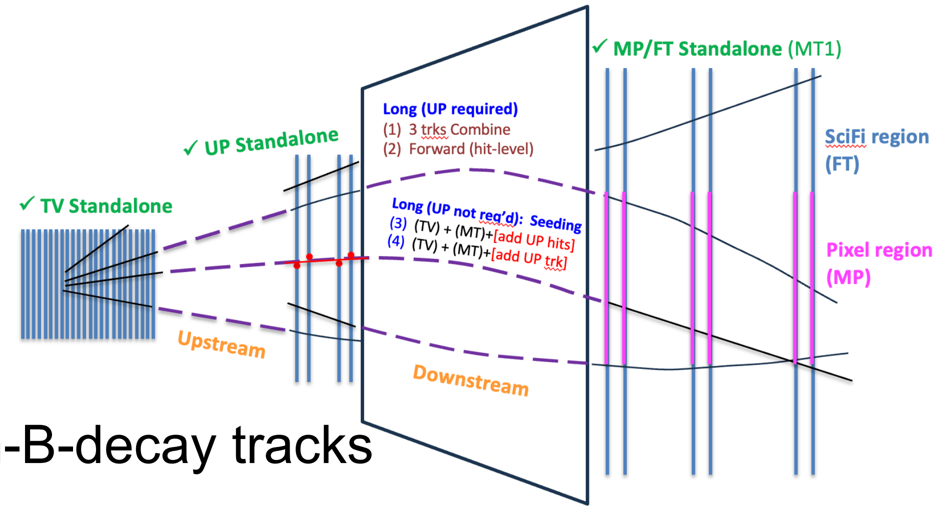
Gapless UP



Performance of LHCb tracks in HL-LHC

Multiple algorithms developed for LHCb (long) track

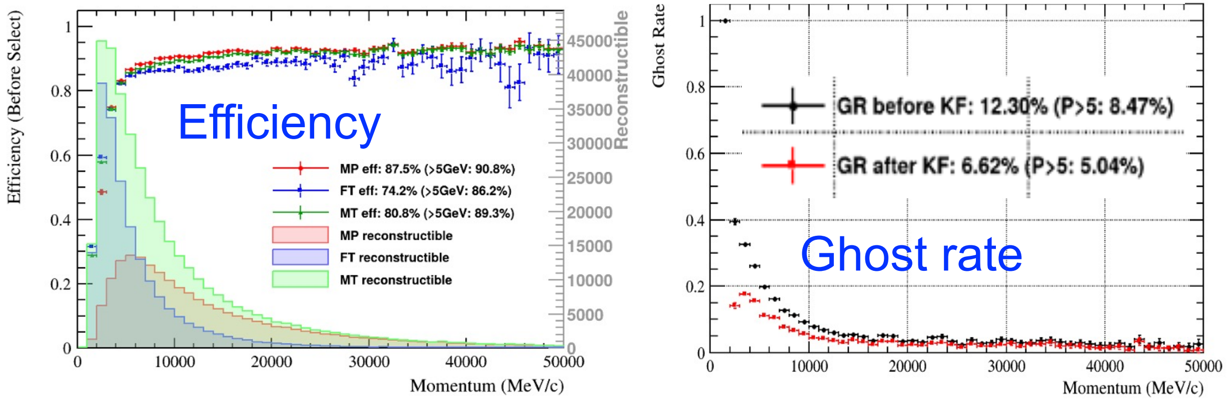
- Forward alg: Tracks from VELO extrapolated forward with hits in UP & MT sequentially
- Match alg: Tracks by VELO and MT, then selected UP info.
- Backward alg: 3 sub-detector tracks combined directly
  - UP+MT tracks passing magnet → better σ(p)



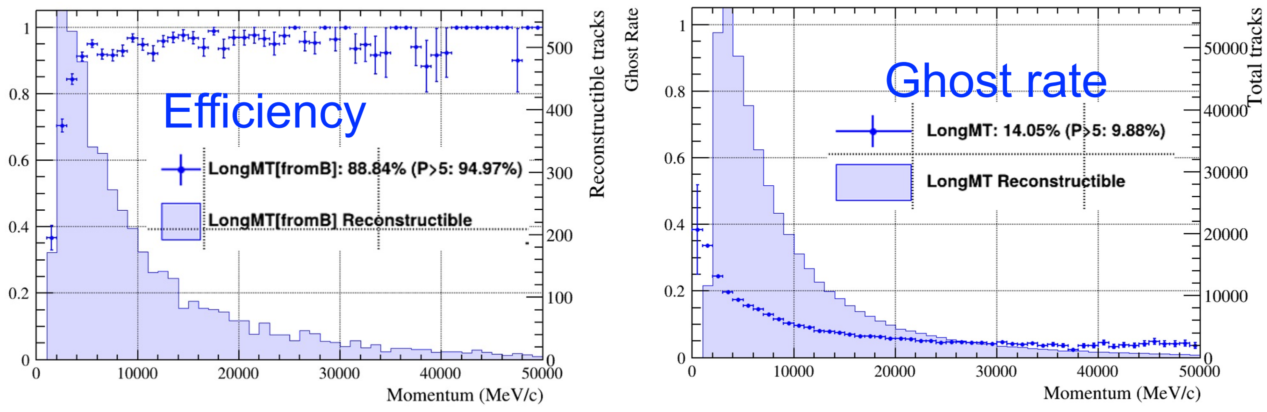
Tracks merged from all three algs. give **ε~95%**, **GR~𝒪(%)** for from-B-decay tracks (Just at PR level, following KF will further suppress GR)

- Similar as current LHCb performance

Long Tracks by "backward alg"



Long Tracks by all 3 algs. after clone killer



UP work package

WPs	Work Packages and Sub-WPs	Leaders
WP.0	TDR preparation	Marina Artuso / Syracuse
WP.1	Simulation, reconstruction and performance	Xuhao Yuan / IHEP, Steve Blusk / Syracuse
1.1	Detector description and simulation software	Xiaokang Zhou / CCNU
1.2	Reconstruction and performance study	Peilian Li / UCAS
WP.2	Pixel sensor chip development	Yiming Li / IHEP, Fabrice Guilloux / IRFU
2.1	Sensor chip design	Xiaomin Wei / NPU, Yang Zhou / IHEP
2.2	Sensor chip evaluation	Elisabeth Niel / LLR, Hui Zhang / IHEP
WP.3	Module and stave	Ray Mountain/Syracuse, Jiesheng Yu/HNU, Manuel Guittiere/Subatech
3.1	Design and prototyping	*(Xuhao Yuan / IHEP),* Theo Bigourdan / Subatech
3.2	Stave mechanical and thermal study	Yi Yang / HNU, (Arnaud Cadiou / Subatech)
3.3	Module evaluation	Charlotte Riccio / IRFU
WP.4	Overall mechanics, installation and cooling	Arnaud Cadiou / Subatech
4.1	Mechanical support	Meriadeg Guillamet / Subatech
4.2	Detector integration and installation	Meriadeg Guillamet / Subatech, Bassem Khanji / Syracuse
4.3	Cooling system	Hangyi Wu / Syracuse
WP.5	Data acquisition system	Kai Chen / CCNU, Zijun Xu / IHEP
5.1	Overal readout scheme	*(Jiachun Wang / IHEP)*
5.2	UP-specific firmware	*(Kai Chen / CCNU)*
5.3	Control and monitoring	*(Zijun Xu / IHEP)*
5.4	DAQ system for evaluation and production	*(Marina Artuso/ Syracuse)*
WP.6	Electronics	Kai Liu / LZU, Christophe Renard / Subatech
6.1	Design of FE electronics	Zhiqiang Fu / LZU
6.2	HV and LV systems	Kechen Li / HTU

PL: Jianchun Wang / IHEP, **DPLs**: Tomasz Skwarnicki / Syracuse (UT), Benjamin Audurier / IRFU (UP)

CCNU Wuhan | HNU Changsha | HTU Xinxiang | IHEP Beijing | IPT Ulaanbaatar | IRFU Saclay | LLR Palaiseau | LZU Lanzhou | NPU Xi'an | Subatech Nantes | Syracuse U Syracuse | UCAS Beijing

Summary

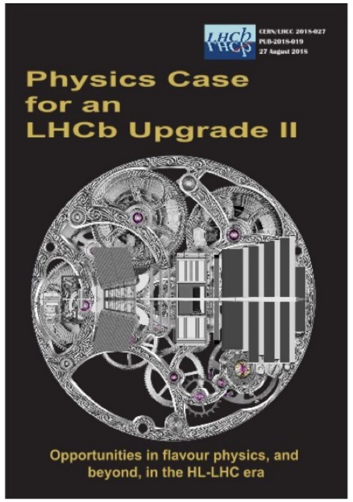
LHCb UP detector: Aiming for Upgrade II: starts in LS4, R&D now

- Based on CMOS MAPS tech
- A four-layer pixel-chip design, crucial for LHCb tracks reconstruction
- TDR by end of 2026

LHCb China group leads UP project

- Strengthen China's leading role in the international collaboration
- Boost high-precision physics capability and discovery potential for LHCb
- Cultivate advanced detector technologies and talents for future collider projects

More physics results can be expected from LHCb



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2018-08-29

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LHCb Upgrades and operation at 10^{34} cm^{-2} s^{-1} luminosity –A first study

G. Arduini, V. Baglin, H. Burkhardt, F. Cerutti, S. Claudet, B. Di Girolamo, R. De Maria, I. Efthymiopoulos, L.S. Esposito, N. Karastathis, R. Lindner, L.E. Medina Medrano, Y. Papaphilippou, C.Parkes, D. Pellegrini, S. Redaelli, S. Roesler, F. Sanchez-Galan, P. Schwarz, E. Thomas, A. Tsinganis, D. Wollmann, G. Wilkinson
CERN, Geneva, Switzerland

Keywords: LHC, HL-LHC, HiLumi LHC, LHCb, https://indico.cern.ch/event/400665

- Expression of Interest, LHCC-2017-003
- Physics case, LHCC-2018-027
- Accelerator study, CERN-ACC-2018-038
- Framework TDR, CERN-LHCC-2021-012

Thank you for your attention