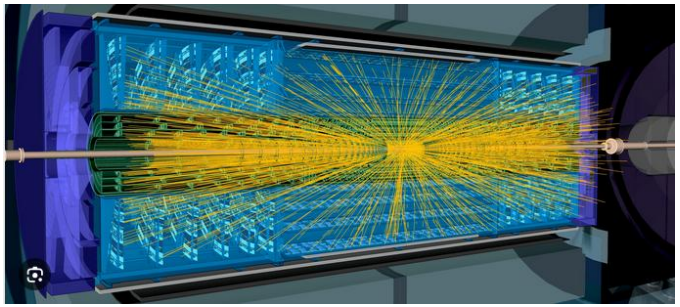
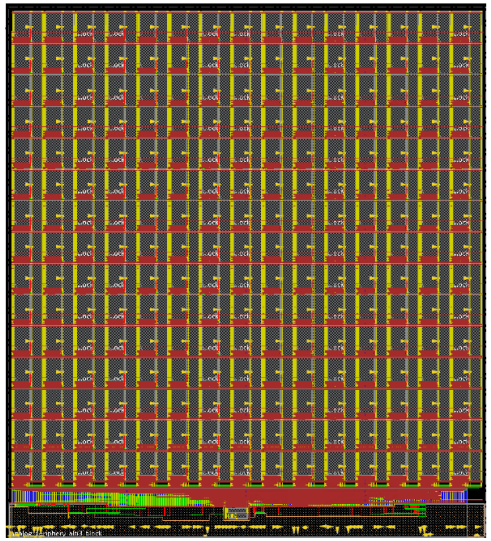
ALTIROC, LGAD readout ASIC for ATLAS HGTD

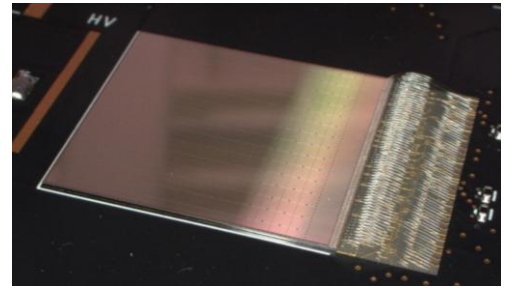


Nathalie Seguin-Moreau (OMEGA/CNRS/Ecole Polytechnique)

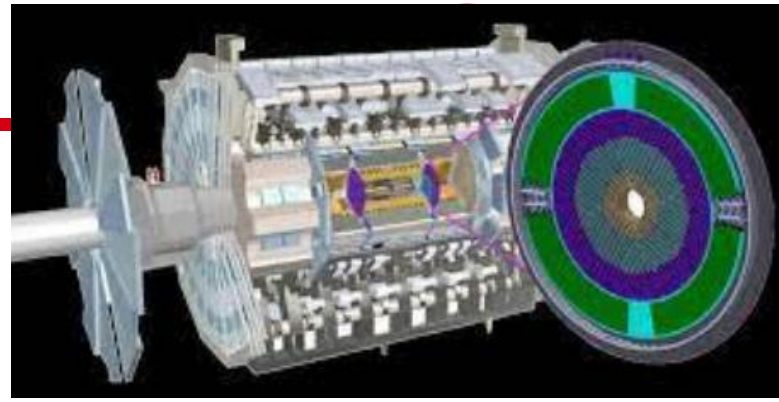
on behalf of ATLAS HGTD collaboration



Workshop on Future Tau-Charm Facilities FTCF2025– Huangshan, China – Nov 23 – 27, 2025



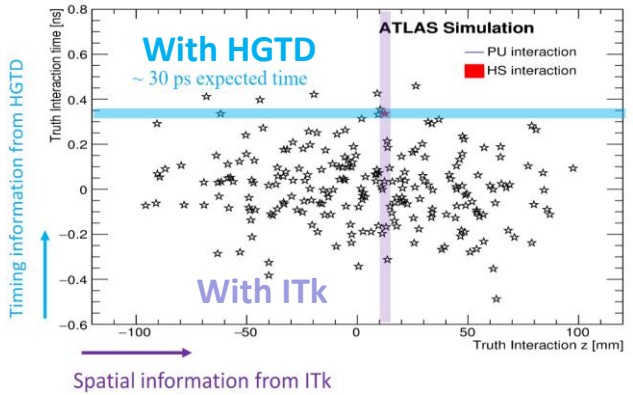
HGTD: new MIP timing detector in ATLAS (HL-LHC)



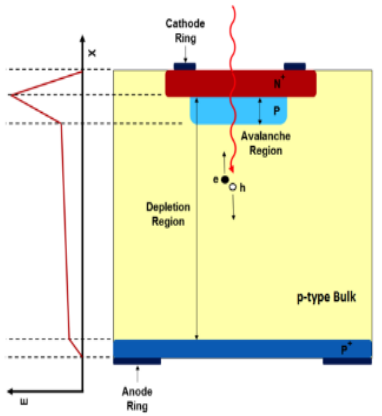
- With the high-luminosity environment of the HL-LHC comes increased pile-up making events discrimination more challenging.

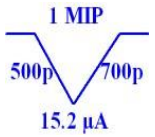
- High-precision timing measurements can be used to improve pile-up rejection when combined with Inner Tracker (ITk) position data.

- The **H**igh-**G**ranularity **T**iming **D**etector for ATLAS aims to provide :
  - Timing information with resolution of **30 ps/track (or 50 ps/hit) at the beginning, 50 ps/track (or 70 ps/hit) after 4000 /fb**
  - Luminosity information by reading hit counts for each bunch crossing



- HGTD detector
  - Located between barrel and End Cap calo, at 3.5 m from the interaction point
  - Sensor : LGAD matrix with 15 x 15 PADs (225 pads), sensor pad = 1.3 x 1.3 mm2 (thickness 50 µm) => Cd = 4 pF
  - LGAD modules on disks, two sensor layers/disk, two disks/side
  - Active radius from 120 mm (η = 4) to 640 mm (η =2.4)
  - Maximum fluence: 2.5 e^{15} neq/cm^2 and 2 MGy at the end of HL-LHC (4000/fb)
  - 8032 modules (one module= 2 ASICs bump bonded on 2 sensors), 3.6 M channels





LGAD Technology:

- N-in-P diode structure with extra p-type gain-layer
- Moderate gain: 10 – 20
- Extra gain layer: Fast **rise time** and larger **signal-to-noise** ratio

→ Excellent time resolution

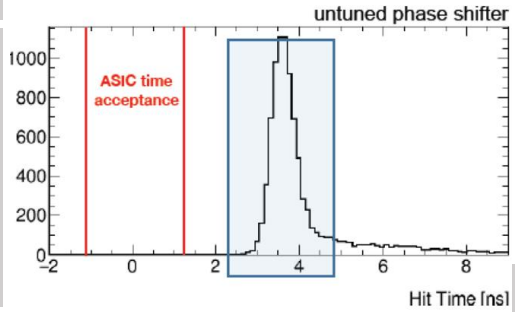
ALTIROC specification

sensor | read-out electronics

$$\sigma^2_{Total} = \sigma^2_{Landau} + \sigma^2_{Jitter} + \sigma^2_{Timewalk} + \sigma^2_{TDC} + \sigma^2_{Clock}$$

Charge dynamics : up to 100 fC
Noise : < 0.5 fC
Cross talk : < 2 % to guarantee single hit with 2 fC threshold

TOA :
Measurement window 2.5 ns
Jitter : 25 ps for Q = 10 fC
65 ps for Q = 4 fC
Conversion time < 25 ns (TDC LSB of 20 ps)



TOT :
For 100 fC, TOT < 20 ns

Landau MPV	4 fC	> 10 fC
Time Walk contribution rms (ps)	25	10
TOT resolution for VPA (ps)	120	120
TOT resolution for TZ (ps)	120	70

Conversion time < 25 ns
TDC LSB of 120 ps enough but TZ better use with 40 ps

40 MHz Clock of the TDC :
Jitter < 10 ps
ASIC global clock aligned with better than 100 ps
Clock skew between channels in ASIC : +/- 150 ps

Luminosity
Provide ASIC number of hits per bunch crossing on two time windows
Similar alignment as for the clock but skew relaxed to +/- 200 ps

Read out bandwidth and latency :
Should cope with 1 MHz with 12.8 µs and 0.8 MHz with 35 µs
ASIC bandwidth adjustable by slow control : 0.32, 0.64 or 1.28 Gb/s

Radiation

	TID [MGy]	NIEL [n_{eq}/cm^2]	SEE [h/cm^2]
ASIC Barrel	2	2.5×10^{15}	$1.\times10^{15}$
Safety Factors	1.5 simulation	1.5 sim x 1.3 monoenergetic beam	1.5 sim x 2 E cut +20 MeV

ASIC power dissipation < 1.2 W

Calibration injection :
Range 0 – 100 fC
Rise time : 0.5 - 1.5 ns

Front-End and electronics jitter (1)

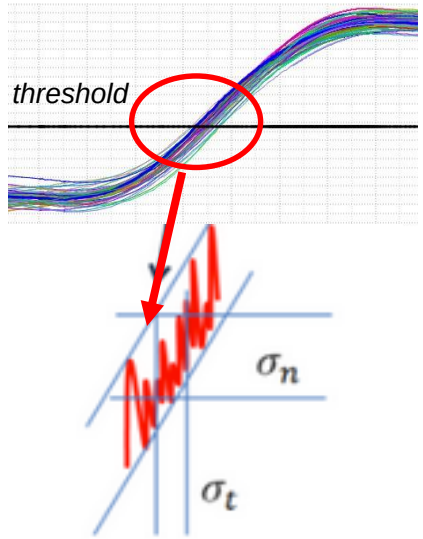
$$\sigma^2_{\text{det}} = \sigma^2_{\text{Landau}} + \sigma^2_{\text{elec}}$$

TW can be corrected with ToT measurement

$$\sigma^2_{elec} = \sigma^2_{jitter} + \sigma^2_{TDC} + \sigma^2_{clock} + \sigma^2_{time-walk}$$

- Jitter due to electronics noise:

$$\sigma_t^J = \frac{N}{\frac{dV}{dt}} = \frac{t_{rise}}{S/N}$$

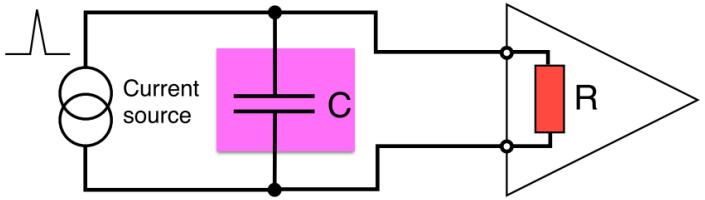


- dV/dt prop to BW, N prop to √ BW => jitter prop to 1/√BW

- Usual conclusion =

⇒ « the faster the amplifier the better the jitter ? »

⇒ « High speed preamps need to be low impedance (50 Ω or less) »



NB : tr = $t_{10\text{-}90\%}$ = 2.2 τ

f_{-3dB} = 1/2π τ = 0. 35 / $t_{10\text{-}90}$

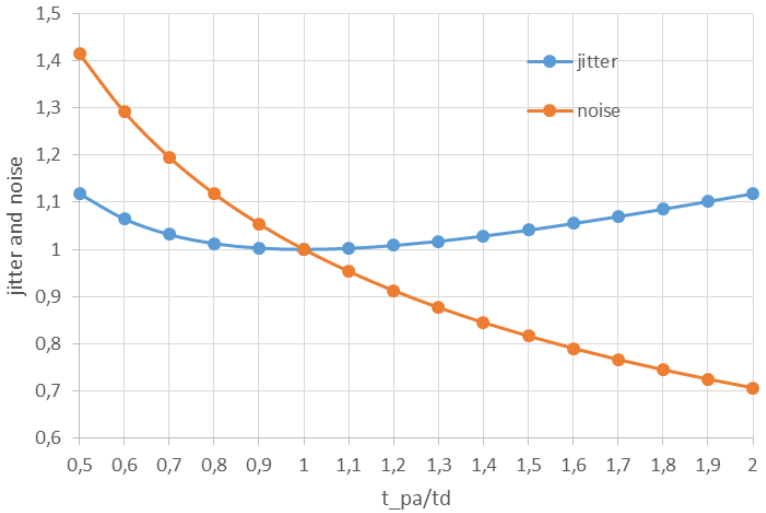
f_{-3dB} = 1 GHz equivalent to $t_{10\text{-}90\%}$ = 300 ps

Front-End and electronics jitter (2)

- Jitter is given by :

$$\sigma_t^J = \frac{N}{dV/dt} = \frac{e_n}{\sqrt{2t_{10-90\_PA}}} \frac{C_d\sqrt{t_{10-90\_PA}^2 + t_d^2}}{Q_{in}} = \frac{e_n C_d}{Q_{in}} \sqrt{\frac{t_{10-90\_PA}^2 + t_d^2}{2t_{10-90\_PA}}}$$

jitter and noise as a function of preamp risetime



- Optimum value: $t_{10\text{-}90\_PA} = t_d$ (current duration)

$$\sigma_t^J = \frac{e_n C_d}{Q_{in}} \sqrt{t_d}$$

Cd: detector capacitance
$t_{10\_10\_PA}$: rise time of the PA
t_d = drift time of the detector ~ 500 ps
e_n preamp noise density

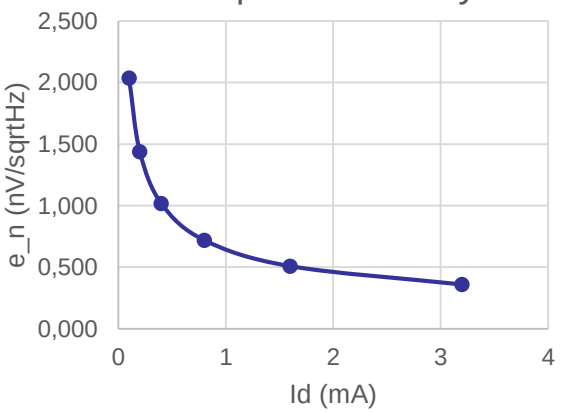
Electronics jitter dominated by sensor
Electronics only gives the spectral density of the input transistor e_n

More details in https://iopscience.iop.org/article/10.1088/1748-0221/15/07/P07007/pdf

- Electronics noise e_n given by the input transistor transconductance g_m:

$$e_n = \sqrt{\frac{2kT}{g_m}} \approx \frac{2kT}{\sqrt{qI_D}}$$

noise spectral density



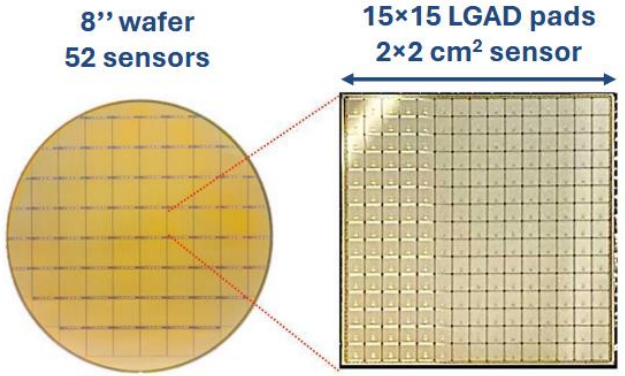
- Expectation : 10 ps for Q=10fC @ C_d=2 pF e_n=2 nV/√Hz t_d=0.5 ns

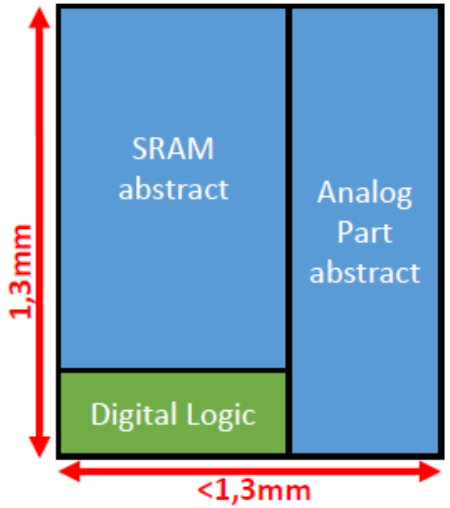
- Altiroc preamplifier = 1 GHz Transimpedance amplifier with variable Id and internal variable capacitor to have the possibility to slow it down

ALTIROC main challenges

Altiroc looks “similar “ to pixels ASIC but

- **Minimum Charge Qmin/ Detector capacitance Cd and 1 GHz bandwidth: Floorplan is crucial**
  - **Altiroc: Qmin/Cd ~ 500 µV** with **Cd ~4 pF** (1300 x 1300 µm2) and Vth min= 2 fC
    instead of usual Qmin/C > 2 mV for pixel ASIC with Cd ~ 50 fF (50 x 50 µm^2) and Vth min = 0.1 – 0.2 fC
- **Preamp BW**
  - Altiroc: **1 GHz**
  - Pixel chips: ~ 20 MHz
- **Pixel ASIC with timing measurement (TDC)**
  - Altiroc TDC bin: **20 ps** and 130 nm technology
  - Existing pixels chip with timing measurement TDC bin : **200 ps** and 65 nm technology
- **Power dissipation and technology**
  - Altiroc: **300 mW/cm2** + techno CMOS **130 nm**
  - Pixel chips : 600 mW to 1 W/cm2 + techno CMOS 65 nm
- **Integration issues and technology**
  - ALTIROC SRAM with a latency of 38.4 µs + techno CMOS 130 nm



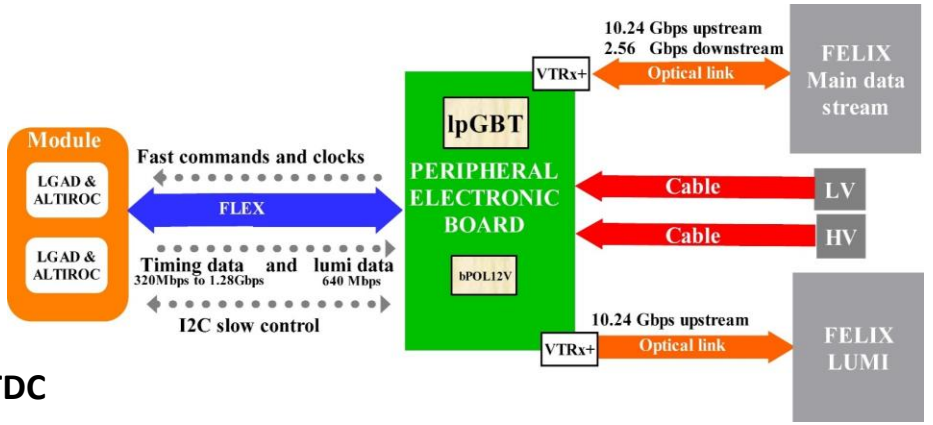


Altiroc pixel

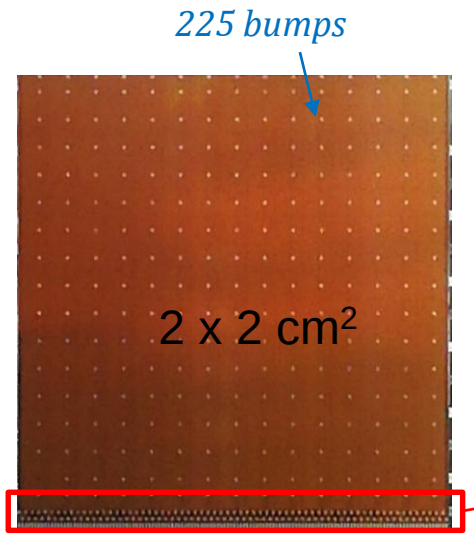
ALTIROC main challenges

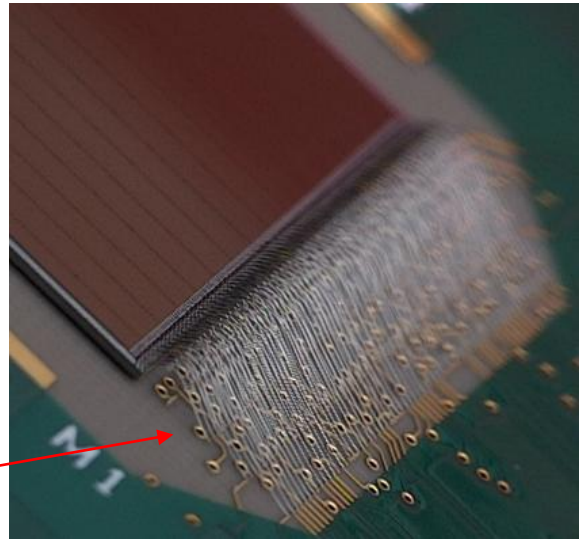
- A module is made of two ALTIROC ASICs bump bonded onto two 15x15 LGAD sensors, each sensor pad = 1.3 x 1.3 mm2 (active thickness 50 µm)

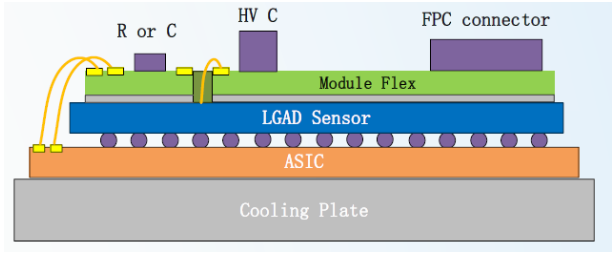
- **Voltage drops**:
  - Chip size 2 x 2 cm^2
  - Bumps for input signals + Wire Bonding I/O PADs for all other signals and power supplies
  - ➔ **Power supplies only from one side, voltage drop control is a key issue in particular for the TDC**

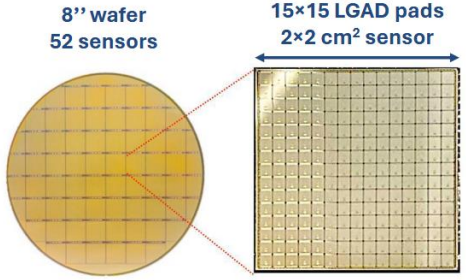


*Slide in backup + more details in **TWEPP2024 talk**: https://indico.cern.ch/event/1381495/contributions/5988493/attachments/2869323/5163702/TWEPP2024_Soulier.pdf*

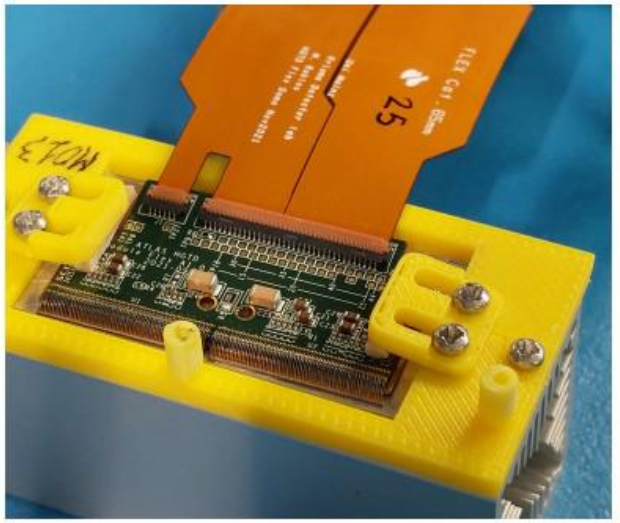




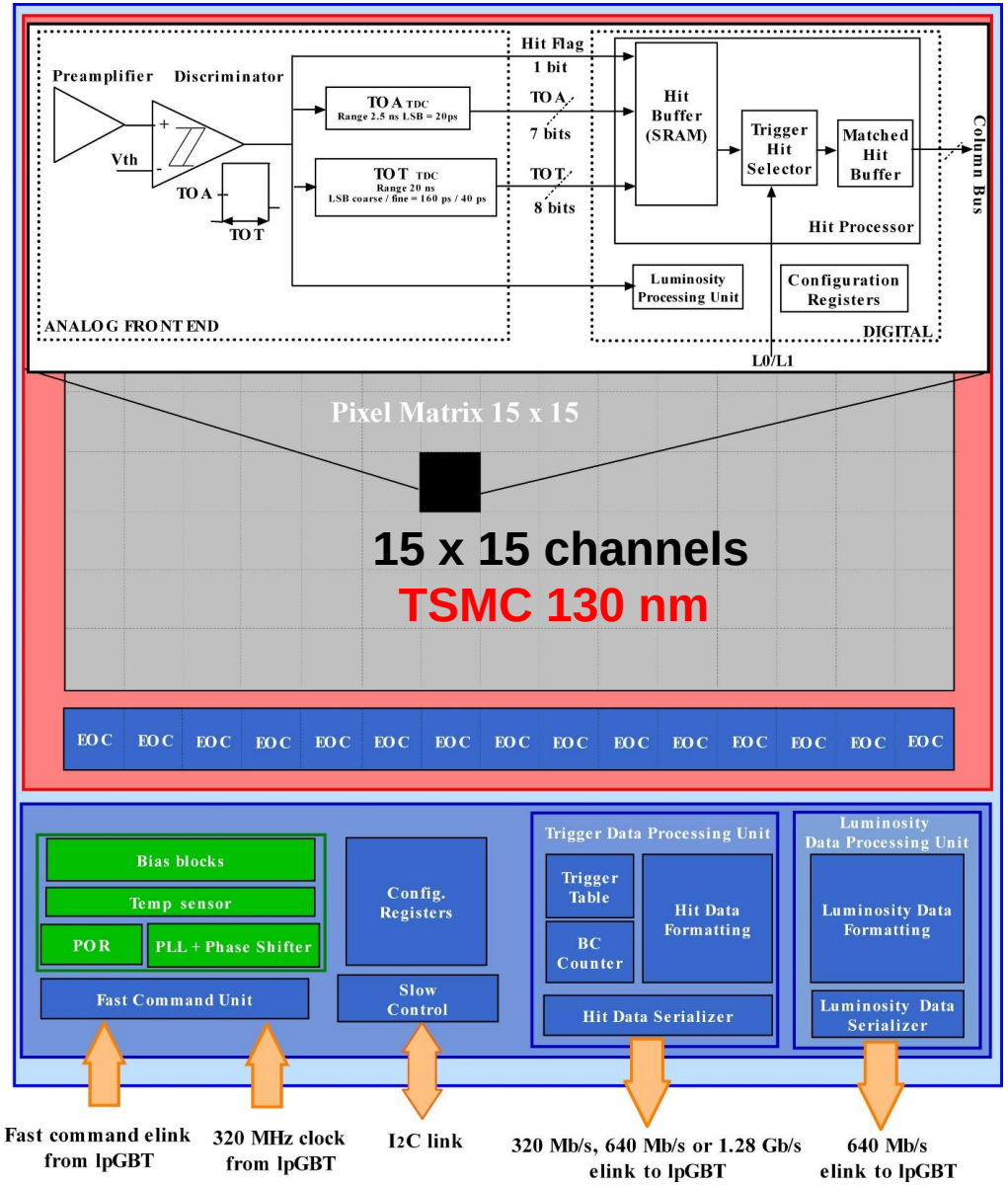




Module with two ALTIROC bump bonded onto two sensors



ALTIROC architecture



Matrix

EOC

Periphery

Pixel

$$\sigma_{jitter} = \frac{N}{dV/dt} = \frac{e_n C_d}{Q_{in}} \sqrt{t_d}$$

- **Analog Front End pixel:Analog FE performance crucial**
  - **1 GHz preamplifier** followed by a high-speed **discriminator**.
  - **Two TDC** (Time to Digital Converter) to provide Time of Arrival (TOA) + Time Over Threshold (TOT) measurement
    - TOA TDC: bin of 20 ps (7 bits), range of 2.5 ns, to be centered on the bunch crossing
    - TOT TDC: coarse/fine bin 160 ps / 40 ps (8 bits), range of 20 ns
- **Digital part of the pixel**
  - One SRAM (Hit buffer) with a latency of 38.4 µs
  - Zero suppress logic (Trigger Hit Selector and Matched Hit Buffer)
  - Luminosity processing unit

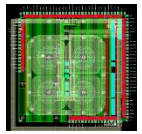
EOC: readout of columns + data transfer to trigger data and luminosity data processing units

Periphery

- **Analog periphery**: Bias, DAC for threshold, temp sensor, PLL, Phase Shifter, clocks receivers, data transmitters (up to 1.28 Gb/s)
- **Digital periphery:**
  - 320 Mbit/s fast commands decoder
  - Reads time data from pixel matrix and packs data into frames before serializing them
  - Timing data transmission: encoded (8b10b) and serialized at different rates (320 Mb/s, 640 Mb/s, 1.28 Gb/s) depending on radial position of the ASIC
  - Luminosity data: encoded (6b8b) and serialized at 640 Mb/s
  - Slow Control: I2C link, 1024 * 8-bit registers (Triplication + auto correction)

ATLAS HGTD Timing detector: ALTIROC (TSMC 130n) history

2016



Altiroc0
2 x 2 mm2
2 x 2 pixels
PA + discri

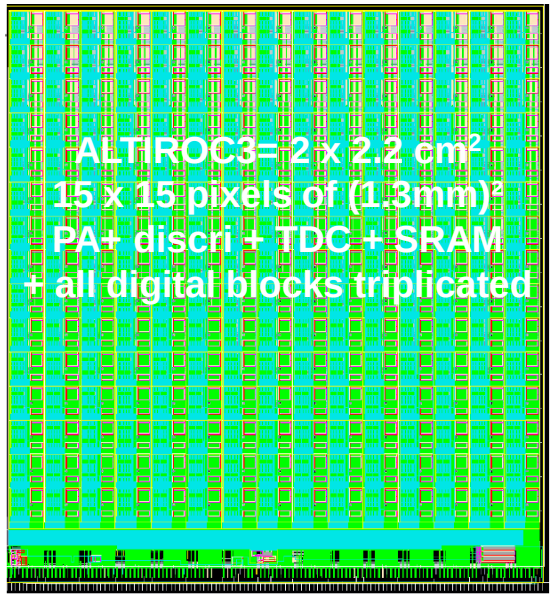
2017-2018

Altiroc0 and 1:
No digital,
To validate the FE part at system level (= ASIC bump-bonded onto a sensor)

Engineering run 2021

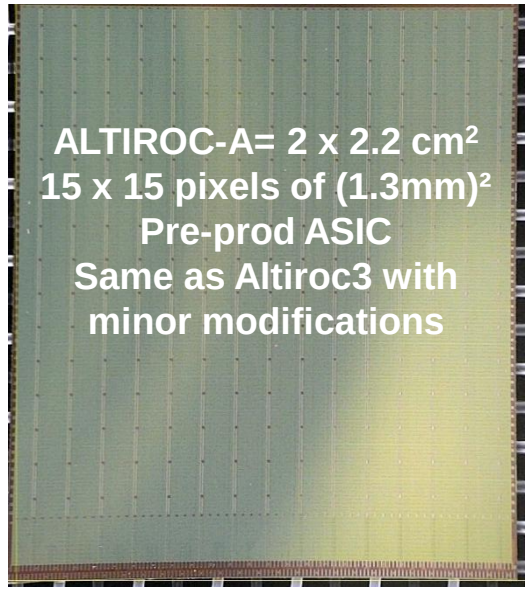
ALTIROC2:
First full size chip with 15 x 15 channels – 2 x 2 cm2
To demonstrate the functionality/performance of the ASIC (time resolution + luminosity counting) alone and bump-bonded onto a sensor
But NOT to be fully radiation hard (against SEE)

Eng run June 2022



ALTIROC3:
Last full chip prototype before pre-production
Full Digital-On-Top
Same as Altiroc2 but fully triplicated
New pinout (TDC IR drops)

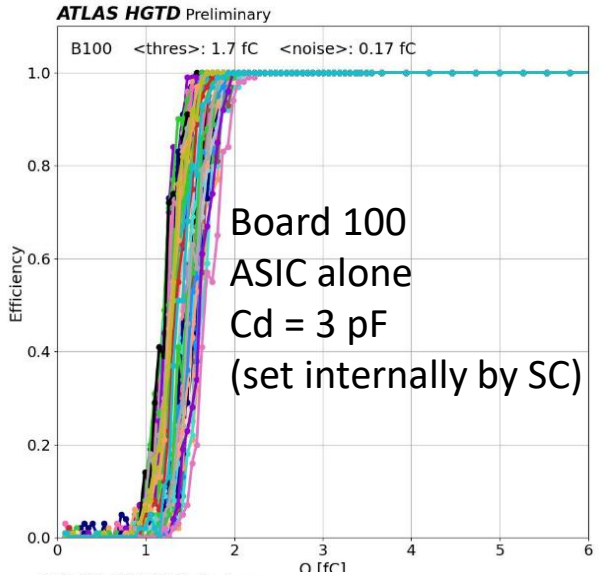
Eng run March 2024

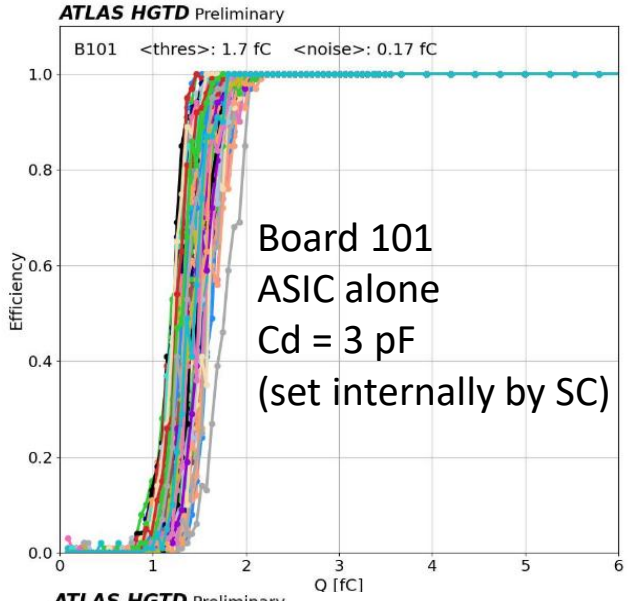


ALTIROCA:
pre-production ASIC
Same masks to be used for the production
Same as Altiroc3 with minor modifications

ALTIROC-A (pre-production ASIC) PERFORMANCE: Efficiency and Qmin

MIP ~ 10 - 15 fC at the beginning of HGTD
MIP ~ 5 fC after full irradiation of the sensors

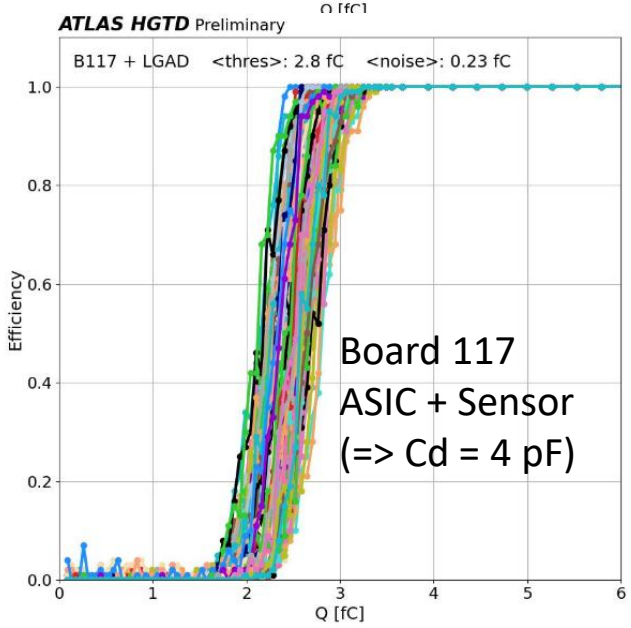


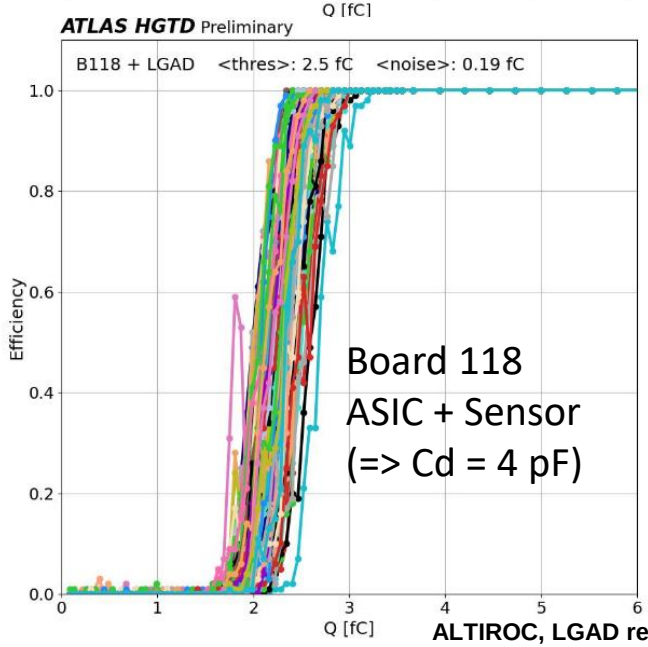


Measurements done with testboards

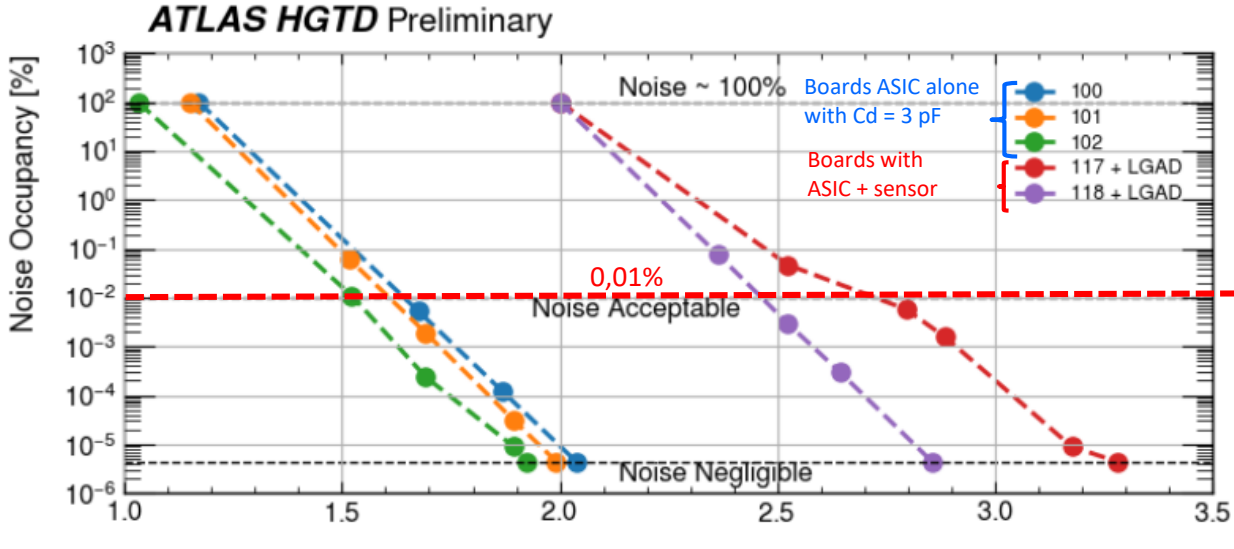
–40 °C in clean room

Charge injection using the ASIC internal calibration system that mimics the LGAD signal



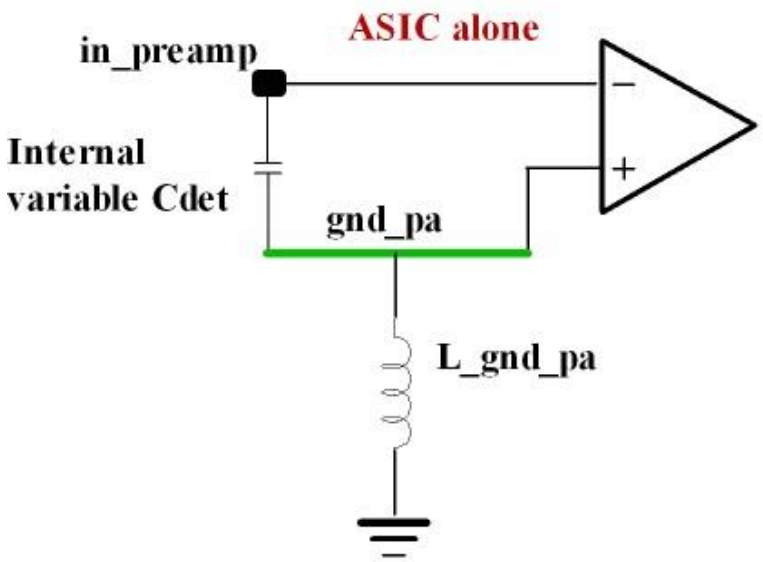


1 million events with Qinj=0 sent to 225 channels and count the number of registered hits versus threshold



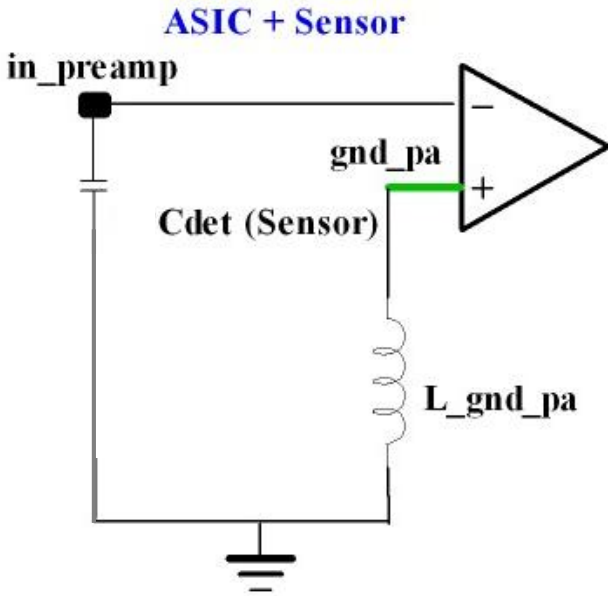
Main challenges: Measurements at system level and digital noise

One channel

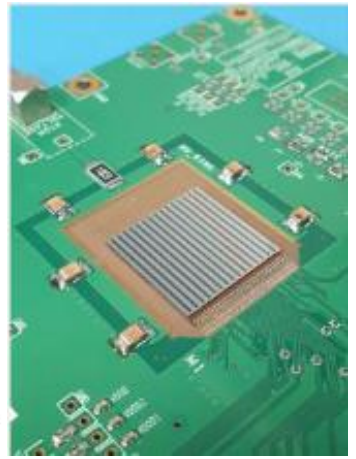


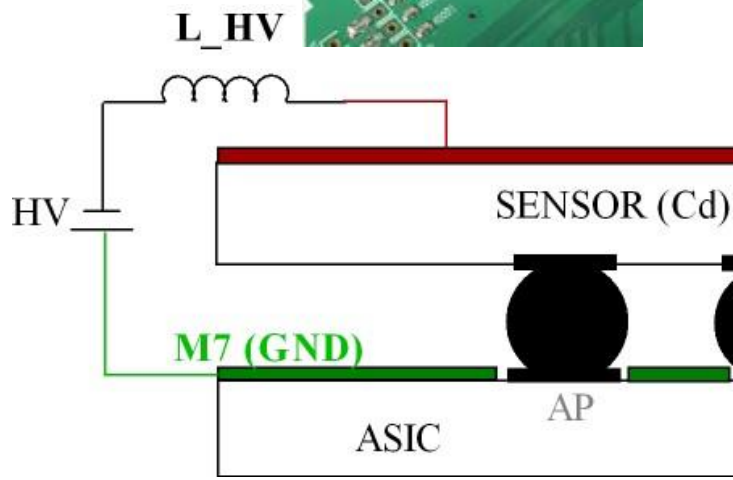
Noise on analog gnd (gnd_pa) amplified x1
"common mode"

ASIC alone = favourable situation



Noise on gnd_pa amplified x20
"differential mode"



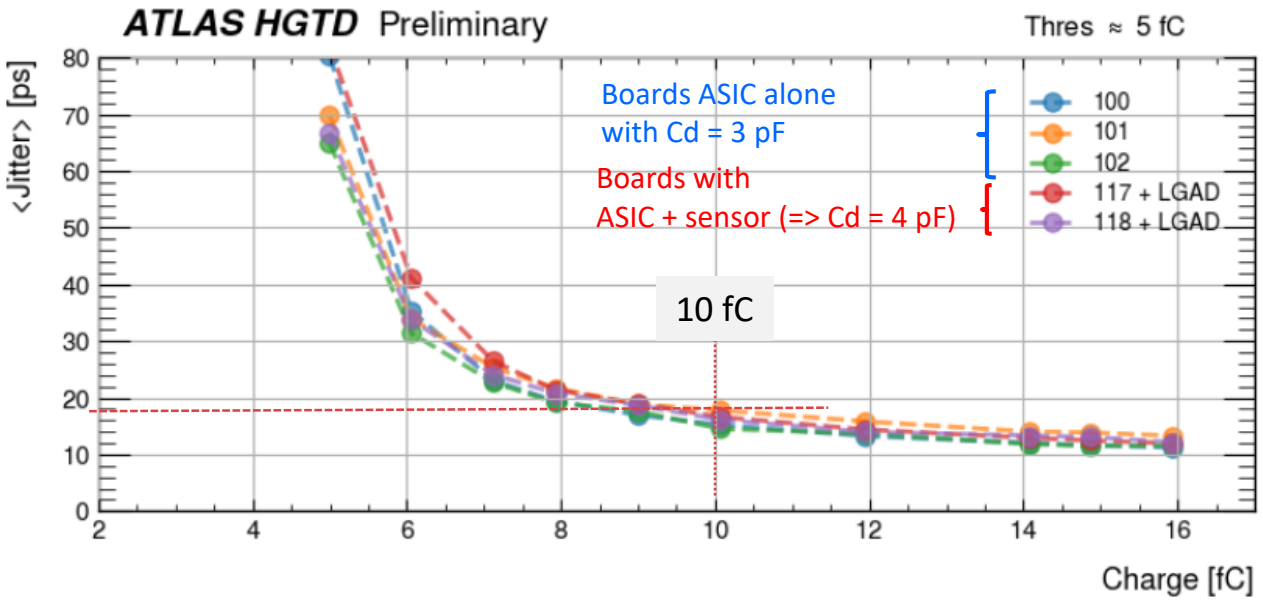


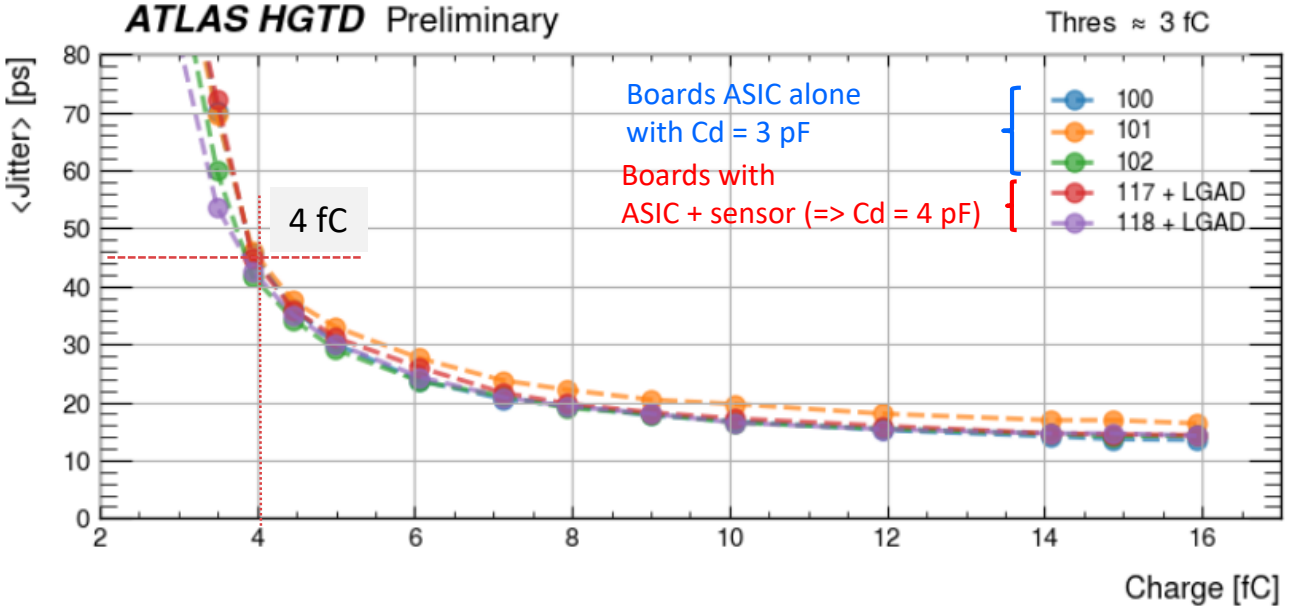
Digital noise injected on the preamplifier ground gets amplified only when the impedance between the detector capacitance and the non-inverting preamplifier input is not zero i.e when the sensor is connected (***Twepp2022 talk***: *https://indico.cern.ch/event/1127562/contributions/4904499/attachments/2511666/4317317/ALTIROC2_ATLAS_HGTD.pdf*)

⇒ **Impacts Qmin**

⇒ **Floorplan is crucial**: Ultra Low impedance (50 mΩ) for the ground of the preamp to minimize Qmin and proper decouplings at system level have also proved to be crucial to reduce Qmin

ALTIROC-A (pre-production ASIC) PERFORMANCE: Jitter versus charge

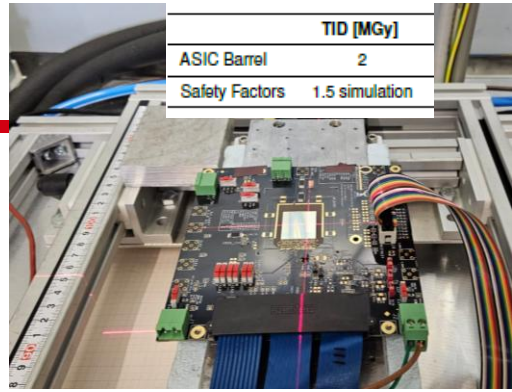




Specification:
Jitter : 25 ps for Q = 10 fC
65 ps for Q = 4 fC
Conversion time < 25 ns (TDC LSB of 20 ps)

MIP ~ 10 - 15 fC at the beginning of HGTD
MIP ~ 5 fC after full irradiation of the sensors

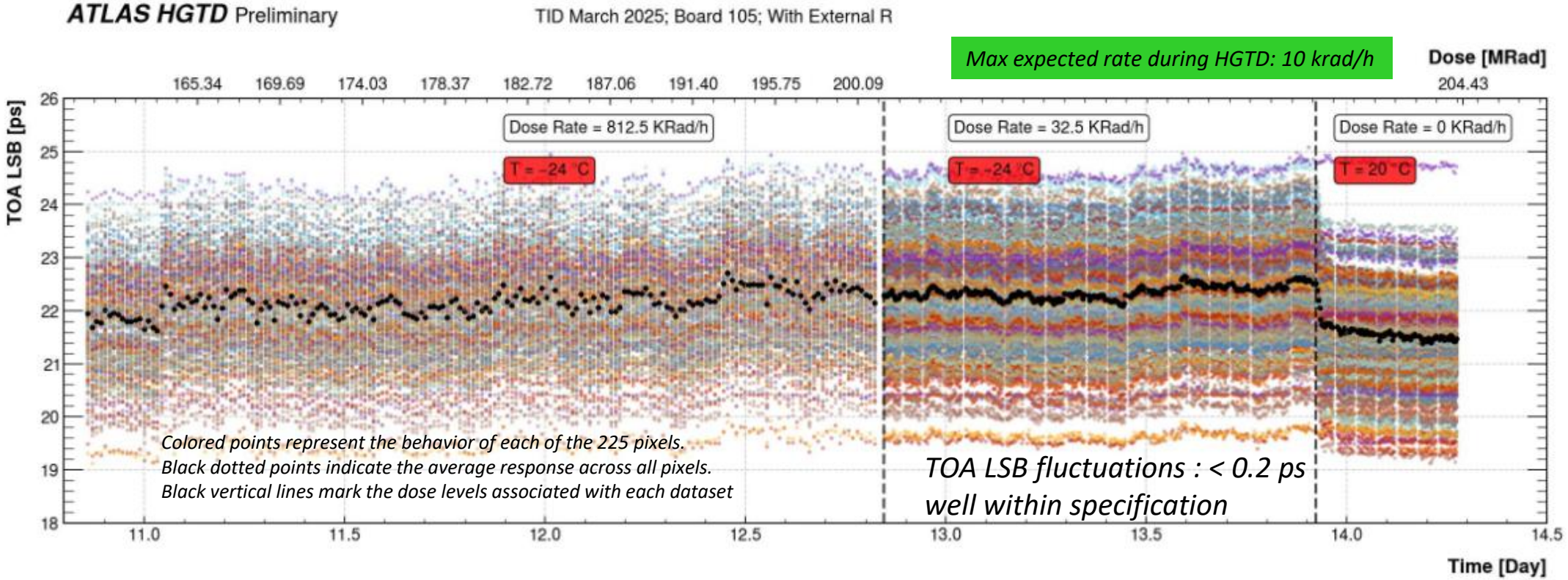
ALTIROC-A (pre-production ASIC) PERFORMANCE: TID irradiation



- TID conditions
  - Use Obelix facility at CERN, 10 keV X-rays (Dec 2024, Jan 2025, March 2025) and ATLAS pixel facility (Feb 2025)
  - Temp -20°C at Obelix, room temp at ATLAS pixel facility
  - Up to **200 Mrad** (= 2 MGy) with beam at the max distance to irradiate all the chip => max dose rate ~1.2 Mrad/h, min dose ~ 16 krad/h

- Continuous measurements during irradiation:
  - DC voltages and power consumptions, Vth & Vthc scan, Charge scans (Qmin), noise, TOA and TOT LSB, Jitter measurements for Qinj = 4 fC and 10 fC

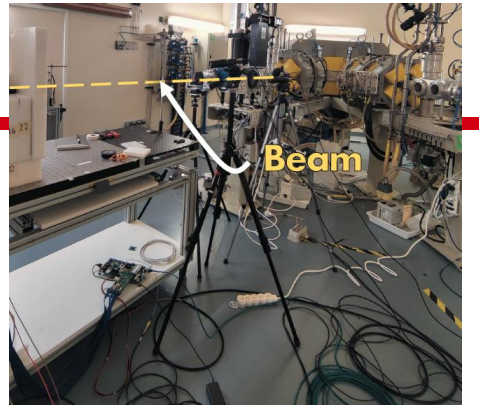
- No variations observed for all the measurements
  - Except for the TOA TDC bin which showed unexpected variations under irradiation: the larger the rate the larger the variations
    - Issue not due to TDC itself but to Control Voltages generated in the periphery for TDC delay lines
    - Issue could be solved at system level and TOA LSB variation under irradiation are now < 0.2 ps, so well within the specifications

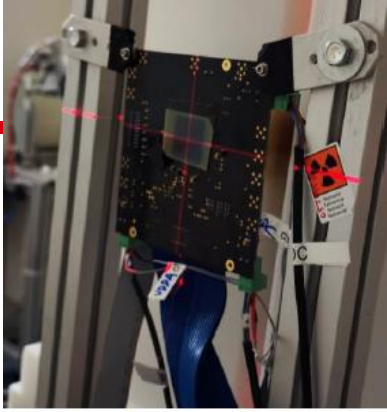


ALTIROC-A (pre-production ASIC) SEE tests summary

- Arronax Cyclotron (Nantes) 68 MeV proton beam
  - Expected flux at the HL-LHC ~ 8.5×10^7 p.cm^{-2}.s^{-1} with SF=2,5
  - Total fluence: ~ 5 10 ^{14} p.cm^{-2} in 5 hours

	Flux $[p.\,cm^{-2}.\,s^{-1}] \times 10^{10}$
$i1$	0.57 ($\sim 250 \times fHL\text{-}LHC$)
$i2$	1.3 ($\sim 580 \times fHL\text{-}LHC$)
$i3$	3.4 ($\sim 1500 \times fHL\text{-}LHC$)
$i4$	6.7 ($\sim 3000 \times fHL\text{-}LHC$)
$i5$	1.5 ($\sim 670 \times fHL\text{-}LHC$)



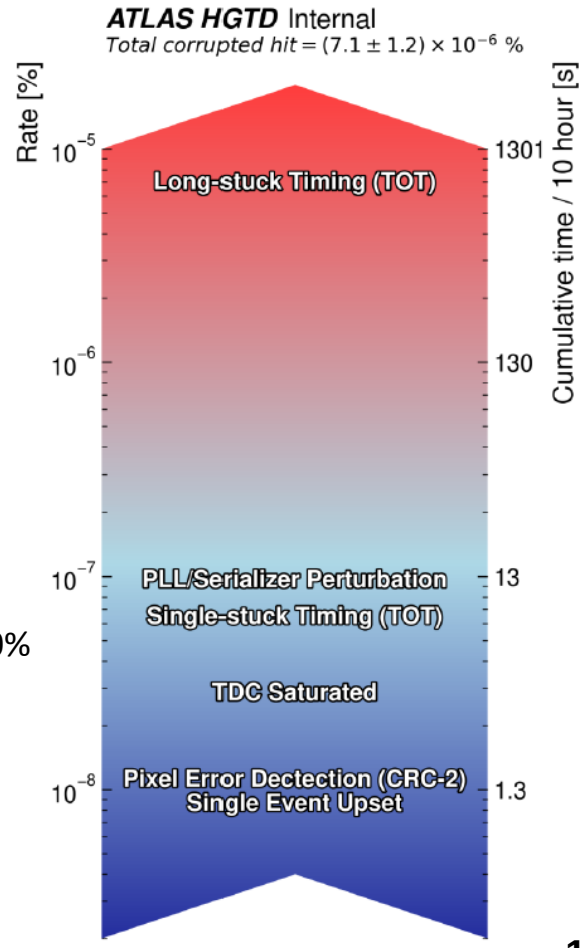


- Data path not triplicated
- Digital blocks for control logic (counters, FSM ..) + configuration registers + corresponding clocks are triplicated

- Configuration registers (all triplicated):
  - Written once at start then read every minute ➔ No errors in configuration detected

- Continuous data taking :
  - No global reset sent ➔ Readout is stable
  - No resynchronization ➔ Output links are stable

- Plot shows the estimated rates of erroneous pixel frames (= hits) and cumulative error duration in seconds, assuming 10% occupancy, a 10-hour fill, and 40 MHz collision rate across the entire HGTD (3.6 millions of pixels):
  - **Negligible corruption rate** : 7 x 10^{-6} % of the 1,4 x 10^{12} hits corrupted per 10-hour fill



ALTIROCA PERFORMANCE: LASER

- Infrared laser (λ = 1064 nm, sub-mm focus) to determine jitter
- Photons deposit their energy in the same depth in the sensor

→ Landau and Timewalk contributions negligible

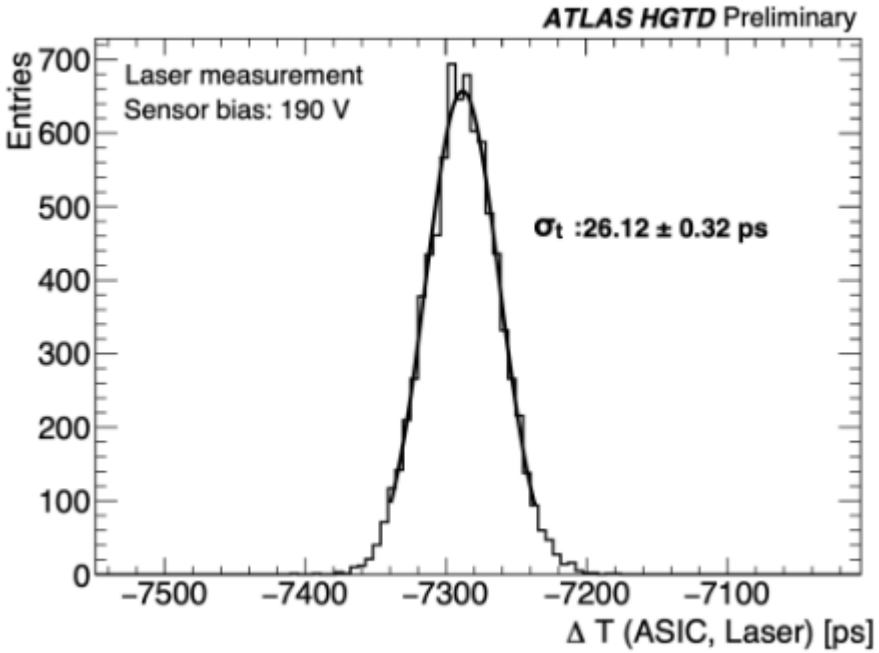
sensor | read-out electronics

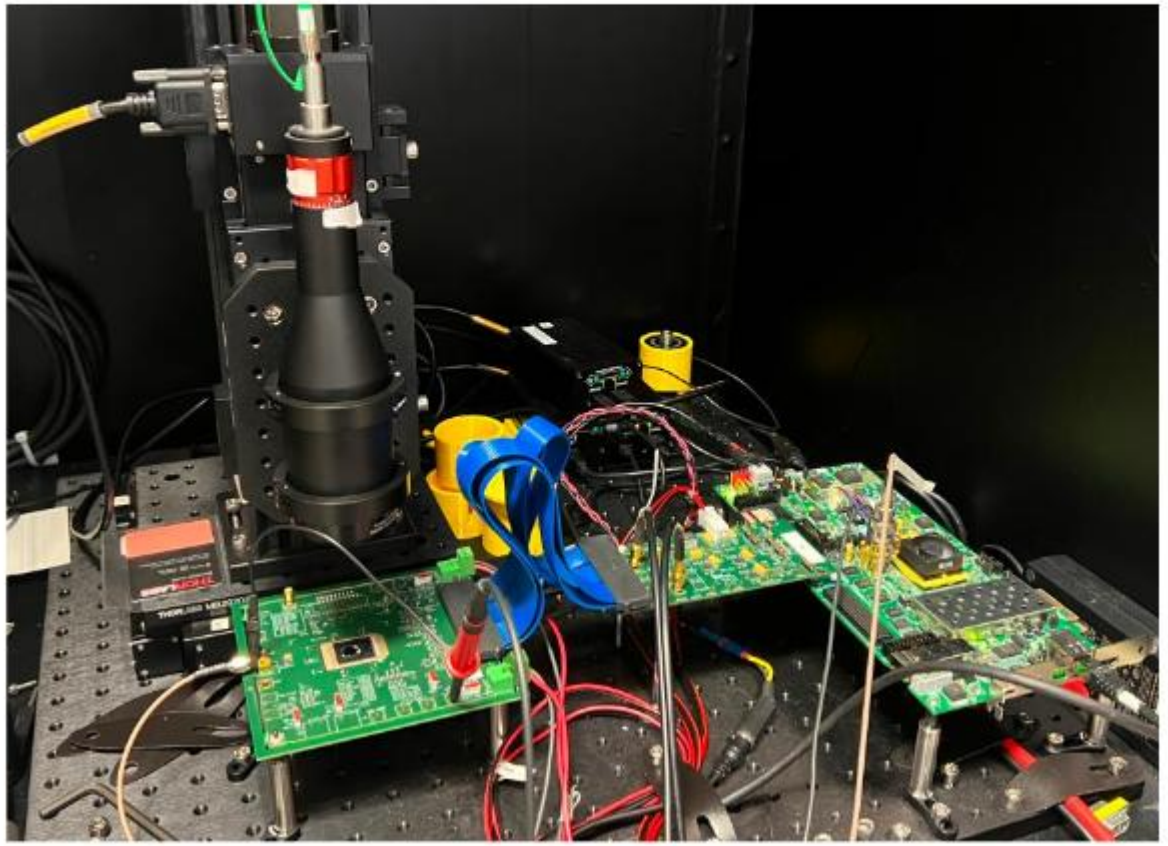
$$\sigma^2_{total} = \sigma^2_{Landau} + \sigma^2_{Timewalk} + \sigma^2_{Jitter} + \sigma^2_{TDC} + \sigma^2_{Clock}$$

- Time reference: precise signal (3 ps jitter) from laser driver
- Jitter measured to be ~ 23 ps

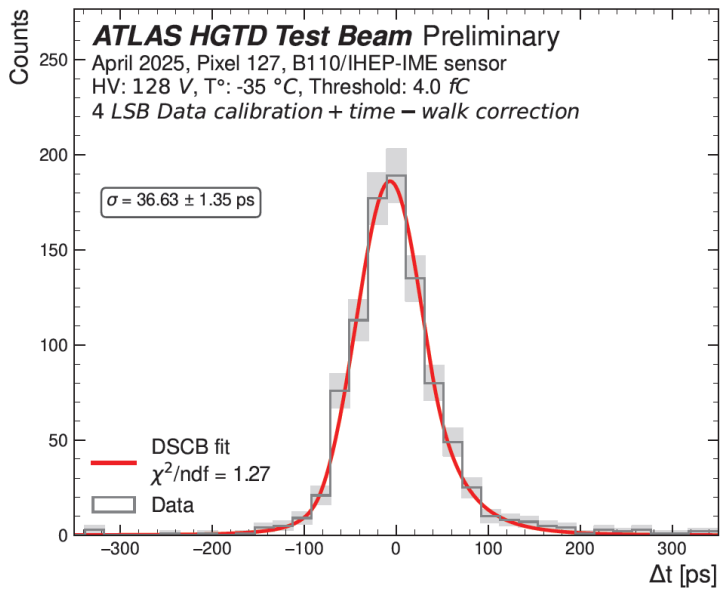
→ Correction for TDC (10 ps) and clock (8 ps) contributions

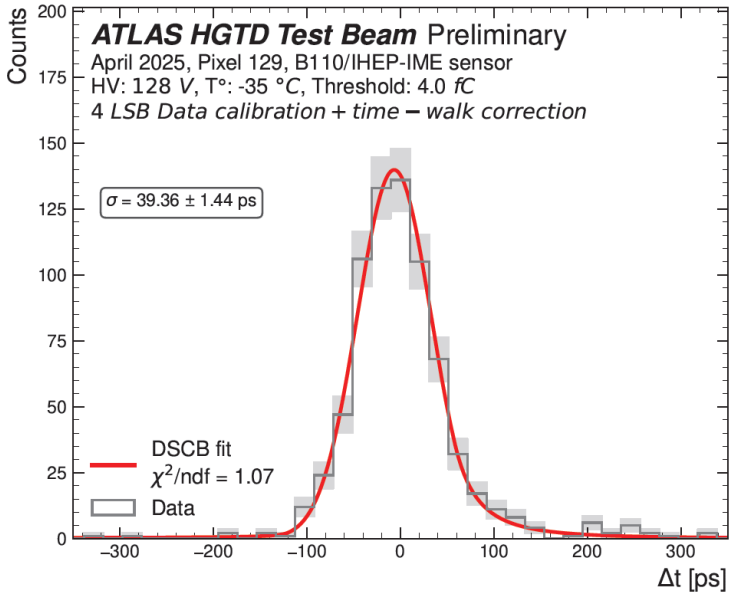
→ Consistent with ASIC test-bench measurements

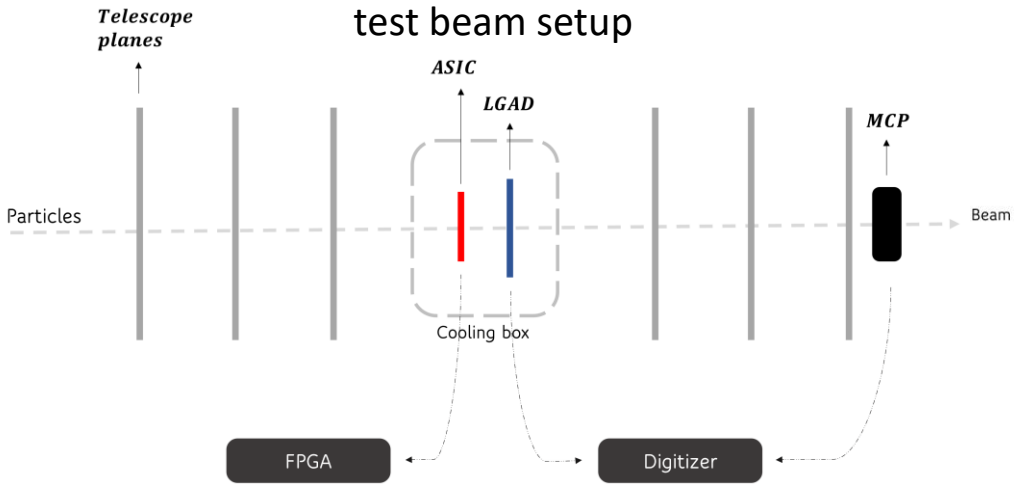


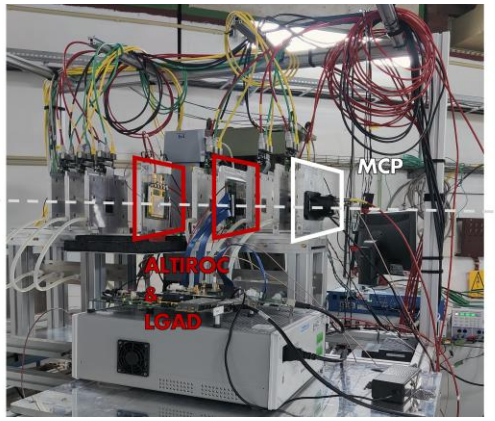


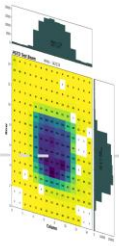
ALTIROC-A PERFORMANCE: TESTBEAM











The readout system is performed using a FPGA for the ALTIROC and the digitizer for the LGAD and MCP (Timing reference)

$$\Delta t = TOA \times LSB - (t_{Clock} - t_{MCP})$$

Time resolution requirement:
50 ps/hit at the beginning of HGTD
70 ps/hit after 4000 /fb

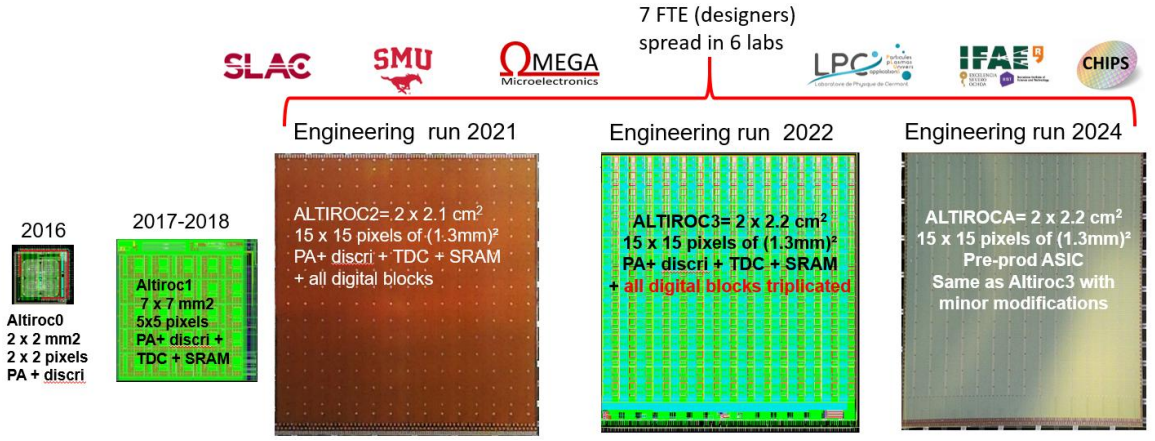
ALTIROC-A hybrid boards achieve time resolution of ~ 40 ps in average at cold

- Electronics jitter ~ 23 ps with a Laser
- TOA LSB extracted from test-beam data
- TOA LSB from calibration different from the one obtained with test-beam data, additional calibration of the TDC in situ at LHC under study

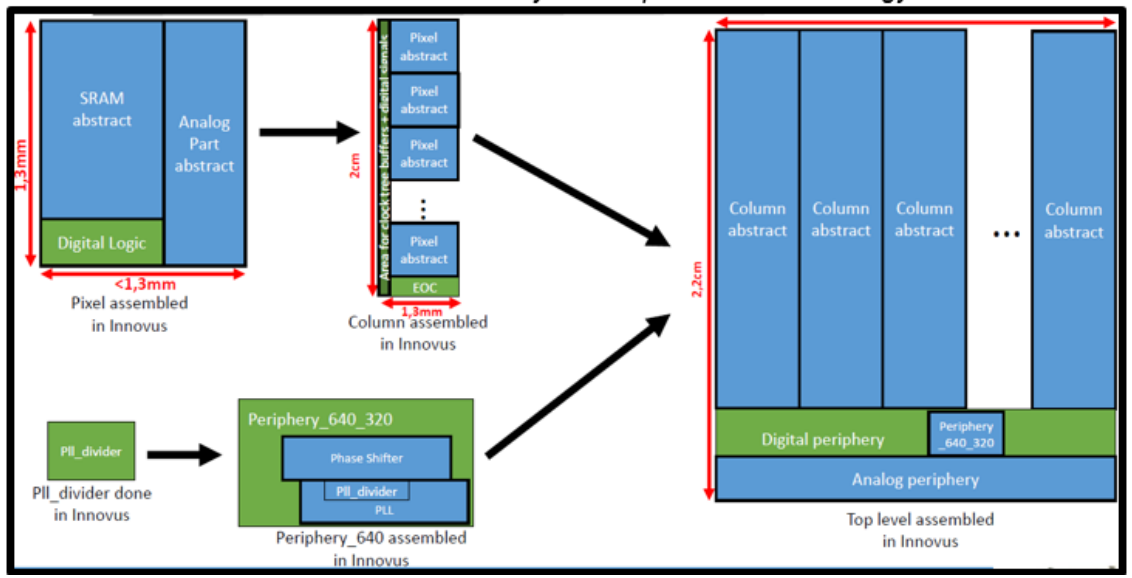
SUMMARY & LESSONS LEARNT: PROTOTYPES AND DESIGN METHODOLOGY ARE CRUCIAL

- **ALTIROC-A (pre-production chip) fulfills the requirements => production of 225 wafers launched this summer**

- **Very challenging ASIC that results of ten years of development, both in design and characterization**
  - Four earlier prototypes—the first two focused on thorough characterization of the Front-End with new LGAD detectors, and the next iterations targeting optimization of the digital architecture
  - ALTIROC2 (2020) was the first 225 channels full matrix LGAD readout chip with 1 GHz preamplifier with 4 pF detector capacitance = new territory in HEP
  - **Joint optimization sensor + readout electronics**
  - 7 FTE spread in 6 labs and stringent schedule and deadlines
  - Use of both DOT and AOT approaches
    - AOT: Analog 30 % of the chip, analog performance and floorplan crucial to guarantee analog performance at system level
    - DOT: Digital 70 % of the chip + 5 clock domains
      - Assembly done Full Digital on Top + UVM verification
      - Top level assembled with INNOVUS
      - Verilog models and lib files to be done for all analog/mixed blocks
      - Analog periphery treated as a macro block



Altiroc3 and A: Physical Implementation strategy



*More details about ALTIROC verification environment in this **TWEPP2023 talk**:*
https://indico.cern.ch/event/1255624/contributions/5443840/attachments/2725854/4737406/Verification%20Environment%20for%20ALTIROC%20ASIC%20of%20the%20ATLAS%20High%20Granularity%20Timing%20Detector%20-%20Simone.pdf

SUMMARY & LESSONS LEARNT: NEXT STEPS

Extensive measurements done on test bench, at wafer level, under irradiations, test beams are crucial

- The ALTIROC experience — along with other complex chips designed for HL-LHC upgrades —clearly highlights the **crucial role of repeated, independent measurements for fully validating complex designs**

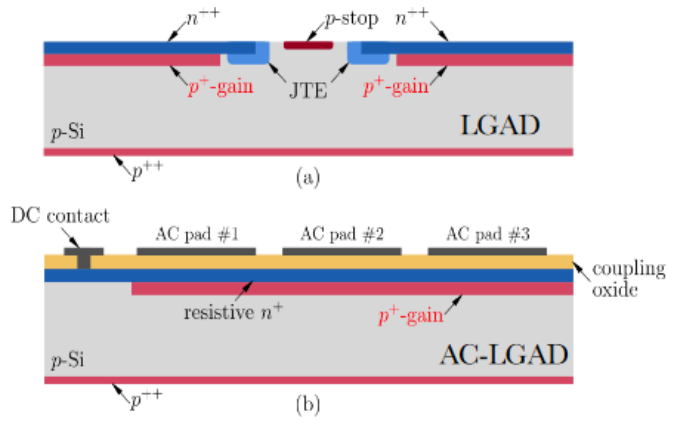
Key Learnings and Achievements

- Extensive experience gained in both human and technical aspects to successfully developed a chip combining **high analog performance challenges** and significant **digital complexity** with multiple clock domains

Looking Ahead

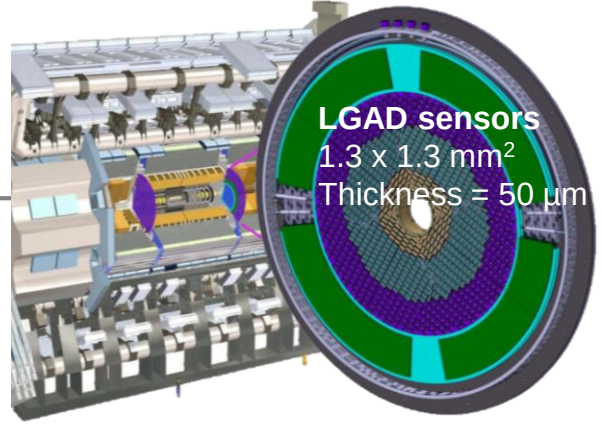
- Acquired expertise enables us to tackle next-generation timing chips in view of FCC, EIC with additional challenges such as streaming readout and power consumption reduced by a factor of 10

- **Part of the ALTIROC team is now working on AC-LGAD** detectors for PID detectors
  - Highly promising technology
  - Offers excellent **timing resolution** (30 ps) and very good **spatial resolution** (30 µm using barycentering)



BACKUP SLIDES

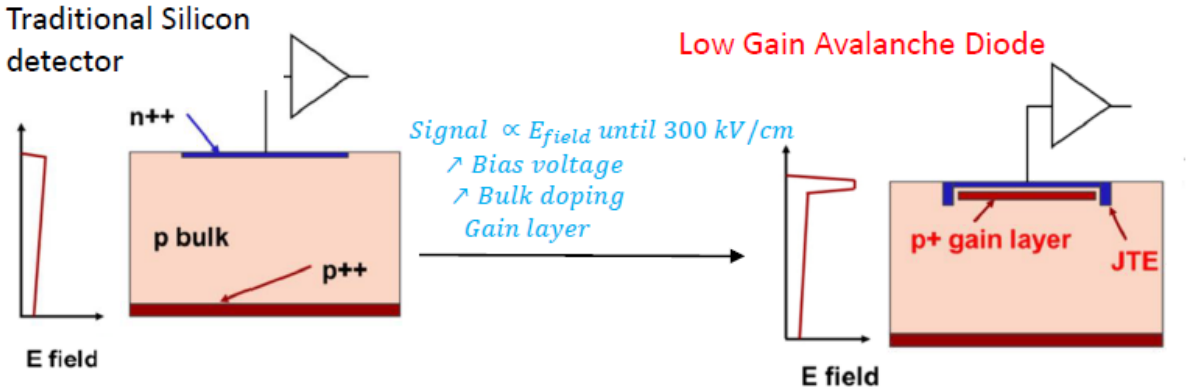
HGTD sensors: Low Gain Avalanche Diodes

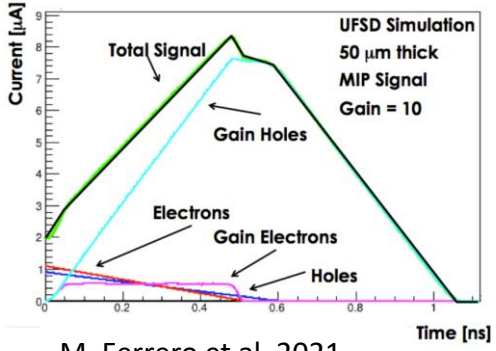


Time resolution <50 ps / MIP / sensor: beyond standard HEP silicon devices

⇒ Low Gain Avalanche Detector (LGAD): n on p sensor with p-type multiplication layer

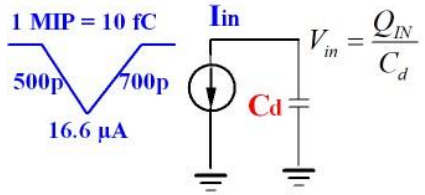
⇒ Low gain (G~10): improve signal slope

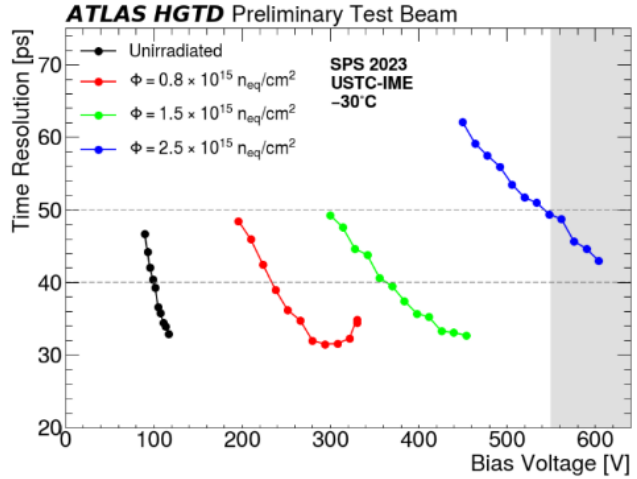




M. Ferrero et al. 2021

LGAD current





Performance with discrete electronics

$$\sigma^2_{\text{det}} = \sigma^2_{\text{Landau}} + \sigma^2_{\text{elec}}$$

$$\sigma^2_{elec} = \sigma^2_{jitter} + \sigma^2_{TDC} + \sigma^2_{clock} + \sigma^2_{time-walk}$$

Can be corrected with ToT measurement

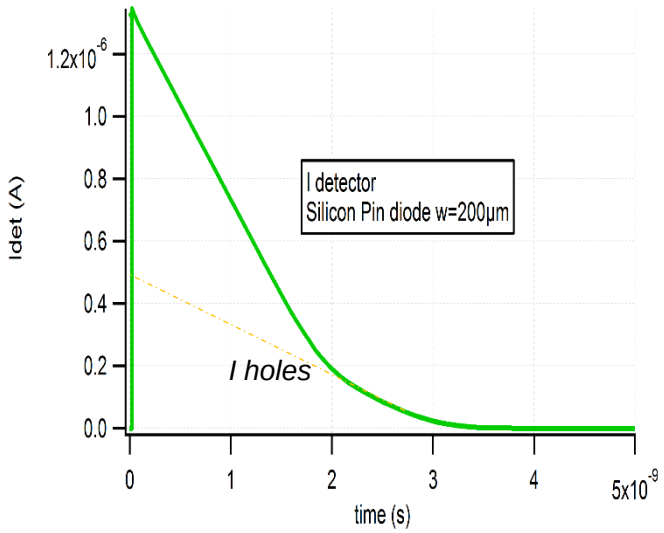
Signal : detector current

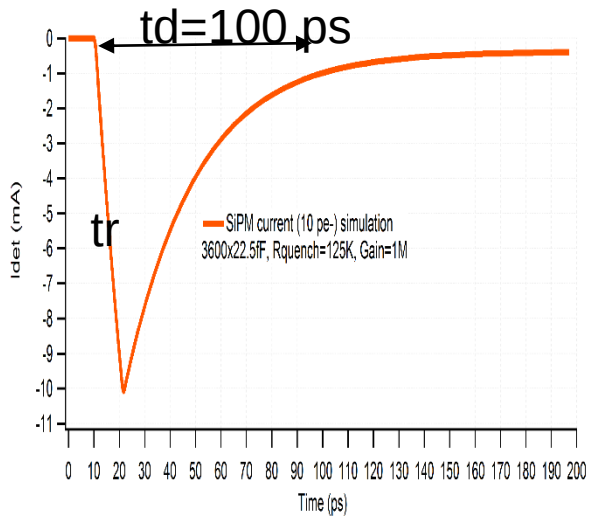
© *sensor people "the beautiful risetime of the detector is spoilt by the electronics"*

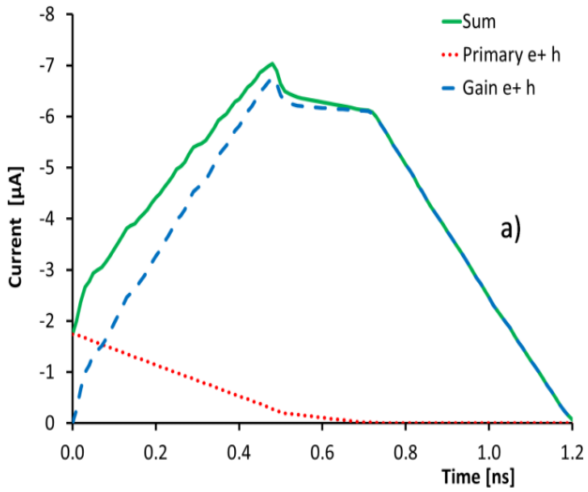
- PN diode w =200µm
- Very short rise time : tr~10ps
- Relatively long «drift time» : td~2ns

- SiPM detector (10pe-)
- very short rise time : tr~10 ps
- Short duration : td~100ps

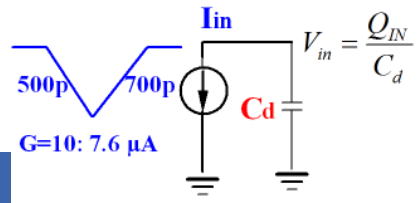
- LGAD sensor w =50µm
- rise time : tr~500ps
- « Decay time» : td~700ps



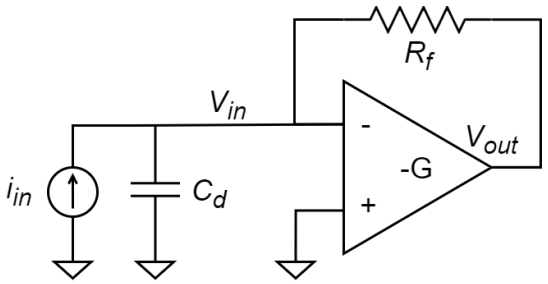




LGAD current



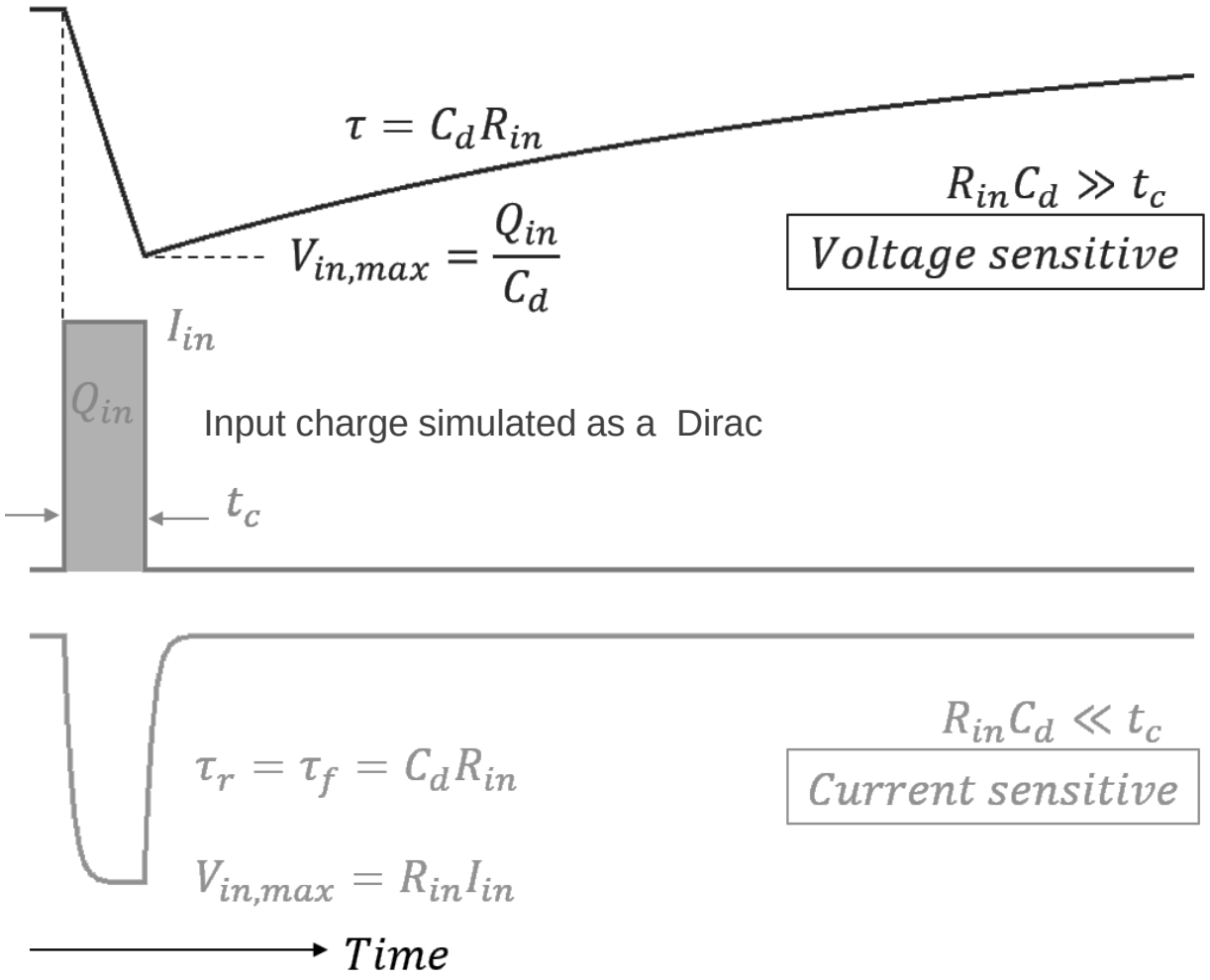
Preamplifier choice: Voltage or current amplifier ?



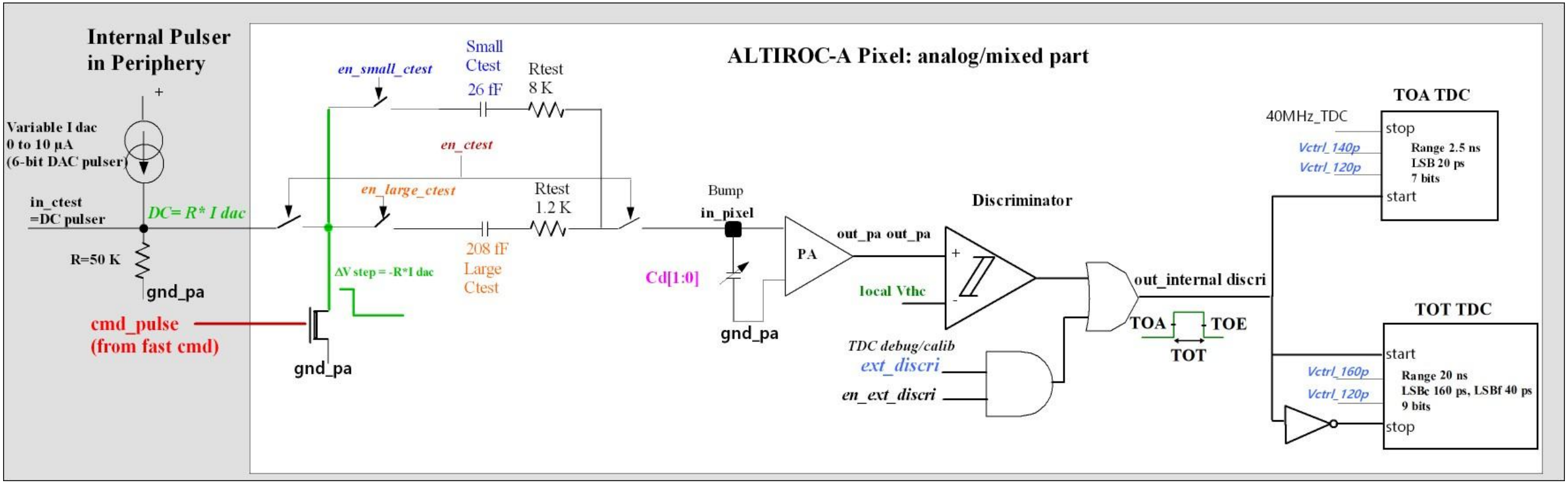
$$R_{in}(\omega) = \frac{R_f}{1 + G(\omega)}$$

$$R_f = \{8\,;\,20\,;\,25\}\ k\Omega$$

TZ VPA



ALTIROC CHARACTERIZATION: INTERNAL CHARGE INJECTION and TDC CALIBRATION



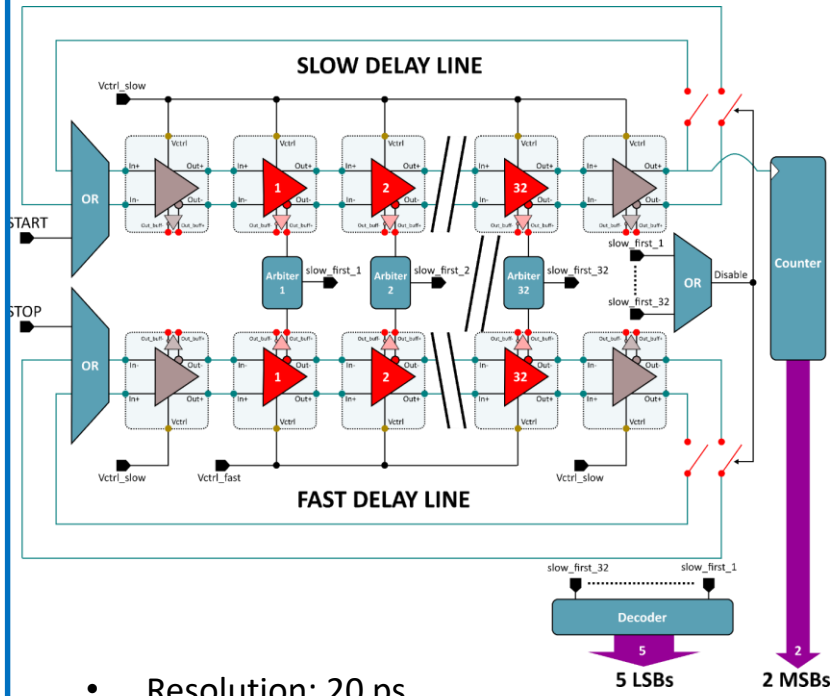
Internal pulser and Ctest capacitors: Injection system that mimics LGAD signals with input charges from 1 fC to 100 fC

Internal Cd (set by Slow Control) to mimic the sensor capacitance in case of ASIC alone tests

"ext_discri"= digital signal made internally from the "CAL" fast command. Used to calibrate the TDC

TOA TDC and TOT TDC

TOA TDC



- TDC range is equal to **128*20 ps = 2.56 ns**

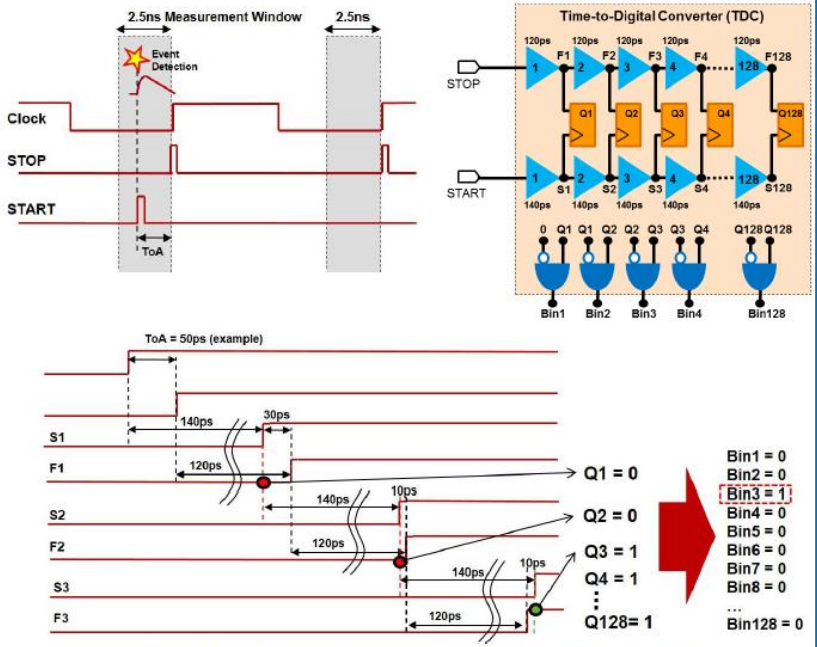


Figure 11: TDC for TOA measurement: principle and delay Vernier line

- Resolution: 20 ps
- Range: 2.5 ns
- 7 bits

TOA conversion: 7 TOA bits = TOA [6:0], TOA overflow

Measured time interval calculation: T_{TOA_meas} = TOA [6:0]*20ps

- Cycling configuration used in order to reduce the total number of Delay Cells.

TOT TDC

The TOT TDC is made of a coarse delay controlled by "vctrl_160p" and of a fine Vernier delay line controlled by "vctrl_160p" and "vctrl_120p".

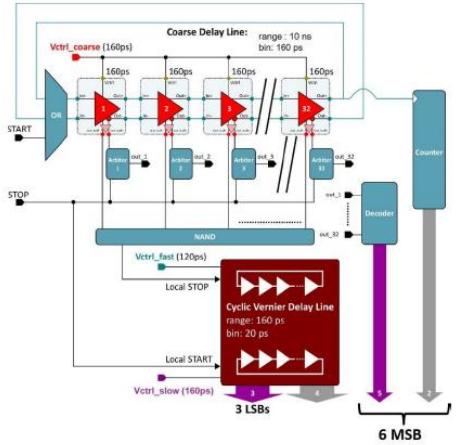


Figure 14: TOT TDC

TOT conversion is made on 9 bits, TOT[8:0]. The resolution is 40 ps and the range 10 ns

Measured time interval calculation is given by: T_{TOT_meas} = TOTc[5:0]*160ps – TOTf[2:0]*40ps= TOT[8:3]*160ps – TOT[2:0]*40ps

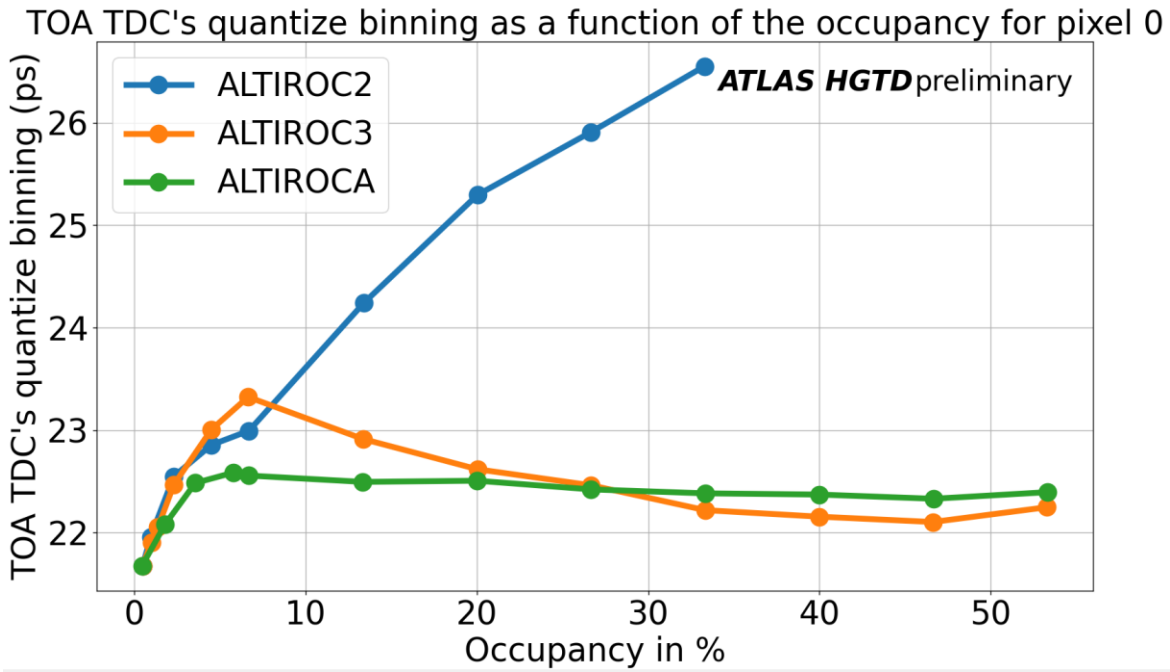
ALTIROCA PERFORMANCE: TOA TDC bin and IR drops

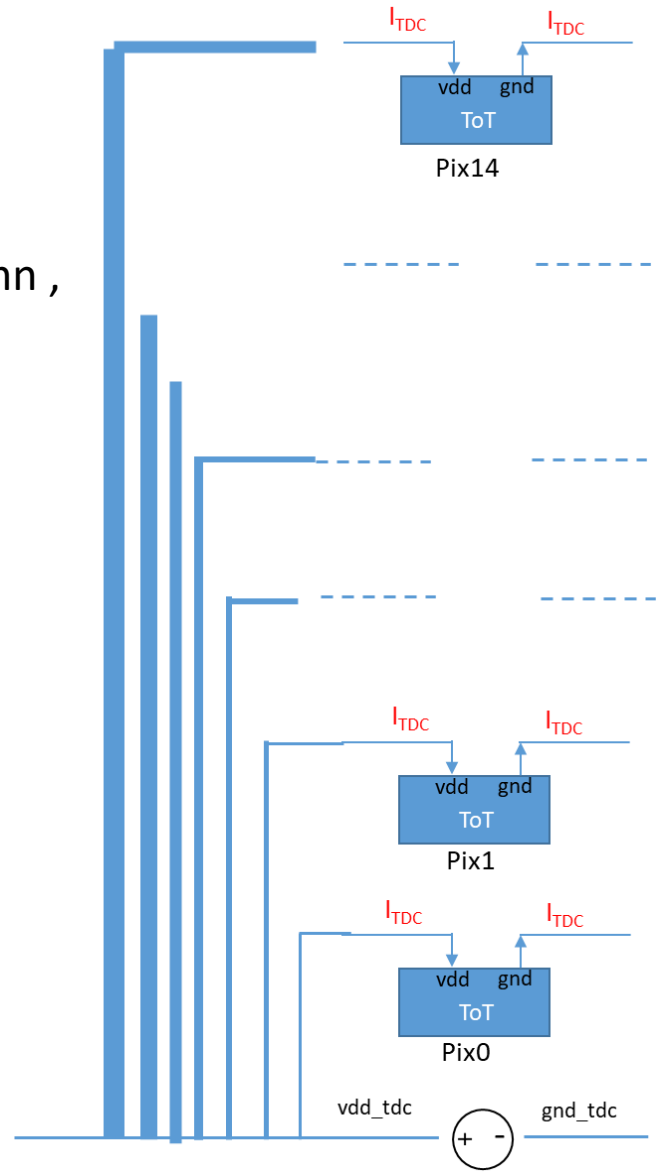
- TOA TDC : Two Vernier lines (140 ps and 120 ps), TDC bin 20 ps

- TDC bin issues in ALTIROC2 related to V drops

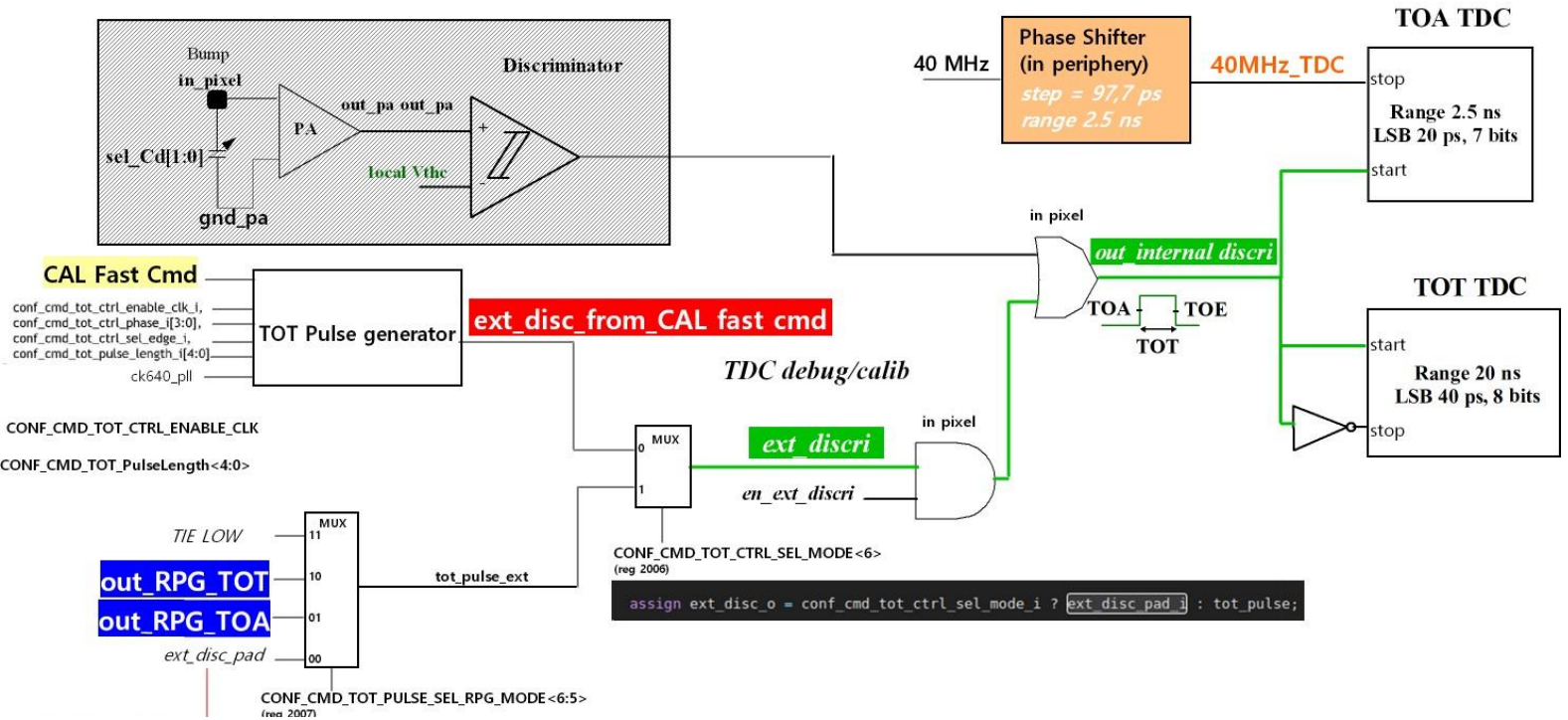
⇒ separated TDC power bus for each column = Vdd_toa, vdd_tot, gnd_toa, gnd_tot per column , same R

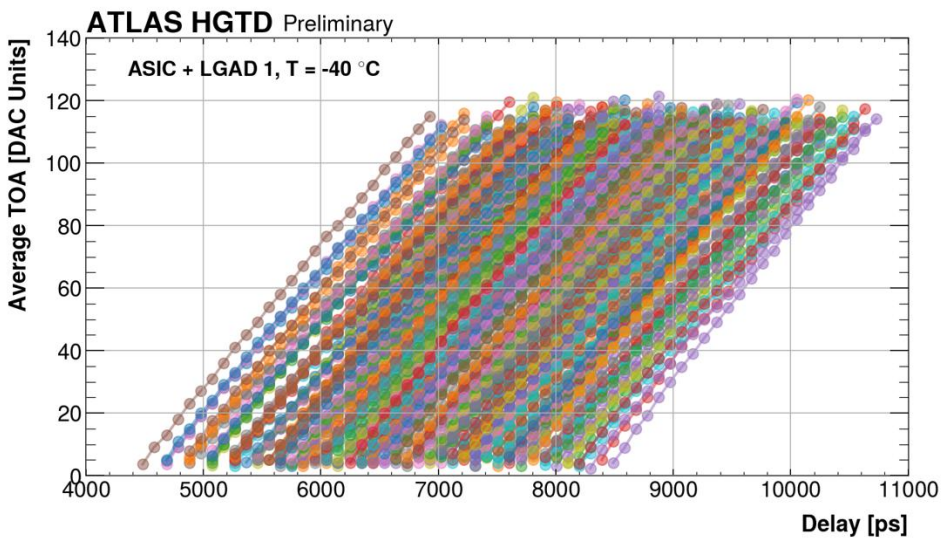
More details in this TWEPP2024 talk:
https://indico.cern.ch/event/1381495/contributions/5988493/attachments/2869323/5163702/TWEPP2024_Soulier.pdf





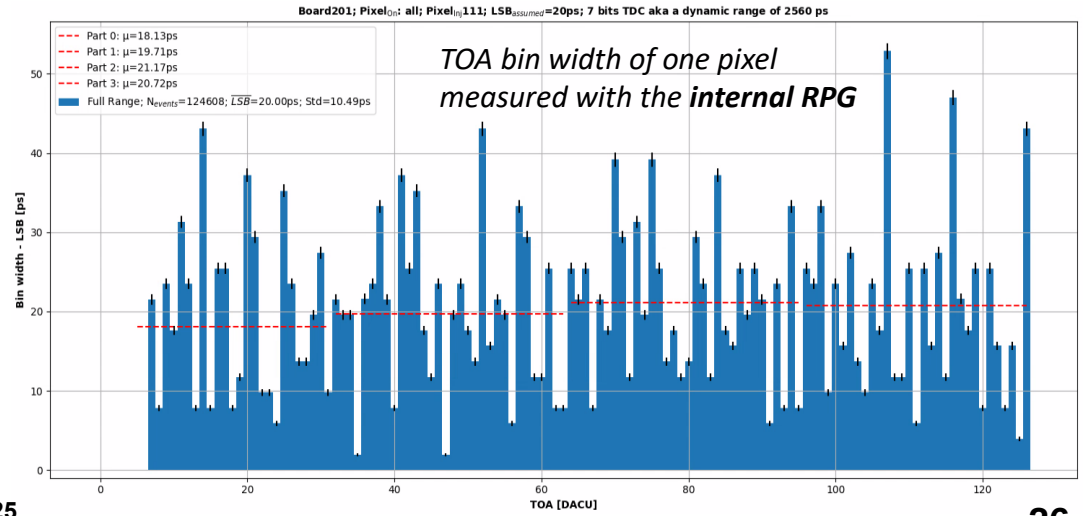
TDC Bin (=LSB) calibration: Delay scans and Random Phase Generator





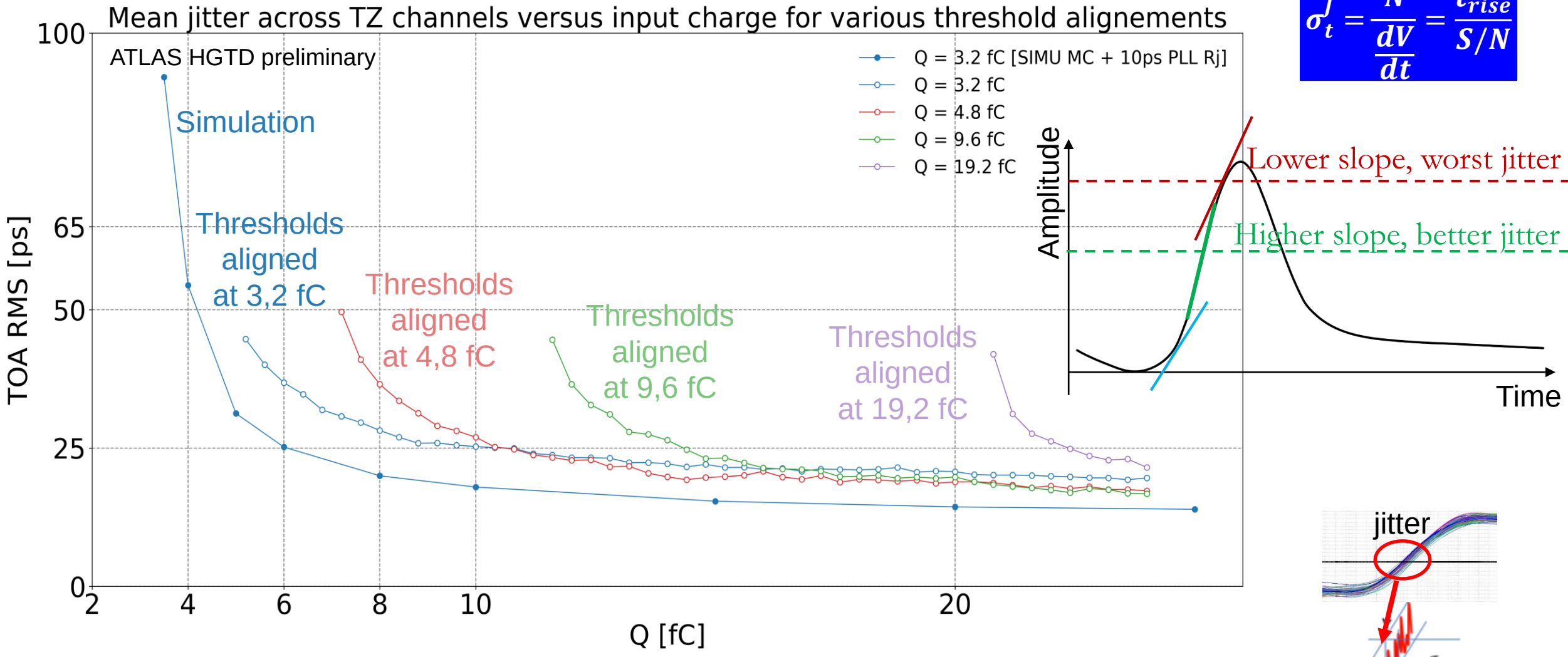
Average Time Of Arrival (TOA) measured with the TDC as a function of the programmable delay using direct injection of a digital discriminator pulse at the input of the TDCs.
Each curve belong to one single channel of the matrix. The TOA bin (LSB) is extracted from the linear fit

- Two calibration systems in ALTIROC
  - Use of an «ext_disc» = created internally from the CAL fast command
    - use of the **internal phase shifter** to delay the 40 MHz ck used by the TOA TDC (**97.7 ps steps**) => measurements of the TOA quantization steps (TOA bin)
    - Varying the pulse width => measurements of the TOT quantization steps (TOT bin)
  - Use of a Random Phase Generator (RPG) to measure the TDC DNL
    - Programmable VCO that generates programmable clocks asynchronous with the 40 MHz ck used by the TDC
    - The TDC distribution is a relative measurements of the TDC bin width



Jitter depends on the charge, but also on the discriminator thres.

$$\sigma_t^J = \frac{N}{\frac{dV}{dt}} = \frac{t_{rise}}{S/N}$$



Threshold trade-off to maximise pulse slope (dV/dt), thus minimize jitter.