STCF Trigger Design and R&D Progress

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On behalf of STCF TRIG group
26/11/2025

Outline

1. STCF and Trigger system
2. L1 trigger algorithm progress
3. L1 trigger hardware platform R&D
4. HLT study
5. Summary

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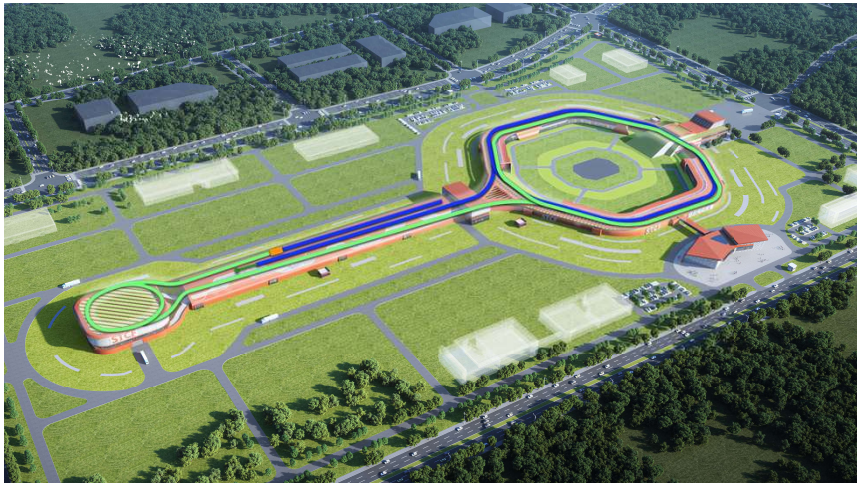
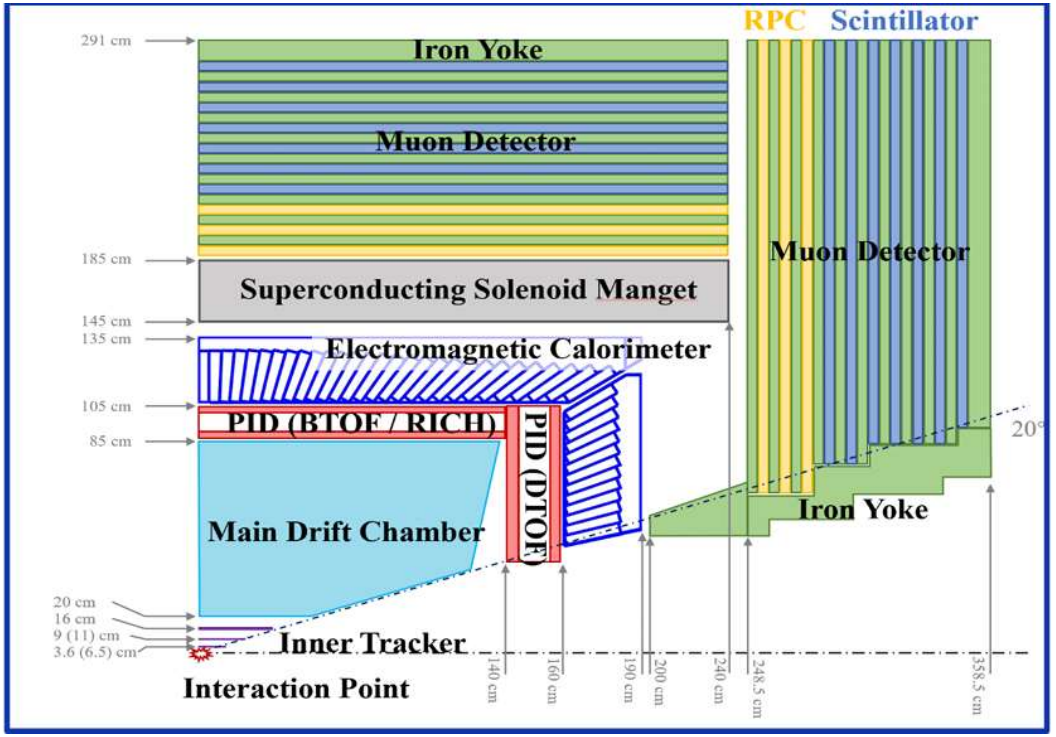
STCF detector

STCF key design parameters

- Luminosity: > **0.5×10^{35} $cm^{-2}\cdot s^{-1}$** @4 GeV
- Center-of-mass energy: **2~7 GeV**
- Highest physic event rate: **400 kHz**



STCF detector cross section



STCF trigger system

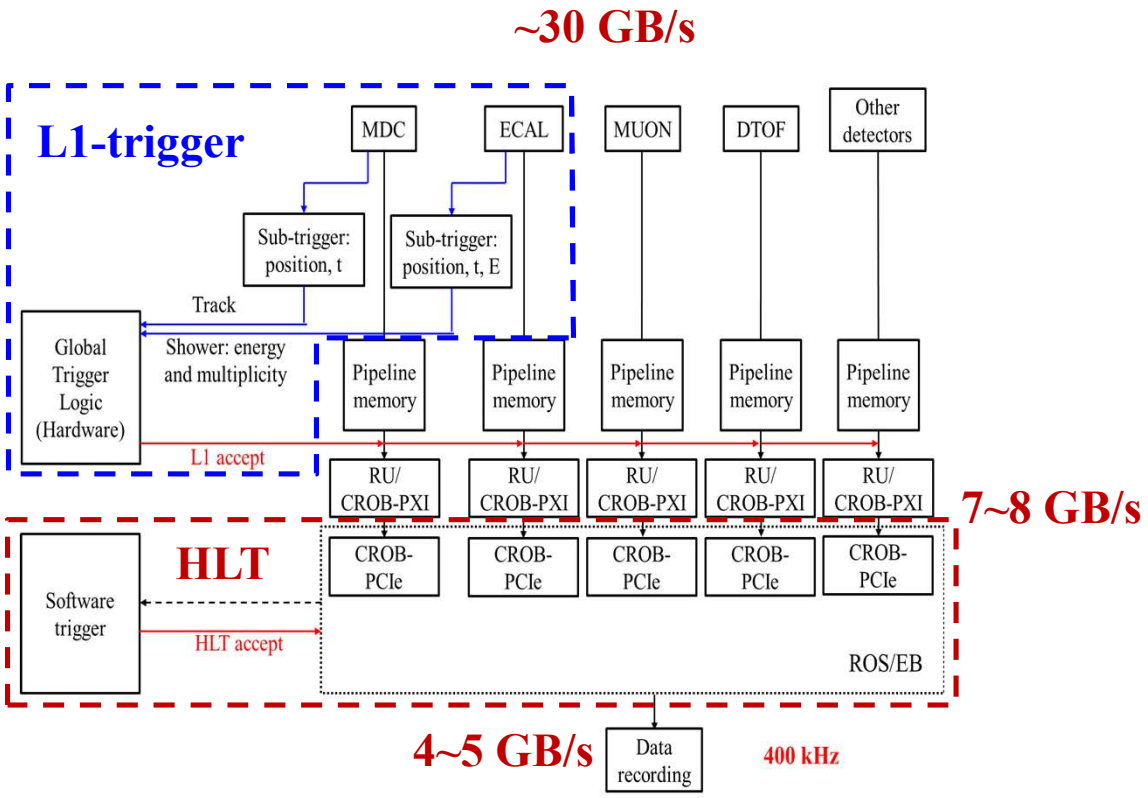
STCF trigger requirements

- High trigger efficiency (~99%)
- Low background trigger rate (< 50 kHz)
- Trigger rate (hundreds of kHz)
- High throughput, low latency

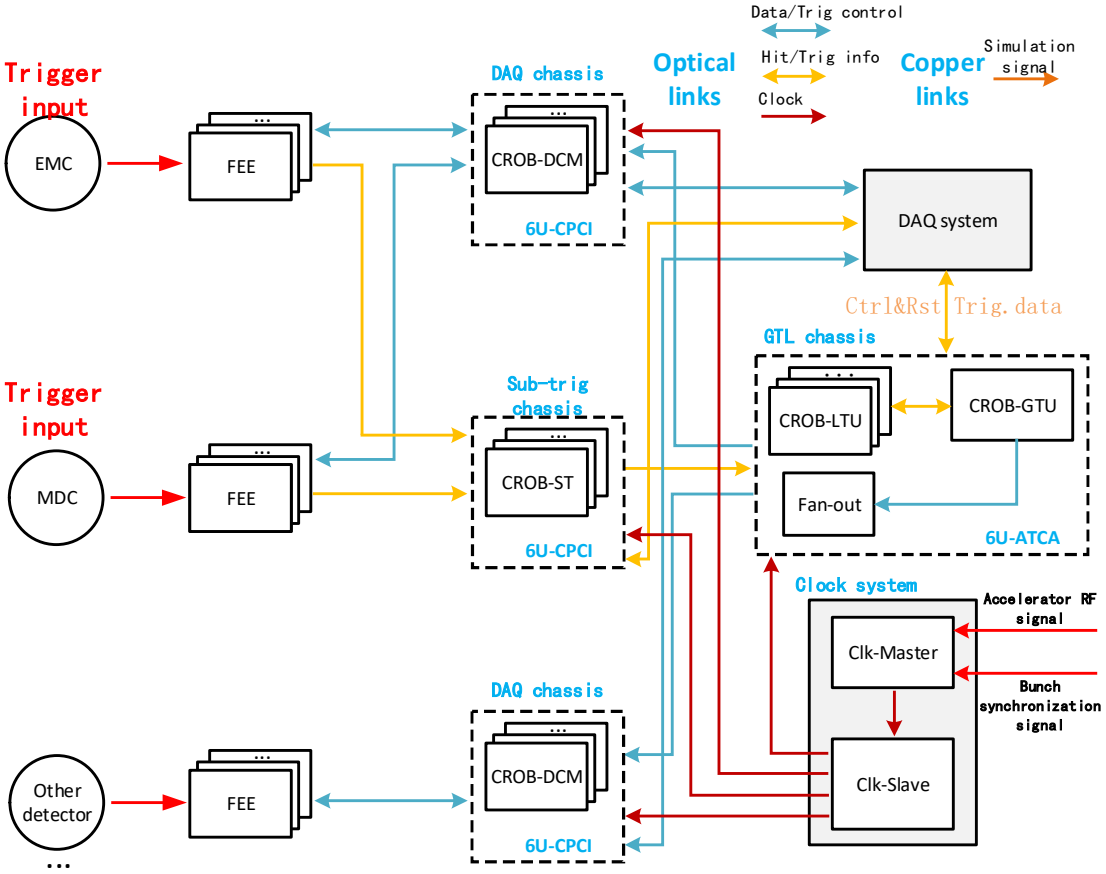
Route of trigger design

- L1 + HLT

Schematic of STCF TRIG system



L1 trigger hardware design

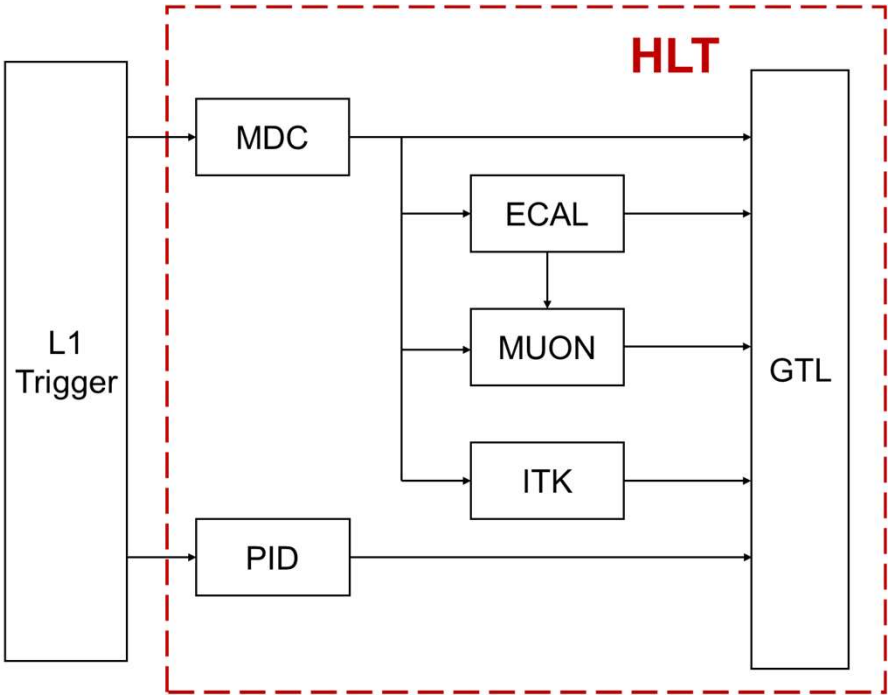


- Separated L1 trigger and DAQ system
- **CROB-DCM** for data collection for DAQ system
- **CROB-ST** for data collection for L1 trigger
- Delivery L1 trigger decision by **DAQ chassis to FEE**
- Global clock: 40 MHz

HLT preliminary design

HLT algorithm flowchart

- CPU + GPU heterogeneous computing framework



HLT design:

- Identify and remove background hits
- Re-filter the data slice in event level

Performance targets:

- Data compression ratio: 70%
- Latency: ~ 100 ms

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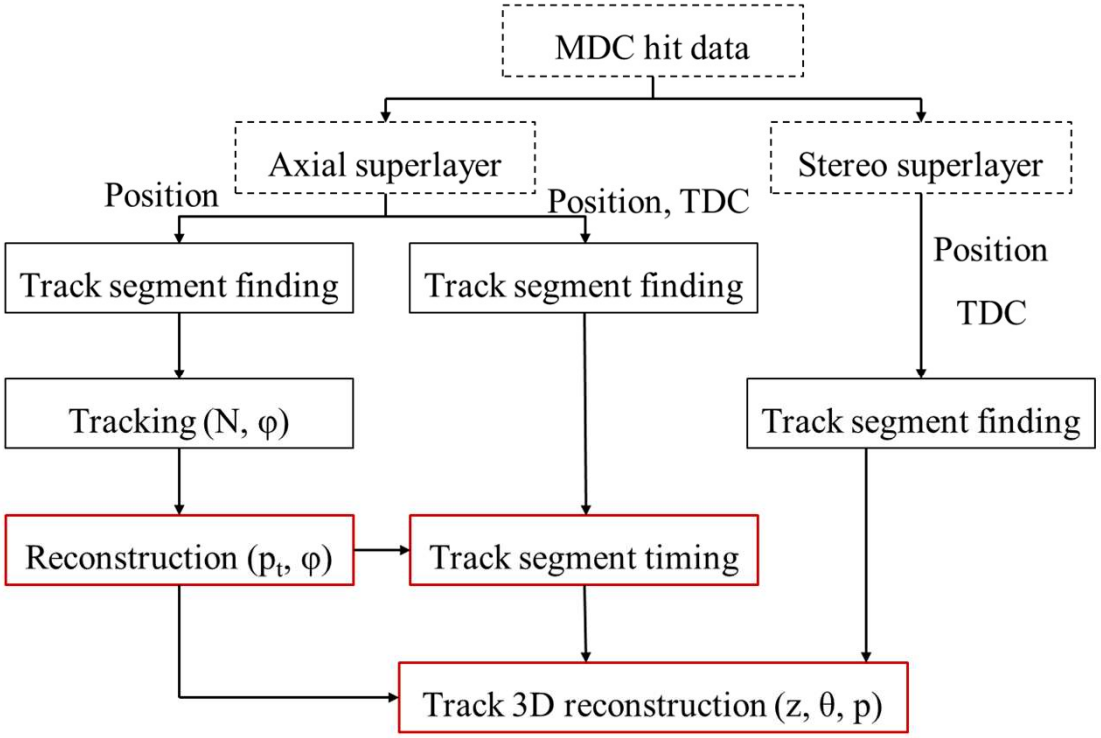
MDC sub-trigger R&D

MDC algorithm



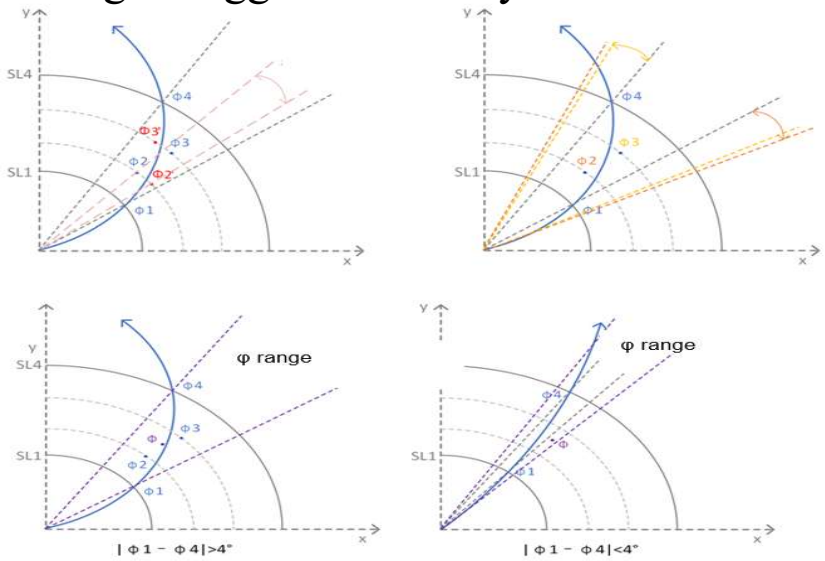
Sub-algorithms

- **2D tracking and reconstruction:**
  transverse momentum(p_t),
  azimuthal angle(φ)
- **Time reconstruction:**
  track segment time,
  track time(t)
- **3D reconstruction:**
  z-vertex,
  polar angle(θ),
  momentum(p)

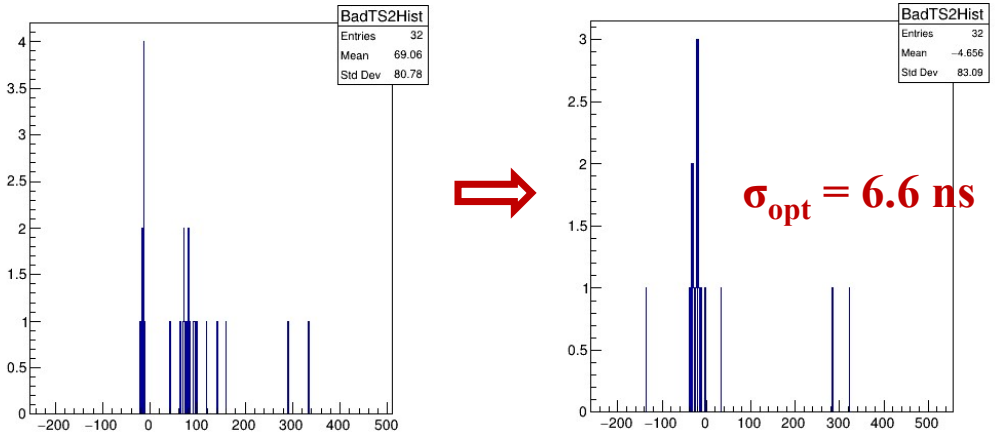
MDC sub-trigger R&D

Optimization for short track tracking

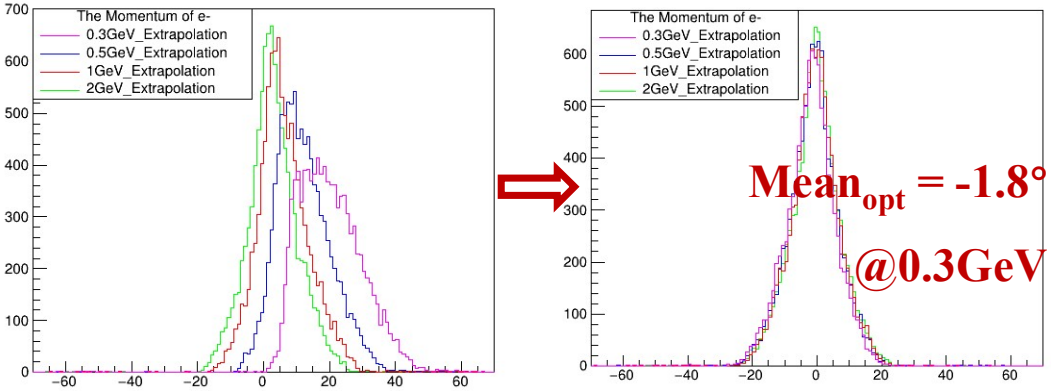
- Using three φ-position constraints
- Single track efficiency exceeds **99%**
- Reduces background false tracking rate in charged trigger channel by **50%**



Track timing optimization

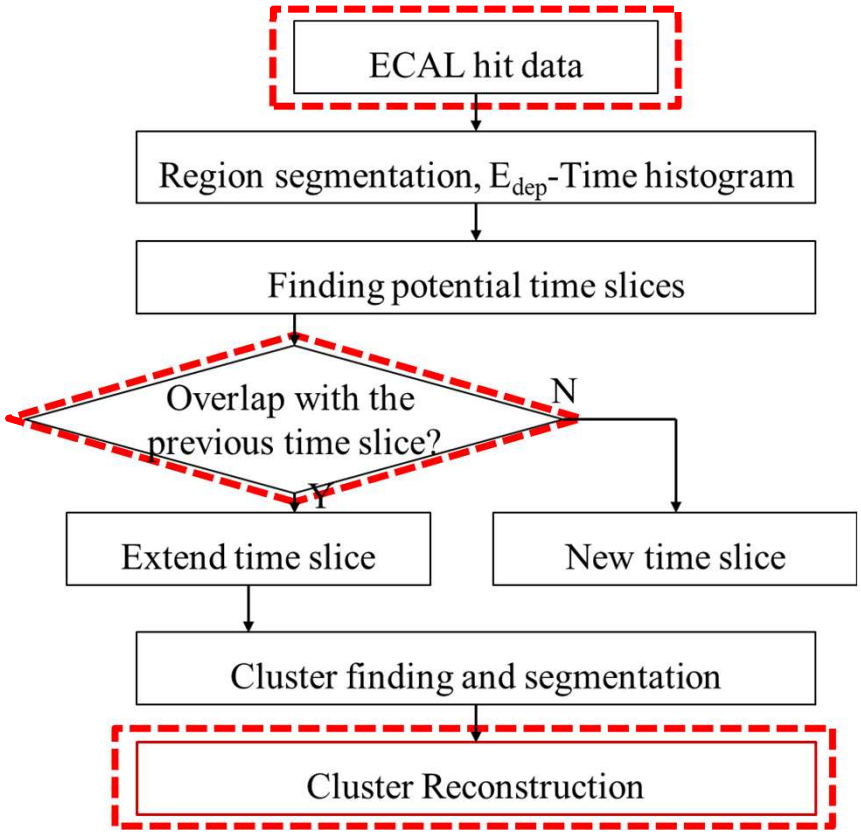


MDC θ positioning optimization

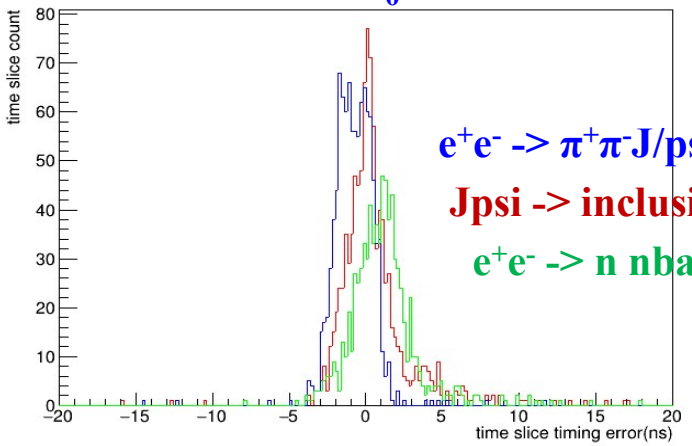


ECAL sub-trigger R&D

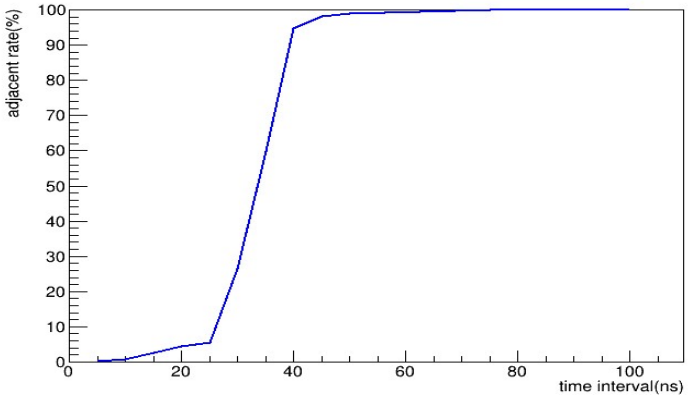
ECAL algorithm



Event T_0 residual



Adjacent events separation



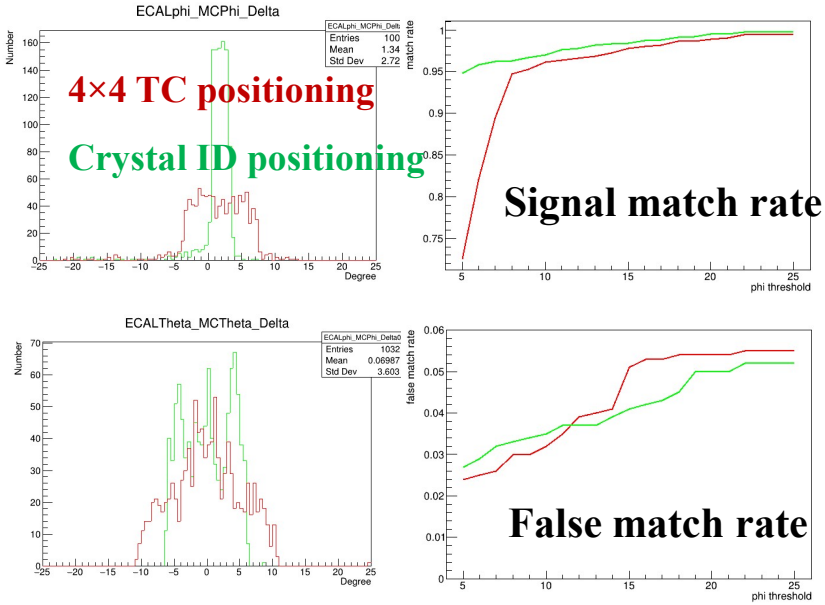
ECAL sub-trigger R&D

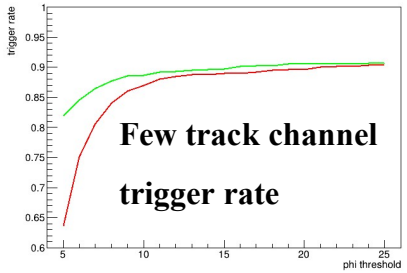
☐ New positioning method for clusters

- FEE transferring T/Q
- Choose crystal with highest ΔE

Performance optimization

- φ resolution : 3.1°→1.0°
- θ resolution : 5.7°→2.5°
- Higher match rate at low threshold



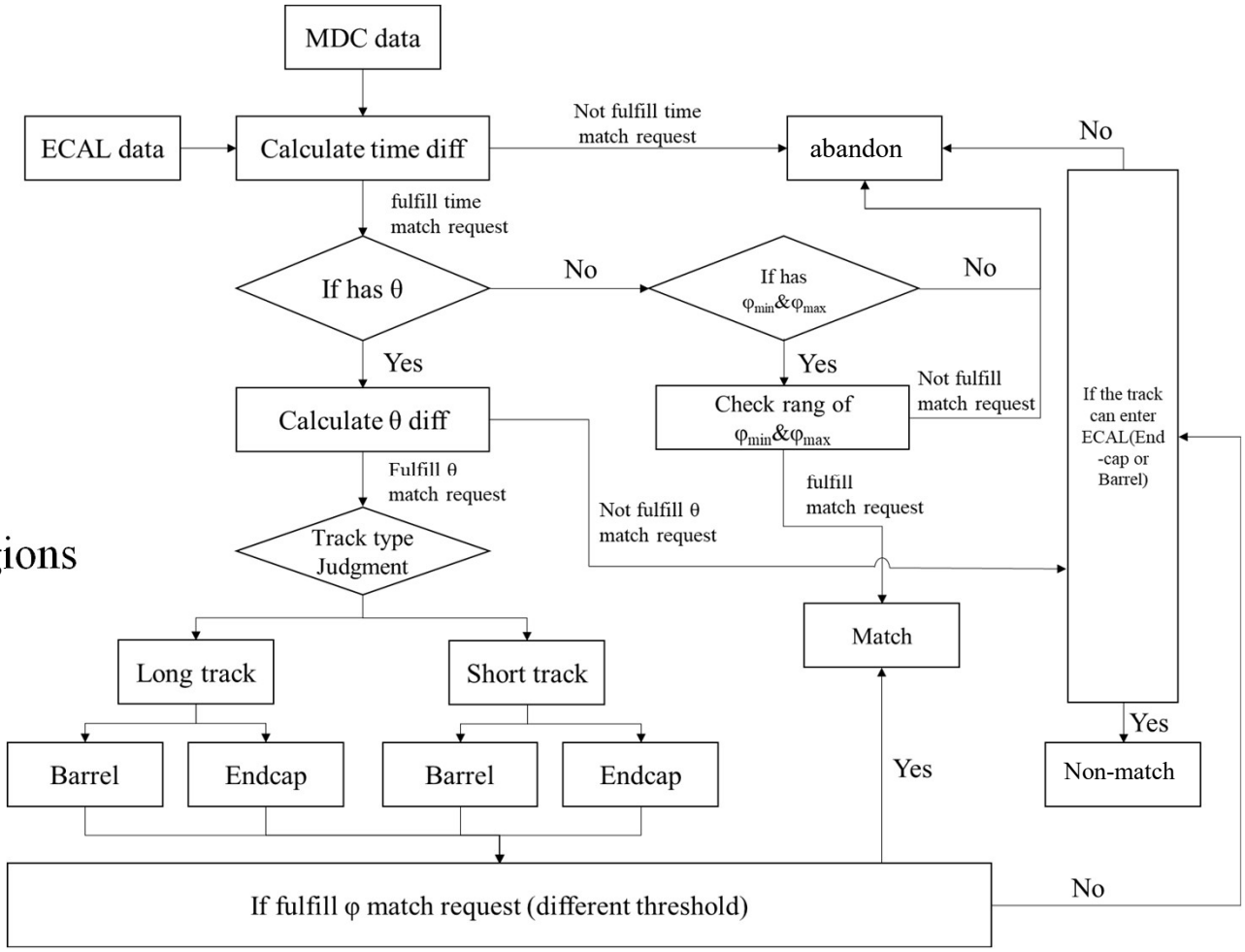


Positioning performance **Match performance** **Trigger performance**

L1 trigger GTL R&D

☐ Match logic optimization

- Un-matched track and cluster
- Using θ in match
- Various criteria in different ECAL regions



Trigger table design

		1	2-1	2-2	2-3	2-4	3-3	4-1	4-2	4-3	5-1	5-2	5-3	6	7	8	9-1	9-2	10-2	10-3	10-4	10-5	11	12-1	12-2	12-3	13	14	15
Charged	1-1	N		Y					Y					Y						Y			N					Y	
	1-2	N		Y					Y						Y	Y				Y			N					Y	
	1-3	N		Y					Y											Y			N				Y	Y	
	1-4	N		Y					Y					Y						Y			N						Y
	1-5	N		Y					Y						Y	Y				Y			N						Y
	1-6	N		Y					Y											Y			N				Y		Y
	2-1	N	Y		N		N	Y				Y					Y		Y			N							
	2-2	N	Y		N		N	Y				Y							Y			N					Y		
	3-1	N			Y	N				Y			Y	Y					Y										
	3-2	N			Y	N				Y			Y		Y	Y			Y										
	3-3	N			Y	N				Y			Y						Y							Y			
	3-4	N			Y	N		Y				Y					Y			Y							Y			
	3-5	N			Y	N			Y								N				Y									
	4-1	N				Y								Y					Y										
	4-2	N				Y									Y	Y			Y										
	4-3	N				Y													Y							Y			
	4-4	N											N	Y					Y										
	4-5	N											N		Y	Y			Y										
	4-6	N											N						Y							Y			
Neutral	5-1	N	Y	N				N																Y						
	5-2	N	Y	N				N																	Y					
	5-3	N		Y	N			N																Y						
	5-4	N		Y	N			N																	Y					
	5-5	N			Y			Y	N															Y						
	5-6	N			Y			Y	N												Y									
	6	N	Y																Y											
L.M.	7-1							Y			Y							Y					Y					Y	
	7-2							Y			Y							Y								Y		Y	
	7-3							Y			Y							Y						N	Y	Y		Y	
	7-4							Y			Y							Y					Y						Y
	7-5							Y			Y							Y								Y			Y
	7-6							Y			Y							Y						N	Y	Y			Y
Random																														

L1 trigger performance

- **Background trigger rate <15 kHz** @ charged channels; **<30 kHz** @ charged + neutral channels

Trigger channel	Physics signal	Energy point	Number of tracks that is matched	Number of miss matched tracks	Signal trigger rate	Background trigger rate(kHz)	Signal trigger rate
Charged channel	J/psi -> inclusive	3.097GeV	2252	9	928/945(937) (≥2)	23.8	98.2%(99.0%)
	$e^+e^- \to \pi^+\pi^- J/psi$, Jpsi -> e^+e^-	4.26GeV	3195	18	946/952 (≥3)		99.4%
	$e^+e^- \to \pi^+\pi^- J/psi$, Jpsi -> $\mu^+\mu^-$	4.26GeV	3185	18	946/948 (≥3)		99.8%
	$e^+e^- \to \tau^+\tau^-$	4.26GeV	1586	10	868/879 (≥2)		98.7%
	$e^+e^- \to \pi^+\pi^- J/psi$, J/psi -> $\Lambda\bar{\Lambda}$	3.097GeV	2043	11	912/918 (≥3)		99.3%
	$e^+e^- \to \pi^+\pi^- J/psi$, J/psi -> $\Xi\bar{\Xi}$	3.097GeV	2220	11	914/922 (≥5)		99.1%
	$e^+e^- \to K^+K^- J/psi$, J/psi -> l^+l^-	4.682GeV	2921	11	962/964 (≥3)		99.9%
	$e^+e^- \to D_0\bar{D_0}$	3.773GeV	2925	15	955/954 (≥3)		100%
	$e^+e^- \to D^+D^-$	3.773GeV	3103	12	984/983 (≥3)		100%
	$e^+e^- \to D_s^+D_s^-$	4.04GeV	3797	15	937/936 (≥5)		100%
Neutral channel	J/psi-> gam invisable	3.097GeV	-	-	521/524 (≥1&&gam_momentum>=1)		99.4%
	e^+e^- -> n nbar	3.097GeV	-	-	535/548 (≥2&&Nbar≥1&&SigEDep_in_EMC ≥0.6)		97.6%
	e^+e^- -> gam n nbar	3.097GeV	-	-	718/730 (≥2&&Nbar≥1&&SigEDep_in_EMC ≥1)		98.2%
	e^+e^- -> gam n nbar(ISR)	3.713GeV	-	-	360/366 (≥2&&Nbar≥1&&SigEDep_in_EMC ≥0.75)		98.4%
Luminosity monitor	Bhabha Scattering	4.26GeV	688	-	391/400 (≥2&&In[21.4,158.6])	0.63%	97.8%

L1 trigger performance

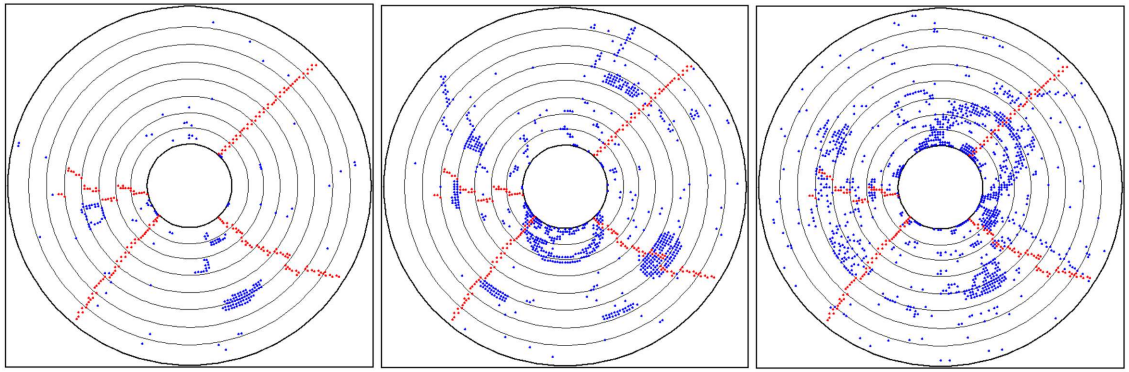
High BKG trigger

- $e^+e^- \to \pi^+\pi^- J/psi,$ $J/psi \to e^+e^-$

	Number of tracks that should(is) matched	Number of false matched tracks	Signal trigger rate	Background trigger rate(kHz)	Trigger channel 05 background trigger rate(kHz)	Trigger channel 02 background trigger rate(kHz)
1bkg	3195	18	99.4%	18.9	7.35	11.6
2bkg	3116	24	99.2%	56.7	36.8	16.8
3bkg	3075	35	98.7%	89.3	63.0	26.3
5bkg	2901	76	98.6%	317.2	220.6	92.4

MDC hitting map

1 bkg 3 bkg 5 bkg



Neutral channel optimizations

- Removed inner endcap region in pure neutral trigger
- Adjusting the thresholds setting according to background level

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3. **L1 trigger hardware platform R&D**
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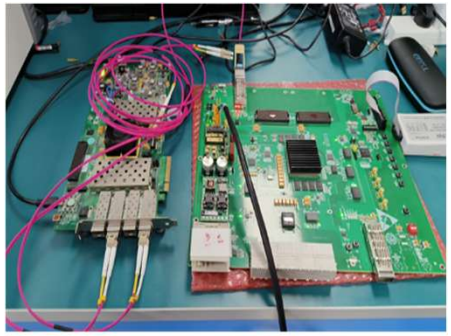
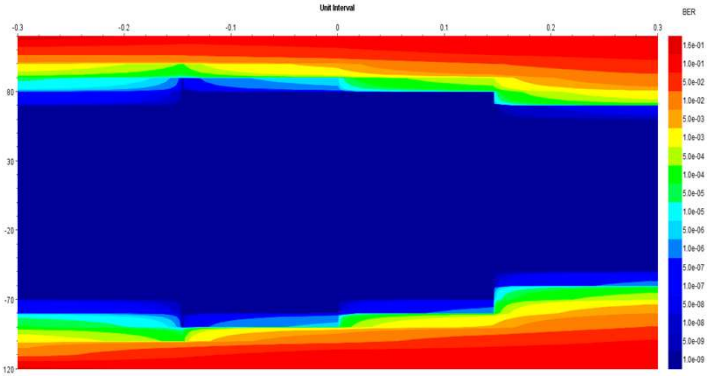
Hardware platform key board R&D

- **CROB-LTU**
- 3rd version of key boards have been manufactured and tested
- 8 DDR4 modules all usable
- **FMC+**
- high-frequency optimizing
- **Data generation board**
- Testing completed
- **CTM board**
- Testing completed


- **10 Gbps eye map of FMC+**



- **Chassis testing**

Hardware algorithm implementation

Resource consumption

- ECAL barrel

Name	CLB LUTs (663360)	CLB Registers (1326720)	CARRY8 (82920)	F7 Muxes (331680)	F8 Muxes (165840)	CLB (82920)	LUT as Logic (663360)	LUT as Memory (293760)	Block RAM Tile (2160)
top_updated	243491	509620	10643	133	31	49537	242662	829	599.5

- ECAL endcap (1 of 2)

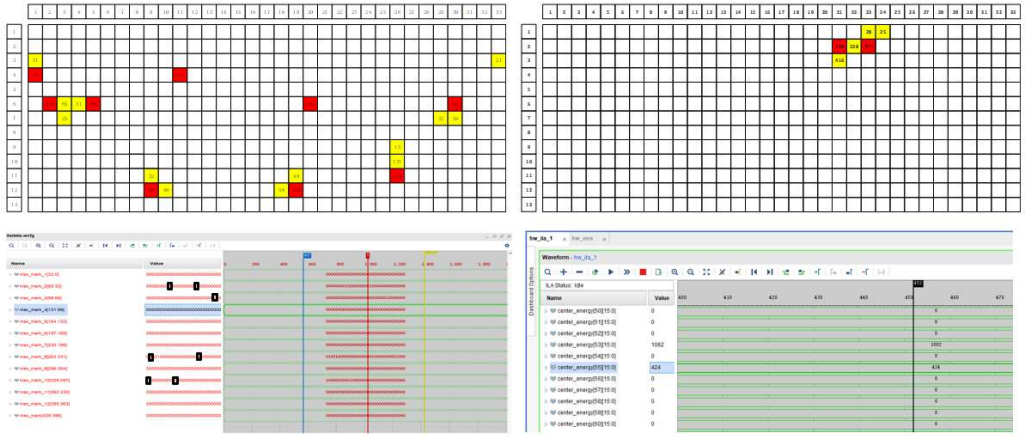
Name	CLB LUTs (663360)	CLB Registers (1326720)	CARRY8 (82920)	F7 Muxes (331680)	F8 Muxes (165840)	CLB (82920)	LUT as Logic (663360)	LUT as Memory (293760)	Block RAM Tile (2160)
top	83341	130684	2858	237	65	17274	82032	1309	132.5

- GTL

	Lut(663360)	Register(1326720)	Carry8(82920)	Muxes(331680)
Gtl_top	147979(22.3%)	366092(27.6%)	18085(21.8%)	5400(1.6%)

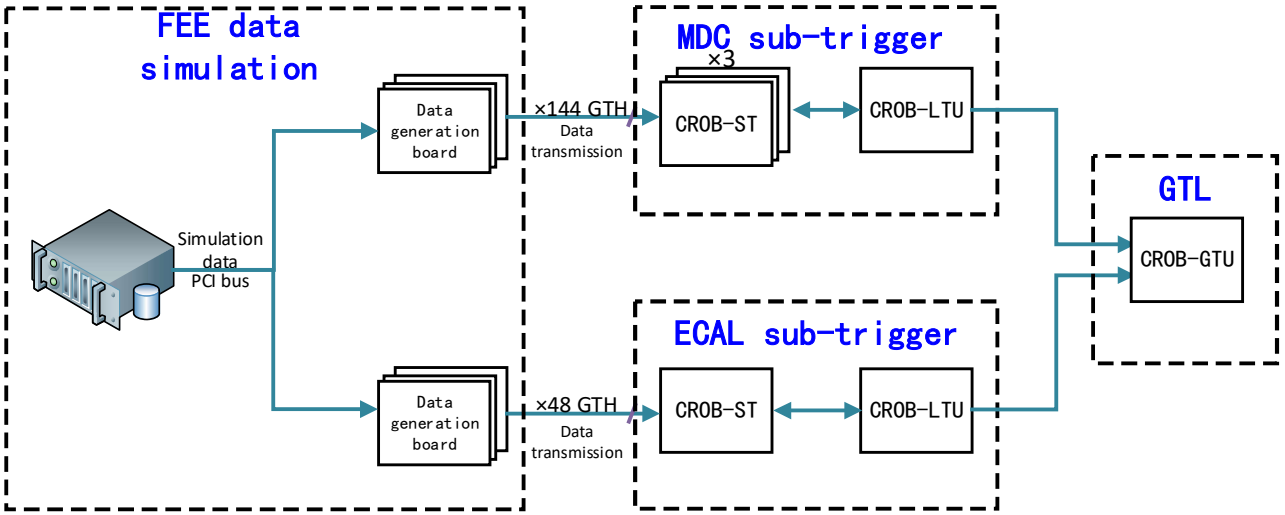
Crosscheck for ECAL algorithm

- Results of cluster splitting by software/hardware algorithm are the same
- Results of cluster energy reconstruction are close
- Hardware latency < 150ns



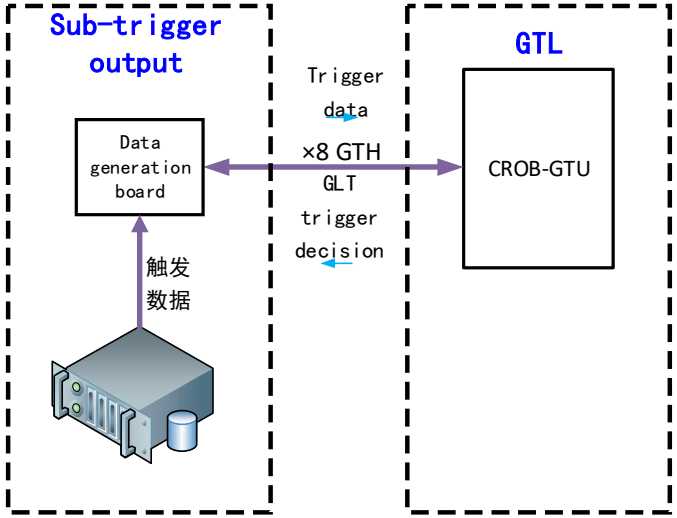
Prototype for L1 trigger

Test for frame and sub-trigger algorithm



- Prototype: 1/8 MDC (cover 1/3 of MDC)、1/4 ECAL
- Frame verification: data transmission, latency
- Sub-trigger algorithm performance evaluation
- GTL performance evaluation

GTL test



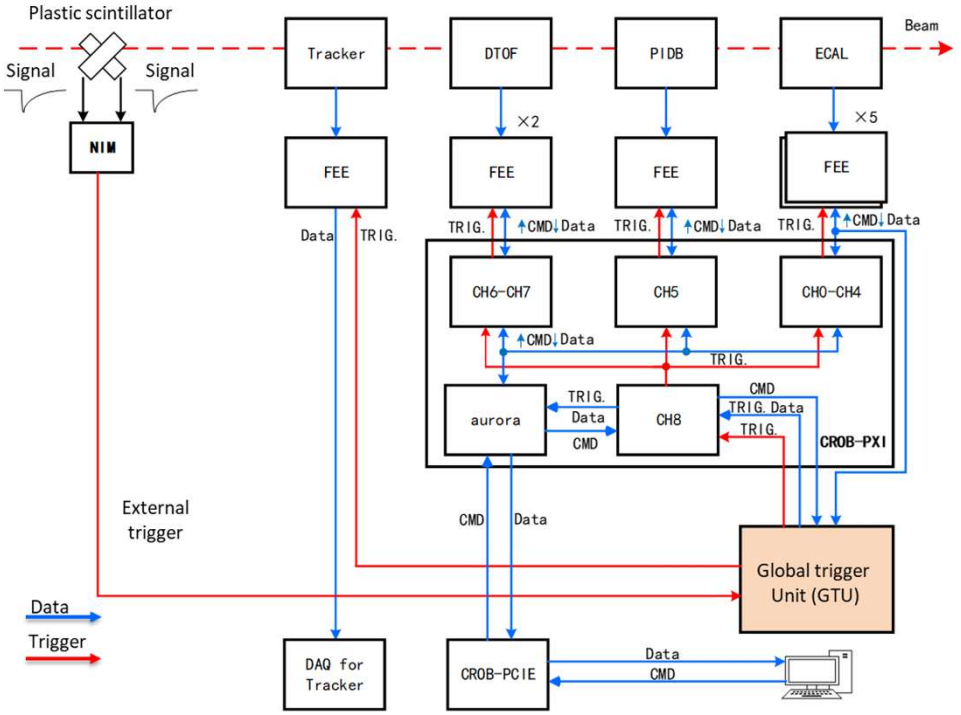
- ✓ **Key boards**
- ✓ **Hardware algorithm**
- ✓ **Simulated input data**

Beam test results

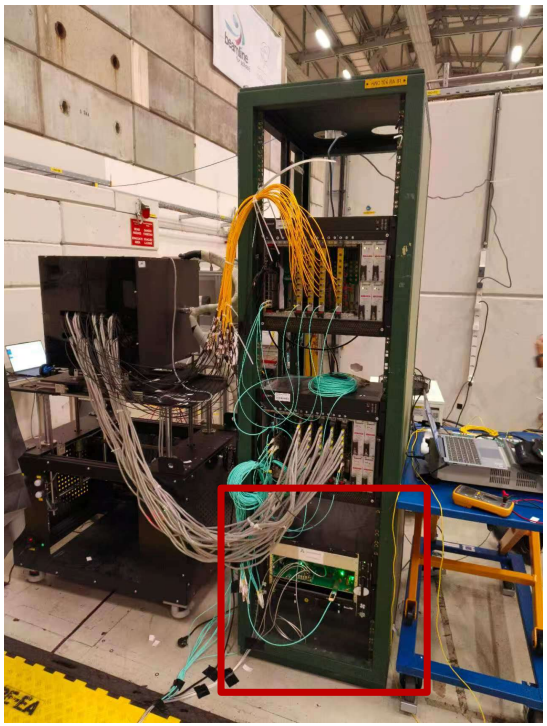
- **GBT link** to PIDB, ECAL, and DAQ implemented
- **Full trigger chain** verified

- Efficiency: **96%** (3.9% loss due to 200 ns trigger deadtime)
- Latency: **1.3 μs**

Beam test setup



Trigger system in beam test



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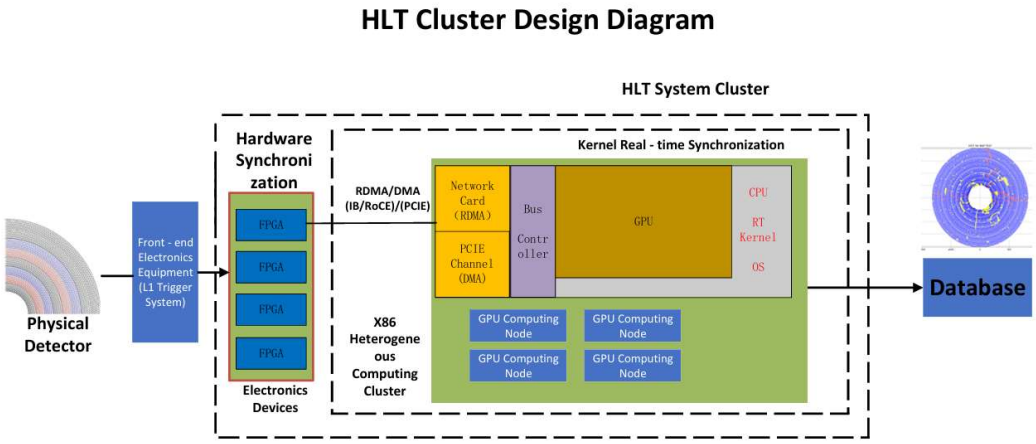
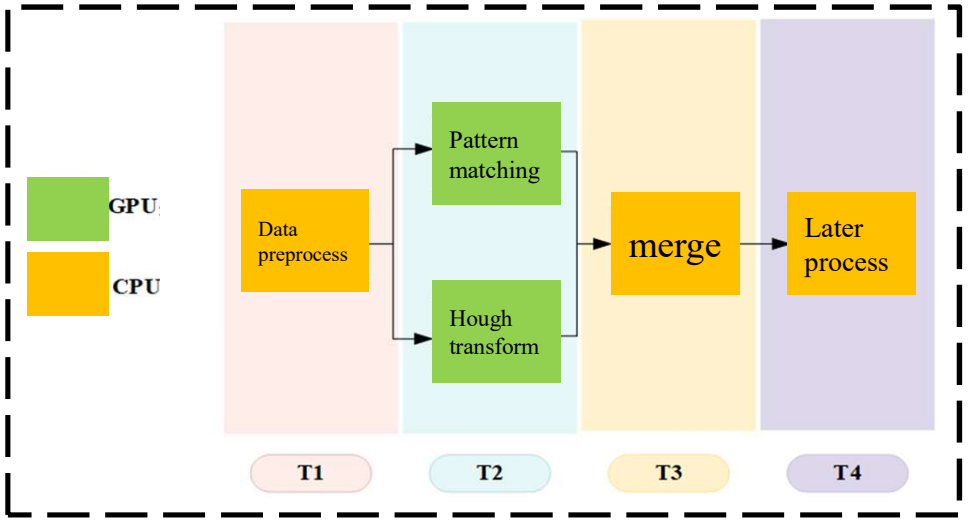
MDC HLT study progress

☐ Hardware design for MDC HLT



- FPGA+X86 heterogeneous system

☐ Algorithm design for MDC HLT

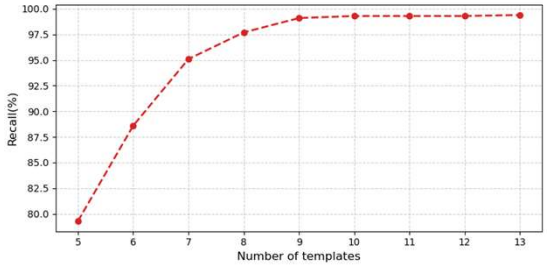


- Pattern matching for high pt track
- Hough transform for low pt track

MDC HLT study progress

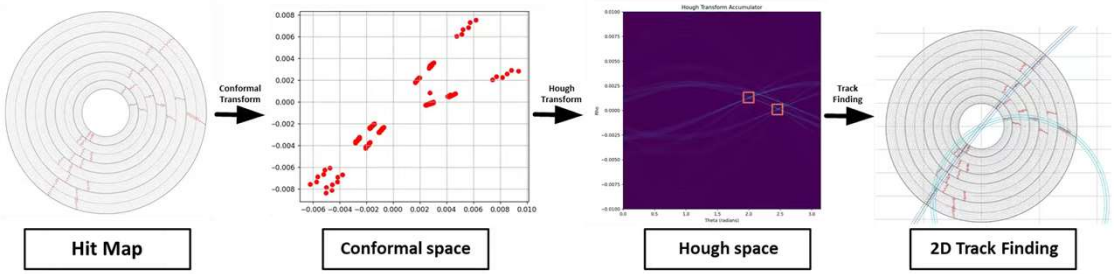
Pattern matching

- Get patterns based on machine learning
- 9 patterns can fit 99% high pt tracks (>400MeV)



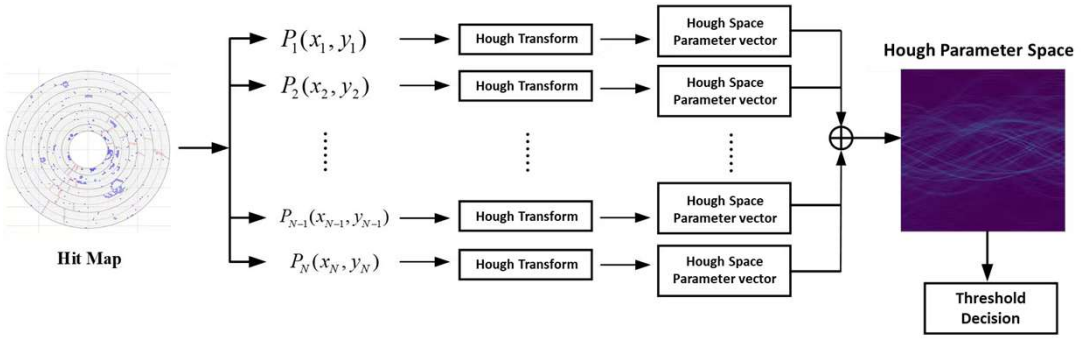
Hough transform

- Find low pt tracks & remove hits
- Parallel acceleration design



Performance

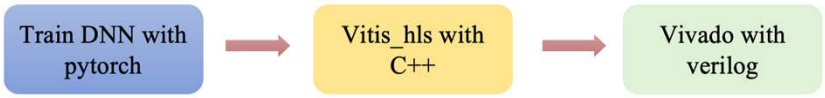
Indicators	KKJPsi	Lambda	taupair	Pipiee	pipimumu
Data compression ratio	0.418	0.492	0.352	0.441	0.446
Signal remain efficiency	0.951	0.947	0.983	0.973	0.977
Ideal data compression ratio	0.331	0.325	0.167	0.262	0.264

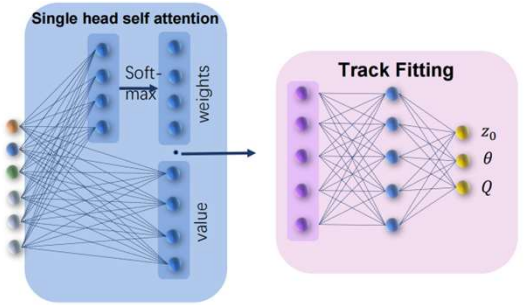


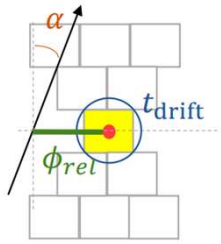
MDC HLT study progress

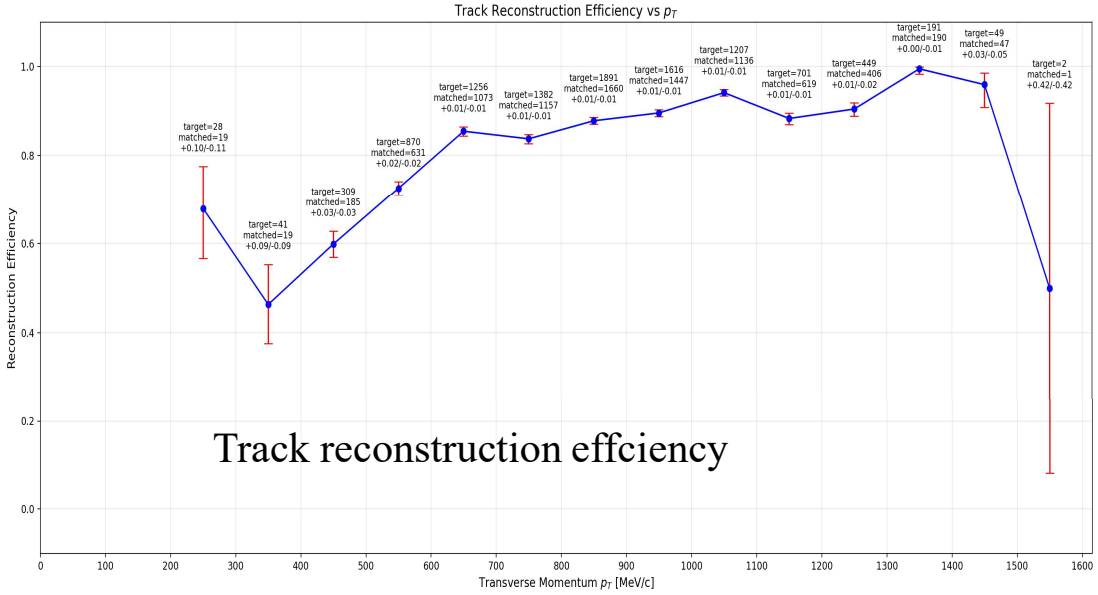
☐ DNN implementation for z trigger

- Use the DNN model in Belle II HLT



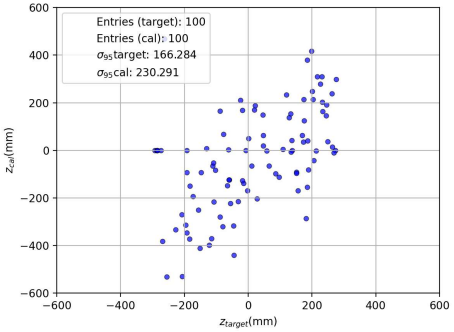






$$\alpha = \arcsin\left(\frac{1}{2}\cdot \mathrm{r_{TS}}\cdot\omega\right), \omega = \frac{1}{R_{track}}$$

$$\varphi_{rel} = \varphi_{cross} - \varphi_{TS} = \varphi_0 - \alpha - \varphi_{TS}$$

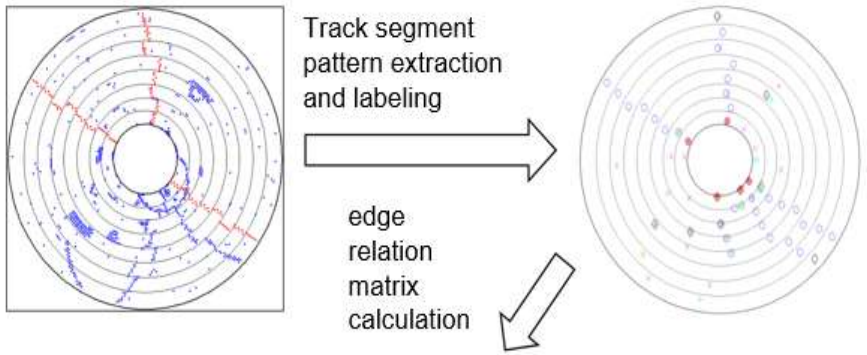


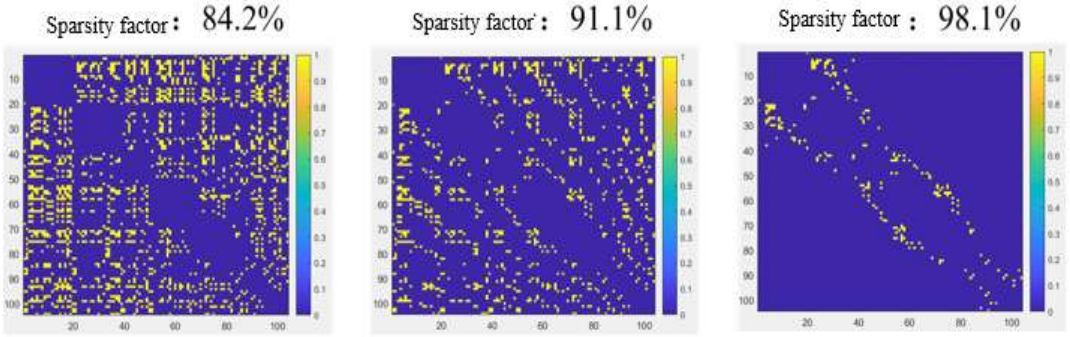
Scatter plot of z fitted by formula and target value

MDC HLT study progress

Track segment finding

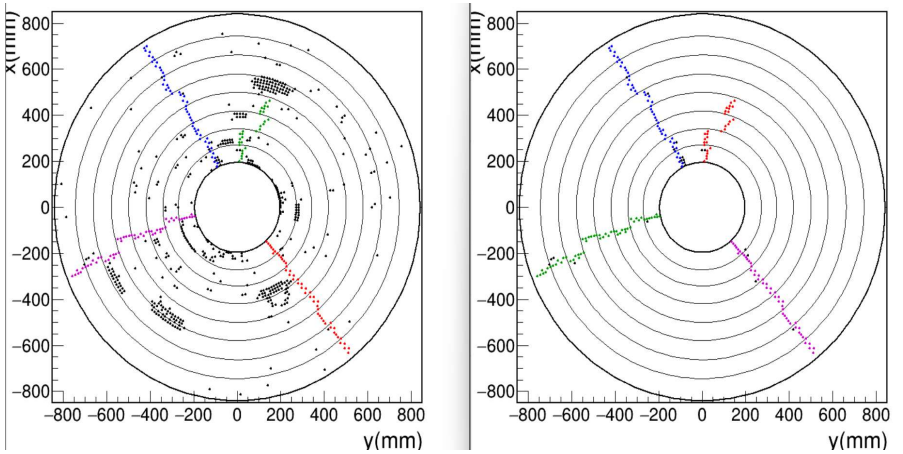
& Connected-component tracking





Preliminary performance

- $(e^+e^- \rightarrow \pi^+\pi^- Jpsi,\ Jpsi \rightarrow e^+e^-)$
- Signal retention ratio 96.1%
- Purity 79.6%
- Data compression ratio 36.5%
- Latency: 80 ms + 150 ms



Outline

1. STCF and Trigger system
2. L1 trigger algorithm progress
3. L1 trigger hardware platform R&D
4. HLT study
5. **Summary**

Summary

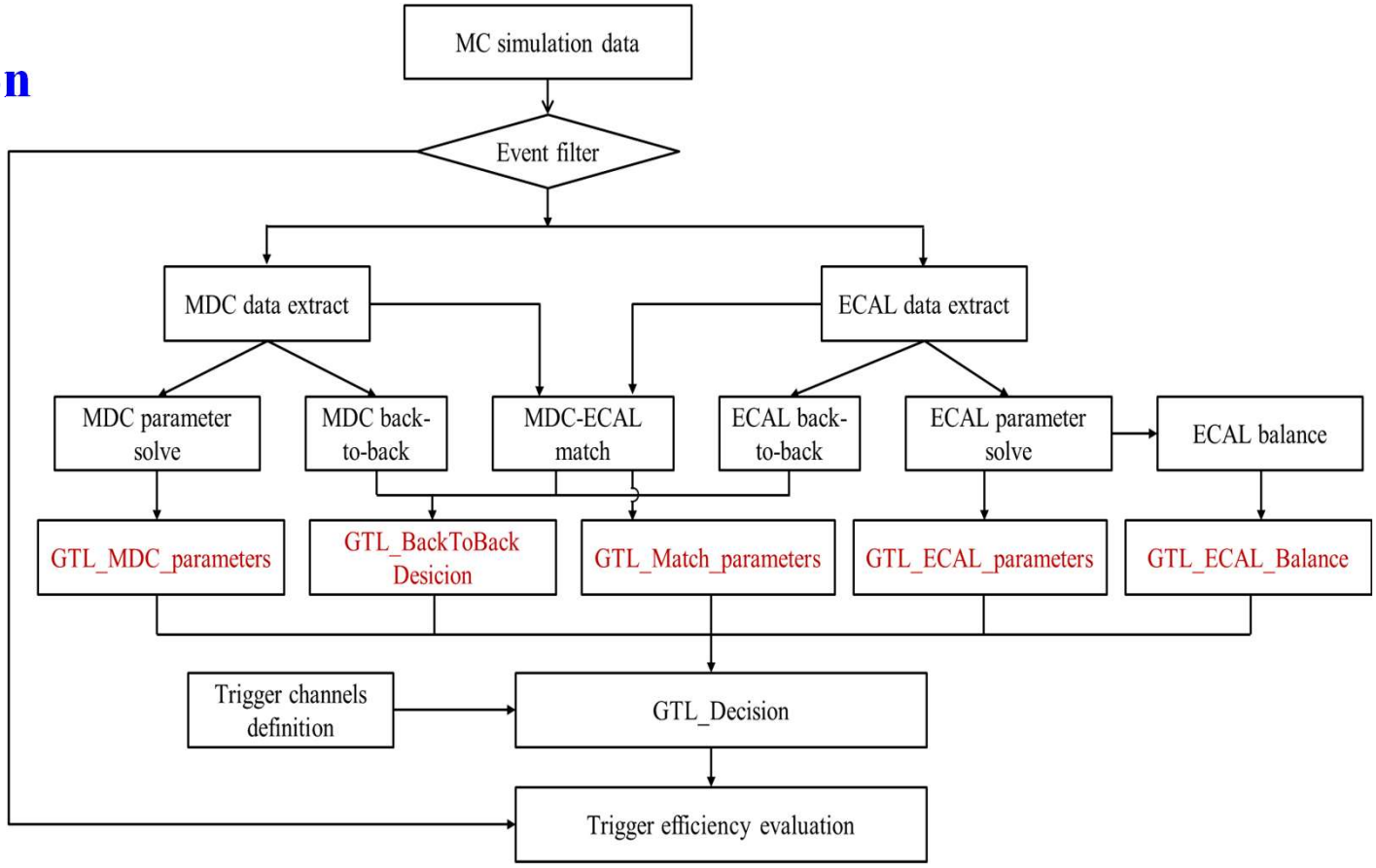
- **L1 trigger algorithm:**
  - ✓ Trigger efficiency to typical charged physics channel: **99%**
  - ✓ Trigger efficiency to neutral channel: **97%**
  - ✓ **Background trigger rate**: **< 30 kHz** @ charged + neutral channels
- **Hardware platform and prototype:**
  - ✓ All key boards have passed the test: CROB-LTU, FMC+ …
  - ✓ Hardware algorithms almost prepared
  - ✓ **Full trigger chain verified** in beam test
- **HLT:**
  - ✓ Investigate MDC HLT via three different approaches

Thanks~

backup

L1 trigger GTL optimization

- Frame design
- Algorithm development
- Trigger table design
- Performance evaluation



Current trigger table

- 4 charged channels
- 2 neutral channels
- 1 luminosity monitor channel

Back up

	No	触发道类型	触发道设置
Charged trigger channel	01	Charged final state with back-to-back characteristic	IfRBB == 0 && (tempEMCpair[x]>=1 || tempMDCpair>=1) && (((EMC_totalclusternumber[x]>=2 && MDC_TWtracknum[x]>=2) && (Barrelmatch_num[x]>=1 || Barrelmightmatch_num[x]>=1 || (Endcapmatch_num[x]>=1 && Endcapmatch_num[x]<=2 && Inner_Endcap_match_num[x]<2)))) && GTL_EMC_TotalEDep[x]>=EMC_totalEDepmidthreshold&&GTL_total_highcluster_EDep[x]<3
	02	Charged final state with few final states (signal track number≤2)	IfRBB == 0 && EMC_totalclusternumber[x]>=1 && EMC_totalclusternumber[x]<=4 && MDC_TWtracknum[x]>=1 && MDC_TWRetracknum[x]<=4 && (((Barrelmatch_num[x]+Endcapmatch_num[x]>=1||Barrelmightmatch_num[x]+Endcapmightmatch_num[x]>=2) && Inner_Endcap_match_num[x]<=1 && GTL_EMC_TotalEDep[x]>=0.15)) &&GTL_EMC_TotalEDep[x]<EMC_totalEDephighthreshold&&EMC_overhighEDepthreshold[x]<=1
	03	Charged final state with middle final states (3≤signal track number≤6)	IfRBB == 0 && (EMC_totalclusternumber[x]>=3 && EMC_totalclusternumber[x]<=7) && ((MDC_TWtracknum[x]>=3 && MDC_TWRetracknum[x]<=7 && (Barrelmatch_num[x]>=1 || Barrelmightmatch_num[x]>=1 || (Endcapmatch_num[x]>=1&&Endcapmatch_num[x]<=2 && Inner_Endcap_match_num[x]<=1)) && GTL_EMC_TotalEDep[x]>=EMC_totalEDeplowthreshold) || (MDC_TWtracknum[x]>=1&&(Barrelmatch_num[x]+Endcapmatch_num[x]+Barrelmightmatch_num[x]) >=1 && (GTL_EMC_TotalEDep[x]>=EMC_totalEDepmidthreshold) && MDC_TWRetracknum[x]<=3) || (Barrelmatch_num[x]+Endcapmatch_num[x]==0 && MDC_TWtracknum[x]>=2 && GTL_EMC_TotalEDep[x]>=0.6))
	04	Charged final state with massive final states (signal track number≥7)	IfRBB == 0 && (EMC_totalclusternumber[x]>=7 || MDC_TWRetracknum[x]>=7) && (Barrelmatch_num[x]>=1 || Barrelmightmatch_num[x]>=1 || (Endcapmatch_num[x]>=1 && Endcapmatch_num[x]<=2 && Inner_Endcap_match_num[x]<1)) && GTL_EMC_TotalEDep[x]>=EMC_totalEDeplowthreshold
Neutral trigger channel	05	Neutral final states	IfRBB == 0 && ((EMC_totalclusternumber[x]>2 && MDC_TWtracknum[x]<=1 && (EMC_BarrelEDep[x]>=0.4 || GTL_EMC_TotalEDep[x]>=0.6)) || (EMC_totalclusternumber[x]==2 && MDC_TWtracknum[x]<1 && (EMC_BarrelEDep[x]>=0.4 || (EMC_OuterEndcapEDep[x]>=0.5 && EMC_OuterEndcapEDep[x]<=1.4))) || (EMC_totalclusternumber[x]==1 && (EMC_BarrelEDep[x]>=0.5 || (EMC_OuterEndcapEDep[x]>=0.5 && EMC_OuterEndcapEDep[x]<=1.4))&&MDC_TWtracknum[x]<=1))&&GTL_total_highcluster_EDep[x]<3
	06	High Neutral Trigger	IfRBB == 0 && EMC_totalclusternumber[x]>=1 && GTL_EMC_TotalEDep[x]>=0.1
Luminosity monitoring trigger channel	07	Radiative Bhabha	((tempEMCRBBpair[x]>=1 || MDC_RBBcount==1) && MDC_TWtracknum[x]>=0 && MDC_TWRetracknum[x]<4 && (GTL_total_highcluster_EDep[x]>=3 || ((EMC_InnerEndcapEDep[x]>=1.5 || (EMC_InnerEndcapEDep[x]+EMC_OuterEndcapEDep[x])>=2.8) && EMC_BarrelEDep[x]<=0.2)) && (Barrelmatch_num[x]+Endcapmatch_num[x])<=3)
Random trigger channel			

Back up

No	Trigger criteria	Definition
		ECAL(簇团能量，簇团位置和数据片段定时信息)
02	ECAL_totalclusternumber	ECAL中的簇团数量>=1, >=2, >=3, >=7
03	ECAL_overEDepthreshold_clusternum	ECAL 中单个簇团能量沉积超过一定阈值的簇团数量
10	ECAL_TotalClusterEDep	ECAL 中的总能量沉积低(除少径迹道和高通过中性道为0.1外其他均为0.28)，中1(0.4)，中2(0.6)，高(3.5)四个阈值
12	ECAL_RegionEDep	ECAL桶部，外端盖，内端盖各自的总能量沉积
14	ECAL_btb	ECAL是否有背靠背簇团
11	ECAL_Total_high_EDep	ECAL中高能簇团(>0.6GeV)沉积的能量之和
		MDC(径迹数量，径迹位置和径迹定时信息)
04	MDC_totaltracknumber	MDC中的识别径迹总数>=1,>=2, >=3
05	MDC_totalretracknumber	MDC中的能够到达ECAL的径迹总数<=3,<=4,<=7
15	MDC_btb	MDC中是否有背靠背径迹
		Global(匹配信息)
06	Barrelmatch_num	桶部的匹配数量
07	OuterEndcapmatch_num	外端盖的匹配数量
08	InnerEndcapmatch_num	内端盖的匹配数量
09	Match_num	总的匹配数量
13	Non-match_num (Might_matchnum)	在空间维度(方位角，极角)没能完成匹配，但是在时间维度上能够与ECAL时间片段匹配的径迹数量
01	IfRBB	是否满足RBB道的触发条件