Status and Outlook of the CLock and Data Transmission System R&D for STCF

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Huangshan
Nov. 26, 2025

Outline

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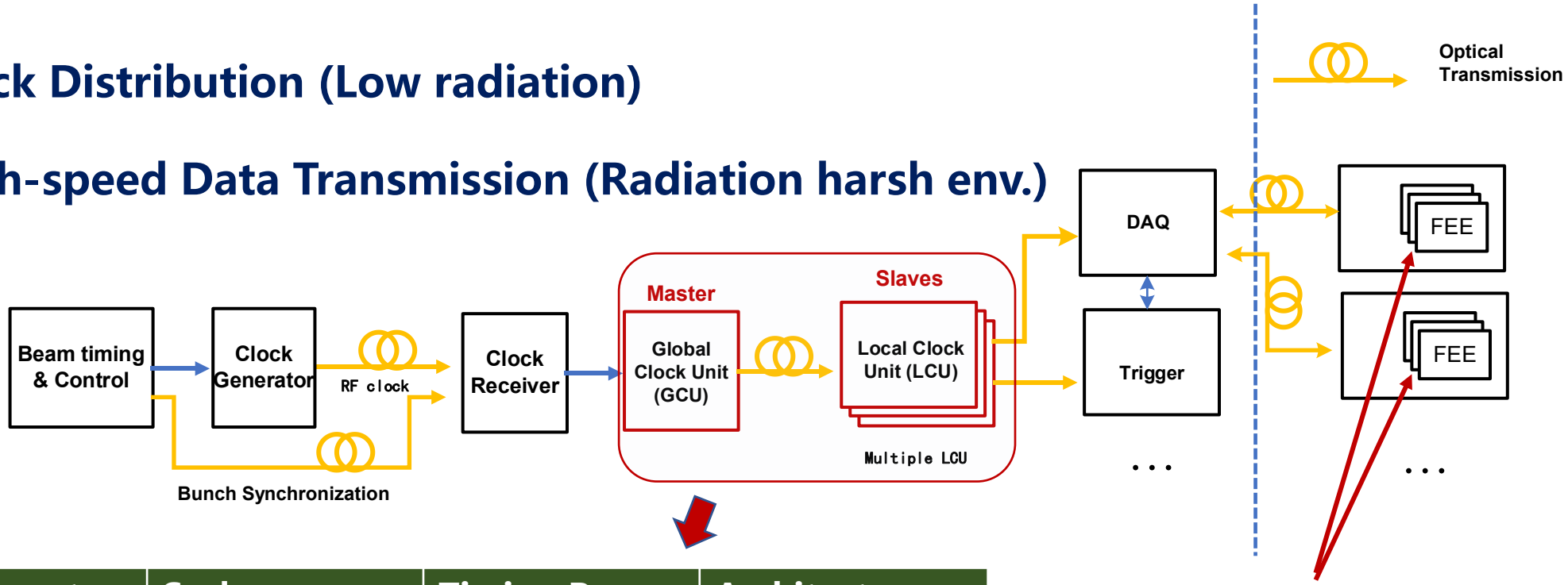
1. R&D Overview

- **Clock Distribution (Low radiation)**
- **High-speed Data Transmission (Radiation harsh env.)**



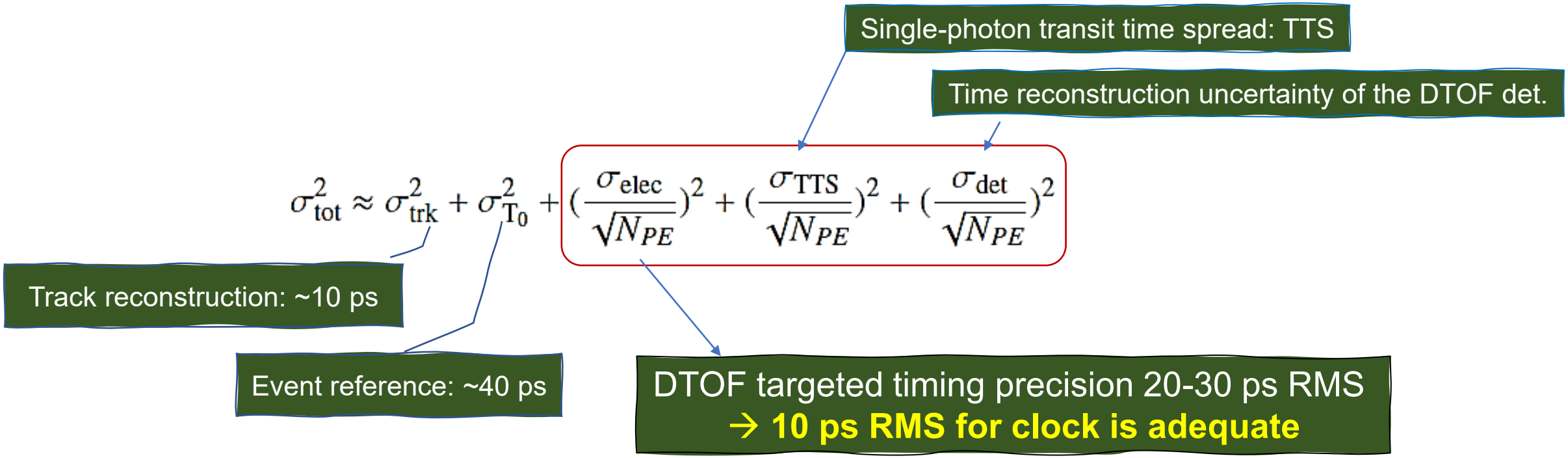
Experiments	Scale	Timing Req.	Architecture
BESIII	x100m	~ 10 ps RMS	Master/Slave
CEE	x100m	~ 5 ps RMS	Master/Slave
LHC/ATLAS	x10 km/x100m	~ 7 ps RMS	Encoding…
STCF	**x100m**	**~ 5 ps RMS**	**Master/Slave**

Custom ASIC on the FEE

- **Transceiver + Optical Links**
- **Uplink: 5-10 Gbps (5.12 Gbps typ.)**
- **Downlink: 1-2 Gbps (1.28 Gbps typ.)**

2. Clock Distribution

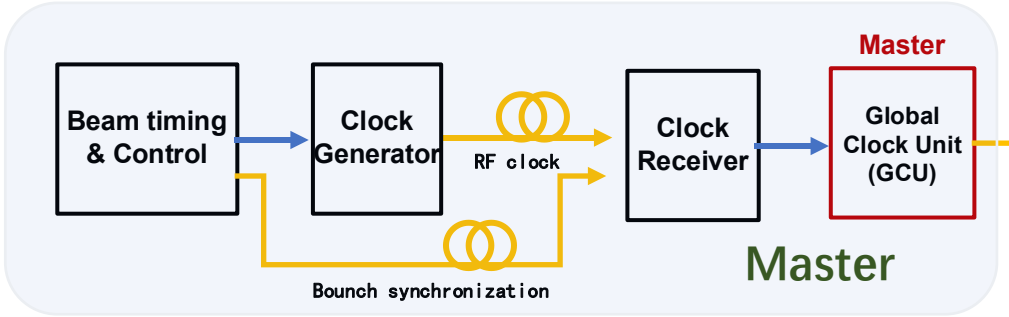
- **Requirement: 5 ps RMS**
- **Dictated by the most timing-stringent sub-system (e.g., DTOF)**

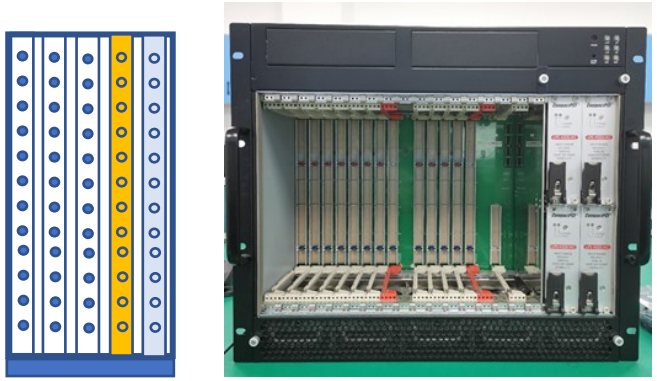


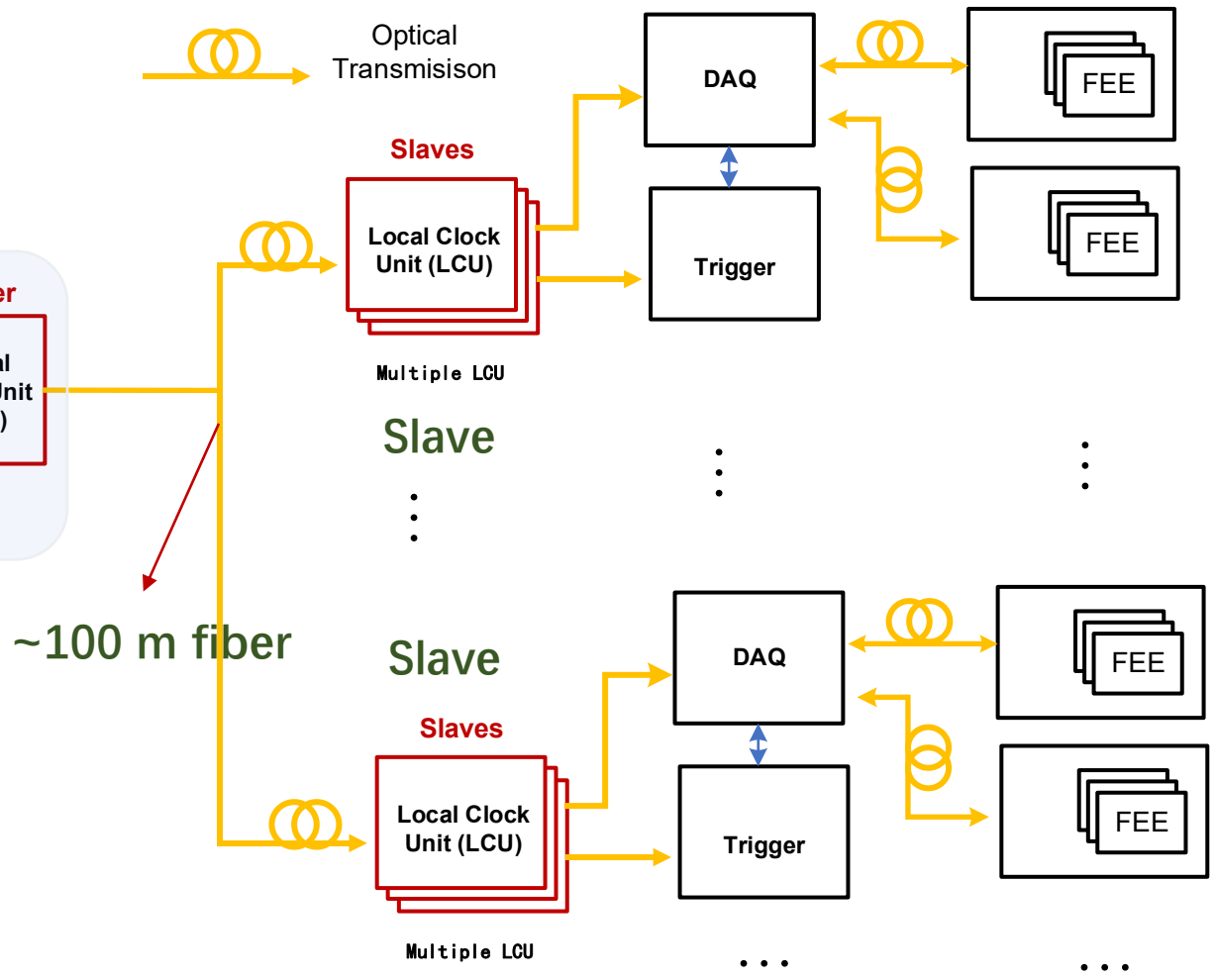
2. Clock Distribution

- **Master/Slave, star-distribution**

~ 500 MHz → 40 MHz



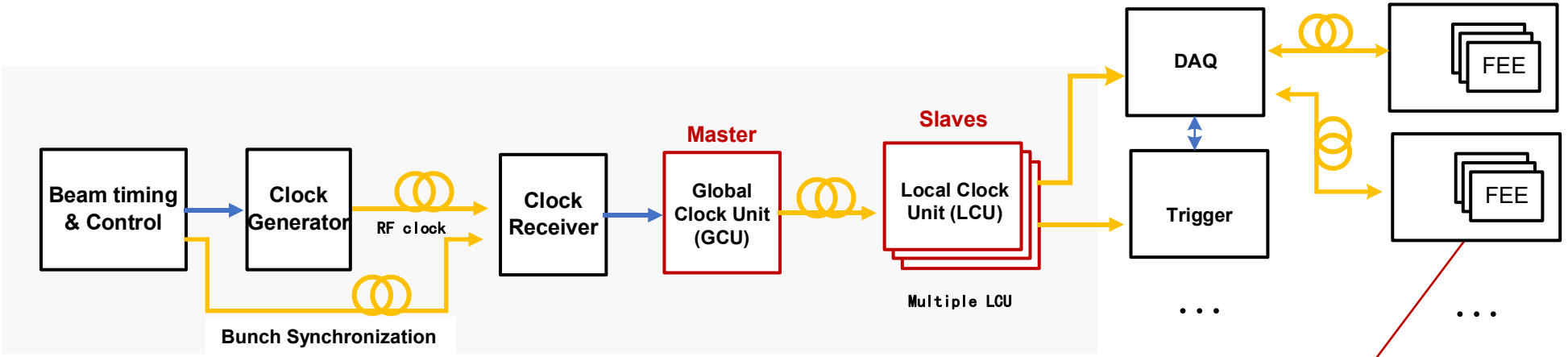




2. High-speed Data Transmission

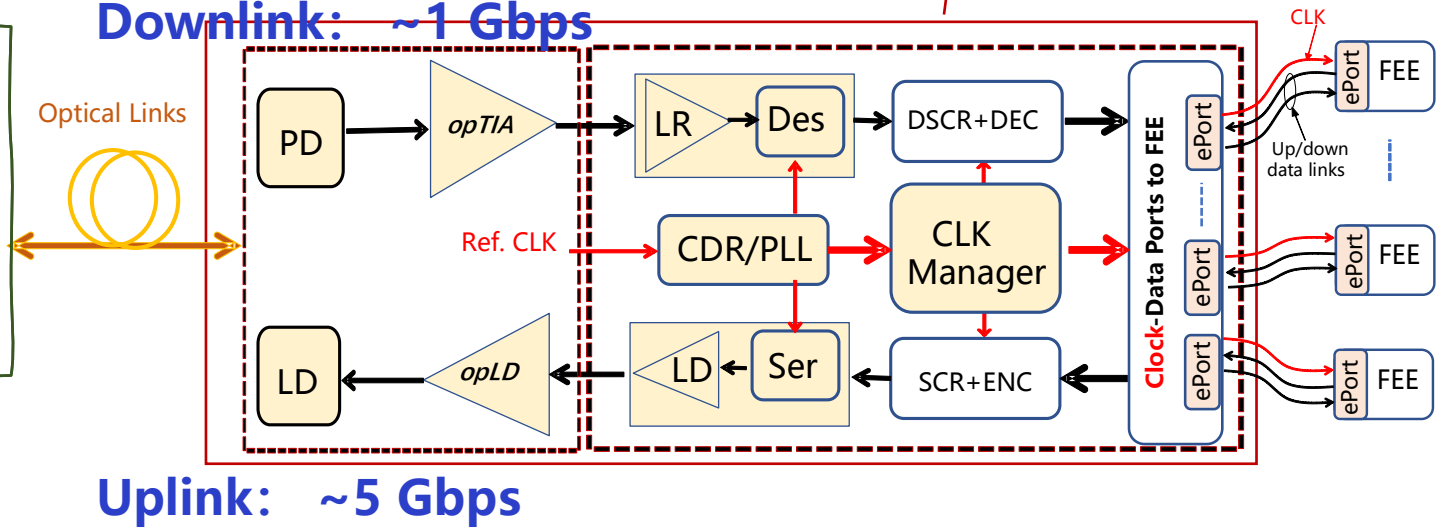
Optical Transmission

- **Radiation Tolerant Optical + Electrical Links**



Four key R&D techniques:

- → **Clocking**
  - CDR, PLL, Clock management
- → **Uplink**
  - SCR+ENC, SER, opLD+LD
- → **Downlink**
  - PD+opTIA, DES, DSCR+DEC
- → **Data Processor: e-ports, frame builder**



2. High-speed Data Transmission

- **Uplink~ 5 Gbps，Downlink ~ 1 Gbps**

Component	Num. of Channels	Ports Num. to DAQ	Readout Time Window(ns)	Data Rate of Payload After L1(GB/s) 1 / 2 / 3 / 5 (times of background)	Expected rate/port Gbps
ITK（Silicon）	1.62e9	35	1000	0.96 / 1.81 / 2.67 / 4.37	0.23/0.41/0.61/1.0
ITK (μRWELL)	10552	15	600	2.59 / 4.53 / 6.48 / 10.37	1.38/2.42/3.46/5.53
MDC	11520	360 → 23	800	0.99 / 1.59 / 2.18 / 3.37	0.34/0.55/0.76/1.17
MDC(Super small Cell)	19488	609 → 26	800	1.40 / 2.30 / 3.20 / 5.01	0.43/0.71/0.98/1.54
PID (RICH)	583200	12	200	0.49 / 0.58 / 0.67 / 0.85	0.33/0.37/0.45/0.57
BTOF	5760	90 → 6	100	1.18 / 1.29 / 1.41 / 1.65	1.57/1.72/1.88/2.2
PID (DTOF)	6912	108 → 7	100	0.72 / 0.80 / 0.88 / 1.03	0.82/0.91/1.01/1.18
ECAL	8670	32	400	1.40 / 2.48 / 3.56 / 5.73	0.35/0.62/0.89/1.43
MUC	13024+25280	8	600	0.48 / 0.69 / 0.91 / 1.34	0.48/0.69/0.91/1.34
FWDR				12	
Total (Max.)		126		7.76 / 12.10 / 16.44 / 25.13	

Uplink ~ 5 Gbps

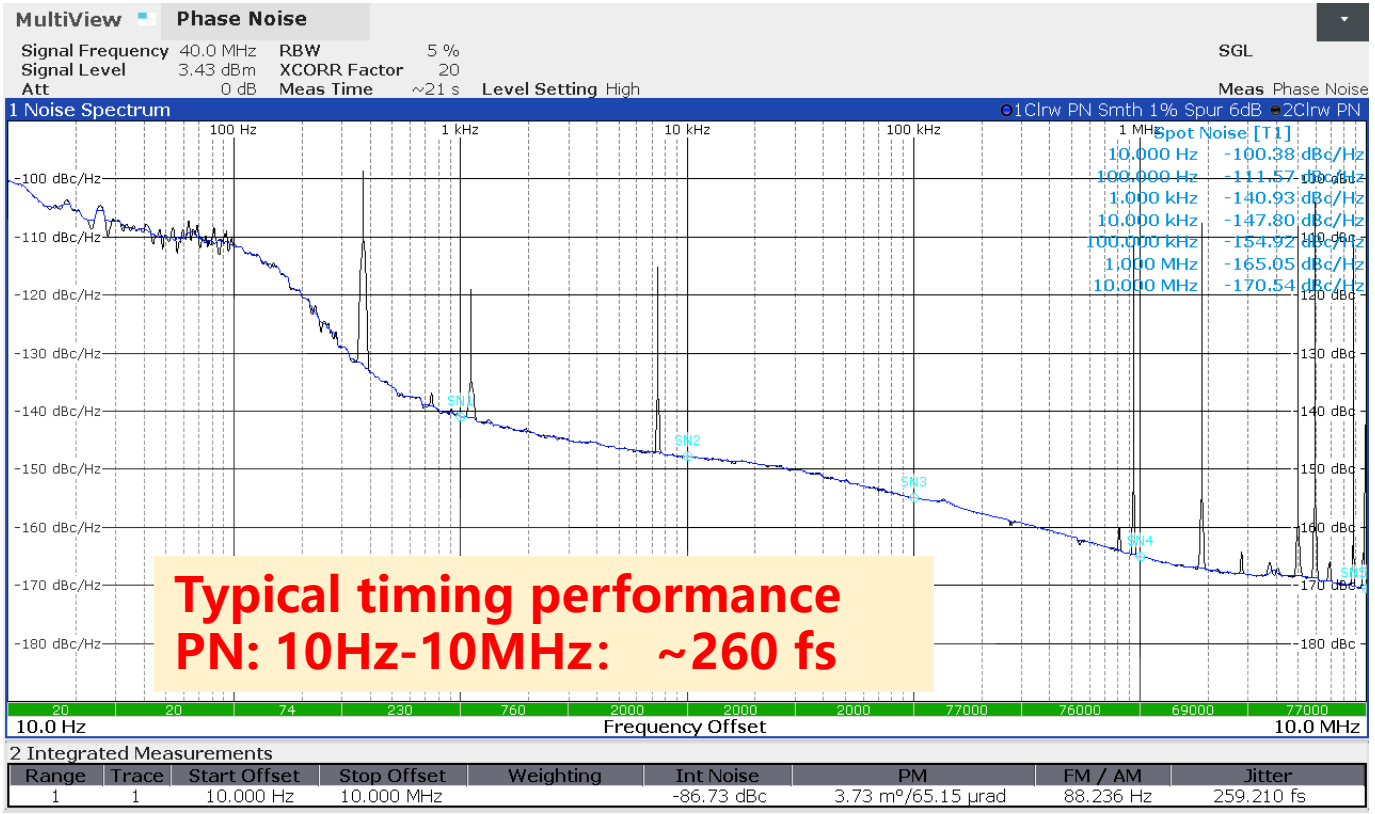
- *Reference, Junfeng Yang, "STCF HLT和计算存储专题讨论"*

- **CERN GBT ASICs:**
  - **GBT: Uplink 4.8 Gbps，Downlink 4.8 Gbps**
  - **lpGBT: Uplink 10.24 Gbps （max），Downlink 2.56 Gbps (max)**

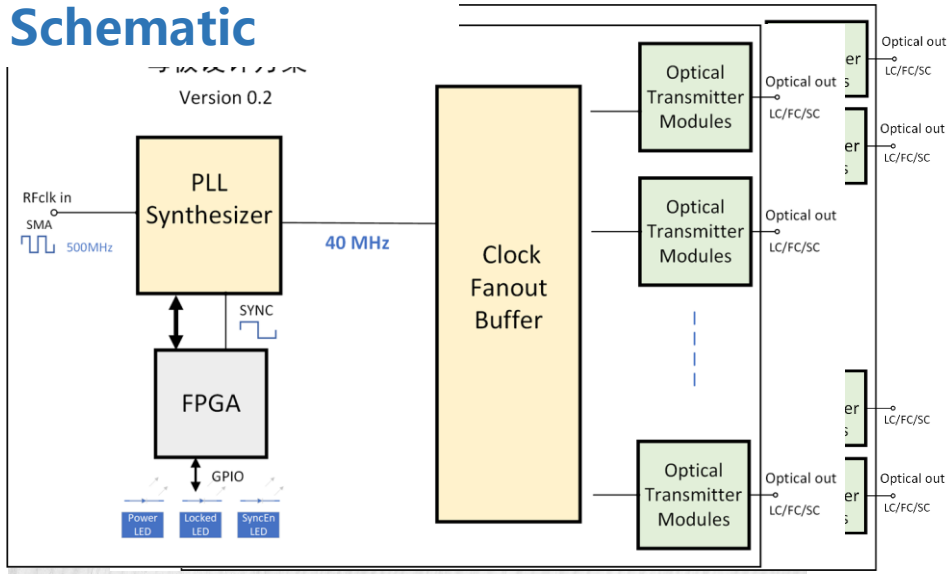
For configuration and control, etc…

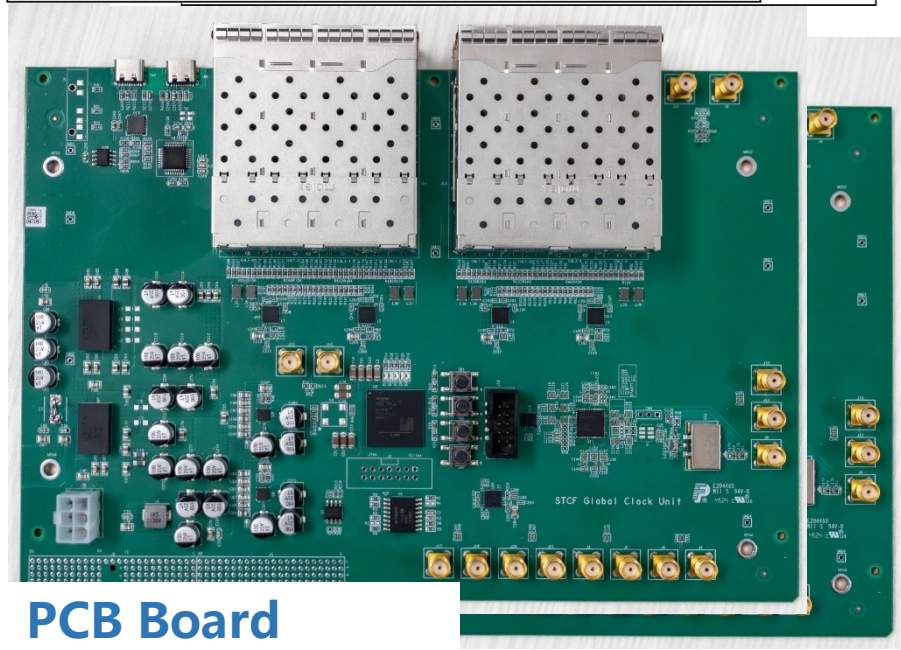
3. Progress: Clock Distribution

- ***Preliminary*** **Design and Evaluation Completed**



Schematic





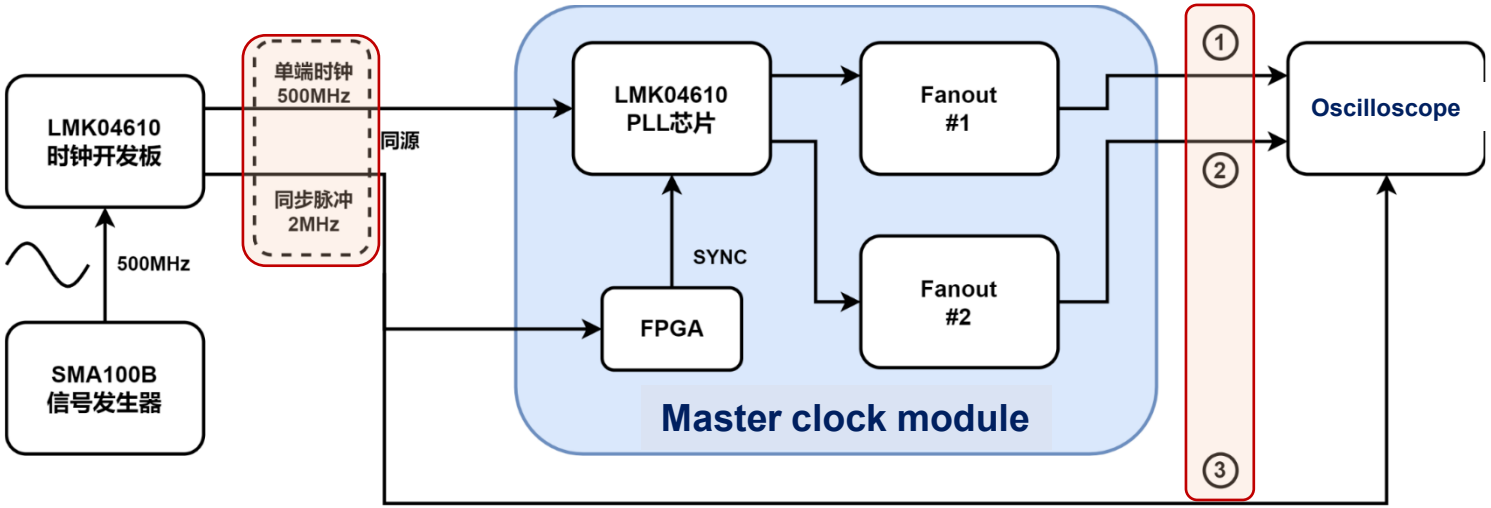
PCB Board

3. Progress：Clock Distribution

- **Beyond timing performance:**

  Relative phase stability among channels, upon pwr cycling

  - ①②：phase difference among output channels
  - ②③：phase difference between input (Syn.) and outputs



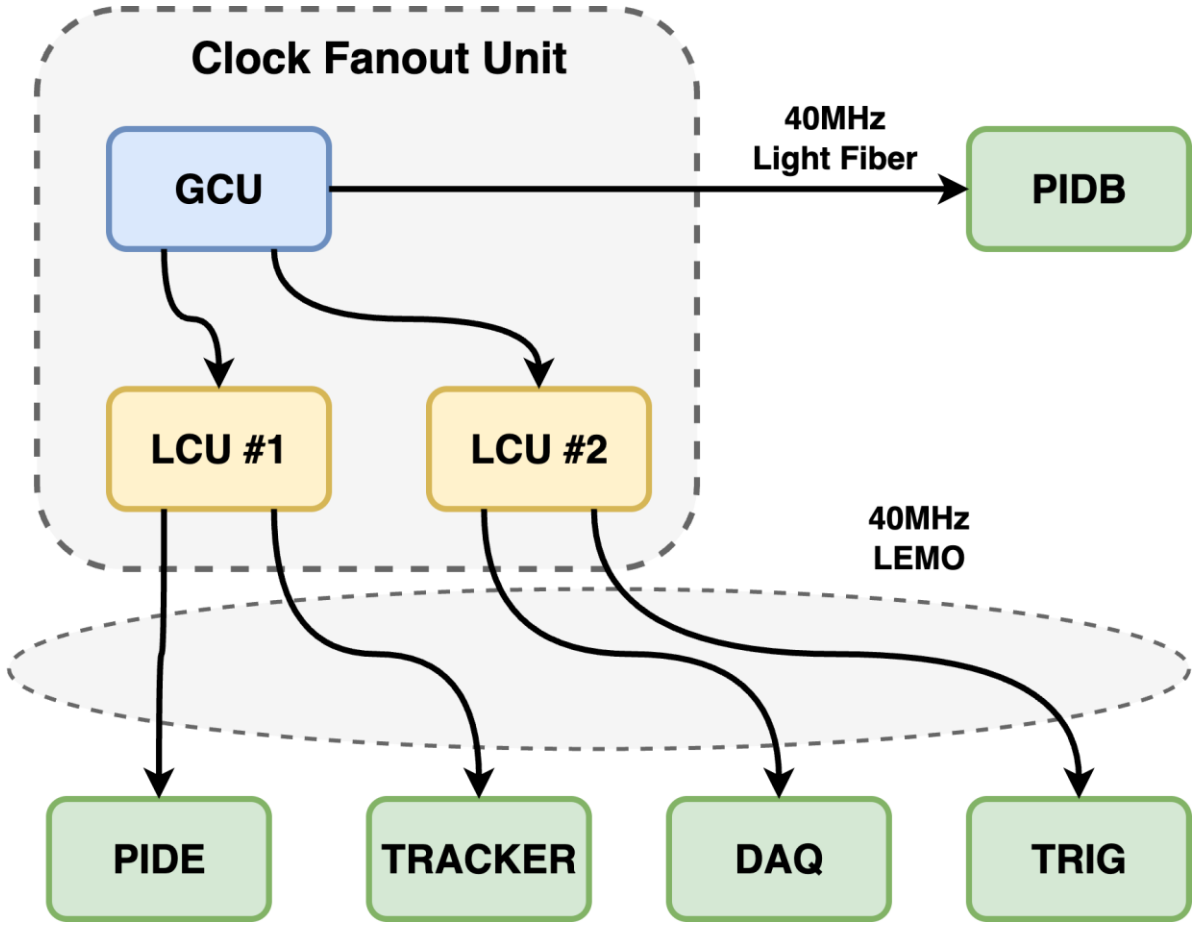
Power cycling	①② delay
#1	416.74ps
#2	416.75ps
#3	416.70ps

Max. 0.05ps

Max. 1.26ps

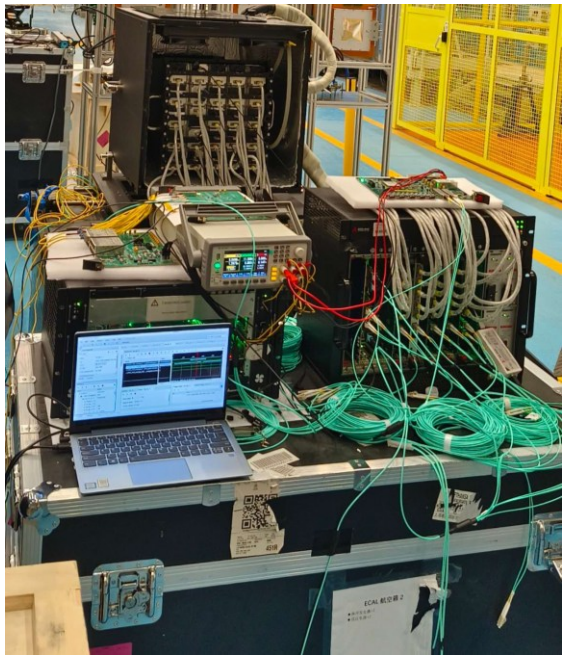
Power cycling	②③ delay
#1	737.30ps
#2	737.20ps
#3	738.46ps

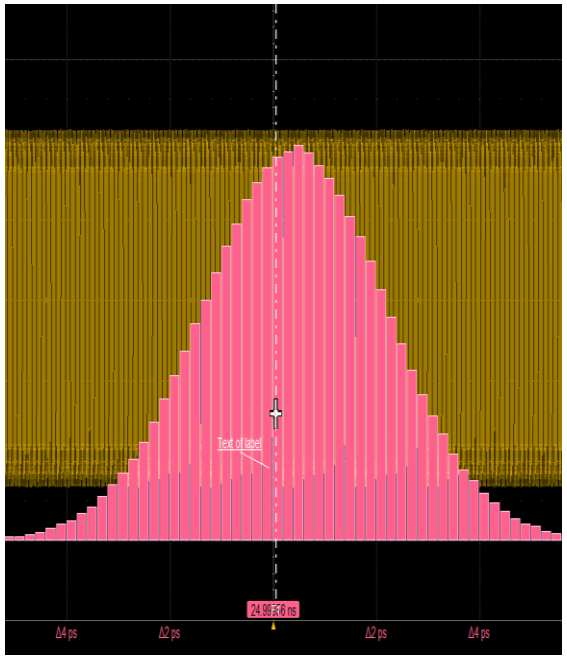
3. Progress: Clock Distribution



Joined detector beam tests at CERN

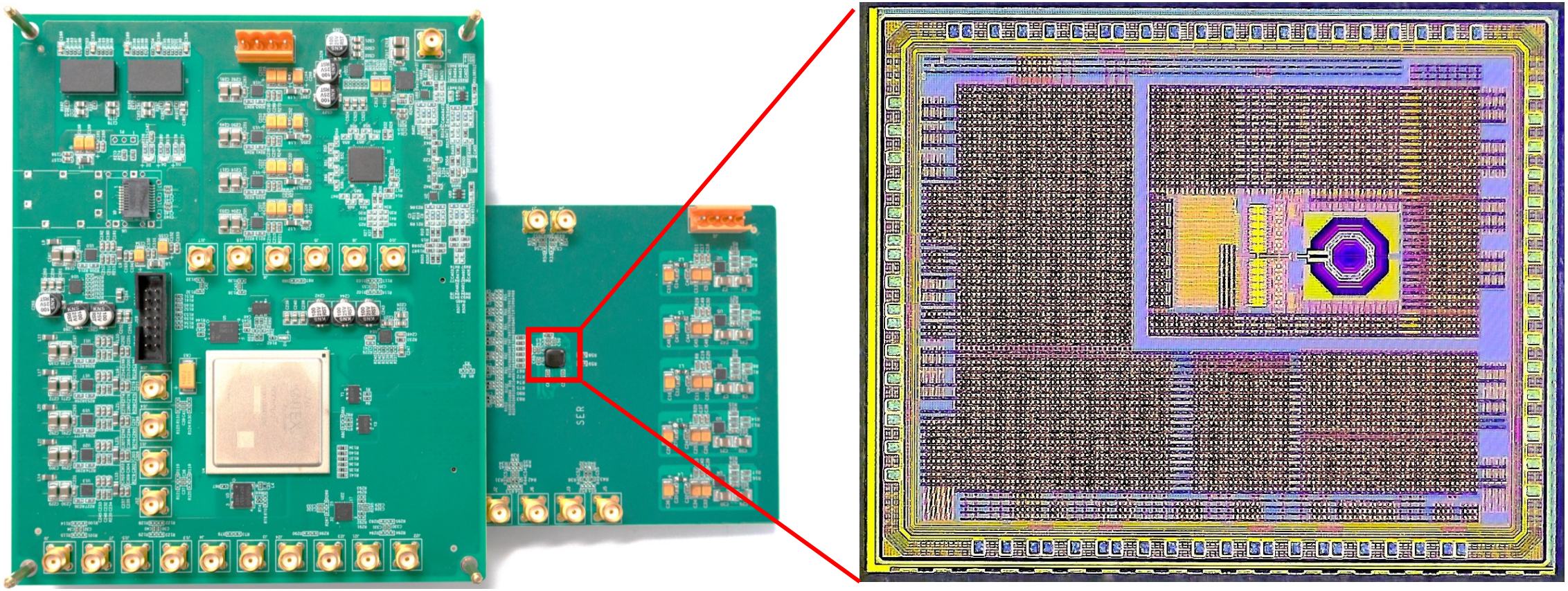
- **Clock Fanout Unit:**
  Global Clock Unit (GCU)
  Local Clock Unit (LCU)
- **Period jitter : 1.8 – 2.5ps (<5 ps RMS)**





3. Progress：High-speed data transmission

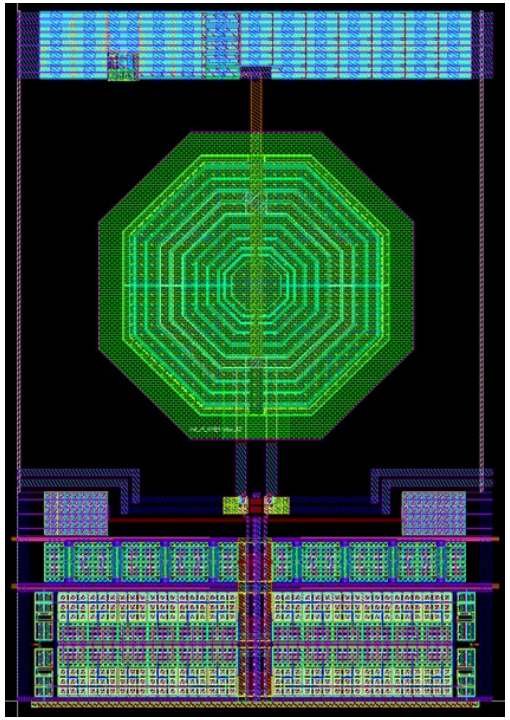
- ~5 Gbps serializer；5GHz clock manager (PLL)；CML/SLVS/LVDS I/Os



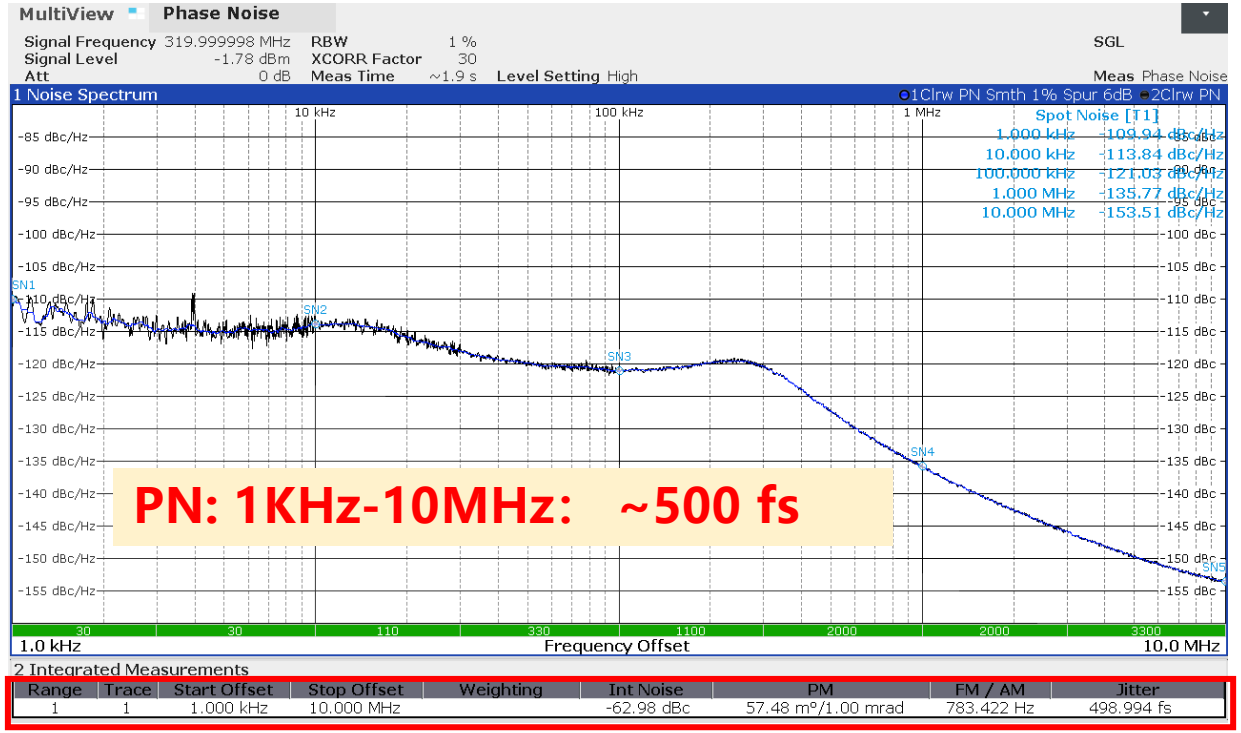
Wire-bonding ASIC Test board

3. Progress: High-speed data transmission

- 4-phase 2.56 GHz output (0/90/180/270), and divided clocks
- Timing performance: -135dBc/Hz @1MHz, jitter ~ 0.5 ps (1kHz-10MHz)

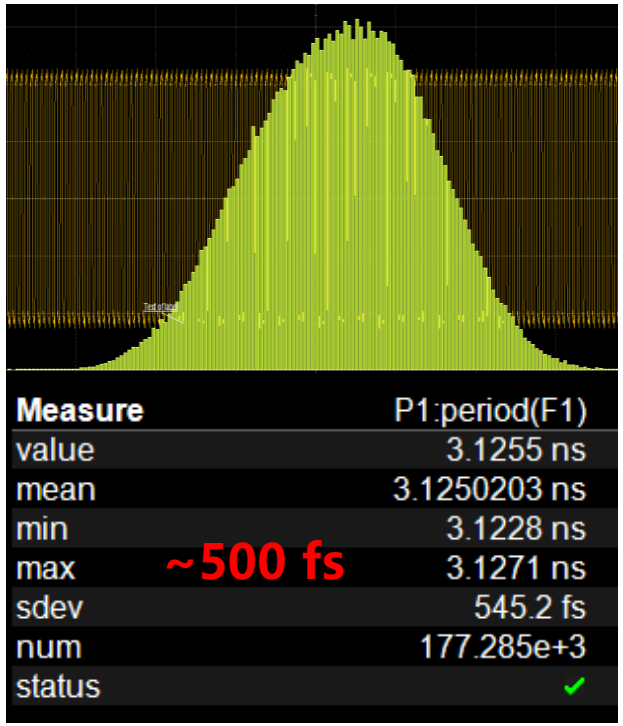


Clock Manager



PN: 1KHz-10MHz: ~500 fs

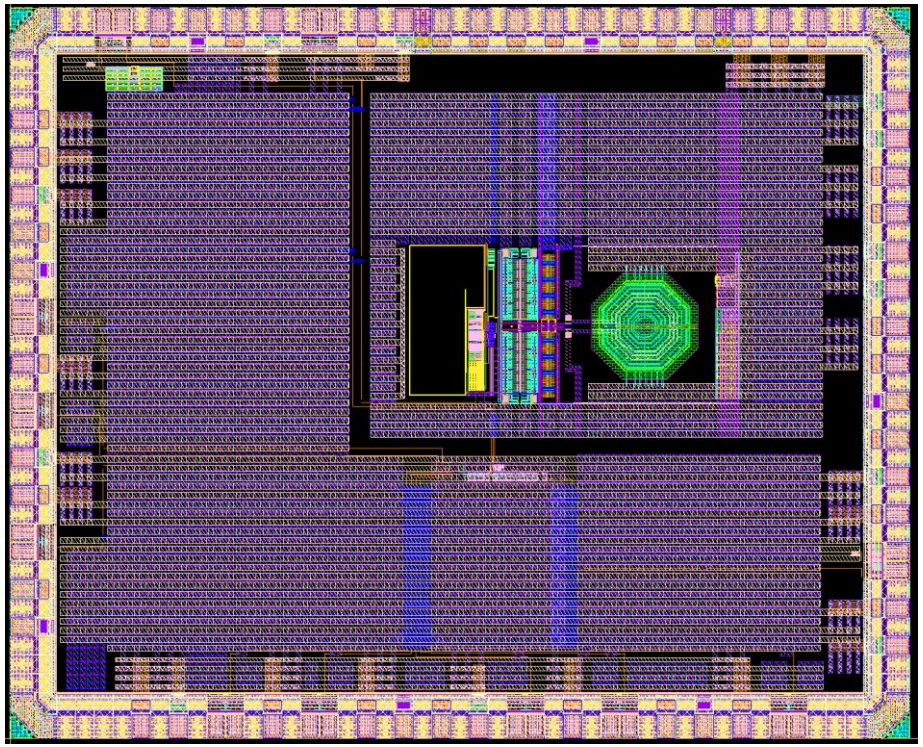
Phase Noise



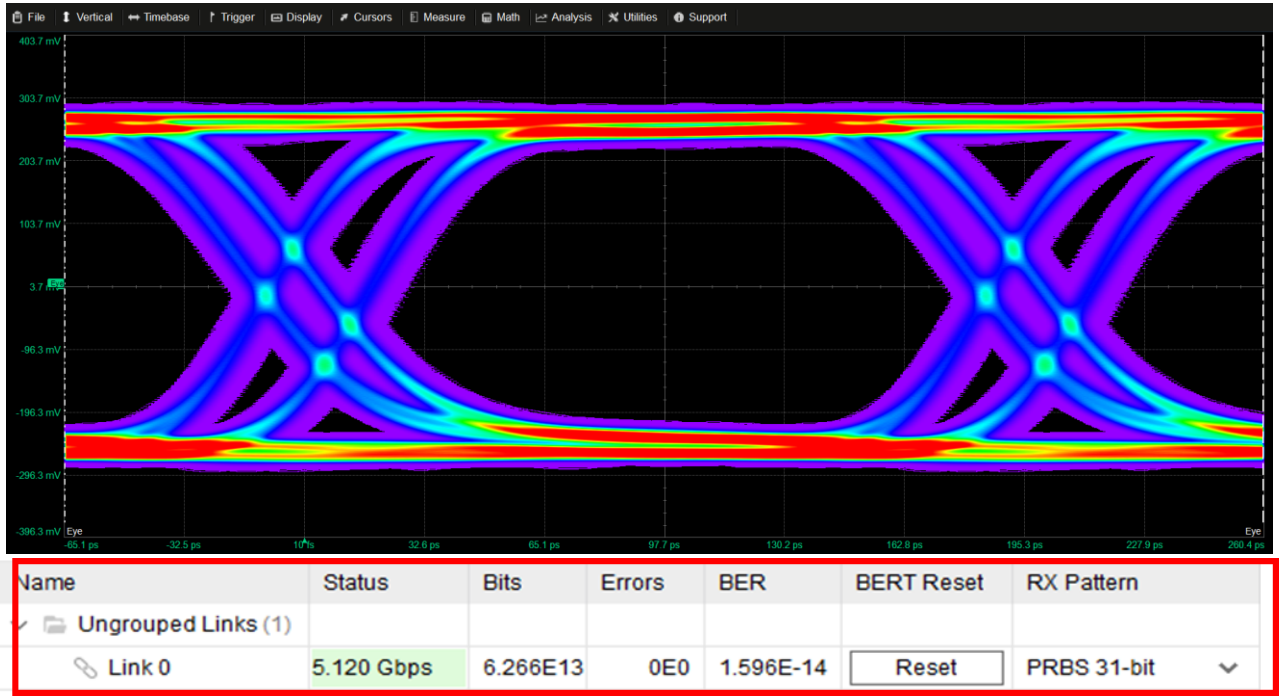
Period Jitter

3. Progress: 5.12 Gbps Serializer

- Targeted rate 5.12 Gbps, can be extended to 10.24 Gbps if required.



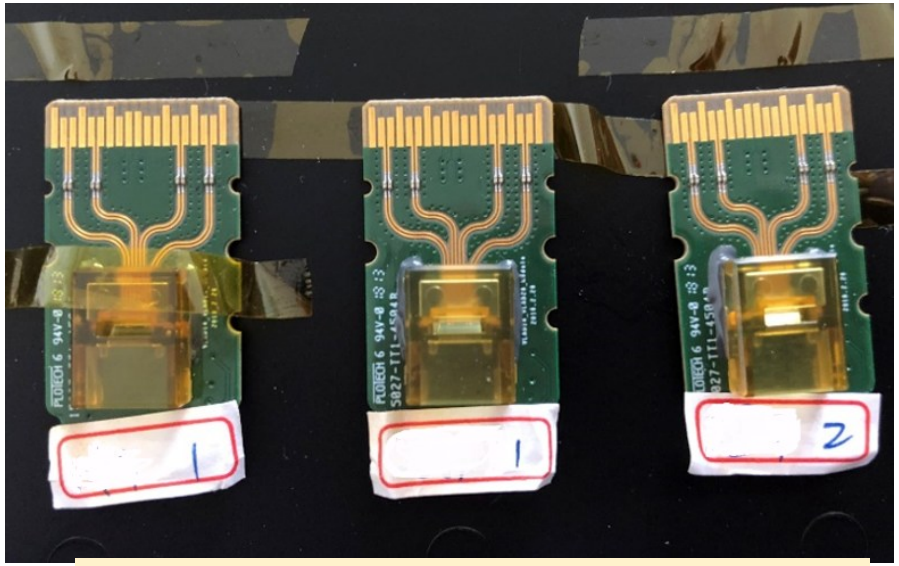
ASIC Prototype



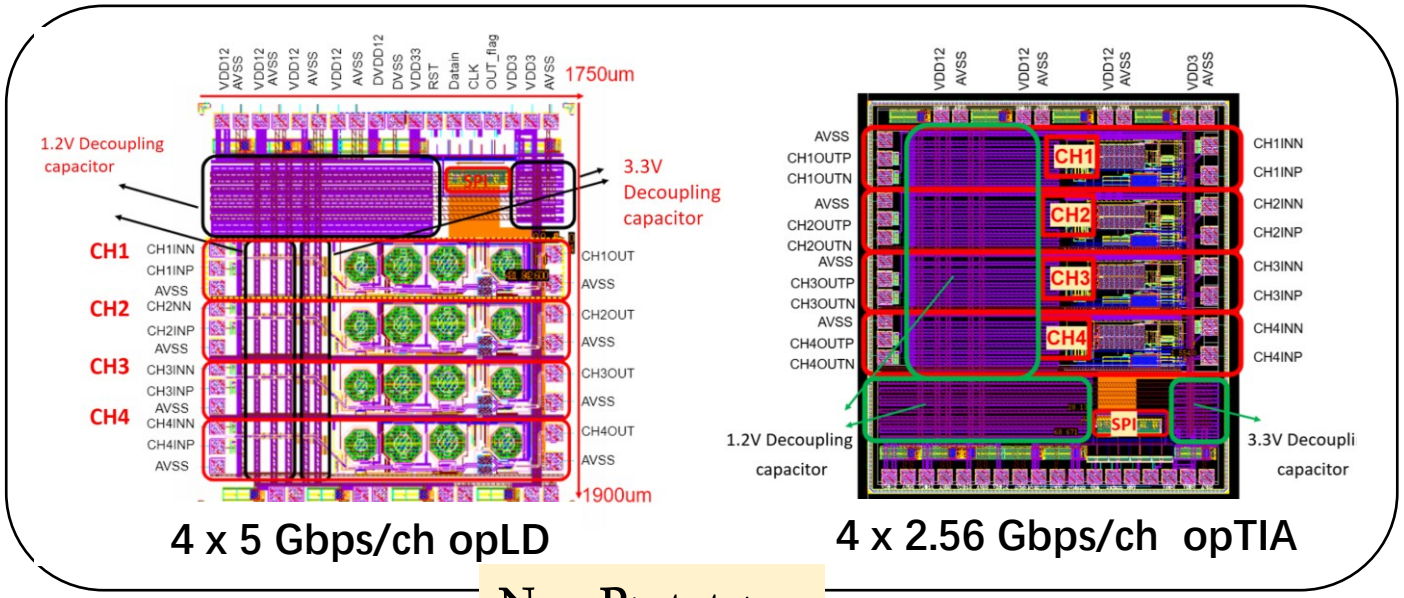
Name	Status	Bits	Errors	BER	BERT Reset	RX Pattern
Ungrouped Links (1)						
Link 0	5.120 Gbps	6.266E13	0E0	1.596E-14	Reset	PRBS 31-bit

Evaluation of serial transmission

3. Progress: Optical Links



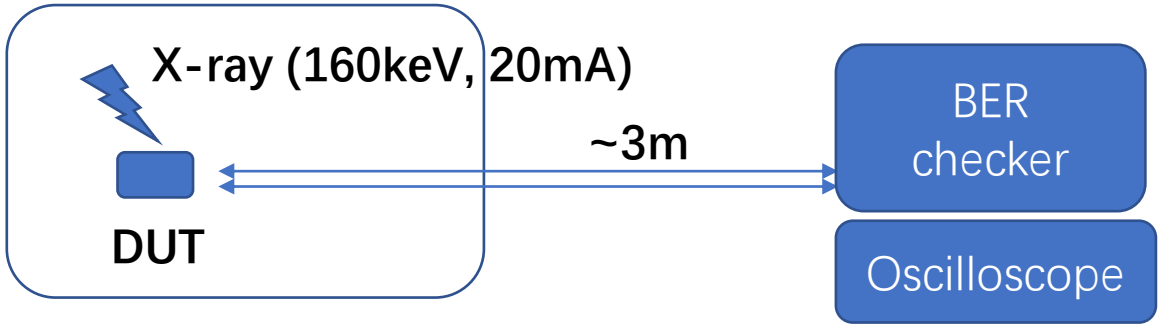
Existing opto-modules in 55nm CMOS

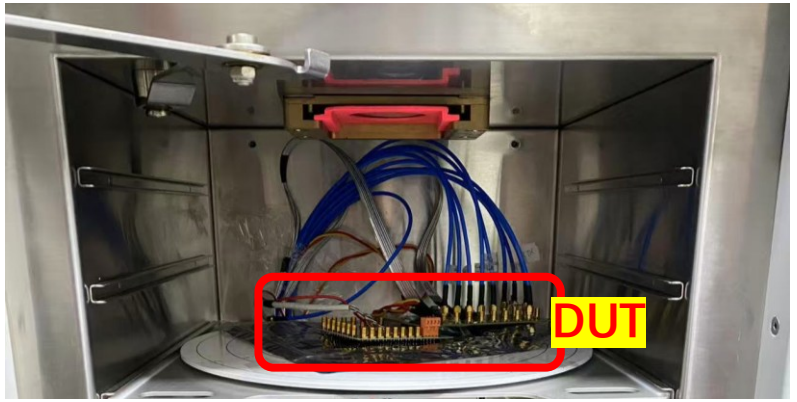


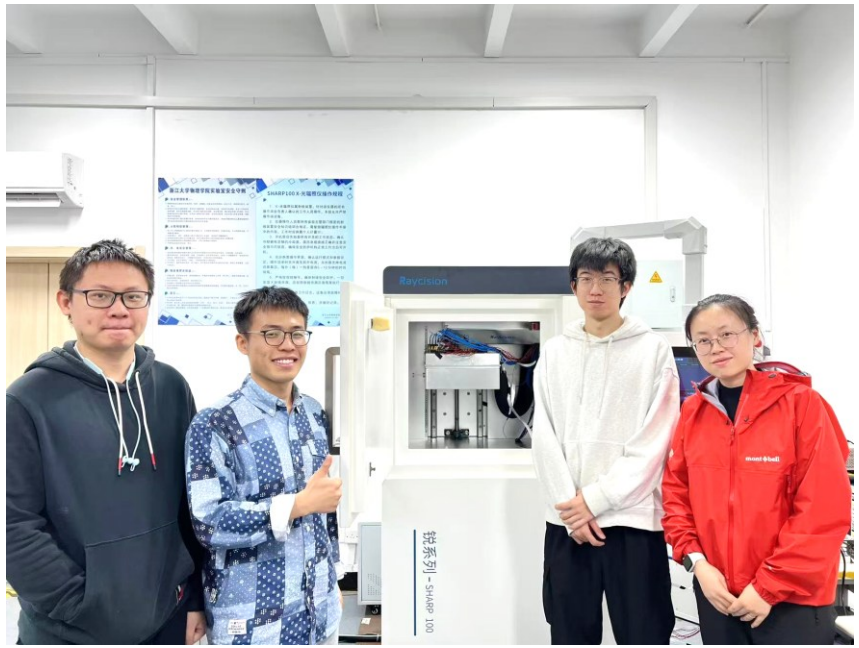
New Prototypes

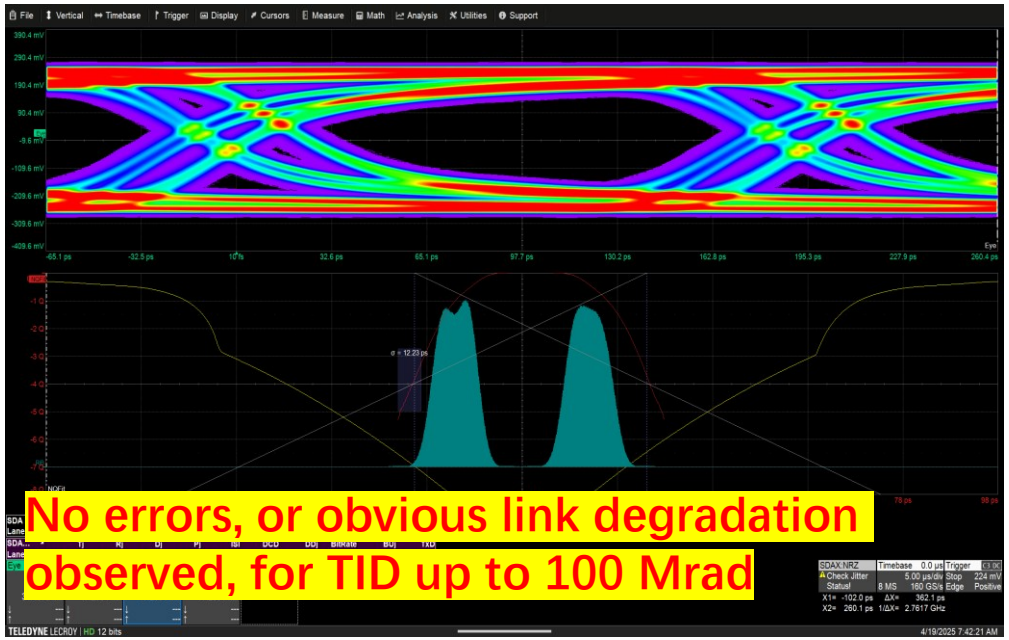
- opLD: 5-10 Gbps/ch (Tx), quad-channel array
- opTIA: 1- 2.56 Gbps (Rx), quad-channel array
- Updated prototype expected to return in Jan. 2026.

3. Progress: Radiation







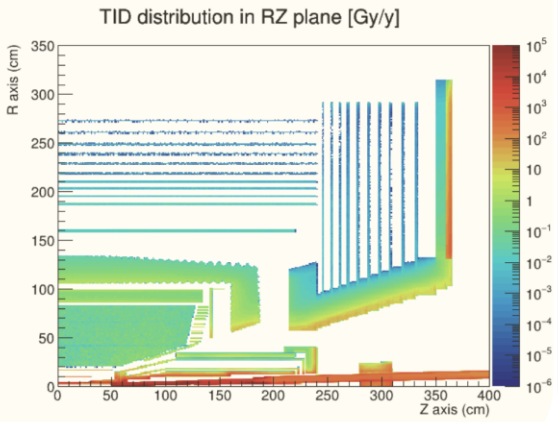


Acknowledging support from Prof. Hongbo Zhu' team @ Zhejiang University

3. Progress: Radiation

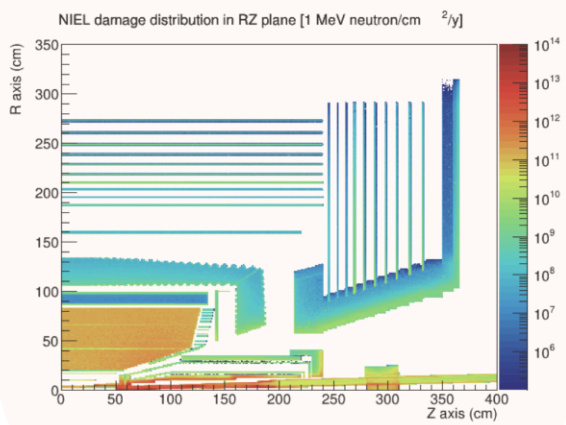
◆ Radiation expected in STCF detector areas

- The highest TID:
  12000Gy/y (ITKM)
  4300Gy/y (ITKW)
- Meets the requirement for a long-term run



Max. TID:
12 Mrad (10 y)

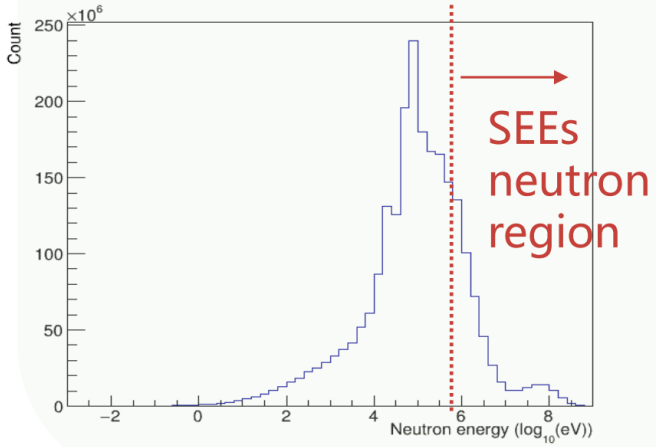
- The Highest NIEL ~1.7×10^{13} (MDC)
- The other parts smaller than $1.\times 10^{11}$
- NIEL is not quite important for MDCs (gas chamber)



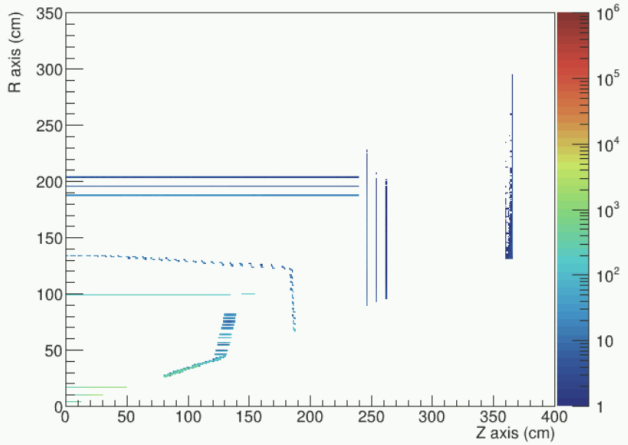
Not a concern for CMOS ICs

- Reference：Mingyi Liu, Yupeng Pei, Zhujun Fang, “Simulation of beam background on STCF”

Energy spectrum of background neutrons



SEES Neutron distribution (electronic system)

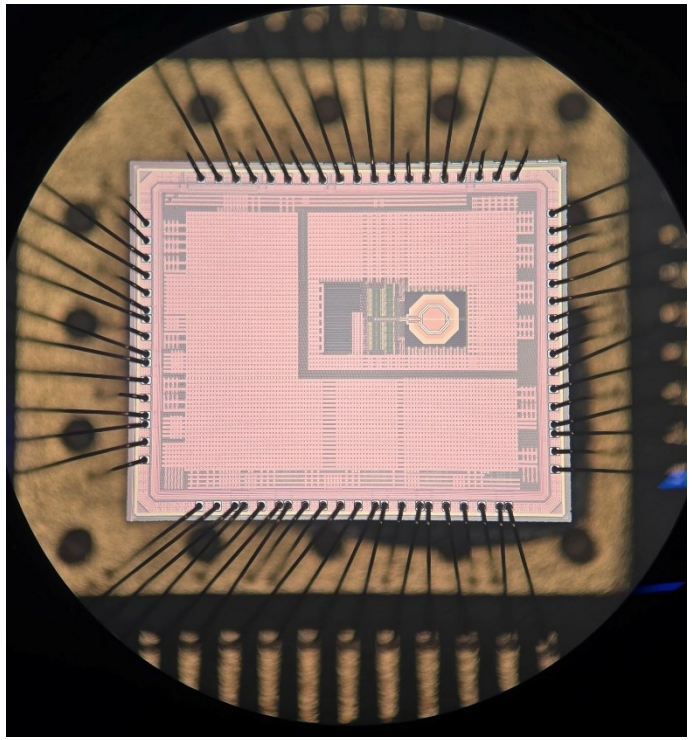


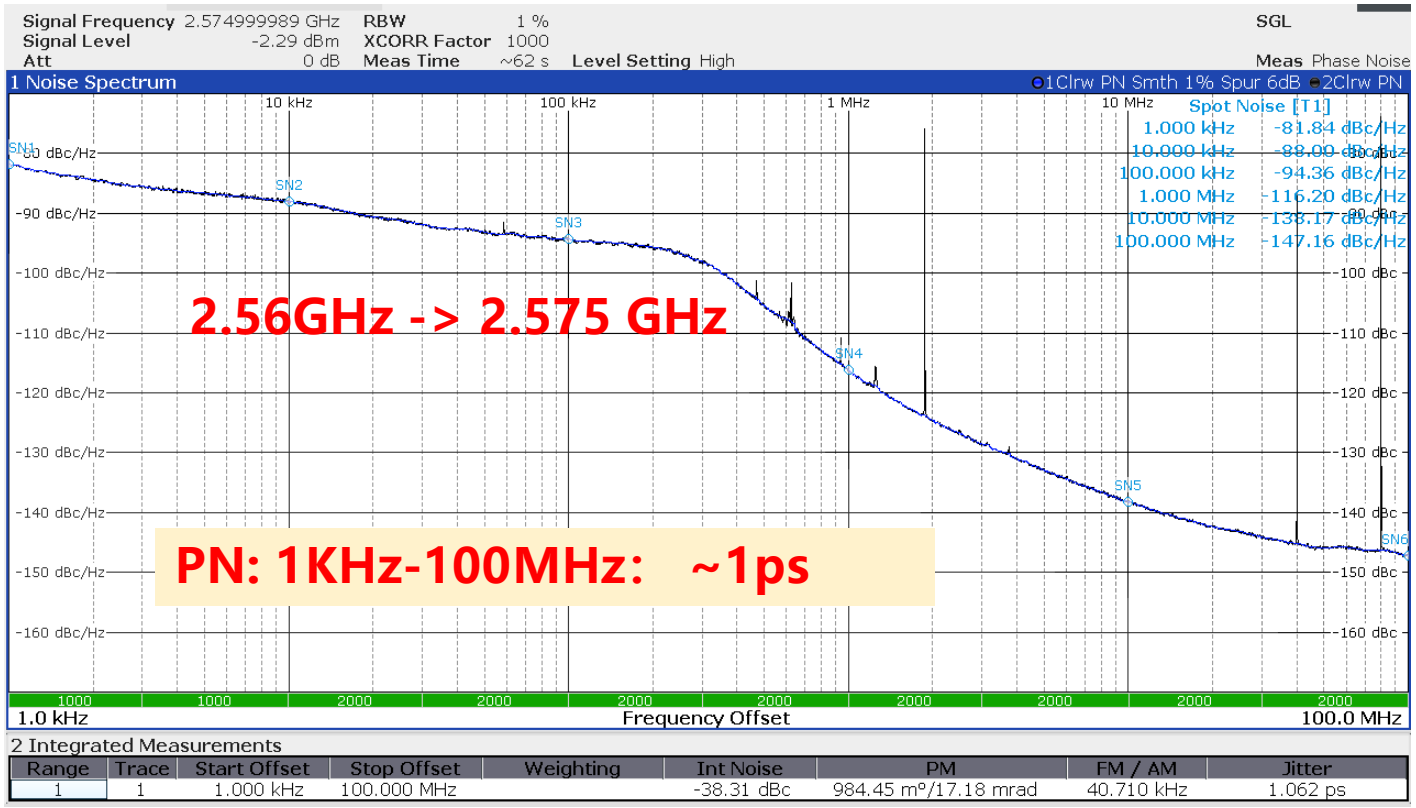
- **High neutron flux (~10^6 – 10^8 n/s)**
- **Wide energy spectrum (MeV – 100s MeV)**

SEE might be a concern

4. Outlook: Digital Clock Manager

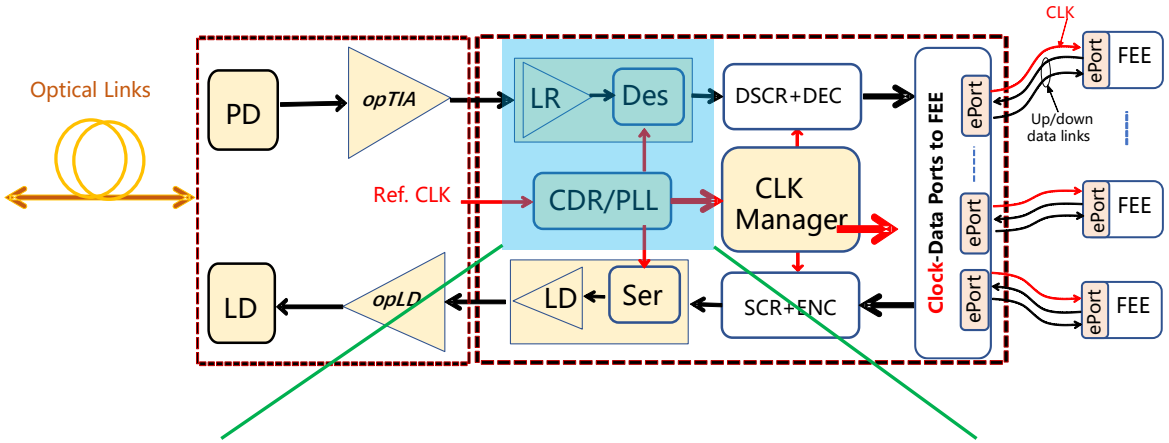
- Leveraging deep-submicron CMOS technology
- Flexibility of digital implementation (SEE management, design portability, etc. …)

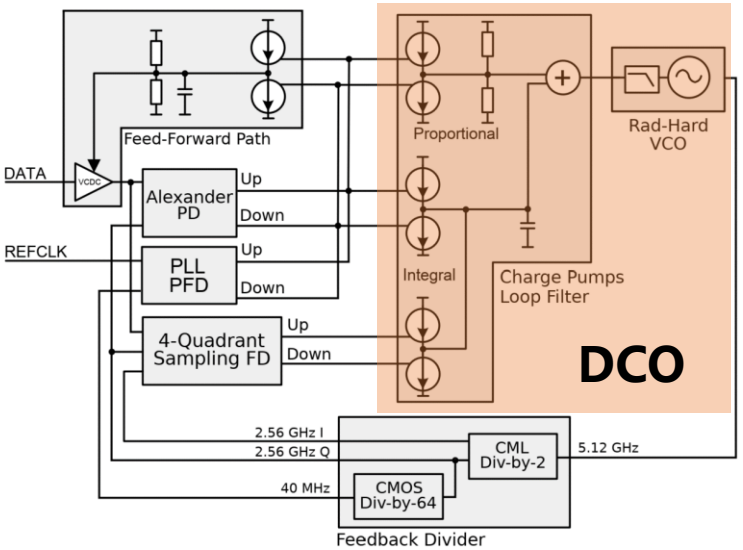


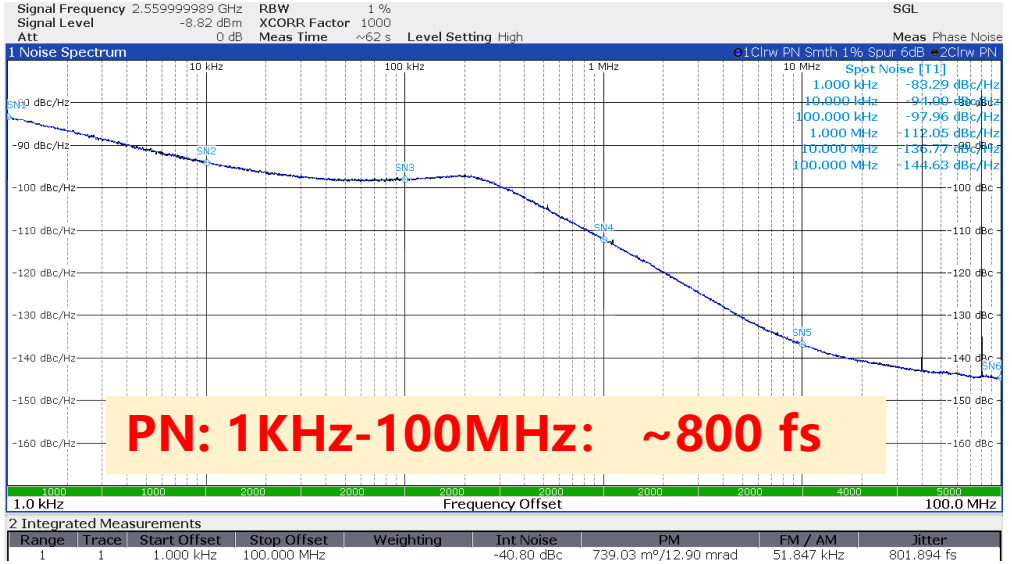


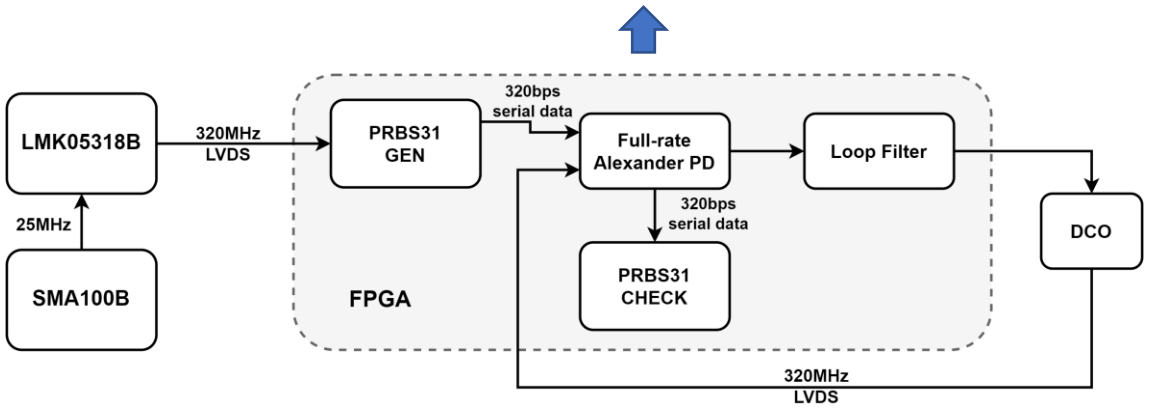
4. Outlook: Digital Clock Manager

- **Clock & Data Recovery**



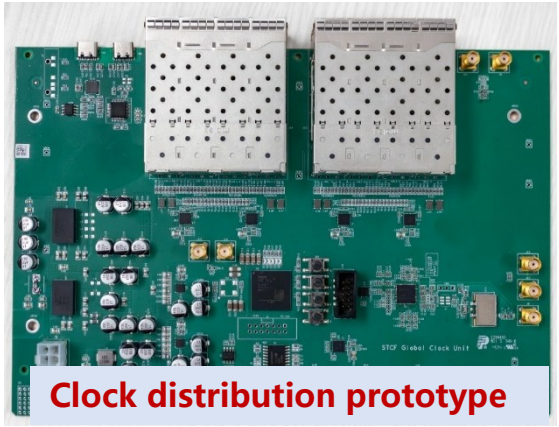




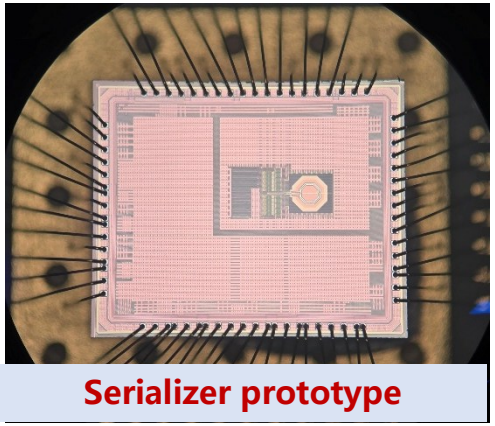


4. Summary

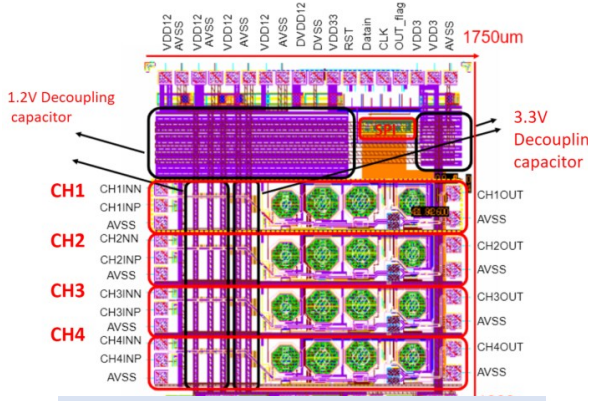
- Overall: CLDT R&D progressed as planned
- CLDT clock distribution: prototypes completed, joined detector beam tests @ CERN
- CLDT ASIC and optical modules: prototypes tested or submitted; initial radiation tests
- Follow-up tasks planned



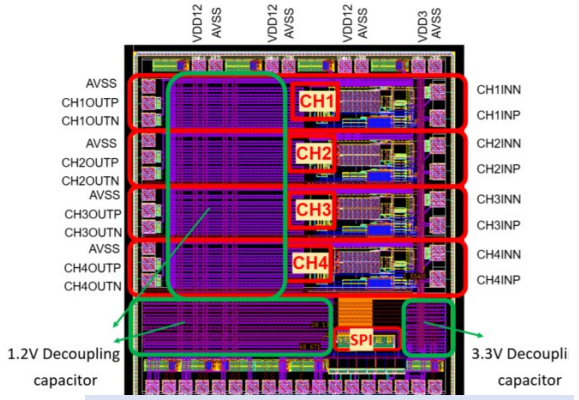
Clock distribution prototype



Serializer prototype



opLD prototype



opTIA prototype