On-the-Fly SEU Correction in FPGAs of the Aerogel RICH at Belle II

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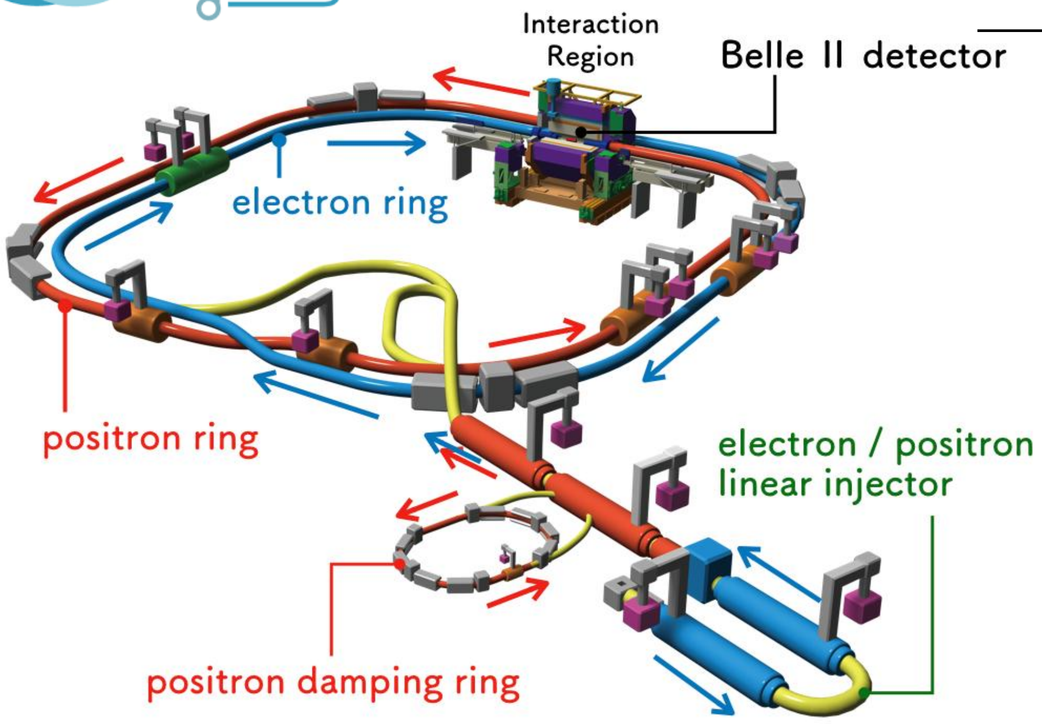
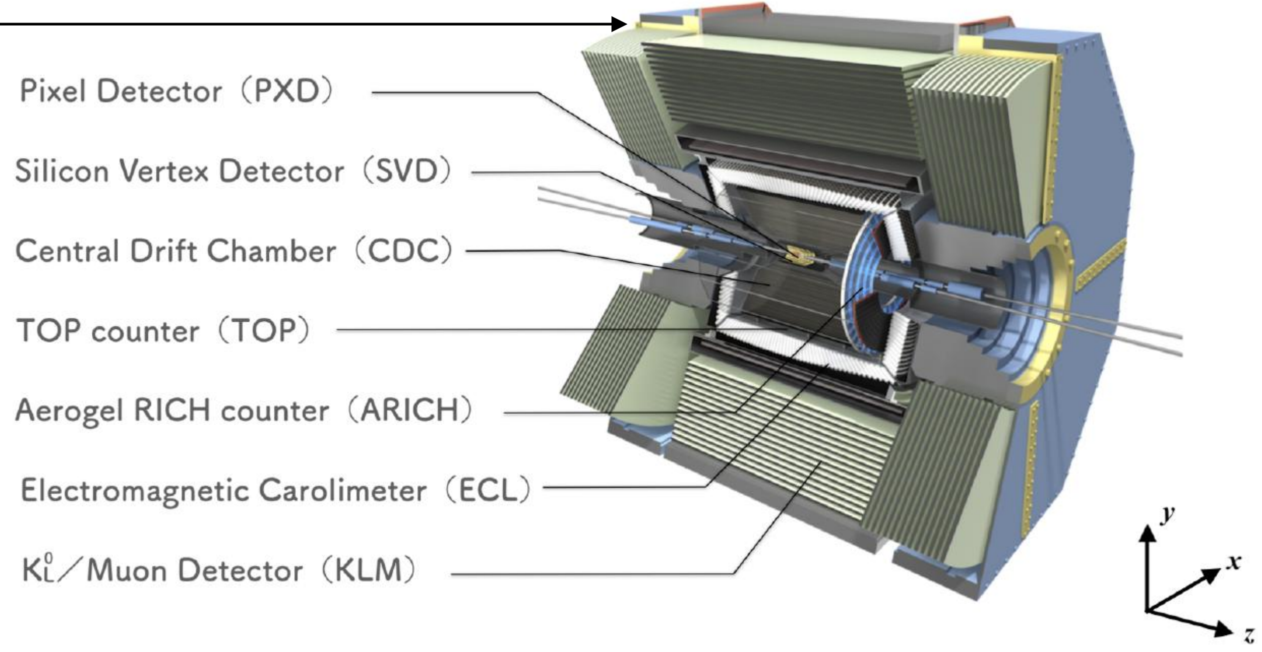
Outline

- SuperKEKB, Belle II and ARICH
- Single event upsets in ARICH front-end boards
- Configuration scrubbing solution and irradiation test
- FPGA-embedded SEU Monitors
- Summary

SuperKEKB and Belle II



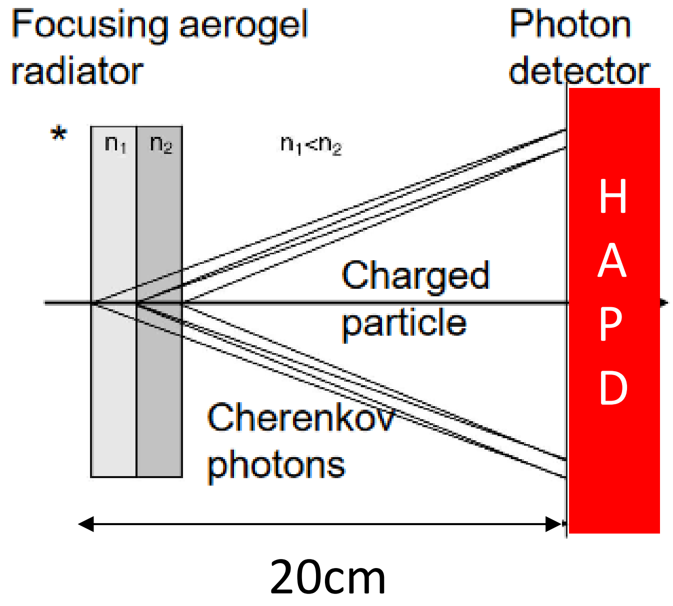


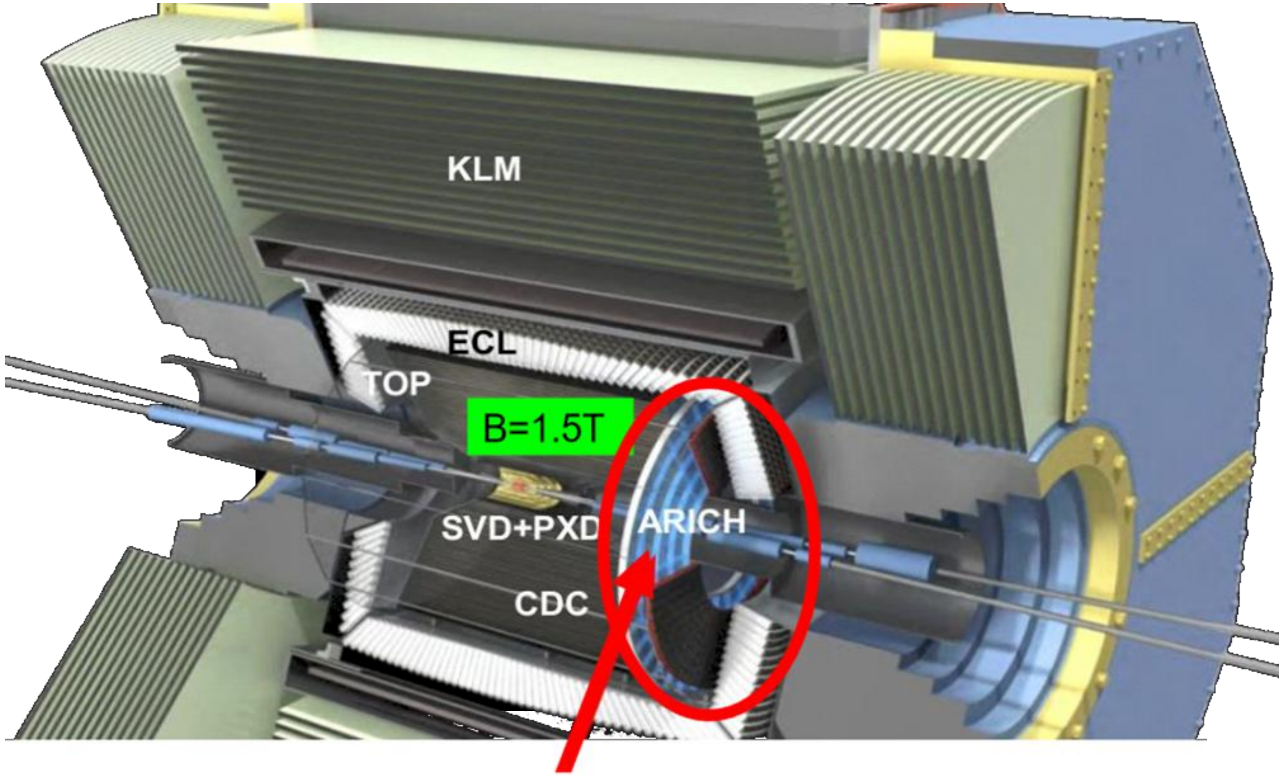
2013/July/29	LER	HER	unit
E	4.000	7.007	GeV
I	3.6	2.6	A
Number of bunches	2,500		
Bunch Current	1.44	1.04	mA
Circumference	3,016.315		m

- SuperKEKB e$^+$e$^-$ B factory @ KEK (Tsukuba, Japan)
- e$^+$ 4 GeV (LER), e$^-$ 7 GeV (HER)
- Target L= 6 × 10^{35} cm^{-2} s^{-1}
- Belle II detector at beam collision point
- Physics beyond the Standard Model at the intensity frontier (CKM matrix elements, CPV studies, rare B,D, τ decays and more)

Aerogel Ring Imaging CHerenkov Counter

- Goals
  - Particle Identification in end cap
  - K/π separation > 4σ in momentum range 1-3.5 GeV/c
- Requirements
  - operation in 1.5T magnetic field
  - limited space ~280 mm
  - radiation hardness
    - 1MeV eq. neutron fluence: 10^{12} n/cm^2
    - Total ionizing dose: 1 kGy

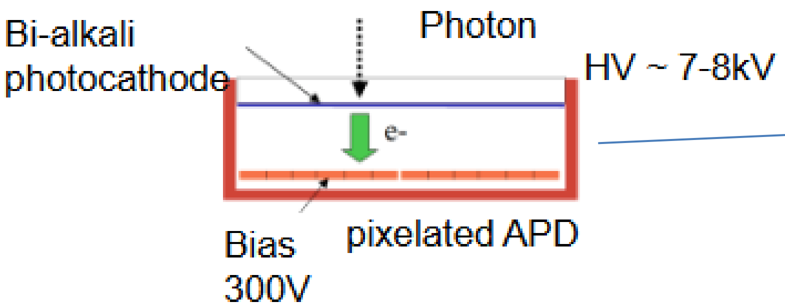


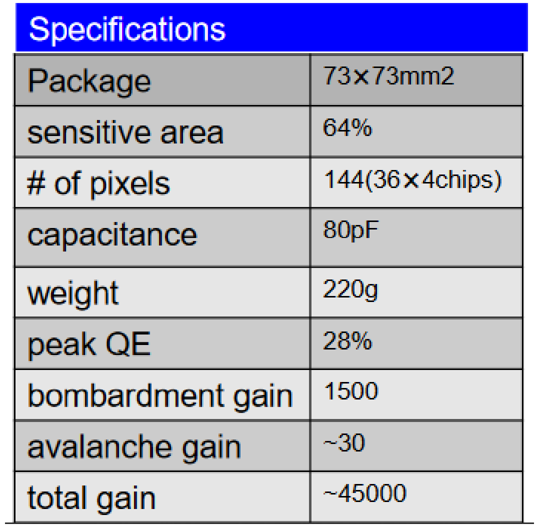


- Proximity focusing aerogel RICH
  - <n> ≈ 1.05
  - θc(π) ≈ 307 mrad@ 3.5 GeV/c
  - θc(π) –θc(K) = 30 mrad@ 3.5 GeV/c
  - pion threshold 0.44 GeV/c, kaon threshold 1.54 GeV/c

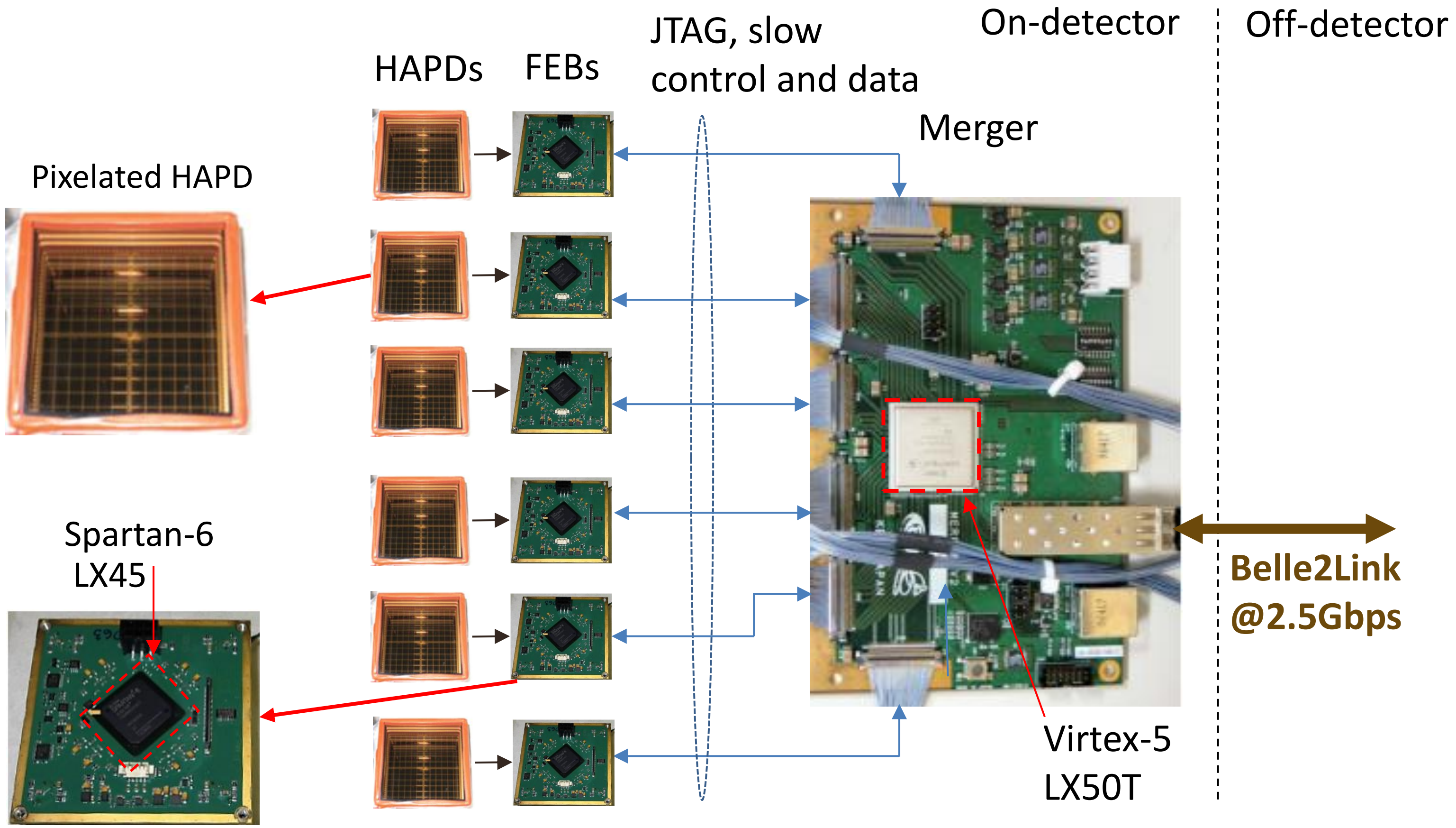
Photon Detector & Readout Electronics

- 420 x 144-channel Hybrid APDs
  - Custom design with Hamamatsu





Specifications	
Package	73×73mm2
sensitive area	64%
# of pixels	144(36×4chips)
capacitance	80pF
weight	220g
peak QE	28%
bombardment gain	1500
avalanche gain	~30
total gain	~45000



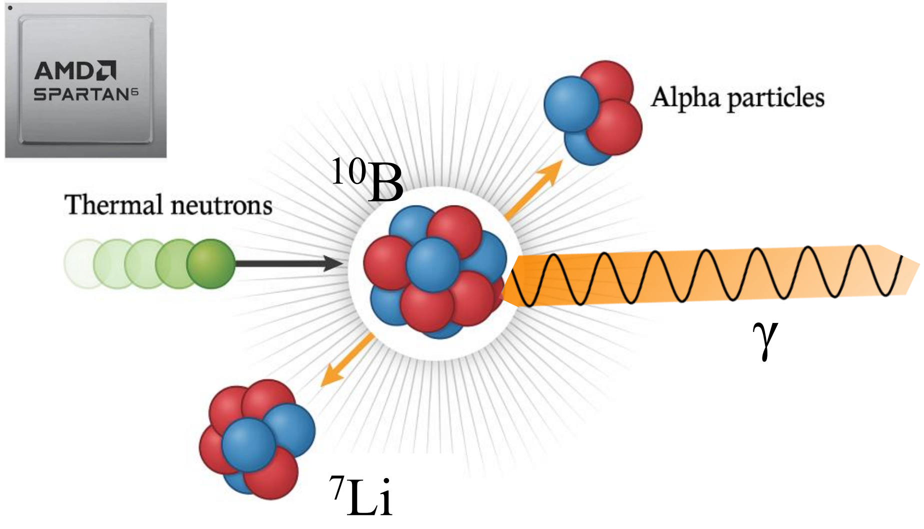
5-6 Front-end Boards (FEBs) per Merger

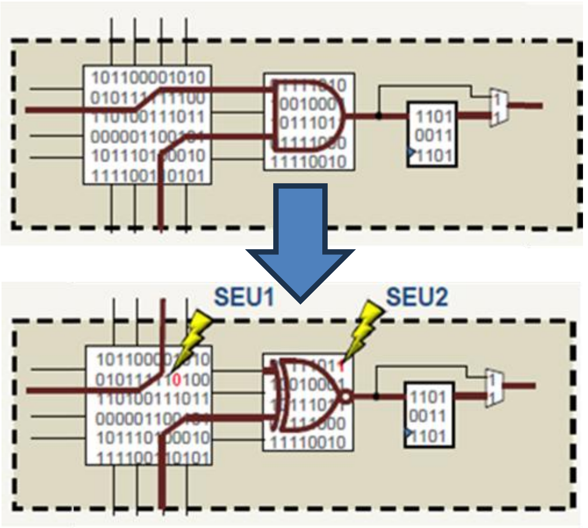
- Mergers aggregate data from FEBs, transmit them over Belle2Link, and manage FPGA configuration via JTAG

Configuration SEUs in FEB FPGAs

- Background neutrons at SuperKEKB Interaction Region
- Spartan-6 devices use Boron as p-type dopant
- ^{10}B (20%) has a high σ for thermal neutron capture => single event upsets (SEUs) in configuration SRAM

$$\left.\begin{array}{ll} {}^{10}\mathrm{B}+n \rightarrow {}^{7}\mathrm{Li} + \alpha + \gamma & (94\%) \\ \rightarrow {}^{7}\mathrm{Li} + \alpha & (6\%) \end{array}\right\} \text{3.5 kbarns}$$



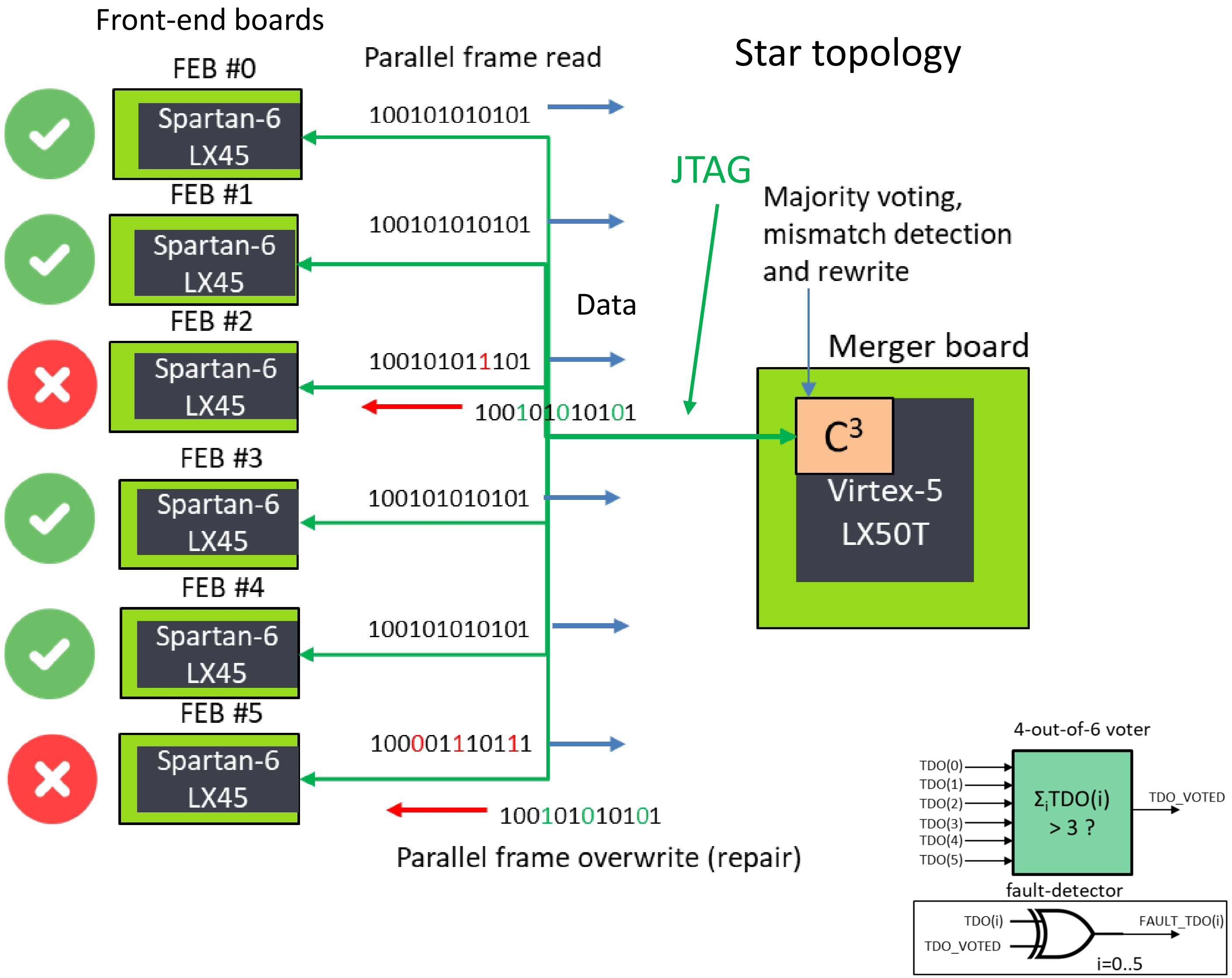


- In October 2019, 5% of front-end FPGAs were affected by at least one configuration SEU over 24 hours
- Effect expected to rise with scheduled luminosity increase => **SEU mitigation effort**

Repairing FEB Configuration On-the-fly

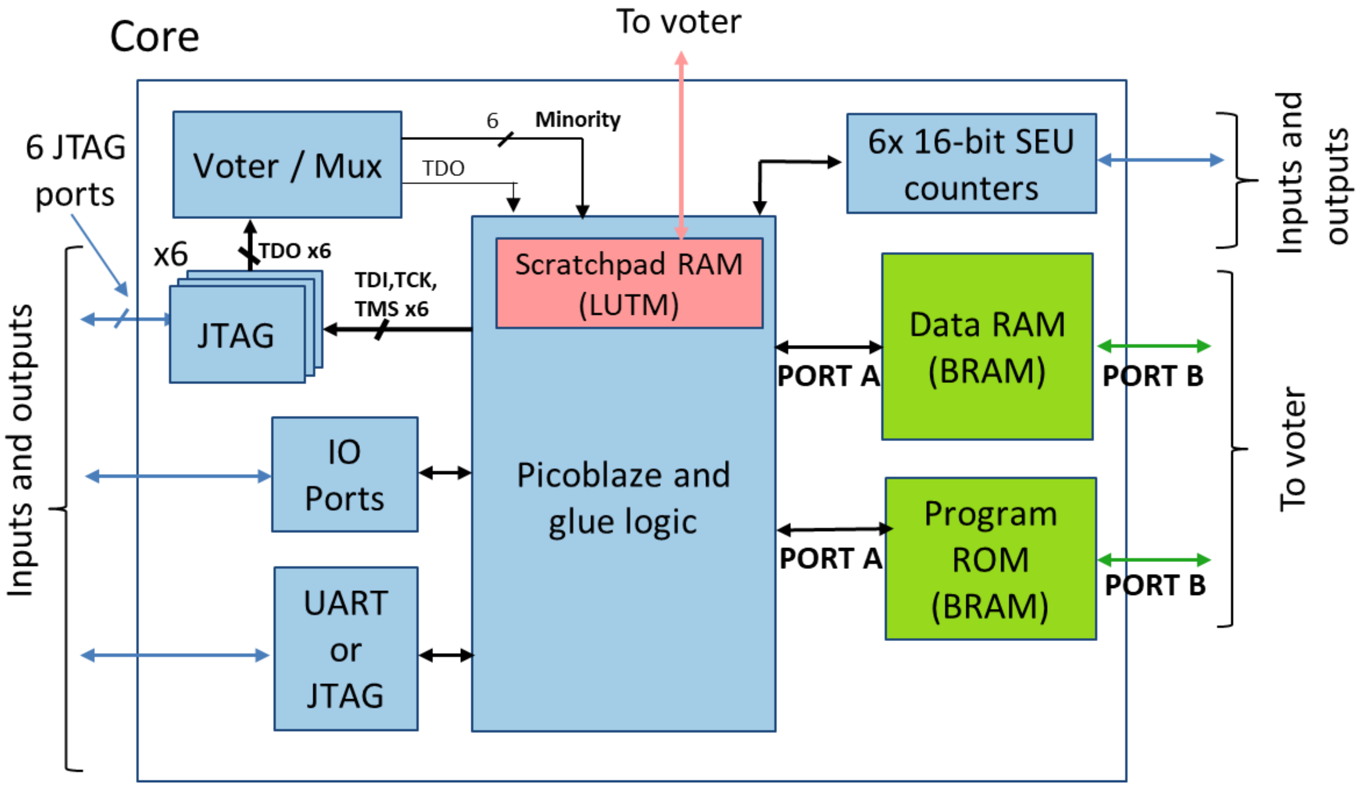
- Front-end boards (FEB) FPGAs are programmed with the same bitstream => redundancy at system-level

- Idea
  - Parallel readback of FEB (Spartan-6) configuration from Merger (Virtex-5)
  - Real-time 4-out-of-6 bitwise majority voting on JTAG streams (TDOs) for error detection
  - Quick single frame reconfiguration for error correction
- Star topology is widely used in DAQ systems, easily-exportable solution



R. Giordano , doi: 10.1109/TNS.2021.3127446

The Configuration Consistency Corrector - C^3

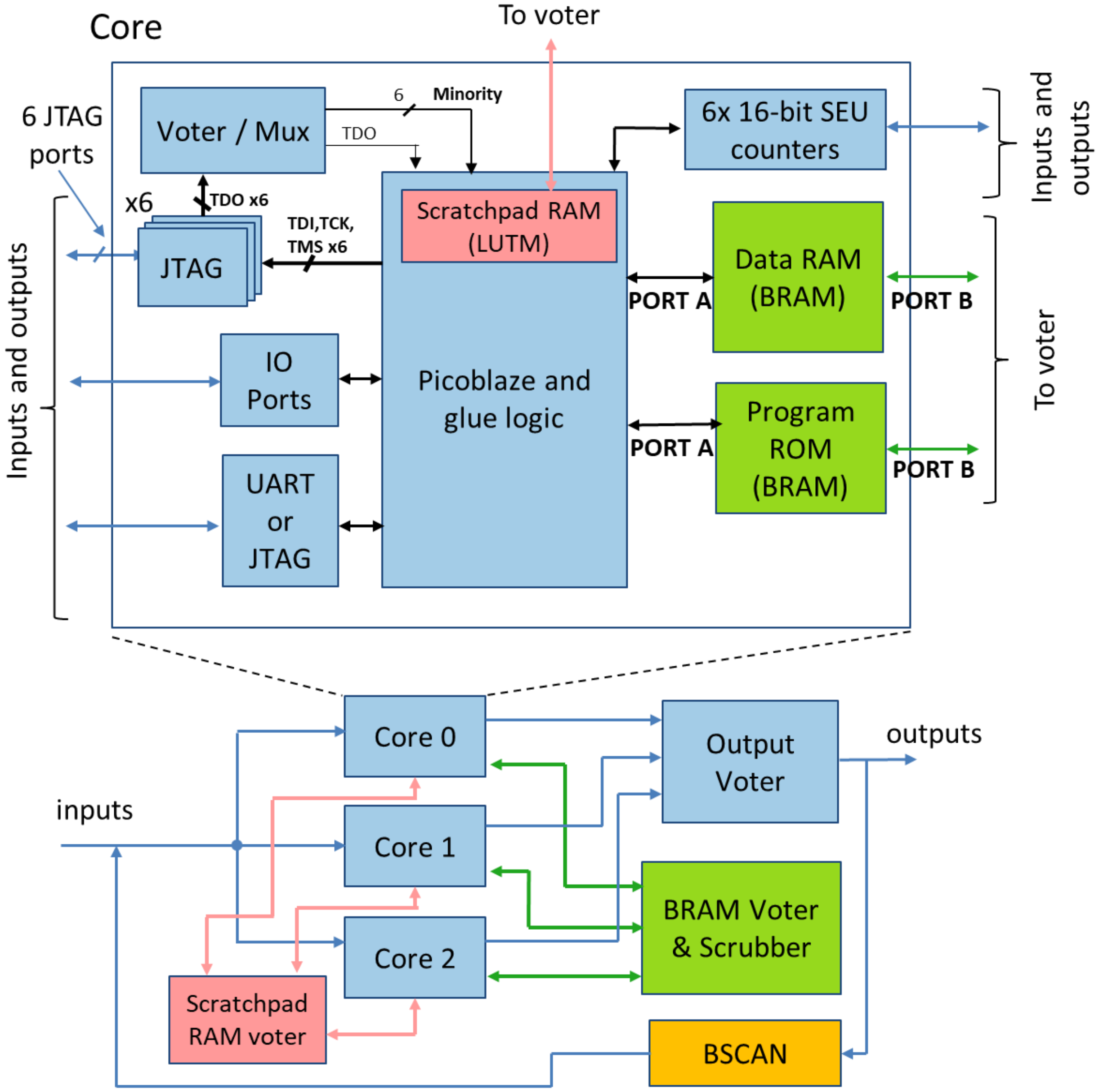


- No golden memory needed and no a priori limit on # of bitflips per frame that can be repaired
- Xilinx Soft Error Mitigation (SEM) controller limited at 2

- Features
  - Majority voting configuration of up to 6 JTAG streams
  - built around Xilinx PicoBlaze6 processor
  - runs at 127 MHz (Belle2Link clock in Merger)
  - 3.3s scrubbing period
- BRAMs store
  - Frame buffers (260x8b)
  - Target FPGA frame addressing device-specific information (1252x8b)
  - uP Program (4096x18b)
- 16-bit upset counter for each target FPGA

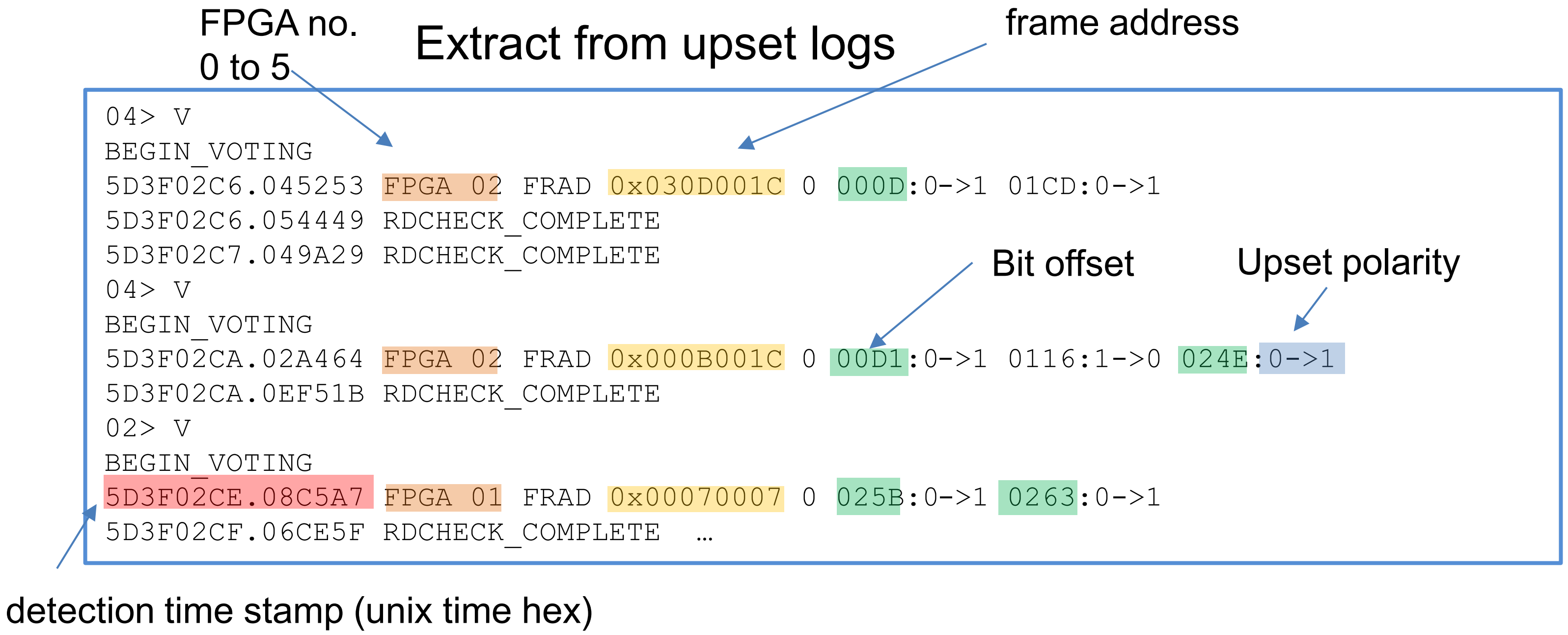
Architecture derived from
R. Giordano et al., “Configuration Self-Repair in Xilinx FPGAs,” doi: 10.1109/TNS.2018.2868992
R. Giordano et al., “Custom Scrubbing for Robust Configuration Hardening in Xilinx FPGAs,” doi: 10.3390/instruments3040056

The Configuration Consistency Corrector – C^3 (2)



- Triple Modular Redundancy for logic and scrubbing for BRAMs
- Periodic reset of uP for internal registers cleanup and scratchpad voting
- UART (or JTAG) for scrubber control and logging of upsets details
- Runs in background, no disruption of user design implemented in FPGA

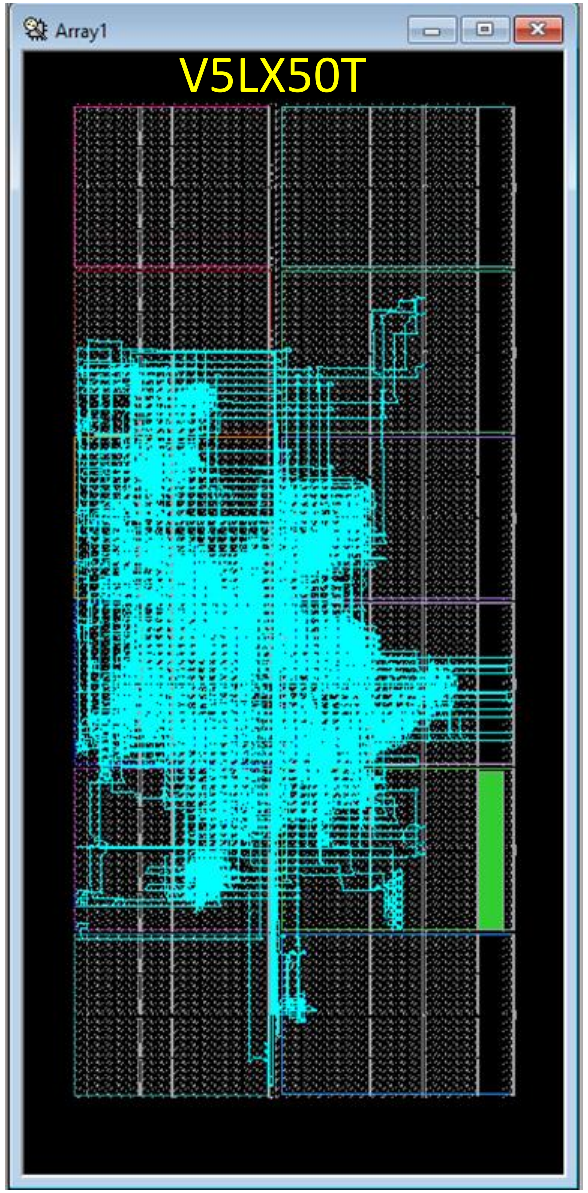
Scrubbing Logs


Extract from upset logs

```
04> V
BEGIN_VOTING
5D3F02C6.045253 FPGA 02 FRAD 0x030D001C 0 000D:0->1 01CD:0->1
5D3F02C6.054449 RDCHECK_COMPLETE
5D3F02C7.049A29 RDCHECK_COMPLETE
04> V
BEGIN_VOTING
5D3F02CA.02A464 FPGA 02 FRAD 0x000B001C 0 00D1:0->1 0116:1->0 024E:0->1
5D3F02CA.0EF51B RDCHECK_COMPLETE
02> V
BEGIN_VOTING
5D3F02CE.08C5A7 FPGA 01 FRAD 0x00070007 0 025B:0->1 0263:0->1
5D3F02CF.06CE5F RDCHECK_COMPLETE …
```

- For each upset, the C^3 sends a text line on UART with
  - unix time stamp, FPGA no., frame address, bit offset(s), polarities
- Very useful for testing and debugging, but the same info could be used to study correlations with of upsets to the radiation environment or to reset FEBs only when essential bits are hit

C^3 firmware standalone



Implementation

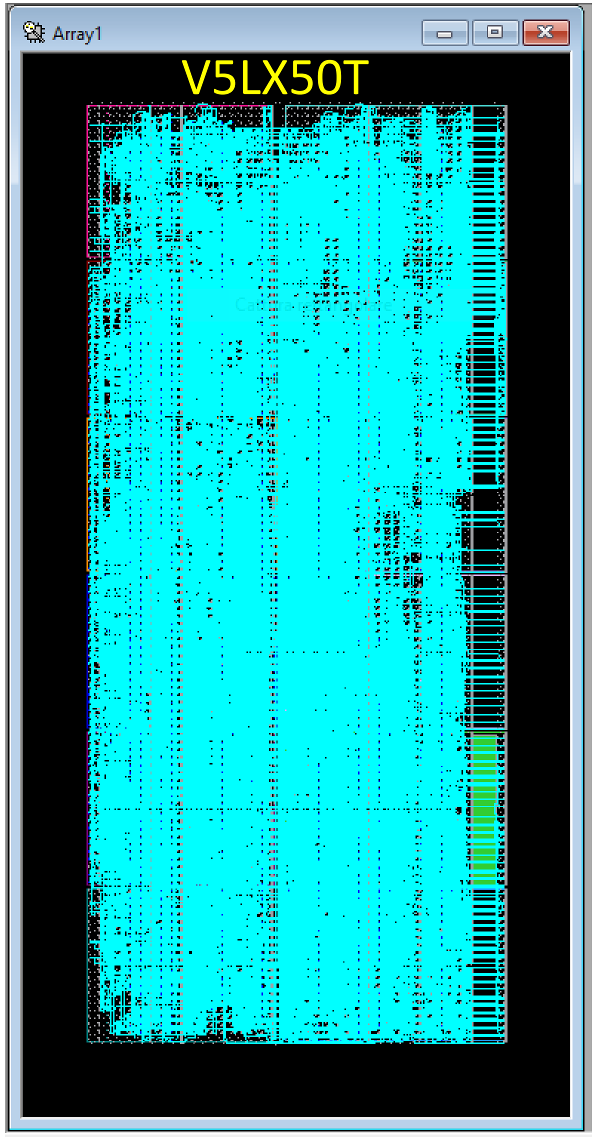
- C^3 has a small logic footprint
- In V5LX50T 828 slices (11%) and 9 BRAMs (15%)
- Projected to Kintex Ultrascale+ K5UP => 1.5% slices and 1.9% BRAM

C^3 firmware standalone

Logic Resources	Used	Available	%
Slices: FFs	1,068	28,800	3
Slices: LUTs	2,005	28,800	6
Slices: overall	828	7,200	11
BUFGs	3	32	9
BRAM 36k	9	60	15
BSCAN	1	4	25

Implementation (2)

Readout + C^3 firmware



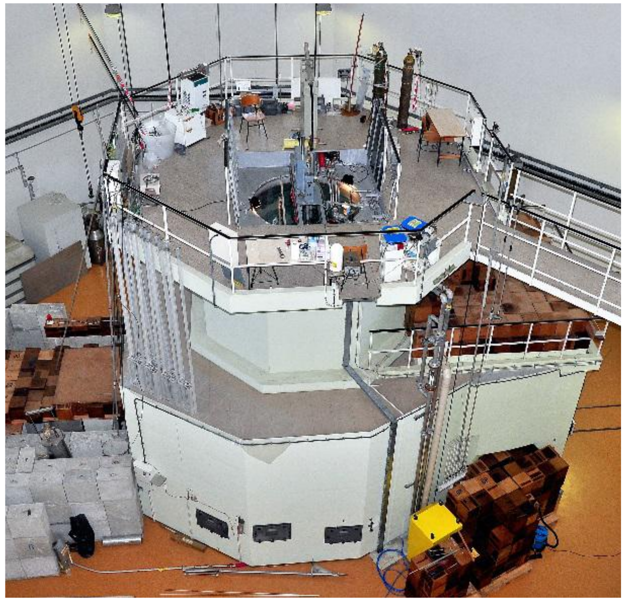
Readout + C^3 firmware

Logic Resources	Used	Available	%
Slices: FFs	14,932	28,800	51
Slices: LUTs	16,159	28,800	56
Slices: overall	5,977	7,200	83
BUFGs	10	32	31
BRAM 36k	35	60	58
BSCAN	1	4	25

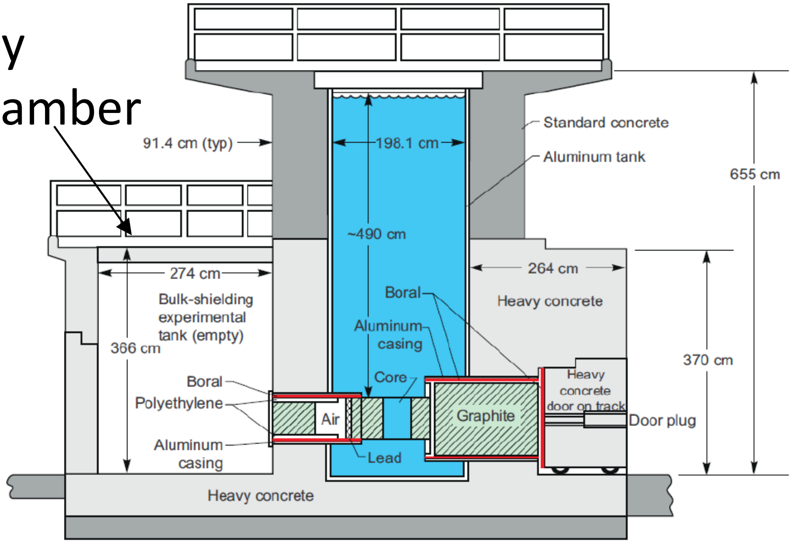
- Implementation of Merger firmware w/ C^3
- Fits V5LX50T resource availability
  - Slices at 80%, BRAMs at 58%

Neutron Irradiation Test

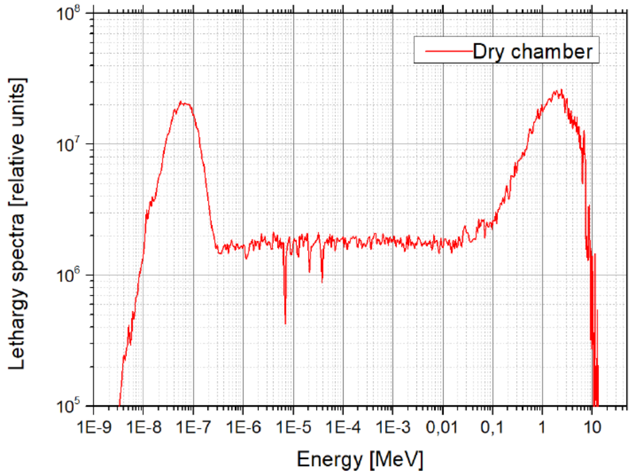
- Irradiation tests at the TRIGA reactor of Jožef Stefan Institute (Ljubljana, Slovenia)
- MARK II 250 kW water-cooled, research reactor from General Atomics
- Dry chamber for large samples (60cm x 60cm)



TRIGA layout



Dry chamber



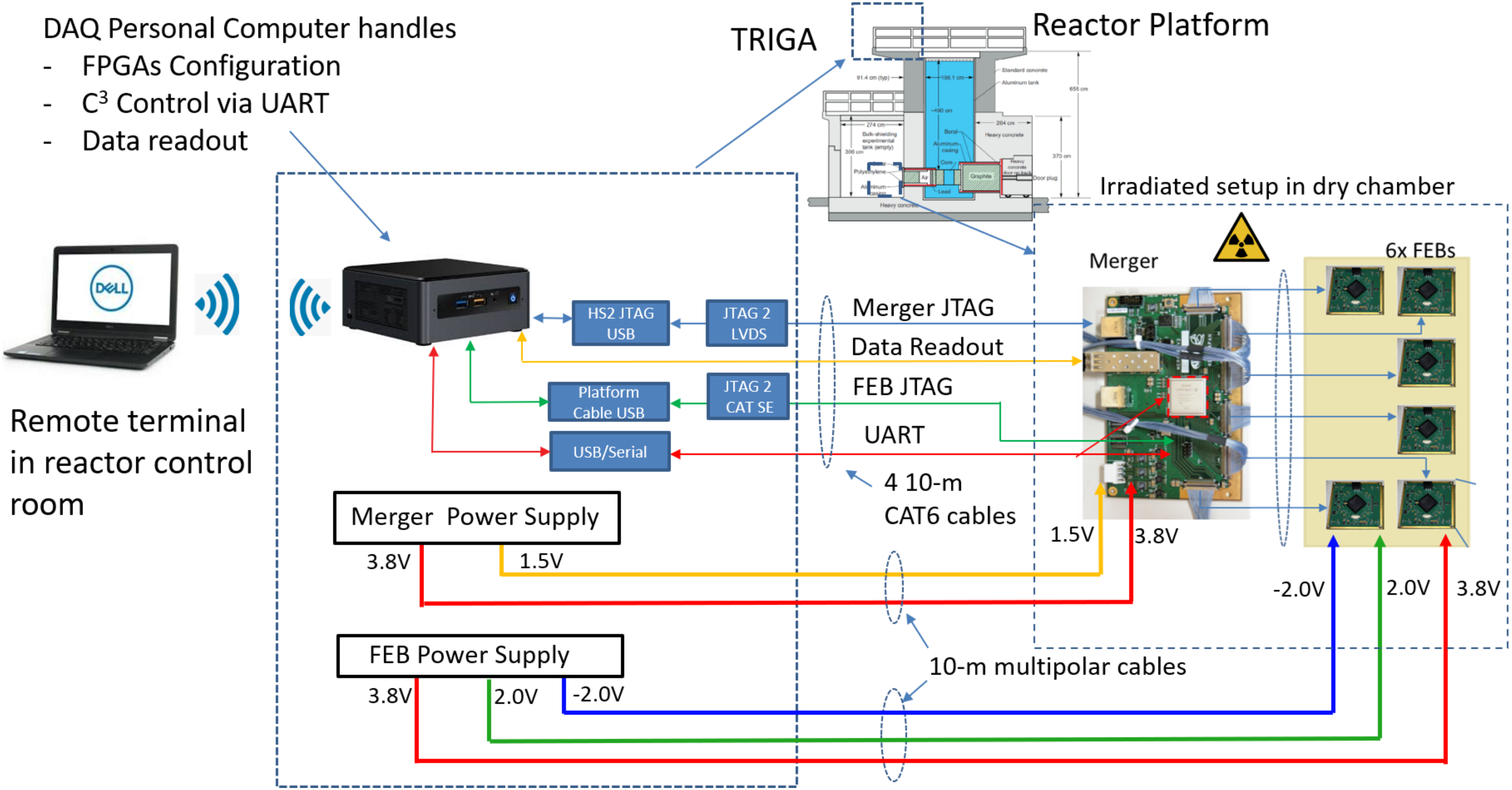
Calculated properties at 250 kW:

	Neutron flux - no fission plate [$cm^{-2}s^{-1}$]	**Neutron flux - fission plate installed [$cm^{-2}s^{-1}$]**
Thermal (< 0.625 eV)	8.8×10^7	8.3×10^7
Epithermal (0.625 – 10^5 eV)	2.6×10^7	2.9×10^7
Fast (> 10^5 eV)	1.7×10^7	9.5×10^7
Total	1.3×10^8	2.1×10^8

Irradiation Test Setup

DAQ Personal Computer handles

- FPGAs Configuration
- C^3 Control via UART
- Data readout



TRIGA

Reactor Platform

Irradiated setup in dry chamber

Remote terminal in reactor control room

HS2 JTAG USB

JTAG 2 LVDS

Platform Cable USB

JTAG 2 CAT SE

USB/Serial

Merger JTAG

Data Readout

FEB JTAG

UART

4 10-m CAT6 cables

Merger

6x FEBs

Merger Power Supply

3.8V

1.5V

1.5V

3.8V

FEB Power Supply

3.8V

2.0V

-2.0V

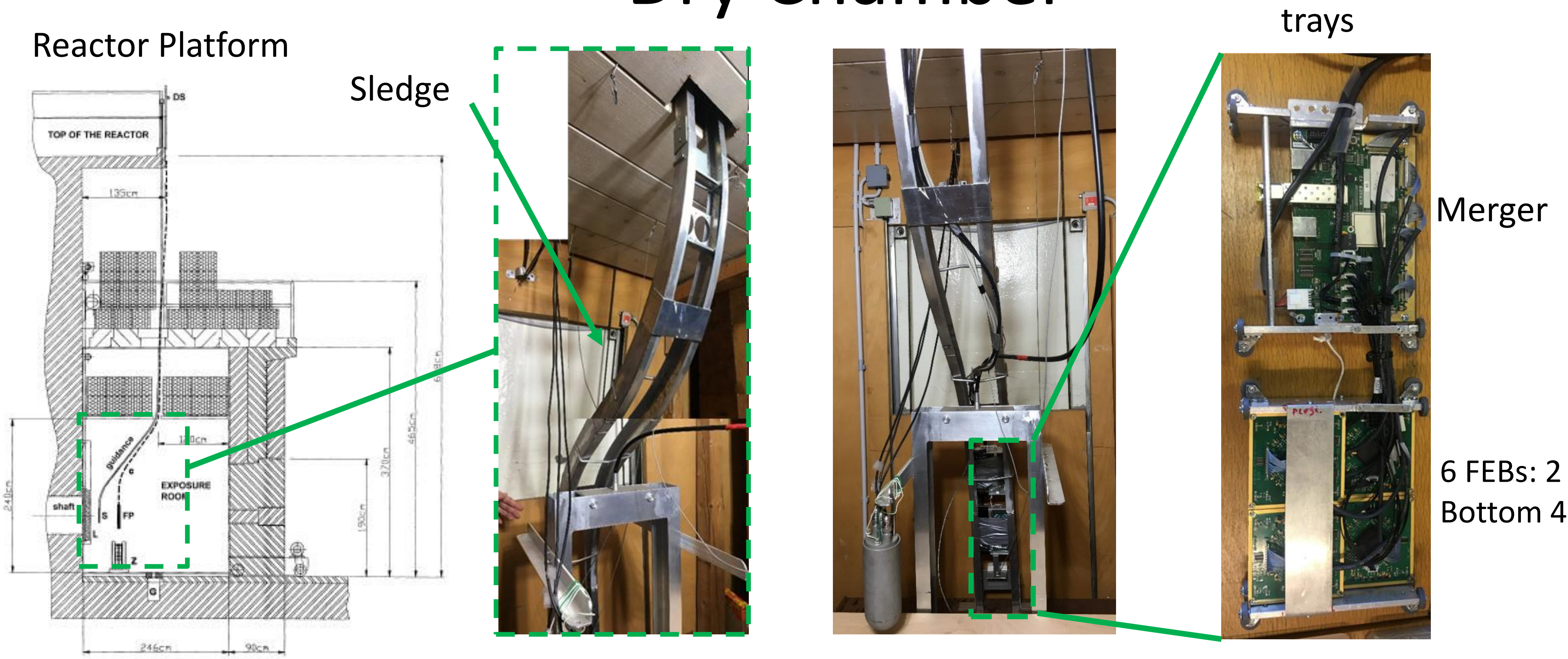
-2.0V

2.0V

3.8V

10-m multipolar cables

Dry Chamber



Side view

- Sledge for sliding DUTs in and out irradiation channel for quick irradiation start/stop
- Reactor always on at 250 kW during test

Test Results: Cross Sections

- 29 runs, total irradiation time 14 hours, on average 29 minutes per run

Description	Value
Total # of C^3 failures – N_{C3} –	10
Total # of upsets Merger – N_{MERGER} –	$1.1 \cdot 10^3$
Mean # of upsets in Merger between C^3 failures	$1.1 \cdot 10^2$
Total # of upsets (bitflips) in 6 FEBs	$3.8 \cdot 10^5$
Total # upsets per FEB – N_{FEB} –	$6.3 \cdot 10^4$
Mean # of upsets per 6 FEBs between C3 failures	$3.8 \cdot 10^4$
Mean # of upsets per FEB between C3 failures	$6.3 \cdot 10^3$
Average upsets rate detected by C^3 per FEB	1.26 Hz

$$\sigma = \frac{\mathrm{N_{events}}}{\Phi}$$

Failure cross section

$$\frac{N_{C3}}{N_{FEB}} = \frac{\sigma_{C3}}{\sigma_{FEB}} = 1.6 \cdot 10^{-4}$$

upset cross section

Upset cross sections

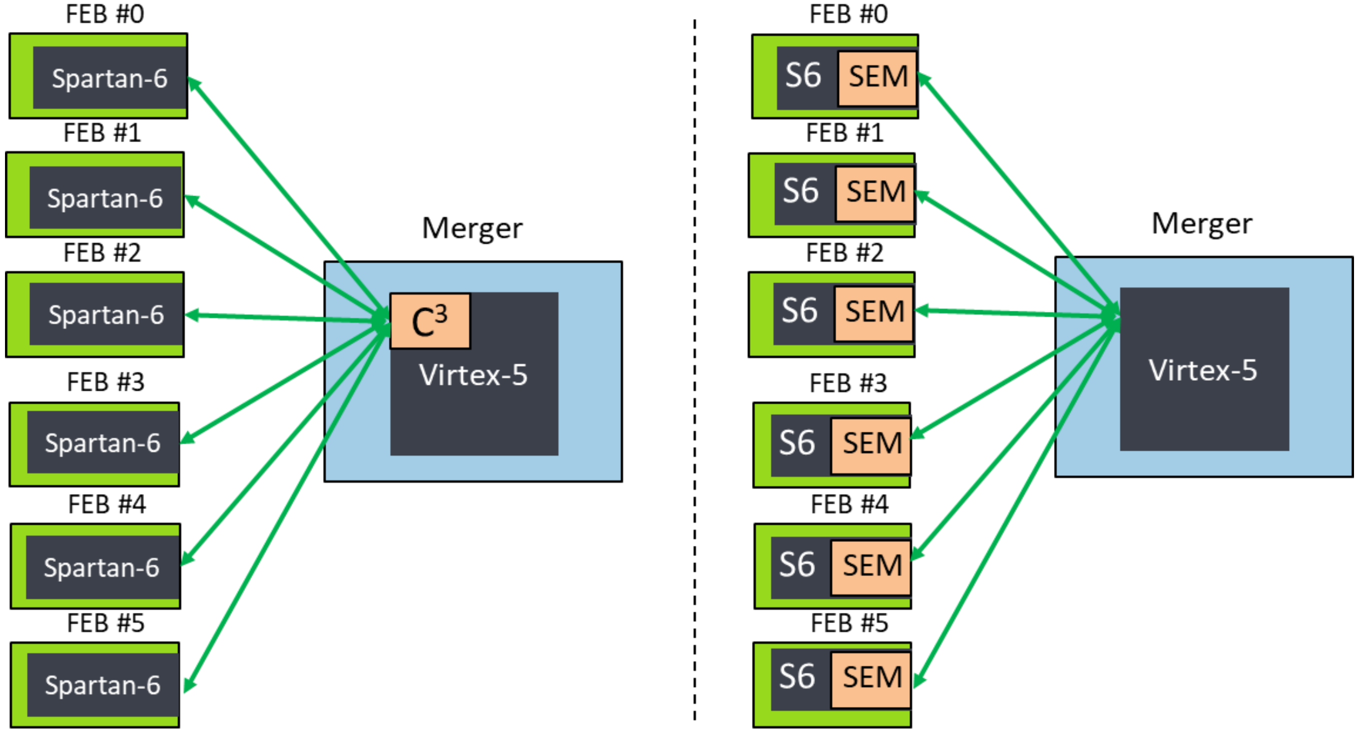
$$\frac{N_{MERGER}}{N_{FEB}} = \frac{\sigma_{MERGER}}{\sigma_{FEB}} = 1.7 \cdot 10^{-2}$$

Assuming same neutron
fluence on merger and FEB

Impact on Readout Functionality: C^3 Vs SEM

- Failure defined as readout interrupted or data corrupted
- Two sets of runs
  - A single C3 implemented in Merger
  - A SEM implemented in each FEB

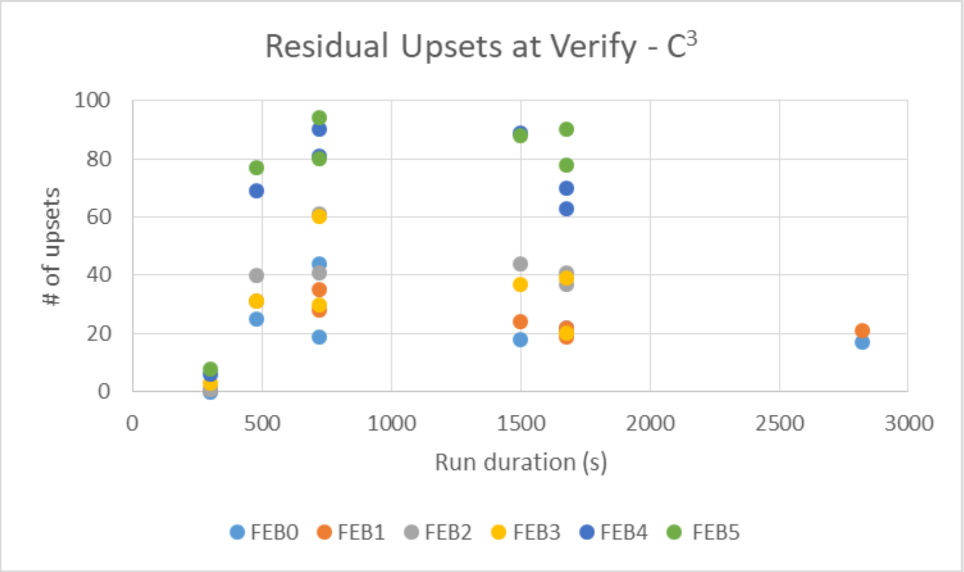
	SEM in FEB	C^3 in Merger
# of runs w/ readout testing	11	13
Test time (h)	4.8	8.0
# of read out failures	10	13
Average upset rate per FEB (Hz)	1.26	1.26
Readout MTBF (s)	$1.7\cdot10^3$	$2.2\cdot10^3$
Readout MTBF (upsets)	$2.2\cdot10^3$	$2.8\cdot10^3$



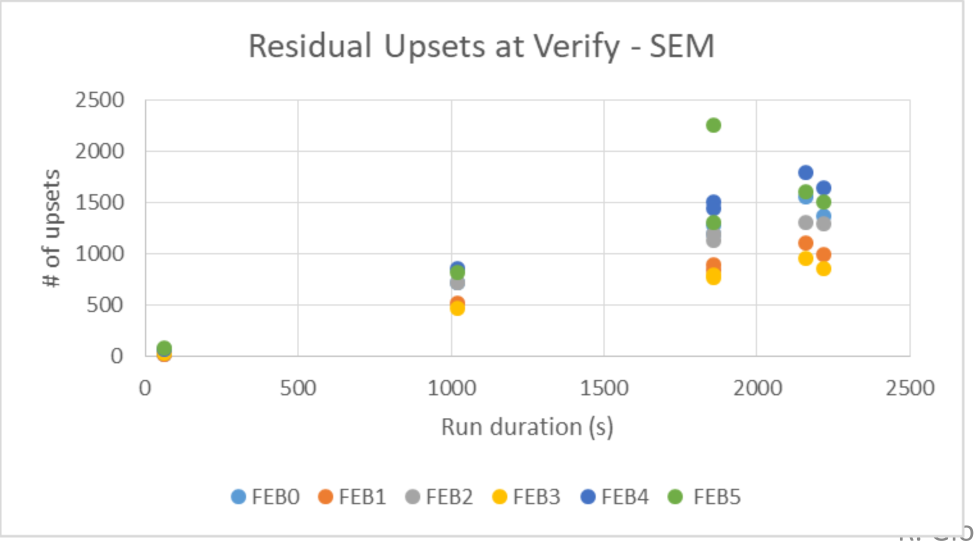
$$\frac{MTBF_{C3}}{MTBF_{SEM}} = 1.3$$

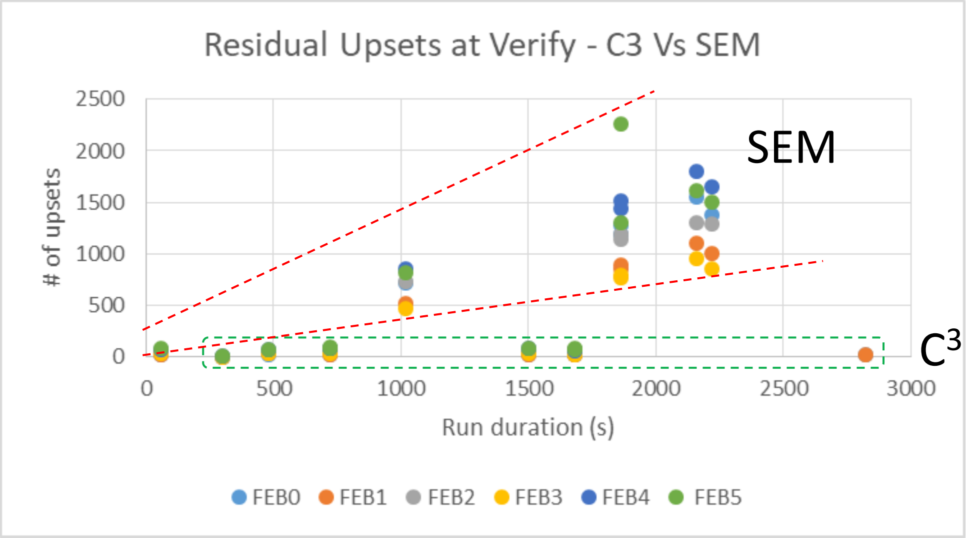
30% improvement moving from SEM to C^3

Upset Correction Capability: C^3 vs SEM

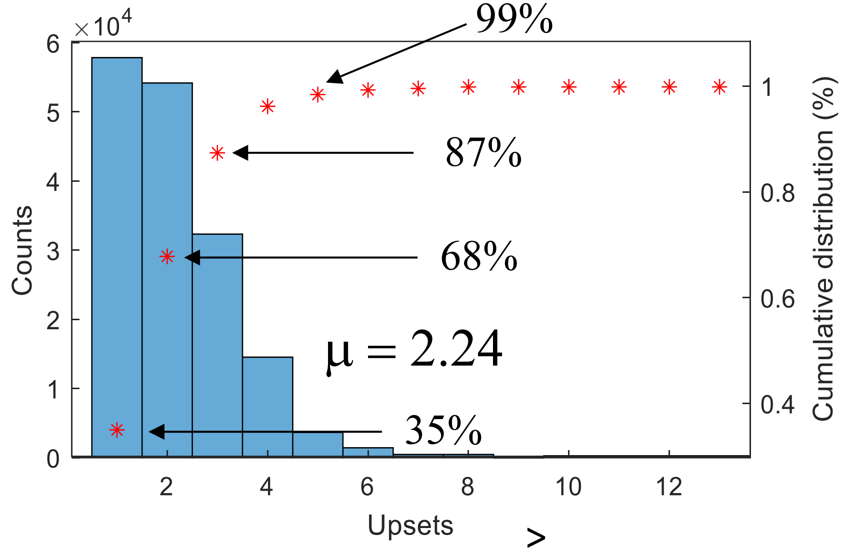


- Residual upsets in FEBs at the end of the run
- SEM lets upsets accumulate over time
- C^3 reduces accumulation
  - Small amount residual related to stop (or failure) of C^3 at the end of the run before verify

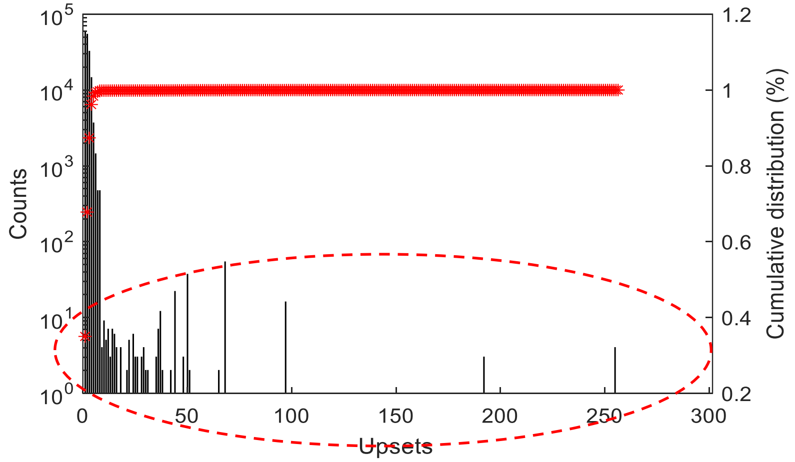




Number of Upsets per Frame



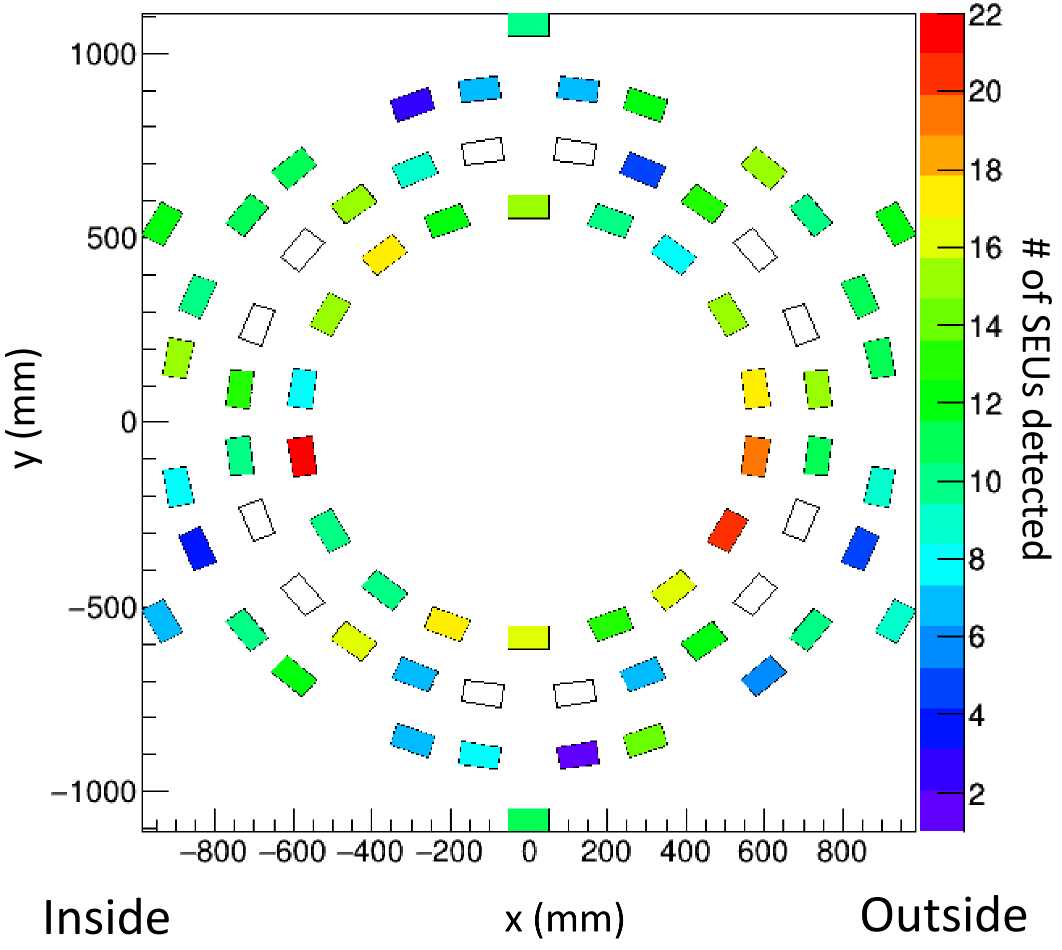
Log scale



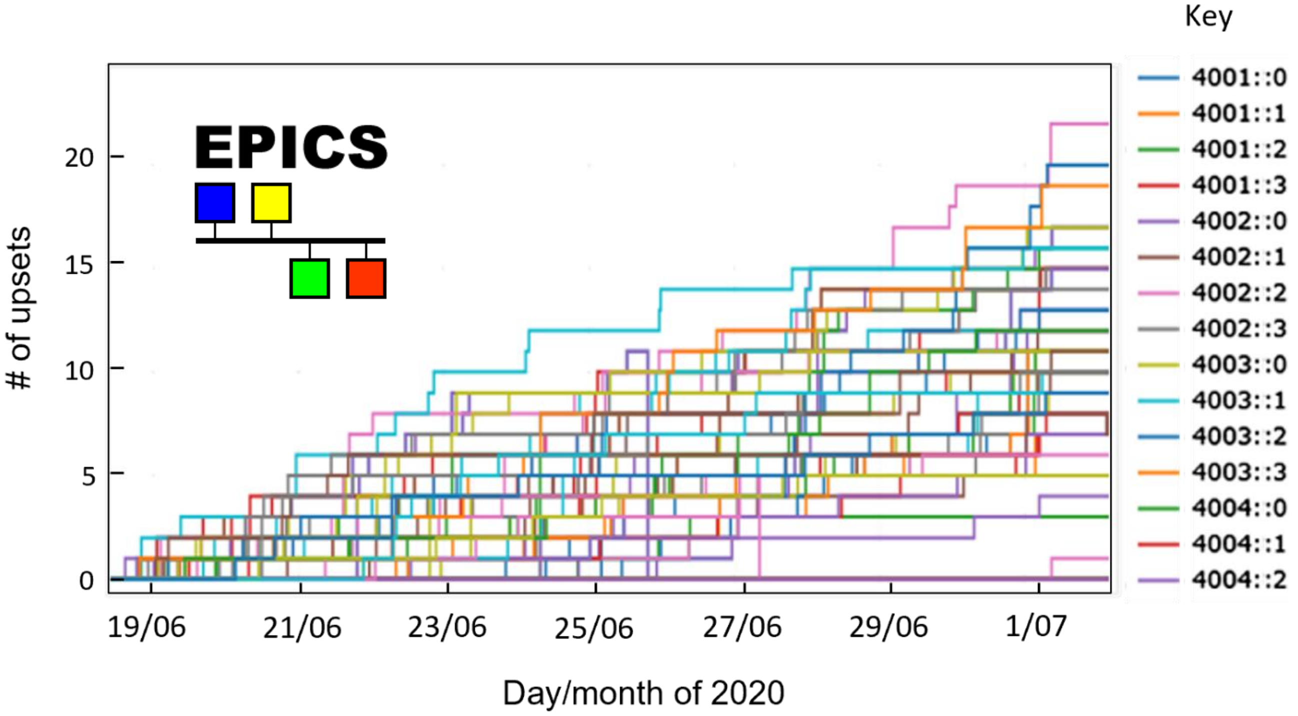
- Distribution of the number of bitflips per frame (multiplicity) in each SEU event detected by C3
- Total events 165k
- Average multiplicity 2.24 upsets per SEU event
- 65% of events have multiplicity > 1 (not correctable by SEM)
- 99% of events have multiplicity <= 5
- Includes also few tens of events w/ up to 256 flips, likely configuration SEFIs

2020 Run

SEU map of FEB groups
(14 days, Jun. 18 to Jul. 1 2020)

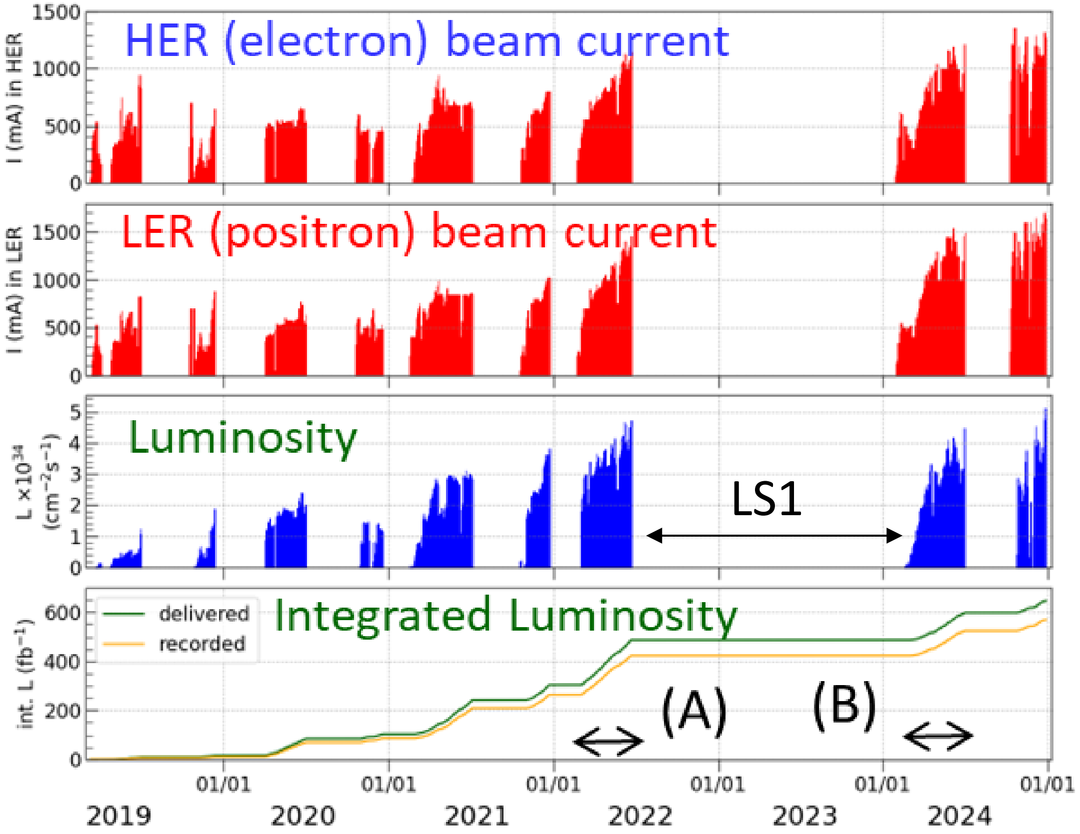


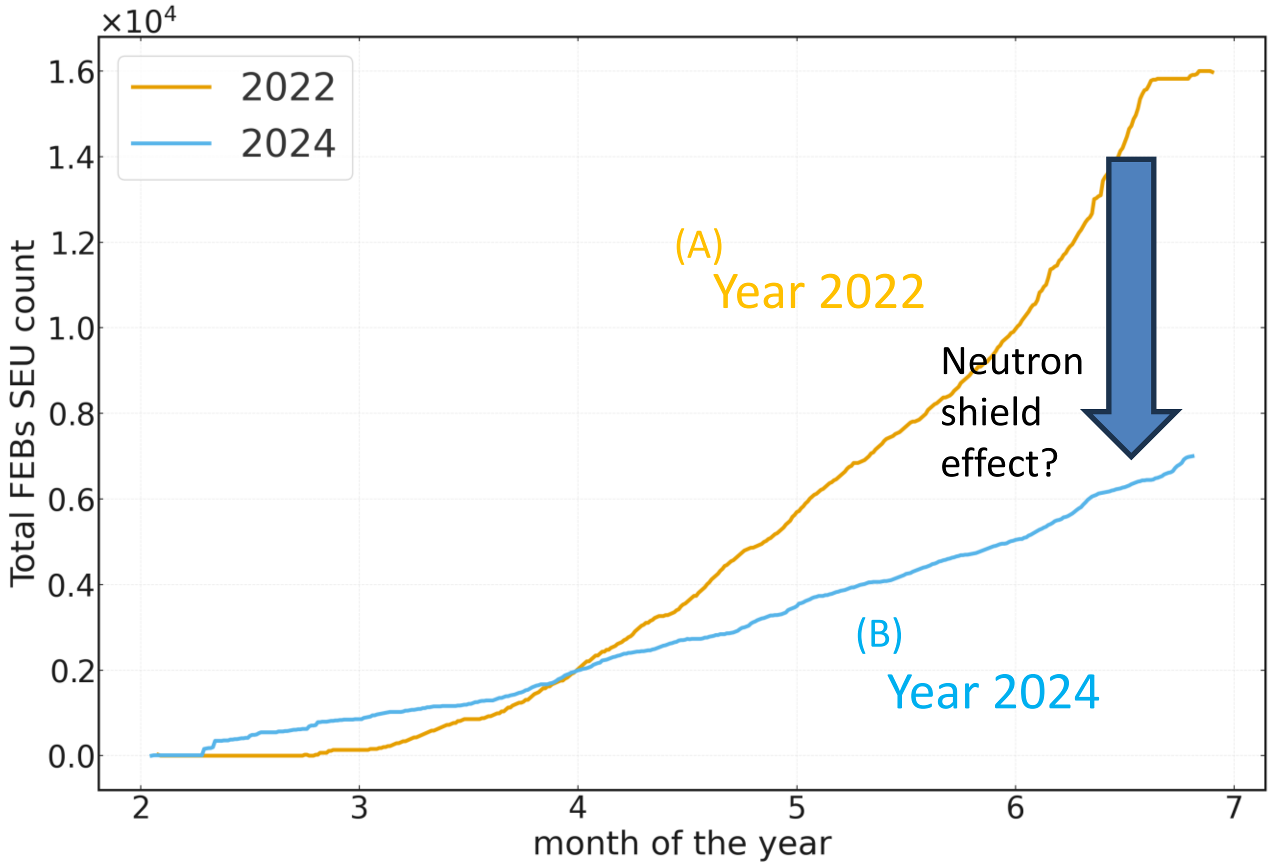
- C^3 fully integrated and running in Belle II TDAQ since the middle of 2020 spring run
- SEUs monitored via EPICS slow control system
- FEBs now robust against configuration SEUs



2022 and 2024 Runs

SuperKEKB Operation



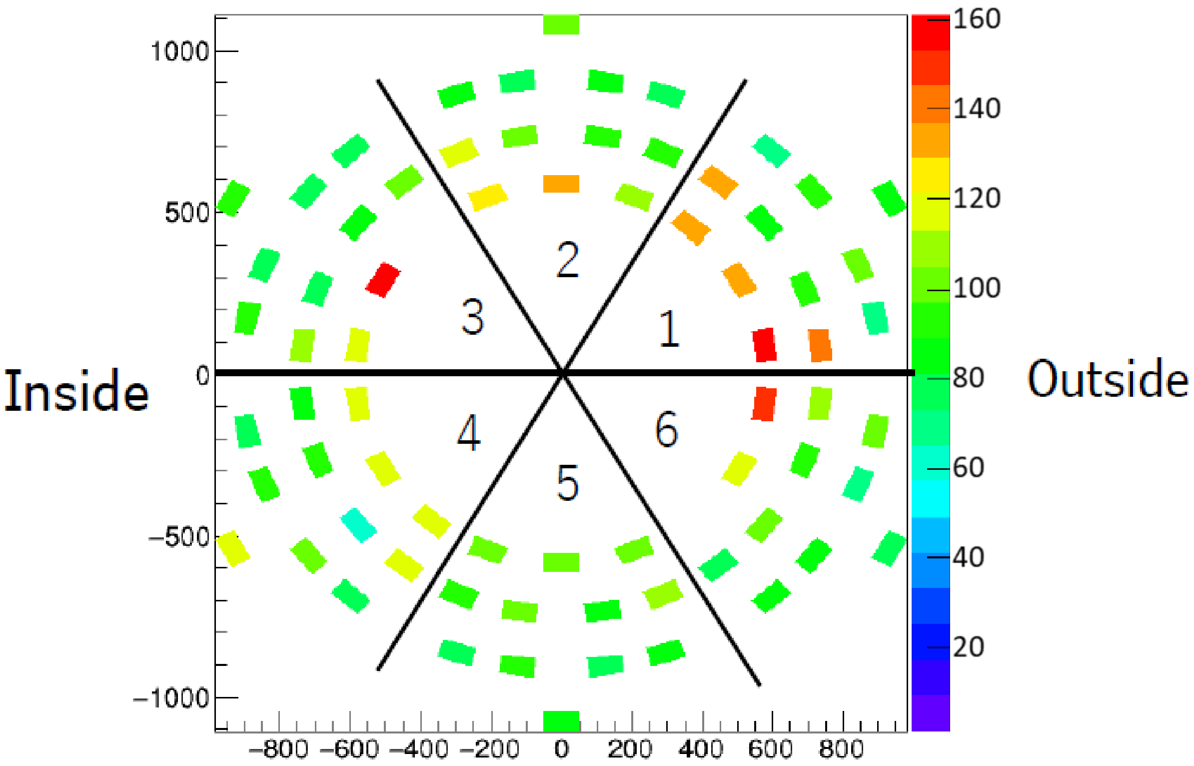


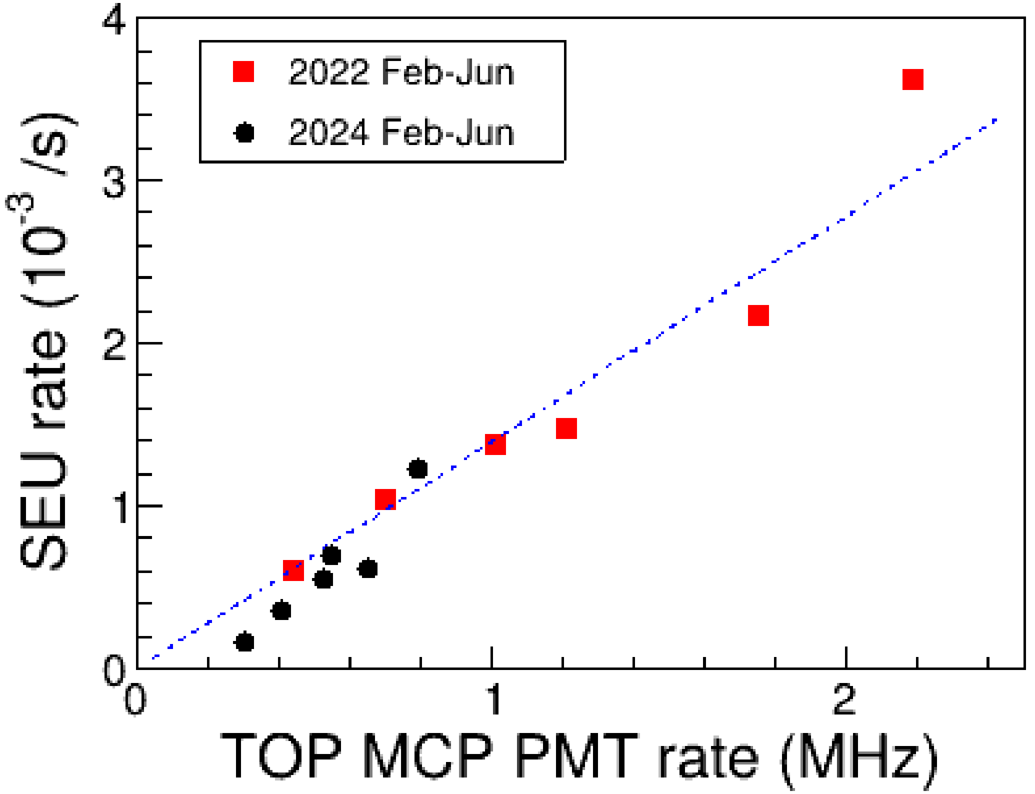
Neutron shield effect?

From Feb. to July of	2022	2024
Total SEUs on 420 FEBs	16k	7k
Detected and fixed SEUs / (FPGA · day)	~0.2	~0.1

2022 and 2024 Runs (2)

2024





- Position dependence of SEU counts is confirmed as in 2020.

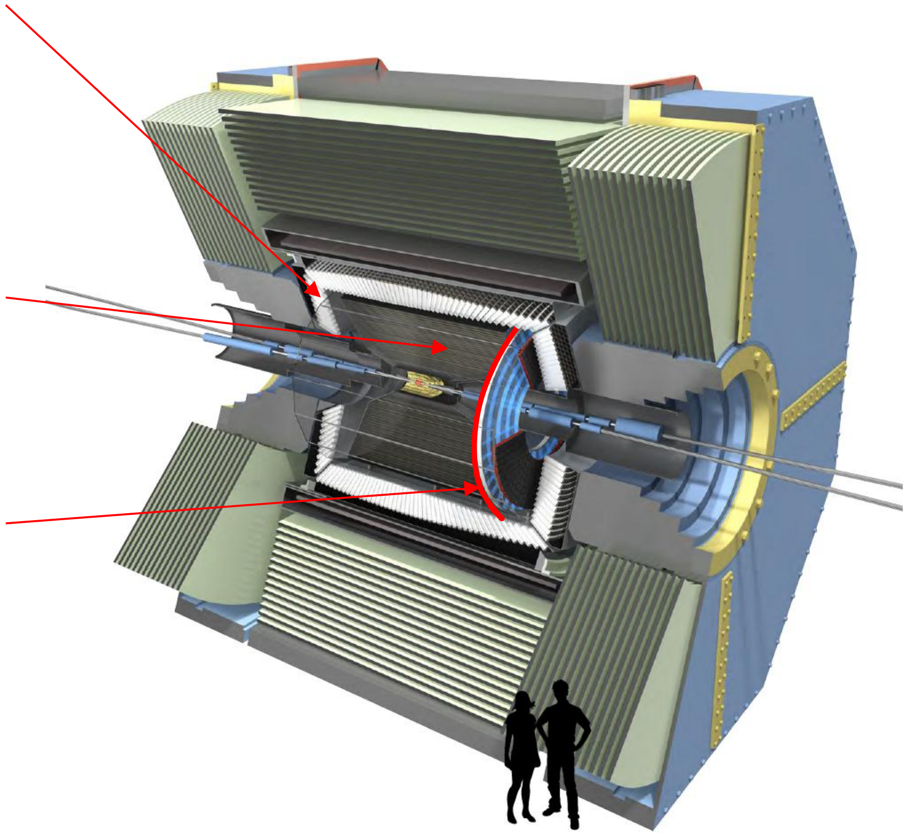
- Each point corresponds to ~ 2 weeks.
- TOP MCP PMT rate is known to correlate well with the SuperKEKB beam background level.
- May be used to predict future SEU rates.

FPGAs at Belle II

Time of Propagation counter
256 Zynq-7030
64 Zynq-7045

Central Drift Chamber
300 Virtex-5 LX155T

Aerogel Ring Imaging CHerenkov counter
420 Spartan-6 LX45
72 Virtex-5 LX50T



- Overall 1100+ SRAM-based FPGAs used on detector
  - 46% for ARICH
- SEU mitigation efforts
  - On-the-fly SEU correction for ARICH (this talk and [1])
  - Concrete, PE and borated-polymer shields against fast and thermal neutrons
  - FPGA-embedded sensors added for monitoring neutrons/SEUs [2,3]

[1] doi: 10.1109/TNS.2021.3127446
[2] doi: 10.1109/TNS.2023.3265740
[3] doi: 10.1088/1748-0221/19/06/P06043

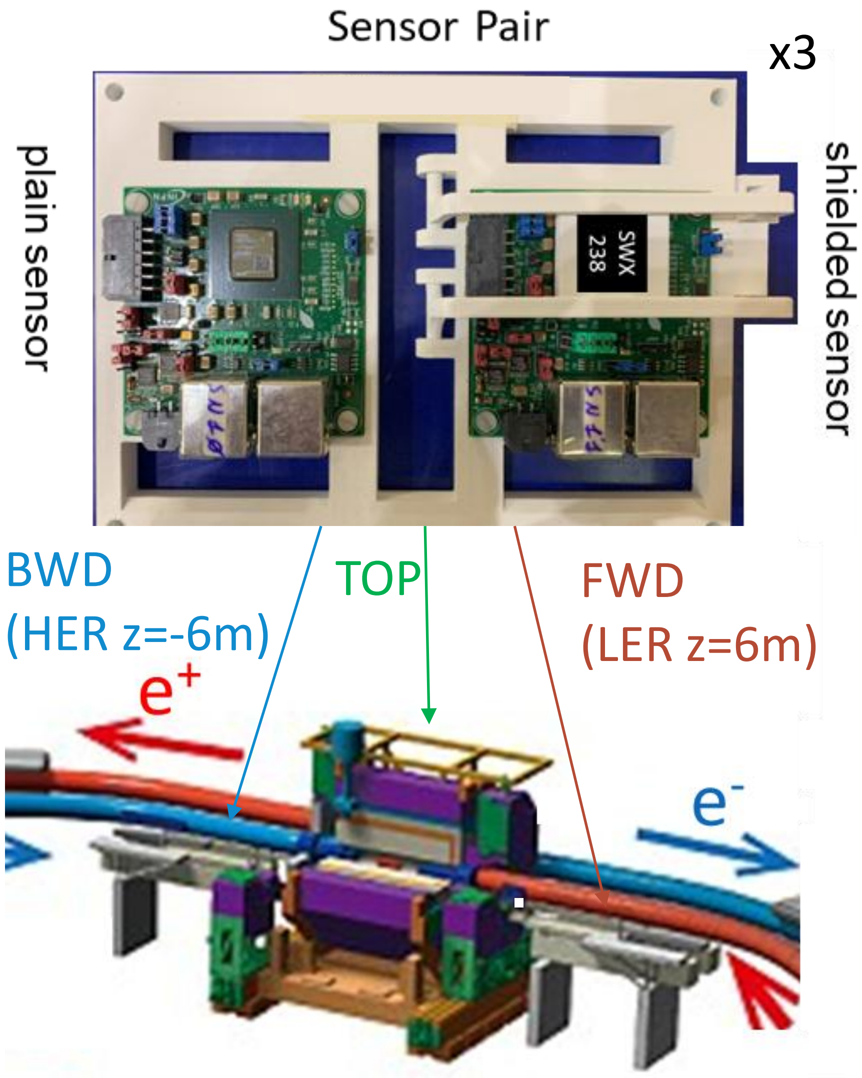
FPGA-embedded SEU Monitors at Belle II

Idea

- Use Artix-7 FPGAs (include Boron) as radiation sensors
- Arrange sensors in pairs, plain (thermal+fast) and shielded against thermal neutrons (only fast)
- Estimate thermal and fast neutrons fluence by difference

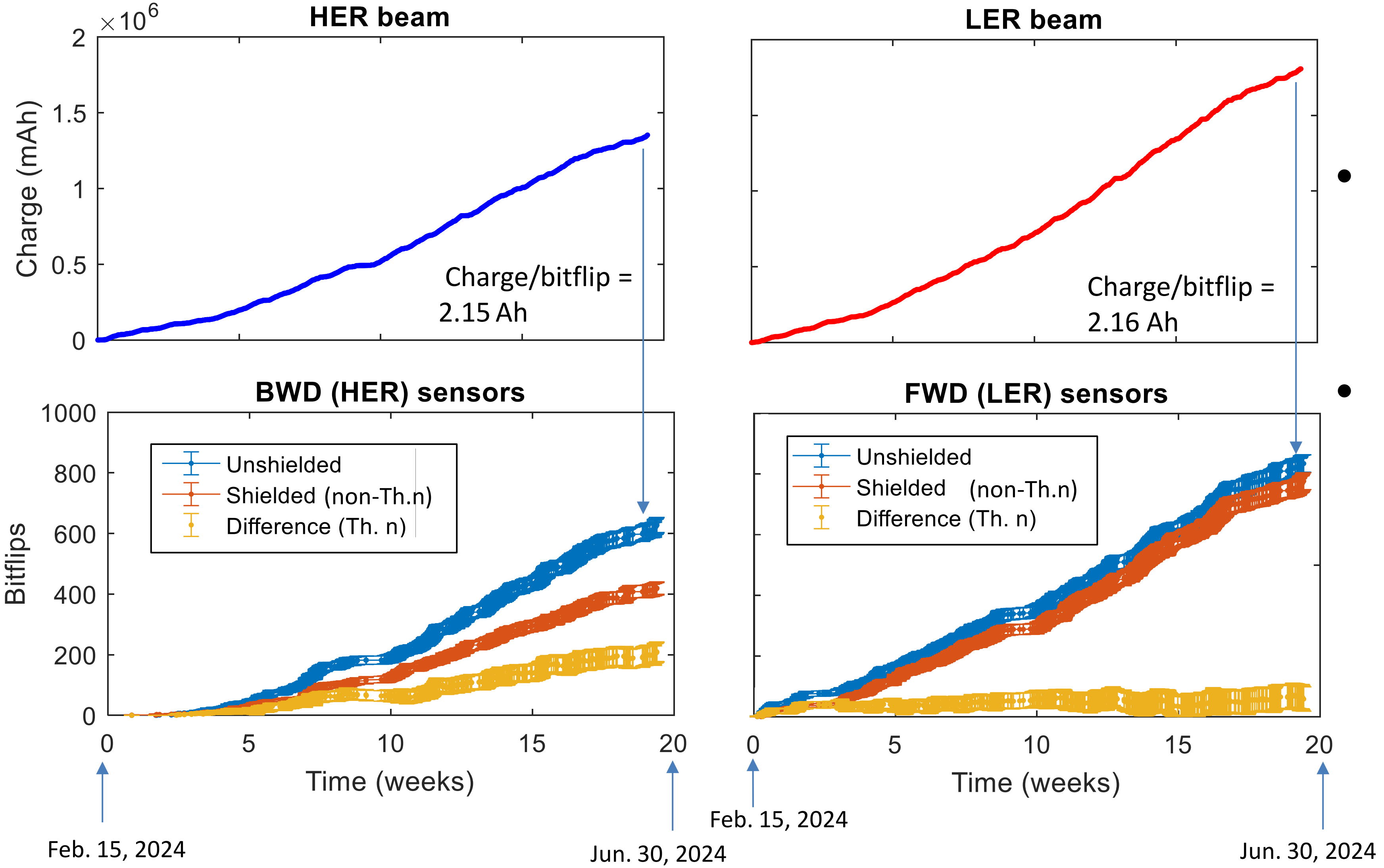
shieldwerx™

- SWX-238 polymer as thermal neutron shield
  - 27.6% Boron in weight
  - 1-layer 1/8” thickness (3.2 mm)
  - Shields 99.75% thermal neutrons
  - Minimal thermalization of fast neutrons



Belle II

Cumulated Bit Flip Trends in 2024



Charge/bitflip = 2.15 Ah

Charge/bitflip = 2.16 Ah

- Correlation with integrated beam currents
  - ρ > 99.57% (correlation coefficient)
- Electron (BWD) vs Positron ring (FWD)
  - Different thermal vs non-thermal contribution
  - (Integrated Beam Current)/(Plain Counts) ratios match within 1%

Summary and…

- Developed a scrubber (C^3) to majority vote configuration across FPGAs connected in a star topology
  - Fast detection by means of parallel readback and correction by partial reconfiguration
- Irradiation test results show
  - σ of failures in C^3 almost four orders of magnitude lower than upset σ in FEBs
  - 30% better MTBF of C^3 w.r.t. SEM
- System installed and fully operational in Belle II since 2020
  - Robust against background increases, SEUs in mergers are probably the next issue to be addressed
- Dedicated FPGA-based SEU monitoring system running since 2024

…Acknowledgments

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  - A. Boiano, A. Vanzanella, A. Pandalone, V. Masone from SER (Electronics and Detectors Service), A. Bertocco and G. Passeggio from PM (Mechanics Design) of INFN Napoli for their technical support to this activity

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Sezione di Napoli

  - JSI TRIGA staff for their technical support during the irradiation test

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Institute

Backup

Resource Usage in a Modern FPGA

C^3 firmware standalone	Virtex-5 LX50T			Kintex Ultrascale+ 5UP*		
Logic Resources	**Used**	**Available**	**%**	**Used**	**Available**	**%**
Slices: FFs	1,068	28,800	3	1,068	434,000	0.25
Slices: LUTs	2,005	28,800	6	2,005	217,000	0.92
Slices: overall	828	7,200	11	~400*	~27,000	~1.5
BUFGs	3	32	9	3	32	9
BRAM 36k	9	60	15	9	481	1.9
BSCAN	1	4	25	1	4	25

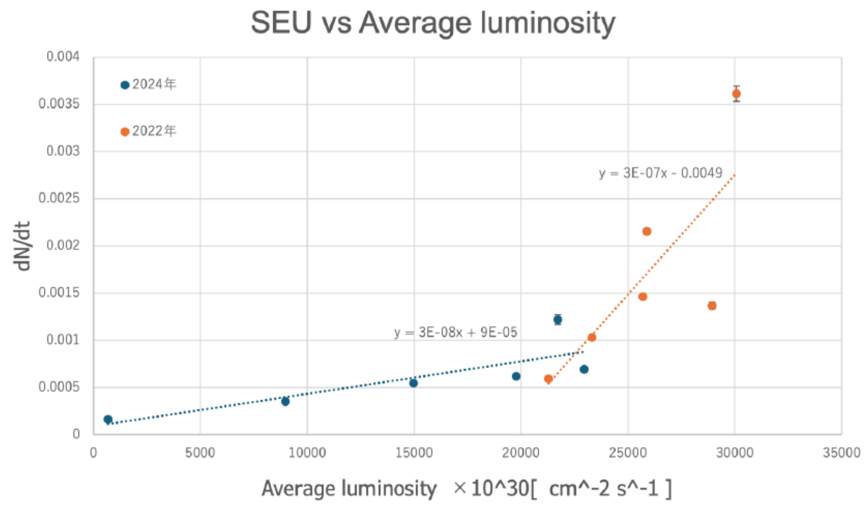
*Projected

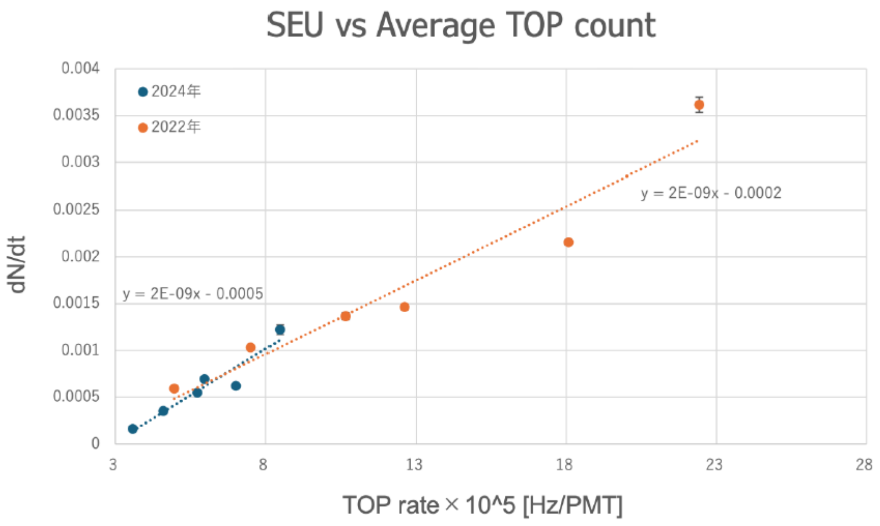
Backup

Comments

- SEUs in FEBs are manageable with the Configuration Consistency Corrector, even the luminosity and/or background increases from now.
- SEUs in mergers are probably the next issue in future.
  - ✓ DAQ errors by ARICH occur a few times per week. Most of them are suspected due to SEUs in mergers.
  - ✓ Possible solution: automatic recovery from SEUs without stopping DAQ.

Backup





- The data shows that the SEU counts depends on the SuperKEKB beam background level, rather than the luminosity or HER/LER currents.

SRAM-based SEU Monitors

- SRAMs used as hadron fluence sensors at LHC [1] and in proton therapy [2,3]
- Hadrons with energy>few MeV and thermal neutrons may indirectly induce SEUs in SRAMs

hadron fluence

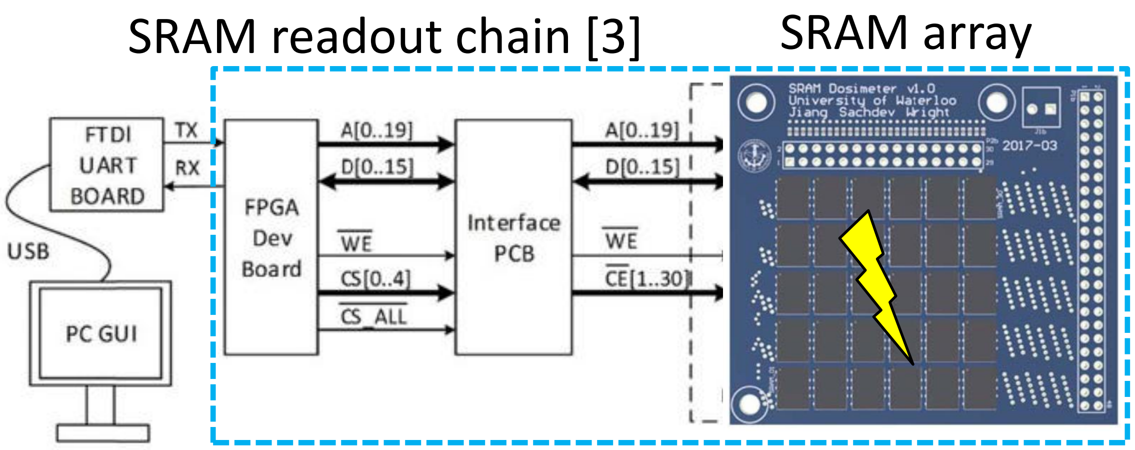
upset count

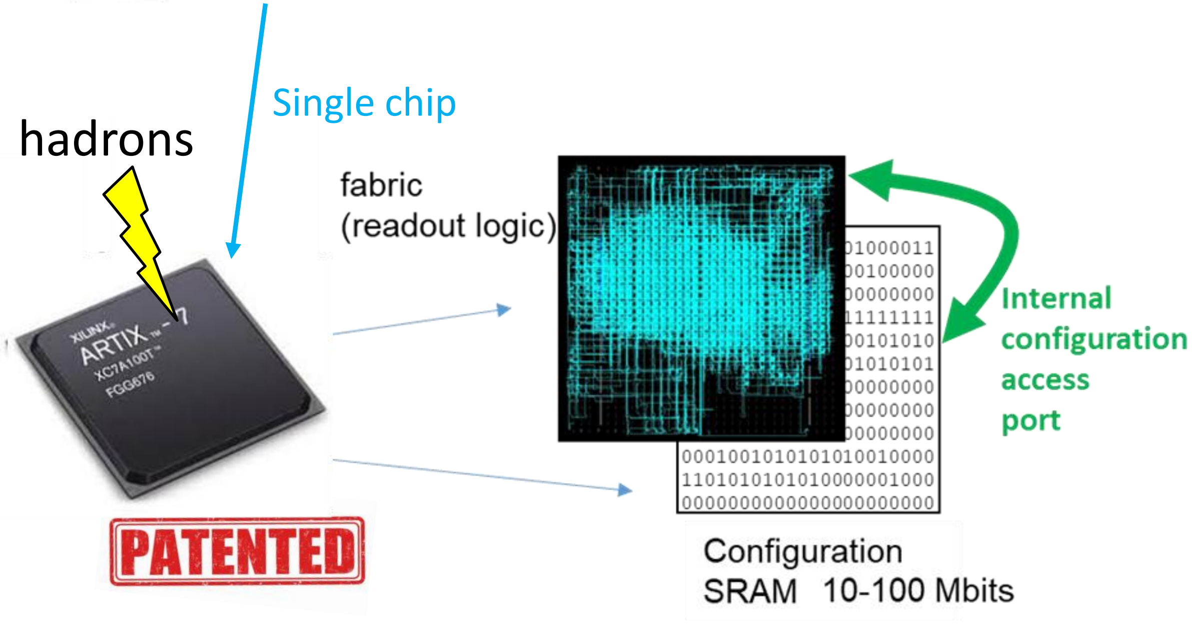
$$\Phi = \frac{N_{upsets}}{\sigma_{bit} N_{bits}}$$

cross section per bit

memory size

- $\sigma_{bit} = \sigma_{bit}$(device, V_{DD}, hadron, E)
- Classic solutions: SRAM + readout device
- Novel solution [4,5]: sensor embedded in a SRAM-based FPGA
  - CRAM as sensitive element + fabric programmed as readout





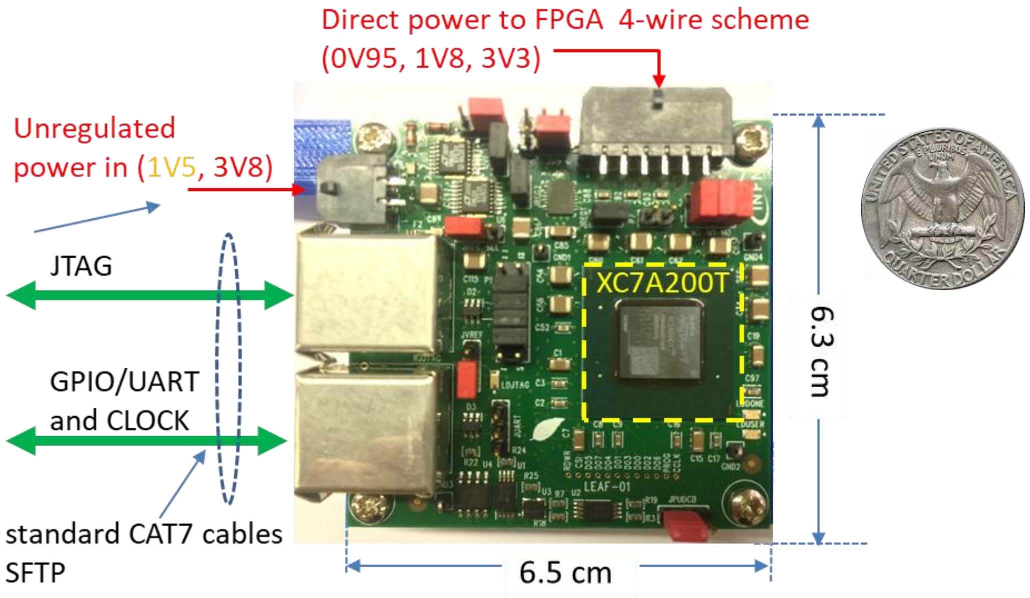
[1] doi: 10.1109/TNS.2014.2365042
[2] doi: 10.1016/j.radmeas.2019.01.001
[3] doi: 10.1109/TNS.2018.2884148
[4] doi: 10.1109/TNS.2023.3265740
[5] tinyurl.com/yxcymnd7

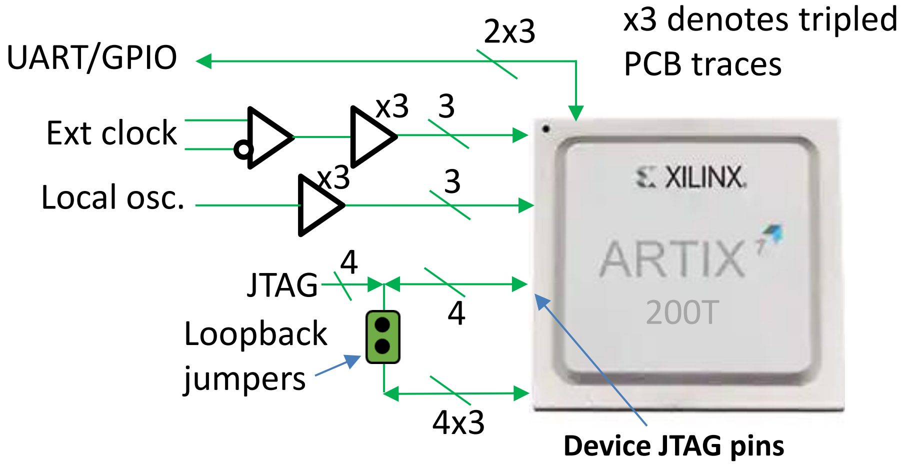
FPGA-embedded SEU Monitor

- Compact PCB
  - Only COTS components, radiation tolerance studies in [1,2]
  - Low power consumption (~0.7 W)
- AMD Artix-7 FPGA
  - 28nm CMOS
  - 59 Mb CRAM
- Radiation-Hardening by Design on PCB and firmware
  - Redundant CRAM content and self-reading firmware
- Artix-7 sensitive to fast hadrons (protons/neutrons) and thermal neutrons

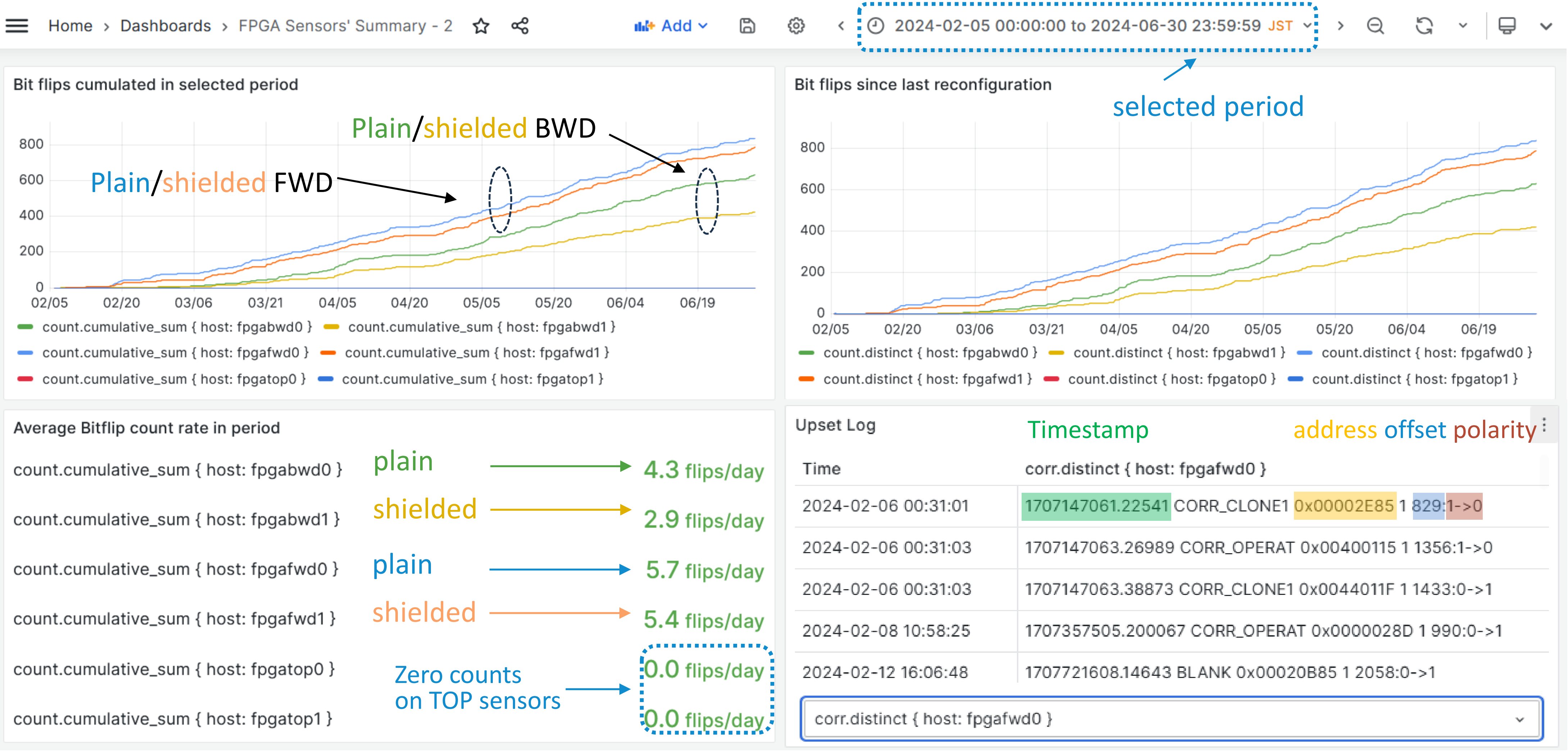
[1] T. Higuchi et al., 2012, doi: 10.1088/1748-0221/7/02/C02022

[2] Y. Nakazawa et al., 2020, doi: 10.1016/j.nima.2019.163247





Grafana Dashboard



Plain/shielded BWD

Plain/shielded FWD

selected period

Average Bitflip count rate in period

count.cumulative_sum { host: fpgabwd0 }	plain →	4.3 flips/day
count.cumulative_sum { host: fpgabwd1 }	shielded →	2.9 flips/day
count.cumulative_sum { host: fpgafwd0 }	plain →	5.7 flips/day
count.cumulative_sum { host: fpgafwd1 }	shielded →	5.4 flips/day
count.cumulative_sum { host: fpgatop0 }		0.0 flips/day
count.cumulative_sum { host: fpgatop1 }		0.0 flips/day

Zero counts on TOP sensors →

Upset Log

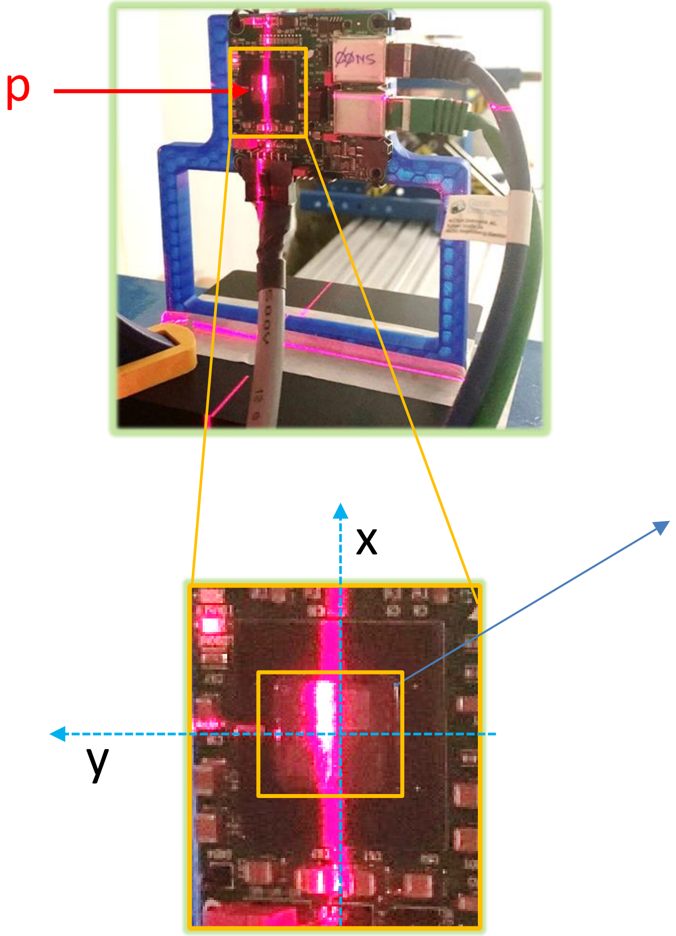
Timestamp address offset polarity

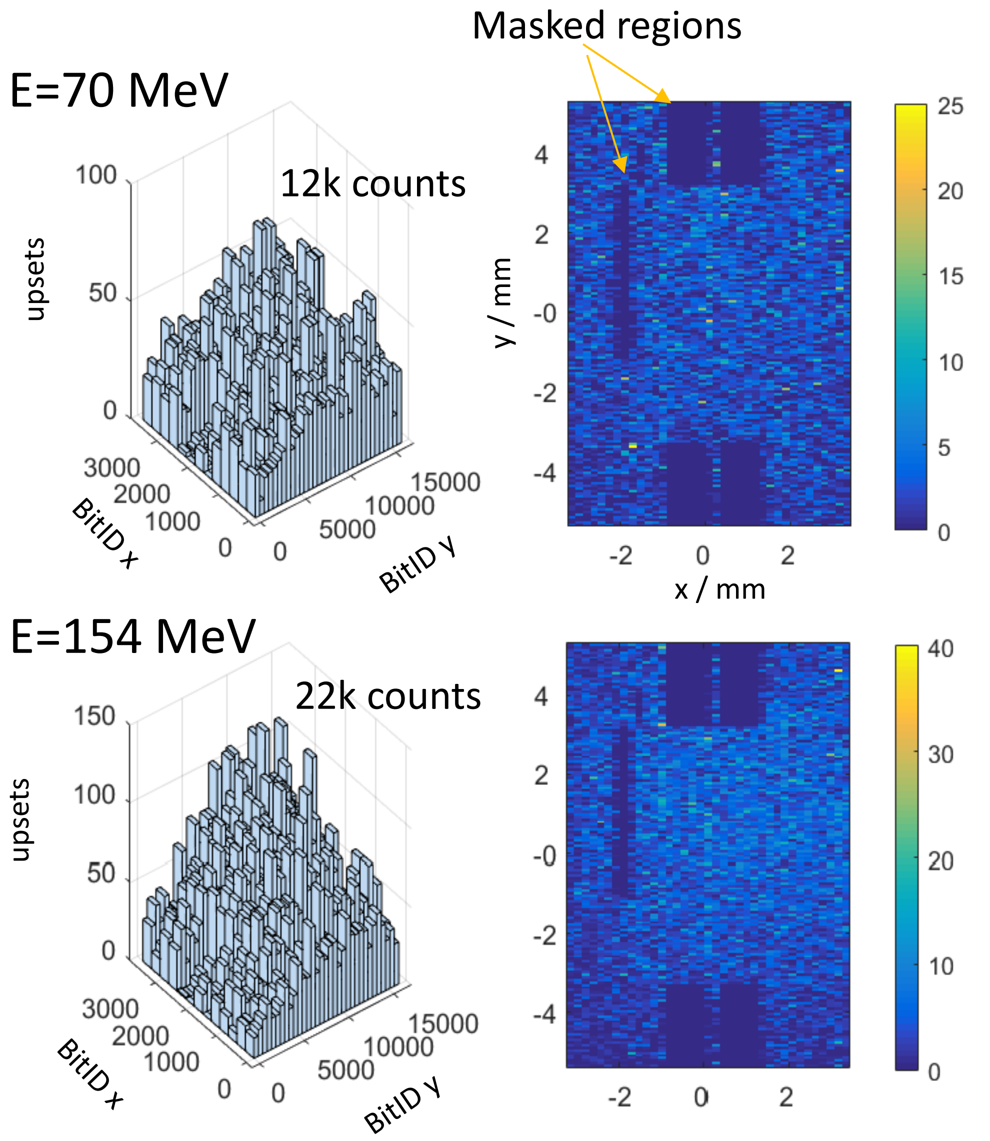
Time	corr.distinct { host: fpgafwd0 }
2024-02-06 00:31:01	1707147061.22541 CORR_CLONE1 0x00002E85 1 829:1->0
2024-02-06 00:31:03	1707147063.26989 CORR_OPERAT 0x00400115 1 1356:1->0
2024-02-06 00:31:03	1707147063.38873 CORR_CLONE1 0x0044011F 1 1433:0->1
2024-02-08 10:58:25	1707357505.200067 CORR_OPERAT 0x0000028D 1 990:0->1
2024-02-12 16:06:48	1707721608.14643 BLANK 0x00020B85 1 2058:0->1

corr.distinct { host: fpgafwd0 }

Imaging the Beam with an FPGA

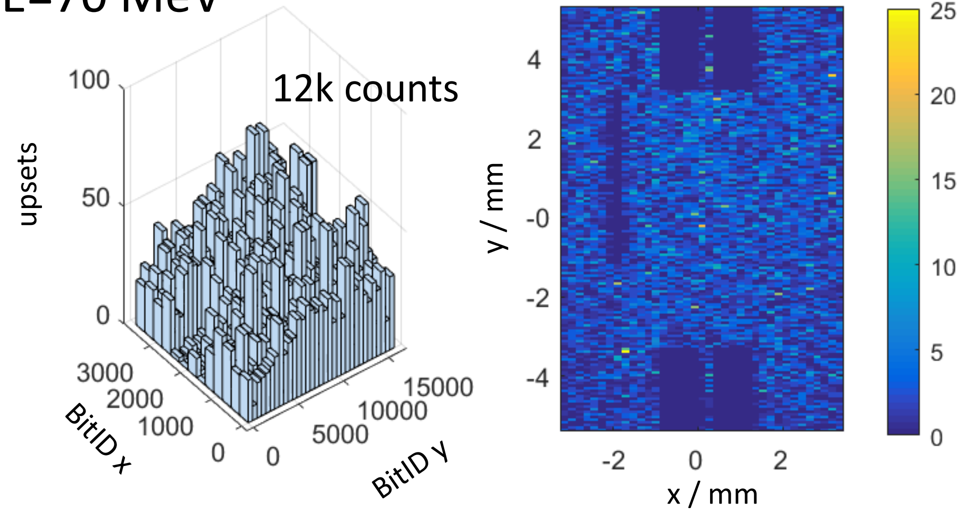
- Readback CRAM bitmap
- Cluster adjacent bits, 1 cluster = 100 bits x 100 bits
- Upsets per cluster => histogram and density map
- Approximate proton beam image
- Masked regions



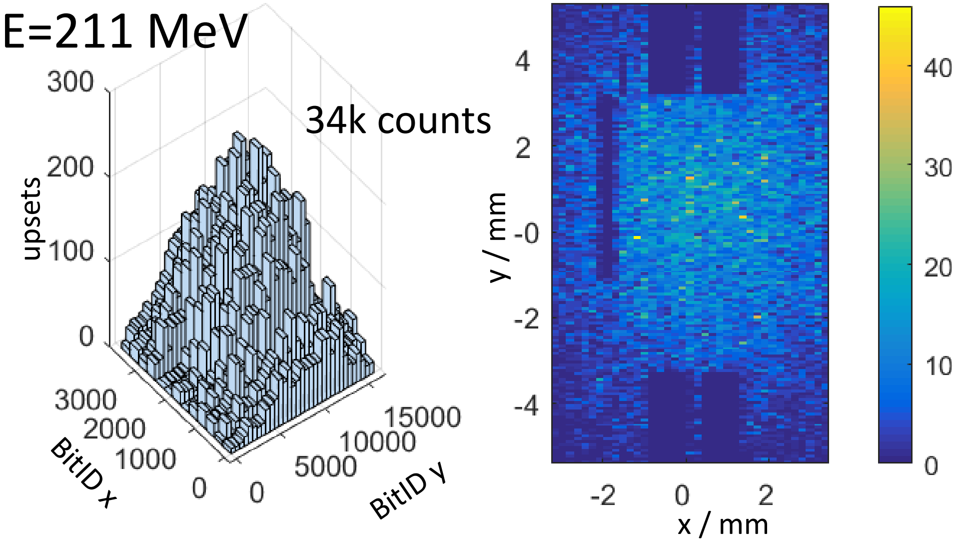


Beam Image Vs Proton Energy

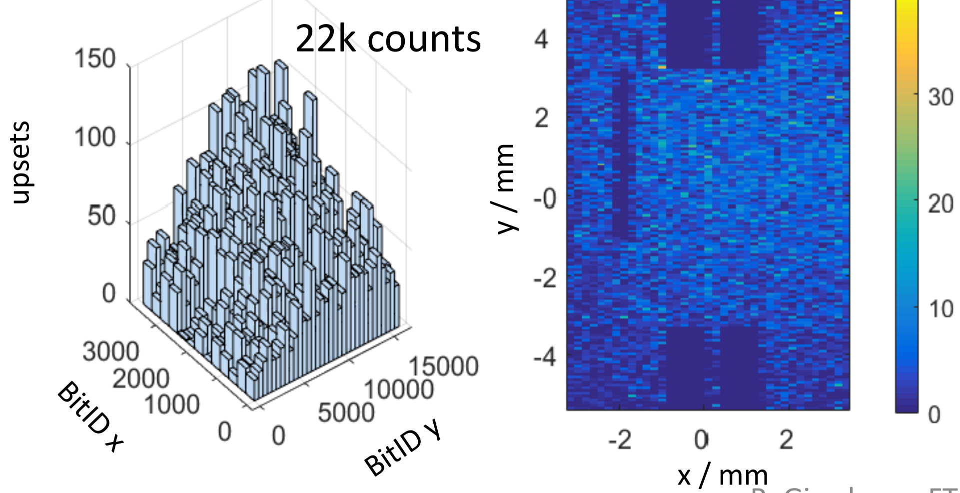
E=70 MeV


12k counts

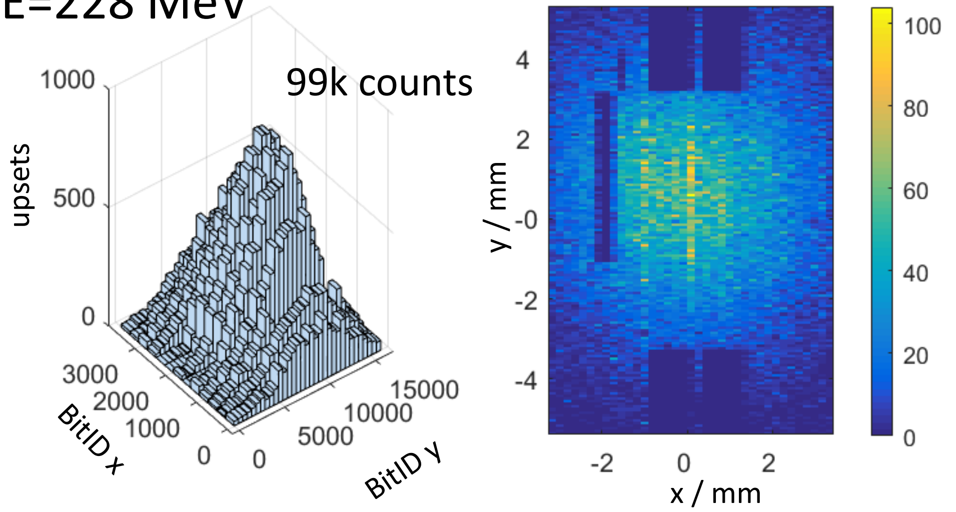
E=211 MeV


34k counts

E=154 MeV

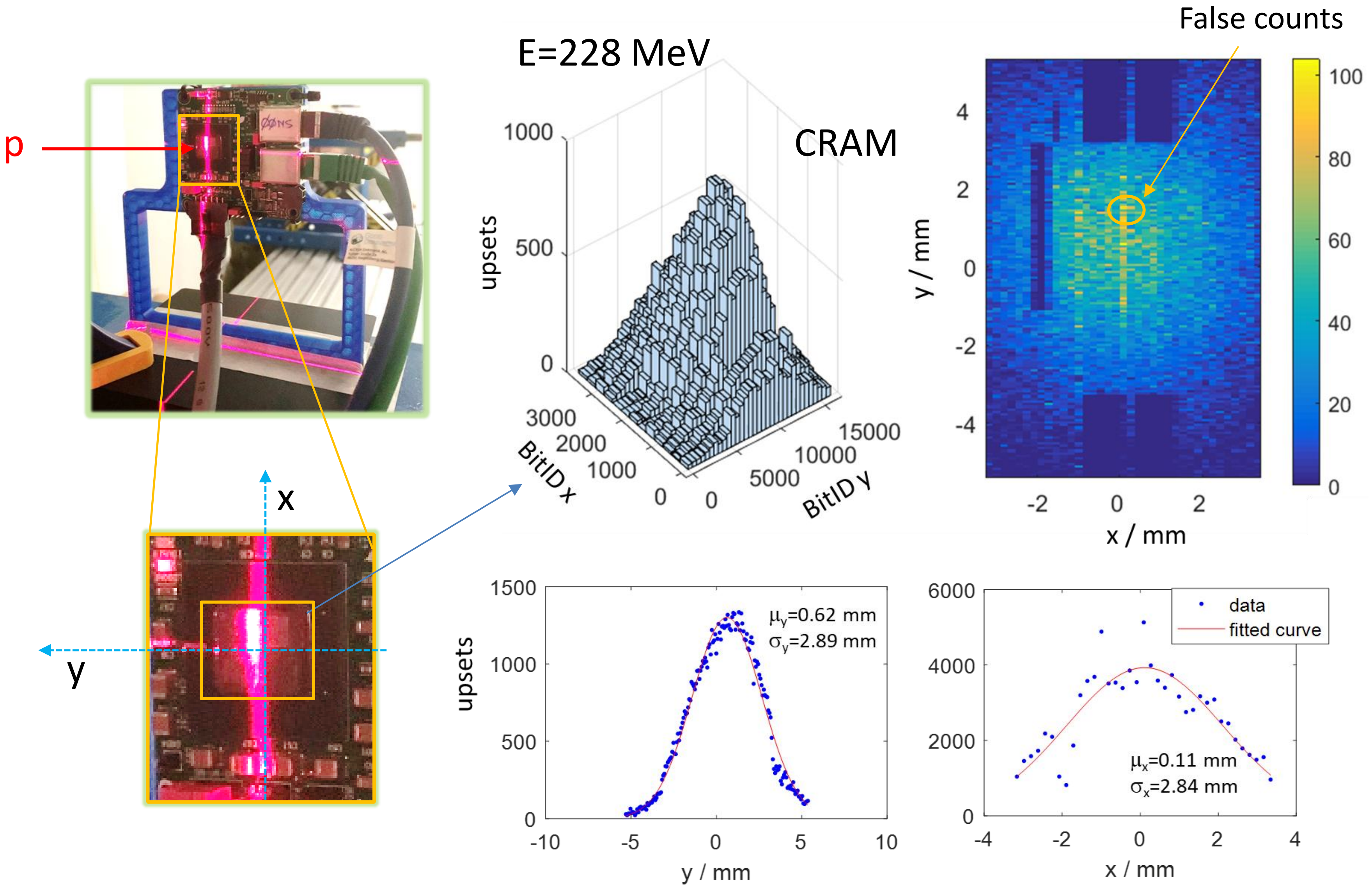

22k counts

E=228 MeV


99k counts

Imaging the Beam with an FPGA (2)

- Useful to check sample alignment and estimate proton fluence
- CRAM access logic SEFIs => false counts
- JTAG failed (13 times), but very reliable
  - $\sigma_{JTAG} = 1.0 \pm 0.2 \cdot 10^{-12}$ cm^2



SWX-238 Specs

Thermal Neutron One-Tenth Thickness: 0.048 inch
Thickness of SWX-238 required to reduce incident flux of thermal neutrons by a factor of 10 (exit thermal flux is 10% of incident thermal flux)

Composition Data

Hydrogen atom density / cm^3:	2.70 x 10^{22}
Hydrogen weight percent:	2.76 %
Boron atom density / cm^3:	2.51 x 10^{22}
Boron natural isotope distribution:	19.6 % ^{10}B and 80.4% ^{11}B
Boron weight percent:	27.6 %
Total Density:	1.64 g / cm^3 (102 lbs. / ft^3)

Radiation Properties

Macroscopic thermal neutron cross section:	18.9 (cm^{-1})
Gamma resistance:	1 x 10^{10} rad
Neutron resistance:	5 x 10^{18} n/ cm^2

Element	**Percent by Weight**	**Number of atoms/cc**
Boron	27.55	2.51 x 10^{22}
Silicon	26.85	9.41 x 10^{21}
Oxygen	23.57	1.45 x 10^{22}
Carbon	18.69	1.53 x 10^{22}
Hydrogen	2.76	2.70 x 10^{22}

Thickness of SWX-238 required to reduce to thermal 90% of an incident neutron flux, as a function of initial neutron energy (exit epithermal flux is 10% of incident neutron flux)