Study of cluster counting method for CEPC drift chamber

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On behalf of CEPC drift chamber group

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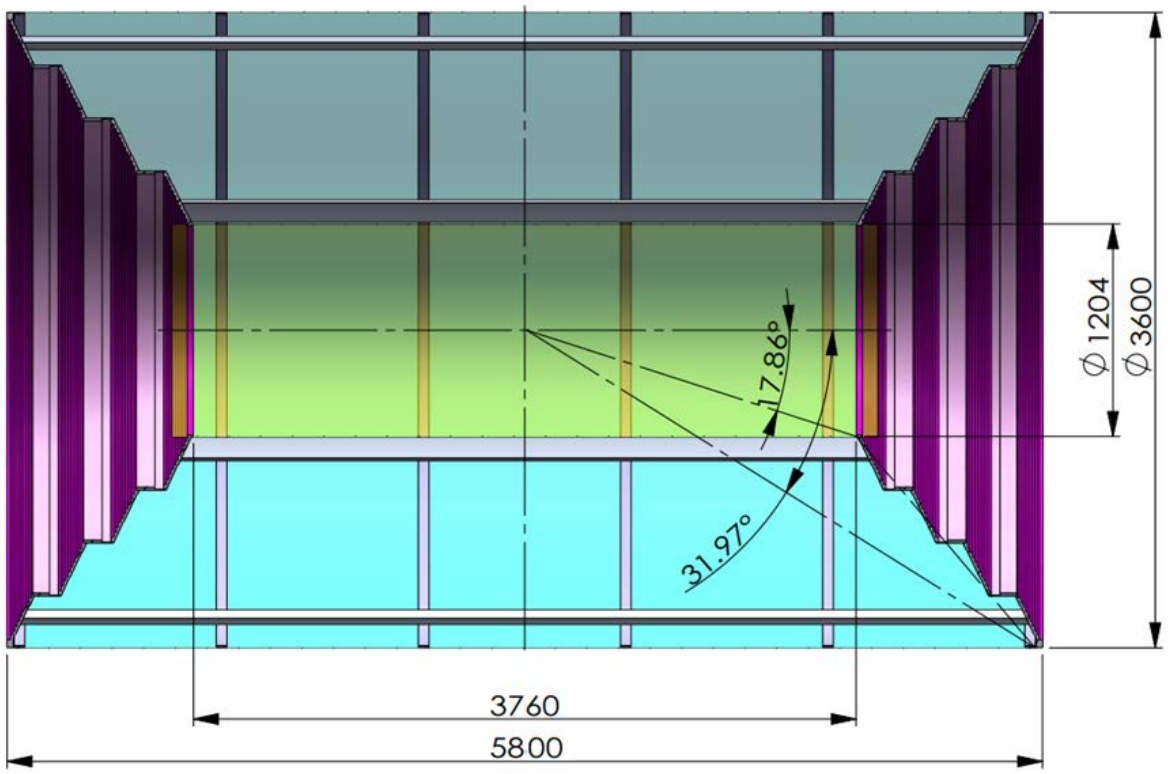
Outline

- Introduction of drift chamber for CEPC
- Simulation study
- Progress of a prototype test system
- Summary

Drift Chamber in CEPC reference detector



- PID is essential for CEPC, especially for flavor physics study

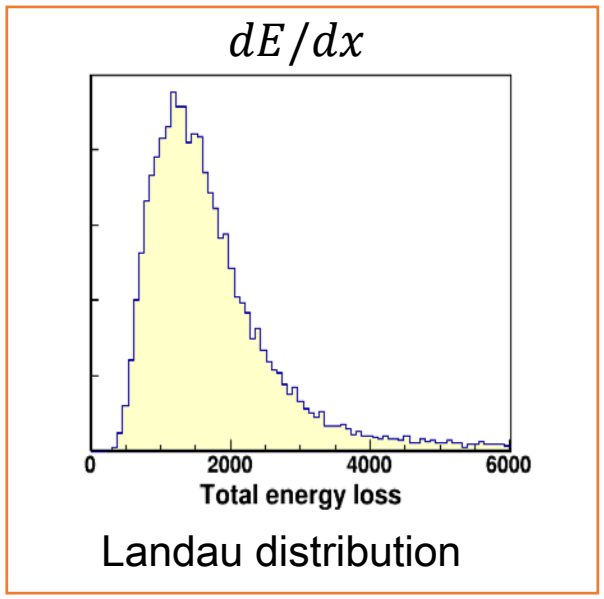
- Drift chamber is an alternative option for CEPC gaseous tracker in CEPC reference detector design

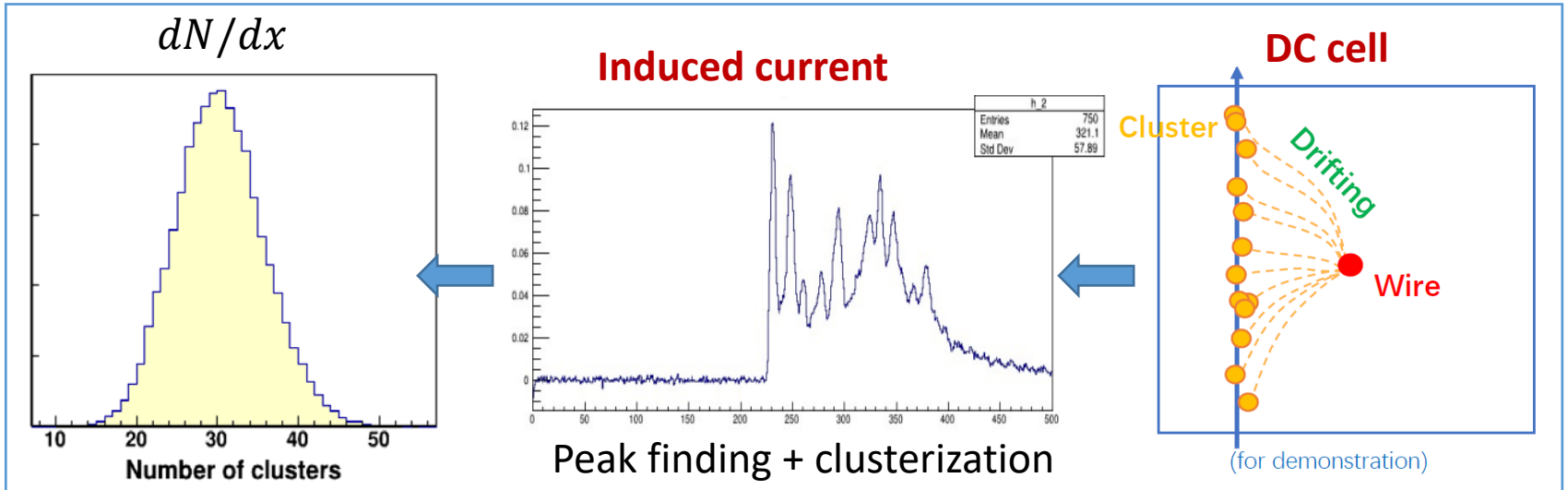
- Besides momentum resolution, PID capability is another important parameter to be optimized
- Design goals: Provides better than 3σ separation power for K/π with momentum up to 20GeV/c

Preliminary design parameters of DC

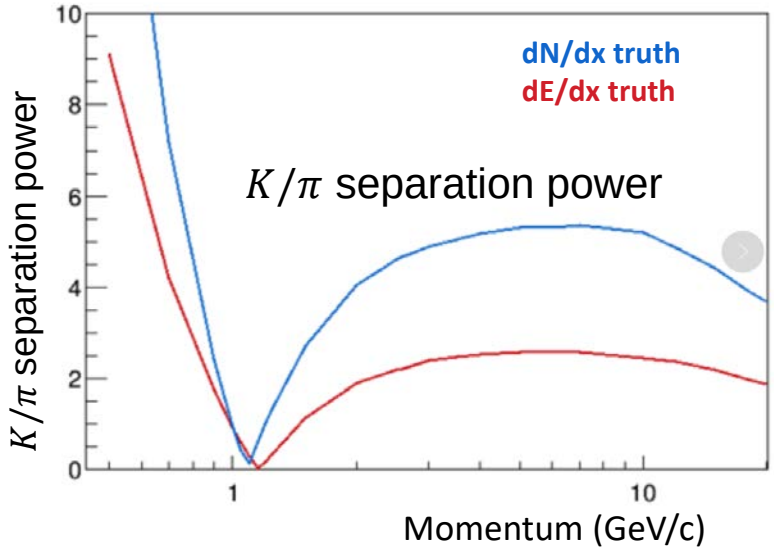
R extension	600-1800 mm
Length （cosθ=0.85）	5800 mm
inner and outer CF cylinder: for gas tightness, without load	Thickness: ~ 300 μm
CF frame structure	8 longitudinal hollow beams + 8 annular hollow beams
Al end plates:	Thickness: 20 mm
Cell size:	~ 18 mm × 18 mm
Layer and cell number:	64 layer and 26483 cells
Ratio of field wires to sense wires	3:1
Gas mixture	He/iC_4H_{10} = 90:10

Cluster counting (dN/dX) method





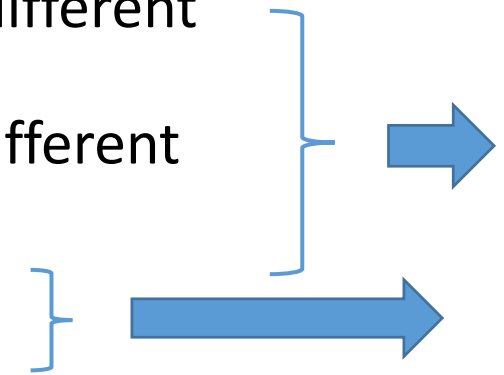
- dN/dx : Measure number of primary ionization over the track
- Yield of primary ionization is Poisson distribution
- Small fluctuation



Simulation： dN/dx has a much better (2 times) K/π separation power than dE/dx

Key issues for DC with dN/dx measurement

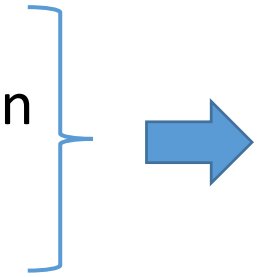
- Challenges in waveform precision testing
  - Sufficient time interval between different ionization signals
  - Reducing interference between different ionization clusters
  - Low noise and sufficient SNR
  - Fast signal shaping



✓ Detector optimization: Cell size, HV, and Gas mixture (low drift velocity, low diffusion, suitable ionization density)

✓ Fast and low noise electronics

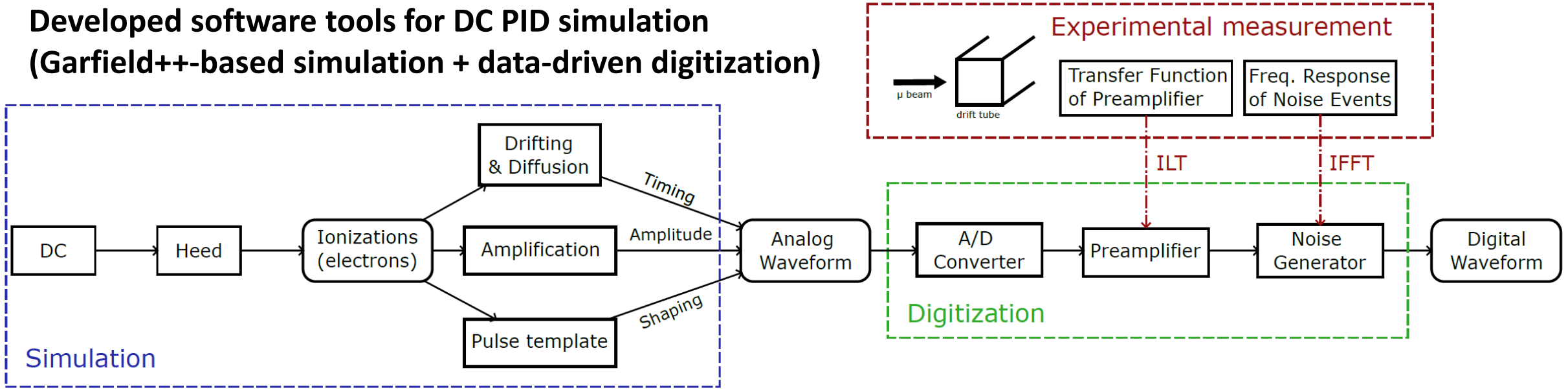
- Challenges in reconstruction algorithm
  - Processing piled-up signals
  - Identifying primary and secondary ionization signals
  - Reducing noise impacts



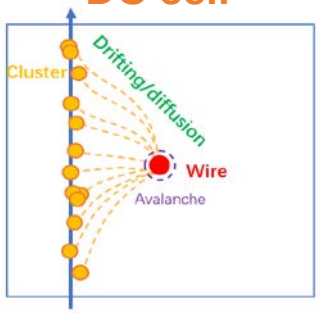
✓ Improve the reconstruction efficiency and purity

Waveform-based full simulation

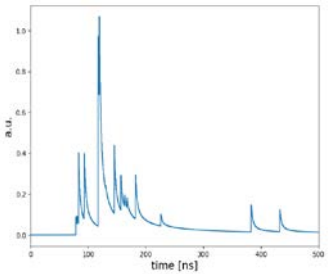
Developed software tools for DC PID simulation (Garfield++-based simulation + data-driven digitization)



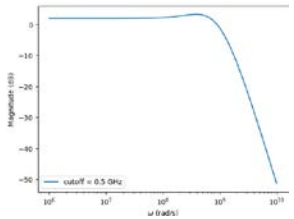
DC cell



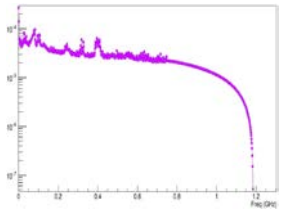
Induced signal



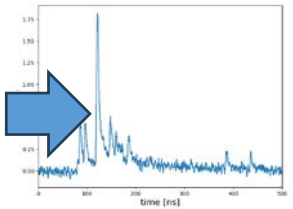
Preamplifier

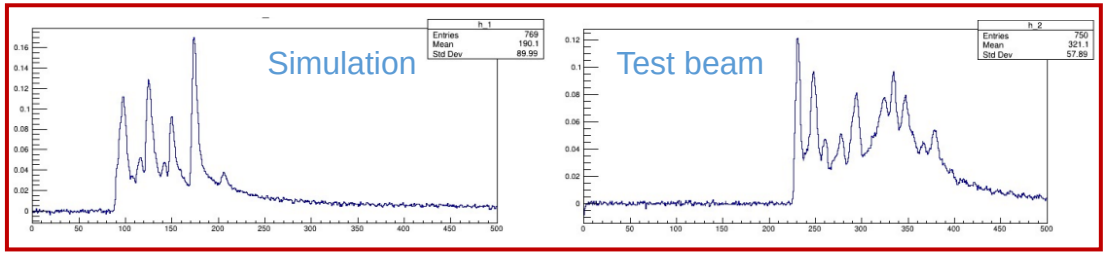


Noise



Waveform



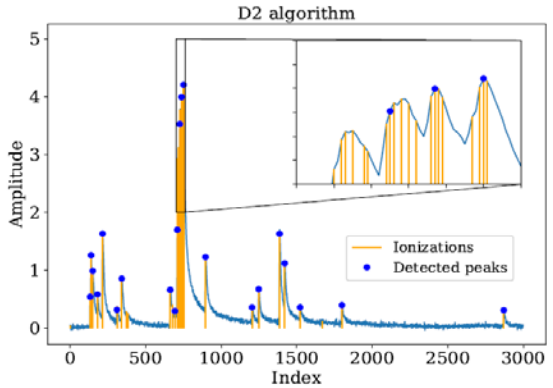


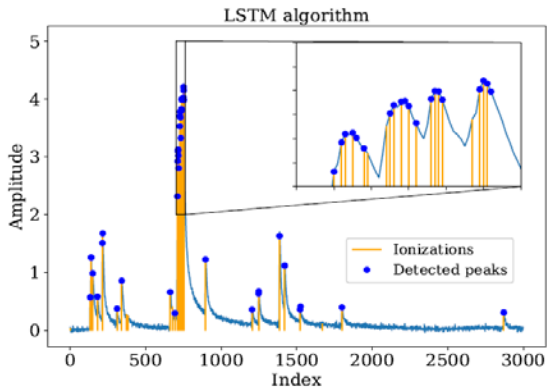
Tuned MC is comparable to data

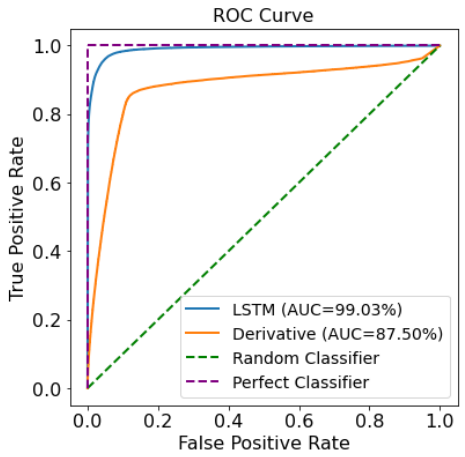
Machine learning reconstruction algorithm

- LSTM-based peak finding and DGCNN-based clusterization
- ~ 10% improvement of PID performance with ML

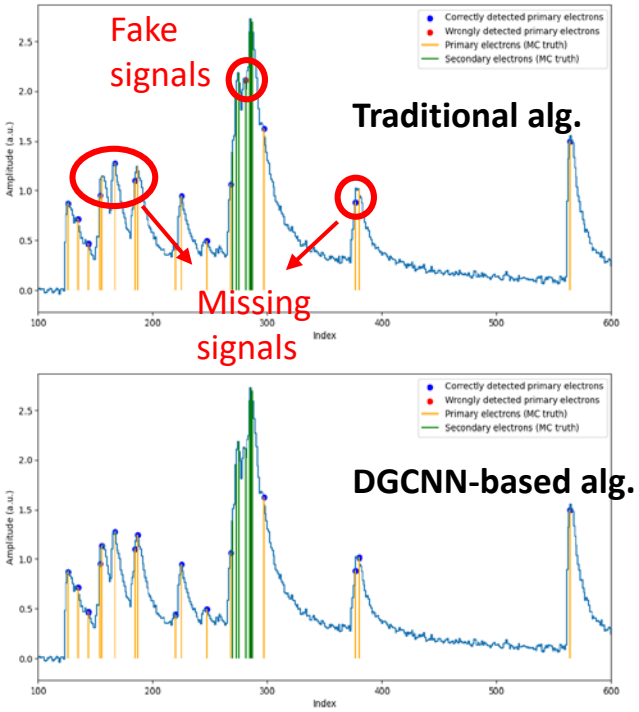
Long Short-Term Memory (LSTM)-based peak finding
higher efficiency than the derivative-based algorithm, especially for the pile-up recovery

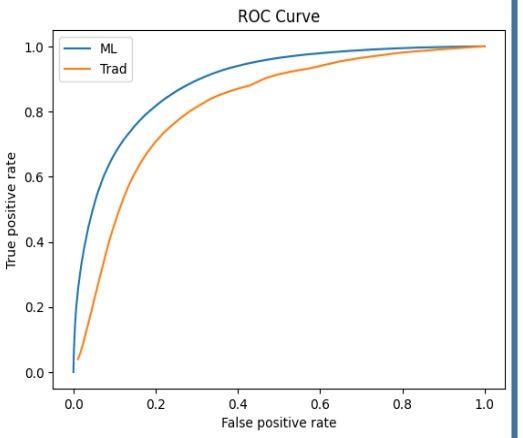






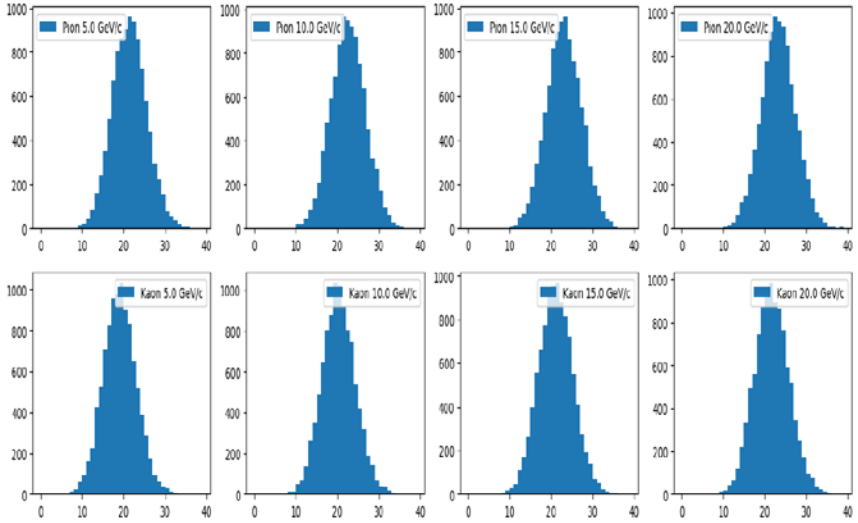
Dynamic Graph CNN (DGCNN)-based clusterization
higher efficiency, and lower fake rate



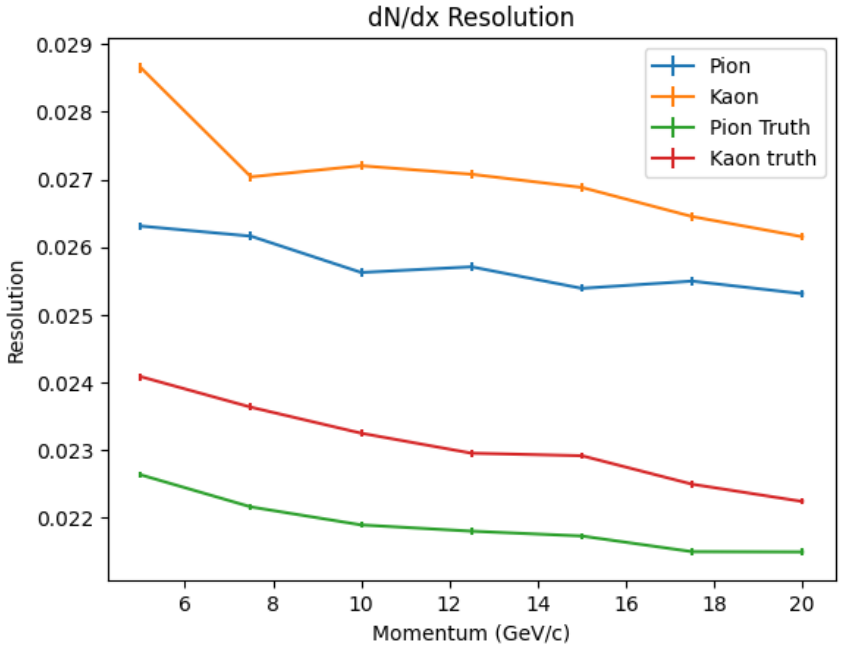


dN/dx Resolution

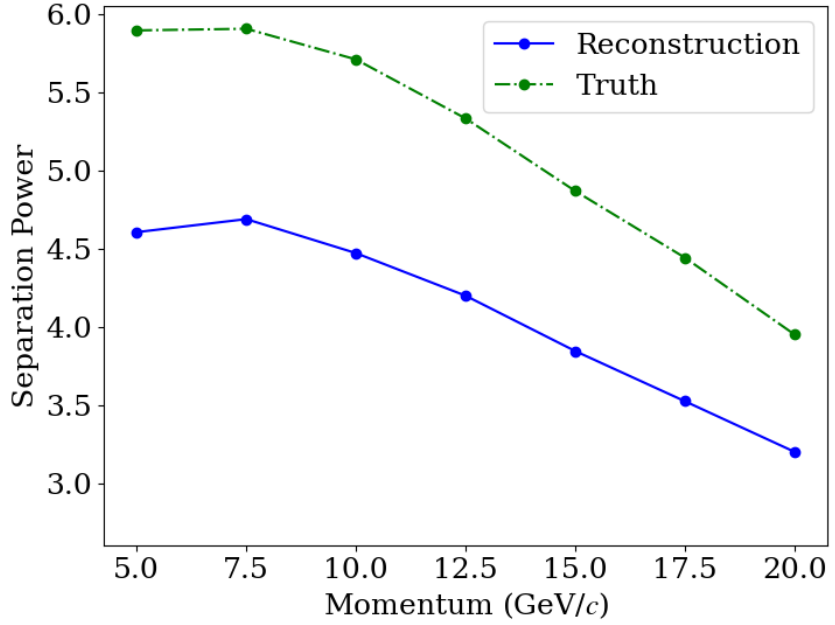
Reconstructed # of clusters distributions



The reconstructed n_{cls} distributions are very well Gaussian-like



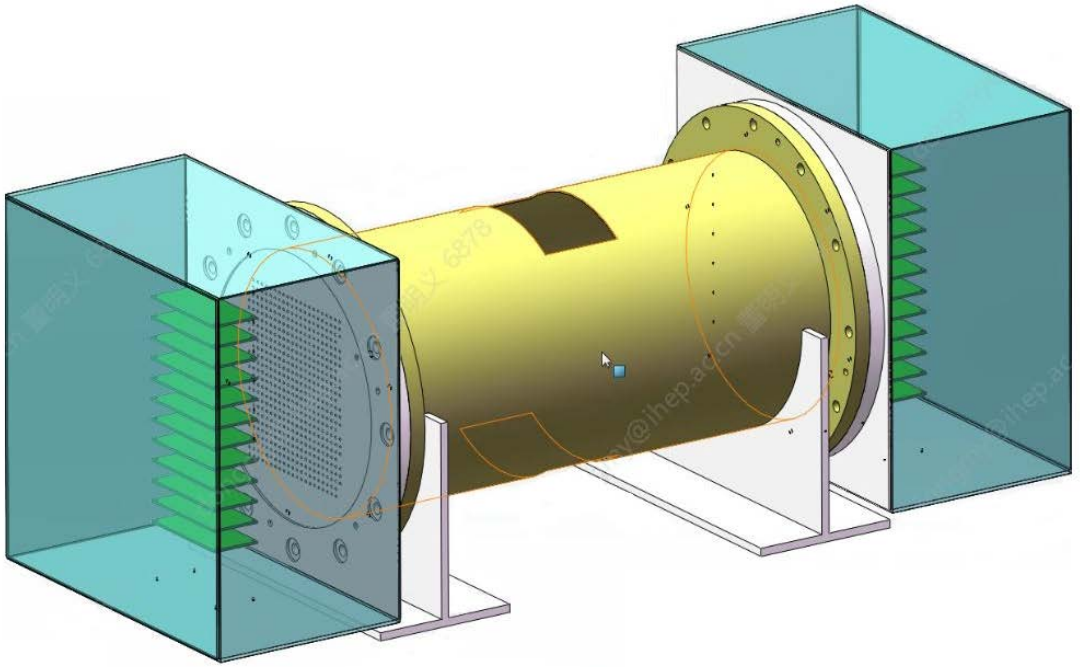
- dN/dx resolution (1.2 m track length):
  - 2.5%-2.6% for Pion
  - 2.6%-2.7% for Kaon

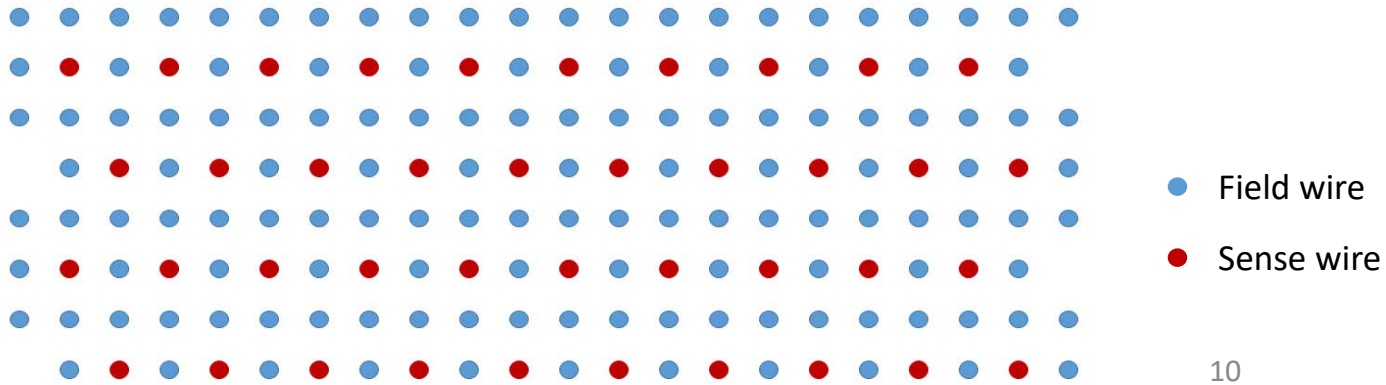


- 1.2 m track length
- For 20 GeV/c K/π, Separation power: 3.2σ

Design of a multi-layer DC prototype

- A prototype was designed for dN/dx resolution study
- Design parameters
  - 12 layers, 10 cells/ layer
  - Length: 60 cm
  - Cell size : 18 mm × 18 mm
  - Sense wire: 20 μm Au-plated tungsten
  - Field wire: 70 μm aluminum

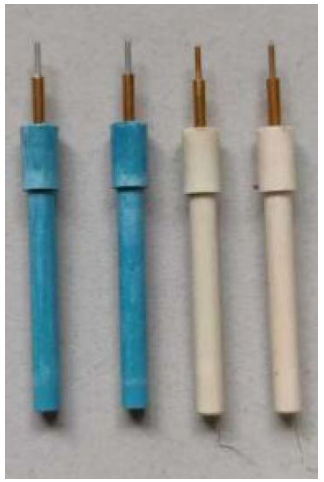




Construction of the prototype

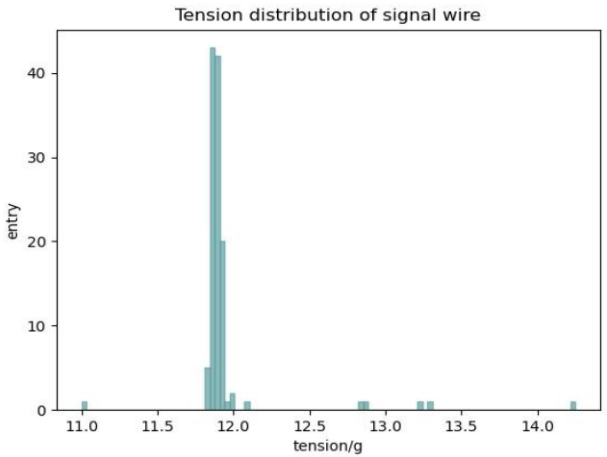
- Wiring, tension test, leakage current test and HV training
  - sense wires tension: 11 g
  - field wires tension: 19 g
  - Deflection: 25 μm
  - Leakage current: < 1 nA

wire

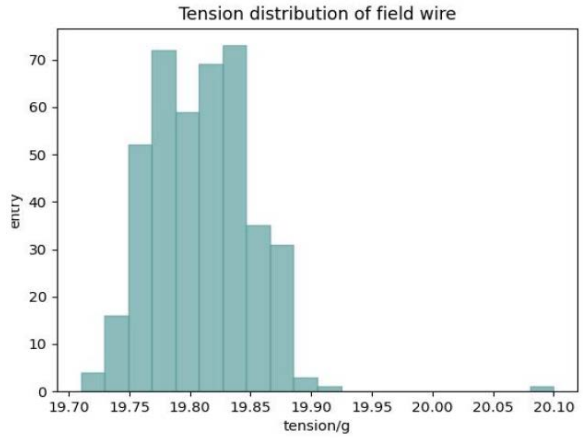


Feedthrough

wiring



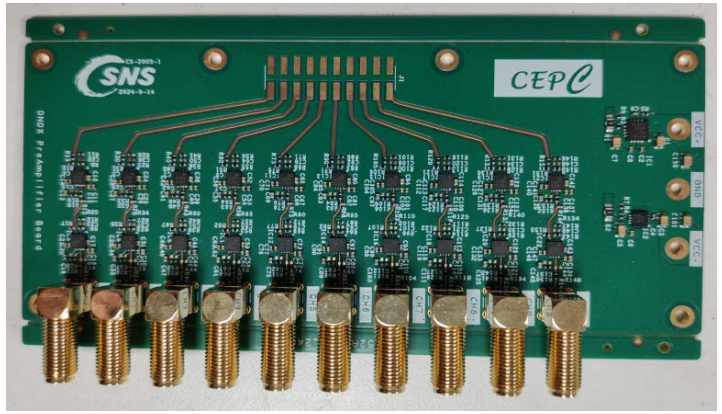
Tension of SW

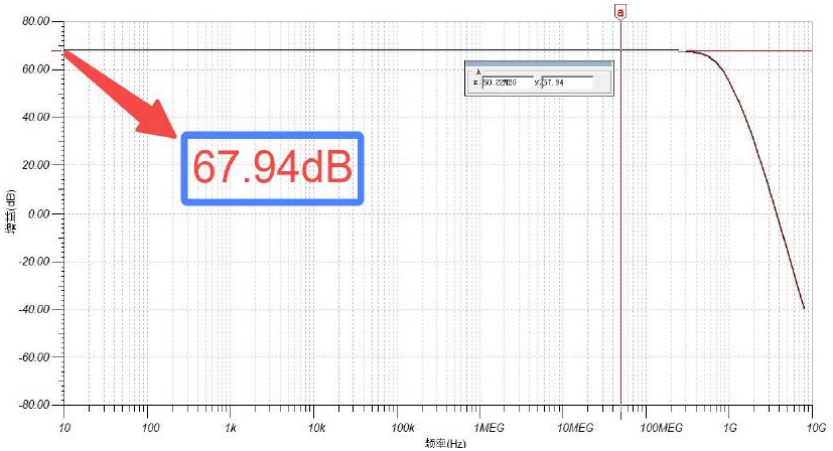


Tension of FW

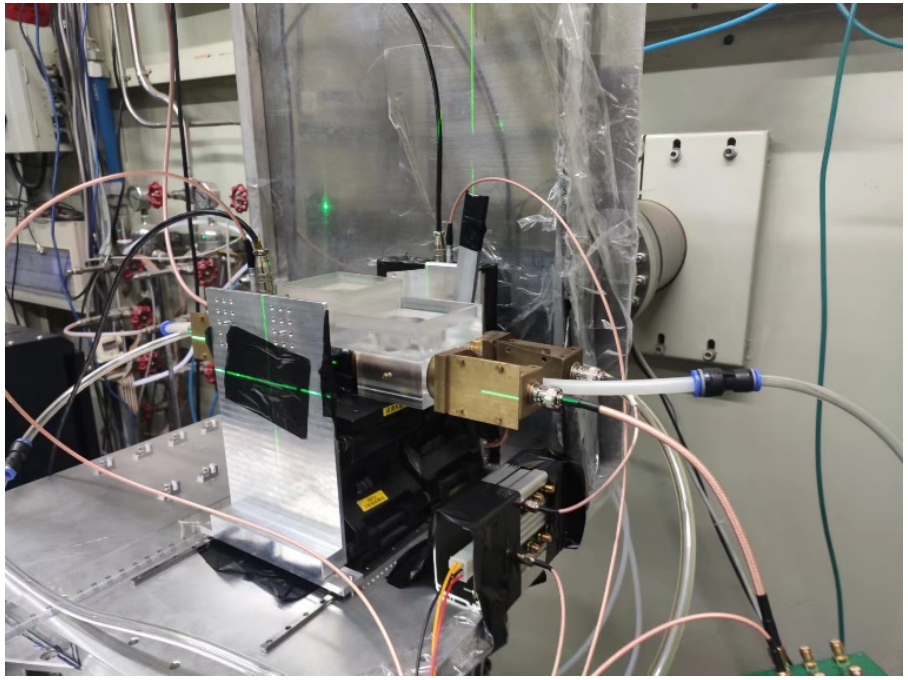
Preamplifier design and test

- Fast current preamplifier based on LMH6629 chips
- High gain, high bandwidth and low noise
  - Current gain： 67.94 dB
  - Bandwidth: 587.74MHz @-3dB
  - Baseline noise: 1.53 mVrms

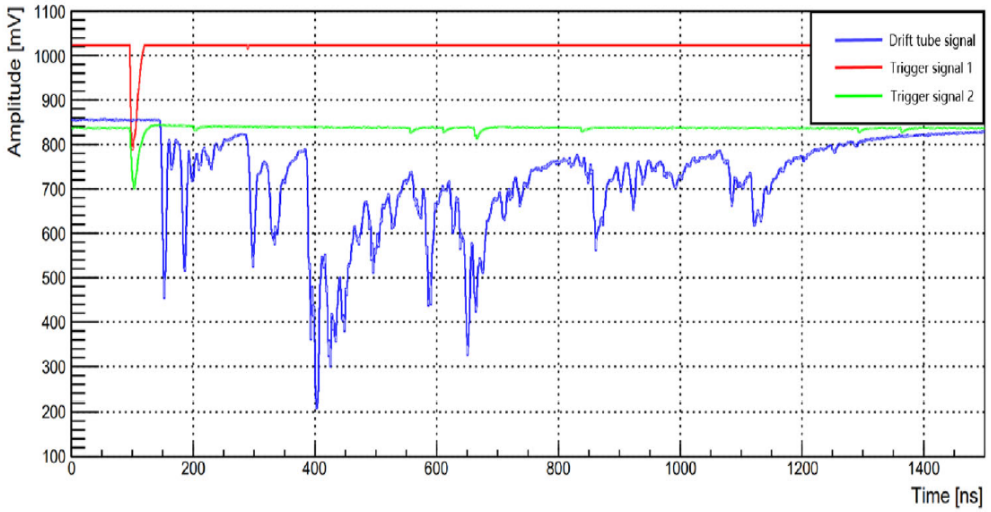




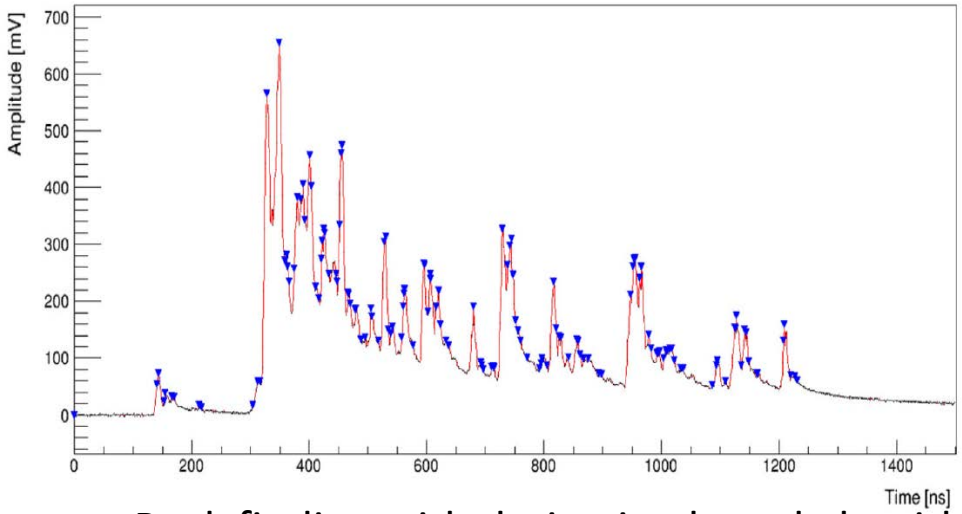
- Beam test has been conducted for performance verification
  - Drift tubes + preamps + ADC (DT 5751 digitizer with 1GHz sampling rate)
  - Two scintillators provide trigger signals



Test results

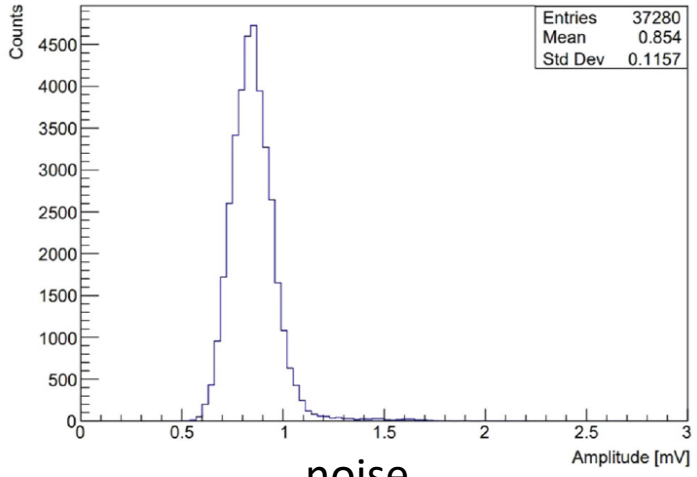


waveform

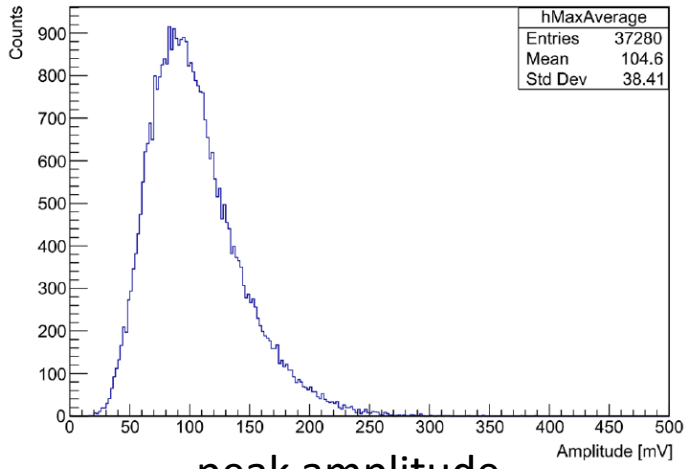


Peak finding with derivative-based algorithm

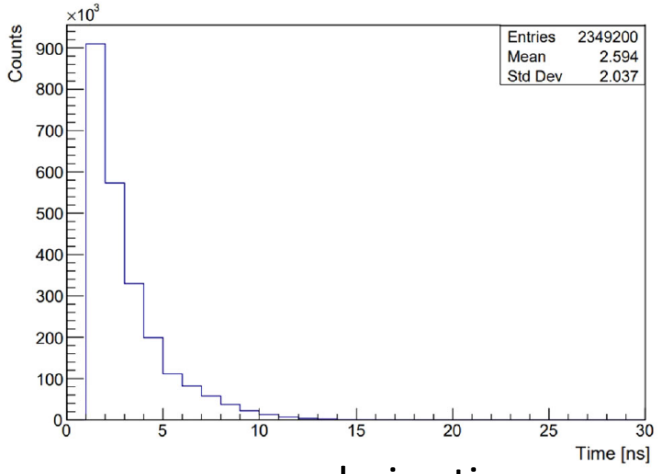
- Clear peaks
- Rise time : ~ ns



noise



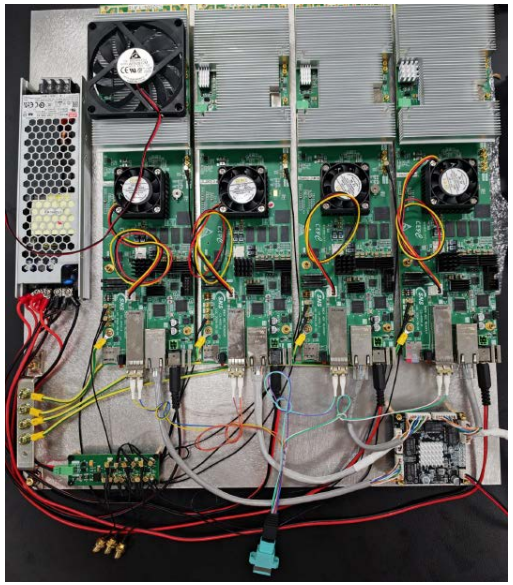
peak amplitude



peak rise time

Readout electronics

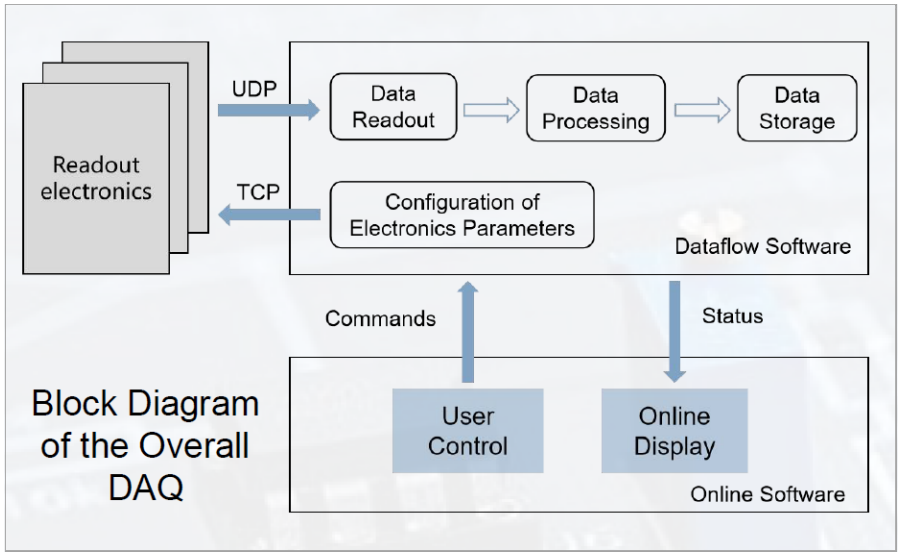
Digitization and FPGA board

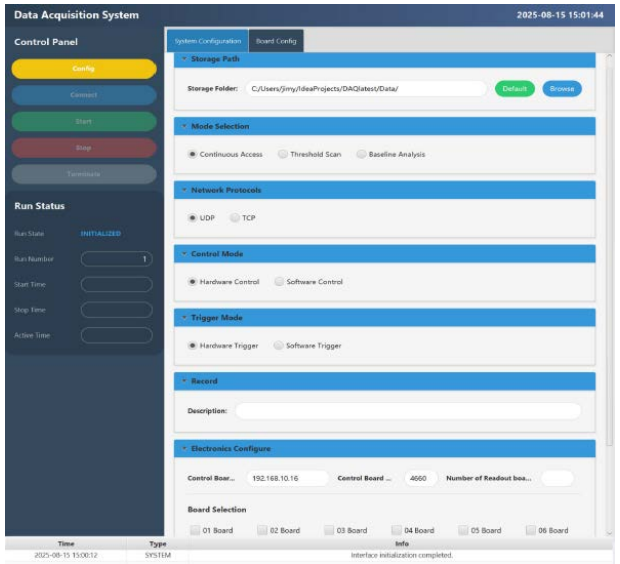


40 channels crate

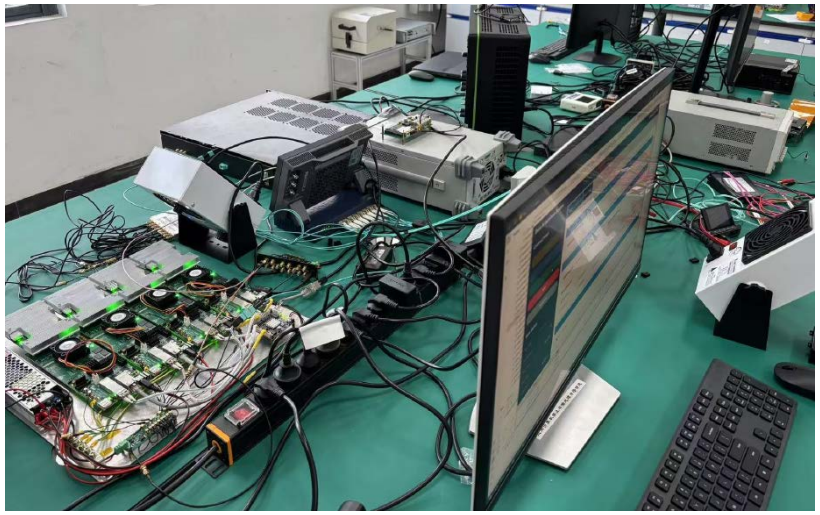
- ADC mezzanine board
  - Sampling rate: 1.3 Gsps, resolution: 14 bit
  - Power consumption: 750 mW/channel
- FPGA readout board
  - Receive data streams from five AD9695 ADCs via 13 Gbps JESD204B links
  - Send processed data to the DAQ server via 10 Gbps UDP links
- Each crate contains 40 digitization channels

DAQ

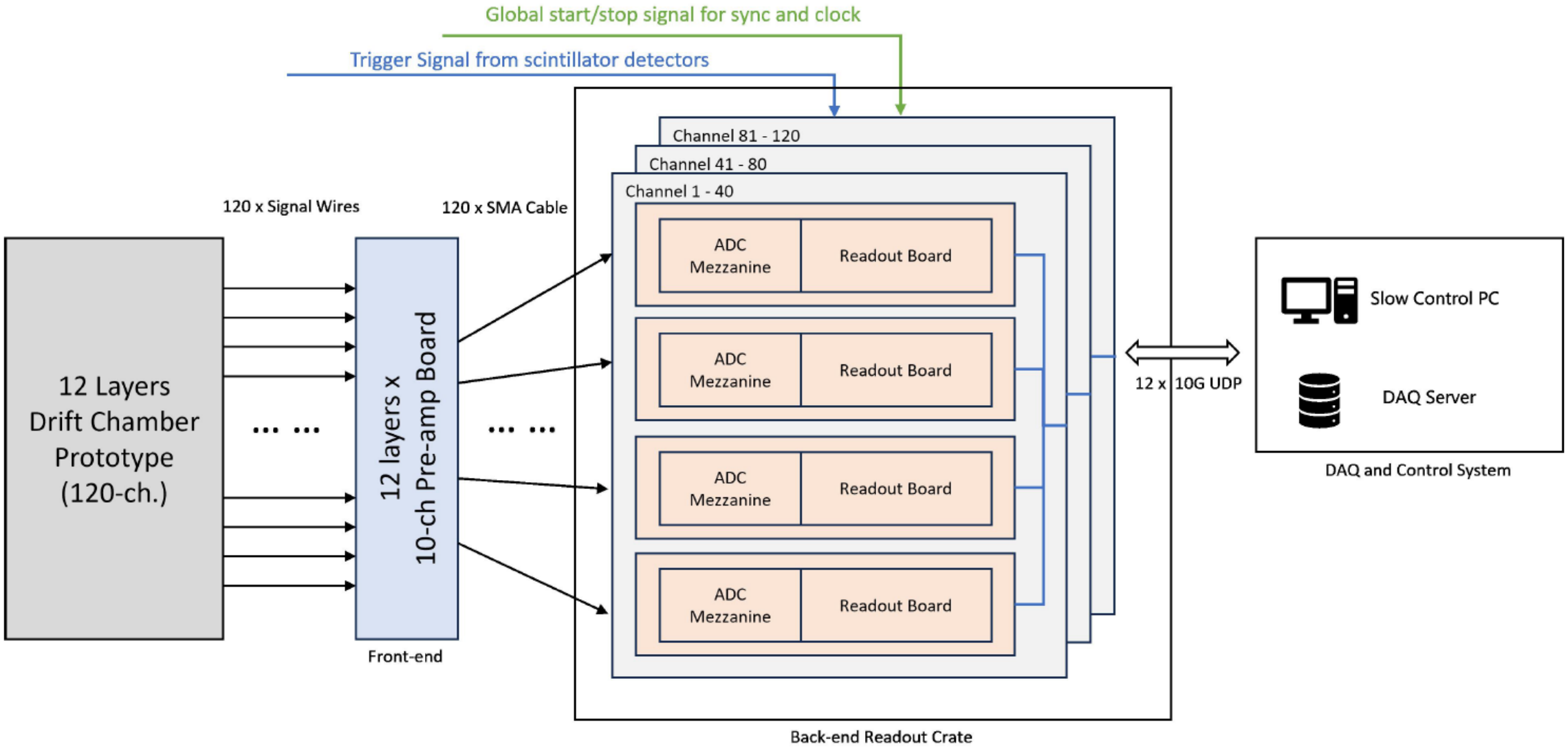




- Transmit data by UDP,
- Configure electronics by TCP
- Dataflow Software
  - Read out , check, configure, …
- Online Software
  - Data check, online data process, …



Testing system setup



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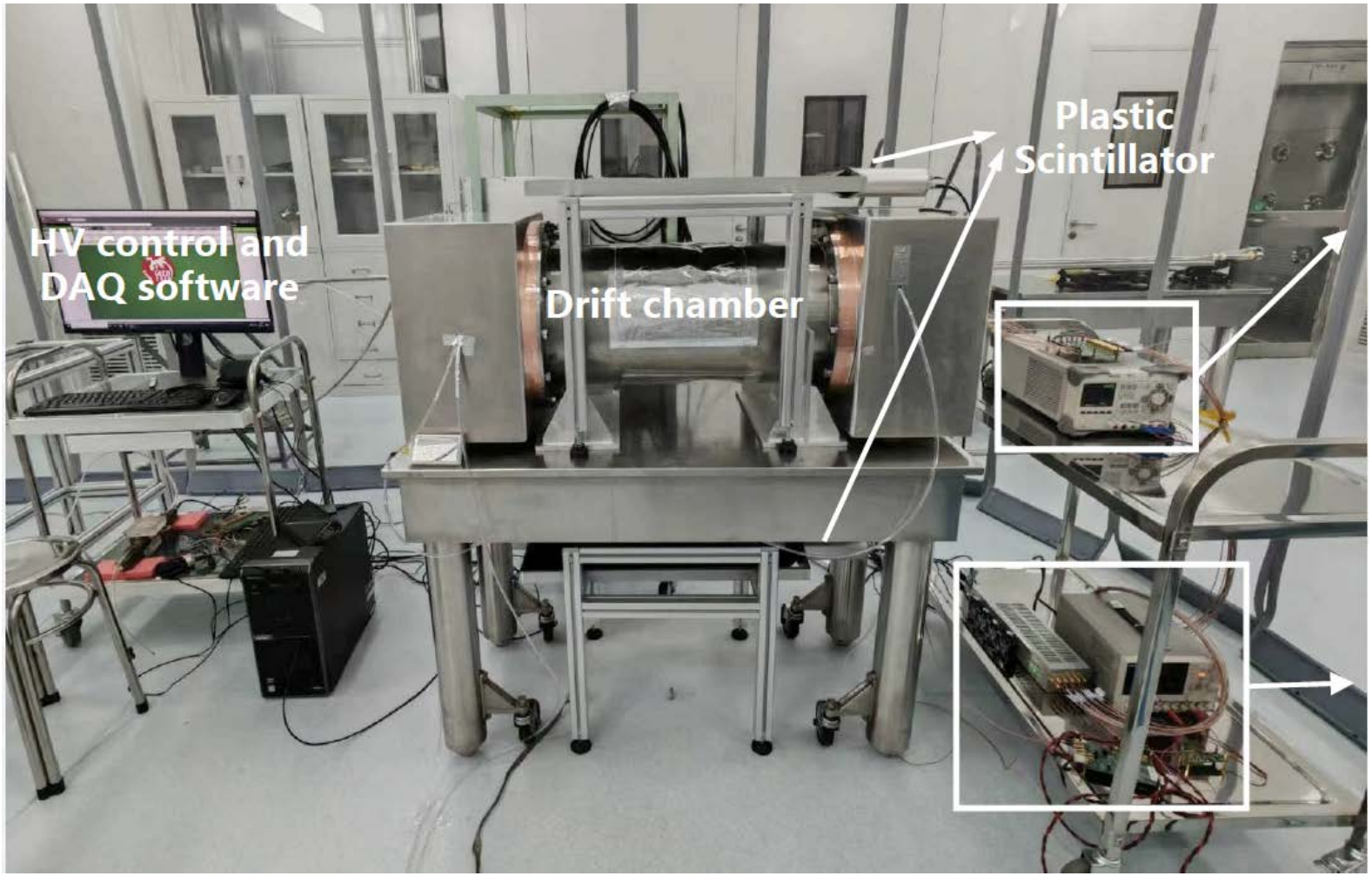
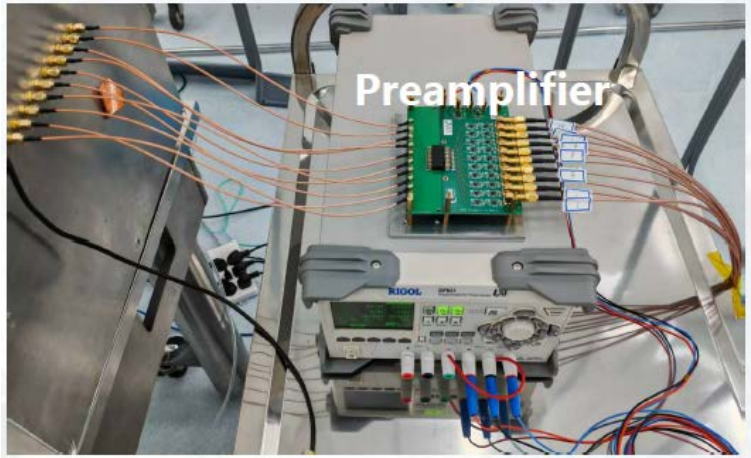
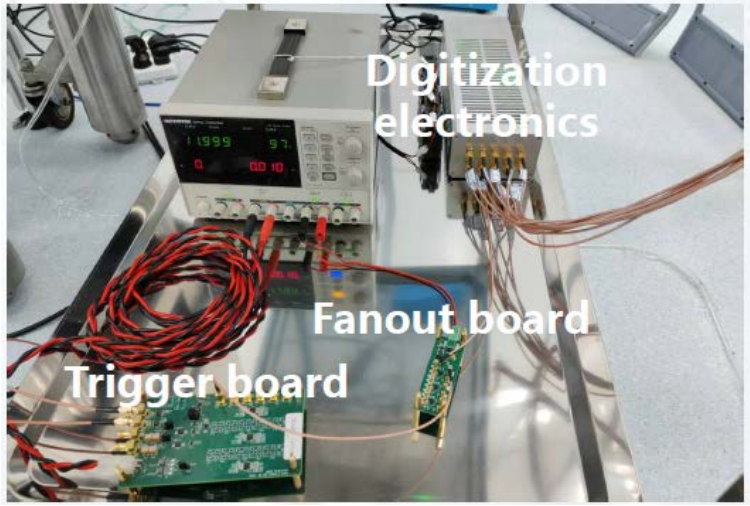
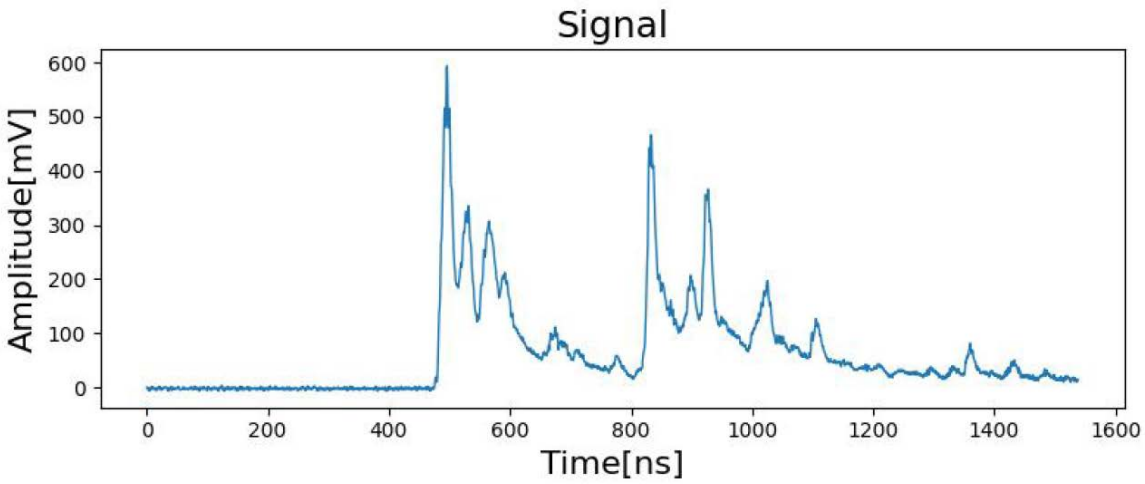
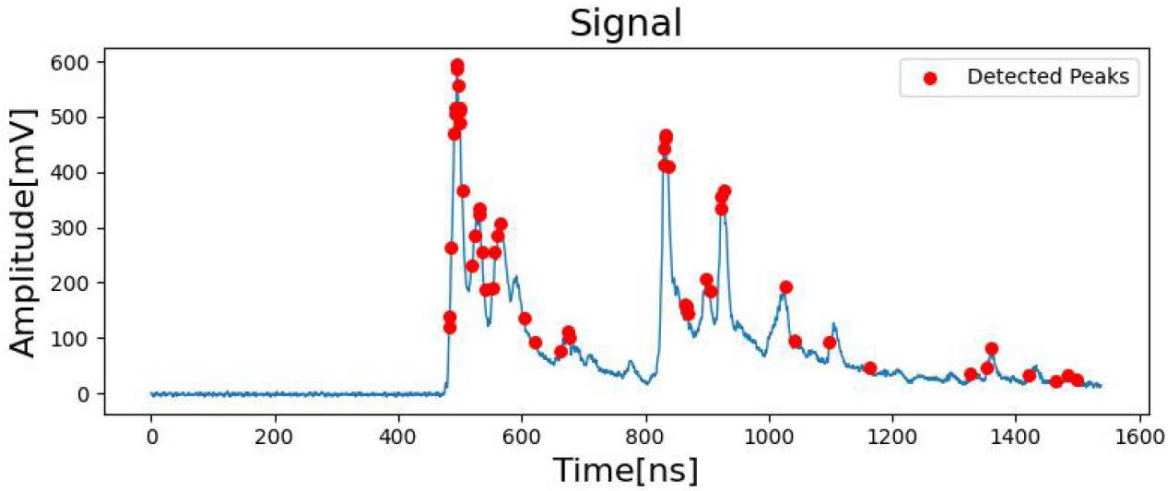


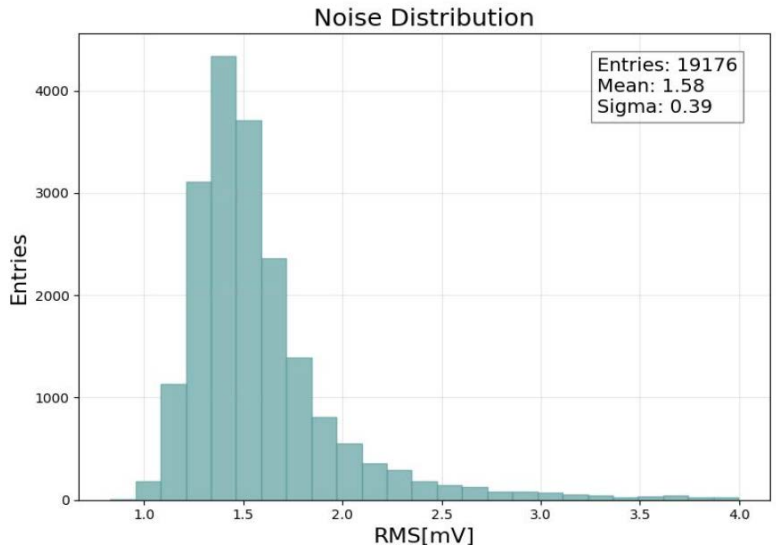


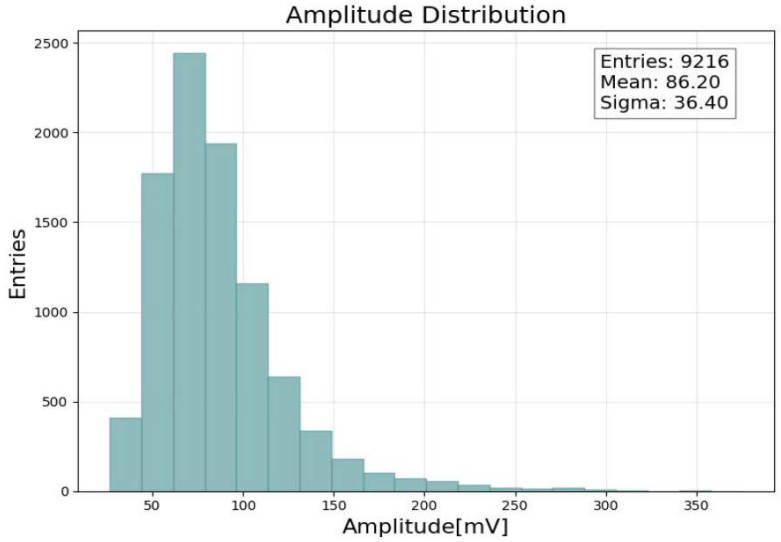


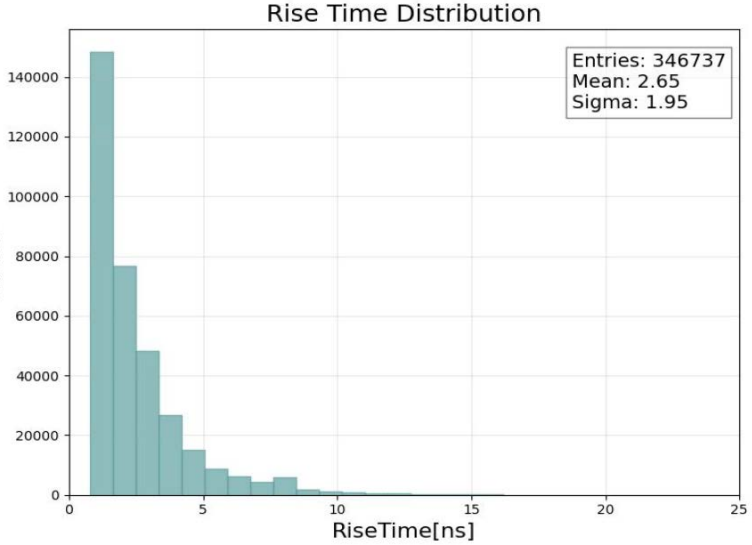
Preliminary cosmic-ray test



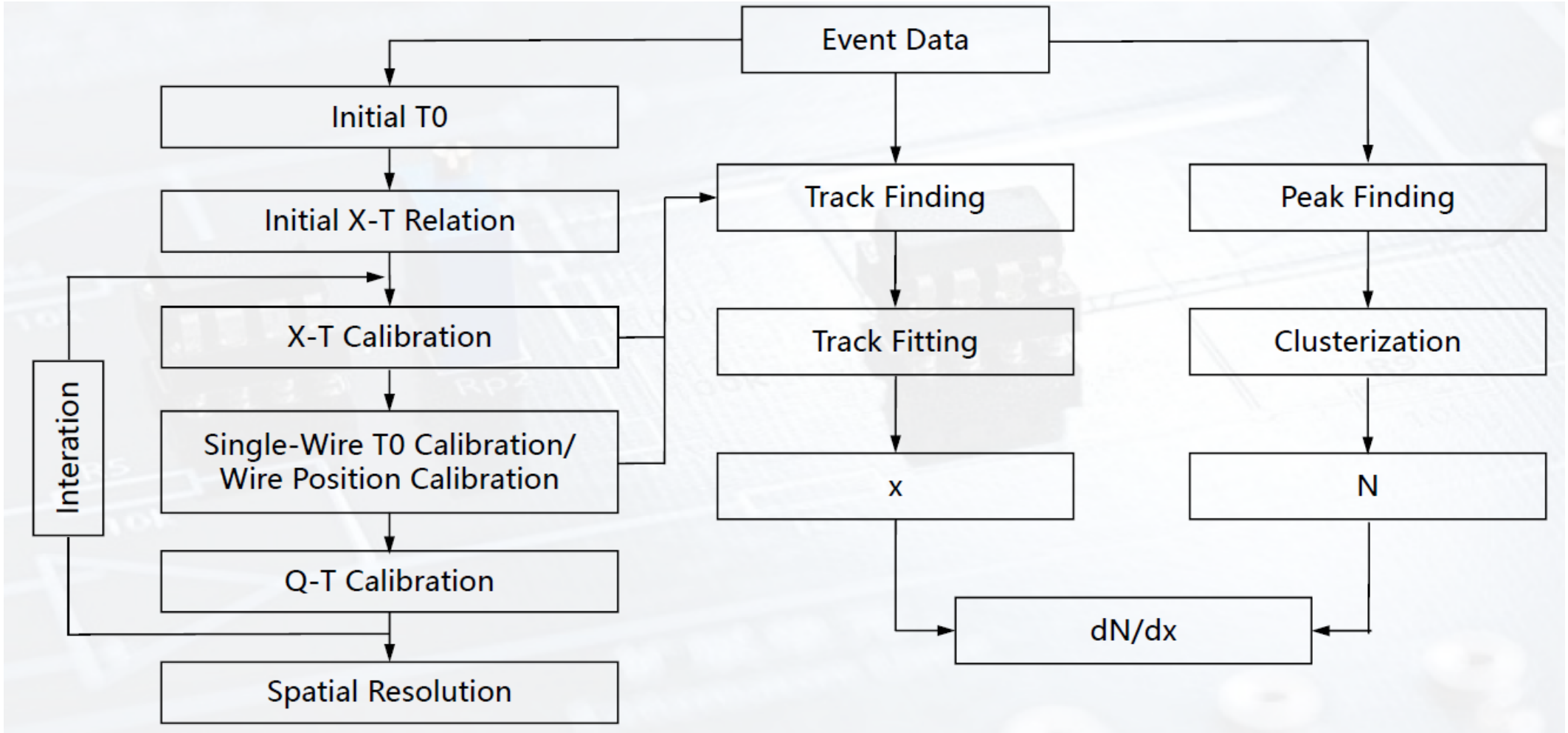






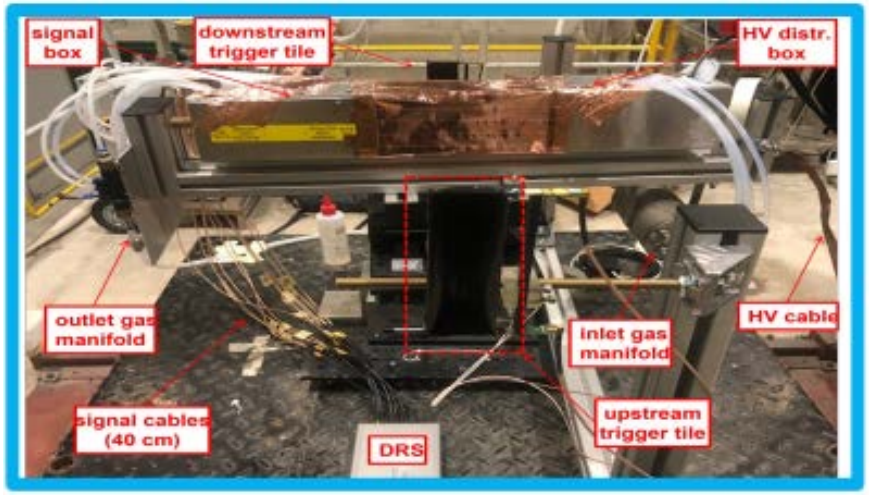


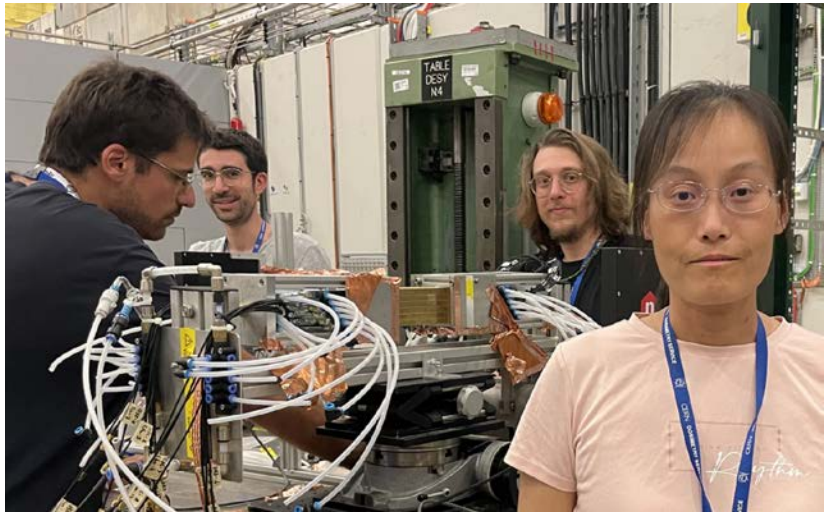
Subsequent data taking and analysis



Collaboration with INFN (IDEA DC group)

- Collaboration focusing on the DC
  - Beam tests and data analysis
  - Reconstruction algorithm
  - Detector structure design
  - Prototyping and tests
  - Academic presentation and discussion





Summary

- Drift chamber is an important option for gaseous tracker of CEPC. Utilizing the dN/dx method can significantly enhance its PID performance. Simulation studies show that 3.2σ K/π separation at 20GeV/c can be achieved with 1.2m track length
- Design and construction of a DC prototype, readout electronics, and DAQ system have been completed to allow for the experimental validation of the dN/dx method
- Preliminary cosmic-ray tests confirms that the system is operating correctly.
- We will take cosmic ray data and study dN/dx performance and optimize reconstruction algorithm