Upstream Tracker Upgrade at LHCb

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On behalf of LHCb Collaboration

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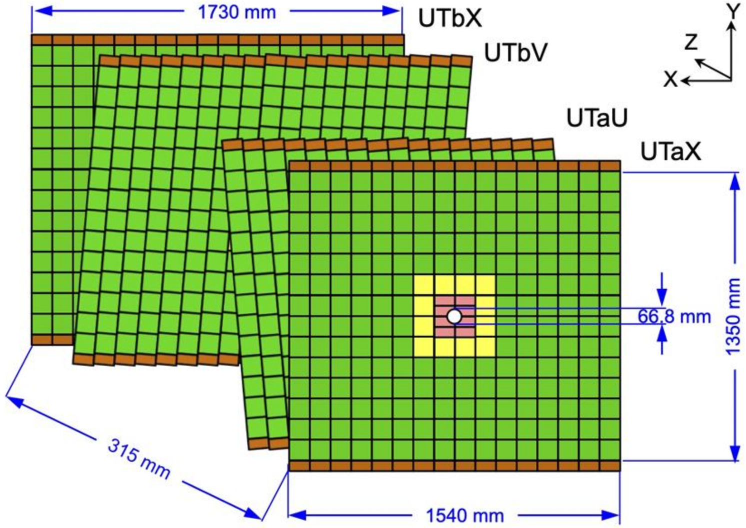
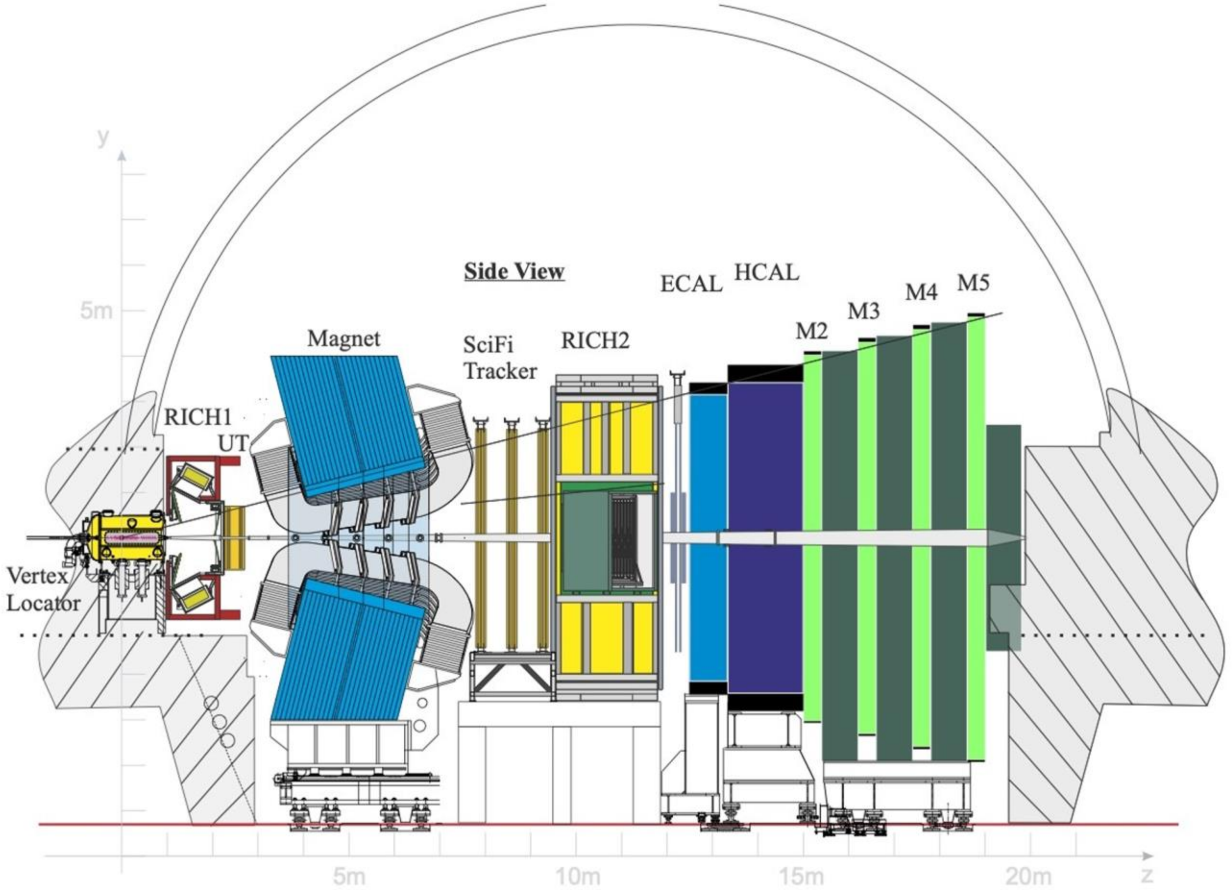
Outline

- LHCb and the future upgrades
- Sensor design and tests
- R&D of Module and stave
- Summary

LHCb : what it looks at present

- Removing the hardware trigger
- Increase luminosity by a factor of 5
  - 4×10^{32} cm^{-2} s^{-1} → 2×10^{33} cm^{-2} s^{-1}
- Upstream Tracker (UT):
  - 4 layers silicon strips detector

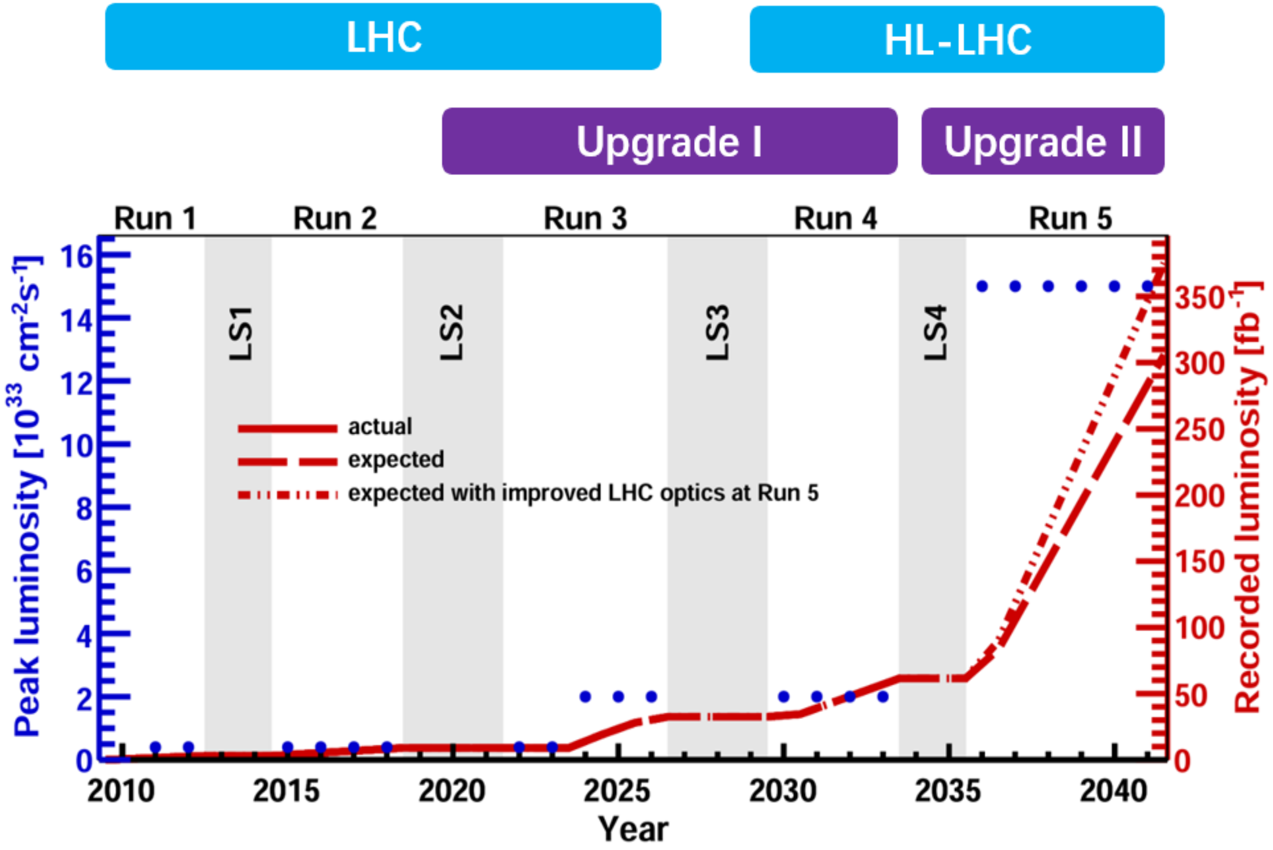




JINST 19 (2024) P05065

LHCb: Future Upgrades

- To fully explore flavour physics potential
- In LS3: enhancement work (Upgrade Ib)
  - For ECAL, RICH, DAQ,…
- Upgrade II operates at HL-LHC
  - Target luminosity $1.0\sim1.5 \times 10^{34}$ cm^{-2} s^{-1}
    - Baseline: 1.5×10^{34} cm^{-2} s^{-1}
    - Middle/low-descoping 1.0×10^{34} cm^{-2} s^{-1}
  - 300~350 fb^{-1}



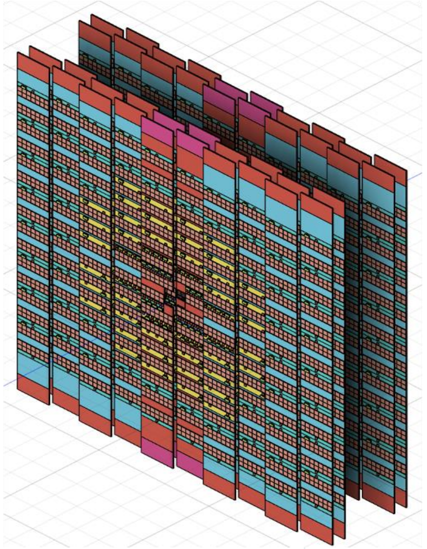
Run 3			LS3			Run 4				LS4		Run 5					
2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041
TDR phase			Construction phase							Installation		Exploitation					

CERN-LHCC-2024-010

LHCb Detector at Upgrade II

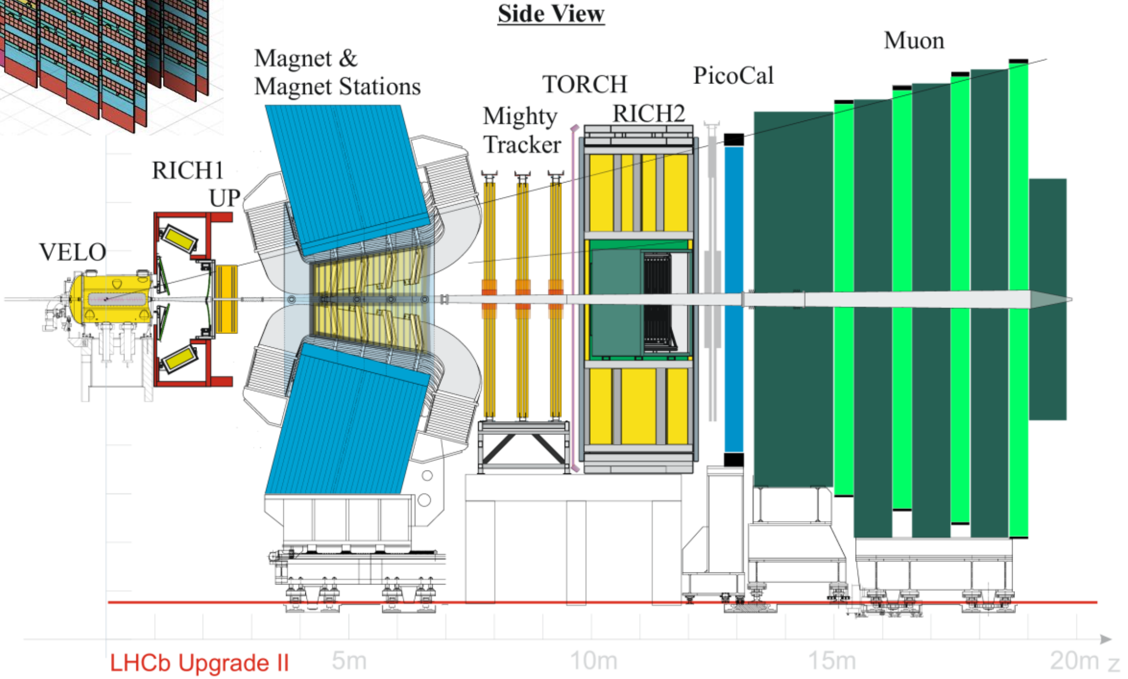
Challenges:

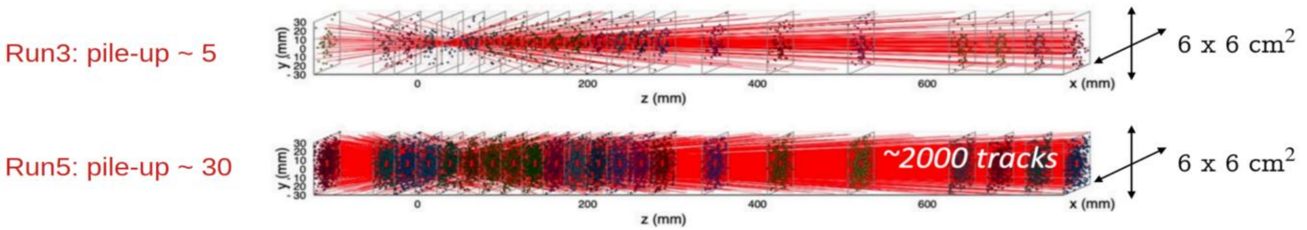
- Pile-up : ~1 → 5 (Upgrade I) → 40 (Upgrade II)
- High multiplicity, hence high occupancy
- Higher requirement on radiation hardness



Upstream Pixel Detector (UP)

- A MAPS based pixel detector proposed



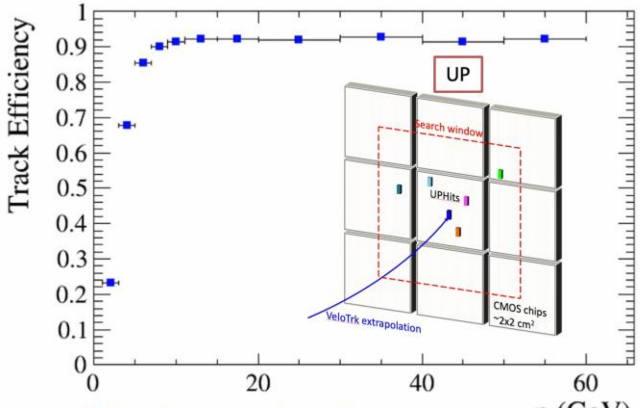


Vertex Locator (VELO)

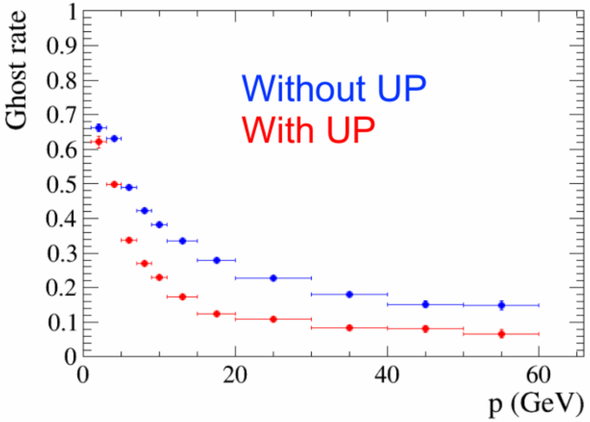
CERN-LHCC-2024-010

Why we need UP detector

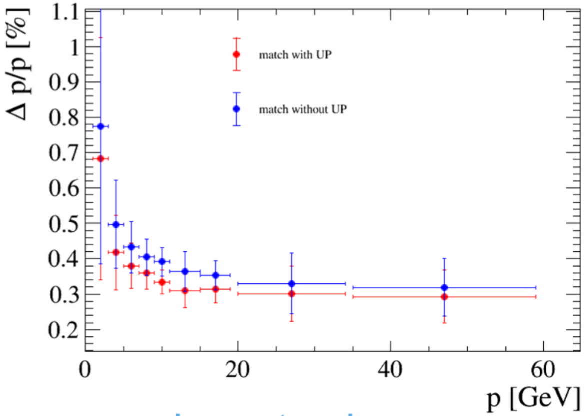
- Upstream and downstream tracks, UP is crucial in
  - Tracking efficiency
  - Reduce ghost rate
  - Momentum resolution
- Improvements for long tracks: with low ghost rate, better momentum resolution



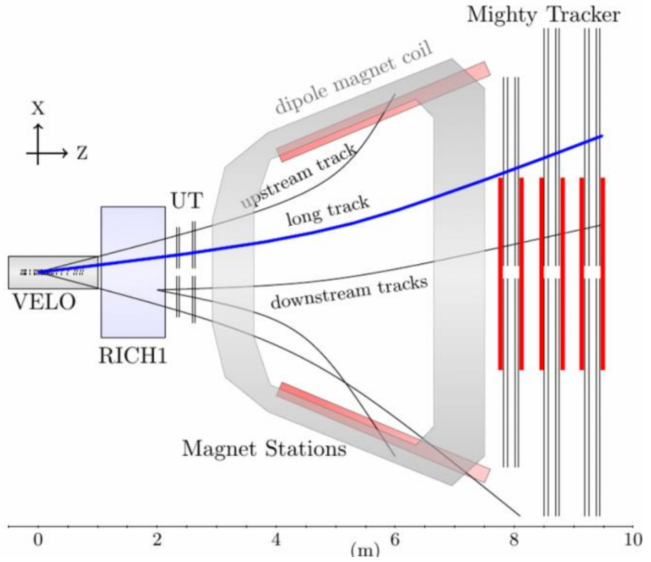
Upstream tracks – Tracking efficiency



Long tracks – ghost rate



Long tracks – momentum resolution



CMOS Sensor : Specifications

Fluka simulations performed, better insight

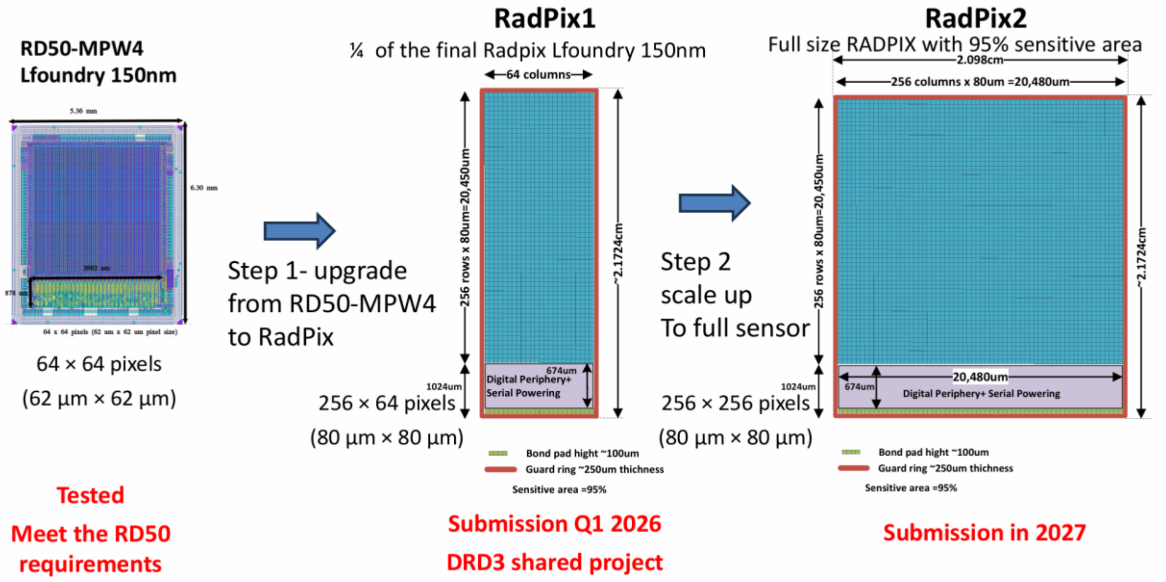
- NIEL: $1 \times 10^{15} N_{eq\ 1MeV}/cm^2$
- TID: 63 Mrad
- If we take the safety factor as 4:
  - NIEL: $4 \times 10^{15} N_{eq\ 1MeV}/cm^2$
  - TID: 250 Mrad

Chip candidates: Radpix, COFFEE, MightyPix, …

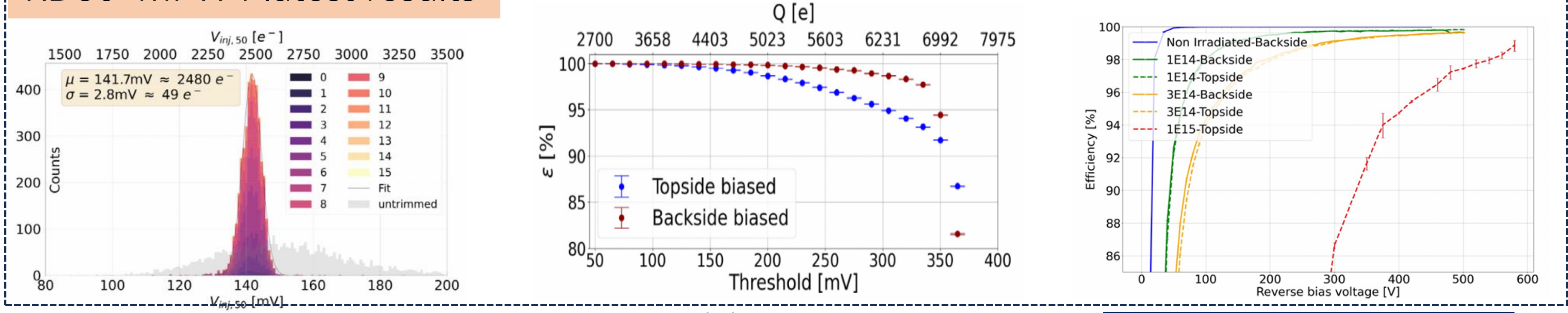
Parameter	Specification
Pixel size, square rectangular	$< 85 \times 85 \mu m^2$ $< 50 \times 200\ \mu m^2$
Substrate thickness	$< 200\ \mu m$
Max. particle rate hit rate	$74\ MHz/cm^2$ $150\ MHz/cm^2$
Max. length of data word	$32\ bits$
Transmission rate	$N \times 1.28\ Gbps$
Overall efficiency	$> 96\%$
In-time efficiency	$> 99\%\ within\ 25\ ns$
Noise rate(end of life)	$< 400\ kHz/cm^2$
Rad-hardness(NIEL) (TID)	$4 \times 10^{15} n_{eq}/cm^2$ $250\ MRad$
Power consumption	$< 200\ mW/cm^2$

CMOS Sensor : RadPix

- Development of ¼-size Radpix1 using Lfoundry 150 nm progressing well, target to have results ready by TDR 2026
- Optimization of Pixel Matrix for power (150 mW/cm^2) and speed (99% in-time efficiency) requirements with the different pixel flavors
- Ongoing:
  - Design of readout periphery for compatibility with LHCb protocols, and power budget
  - Analog blocks (LVDS transmitter & receiver, power-on-reset, voltage regulator)
  - Design verification and FPGA emulation



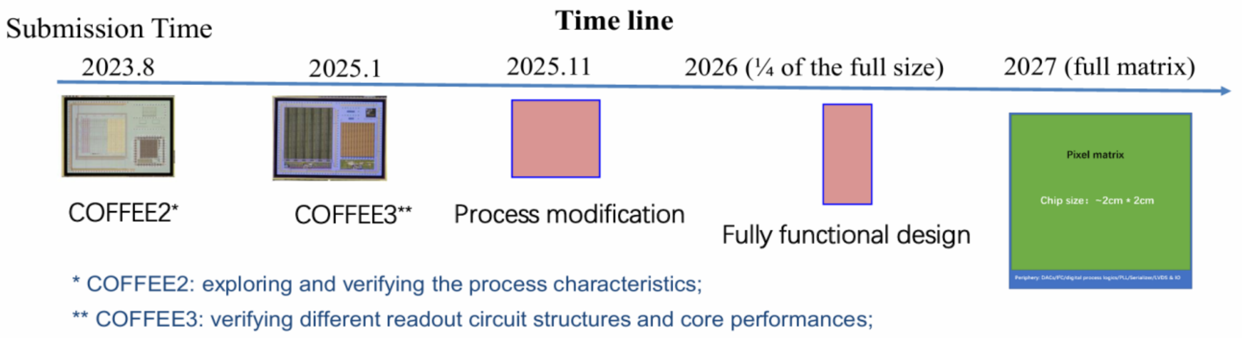
RD50-MPW4 latest results



NIMA 2024,169839

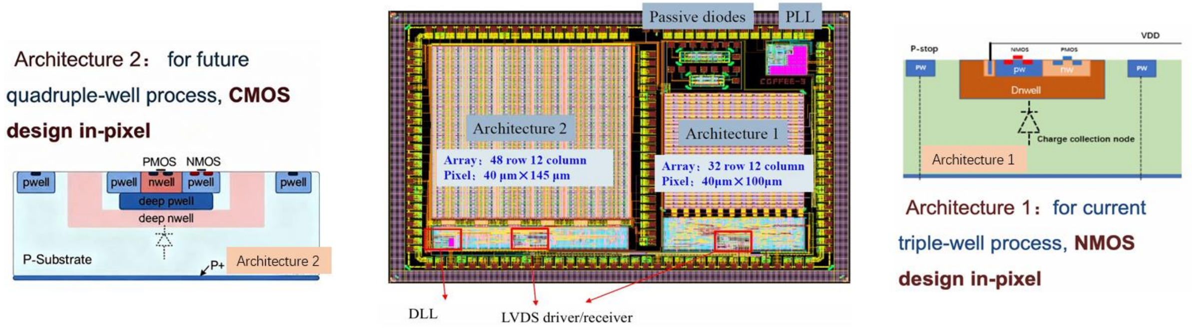
CMOS Sensor : COFFEE

- COFFEE1: validate the low leakage process
- COFFEE2: exploring and verifying the process characteristics
- COFFEE3: verifying different readout circuit structure and core performances
- In future : fully functional small size → fully functional full size



COFFEE3:

- a small prototype to implement two complete readout pixel array scalable for larger chip;
- chip submitted in January and received in end May
- A lot of encouraging results have been obtained

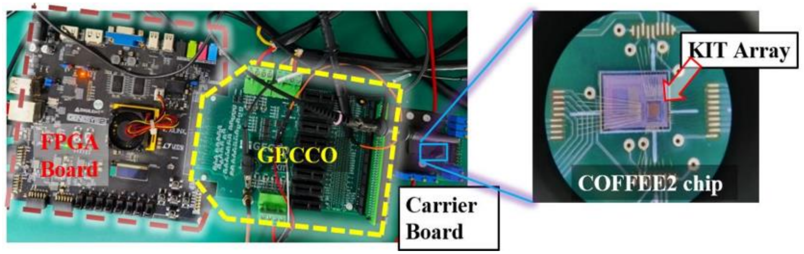


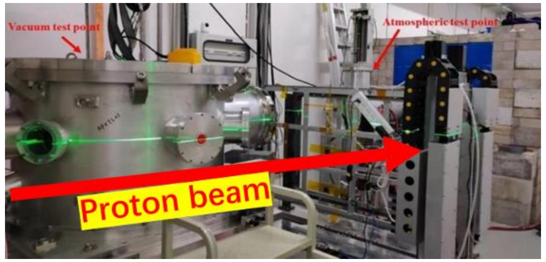
COFFEE3 design

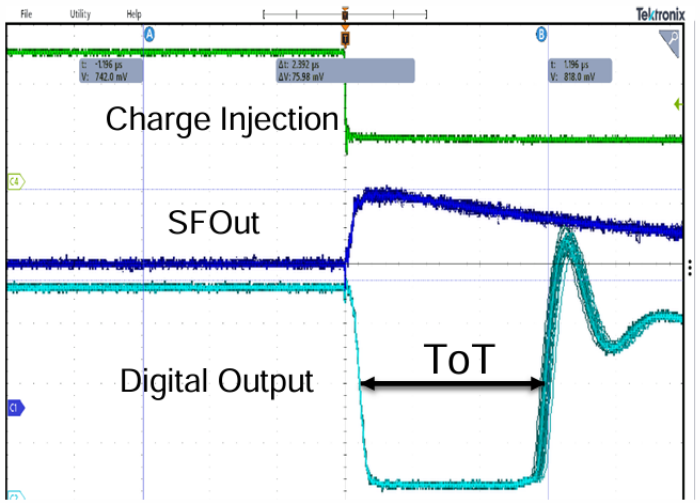
COFFEE2: Irradiation Study

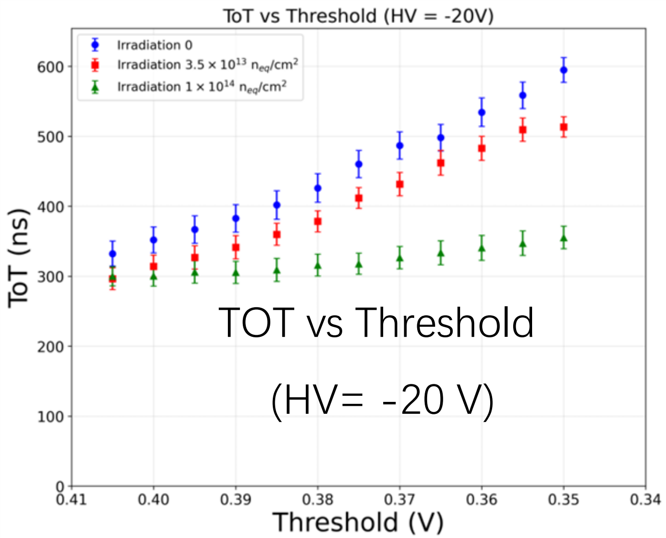
- Proton irradiations at CSNS (China Spallation Neutron Source)
- Under an irradiation fluence of $1 \times 10^{14} n_{eq}/\mathrm{cm}^{-2}$,

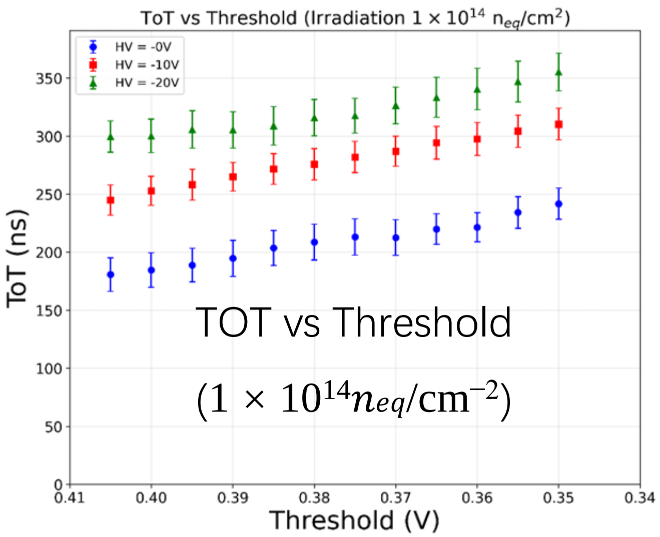
  the chip can still maintain normal operation, proving strong radiation tolerance





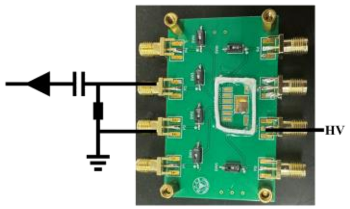


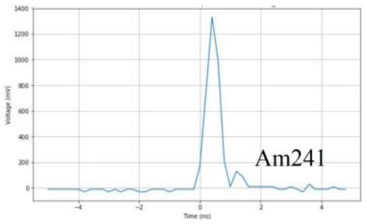


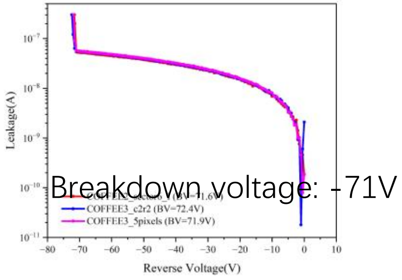


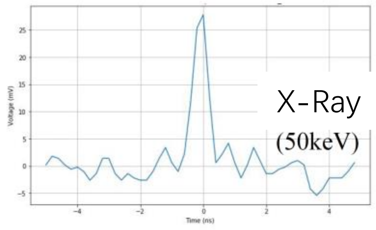
COFFEE3 Tests: Peripheral Modules and PDA

Passive diode array(PDA):



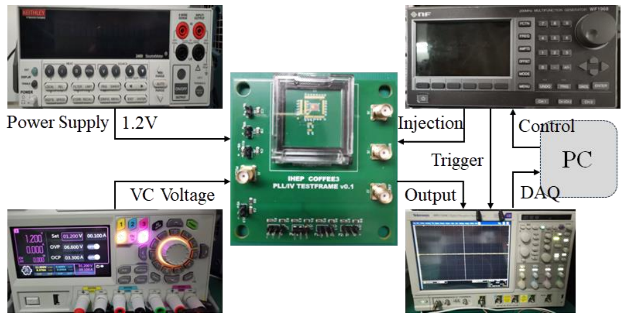


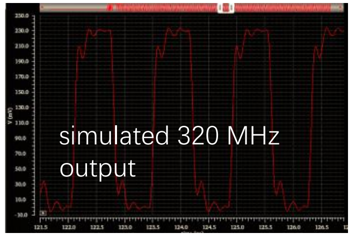




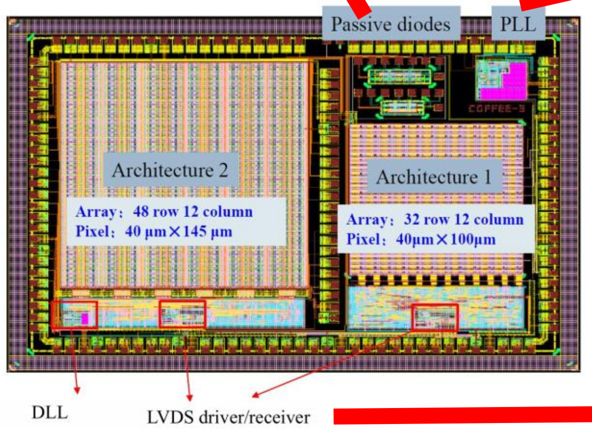
Responsive to α- and X-rays

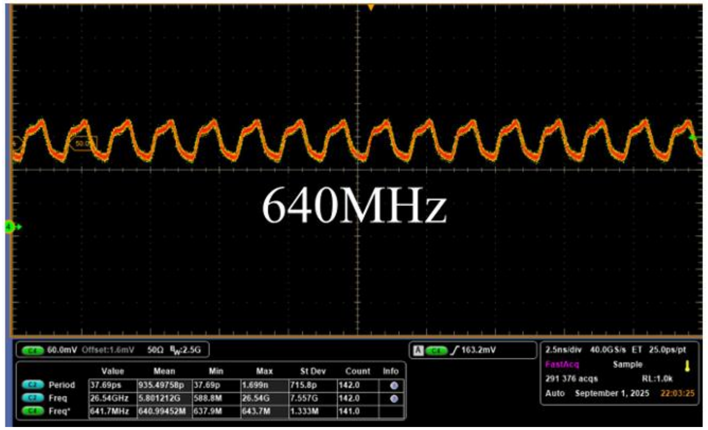
PLL:





- Breakdown voltage ~70 V
  Leakage ~ few tens pA
- LVDS transceiver supporting 1.28 Gbps data transmission
- Delay Locked Loop(DLL) delivers clock phase decay as expected

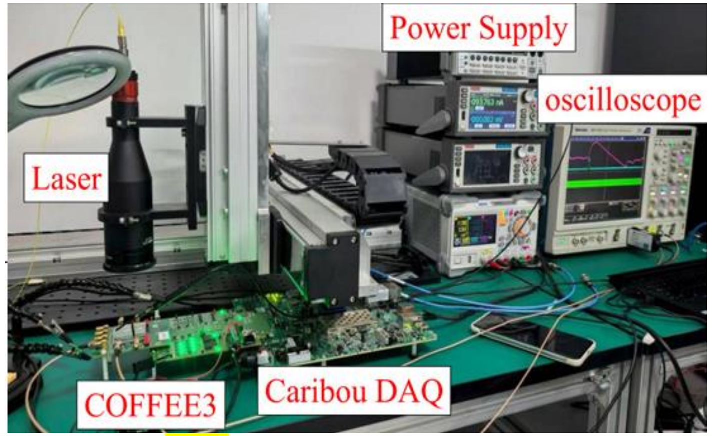




LVDS & DLL

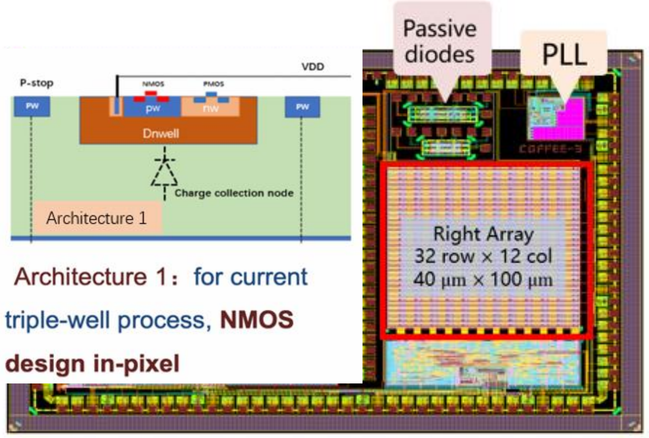
COFFEE3 Tests: Architecture1

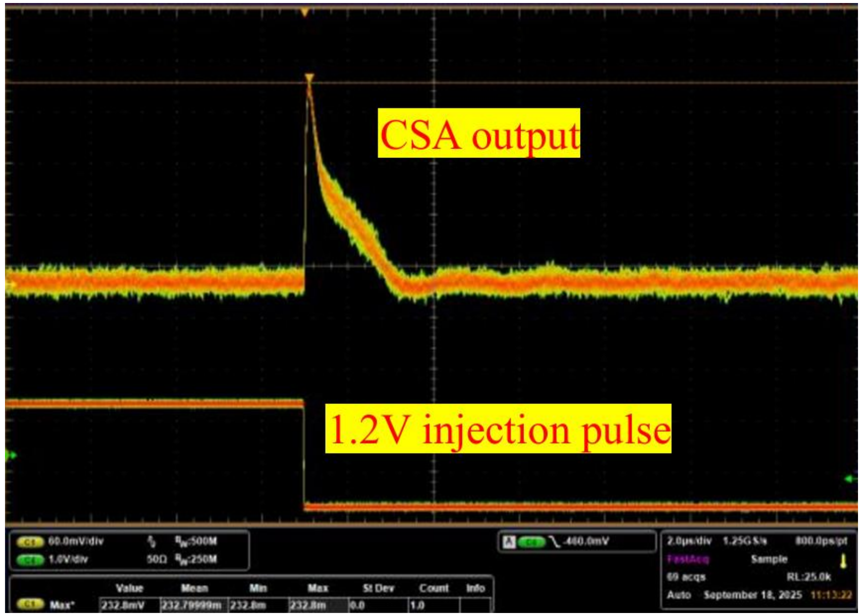
- CSA(charge sensitive amplifier) working as expected with charge injection
- End of column readout function validated



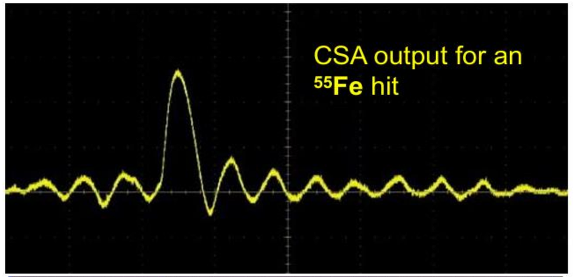
NMOS-only in-pixel digital design:

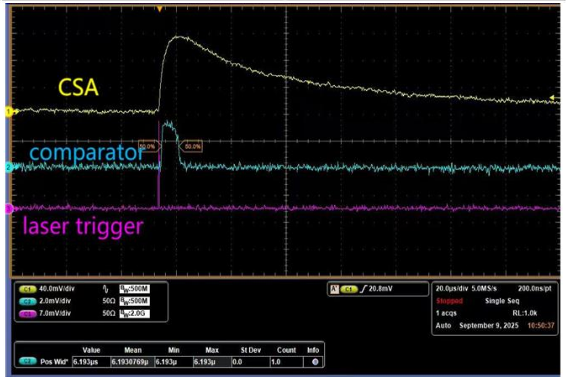
lower power consumption in pixel

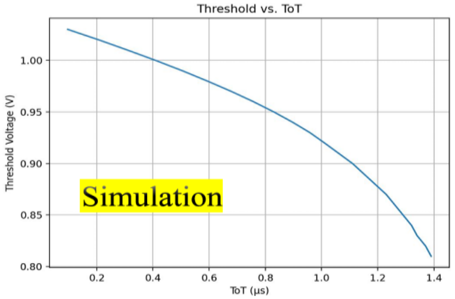


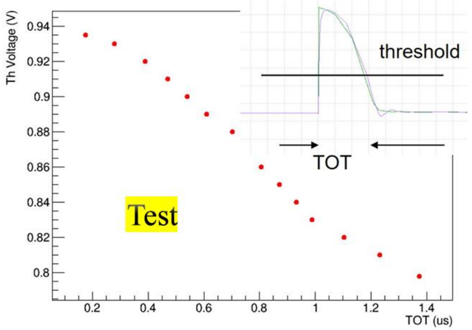


COFFEE3 Tests:Architecture2



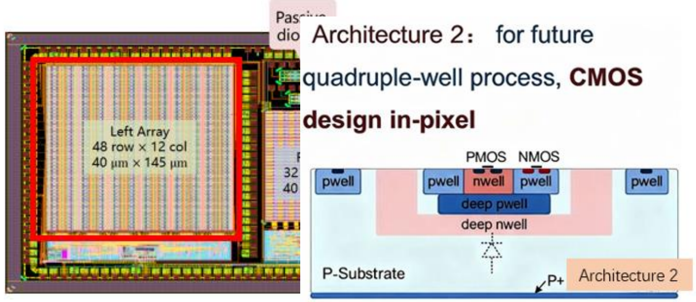




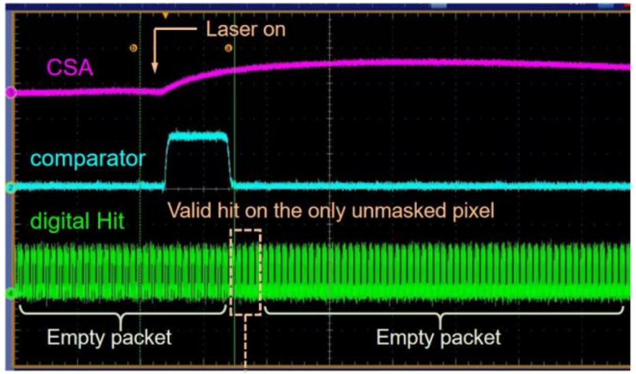


CSA+Comparator

- In-pixel CSA and comparator working as design
  - With laser irradiation, clear CSA and comparator output
  - Typical TOT of laser signal 1-2 μs, agree with simulation
- Pixel also response to Fe55 signal (X-Ray)



- CMOS digital circuits within pixels.
- Fully exploiting the advantages of the 55nm process. Integrate TDC within pixels.



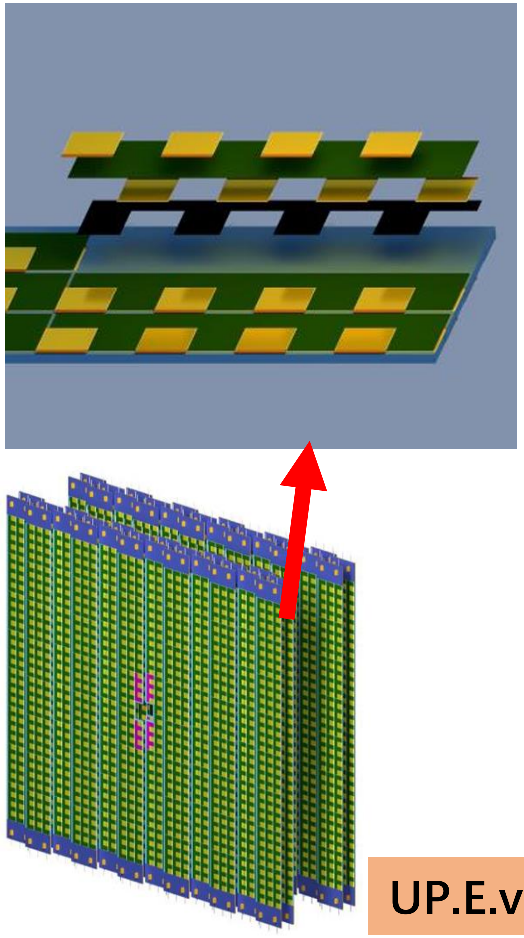
Full readout chain

Full readout chain verified with laser test:

Sensor →in-pixel CSA+comparator→end of column readout circuit

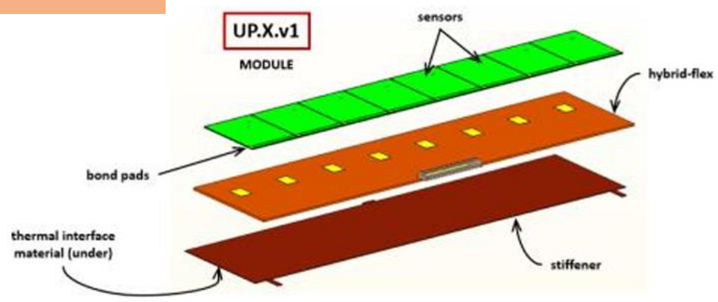
Module and Stave : Design

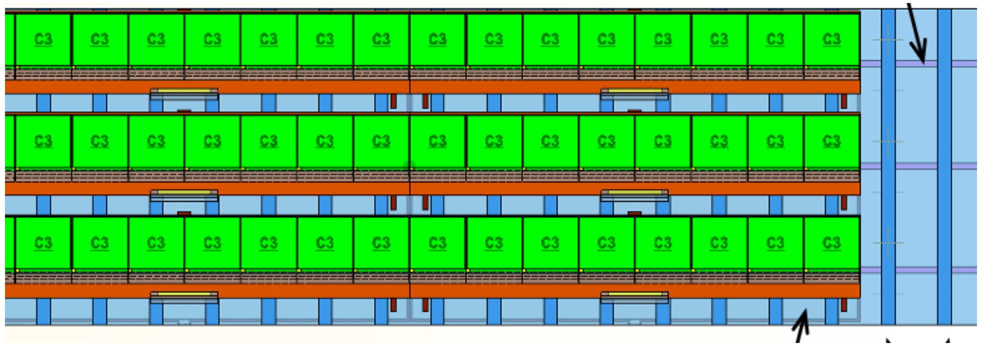
Three designs under consideration,
will converge on a design following an evaluation process based on requirements.



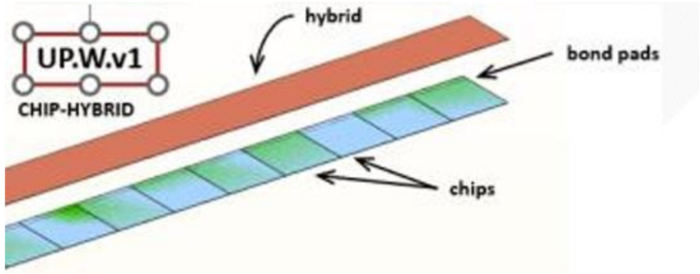
UP.E.v2

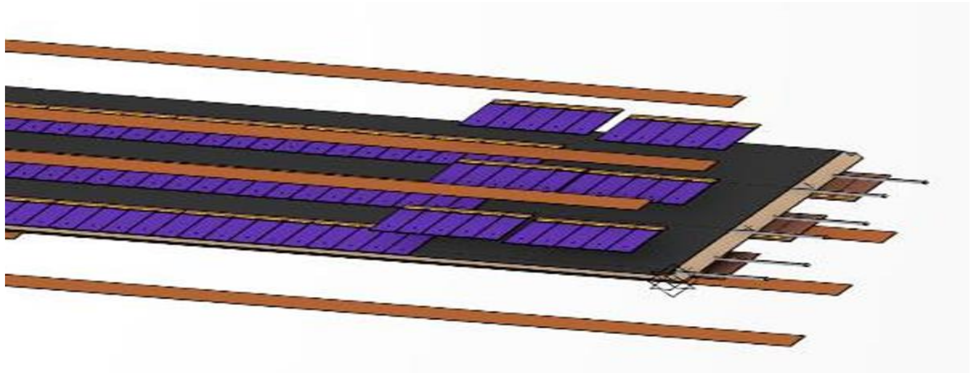
UP.X.v1



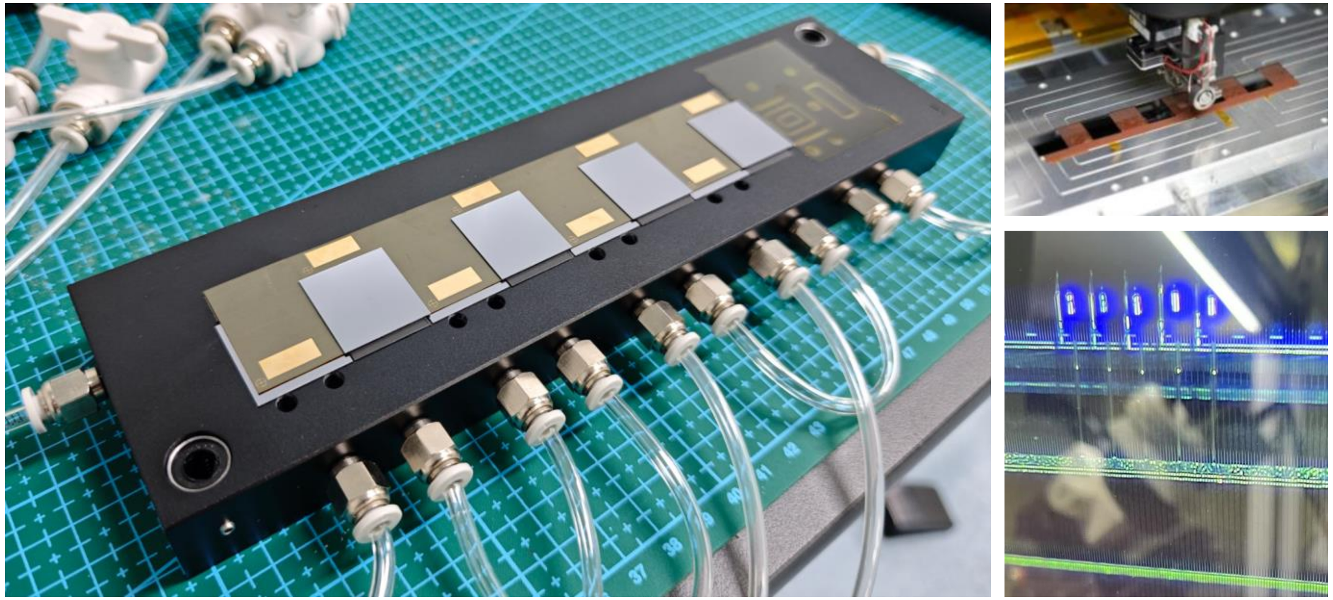


UP.W.v1

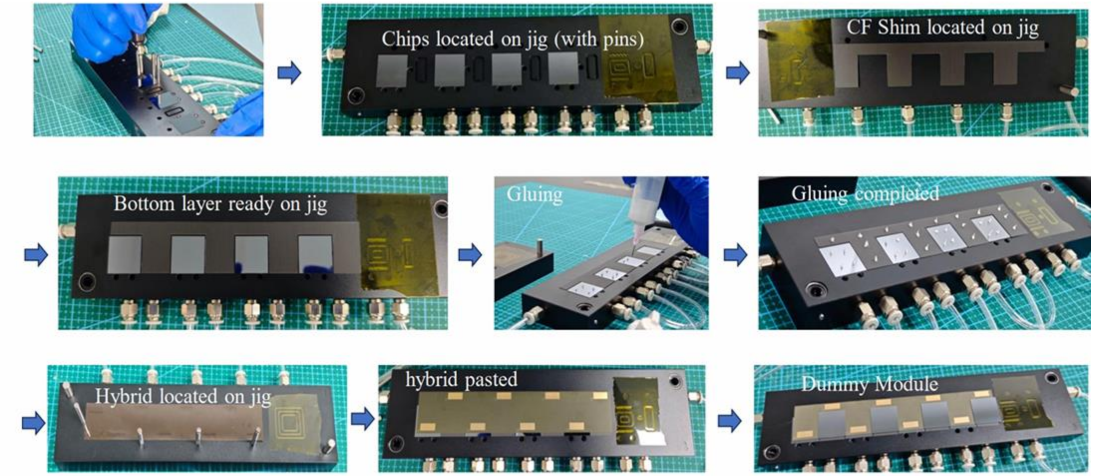




Module and Stave : Prototyping



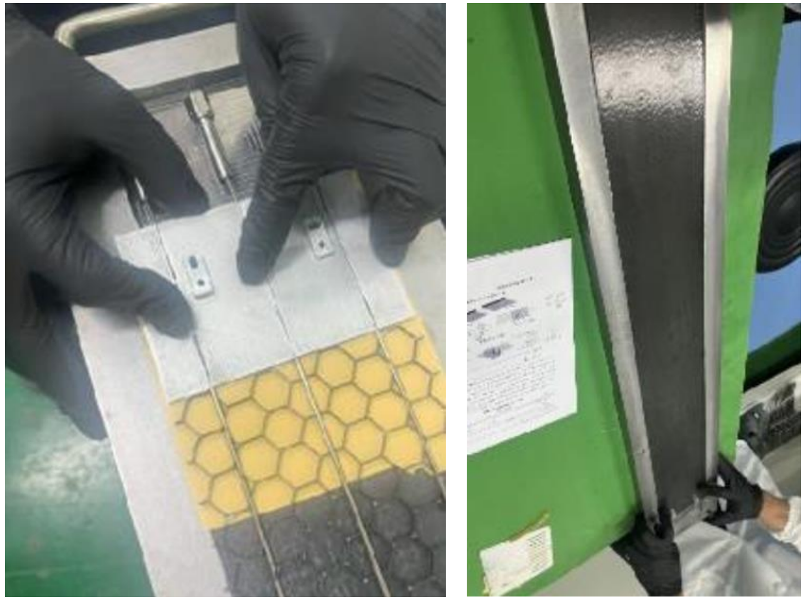
Module prototype



UP.E.v2 design:

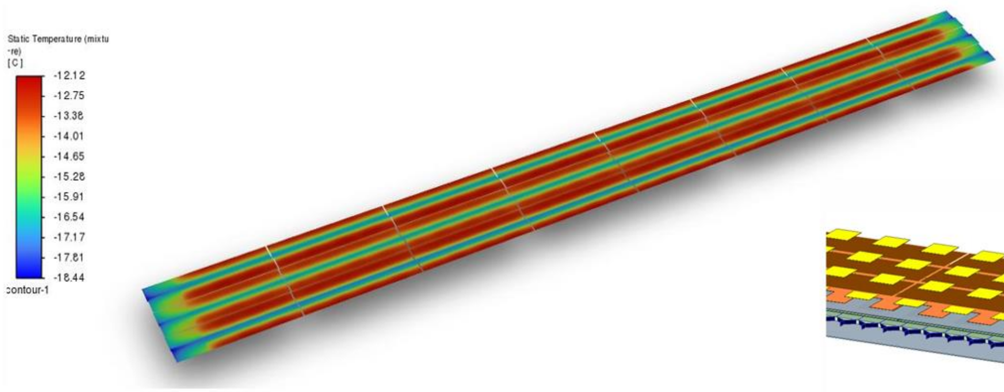
- Prototyping on Module and Bare stave are ongoing
- For the dummy module, wire bonding test also performed

Prototyping of the other designs also carried out, ongoing.

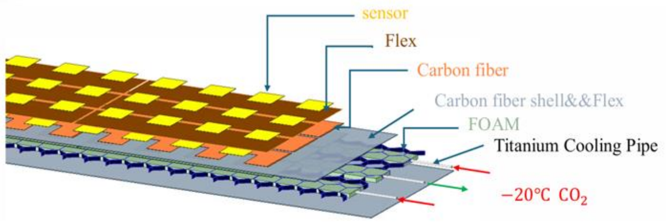


stave prototype

Module and Stave : Thermal Simulations



- Chips thermal power: 200 mW/cm^2
- flex power: 40 mW/cm^2
- UP box temp: 26.8 ℃
- CO_2 input temp: -20℃,
- Pressure: 2 Mpa



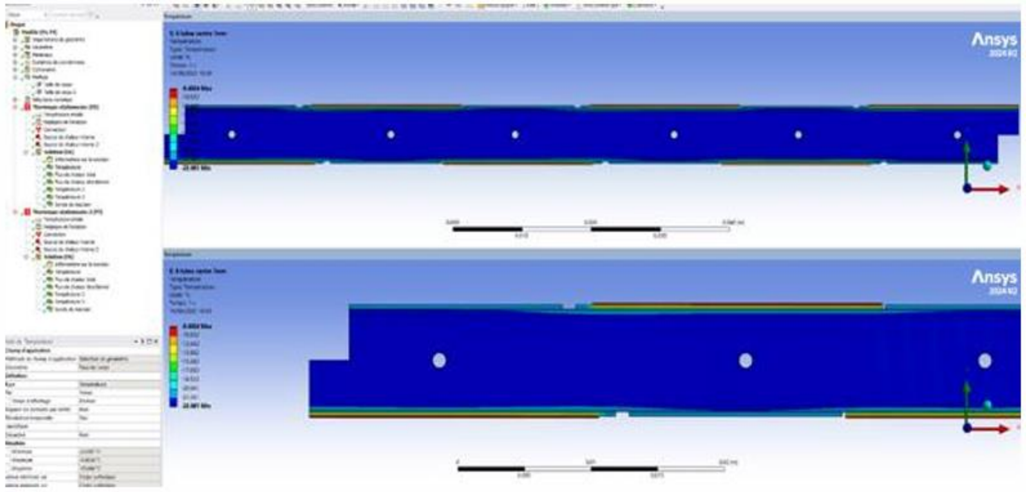
Thermal resistances of flexes dominate

- Controls ΔT for the full stave and module
- Aside: if use honeycomb *only* for core, ΔT increases significantly

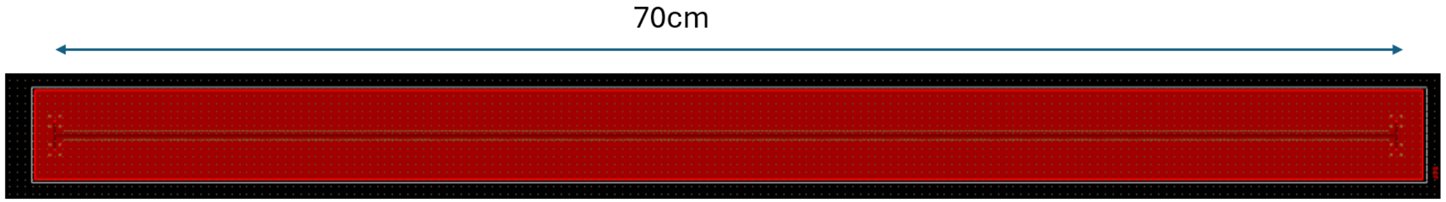
$\Delta T[K] = R_{TH}\dot{Q}[W]$			
	for MODULE	4.292	℃
	for FLEX	4.020	℃
	for BARE STAVE	1.695	℃
	for INTEGRATED STAVE	**10.007**	℃

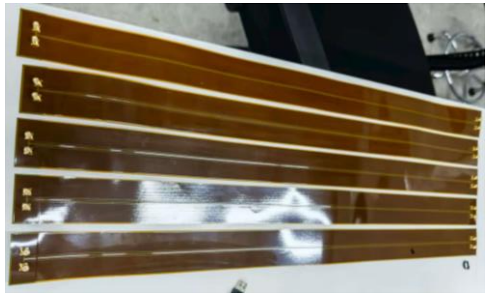
← ΔT

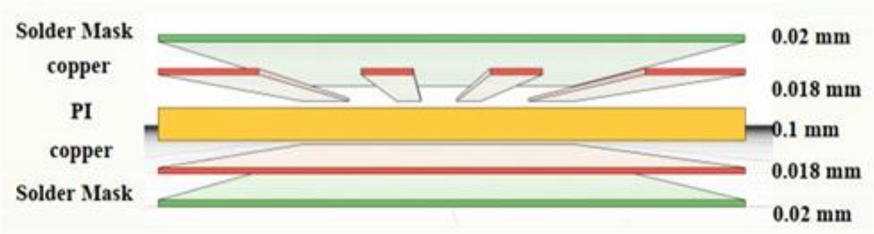
- Thermal studies w.r.t different detector designs kicked-off
- Input for evaluating the detector designs

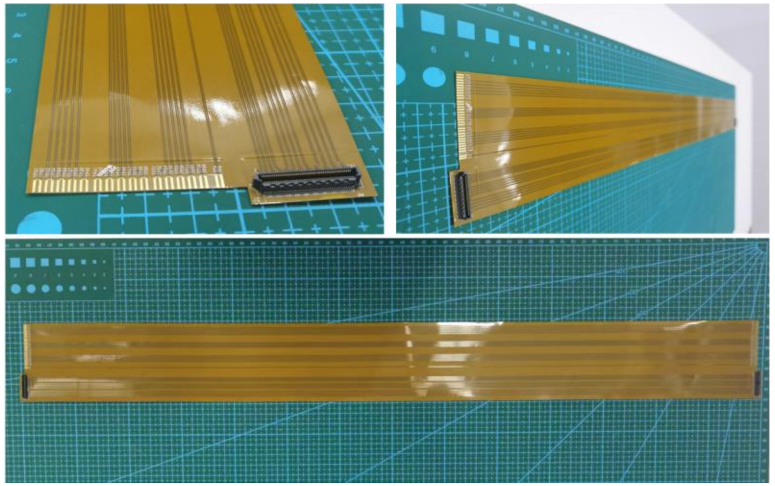


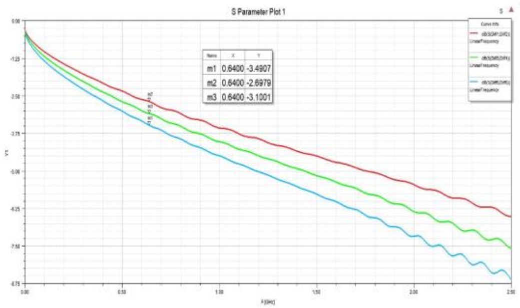
Module and Stave: Readout Flex

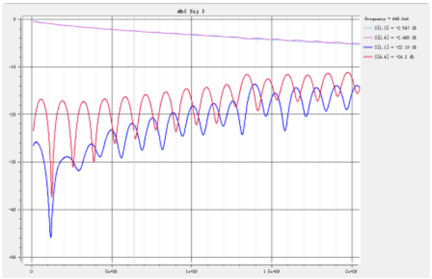


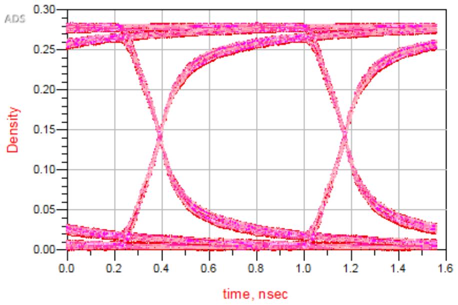












Item	value
Test time	~45 min
N bits	3.4×10^{12}
NUM. Error bits	0
Bit Error Rate (95%CL)	$<8.8\times 10^{-13}$

- Single differential pair with impedance 100 Ω
- Balance between signal integrity and material budget
- Test the maximum length of differential pairs

Summary

- LHCb detector faces challenges for the Upgrade II phase with high-luminosity.
- Upstream Tracker will be upgraded to Upstream Pixel detector (UP)
- UP detector R&D studies progressing well
- Good results on chip development, module/stave design and prototyping, software studies.

Thank you for your attention!