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Status of the STCF MAPS-based inner tracker

Hao Han
on Behalf of the STCF ITKM Working Group

University of Science and Technology of China
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Outline

- MAPS-based Inner Tracker for STCF
- R&D of MAPS
  - Prototype chip design
  - Test of MAPS
- Stave & Mechanical Design
- Conclusions

Super Tau-Charm Facility

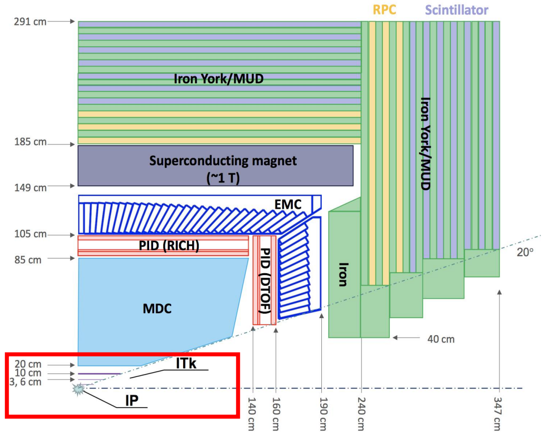
- **Super Tau-Charm Facility , STCF**
  - ➢ next generation e^+e^- collider in China
  - ➢ E_{cm}=2~7 GeV, Peaking luminosity >0.5×10^{35} $cm^{-2}s^{-1}$
  - ➢ Exhibits potential for further enhancement of peak luminosity and achievement of beam polarization
  - ➢ Research target
    - ✓ Detailed study of Tau-Charm physics
    - ✓ More precise tests of the Standard Model
    - ✓ Search for new physical laws

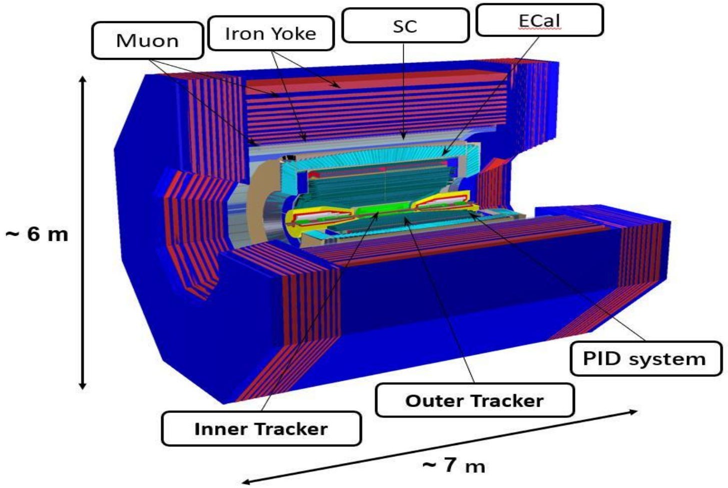
Extremely low material budget

High event rate capability

Good radiation tolerance

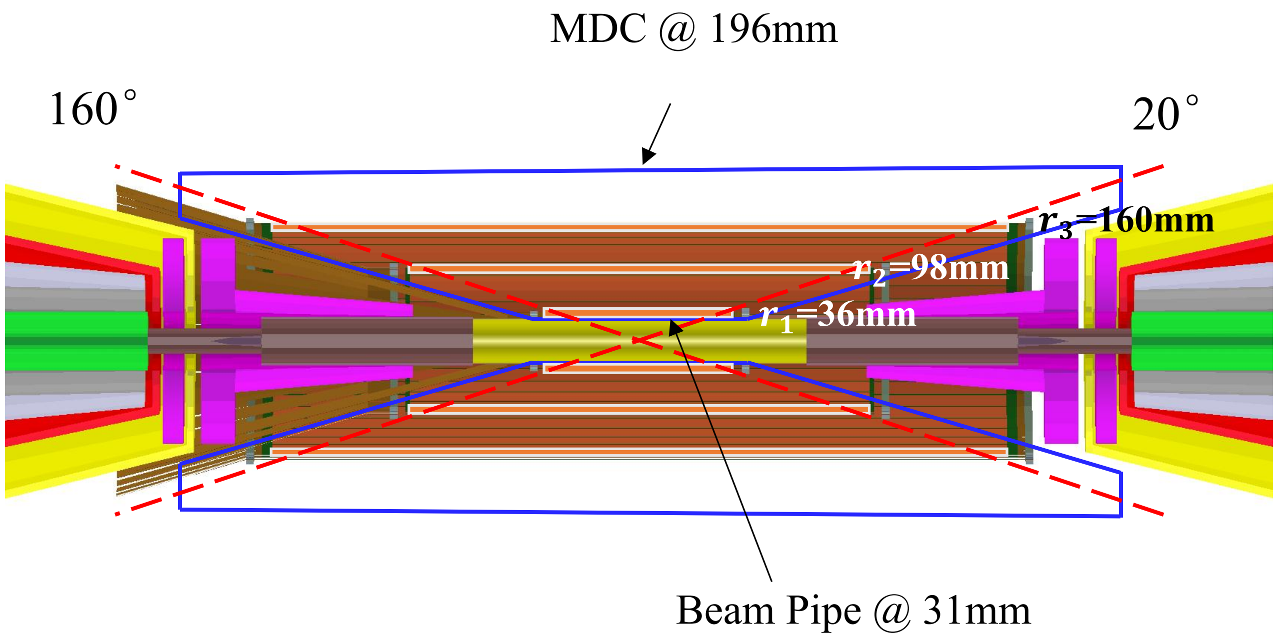
Inner Tracker, ITK

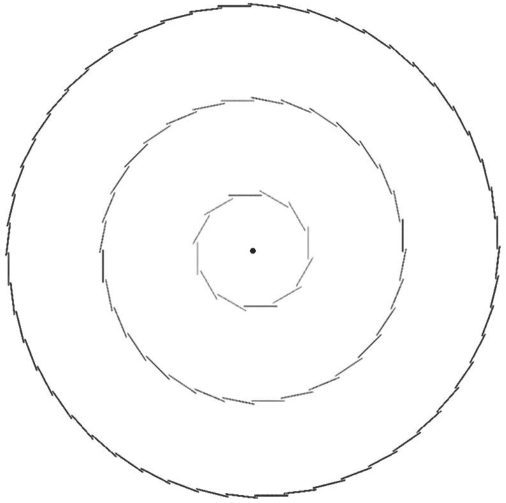




STCF detector

Conceptual design of ITKM





	Min radius/mm	stave no.	chip no.	Area/cm²
ITKM1	36	12	12	583.9
ITKM2	98	32	30	3892.7
ITKM3	160	52	48	10120.9

- A three layer design at present
- Single chip size ~**2cm×2cm**
- Covering polar angle **20° -160°**
- Total area: 15000cm²
- 3600 chips

The updated design will be based on a four-layer structure

MAPS-based Inner Tracker for STCF

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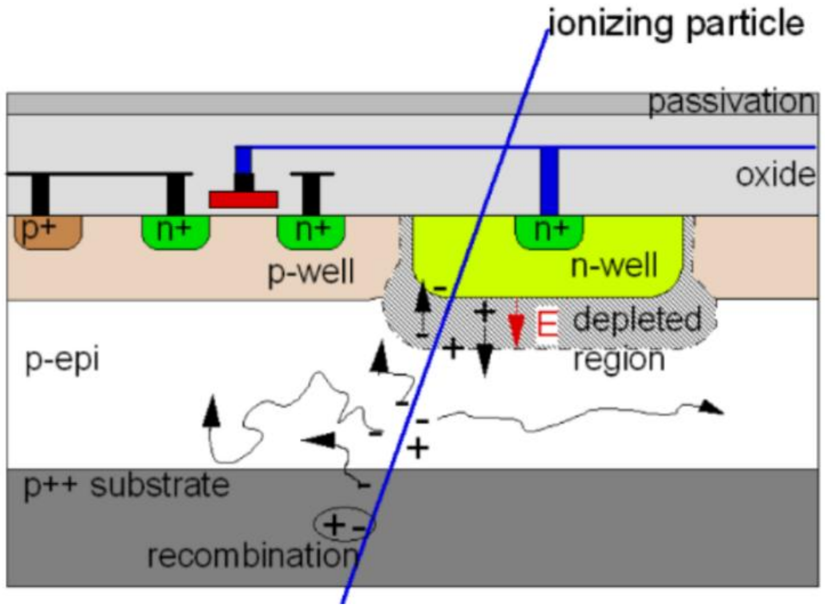
- **Requirements for Inner Tracker**
  - ~0.3% X_0 per layer
  - $\sigma_{r\varphi} < 100\ \mu m$
  - Tracking efficiency >90% @100MeV/c
  - Hit rate 1 MHz/cm^2, TID 1 Mrad/y, NIEL $1\times10^{11} n_{eq}/cm^2/y$



- **Requirements for MAPS**
  - Power consumption <50 mW/cm^2
  - Moderate position resolution ~30 μm
  - Good timing of ~20 ns
  - Detection of energy deposition(ToT)

It is highly challenging for the chip to meet all the above specifications.

Monolithic **A**ctive **P**ixel **S**ensor
- ✓ Mature CMOS technology
- ✓ Highly integrated
- ✓ Small pixel pitch
- ✓ Low material budget
- ✓ High SNR
- ✓ …

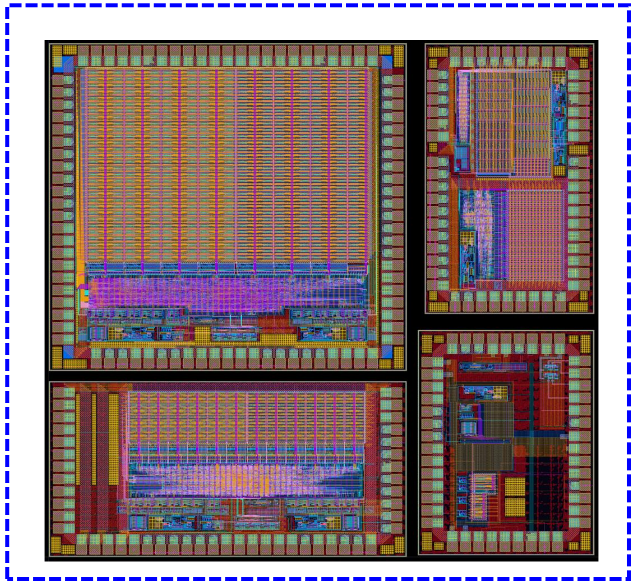
Chip design overview

- Prototype MAPS design under different technologies

180nm process

- Low res substrate + high res (>1 kΩ·cm) EPI
- Mature process in HEP
- Baseline techno

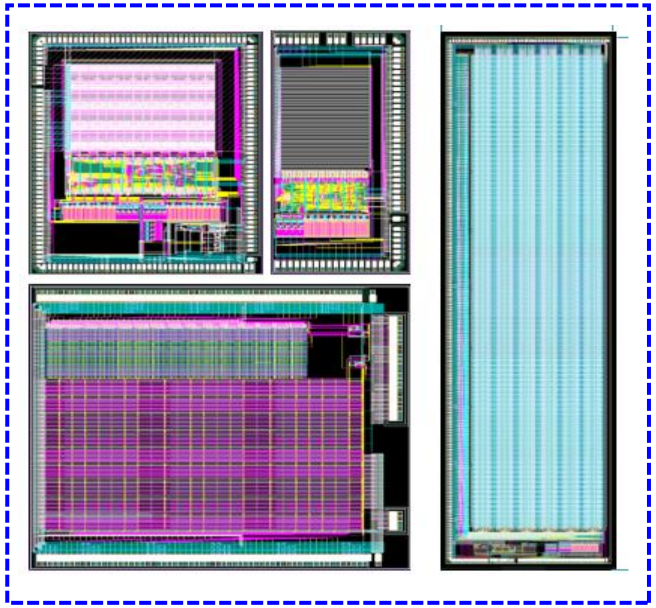
CharTPix_180



130nm process

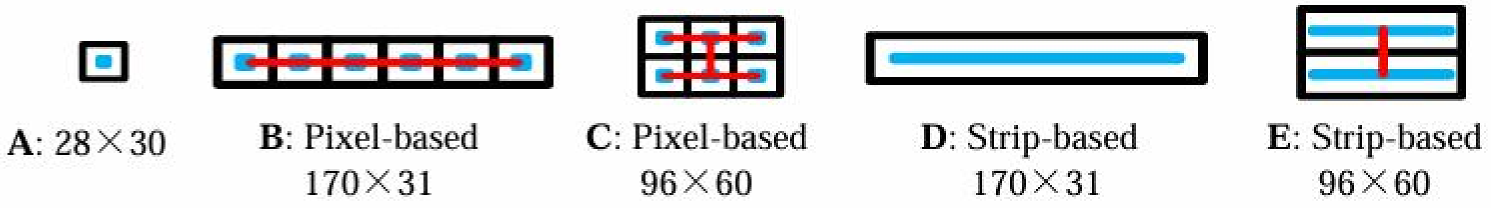
- High res substrate, no EPI
- Domestic techno

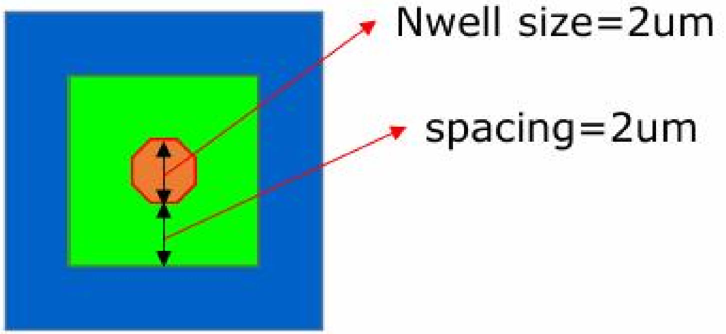
CharTPix_130



CharTPix_180 Overview

- Compare different pixel geometry & connection





Metal line connected
✓ small input capacitance

Nwell (active) connected
✓ faster charge collection

- Four flavors of prototype chips:
  - **Chip 1**: Small pixel, Low power consumption
  - **Chip 2 & 3**: Enlarged pixel size, timing with TOA, TOT
  - **Chip 4**: Analog readout for sensor performance comparison

	Chip1	Chip2		Chip3		Chip4
Pixel size (μm×μm)	28.1×30.1	96.4×59.6		170.0×31.0		Mixed
Sensor	A	E	C	D	B	A+B+C+D+E
Pixel array	16×30	8×12	8×12	60×8	60×7	Mixed
Readout	Column-drain	Column-drain		Column-drain		Analog readout
ToA & ToT	×	✓		✓		×
Chip area (mm^2)	1.5×1.4	2.5×1.6		2.8×3.1		1.2×1.4

CharTPix_180 Full-functional chip

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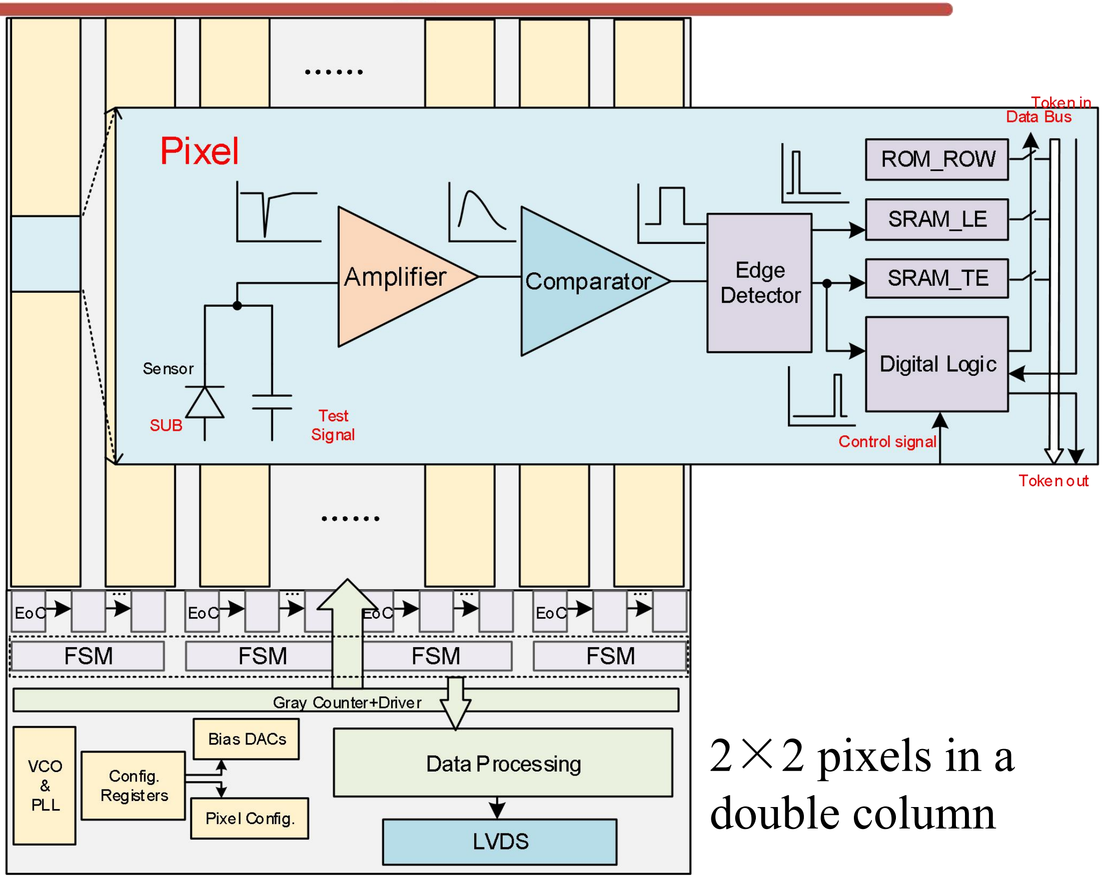
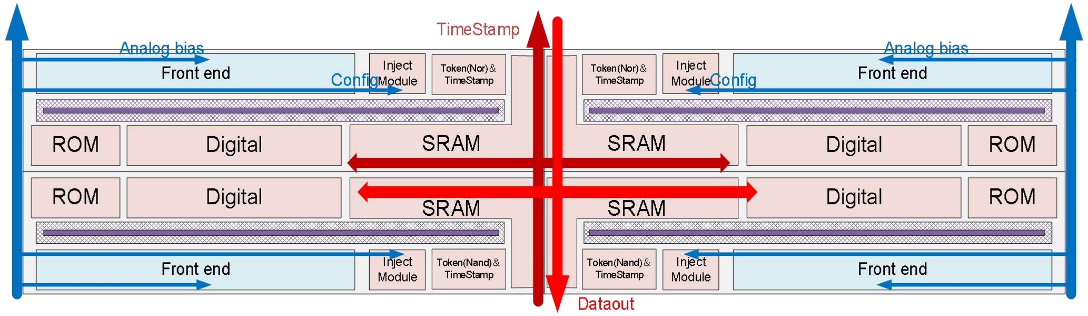
Chip 2 & 3

- Column-drain readout
- 20 MHz clock distributed to the pixel array
- LE & TE timestamp recorded (8+8 bits)
- Power consumption estimation for 2×2 cm^2 chip
  - ➢ Metal line connected: 46.2 mW/cm^2
  - ➢ Nwell connected: 55.7 mW/cm^2
- >99% readout efficiency @8.72 MHz/cm^2
- Timing ability σ_{ele}~22.0 ns@Q_{inj}=600 e^-



2×2 pixels in a double column



CharTPix_130 Overview

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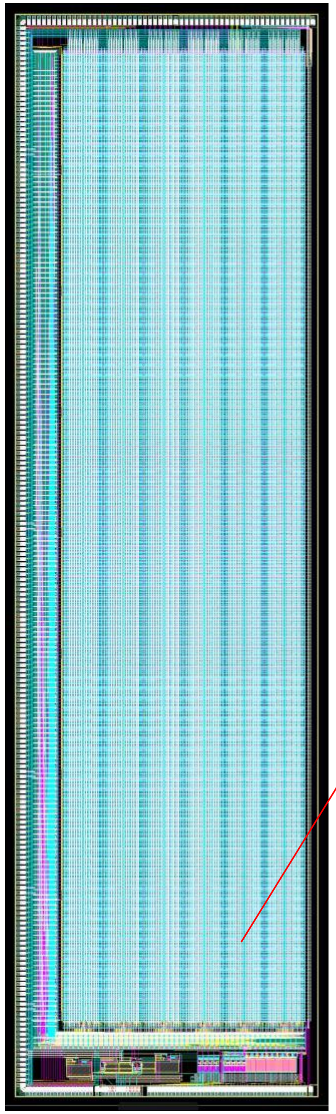
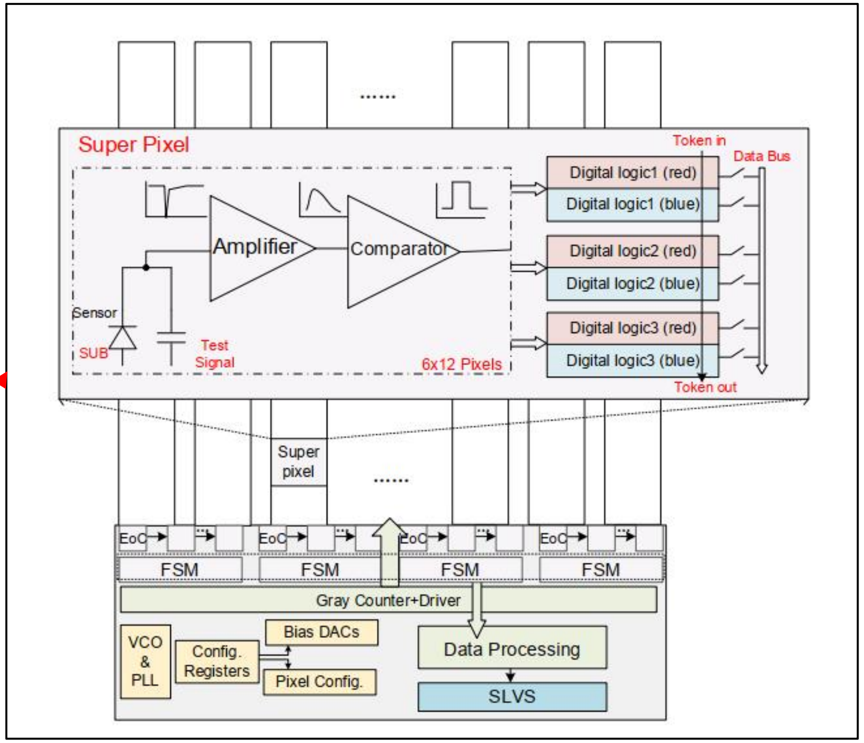
A: 30×28 B: Strip-based(170×31) C: Pixel-based (170×31) D: 33×33

	Chip1		Chip2	Chip3	Chip4
Pixel size (µm×µm)	170×30		30×28	Mixed	33.2×33.2
Sensor	B	C	A	A+B+C	D
Pixel array	60×8	60×8	60×48	Mixed	576×144
Readout	Column-drain		Column-drain	Analog	Column-drain (Super pixel based)
ToA & ToT	✓		×	×	✓
Chip area (mm²)	5.25×4.4		4.3×2.2	4.2×4.9	21.0×6.0



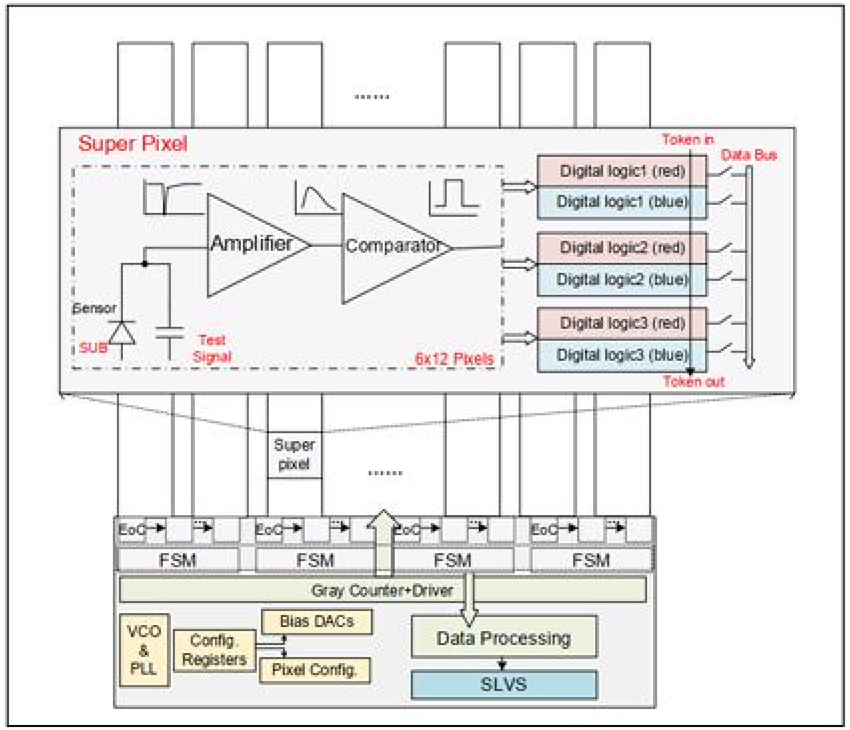
Chip4

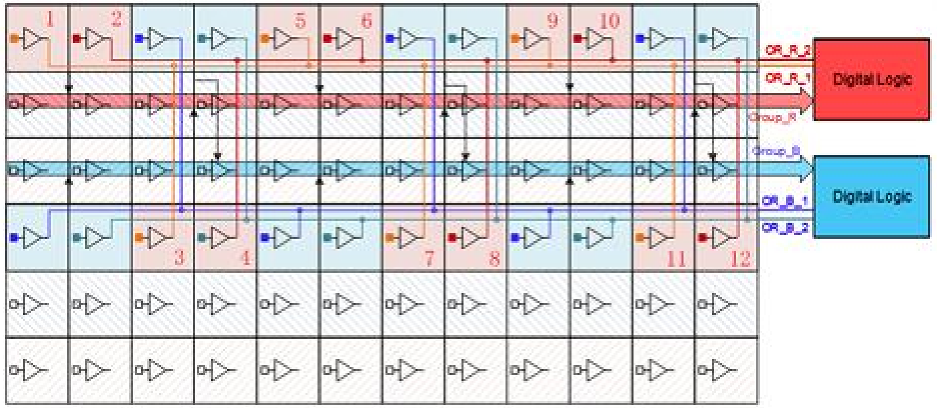
- **Novel super pixel design**
- 33×33 µm² pixel
- 500 MHz VCO for fine LE timing
- Expected power consumption ~40mW/cm²



CharTPix_130 read out

- Pixel Core: Minimal repeatable layout array
  - ➢ Core size: 6×12 pixel
  - ➢ No pixel information is lost when the cluster area is smaller than 3×4 pixels





- Pixel Pitch: 33 μm×33 μm
- Simulated Threshold: ~ 150 e^-
- Fine Time Bin: 500 MHz VCO

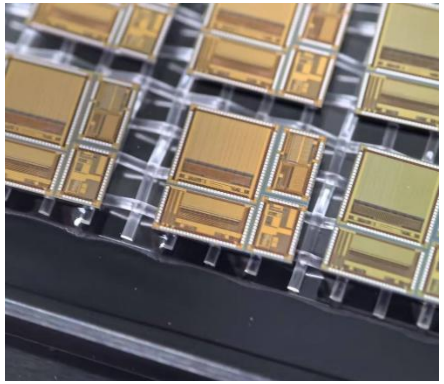
(to achieve fine time interpolation)

- Simulated Power Consumption: ~ 40 mW/cm²

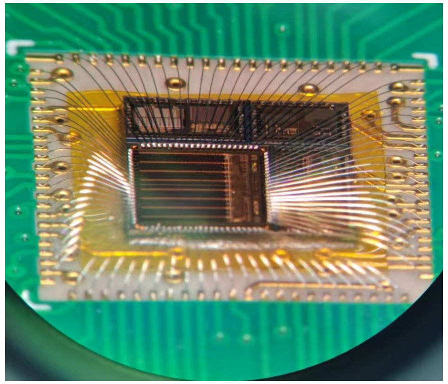
Test Overview

- CharTPix_180
  - Electronics test:
    - ✓ Basic electrical performance testing
  - Laser test:
    - ✓ Preliminary detection efficiency and position resolution testing
- CharTPix_130
  - Fe55 test and laser test of 130nm 3T chip
  - Electronics test
  - Fe55 test:
    - ✓ Characterize charge collection performance and calibrate the injection capacitance
  - Power consumption test
- Beam test: Evaluation of detection efficiency and position resolution
  - CharTPix_180
  - CharTPix_130

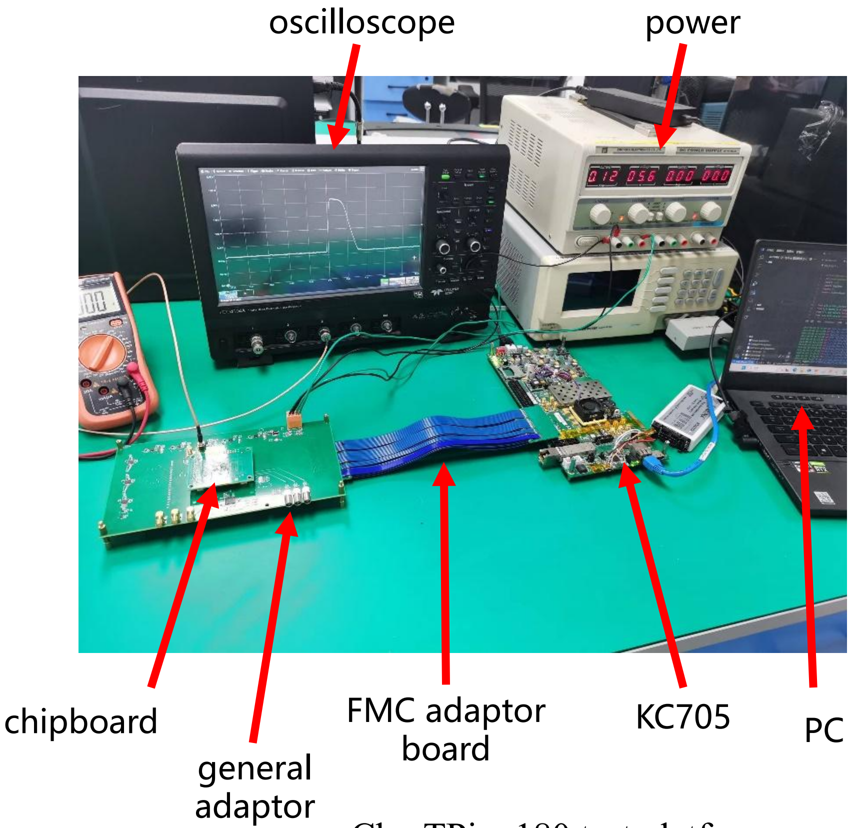
CharTPix_180 test platform



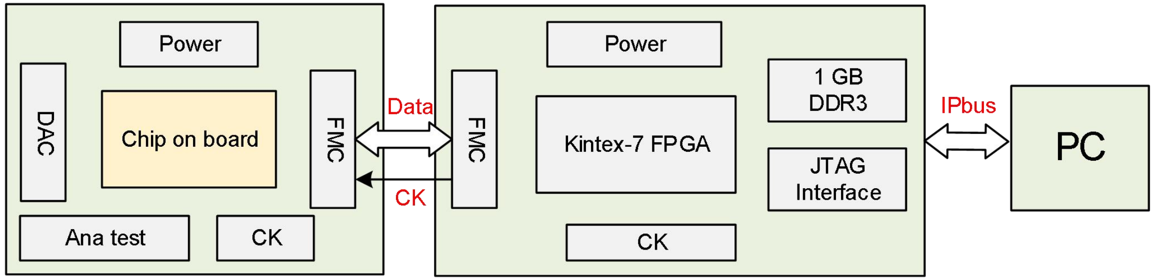
CharTPix_180



Wire bonding



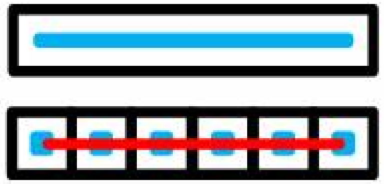
CharTPix_180 test platform



Test system block diagram

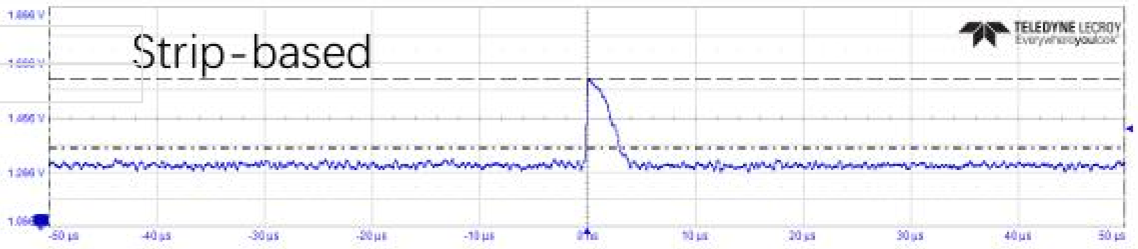
Electronics Test

- Test of CharTPix_180_chip3, which includes two types of sensors
  - ➢ Strip-based 170 μm × 31 μm
  - ➢ Pixel-based 170 μm × 31 μm

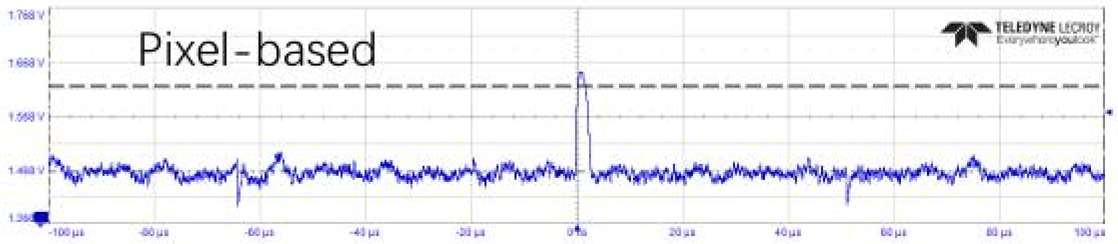


- Normal readout operation under -6 V substrate bias, with improved electrical performance (coarse working point adjustment)

SUB/V	Thr_mean/e	Mismatch/e	TN/e	OUTA range/mV
-2	343	8.2	45.5	263
-3	389	17.3	52.6	278
-4	325	8.7	37	255
-5	295	8.9	34.3	244
-6	298	10.6	36.8	240

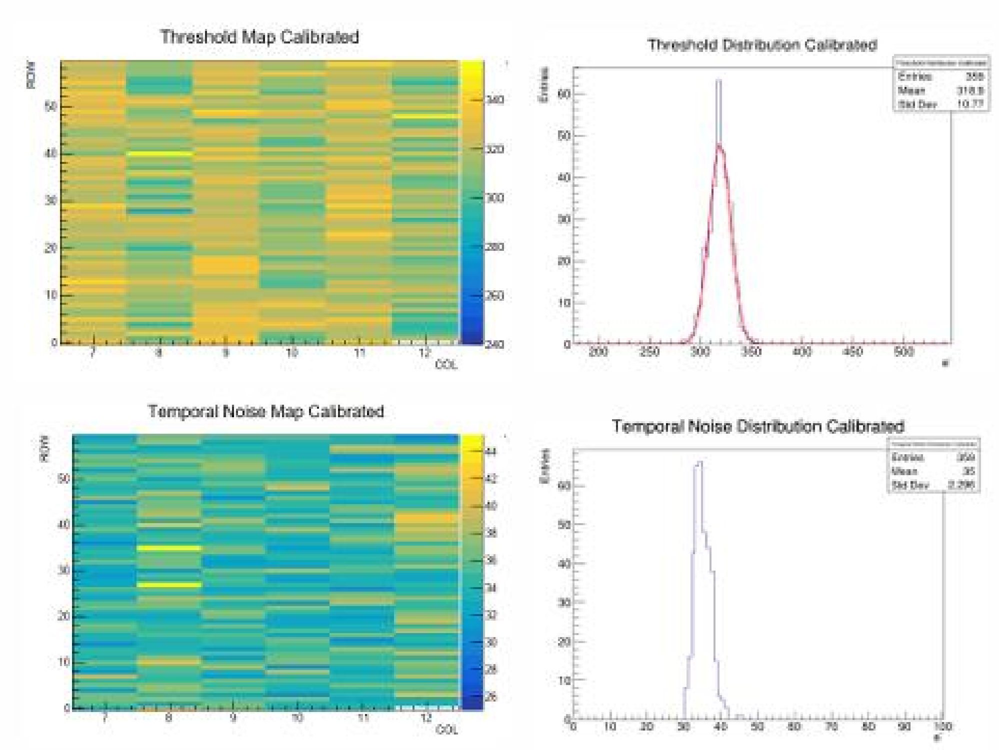


SUB/V	Thr_mean/e	Mismatch/e	TN/e	OUTA range/mV
-2	402	10.7	18.2	523
-3	352	4.1	23	477
-4	318	1.2	23.1	417
-5	267	8	17	348
-6	273	10.7	18.2	292

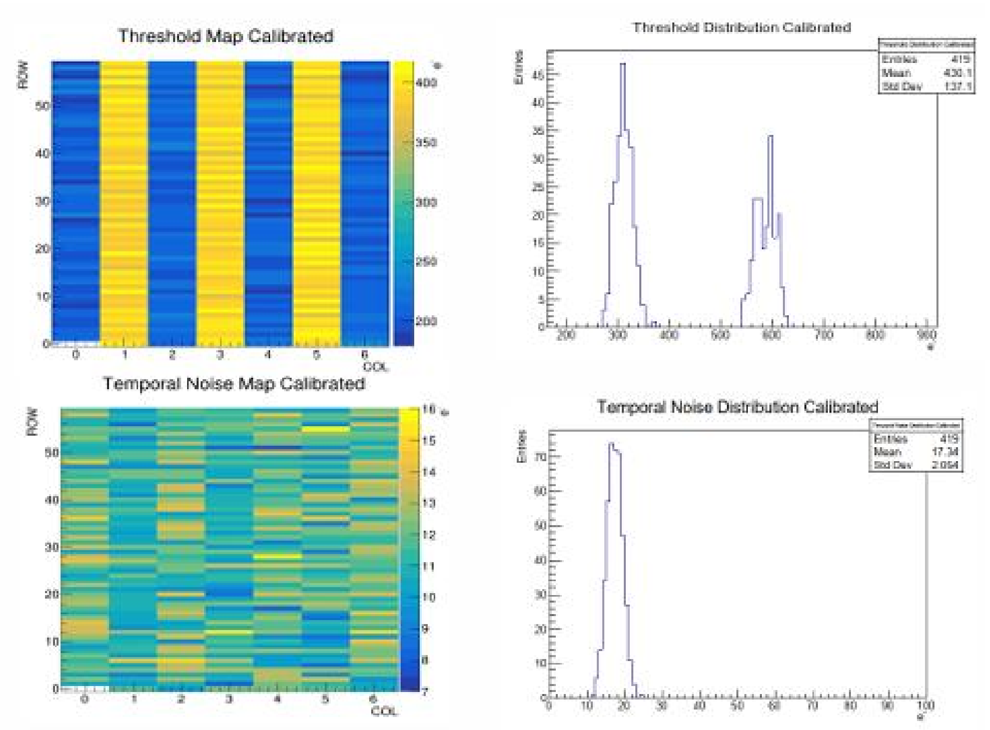


Electronics Test

- With a -6 V substrate bias applied, S-curve scans were performed across various analog configuration combinations to identify the optimal working point
- Threshold: ~ 330 e^- Mismatch: 10 e^-
- TN: 35.0 e- TN sigma: 1.9 e^-



strip-based



pixel-based

Laser test

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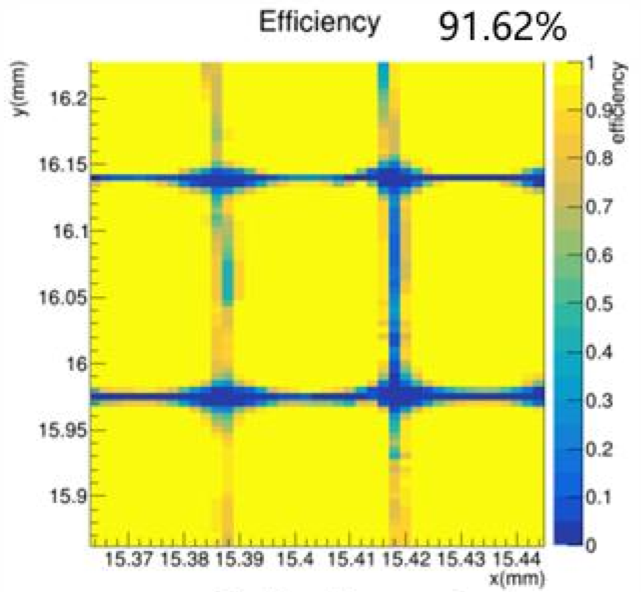
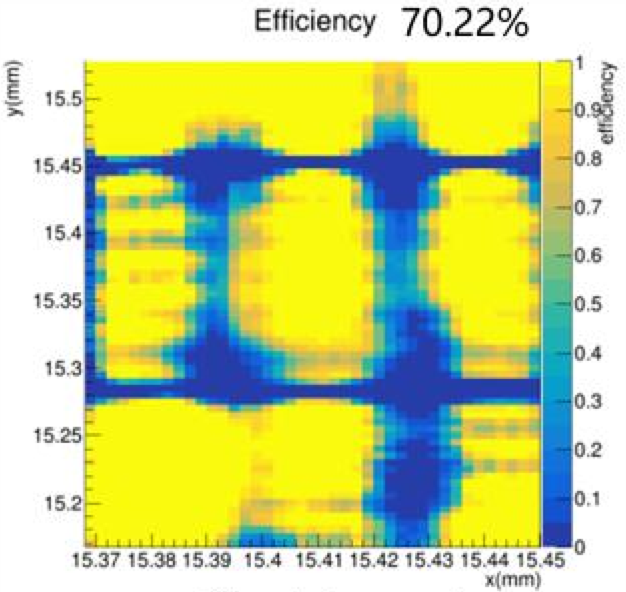
- Laser-based detection efficiency testing

A laser intensity of ~600e$^-$ (<0.375 MIP) was established via S-curve calibration

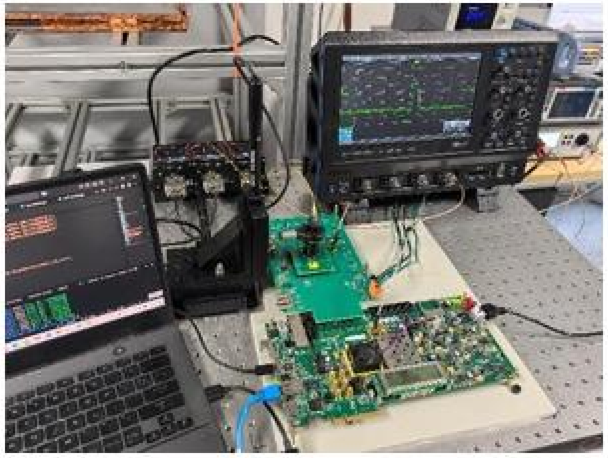


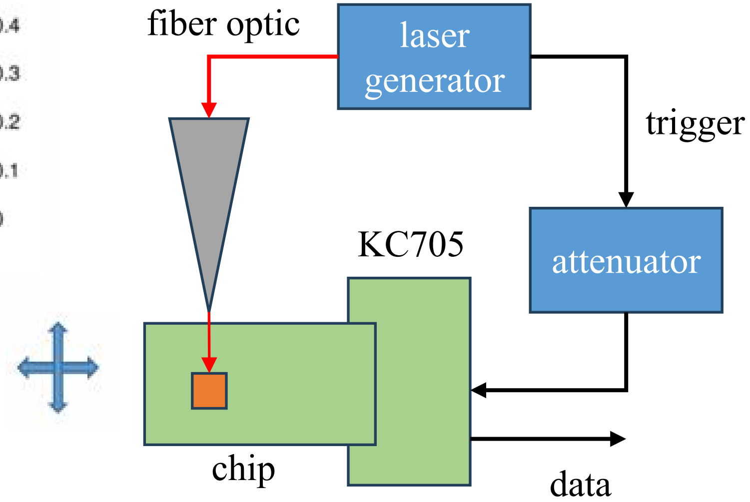
Strip-based



Pixel-based

- Strip-based array demonstrates better detection performance compared to the pixel-based array





Laser test

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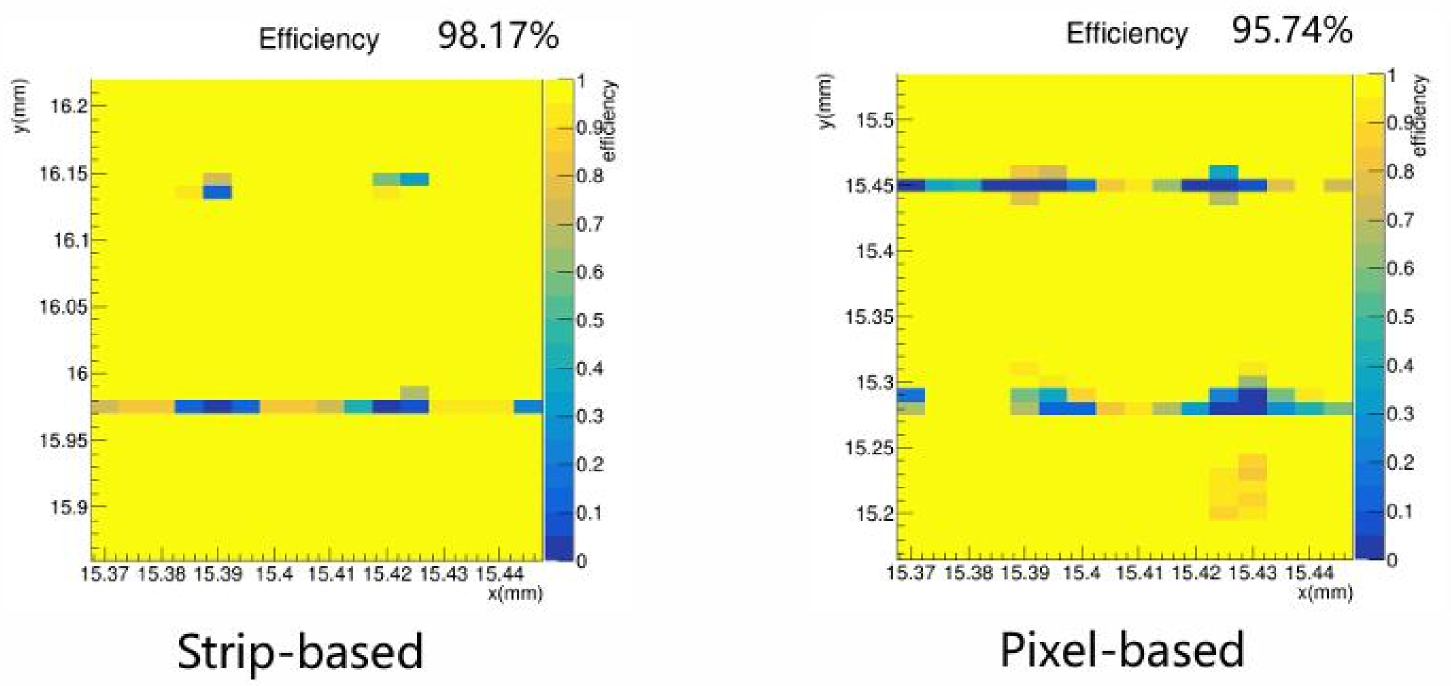
- Laser-based detection efficiency testing

A laser intensity of ~800e$^-$ was established via S-curve calibration



Test of CharTPix_130 3T chip

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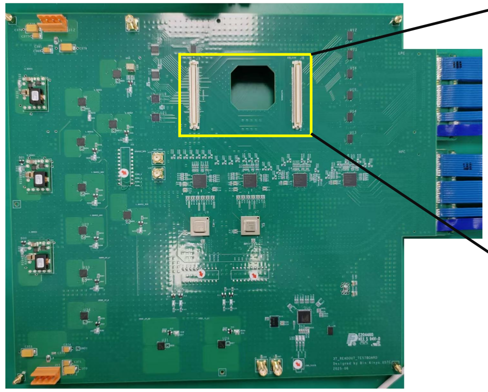
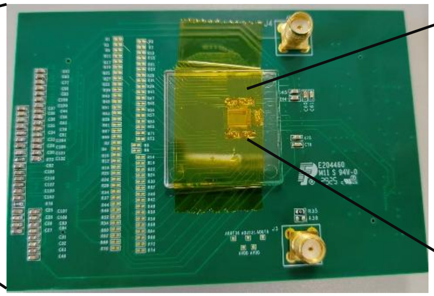
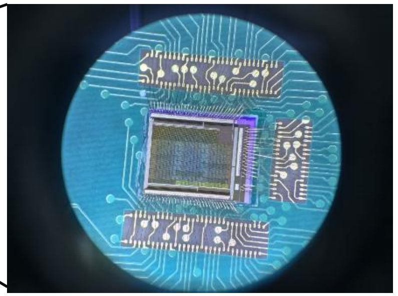
- CharTPix_130 3T Chip
  - ➢ 6×6 pixel test structure with parallel analog readout of all pixels
  - ➢ Available in 45 combinations of sensor variants
- 1st Ver. 3T test system
  - ➢ up to 16ch. data acquisition
  - ➢ 2nd Ver. test system construction on-going
    - ✓ Up to 32ch. Data acquisition
- Test methods



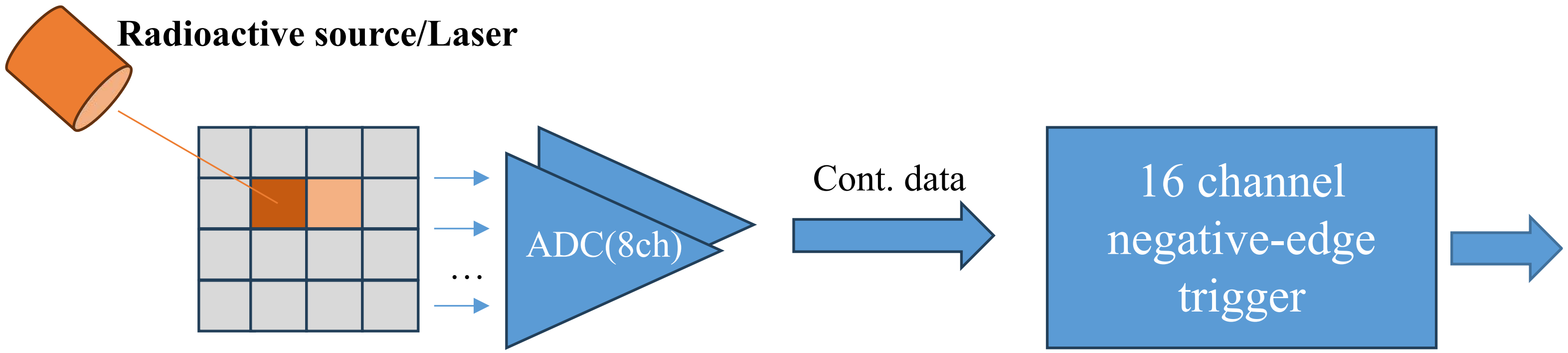
1st Ver. Mother board

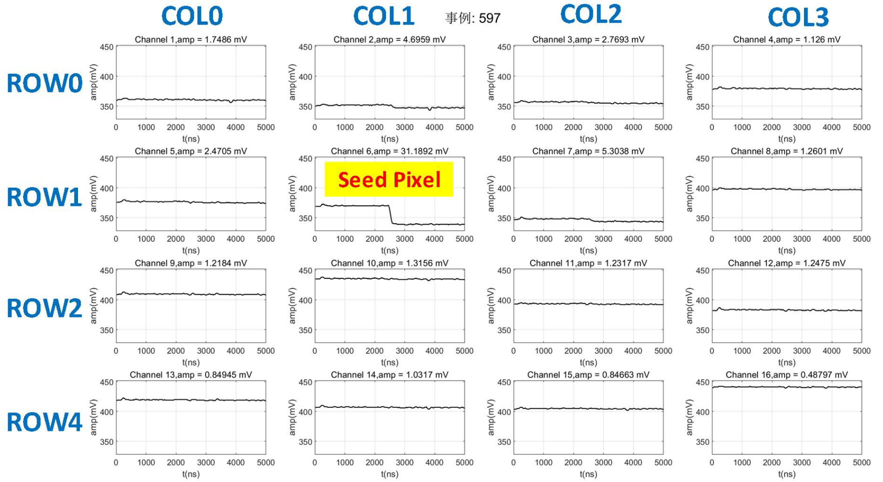


Chip carrier board



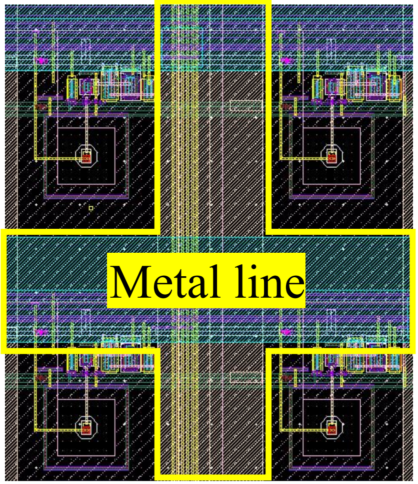
Wire bonding



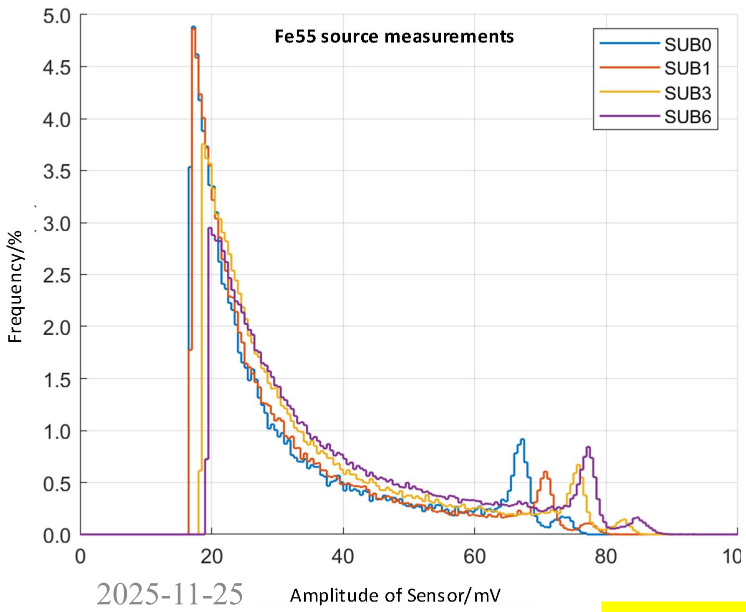


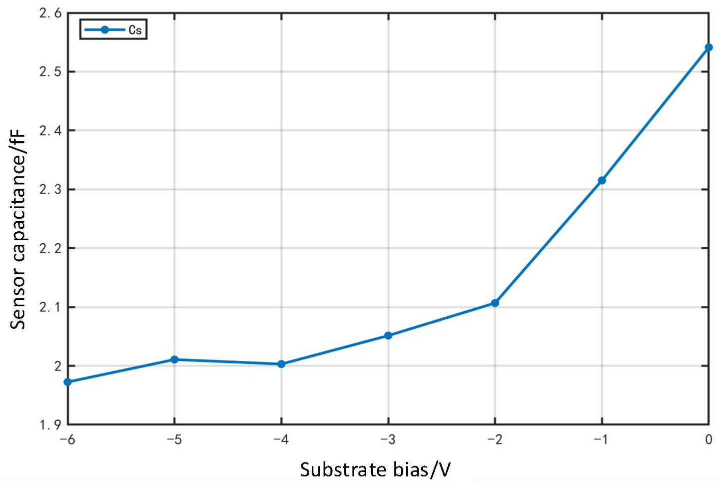
Preliminary Results for 3T sensors

- Sensor variants: NW size=2μm, PW spacing=2μm, diode reset; Pitch 28μm×28μm
- Full energy peak can be seen from SUB bias=-6 V to 0 V
- Calculated Cs = 1620 e- / ($V_{out,peak}/A_v$)– C_{cc} – C_{FE}, C_{cc} & C_{FE} extracted from layout
- Laser measurement: Efficiency drops to 0 at pixel edge
  - Possibly due to laser light being reflected by the metal line

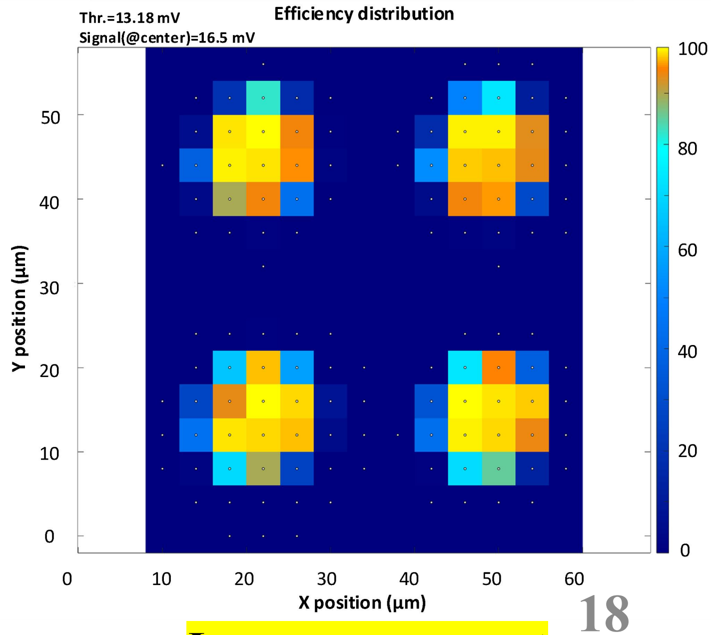


Layout of 4 pixels





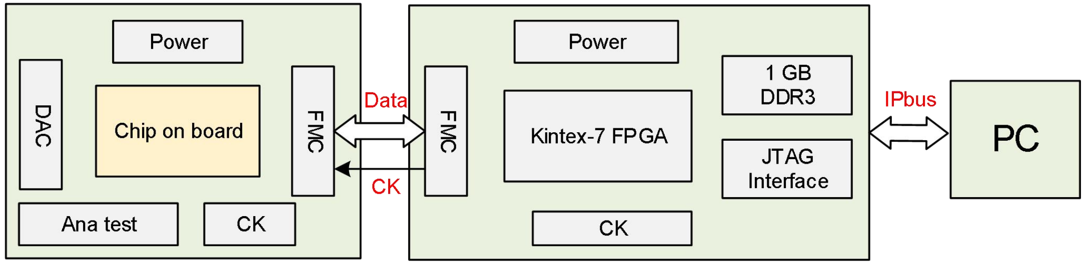
Fe55 measurement



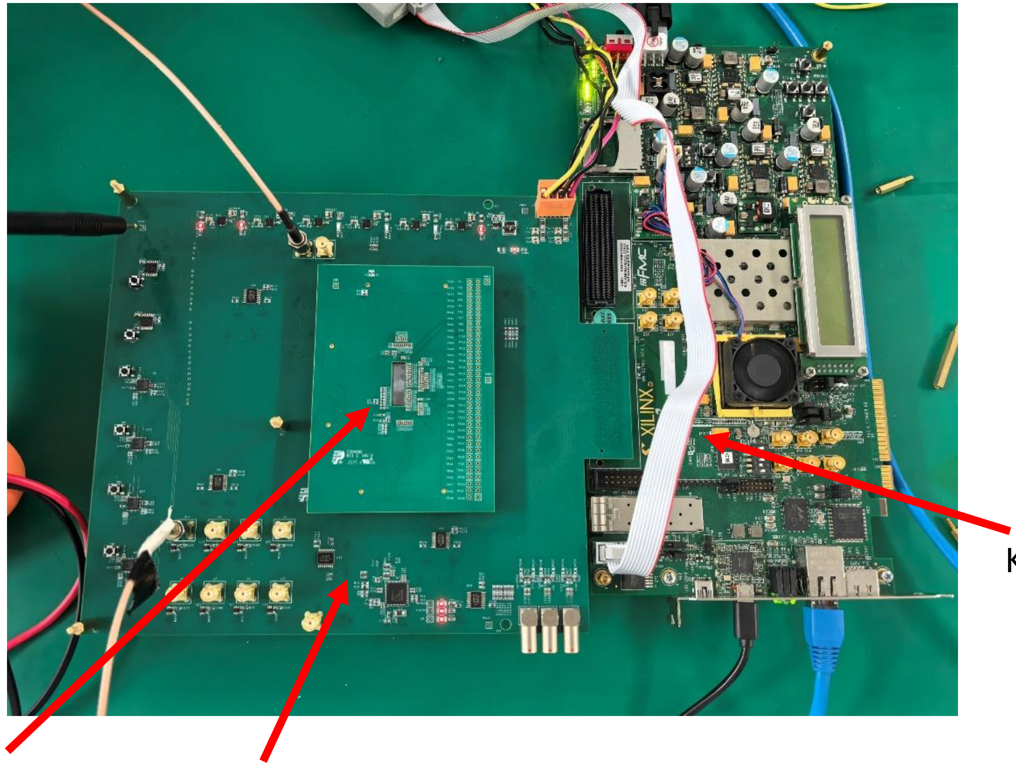
Laser measurement

CharTPix_130_chip4 test platform

Wire bonding



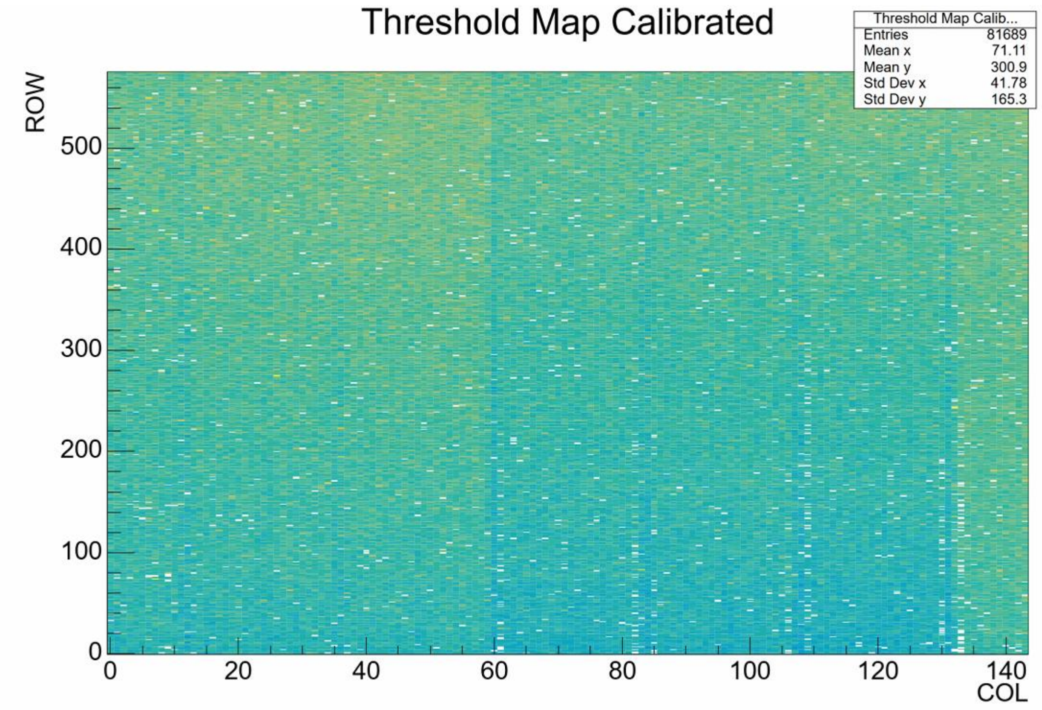
Test system block diagram

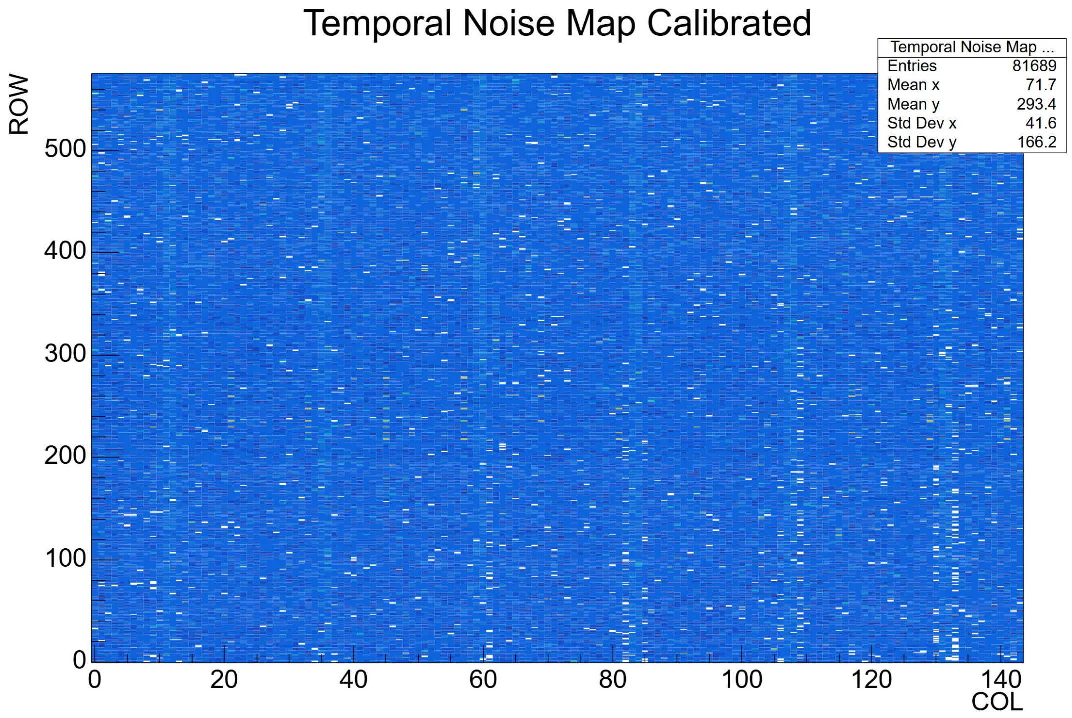


CharTPix_130 test platform

Electronics Test

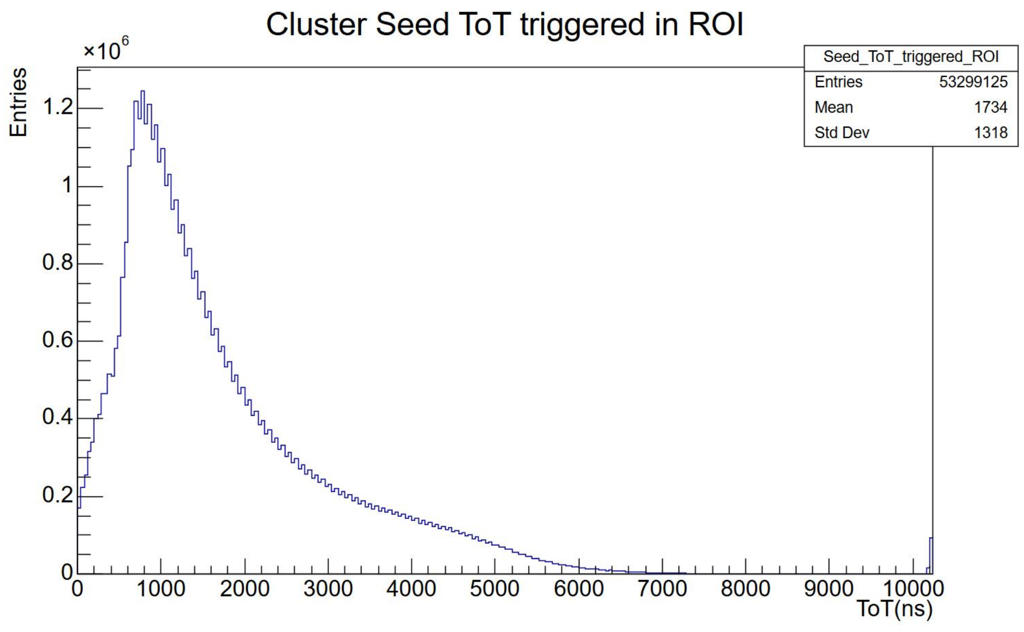
- Threshold: 252.0 Mismatch: 31.0
- TN: 7.1 TN sigma: 2.3(@SUB = -4 V)



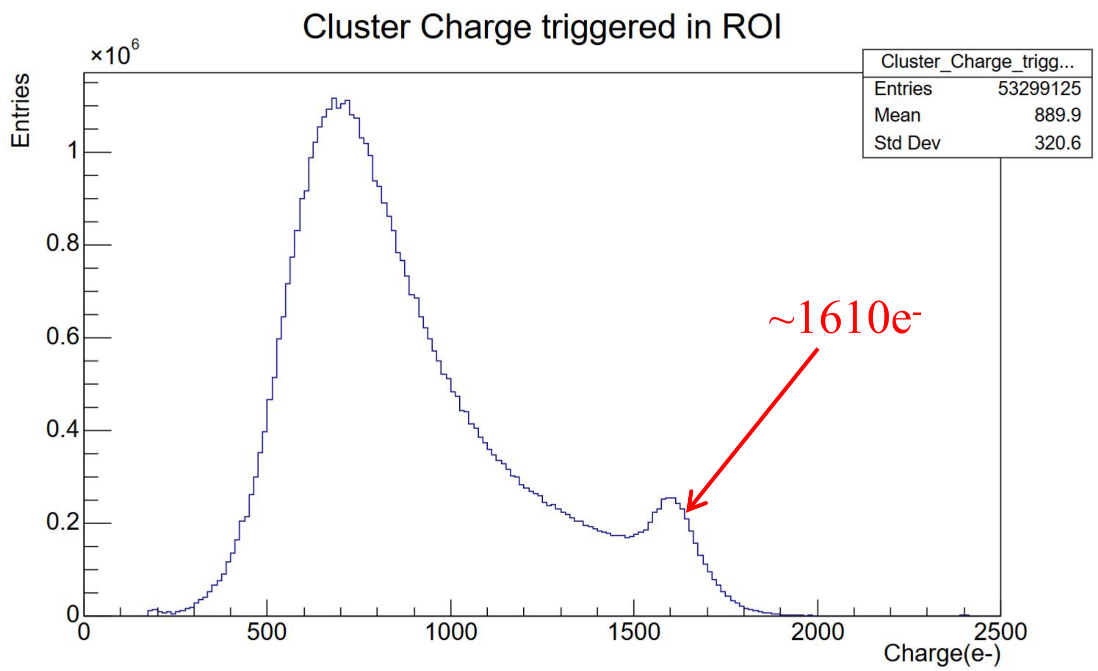


Fe55 test

- Per-pixel ToT - Qinj calibration
- The Kα peak is clearly observed, with its spectral position consistent with expectations



ToT Distribution



Spectrum

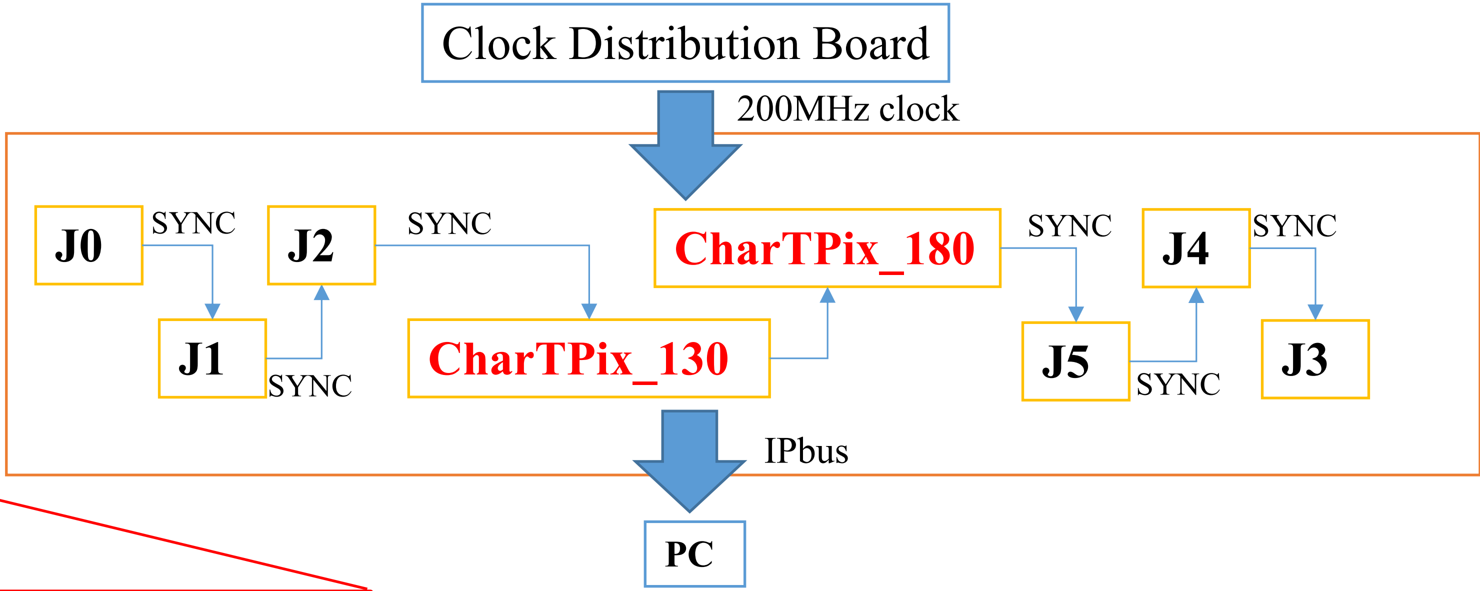
Power consumption test

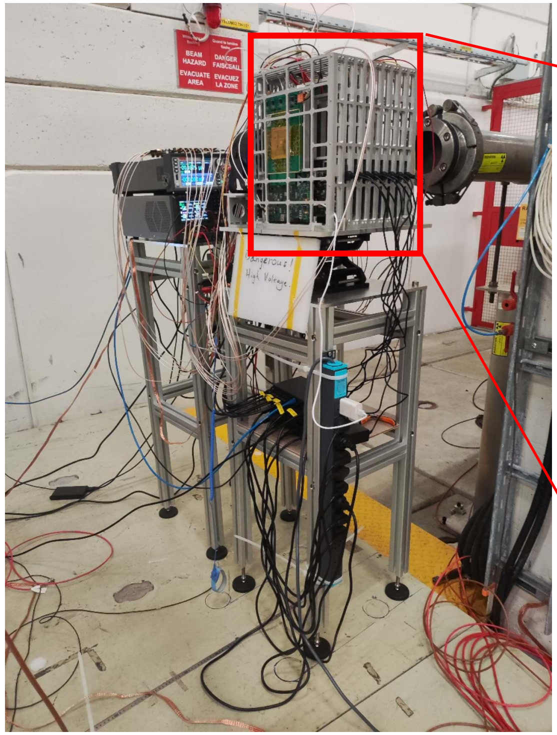
- The power consumption generated by different sections of the CharTPix_130 is as follows:

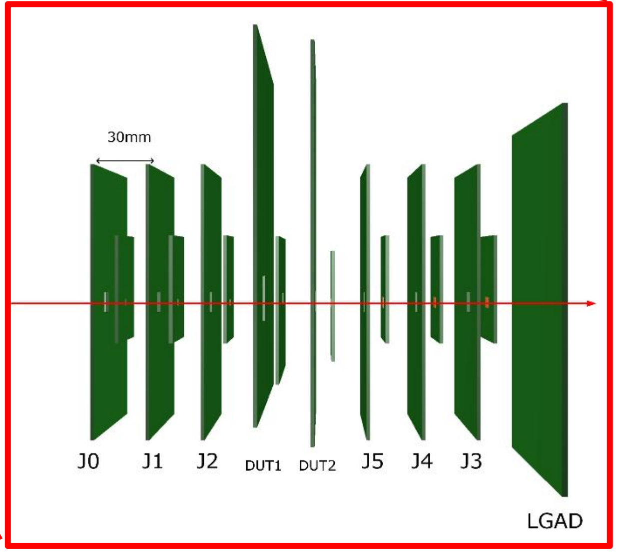
	Design Value		Measured Value	
Contribution	power consumption	Remarks	power consumption	Remarks
Pixel Array Analog Power	16.3 mW/cm^2	Pitch 33.2 μm	20.9 mW/cm^2	Including analog configuration circuit power consumption
Timestamp Distribution Power	11.0 mW/cm^2	40 MHz	6.3 mW/cm^2	25 MHz
Pixel Array Dynamic Power	2.1 mW/cm^2	8.7 MHz/cm^2	31.3 mW/cm^2	End-of-column driver anomaly
Peripheral Digital Circuit Power	6.4 mW	Double column×6		
PLL + Serializer + SLVS Power	5 mW			
Analog Configuration Circuit Power	6.3 mW	DAC + End-of-Column Current Mirror		
Total Chip Power Consumption	44.5 mW		~60 mW/cm^2	

Beam test

- Telescope System Introduction
  - ✓ Particle Species
    - ➢ 4 GeV hadron
    - ➢ 10 GeV hadron
    - ➢ 10 GeV muon
    - ➢ 1 GeV electron+





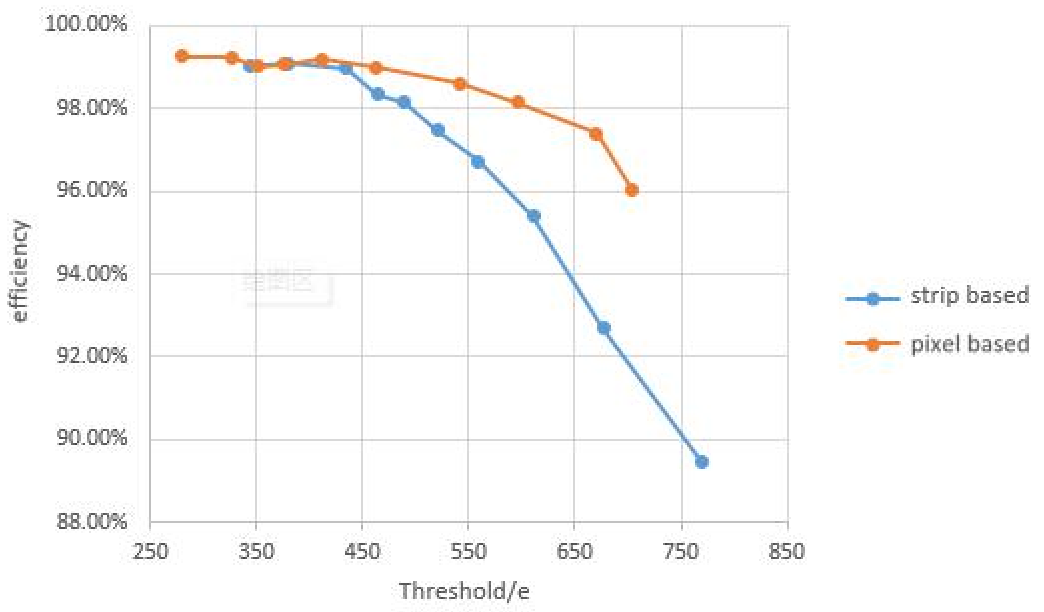


- Telescope System
  - ➢ Six layers of Jadepix-3 chips serving as reference tracking detectors (J0-J5)
  - ➢ One layer of LGAD as the timing reference detector
  - ➢ Two DUT layers: CharTPix_180 and CharTPix_130

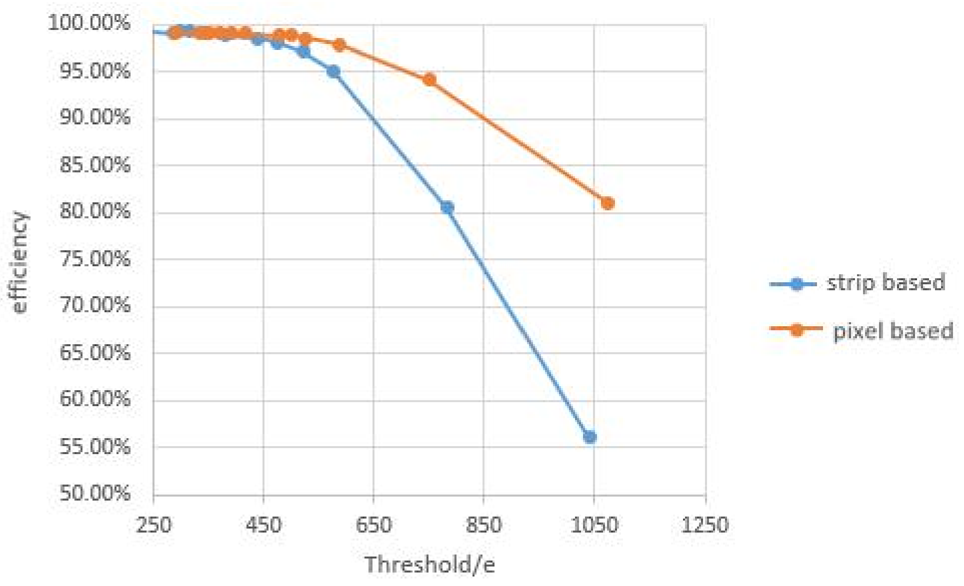
Preliminary Analysis of Beam Test Data

- CharTPix_180 detection efficiency

SUB = -6 V，10GeV hadron



SUB = -4 V，4GeV hadron



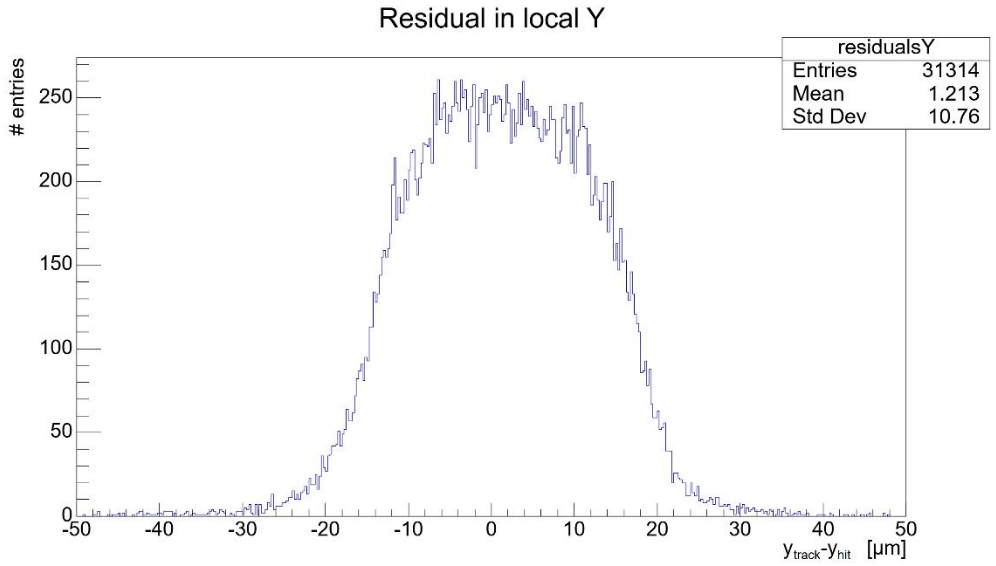
- Even at a threshold of 700e, the efficiency of both types of pixels can exceed 90%
- indicating the excellent charge collection performance of the strip based pixels.

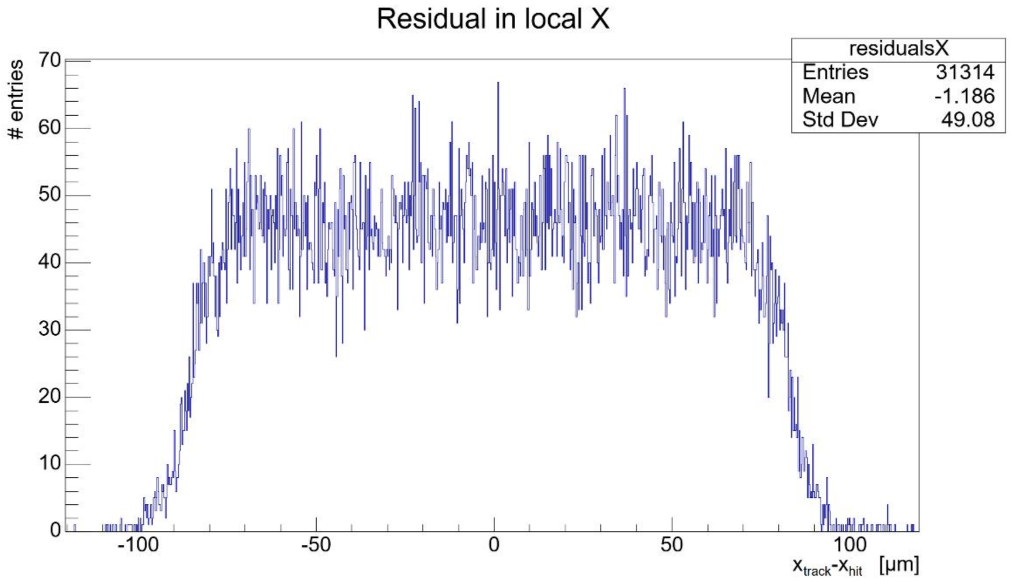
- Under a -4 V bias voltage, although the detection efficiency shows some degradation, it still maintains a level above 98% at a threshold of 500 electrons.

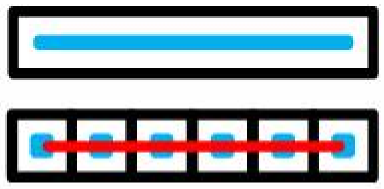
Preliminary Analysis of Beam Test Data

University of Science and Technology of China

- CharTPix_180 spatial resolution





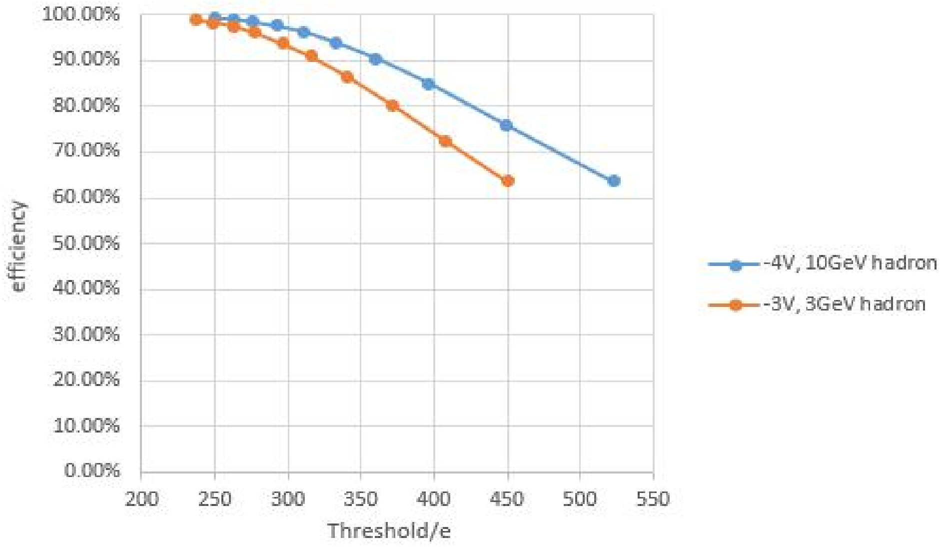


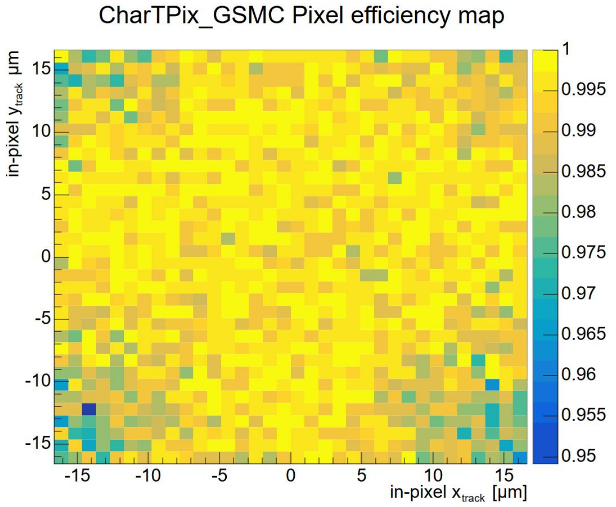
@SUB = -6 V , Threshold = 500 e

- Position resolution (without track error subtraction)
  - Long-side 49.1 μm
  - Short-side 10.8 μm

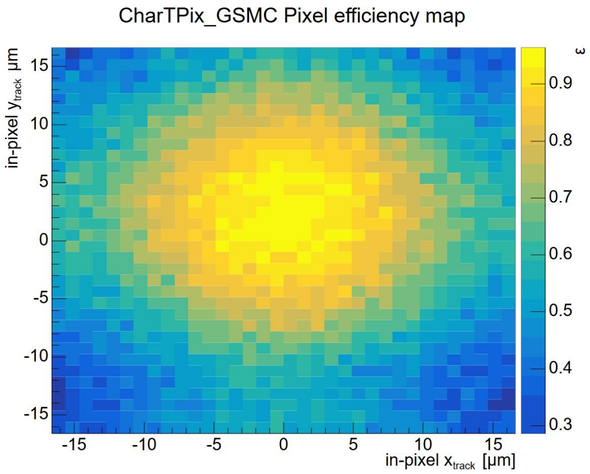
Preliminary Analysis of Beam Test Data

- CharTPix_130 detection efficiency
- 10 GeV hadron beam, -4 V substrate bias
  - ➢ Detection efficiency >99% at 250 e⁻ threshold
  - ➢ Higher efficiency at pixel center, lower at edges — correlated with charge sharing
- 4 GeV hadron beam, -3 V bias:
  - ➢ Detection efficiency ~98.9% at 240 e⁻ threshold
  - ➢ More pronounced efficiency degradation with decreasing threshold





Threshold 250 e



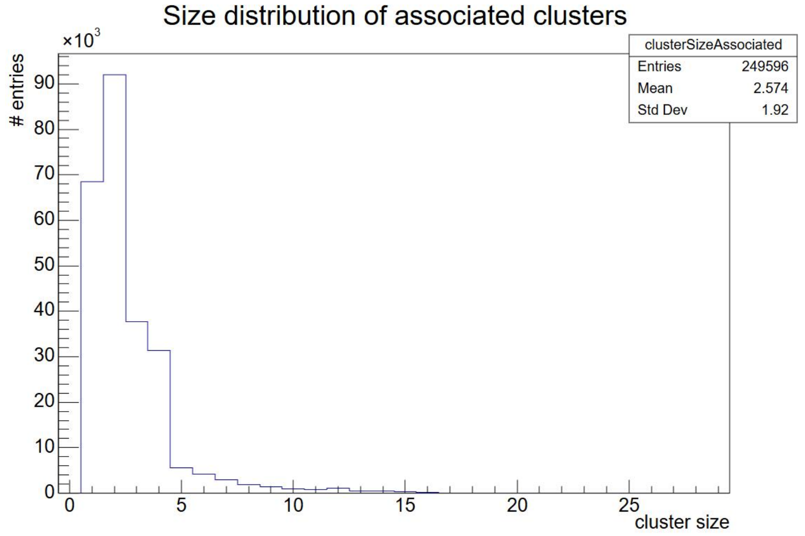
Threshold 520 e

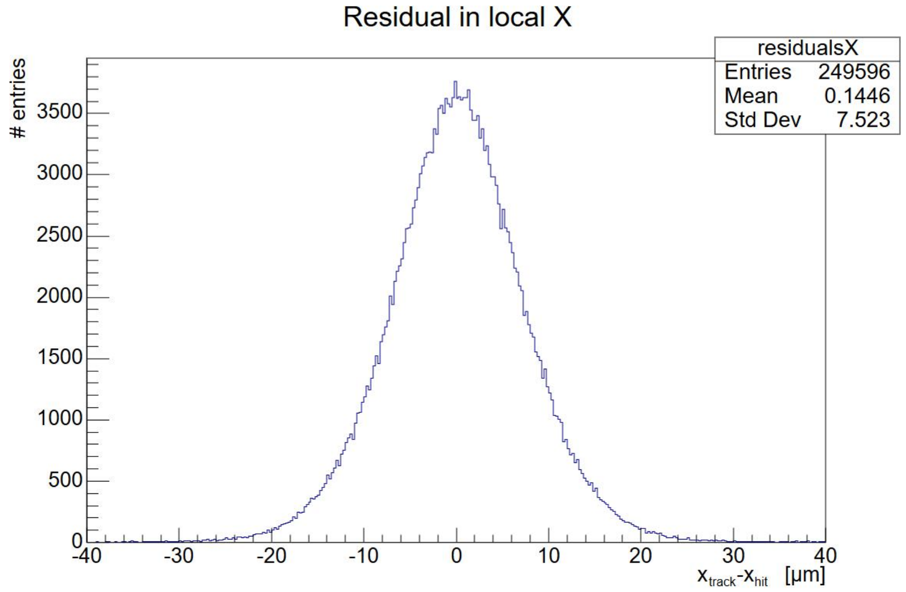
Preliminary Analysis of Beam Test Data

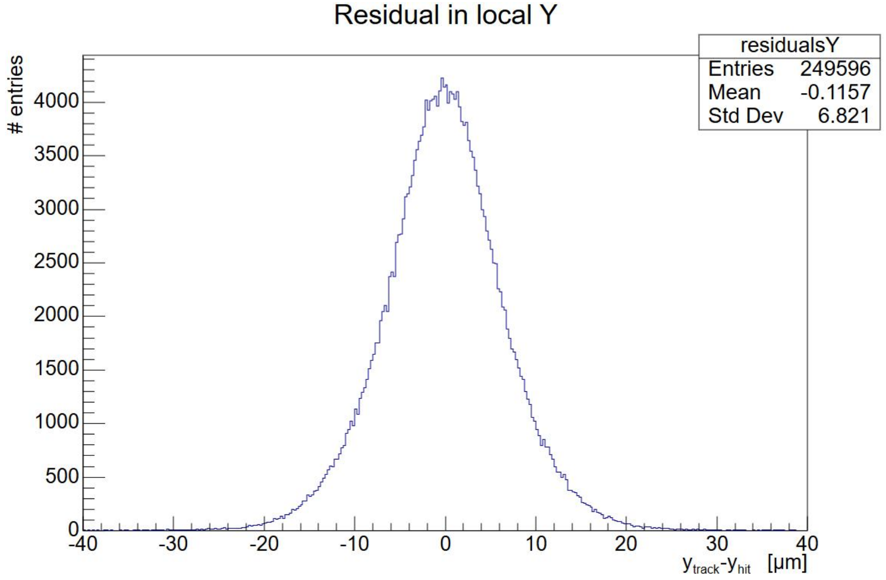
- CharTPix_130 spatial resolution

  @SUB = -4 V , Threshold = 260 e

  - Position resolution (without track error subtraction)
    - Column-direction 7.5 μm
    - Row-direction 6.8 μm
  - Average cluster size 2.57



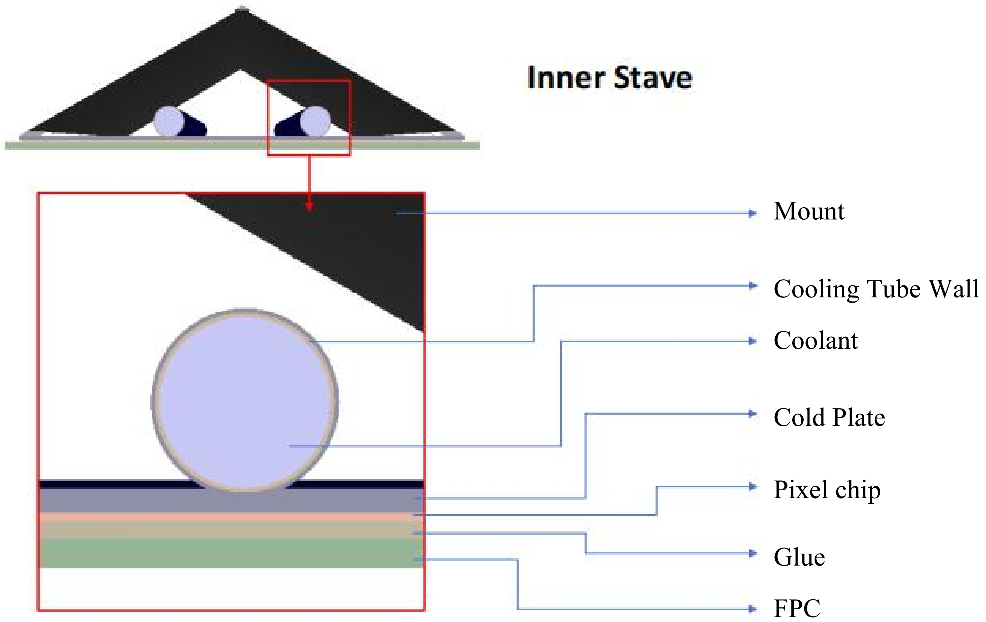


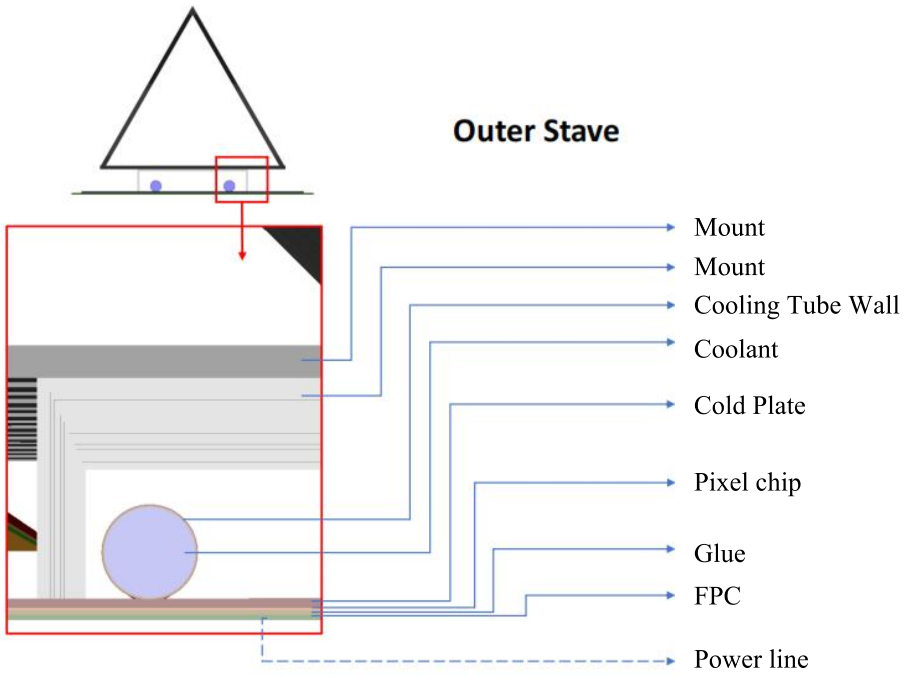


Outline

- MAPS-based Inner Tracker for STCF
- R&D of MAPS
  - Prototype chip design
  - Test of MAPS
- **Stave & Mechanical Design**
- Conclusions

Stave design





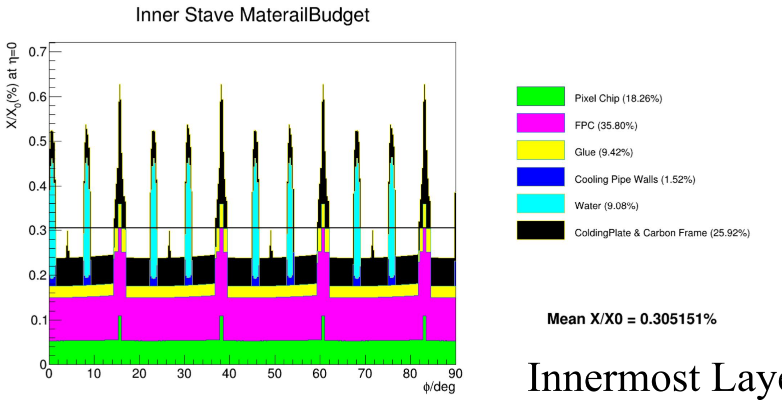
- ✓ 300mm Length Inner Structure – Maximum Deformation: 49.3 µm
- ✓ 500mm Length Inner Structure – Maximum Deformation: 330.9 µm
- ✓ 1.45m Length Outer Structure – Maximum Deformation: 204 µm

The ITKM employs an Inner Stave structure for its innermost layer, while the outer two (or three) layers use an Outer Stave structure.

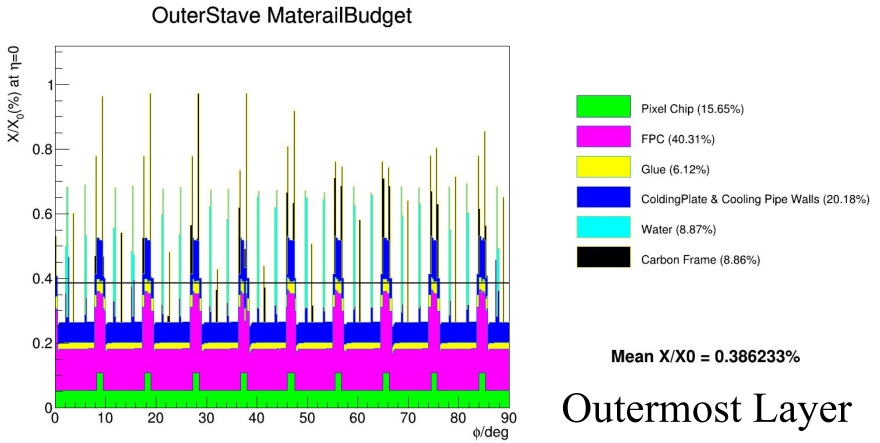
Stave design

- Material Budget Estimation

	Material Budget Estimation（X/X0）
Support Structure (Mount + Cold Plate)	ITS2 Inner Structure (single-row chips): 0.05% ITS2 Outer Structure (double-row chips): 0.08%
Cooling Circuit (Piping + Water) (Based on 0.5mm radius)	0.03%(Single Pipe & Water)
FPC(2*25um Al+Kapton)	0.11% + 0.04~0.05%(Per Additional Aluminum Layer)
Chip (based on 50μm Si)	0.06%
Glue (based on total 100μm Epoxy)	0.03%
Total (including n additional aluminum layers and two cooling pipes)	ITS2 Inner Structure: 0.31% + (0.05%) × n ITS2 Outer Structure: 0.34% + (0.05%) × n



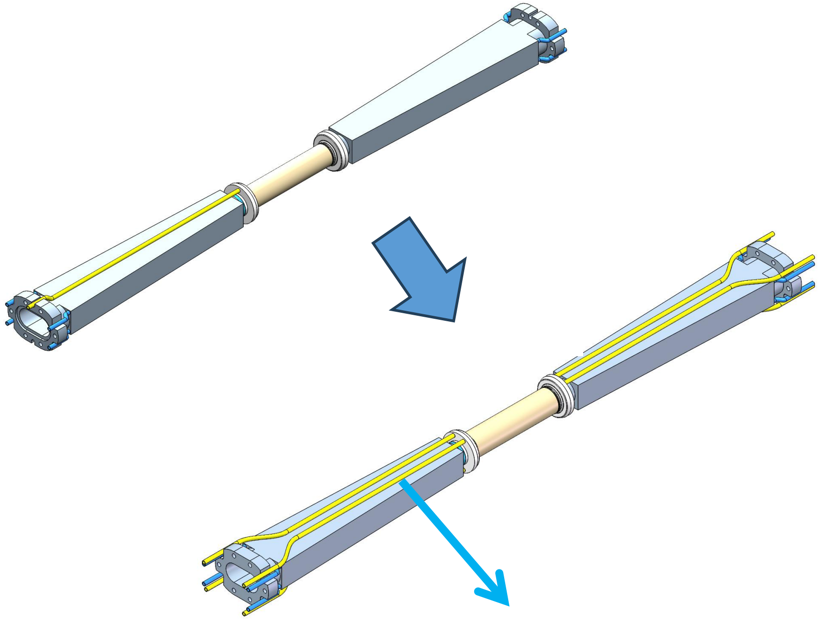
Innermost Layer



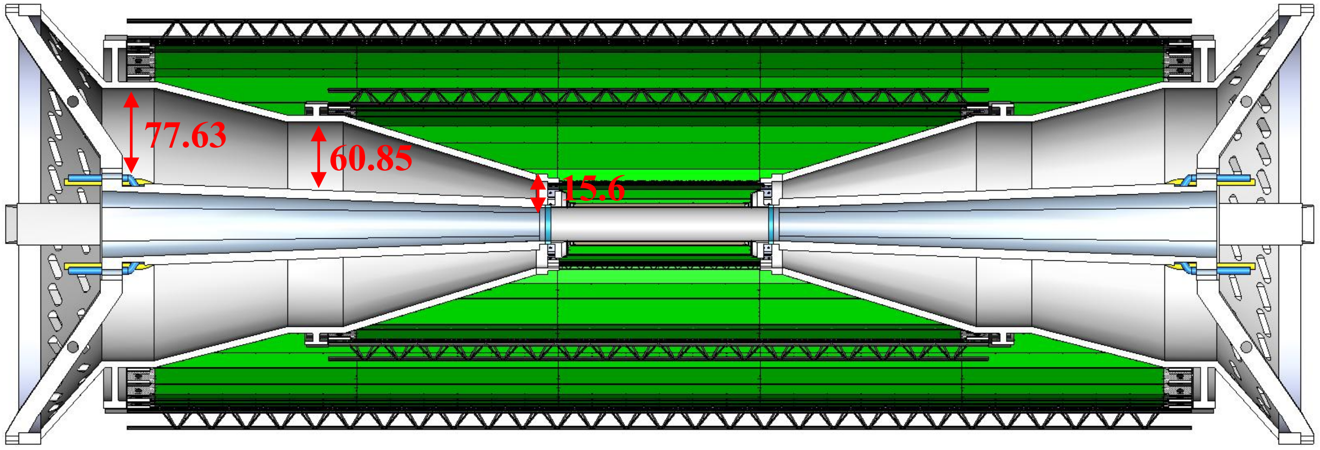
Outermost Layer

Mechanical Structure

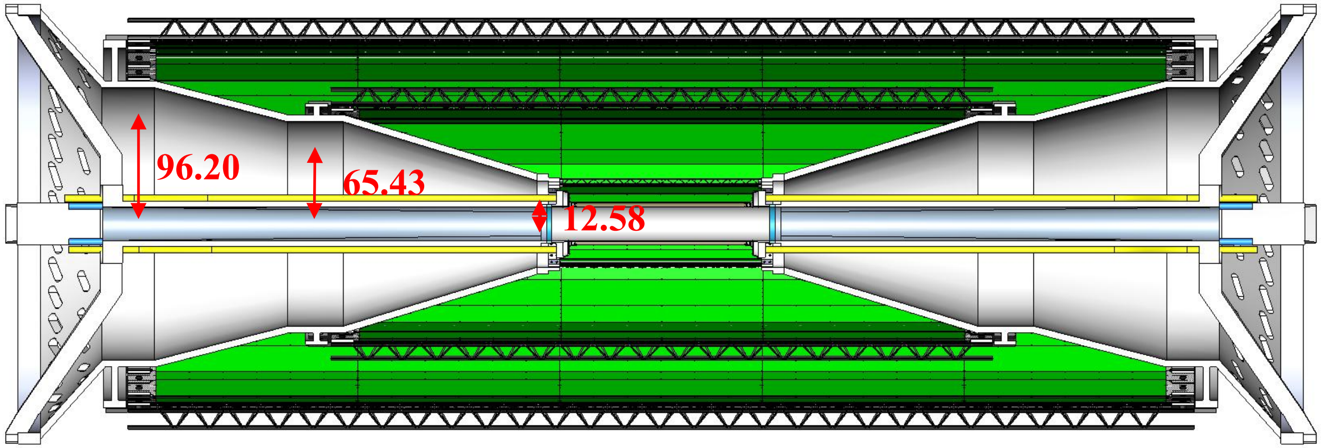
- Spatial Geometry Dimensions Between Inner Barrel and Beam Pipe



Cooling Pipes (Total: 4)



X-direction



Y-direction

The minimum distance in the X-direction to the beam pipe is about 15.6 mm.
The minimum distance in the Y-direction to the beam pipe cooling pipe is about 12.58 mm.

Conclusions

- MAPS-based inner tracker for STCF is under R&D, aiming at:
  - $\sigma_{r\varphi}$<100 μm
  - time resolution ~20 ns
  - power consumption ~50 mW/cm^2
  - material budget ~0.3% X_0 per layer
- The design work for Version 1.0 prototype chips implementing two different technologies has been completed, along with preliminary testing.
- Promising test results have been obtained, and technical optimization is currently underway.
  - CharTPix_180

    Detection efficiency:almost 99%

    spatial resolution:49.1 μm and 10.8 μm
  - CharTPix_180

    Detection efficiency:almost 99%

    spatial resolution:~7 μm
- ITKM mechanics also under design.

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THANKS!

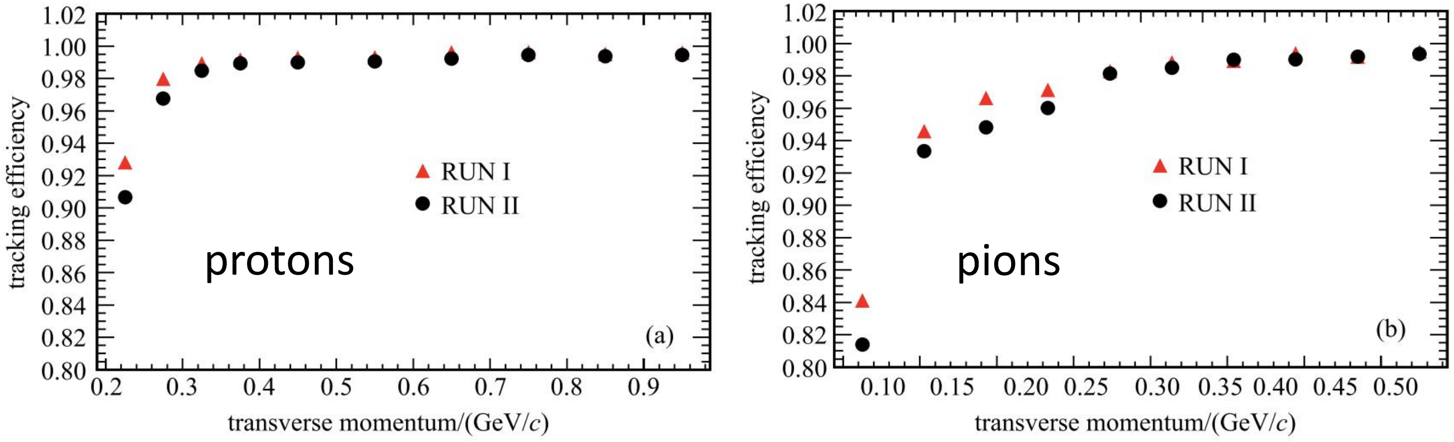
Back up

STCF ITK Physics Requirements

- STCF Physics target

Process	Physics Interest	Optimized Subdetector	Requirements
$\tau \to K_s \pi \nu_\tau$,	CPV in the τ sector,		acceptance: 93% of 4π; trk. effi.:
$J/\psi \to \Lambda\bar{\Lambda}$,	CPV in the hyperon sector,	ITK+MDC	$> 99\%$ at $p_T > 0.3$ GeV/c; $> 90\%$ at $p_T = 0.1$ GeV/c
$D_{(s)}$ tag	Charm physics		$\sigma_p/p = 0.5\%$, $\sigma_{\gamma\phi} = 130\ \mu m$ at 1 GeV/c

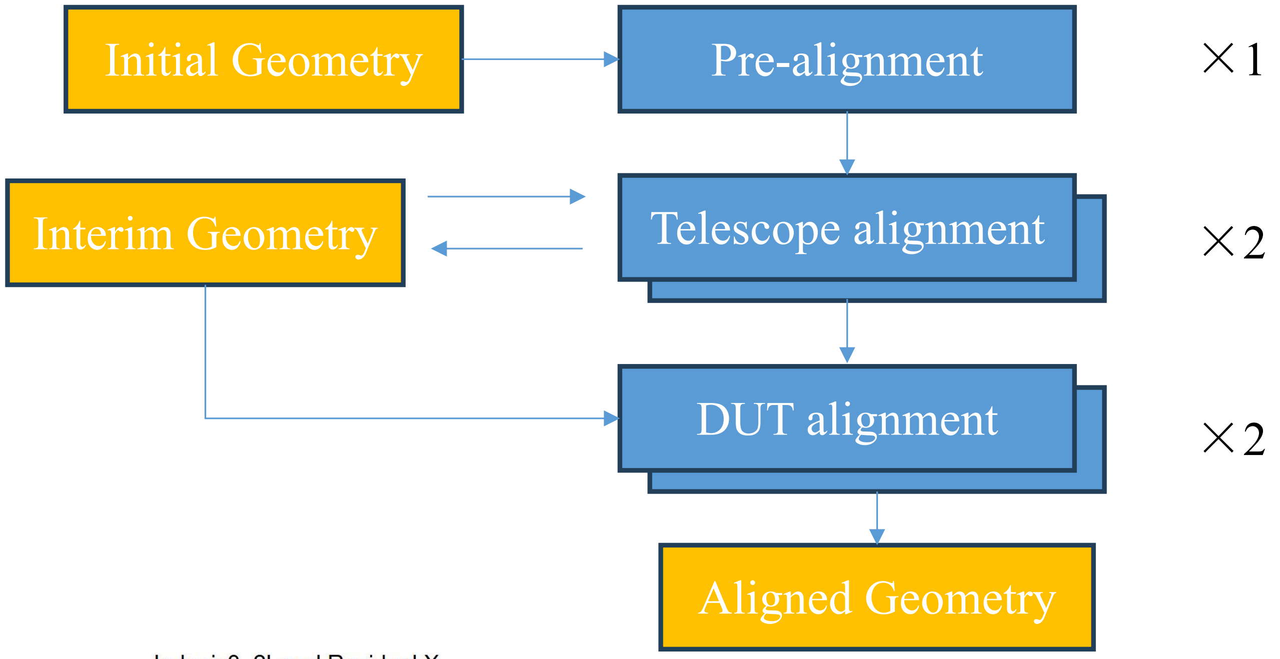
- Challenges in the detection of particle tracks in the low momentum energy region
  - Multiple Coulomb scattering leads to low efficiency of track detection
  - For BESIII, the tracking efficiency drops sharply below 100MeV

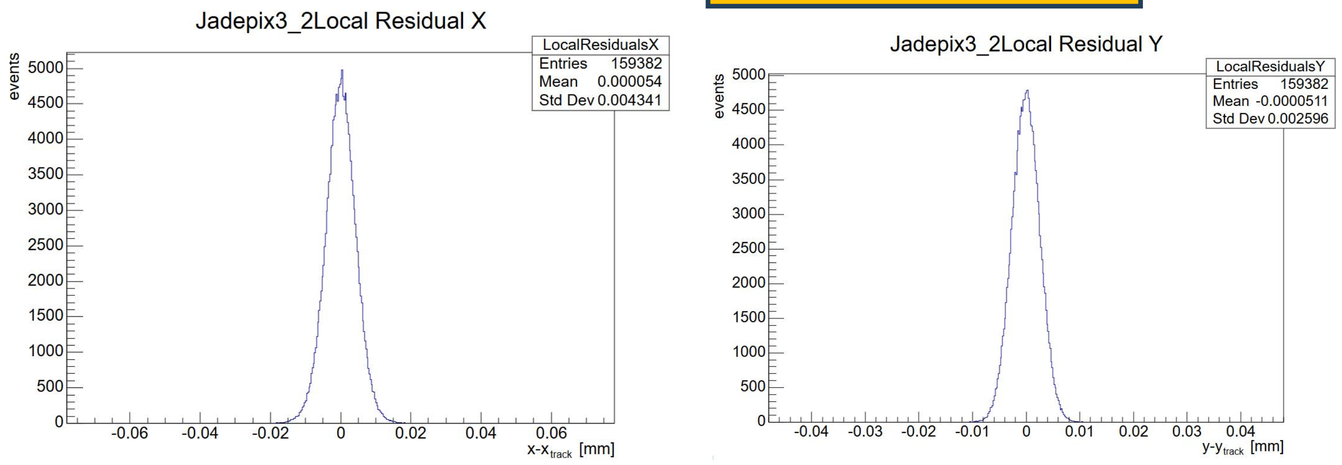


Low material budget is a necessary condition for Inner Tracker

Testbeam Detector Alignment

- Using the first Jadepix-3 layer as reference, align the positions and orientations of all other detector layers
- The alignment procedure consists of three steps:
  - Pre-alignment: Performs initial position corrections based on correlations between hit positions on each detector layer.
  - Telescope alignment: Conducts global track fitting by minimizing the total chi-square to determine positions and orientations of all telescope layers.
  - DUT alignment: Performs global track fitting by minimizing residuals between extrapolated tracks and DUT hits to determine positions and orientations of each Device Under Test.





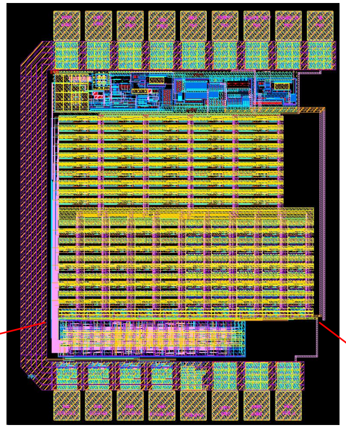
Track residuals on Jadepix3_2

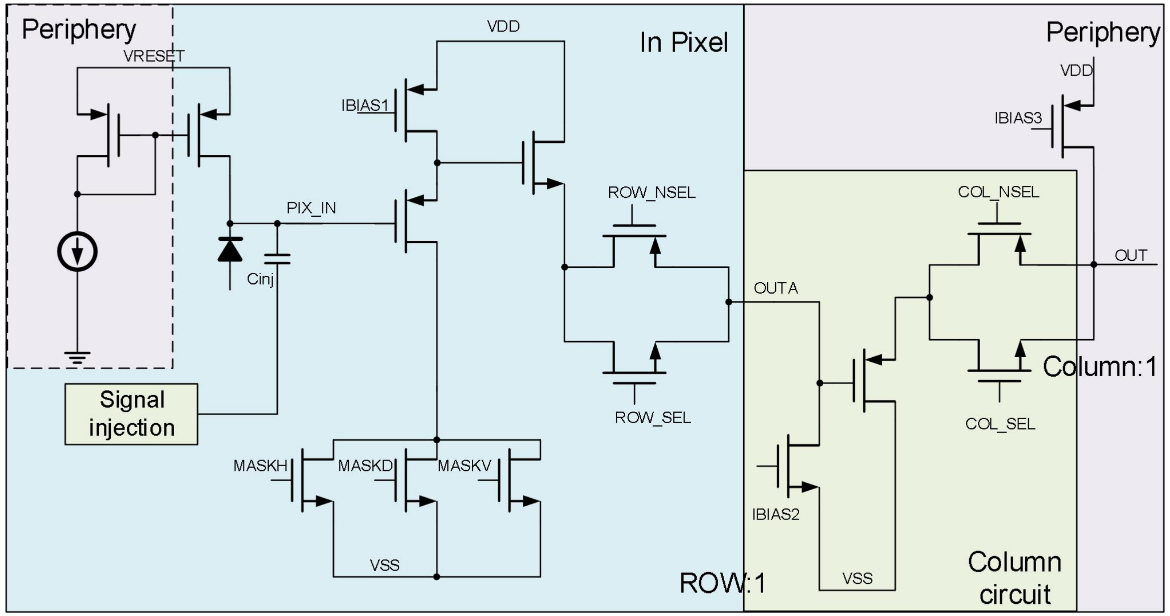
CharTPix_180 Characterization chip

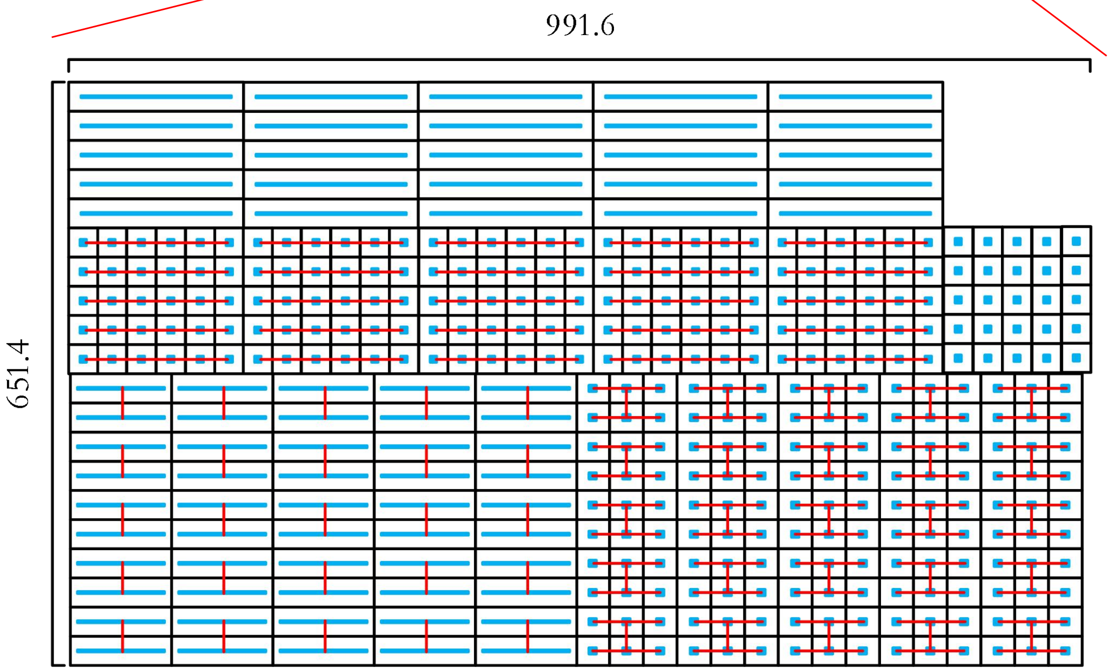
中国科学技术大学
University of Science and Technology of China

Chip 4

- To study performance of different pixel layout
- 5×5 array for each type of pixel
- Pure analog readout: source follower + matrix parallel readout

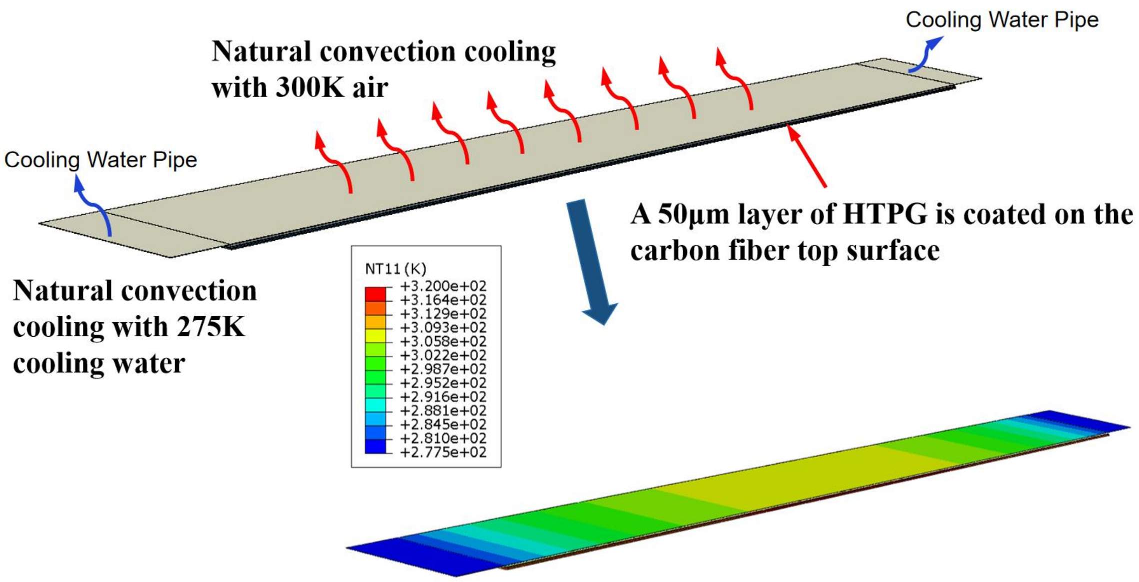


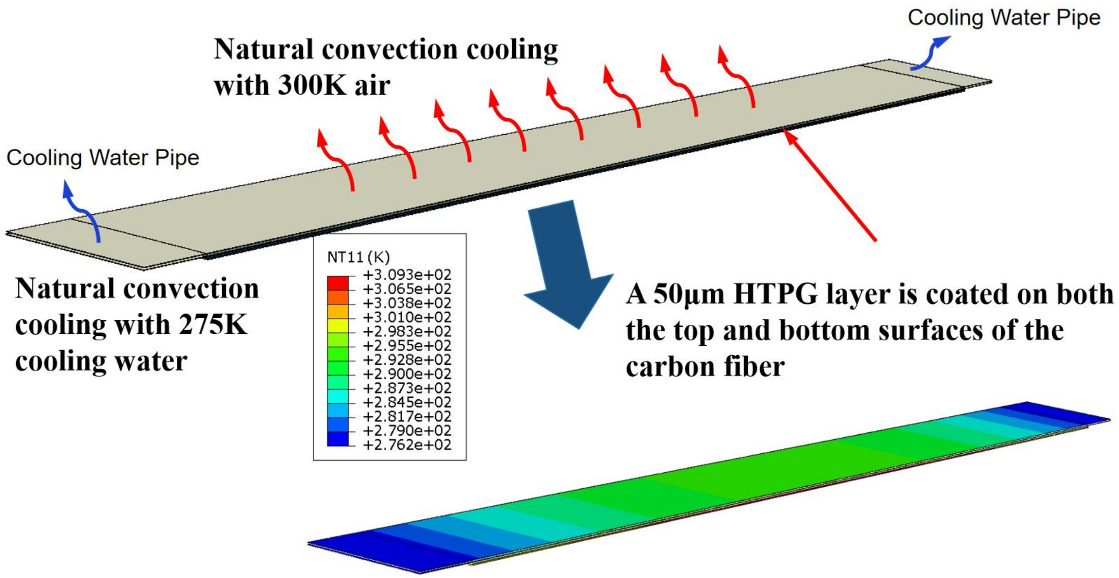




Thermal Design

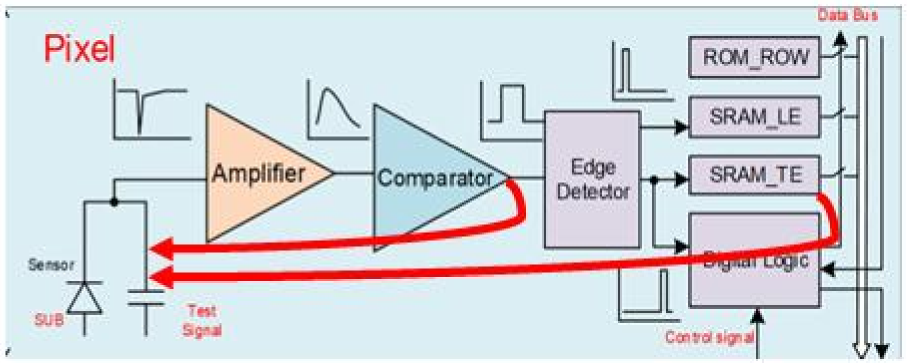
- Thermal Solution Alternatives
  - ➢ Utilizing High-Thermal-Conductivity Pyrolytic Graphite(HTPG) to conduct heat to both ends of the stave for cooling.
  - ➢ Thermal conductivity can reach 1500-2000 W/(m·K) or higher, which is over four times that of copper.





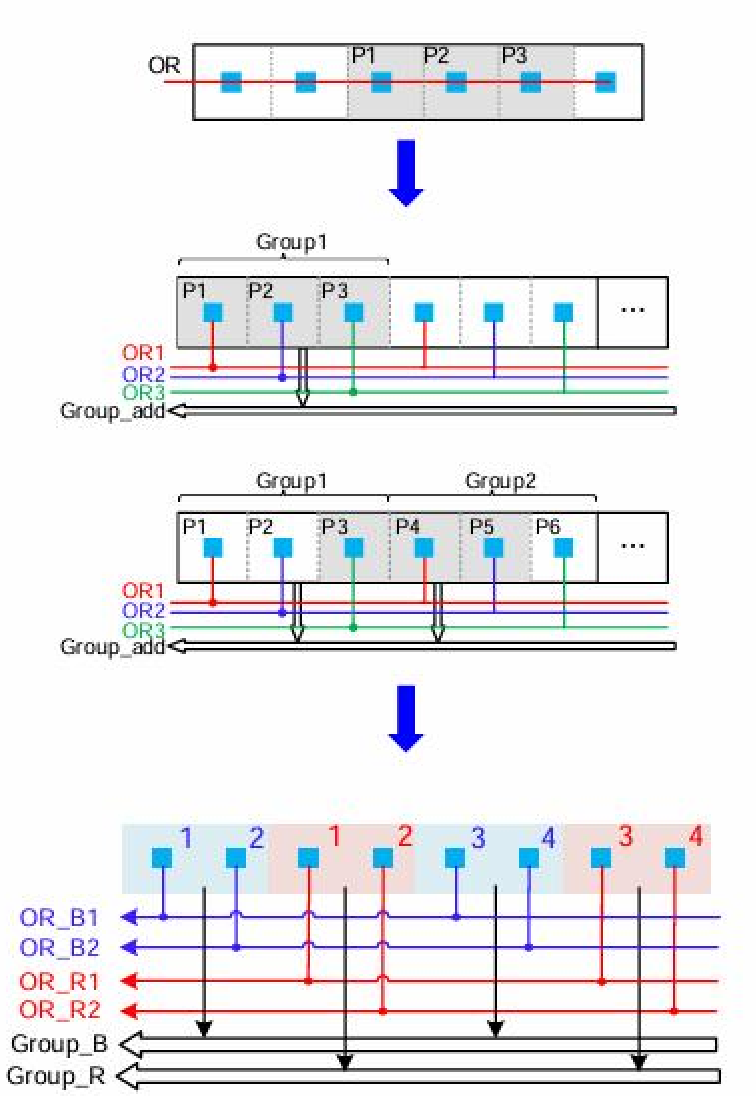
On-chip crosstalk issue

- After injecting charges, continuous reading occurs in the current column:
  - ➢ Crosstalk from the priority readout circuit to the input
  - ➢ Crosstalk from the discriminator output to the input



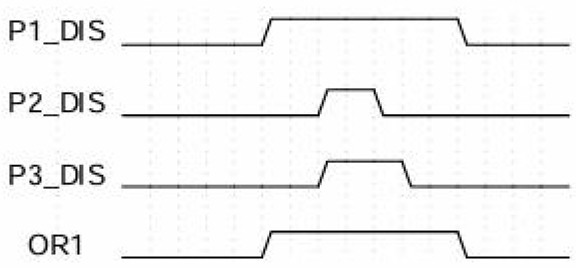
- Solution
  - ➢ Digital reset: After the FPGA receives the readout data, it performs a global reset
  - ➢ Analog reset: After the FPGA receives the readout data, it resets the bias current
- All subsequent tests only read the first hit signal

CharTPix_130 Super Pixel



Adjacent pixels are OR-ed

- ✓ Loss of ToT for small signal pixels (when cluster size > 1)



Offset pixels are OR-ed

- ✓ Prevents ToT loss for small-signal pixels (when cluster size > 1)
- ✓ Reads out the address of the valid group
- ✓ Position information is lost when multiple groups are valid at the same time

Offset pixels are OR-ed, Staggered group layout

- ✓ Prevents ToT loss for small signals
- ✓ Prevents loss of position information
- ✓ Additionally reduces digital power consumption

ToT-Qinj calibration