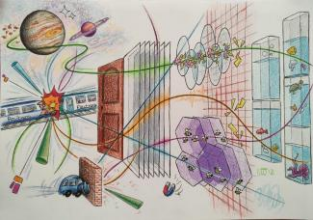


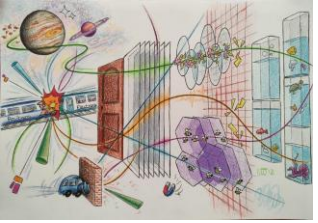
DRD3

DRD3 collaboration
(R&D on Solid-state Detector Technologies)

Gregor Kramberger on behalf of the collaboration

Jožef Stefan Institute, Slovenia

JSI
Ljubljana
Slovenia



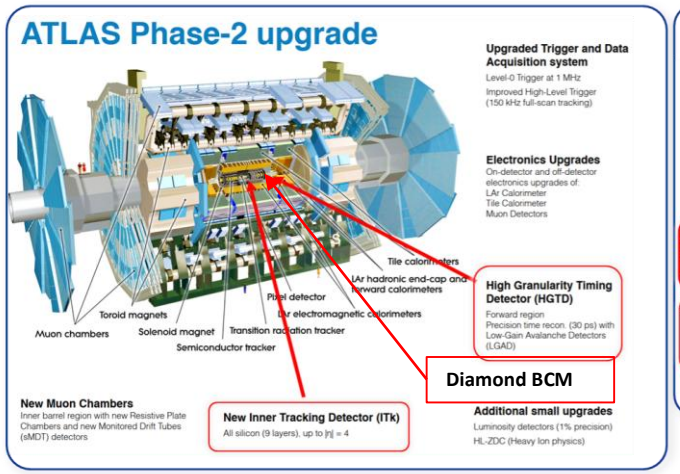
Semiconductor sensors

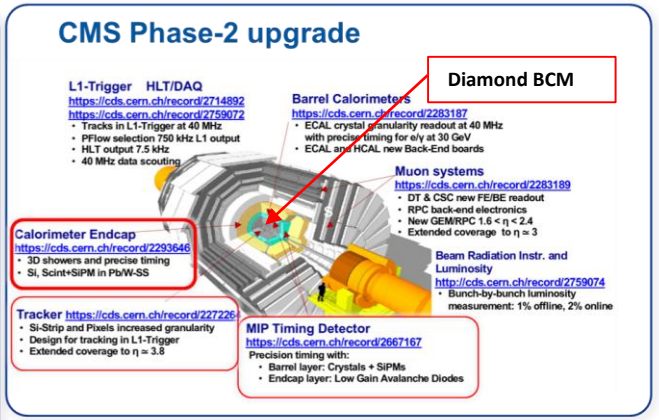
DRD3

Semiconductor detectors are the cornerstone of all present and future experiments:

- Several R&D collaborations (RD39,RD42, RD48 and RD50) in the past with crucial contribution to the HL-LHC upgrades in all experiments
- Improvements:
  - position resolution (CMS/ATLAS hybrid pixels on p type silicon)
  - timing layers (ATLAS-HGTD, CMS-ETL)
  - large scale use in calorimeters (CMS HGCAL, p-type Si)
  - lightweight monolithic pixel detectors (ALICE ITS) with excellent position resolution

Coming after the accelerator upgrade in 2029



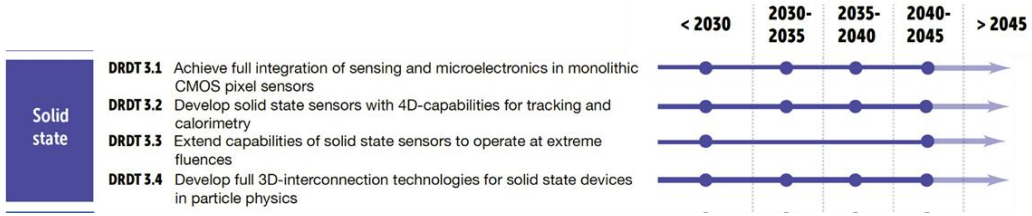


…also very close collaboration with LHCb!

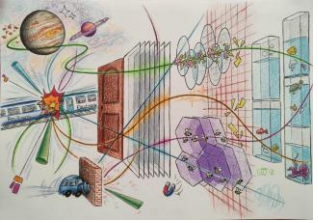
New Major Challenges for the future:

- FCC-ee/CEPC/ILC/STCF: vertex detectors with low mass, high resolution (Target per layer spatial resolution of ≤ 3-5 µm and $X/X_0 \leq 0.05\%$),
- FCC-hh/SppC: low power and high radiation hardness (up to $8 \cdot 10^{17}$ $n_{eq}cm^{-2}$). Resolving many pp hits in a bunch by ultra-fast timing in O(10-100ps)
- Full integration with electronics, mechanics, services
- Large area sensors at low cost for calorimetry

European Commission for Future Accelerators
Road map document on sensors



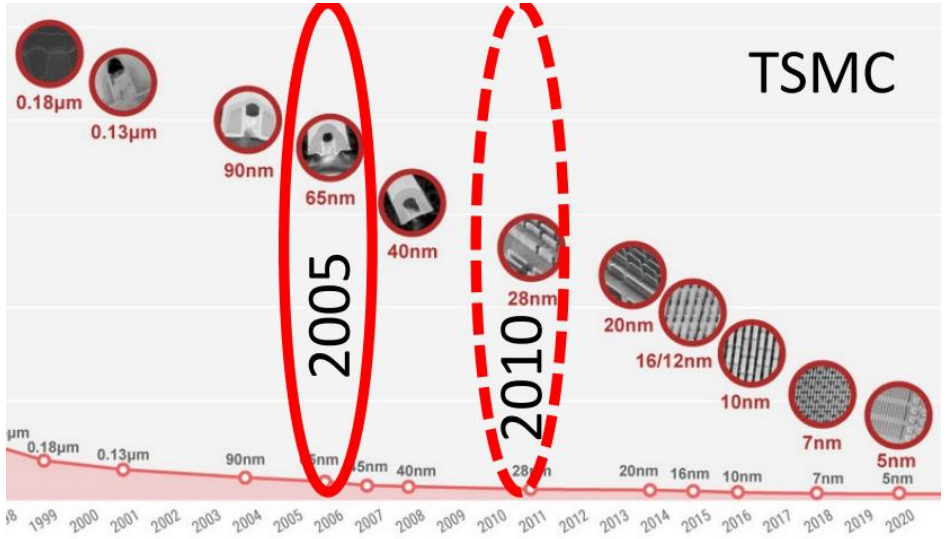
ECFA Detector R&D roadmap [CERN CDS]

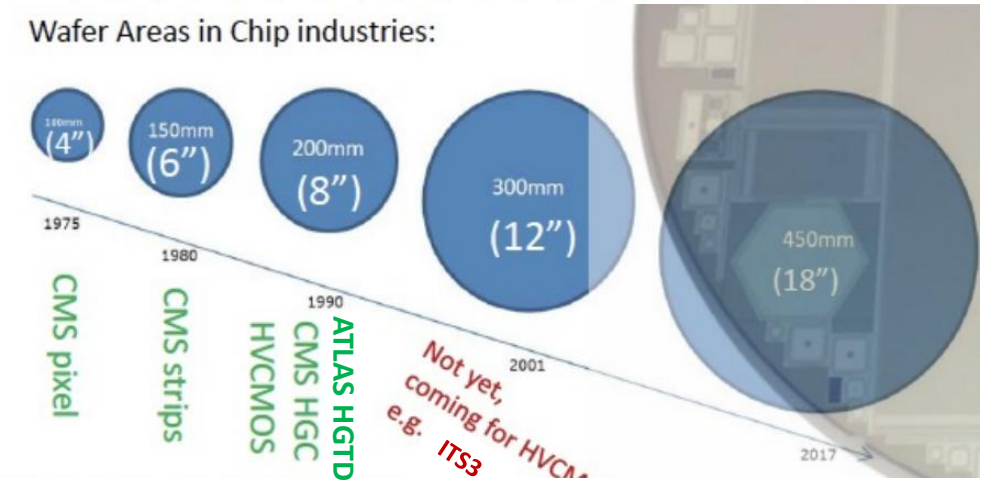


Evolution of Si particle sensors

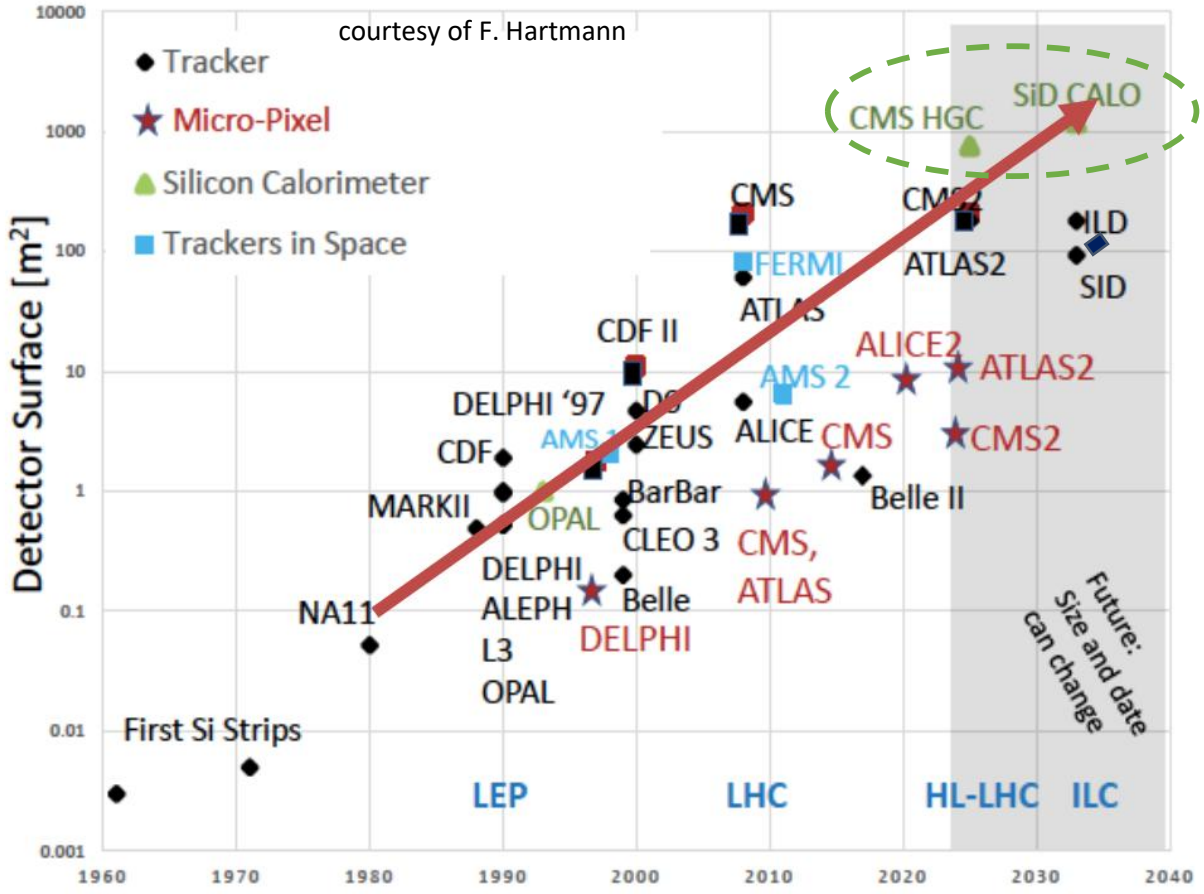
DRD3

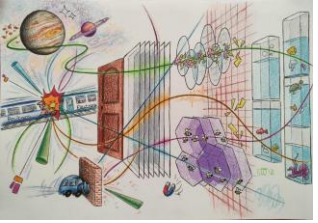
Remarkable advances in electronics. **HEP is still forefront of the mixed/analogue electronics development.**





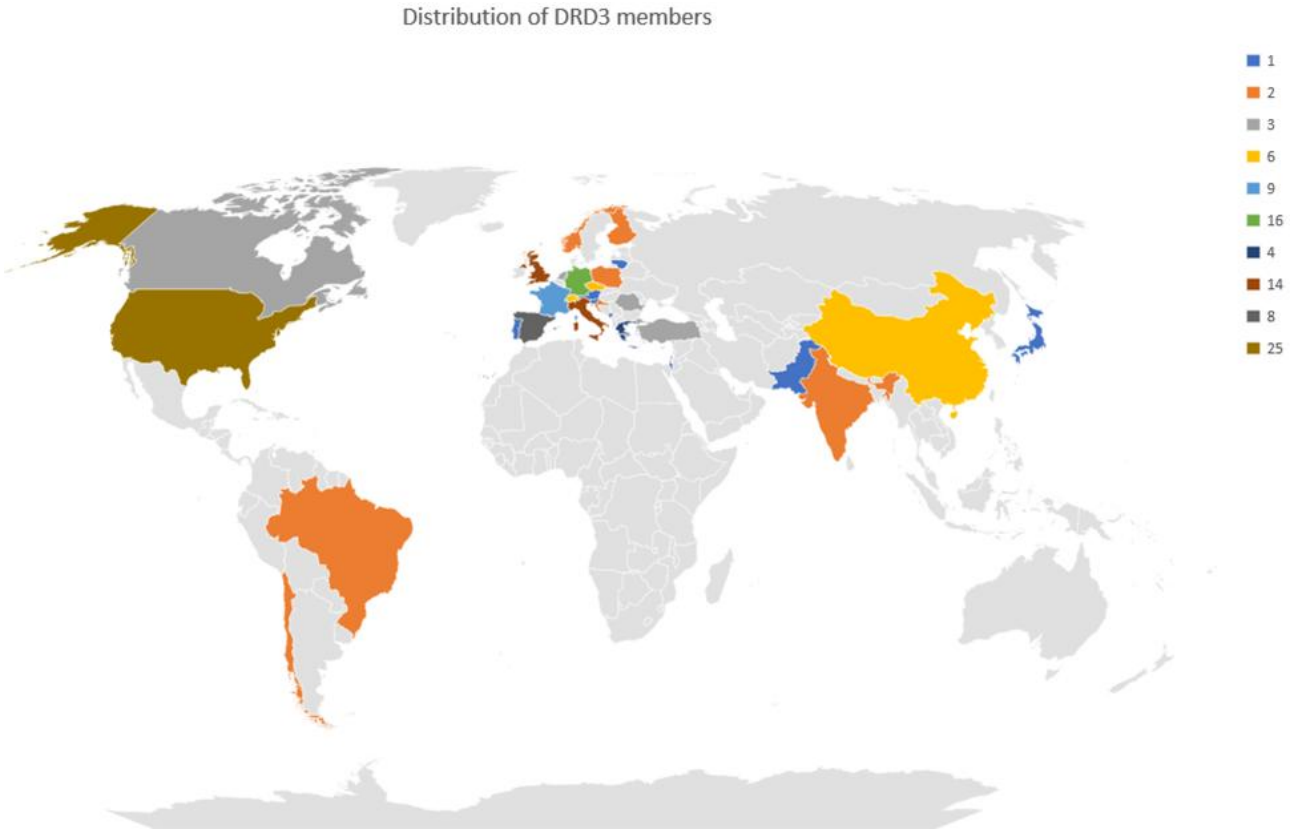
Huge growth of semiconductor particle detectors in various fields **Detector area** increased by one order of magnitude each decade (1 m^2 → 10 m^2 → 200 m^2 → 600m^2)





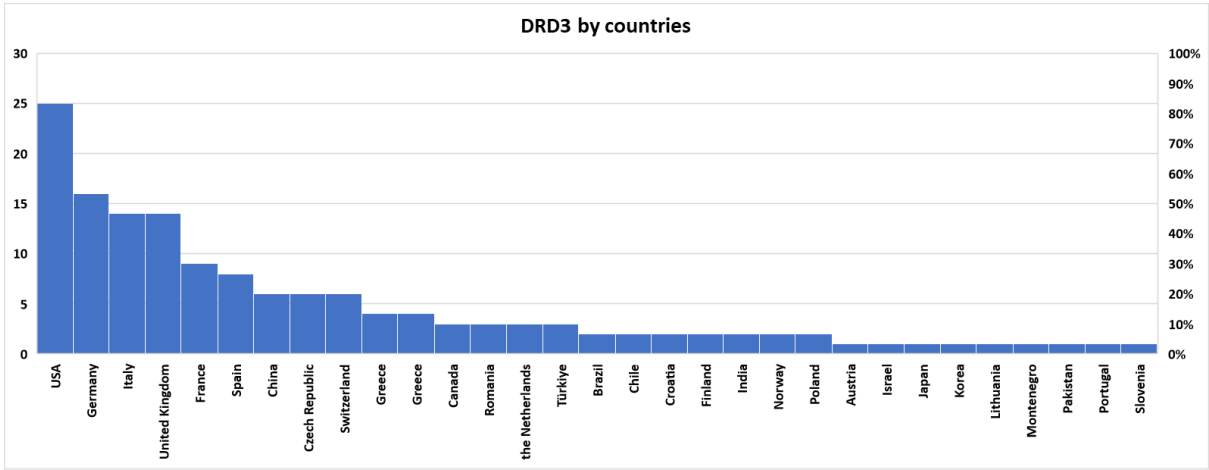
The DRD3 collaboration

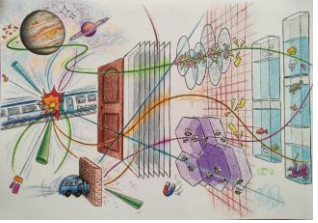
A large collaboration on semiconductor has been formed at CERN to guide and steer the developments of semiconductor sensor developments in the next decades. **148 Institutes currently involved with 700+ people**



Large interests from the community:

- Integration of most **RD39, RD48, RD50** groups
- Integration of the **RD42** groups
- Larger number of institutions from outside

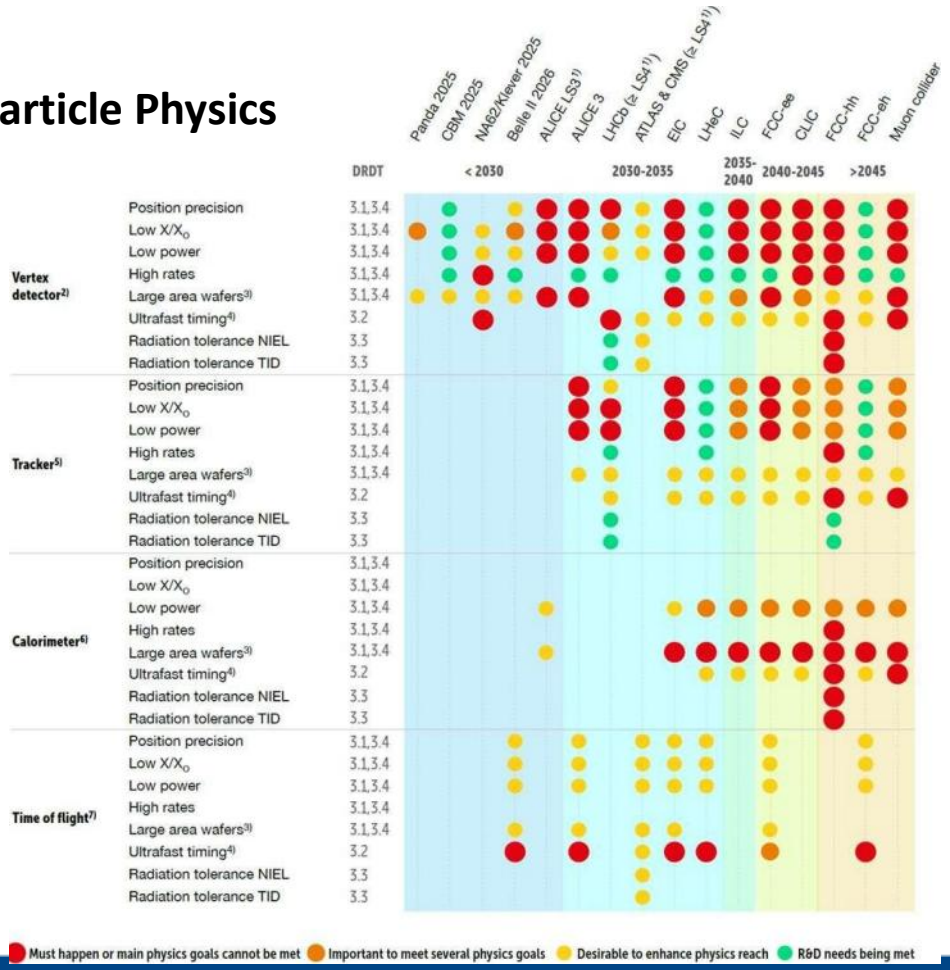


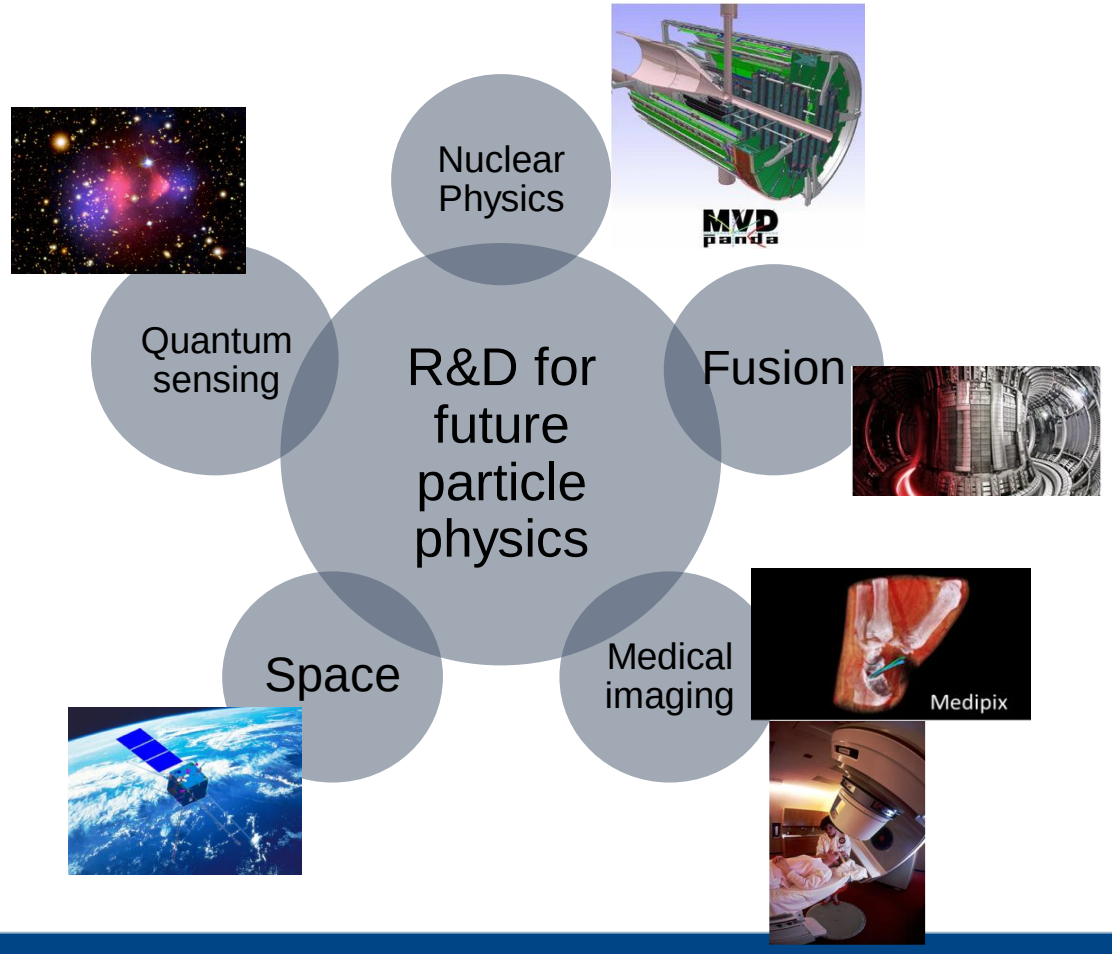


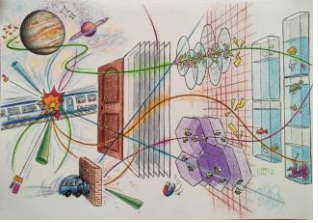
Objectives of the collaboration

The DRD3 collaboration has the dual purpose of pursuing the realization of the **strategic developments** outlined in the ECFA road map and **promoting blue-sky R&D** in the field of solid-state detectors including the synergies with other fields of science where charged particle detection is a key ingredient.

Particle Physics







Organizational structure

June 2025

Collaboration board
CB Chair: G. Pellegrini (CNM)
Deputy: R. Arcidiacono (INFN-TO)

DRD3 management
G. Kramberger (JSI) - SP
M. Moll (CERN)-DSP
I. Gregor (DESY)-DSP
S. Seidel (UNM)-DSP

Steering committee:
DRD3 management + CB Chair + WG conveners

DRD3 bodies
- Secretariat/administration
- Resource coordinator /Budget Holder (D. Muensterman, HRM/Lancaster)
- Cross-DRD coordination
  CPAD coordination
- Speakers committee (U. Parzefall - Freiburg)

R&D activities

WG 1	WG 2	WG 3	WG 4	WG 5	WG 6	WG7	WG 8
Convener(s)	Convener(s)	Convener(s)	Convener(s)	Convener(s)	Convener(s)	Convener(s)	Convener(s)
Monolithic silicon technologies	Hybrid silicon technologies	Radiation damage & extreme fluences	Simulations	Characterization techniques and facilities	Wide band-gap and innovative sensor materials	Interconnections and device fabrication	Dissemination & outreach
H. Pernegger (CERN) E. Vilella (Liverpool) J. Baudot (Strasbourg)	A. Macchiolo (UZH) M.v.Beuzekom (NIKHEF) A. Tricoli (BNL)	Ioana Pintilie (NIMP) J. Schwandt (Uni. HH)	H. Wennloef (NIKHEF) M. Mandurrino (INFN-TO)	I. Vila (IFCA) B. Hiti (JSI)	A. Oh (Manchester) X. Shi (IHEP),T. Yang (LBNL)	G. Calderini (LPNHE) D. Dannheim (CERN) F. Huegging (Bonn)	C. Nellist (NIKHEF) U. Parzefall (ex-officio)

WP1	WP2	WP3	WP4
Leader(s)	Leader(s)	Leader(s)	Leader(s)
Monolithic CMOS sensors	Sensors for 4D-tracking	Sensors for extreme fluences	3D-integration& Interconnections

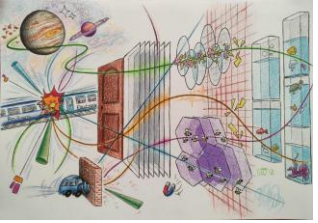
Strategic/Targeted R&D projects

WG conveners serve also as leaders of the matching WPs.

12-2023 - provisional approval
01-2024 - formation of CB
03-2024 - election of SP
05-2024 - formation of WG-WPs
06-2024 - **approval (scientific proposal)**
06-2024 - first DRD3 week
07-2024 - start of scientific meetings and preparation of WP projects
10-2024 - **approval of the DRD3 rules**
12-2024 - second DRD3 week
01-2025 - finalization of WP projects (adjustment to funding reality)
02-2025 - first DRDC review
06-2025 - third DRD3 week approval of the first WP projects
11-2025 - fourth DRD3 week
- finalization of MoU

- **Working Group (WG) = long term R&D activity (strategic or generic) linked to certain technology/purpose/application/method aiming to fulfil the research goals in scientific proposal**
- **Work Package (WP) = strategic R&D activity and is linked to DRD Tasks. It should pursue the goals listed there.**

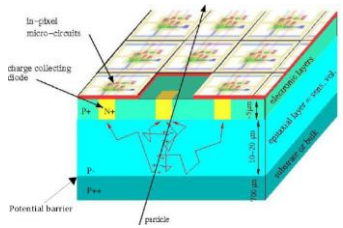
Each work package consist of several WP projects - not yet **fully** resource loaded at the moment.

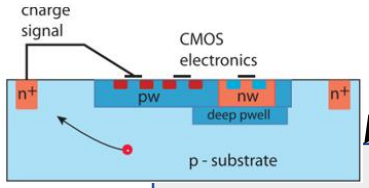


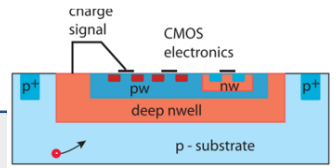
Paths of present silicon sensor R&D

DRD3

Monolithic devices
(WG1/WP1-CMOS)
55-180 nm processes







MAPS

Small electrode device

Large electrode device

with gain

Depleted MAPS wo Gain

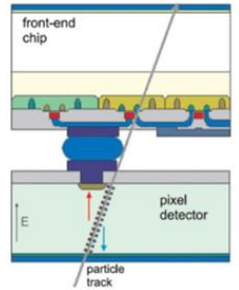
Depleted MAPS wo Gain

with gain

Optimized for rates/power/position resolution

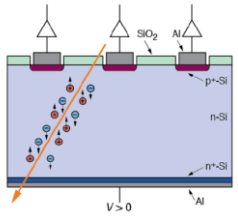
Optimized for radiation hardness /timing

Hybrid devices
(WG2/WP2-4D tracking)



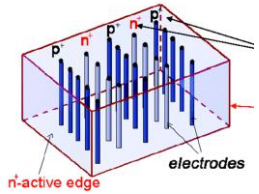
Readout ASIC chip

The sensor



Planar

3D devices



Large area passive devices (strips)

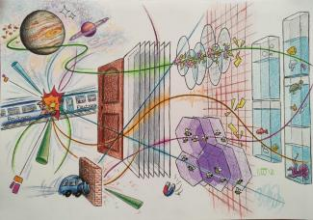
With Gain (LGADs)

Trench 3D

Column 3D

With Gain

proof of concept ongoing
recent research (working prototype)
proven/demonstrated

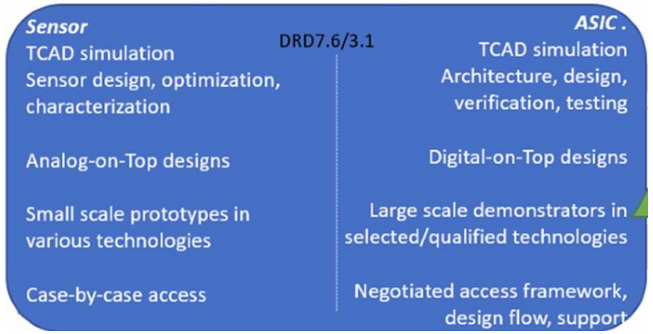


WG1/WP1 Monolithic silicon sensors

Aim is to advance the performance of monolithic CMOS, combining sensing and readout elements, for future tracking applications, tackling the challenges of:

- very high spatial resolution (≤3 µm)
- high data rate (~100 MHz/cm2)
- high radiation tolerance (10^{16} n_{eq}/cm^2 NIEL and 500 Mrad)
- low mass (~0.05% X_0)
- Good timing (->20 ps/hit)
- covering large areas
- reducing power (few tens mW/cm^2)
- keeping an affordable cost

Program shared between DRD3/7

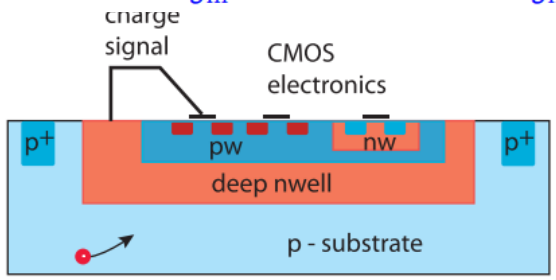


TWO approaches

taken from N. Wermes

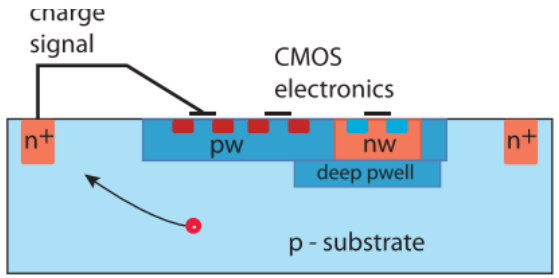
LARGE ELECTRODE DESIGN

$\tau \propto \frac{C}{g_m}$, $ENC_{thermal} \propto \frac{kTC}{g_m}$ compensated by power (g_m)

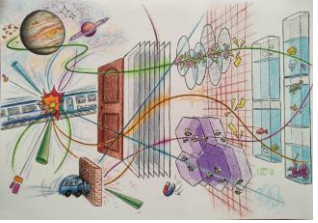


- Large electrode: $C \approx 300$ fF
- Strong drift field, short drift paths, large depletion depth
- Higher power, slower
- Threshold ~ 2000 e^-

SMALL ELECTRODE DESIGN



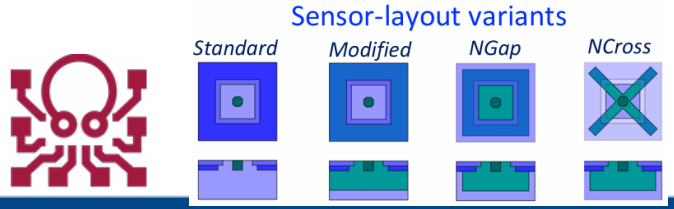
- Small electrode: $C \approx 3$ fF
- Low analogue power
- Faster at given power
- Difficult lateral depletion, process modifications for radiation hardness
- Threshold ~ 300 e^-



WG1/WP1 Monolithic silicon sensors

Projects **running**, **proposal draft submitted (work ongoing)**, **proposals in preparation (work ongoing)**:

- 55 nm SMIC
  - Development of HVCMOS sensors using 55nm process - COFFEE
- 65 nm TPSCo technology (in co. with DRD7.6a):
  - OCTOPUS - Optimized CMOS Technology for Precision in Ultra-thin Silicon
  - MANTA - Versatile MAPS
  - TPSCo 65nm MCMOS with high precision timing
- 150 nm LF technology
  - Towards large electrode CMOS sensors with intrinsic amplification for ultimate timing performance
  - Radiation hard HVCMOS detectors
  - Passive large area strip sensors
- 180 nm TJ technology
  - CMOS Active SenSor with Internal Amplification - "CASSIA"
  - Radiation hard read-out architectures

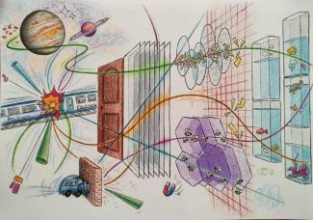


Main challenges (from DRD3 point):

- availability of the active volume (60-80 e-h/μm)
  - epitaxial layer decreases with smaller node processes (350 nm->28 nm). Also, the lateral drift becomes even bigger problem for thin epitaxial layers.
  - few foundries are/will be open to use high resistivity substrate wafer
- costs increase rapidly with the smaller node (MPW runs may not be available)
- allocating the vendors that are open to our needs
  - minimum information about the process-> difficult simulation of particle detection in the devices.
  - adaptation of the process to specific needs
- accessibility to the processes – licensing (access to process development kits - PDK)
- requirements of additional processing (back side processing), back side metallization …

The work is ongoing in all of the projects:

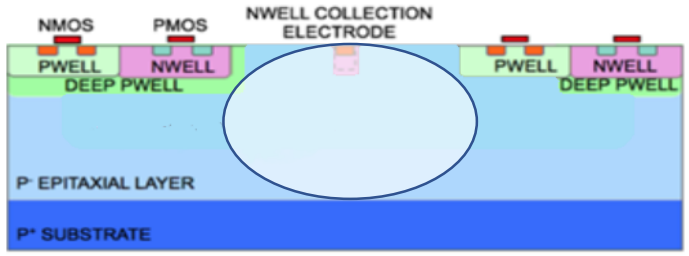
- Resources are at least partially secured
- TPSCo 65 nm (organization together with DRD7/ESE in 2026/27)
- LF15 run is coming in 2026 with resources secured (RD50 legacy)
- TJ180 MPW runs



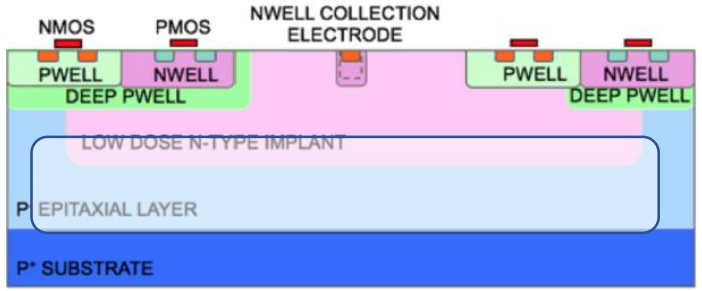
An example of advances in the design MALTA (Tower Jazz 180 nm process)

https://indico.cern.ch/event/1402825/contributions/6002315/attachments/2878704/5043098/MALTA_240617_DRD3_v5.pdf

W. Snoeys et al., Nucl. Instrum. Meth. A 871 (2017) 90.
H. Pernegger et al 2023 JINST 18 P09018

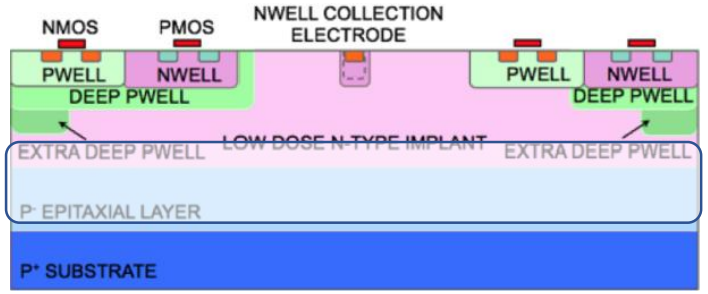


Standard (few V)



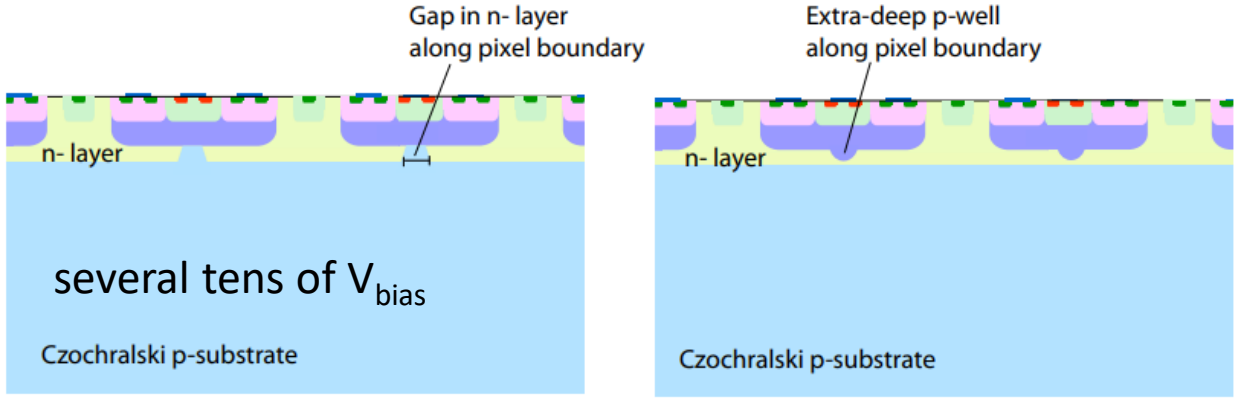
Modified implant (lateral collection)

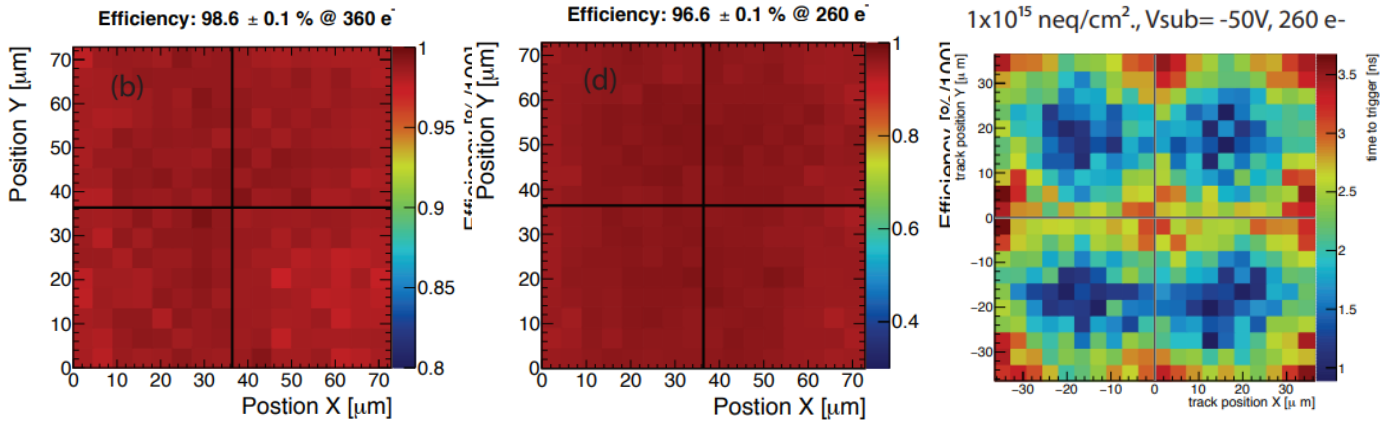
Figure 1. Improved pixel design with n-gap [8]



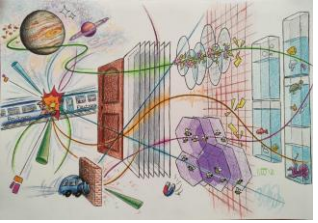
Modified implant – additional notch

MALTA-Cz – high resistivity substrate





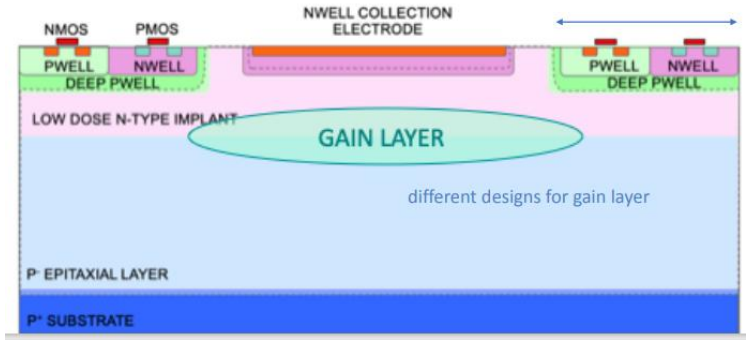
- good efficiency over the pixels even after 3e15 cm^{-2}
- ToA distribution shows differences in signal speed ~2 ns resolution



Future advances – CMOS with gain

- CMOS sensor with gain – can the process be modified in the way that you create an internal gain structure
  - **faster rise time and better S/N - better timing**
  - **better position resolution**
  - **less power consumption**
- Examples of different approaches to reach gain layer multiplication (small electrode design seems more suitable)

Cassia (DRD3 WP1 project)

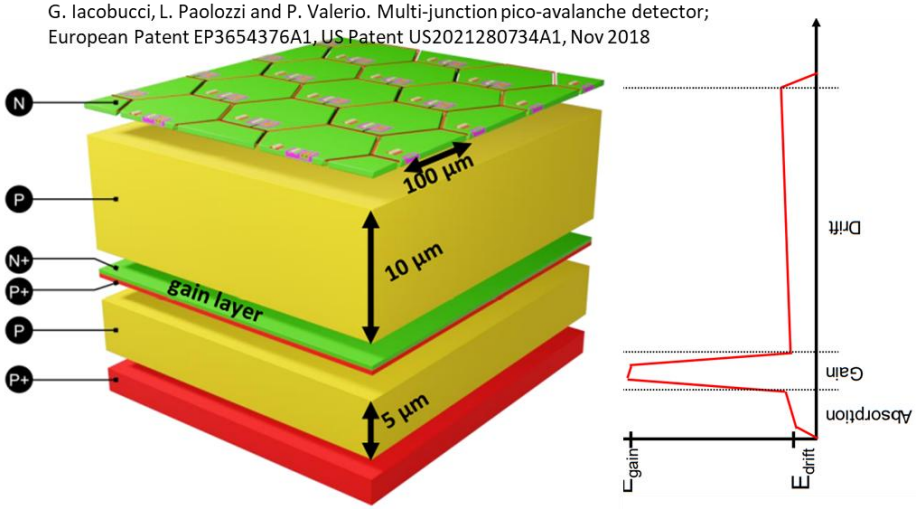


"deep junction" gain layer design

- TJ180 conventional LGAD

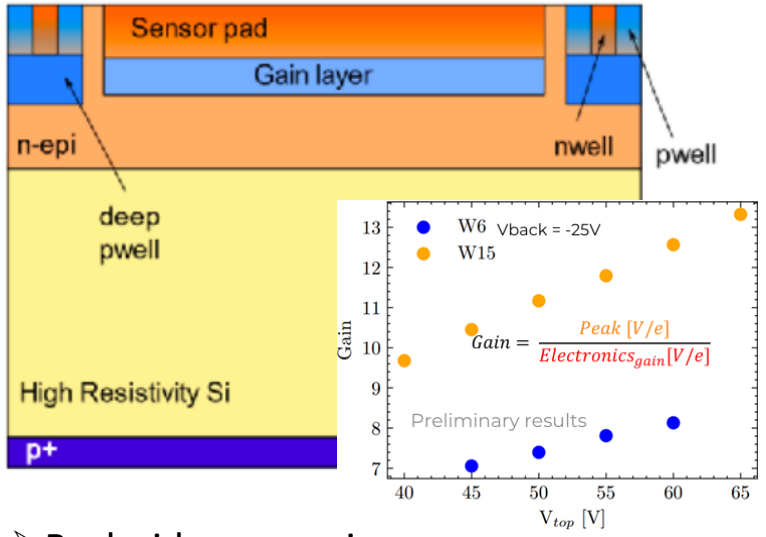
PicoAdd SiGe130 nm IHP (Uni-Geneve)

G. Iacobucci, L. Paolozzi and P. Valerio. Multi-junction pico-avalanche detector; European Patent EP3654376A1, US Patent US2021280734A1, Nov 2018

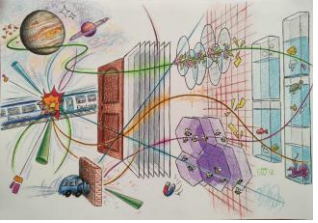


- SiGe bipolar amplifiers – fast (good timing)
- CMOS for digital electronics (monolithic)
- Gain-layer removed from the surface allowing very good spatial resolution without dead area

ARCADIA LF110 nm (DRD 3.1/7.6 – INFN-TO)

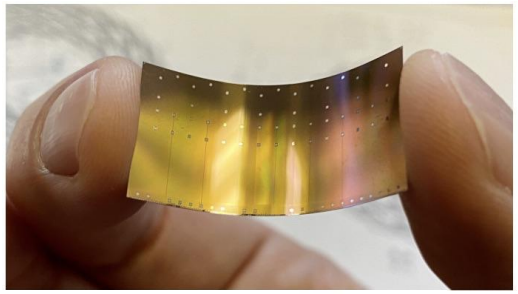


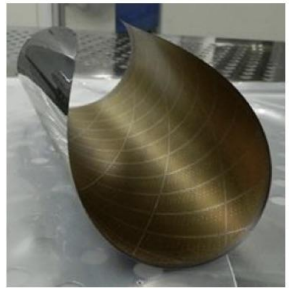
- Back side processing
- High-field grows from the back side – high drift field at the back.
- First results Gain 7-13 – more soon!

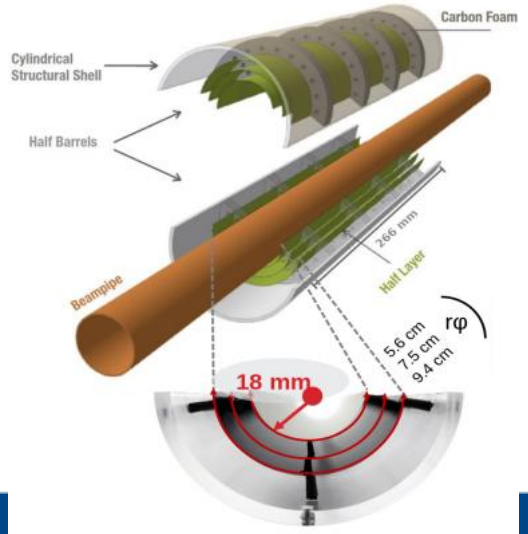


Future advances – scaling up

- Chip-Chip transmission and serial powering
- Stacking up the wafers – better electronics
- **Large-scale reticle stitching of thinned foldable MAPS**

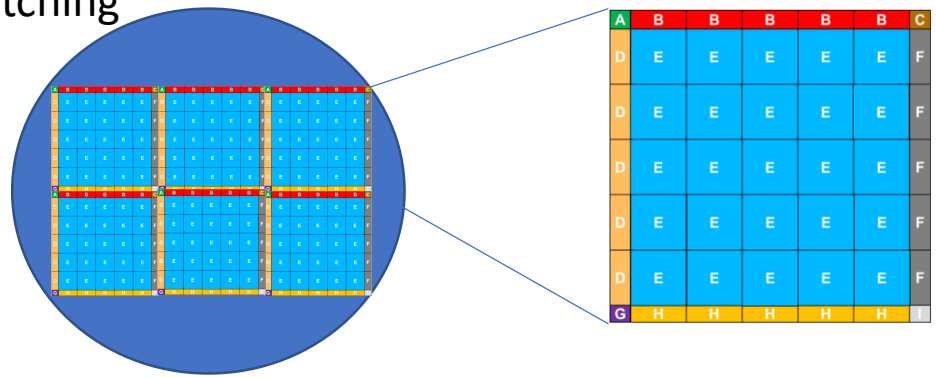






Most notable
ITS3
CEPC, FCC-ee

Stitching

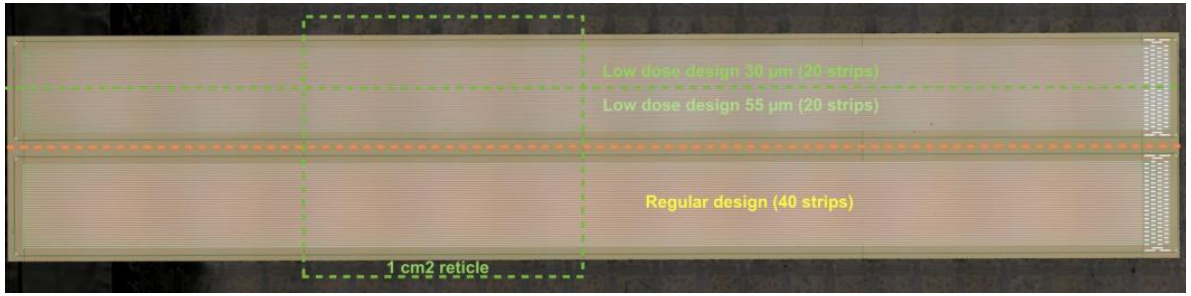


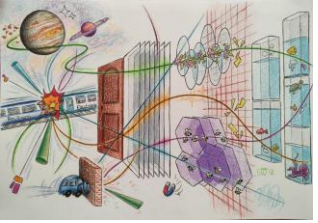
Large area strip/macro pixel sensors

- Reduced material budget
- Easier integration
- Potentially low cost and availability

Monolithic CMOS Strip Sensors for large area detectors (Dortmund, Freiburg, DESY, Bonn)
LFA150 nm - Resistivity of wafer: >2000 Ω·cm

Next step is implementation of the FEI4 like readout per strip



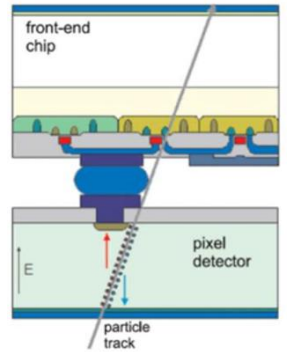


WG2/WP2: Hybrid silicon technologies and 4D tracking

DRD3

By “4D tracking” we mean the process of assigning a space and a time coordinate to a hit - ~10-30 μm position **and ~10-30 ps time resolution** – simultaneously (many benefits in dense particle environment for tracking and PID)

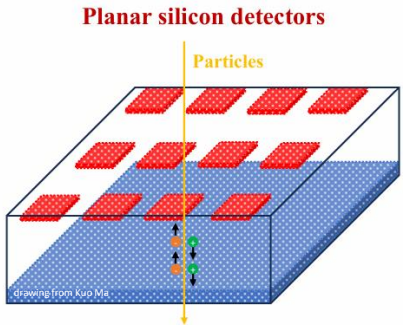
The above goals can be achieved in planar technology with gain (LGADs) or 3D detectors (key requirement - high signal and short collection time)



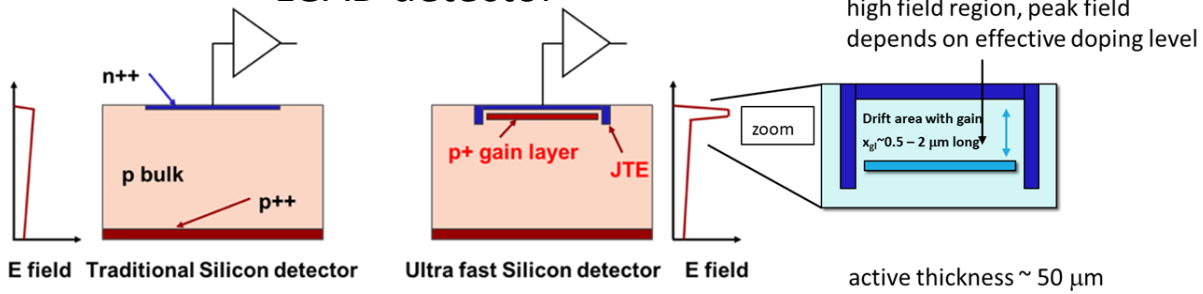
HYBRID

Readout ASIC chip

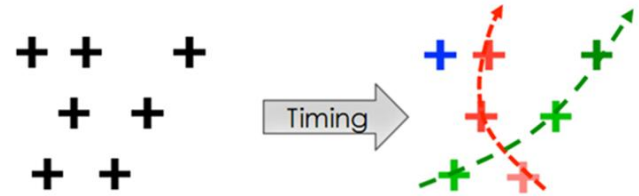
The sensor

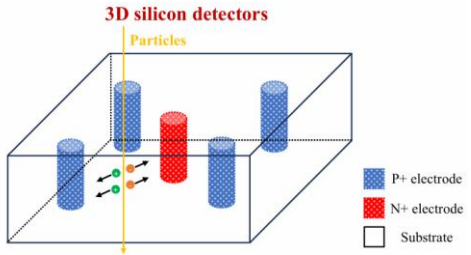


LGAD detector

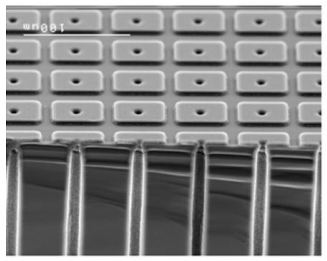


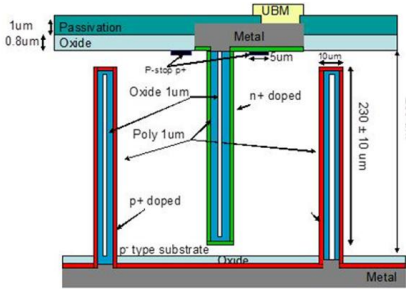
4D tracking (not only track timing)



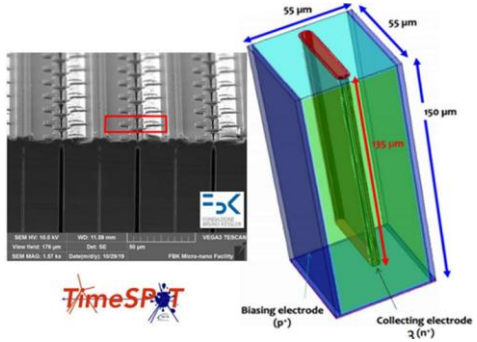


Column-3D detectors

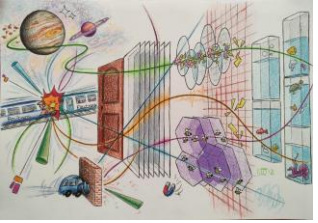




Trench-3D detectors



WG2 research goals <2027	
	Description
RG 2.1	Reduction of pixel cell size for 3D sensors
RG 2.2	3D sensors for timing (50 × 50 μm, < 50 ps)
RG 2.3	LGAD for 4D tracking < 10 μm, < 30 ps, wafer 6” and 8”
RG 2.4	RSD for ToF (Large area, < 30 μm, < 30 ps)



WG2/WP2: Hybrid silicon technologies and 4D tracking

Projects **running** (resources at least partially secured), several WP projects and CCF in preparation

LGAD projects

- LGAD based timing tracker development for future electron collider
- Development of Ultra Fast-Time Low Mass Tracking Detectors
- Development of TI-LGADs for 4D Tracking

- 3D projects
  - Development of very small pitch, ultra rad- hard 3D sensors for tracking & timing applications at FBK
  - Novel silicon 3D-trench pixel detectors based on 8-inch CMOS

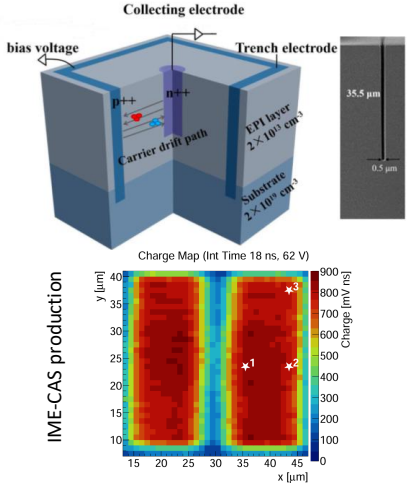
Main challenges and developments:

3D detectors:

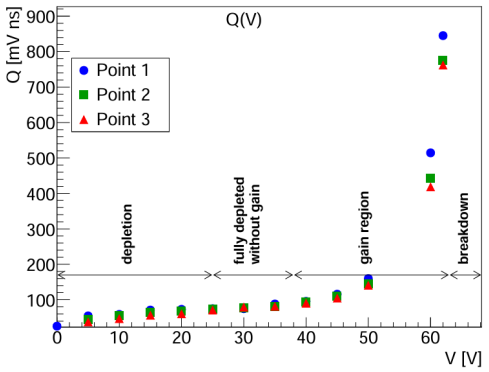
- increase of column-width/depth->100 – narrower columns/trenches (~0.5-1 μm) that would allow for controlled **multiplication/gain device** (**recently achieved within WP2 project**)
- Scalability to 8” wafers **(ongoing)**
- Reduction of cell sizes to 25x25 μm^2 and thickness with gain leading to smaller capacitance **(ongoing)**
- Optimization of geometry for best timing performance

LGADs:

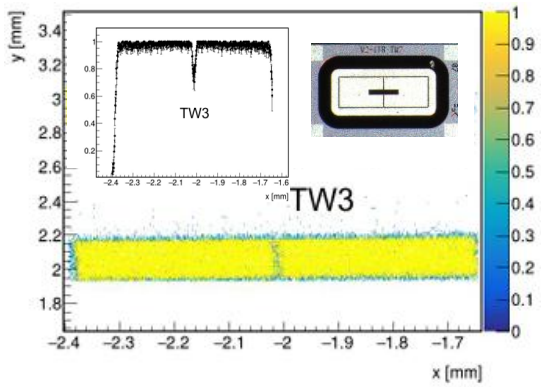
- Solution to fill factor problem – 100% surface efficiency. Addressed in several WP2 projects: TI-LGADs, RSD (AC/DC) LGADs
- Addressing the radiation hardness – defect engineering
  - Co-implantation of impurities (Carbon) – addressed in WG3
  - Compensated LGADs – addressed in WG3

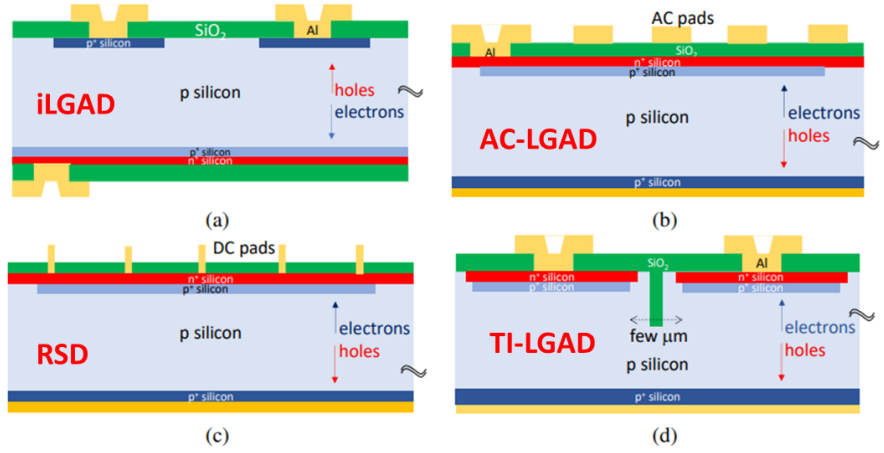


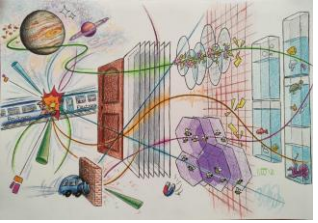
3D-detectors with GAIN



TI-LGAD







WG3,6/WP3 extreme fluence and WBS

Improve the radiation hardness of the semiconductor detectors and exploitation of the benefits of WGS for particle physics

Projects **running**, **proposal draft submitted (work ongoing)**, **proposals in preparation (work ongoing):**

- Understanding silicon at extreme fluences (**devices developed with in WP2**)
  - Radiation damage in Si PiN and LGAD sensors
  - Many RD50 projects running on the radiation hardness
- Wide-Bandgap-Semiconductors
  - SiC LGAD Detector (one running one in preparation)
  - Development of radiation-hard GaN devices for MIP detection
  - Radiation hardness of 25 µm 3D diamond detectors
  - Graphene/SiC Detector

Main challenges and developments:

Silicon at extreme fluences:

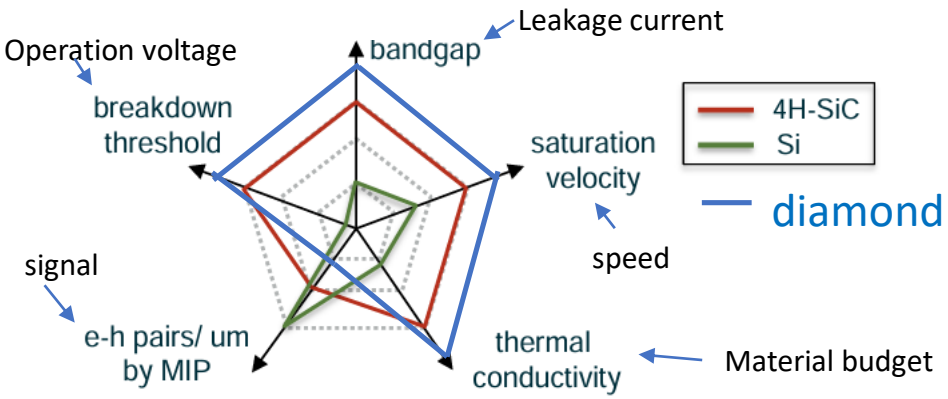
- understanding material properties (impact ionization, mobility, trapping…)
- understanding the operation

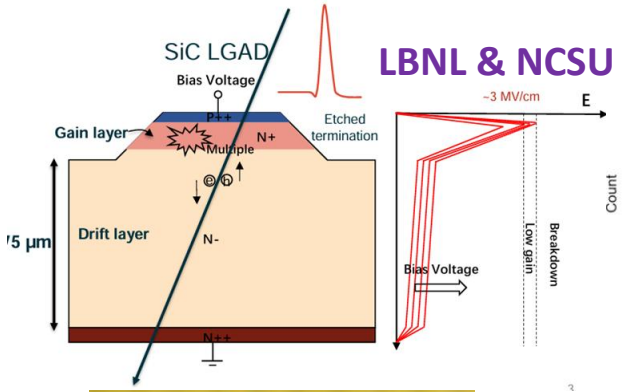
SiC/GaN

- understanding the material properties – defects formation
- processing of large device SiC-LGADs

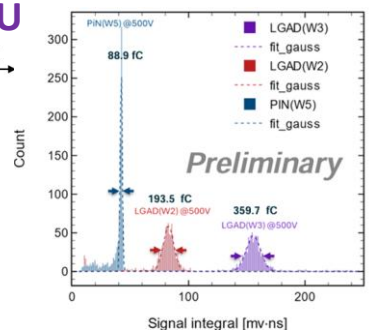
Diamond:

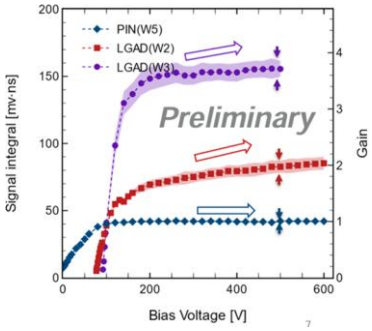
- scalability of 3D column processing
- availability of high quality large diameter wafers

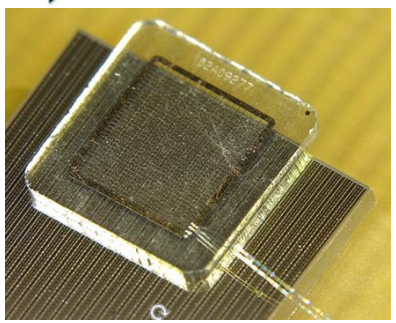


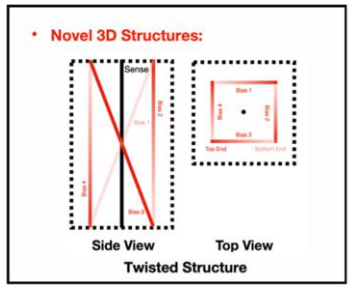


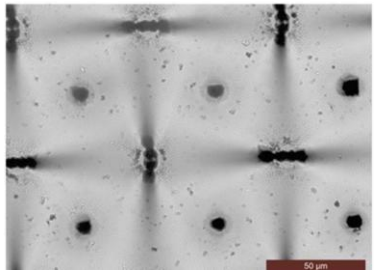
LBNL & NCSU

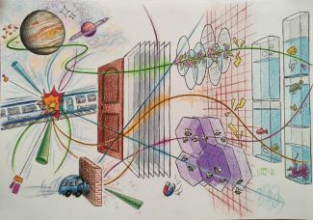






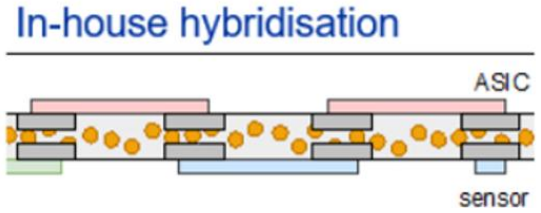






WP4: 3D-integration and interconnections

The goal of the DRD3 interconnection task is to organize the different technological readiness levels of interconnection solutions and the effort towards future advances in the field to match the requirements of future detectors in a coherent and coordinated way.



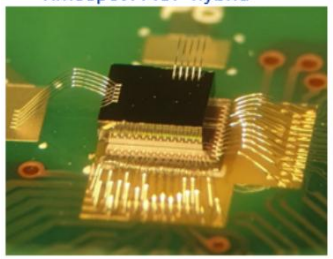
Projects **running**

- In-house plating, hybridization and module-integration technologies for pixel detectors

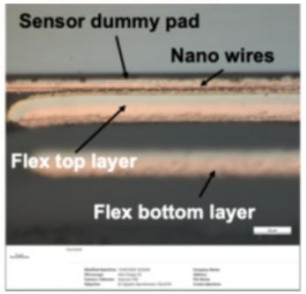
CCF project:

- CMOS Pixel Detector Demonstrator with Serial Powering and Innovative Interconnections

Timespot1 ACF hybrid



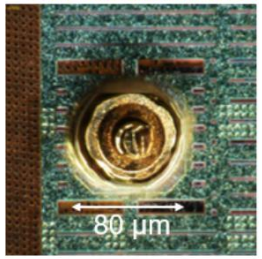
Nanowires on flex



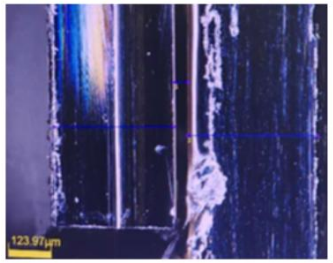
In-house hybridization, module integration

- Exploring innovative **bonding** methods, adapted to the requirements of various projects
  - **Conductive adhesives (ACF / ACP)**
    → good results for <1cm^2 devices and >~50 µm pitch
  - **Nano wires**
    → successful bonding of MALTA2 to flex
  - **Gold studs** + epoxy
    → successfully used for large (>100 µm) pitch
    → developed **low-temperature bonding process** suitable for **irradiated samples**

Gold-stud on ALTIROCA



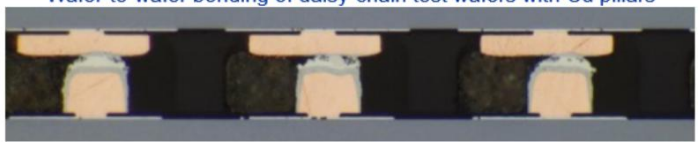
ALTIROCA + irradiated LGAD

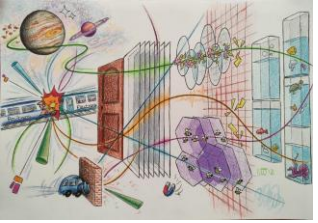


Wafer-to-wafer bonding

- Target: ultra-thin hybrid detectors with TSV
- Pilot project U Bonn / IZM: passive CMOS sensors + Timepix3

Wafer-to-wafer bonding of daisy-chain test wafers with Cu pillars





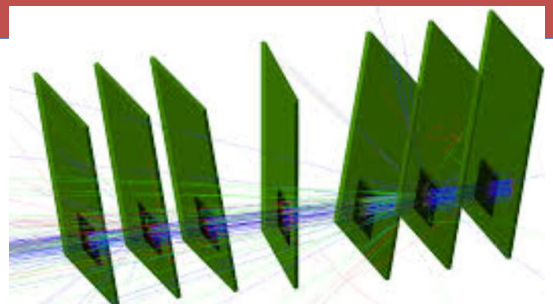
WG 4: Simulations

Simulations are essential for planning, understanding the performance and designing of devices. Aim to develop tools that could be (easily) implemented to simulate any specific detector or measurement.

"Monte Carlo"
(predicting the performance of complex detector assemblies)

AllPix2 / Garfield++ as the main tool complement by other ones (also RASER, KDetSim…)

GOALS:
- Implementation of improved semiconductor models (e.g. mobility, impact ionization, trapping …)
- Adaptation of WBS sensors
- Adaptation of dynamic /adaptive E,E_w
- Implementation of common electronics/digitization



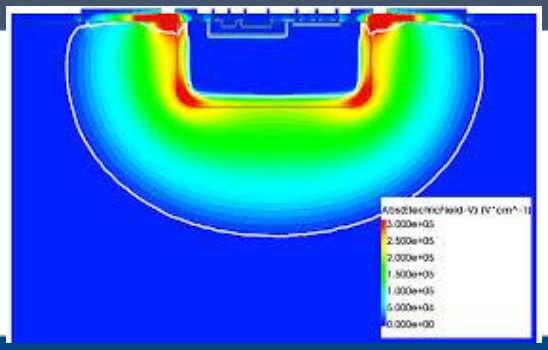
GEANT4

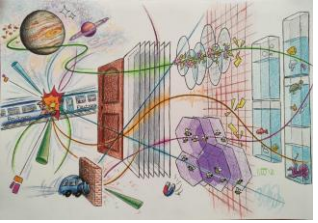
E,E_w

TCAD
(understanding the sensors)

Synopsis, Silvaco …

GOALS:
- Developing and verification of damage models (effective and defect based)
- Establish how to benchmark/evaluate the models against the measured properties (important milestone)
- Improving the TCAD with new findings (WBS, extreme fluences)
- Develop a flexible framework to simulate performance of different processes (CMOS)





WG5: R&D on new techniques, common infrastructures, and characterization facilities

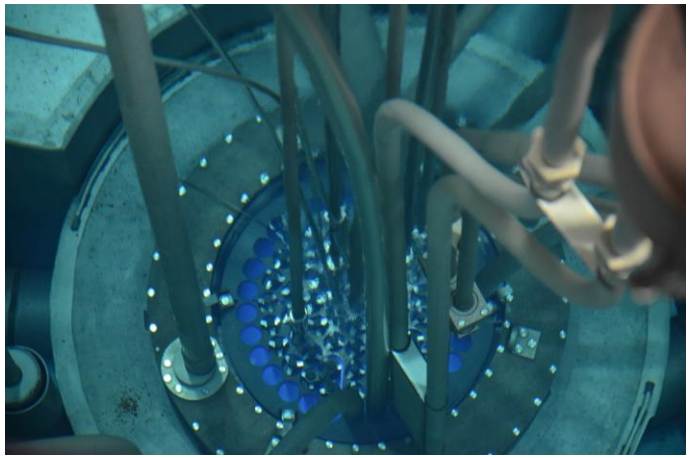
Lines of actions:

- Development/improvement/diffusion of **methods and techniques for characterizing sensors** (those for defects spectroscopy DLTS,TSC, EPR…. as well those for characterization TCT, Beta-scope…)
- Joint research activities for the **delivery of common infrastructures for sensor testing** (common sensor readers, jigs, test fixtures,…)
- Promoting the **use of unique irradiation and characterization facilities.**

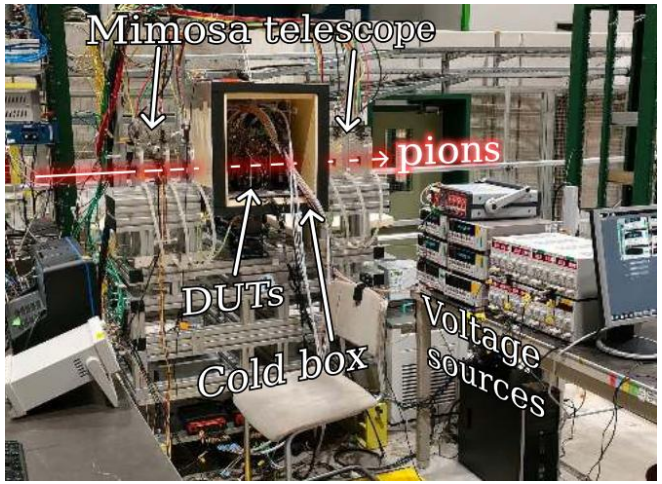
Activities in the last year:

- Centrally organized irradiations to 10^{18} cm^{-2} with reactor neutrons, now also PS and FNAL irradiations
- Organization centrally organized TB campaign (many DRD3 groups benefited)
- Setting up know-how and infrastructure at ELI-beams
- Development new techniques e.g DB-TCT
- …

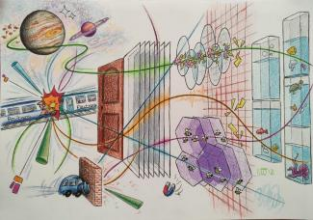
Irradiation facilities (e.g. JSI reactor)



Test beam activities (CERN/DESY)



fs high intensity laser facilities (ELI Prague, SGIKER Bilbao…)



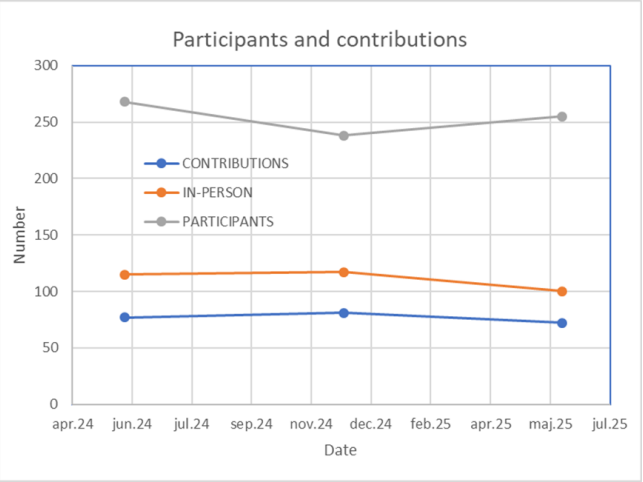
Outreach and visibility

DRD3

We keep all he information in DRD3 www page (drd3.web.cern.ch):

- announcements of interesting events schools/conferences/ workshops
- open positions
- repository of relevant literature and documents
- links to CDS records of proposals and internal documents

DRD3 weeks
our main events
open to everyone

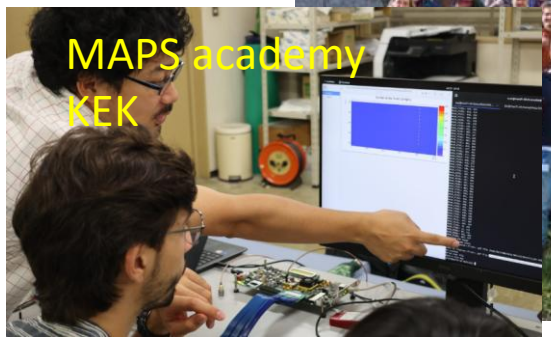


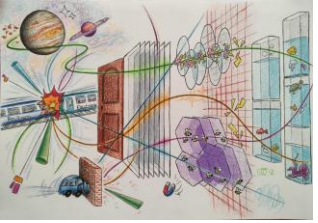
Presentations:

- at student lectures/schools
- several overview presentations at various conferences/workshops

Schools organized within/by DRD3 in last year:

- 1st DRD3 TCT School (March 2025)
- MAPS academy (July 2025)
- 2nd DRD3 TCT School (September 2025)





Conclusions

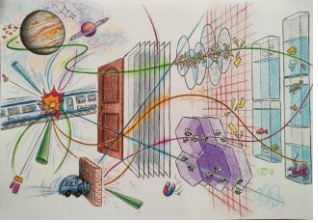
- We are large collaboration still in shaping – many RD39,42,50 groups are part of DRD3 collaboration.
- We have many project running (funded) from RD50 collaboration – so a lot of R&D activities are a continuation of work
- The **strategic funding of the activities (HEP detector R&D) are being shaped in the form of WP projects** – each WP is a framework for dedicated projects
  - all semiconductor technologies are pursuit
  - we welcome new ideas and collaborators
- The collaboration has a common fund from which many smaller R&D projects/schools/common activities (TB, laser, irradiations) will be supported also for synergies with other fields and Blu-Sky R&D
- Many activities are ongoing: 4 DRD3 weeks, DRD3 TCT Schools (two), MAPS academy
- More information can be found on drd3.web.cern.ch

"Far better it is to dare mighty things, to win glorious triumphs, even though checkered by failure, than to take rank with those poor spirits who neither enjoy much nor suffer much, because they live in a gray twilight that knows not victory nor defeat."

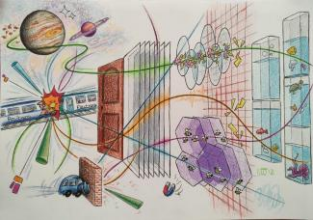
-- Theodore Roosevelt, 1899

…. we dare mighty things …

Thank you!



Backup/additional slides



WG3/WP3: Radiation damage characterization and sensor operation at extreme fluences

DRD3

- WG covers 3 main areas around radiation hardening (see below)
- WG closely related to all other WGs

WG4: Simulations

Need for simulations in all areas

- on the material level
  Geant4, TRIM, NIEL, DFT, KMC, …
- on the device & system level
  TCAD, AP2, Signal & MC simulators, generic sensor parameter simulations (e.g. Hamburg model)
- extrapolation to extreme fluences
  do models still deliver reliable results?

WG5: Characterization techniques

Need for tools in all areas

- on the material level
  EPR, FTIR, PL, DLTS, TSC, …
- on the device & system level
  TCT, CV, IV, IBIC, test-beams, ….
- extrapolation to extreme fluences
  which tools still deliver reliable results?
  radiation facilities,…

WG3: Radiation Hardening

Radiation hardening of material
understand fundamental damage process, defect formation, impact of defects on device performance (also non-silicon!), material and defect engineering

Radiation hardening of devices and systems
understand device operation with radiation damage, device engineering

Extreme fluences
understand physics, possibilities for operation of detectors

WG6: Non-silicon based detectors

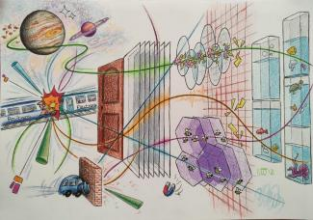
- Material & devices to be studied and understood as silicon in terms of radiation damage in all areas (simulations, material/sensor characterization, tool development)
- Developments for extreme fluence

WG1 & WG2: Silicon based detectors

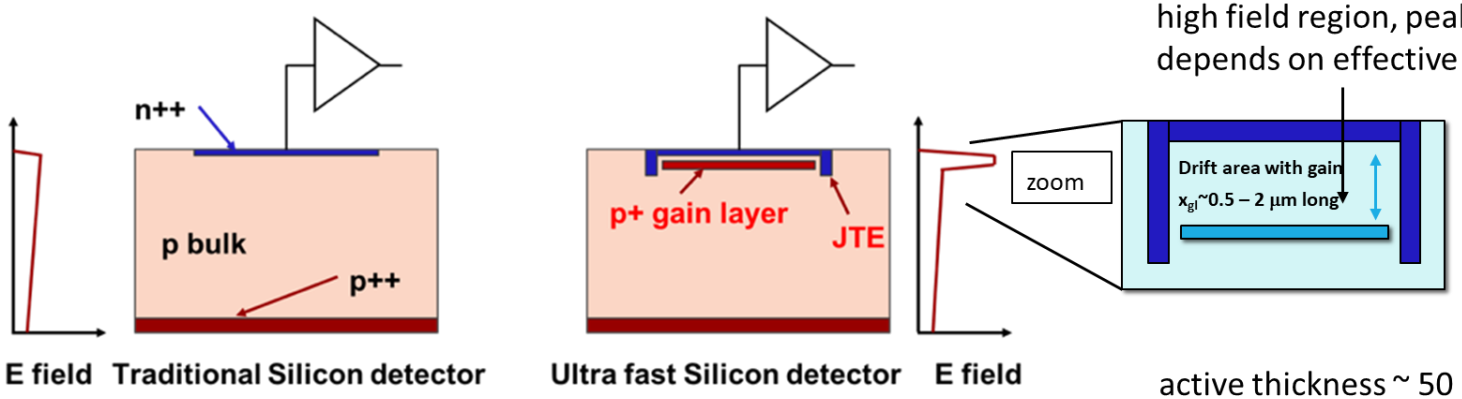
- Radiation hardness evaluation of all sensors with exposure to radiation (existing and newly developed sensors/sensor concepts)
- Developments for extreme fluence

Synergies with other application areas in radiation fields

- Detectors for nuclear physics, space applications, fusion, medical applications, …



WG2/WP2: LGADs



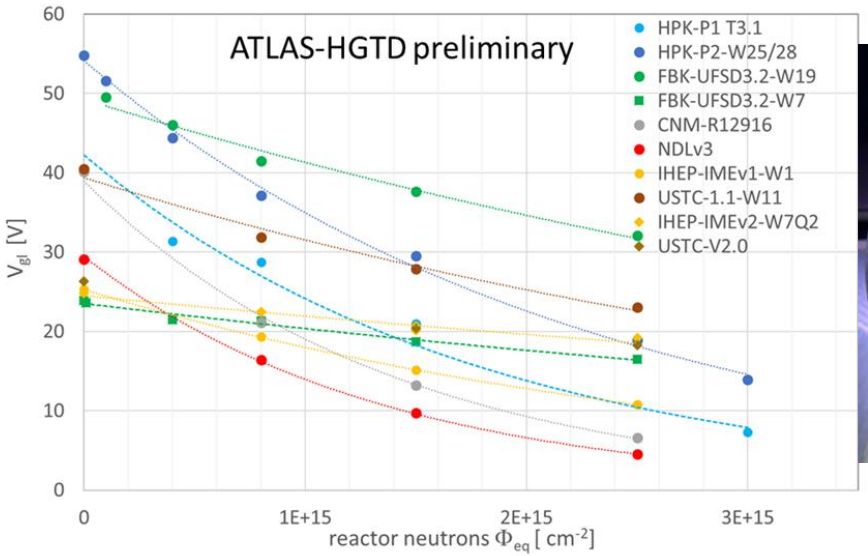
Typically 25-50 µm thick with signals of 20fC (G~40)

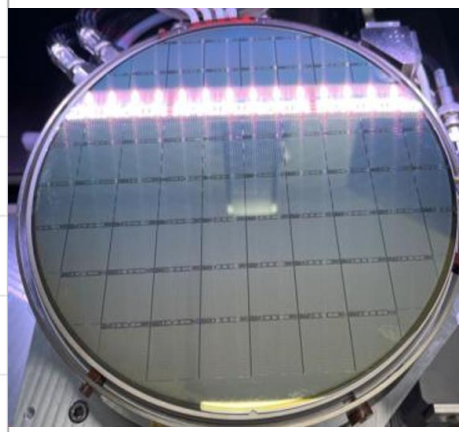
Limitations for conventional LGADs:

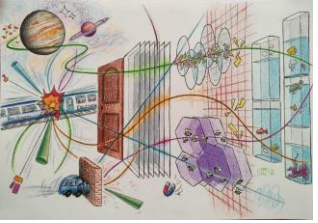
- Fill factor (large cell devices) due to JTE
- Radiation harness – **currently to ~3e15 cm^{-2}**

Radiation hardness:

- C-enrichment of the gain layer (prevention of B removal – reduction of the field) - IME (USTC&IHEP) mastered the C-enrichment and has so far produced most radiation hard sensors for ATLAS-HGTD – is there still room for improvement?
- Compensated LGADs – use of compensated p+ silicon in gain layer which if carefully tuned would not suffer from reduction of negative space charge with irradiation (both P and B are removed)
- Thermal treatment >200°C reactivation of space charge







WG2: LGADs different flavors

Several technologies were proposed and are investigated to overcome fill factor problem:

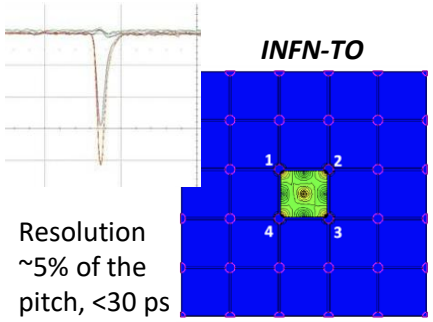
iLGAD – segment the side without multiplication no p-stop, JTE at the bottom (**complex processing, radiation hardness, hole collection**, ideal for high rate)

TI-LGAD – use SiO_2 trenches to isolate the pads, reducing the gap by an order of magnitude (C-enriched produced)

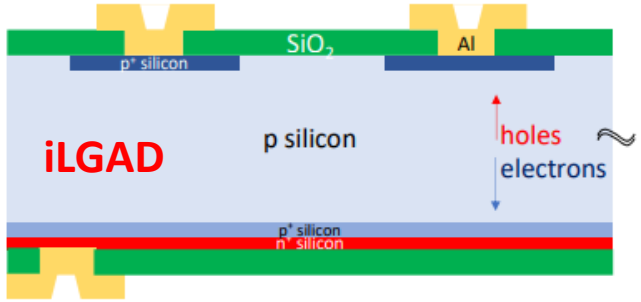
AC-LGAD / RSD– use AC coupling – bipolar signals:

- superb spatial and time resolution (order of magnitude better than pitch)
- **rate limited, radiation hardness**

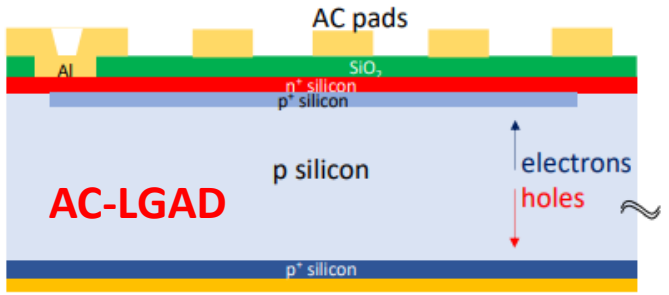
DJ-LGAD



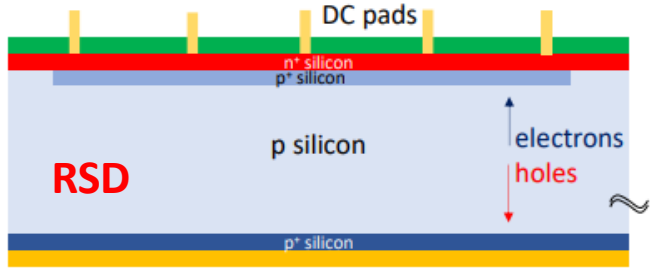
Resolution ~5% of the pitch, <30 ps



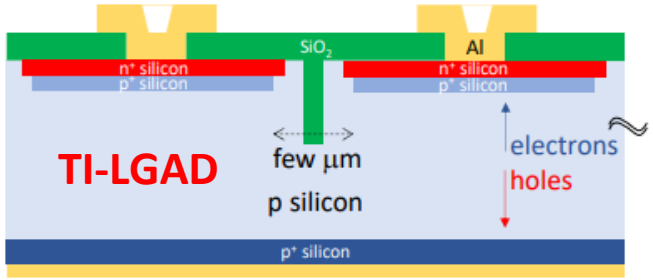
(a)



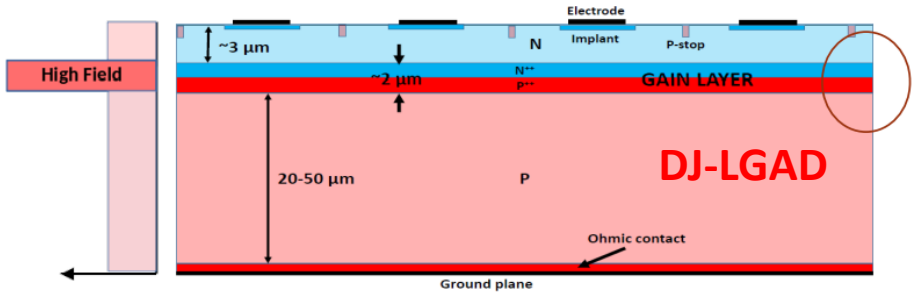
(b)



(c)



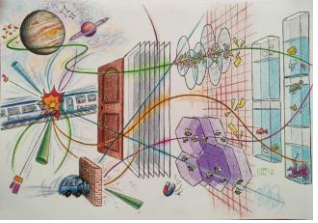
(d)



LGADs are the only planar technology good enough for precise timing (<50ps), but excellent electronics is needed.

marriage of LGAD + CMOS

DJ-LGAD, CASSIA, MONOLITH, ARCADIA…



WG2/WP2: 3D detectors

3D technology as timing detectors:

- They have fill factor ~100% (inclined tracks – ATLAS IBL)
- The radiation tolerance of small cell size (smaller depletion depth, lower bias, smaller power consumption) – operation at the levels of up to ~1e17 cm^{-2} were shown
- Technology is already mature-latest 3D detectors are done in single sided processing – this simplifies to large extent the production

Challenges (most advanced is now IME-CAS):

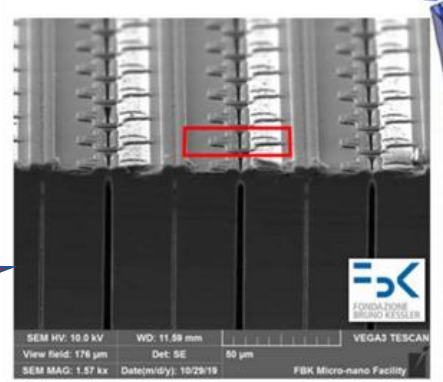
- Performance drawbacks is mainly in larger capacitance (hence noise and the jitter) particularly for thick sensors with large signals and to smaller extent fill factor
- Recent advances in very narrow columns/trenches (100:1 at IME) allow for columns/trenches of <1 μm.
- scalability of the processing to standard CMOS 8” line

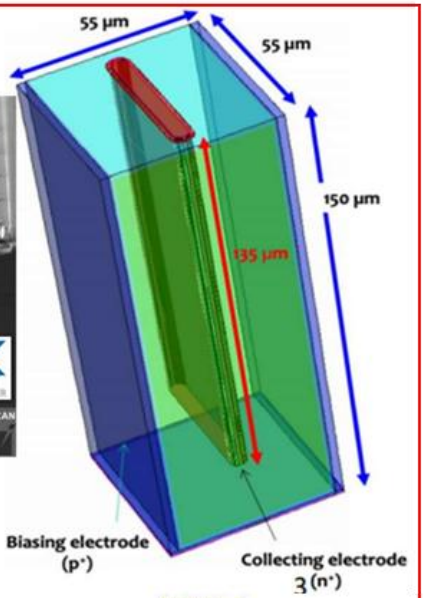
Trench 3D

(INFN – FBK)

3D silicon detectors

<30 ps mips

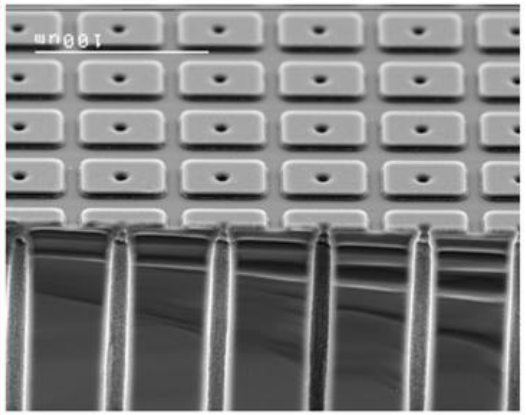


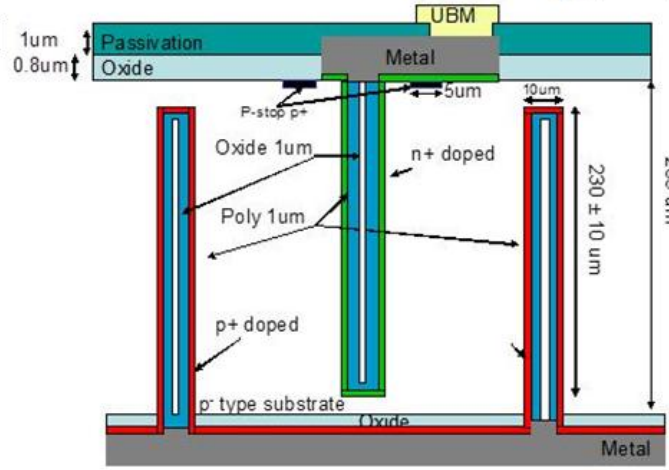


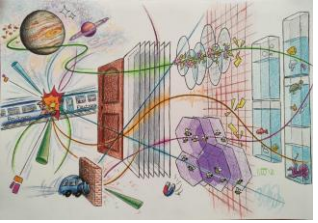
TimeSPOT

Column 3D

(CNM/FBK/Sintef/IME…)







3D with gain (4D tracking in harsh env.)

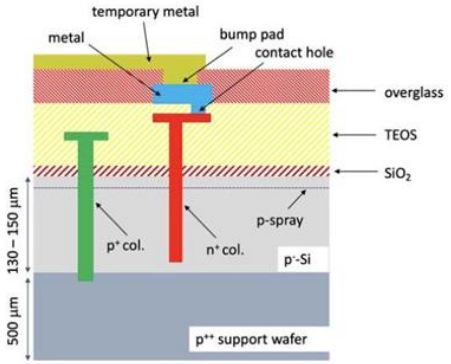
Can we progress from "solid state ionization chamber" to semiconductor "wire proportional chamber"?

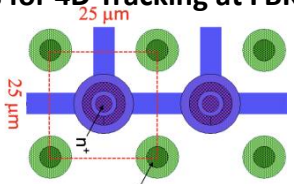
An ideal 4D tracking sensors – thin 3D detector with gain

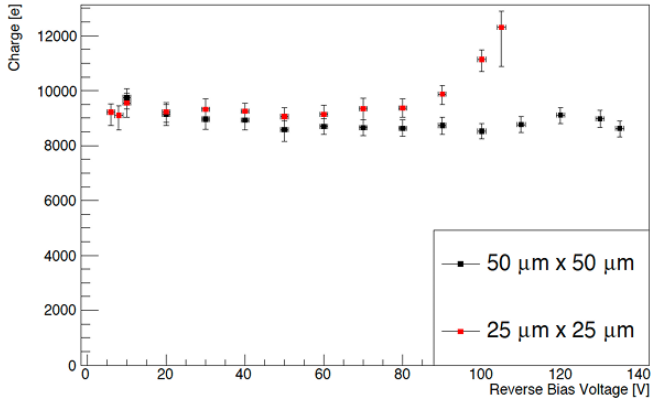
- very radiation hard
- low power consumption (small bias and current)
- low material budget
- very fast

WP2 project : Development of very small pitch ultra rad 3D sensors for 4D Tracking at FBK

3D-sensors with gain (FBK/UNM/INFN)

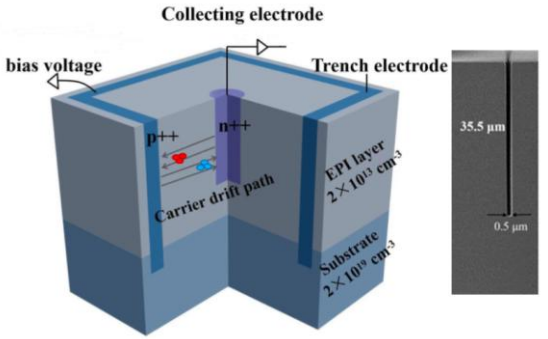




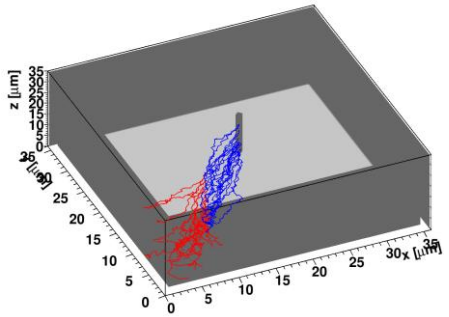


WP2 project : Novel silicon 3D-trench pixel detectors based on 8-inch CMOS process (IME)

Two proton absorption TCT



Simulation of the track



Charge Map (Int Time 18 ns, 62 V)