STCF Detector and Performance

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FTCF2025, Huangshan, China
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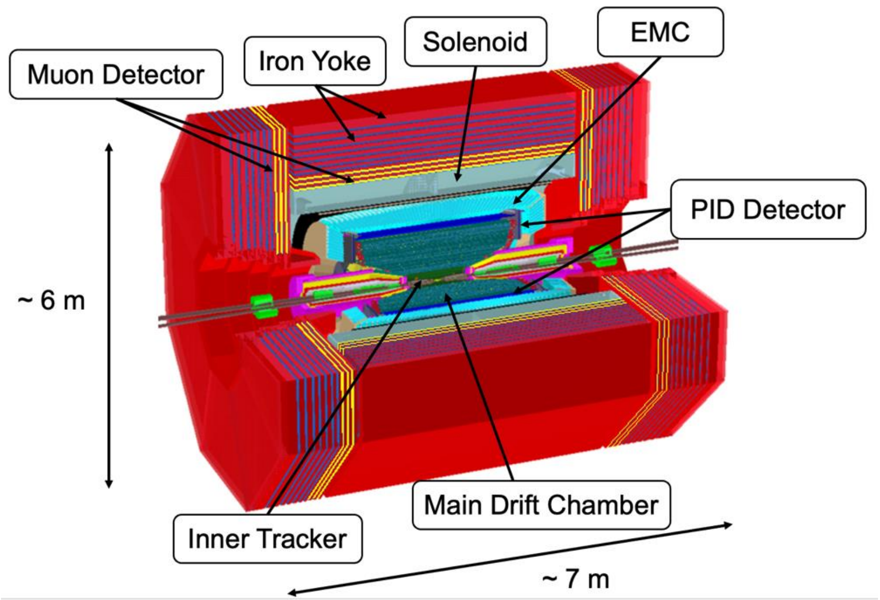
Requirements for STCF Detector

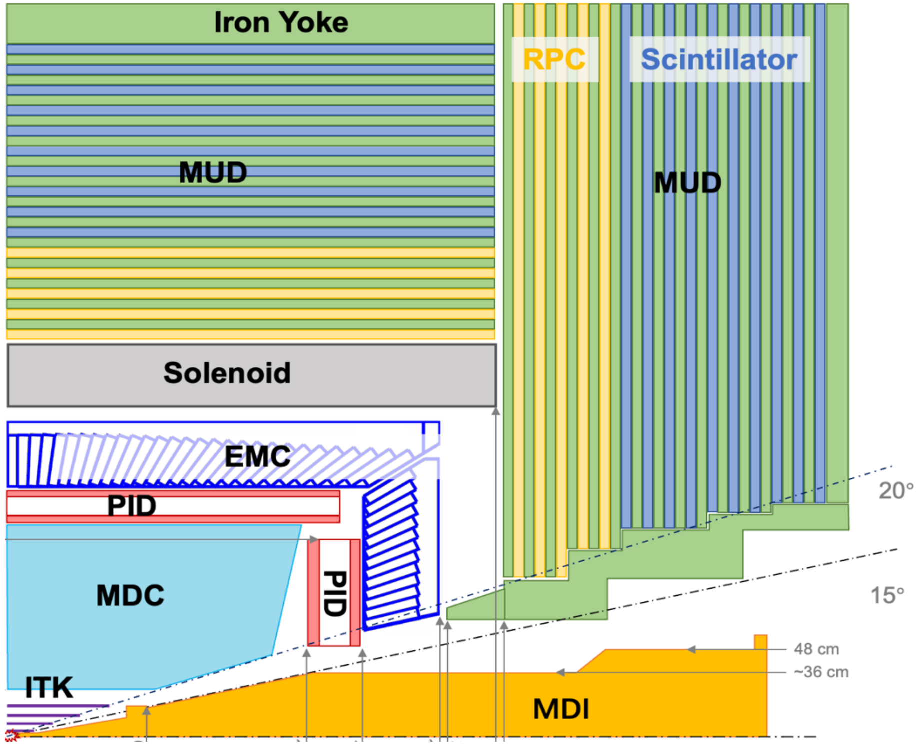
- **Highly efficient and precise reconstruction of exclusive final states produced in 2-7 GeV e^+e^- collisions**
  - High tracking efficiency (>90% @ 0.1 GeV/c) and high momentum resolution for low-p (<1GeV/c) charged particles, precise measurement of low-energy (<1GeV) photons.
    → low mass tracking and PID detectors
  - Excellent PID: π/K and μ/π separation in full momentum range (up to 3.5 GeV)



Process	Physics Interest	Optimized Subdetector	Requirements
$\tau \to K_s\pi\nu_\tau$, $J/\psi \to \Lambda\bar{\Lambda}$, $D_{(s)}$ tag	CPV in the τ sector, CPV in the hyperon sector, Charm physics	ITK+MDC	acceptance: 93% of 4π; trk. effi.: $> 99\%$ at $p_T > 0.3$ GeV/c; $> 90\%$ at $p_T = 0.1$ GeV/c $\sigma_p/p = 0.5\%$, $\sigma_{\gamma\phi} = 130\ \mu$m at 1 GeV/c
$e^+e^- \to KK + X$, $D_{(s)}$ decays	Fragmentation function, CKM matrix, LQCD etc.	PID	π/K and K/π misidentification rate $< 2\%$ PID efficiency of hadrons $> 97\%$ at $p < 2$ GeV/c
$\tau \to \mu\mu\mu$, $\tau \to \gamma\mu$, $D_s \to \mu\nu$	cLFV decay of τ, CKM matrix, LQCD etc.	PID+MUD	μ/π suppression power over 30 at $p < 2$ GeV/c, μ efficiency over 95% at $p = 1$ GeV/c
$\tau \to \gamma\mu$, $\psi(3686) \to \gamma\eta(2S)$	cLFV decay of τ, Charmonium transition	EMC	$\sigma_E/E \approx 2.5\%$ at $E = 1$ GeV $\sigma_{\rm pos} \approx 5$ mm at $E = 1$ GeV
$e^+e^- \to n\bar{n}$, $D_0 \to K_L\pi^+\pi^-$	Nucleon structure Unity of CKM triangle	EMC+MUD	$\sigma_T = \frac{300}{\sqrt{p^3({\rm GeV}^3)}}$ ps

Beam background at the inner most layer : ~1 Mrad/y, ~1×10^{11} 1MeV n-eq/cm^2/y, ~1 MHz/cm^2

Updated Detector Design



Main Performance requirements

Tracking: eff>90%@0.1GeV, σ_p/p~0.5%@1GeV

Energy meas. : 25MeV-3.5GeV
σ_E/E ~ 2.5% @ 1 GeV

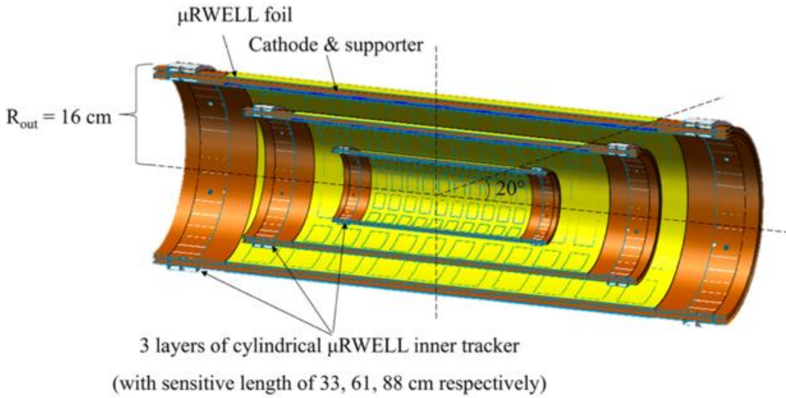
Hadron ID: π/K ~4σ @ 2 GeV, ~3σ @ 3 GeV

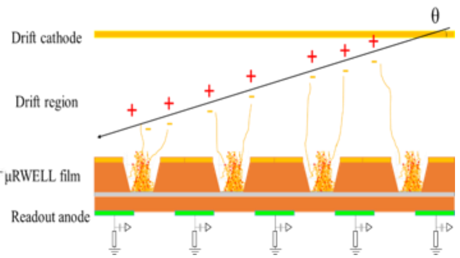
Muon ID: eff. >95%, mis-rate <3.3% @1 GeV

- **Inner Tracker** (4 layers)
  - MPGD: cylindrical uRGroove, σ_x ~100 μm
  - Silicon: low-mass MAPS, <0.3%X_0/layer
- **Main Drift Chamber** (σ_p/p~0.5% @ 1GeV)
  - Small cells with helium-based gas, σ_x <130 μm
- **PID System** (π/K ~4σ @ 2GeV, <0.3X_0)
  - Barrel: DIRC-like TOF - BTOF (σ_t~30 ps)
  - Endcap: RICH (<4mrad) or ASHIPH
- **EMC**
  - pCsI + APD + waveform readout: (σ_E/E~2.5%, σ_x~5 mm @ 1GeV & ~1 MHz/crystal)
- **Solenoid** : 1 T
- **Muon Detector** (eff. >95%, mis-rate <3.3% @1GeV)
  - inner 5 layers : glass RPC, > 300 Hz/cm^2
  - outer 10 layers : scintillator strip + SiPM, ~ 2.4 m

Tracking System : ITK + MDC

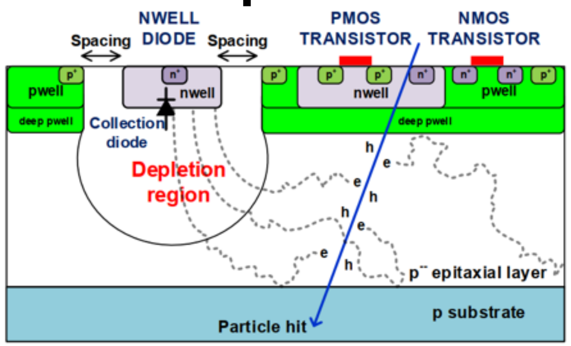
ITK Gaseous option : MPGD



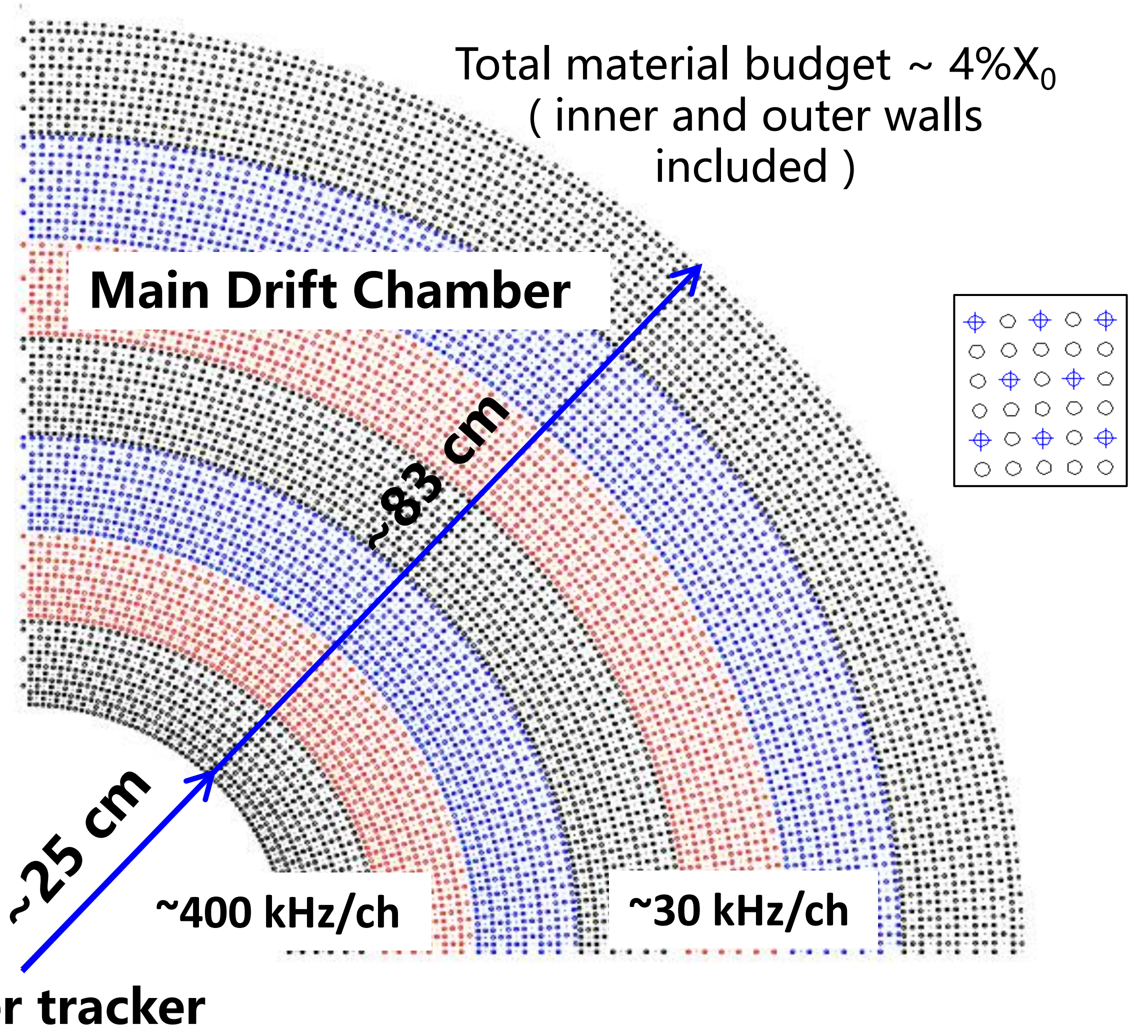


Material budget ~ 0.3%X_0/layer

ITK Silicon option: CMOS MAPS



单片有源像素探测器



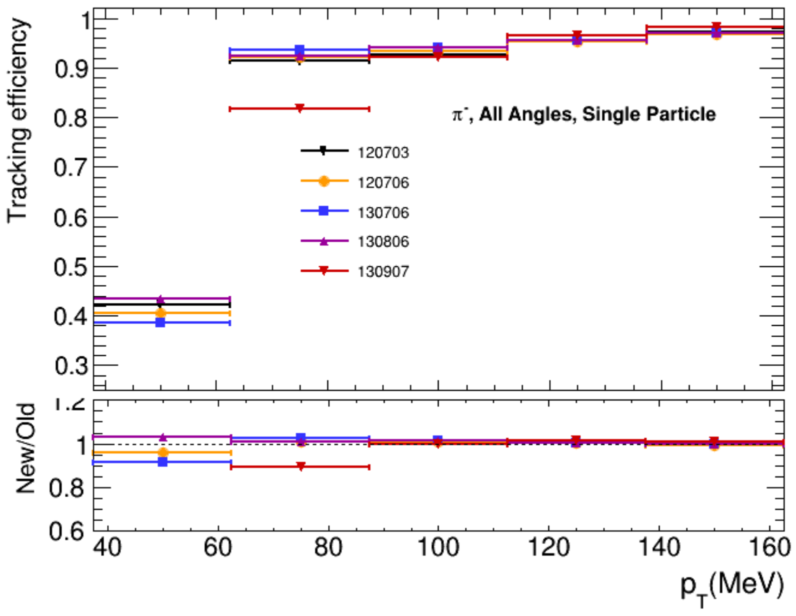
Inner-outer separate designs to accommodate different levels of radiation background

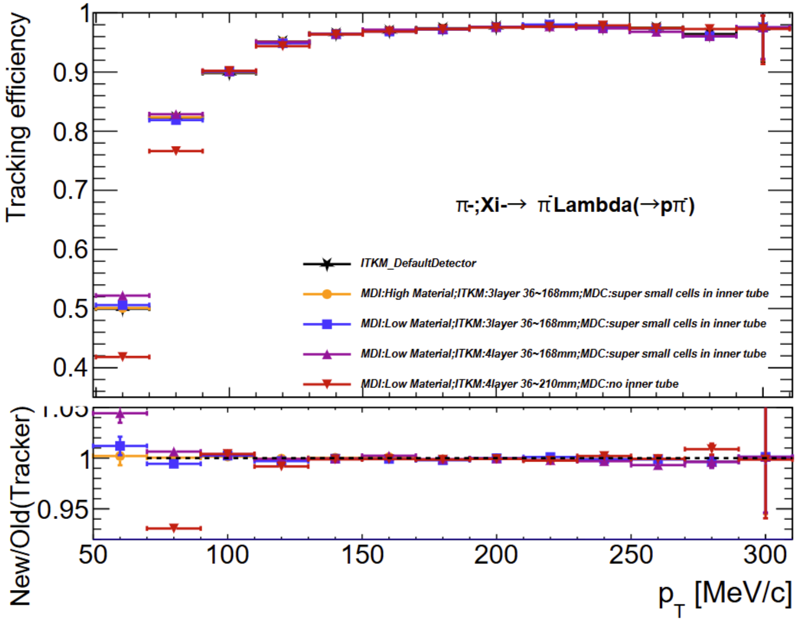
Tracking System Layout Optimization

Layout Options	Beam Pipe	ITK	MDC
CDR	high material budget	3 layers, 36~168 mm	48-layers, 20~80 cm
1		3 layers, 36~168 mm	inner chamber with super small cells + 42 regular layers, 20~83 cm
2	low material budget	3 layers, 36~168mm	inner chamber with super small cells + 42 regular layers, 20~83 cm
3		4 layers, 36~168 mm	inner chamber with super small cells + 42 regular layers, 20~83 cm
4		4 layers, 36~210 mm	42 regular layers without inner chamber, starting with stereo layers, 25~83 cm

- **All the above detector geometries were implemented in OSCAR**
- **Full simulation and track reconstruction with Hough+GenFit were performed for benchmark physics processes to assess tracking performance**

Tracking Performance with Different Layouts



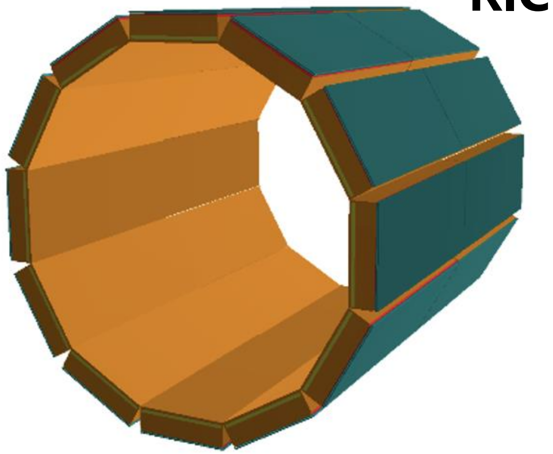


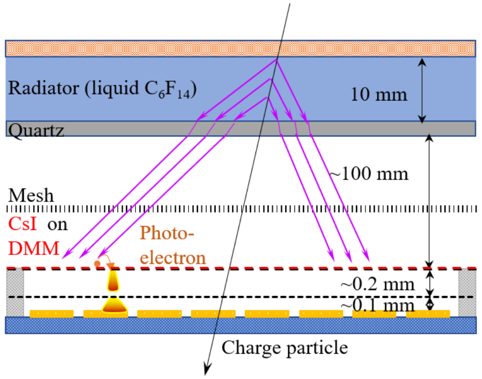
- ❖ **Same tracking efficiency for different layouts when pt >100 MeV/c**
- ❖ **Important to have axial layers in the MDC inner part to maintain tracking efficiency for pt < 100 MeV/c with the baseline track reconstruction algorithm**
- ❖ **The optimized tracker layout : 4 ITK layers + 42 MDC layers started with 10 axial layers. Detailed performance studies are underway.**
- ❖ **Further optimization of drift cell shape is underway (by BINP)**

Evolution of PID Detector Options

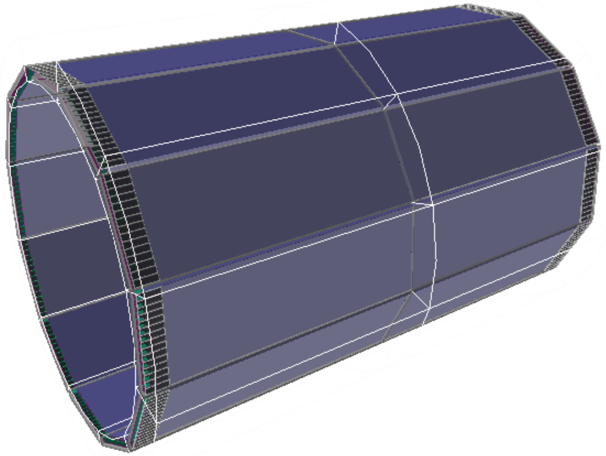
❖ Barrel : baseline changed from RICH to BTOF

RICH



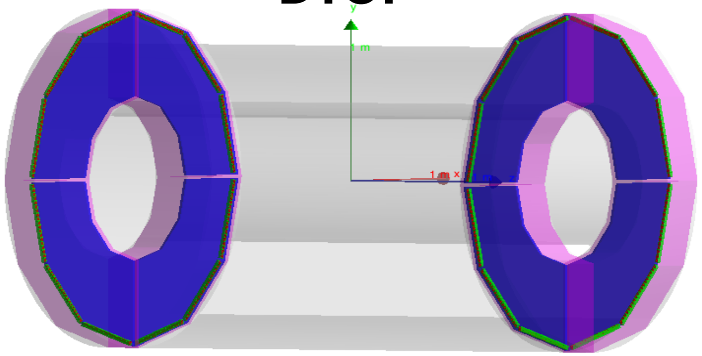


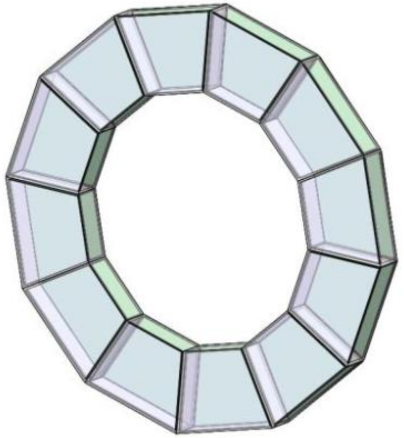
BTOF



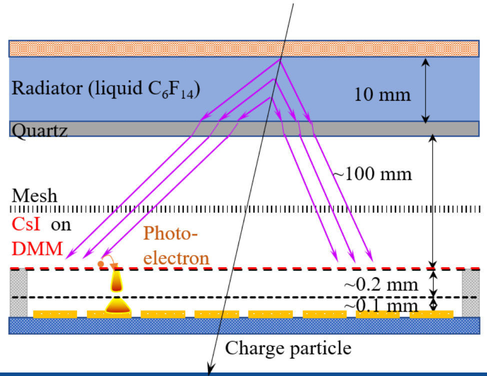
❖ Endcap : RICH and ASHIPH in addition to the well-developed DTOF

DTOF





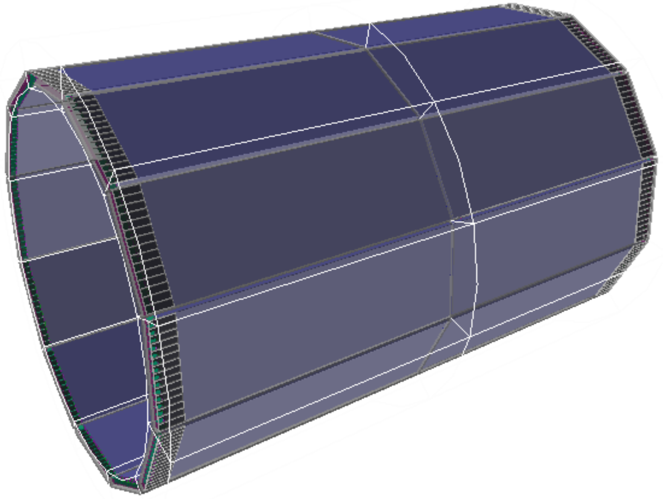
RICH

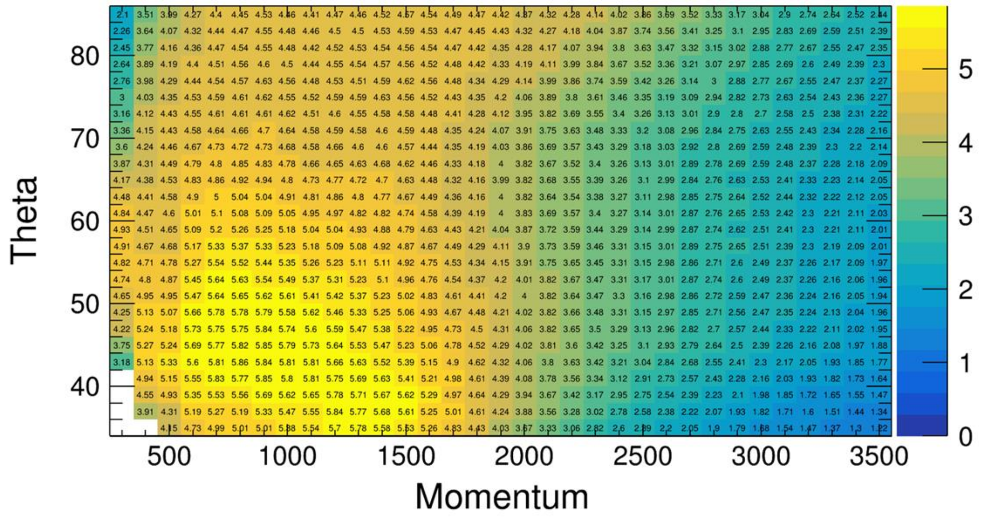


ASHIPH

BTOF : DTOF in Barrel (new baseline for barrel PID)

- **Design of a barrel PID detector based on the DTOF technology (BTOF) has been developed**
  - 12 sectors with 2 modules placed longitudinally in each sector, 24 quartz plates in total
  - Quartz plate parameters : R = 875mm H = 20mm L = 1350mm D = 450mm
  - Quartz side plane is equipped with MCP-PMT for readout
- **Performance assessed with full simulation, fulfilling PID requirements.**
- **Ongoing effort to optimize the design:** bonding of BTOF modules, radiator thickness, optical filter (wavelength cut-off range), optical expanding volume …

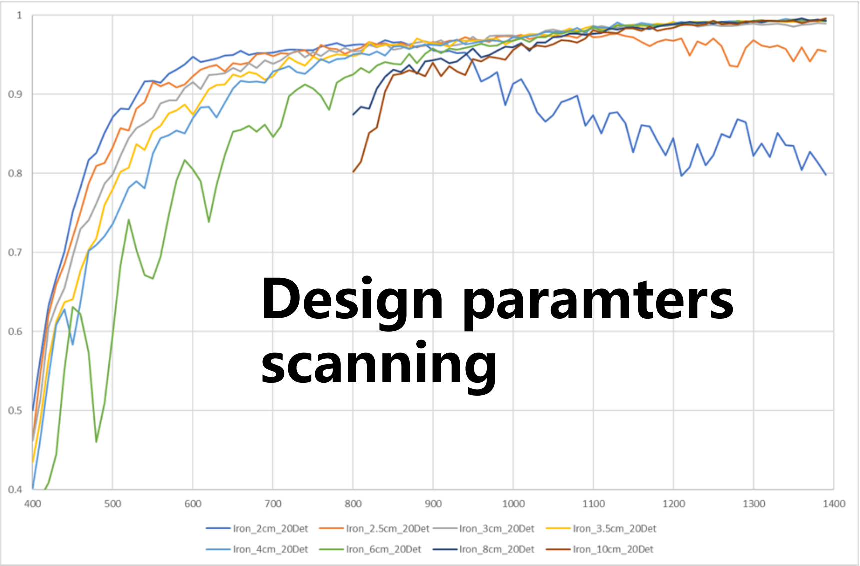


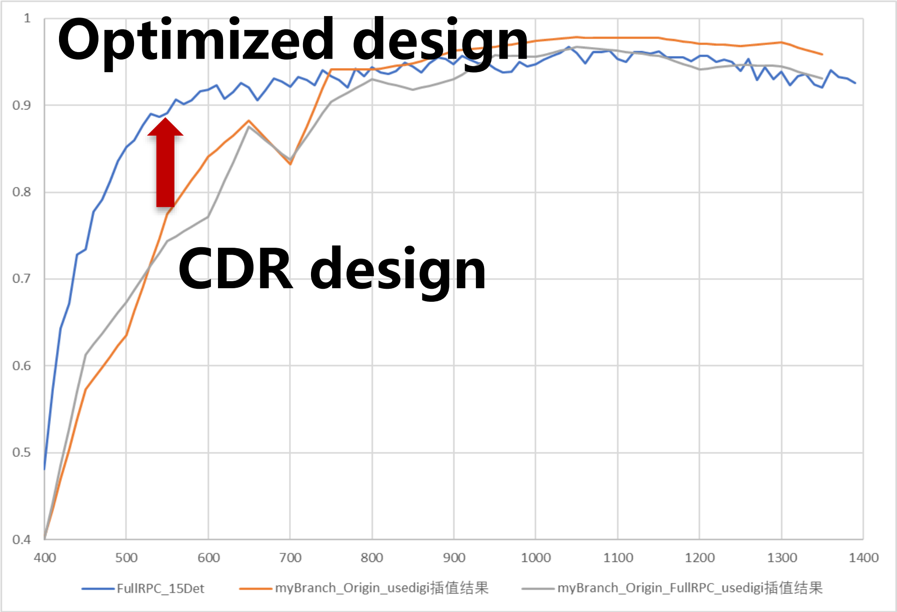


A lot of synergy with LHCb-TORCH is being explored

Muon Detector Optimization

- **A hybrid design with RPC (not sensitive to background) and scintillator strips (sensitive to hadrons) for optimal overall muon and neutral hadron identification performance.**
- **Muon detector design has been optimized by scaning key design parameter: number of layers, iron absorb layer thickness, detector option combination**





Optimized design : 15 detector layers (5 RPC layers + 10 scintillators layers) with 14 layers of iron yoke (2, 2, 2, 2, 2, 2.5, 3, 3, 3.5, 4, 4, 5, 6, 10 cm in thickness)

Detector R&D Breakdown and Organization

	System name	Code	Participating Institutes
1	Inner Tracker - MPGD	ITKW	USTC, IMP
2	Inner Tracker - MAPS	ITKM	USTC, SDU, CCNU, NPU
3	Main Drift Chamber	MDCH	IMP, SDU, USTC, SZTU, BINP
4	Endcap PID Detector	PIDE	UCAS, USTC, GXU, BINP
5	Barrel PID Detector	PIDB	USTC, XIOPM
6	EM Calorimeter	ECAL	USTC, UCAS, SJTU
7	Muon Detector	MUON	LZU, ZZU, SDU, USTC
8	Clock and Data Trans.	CLDT	USTC, CNNU, HUST
9	Trigger System	TRIG	USTC, HUST, SDU
10	DAQ system	DACQ	USTC, CNNU
11	Forward System	FWDR	ZJU, GXNU, USTC, LNU, NJU, DZU, Academia Sinica
12	Detector Magnet	DSSM	SIEMENS SZ, IASF SZ, USTC
13	Mechanical System	MECH	AUST
14	Detector Control System	DCSS	USTC, IMP

Working Groups Meetings and Topical Workshops

- **Weekly or bi-weekly meetings for sub-working groups and detector group plenary meetings on a monthly basis. Mini-workshops on dedicated R&D topics.**

January 2024
- Jan 23 Detector Division Technical Discussion Meeting

November 2023
- Nov 30 Detector Division Technical Discussion Meeting

October 2023
- Oct 27 Detector Division Progress Review Meeting

September 2023
- Sep 27 Detector Division Technical Discussion Meeting
- Sep 08 Detector Division Progress Review Meeting

MAPS-ITK Working Group	85 events	➜
MPGD-ITK & MDC Working Group	31 events	➜
PID Working Group	39 events	➜
EMC Working Group	32 events	➜
MUD Working Group	35 events	➜
Trigger & DAQ Working Group	37 events	➜
Clock and Data Transmission Working Group	7 events	➜
Detector Control System Working Group	1 event	➜
Mechanical Working Group	13 events	➜
Forward Region Working Group	19 events	➜
Magnet Working Group	3 events	➜
General Meetings	21 events	➜

2:00 PM → 2:10 PM **Introduction** 10m
Speakers: Jianbei Liu (University of Science and Technology of China), Qian Liu (University of Chinese Academy of Sciences), Yi Qian (Institute of Modern Physics, Chinese Academy of Sciences), Lei Zhao (University of Science and Technology of China), Dongdong Hu (University of Science and Technology of China)
进度和质量...

2:10 PM → 2:30 PM **MAPS Inner Tracker（ITKM）** 20m
Speakers: Jiajun Qin (University of Science and Technology of China), Lailin Xu (University of Science and Technology of China)
STCF_MAP...

2:30 PM → 2:50 PM **uRWELL Inner Tracker（ITKW）** 20m
Speakers: Yi Qian (Institute of Modern Physics, Chinese Academy of Sciences), Yi Zhou (University of Science and Technology of China)
STCF分总...

2:50 PM → 3:10 PM **Main Drift Chamber（MDCH）** 20m
Speakers: Limin Duan (Institute of Modern Physics, Chinese Academy of Sciences), Zhe Cao (University of Science and Technology of China)
MDC9月总... MDC读出...

3:10 PM → 3:30 PM **Barrel Particle Identification Detector（PIDB）** 20m
Speakers: Lei Zhao (University of Science and Technology of China), Qian Liu (University of Chinese Academy of Sciences)
20230907 ...

3:30 PM → 3:50 PM **Endcap Particle Identification Detector（PIDE）** 20m
Speakers: Ming Shao (University of Science and Technology of China), Yonggang Wang (Univeristy of Science and Technology of China)
STCF谱仪...

3:50 PM → 4:10 PM **Electromagnetic Calorimeter（ECAL）** 20m
Speakers: Yunlong Zhang (University of Science and Technology of China), Zhongtao Shen (University of Science and Technology of China)
STCF EMC ...

4:10 PM

4:30 PM

2:40 PM → 3:10 PM **MAPS Inner Tracker ASIC**
Speakers: Jiajun Qin (University of Science and Technology of China), Lailin Xu (University of Science and Technology of China)
STCF ASIC讨论会...

3:10 PM → 3:50 PM **uRWELL Inner Tracker & PIDB ASIC**
Speaker: jiaming li (University of Science and Technology of China)
STCF RICH μRWELL...

3:50 PM → 4:20 PM **Endcap Particle Identification Detector ASIC**
Speakers: Yonggang Wang (Univeristy of Science and Technology of China), 然 王
2023-09-27_DTOFA...

4:20 PM → 4:50 PM **Muon Detector ASIC**
Speaker: Feng Li (University of Science and Technology of China)
MUD ASIC进展2023...

4:50 PM → 5:20 PM **Data Transmission ASIC**
Speakers: Jinhong Wang (University of Science and Technology of China), 迪 郭 (华中师范大学)
时钟与高速数据传...

高亮度实验触发和数据获取系统设计研发讨论会

会议通知

高亮度实验触发和数据获取系统设计研发讨论会定于 2023 年 2 月 17 日在合肥中国科学技术大学举行。本次会议由核探测与核电子学国...

高亮度实验MAPS研发讨论会

Saturday, 1 April 2023 from **08:00** to **20:00** (Asia/Shanghai)
at **物质科研楼 (A608)**
中国科大东校区

Manage

Description 高亮度实验MAPS内径迹探测器研发讨论会定于2023年4月1日(3.31报道，4.1全天开会，4.2离会）在合肥中国科学技术大学举行。本次会议由核探测与核电子学国家重点实验室中国科学技术大学部主办。

高亮度前沿是高能物理实验目前三大前沿研究方向之一，对研究稀有事例，探索新物理有重大推动作用。在高亮度环境中低动量带电粒子的径迹重建具有重大挑战。本次会议将针对高精度、低物质量、低功耗的MAPS内径迹探测器的研发展开相关讨论，并针对国产MAPS工艺的关键技术攻关进行研讨。

STCF探测谱仪机械设计研讨会

Monday Aug 19, 2024, 9:00 AM → 6:05 PM Asia/Shanghai
物质科研楼三楼会议室 (中国科学技术大学)

Description 本次会议将针对STCF实验谱仪机械结构的设计研发问题进行深入讨论，议题包括：谱仪整体的支撑移动系统设计、各探测器系统的内部与谱仪层级机械连接装配设计、电子学芯片散热设计等。

腾讯会议：456-104-342

https://meeting.tencent.com/dm/3arobCI1DURC

STCF HLT 计算存储专题研讨会

Thursday Nov 21, 2024, 2:00 PM → 11:05 PM Asia/Shanghai
物质科研楼三楼会议室 (中国科学技术大学)

Description 高层级触发（HLT）设计是决定STCF实验数据量的关键环节，计算存储方案则影响了后续的长期数据存储、分析、利用的规划，都是工程化阶段需要慎重考虑的系统。目前粗估输入给HLT的数据量约10 GB/s，每年数据存盘量在200 PB水平，需要详细讨论两个系统的设计与实现方案以获得更好的综合性能，保障STCF的长期稳定运行。

https://cern.zoom.us/j/67548157547?pwd=S0B7TYHk4M6hcDtEuy5qjNzPFv2aBJ.1

ZOOM ID: 675 4815 7547

Password: 325525

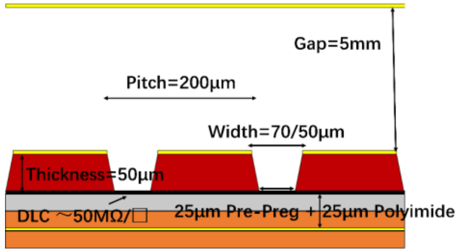
2:00 PM → 2:20 PM **STCF初步采数规则说明**
Speaker: Xiaorong Zhou (University of Science and Te
STCF_data_taking_...

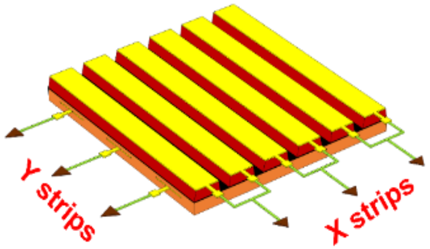
2:20 PM → 3:10 PM **STCF HLT研究进展与计算资源估算**
Speaker: Zhujun Fang (USTC)
20241118 STCF HL...

3:10 PM → 4:10 PM **从DAQ角度看STCF计算中心需求_FTCF2024**
Speaker: Junfeng Yang (USTC)
从DAQ角度看STCF...

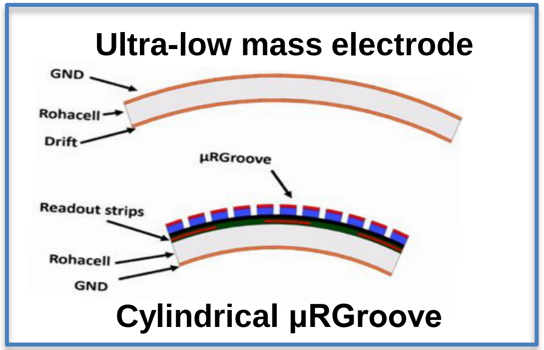
MPGD ITK : μRGroove

- Proposed and developed a novel single-stage MPGD, micro-resistive Groove detector (μRGroove), for the inner tracker: larger signals and easier production compared to μRWELL.

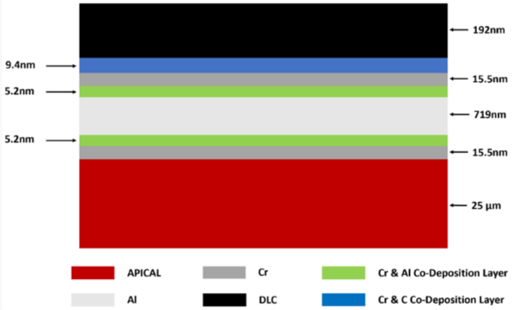


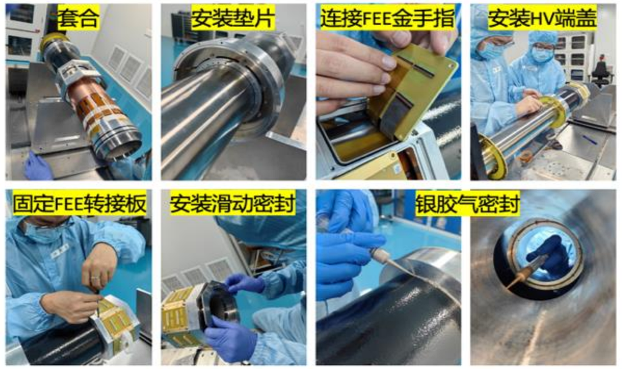


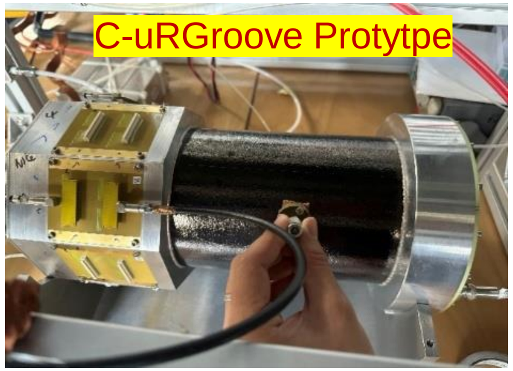
- Developed a set of techniques and procedures for fabricating a cylindrical low-mass μRGroove detector and built a low-mass c-μRGroove prototype: material budget ~ 0.23%X0/layer, the best in cylindrical MPGDs.



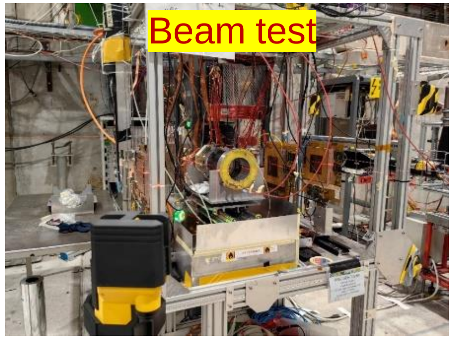
Ultra-low mass electrode

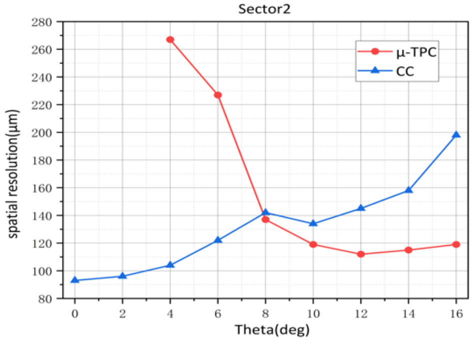






- Conducted multiple beam tests of the prototype at CERN. Position resolution < 100μm for vertical tracks, and <130μm for inclined tracks or in 1T magnetic field.

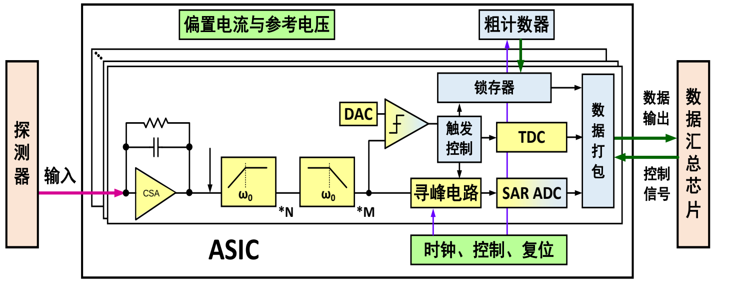




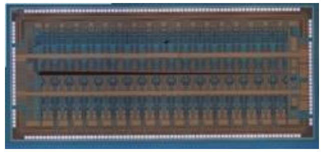
MPGD ITK : Electronics

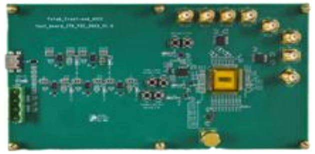
- **ASIC is required for readout. Very challenging performance requirements (event rate much higher than VMM). Designed and produced a 32-channel prototype ASIC chip with full function, and tested it with a detector prototype.**

- **Development of readout electronics with the ASIC is well underway**

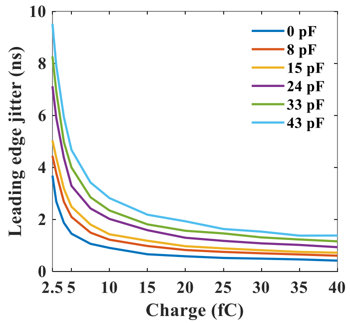


ASIC Specs	Demands
Charge Range	40 fC
Charge precision	～1 fC RMS
Time precision	< 10 ns RMS
Max. event rate	4 MHz

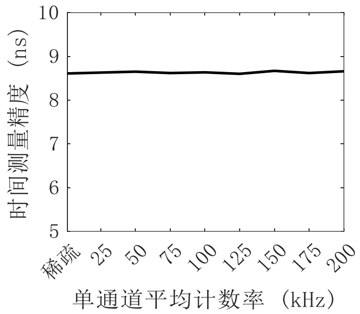


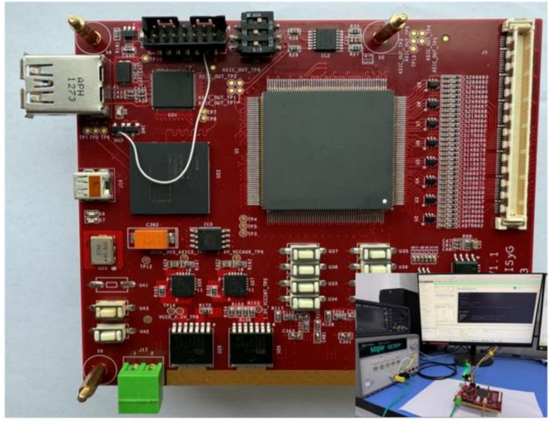


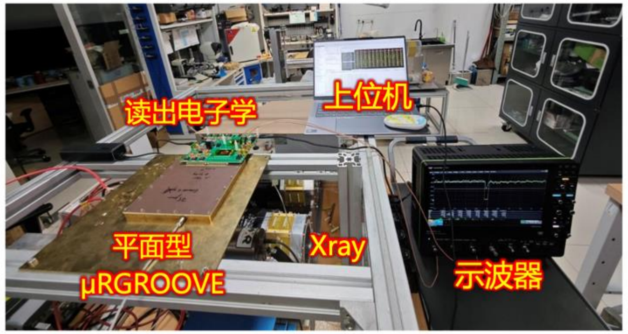
Time Resolution



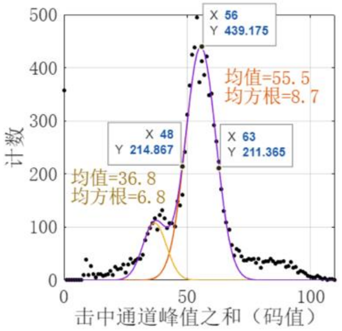
Counting rate



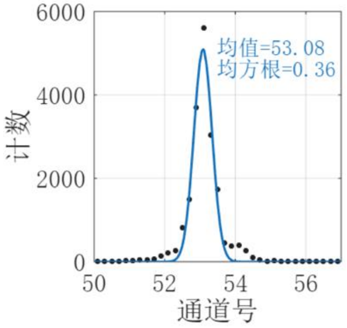




联调现场照片



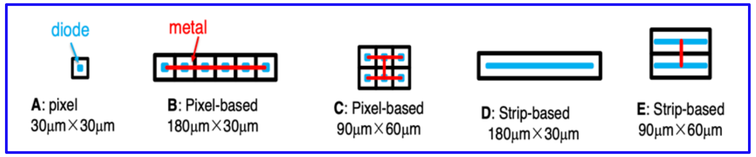
-475 V -1000 V偏压下
的能谱测量数据

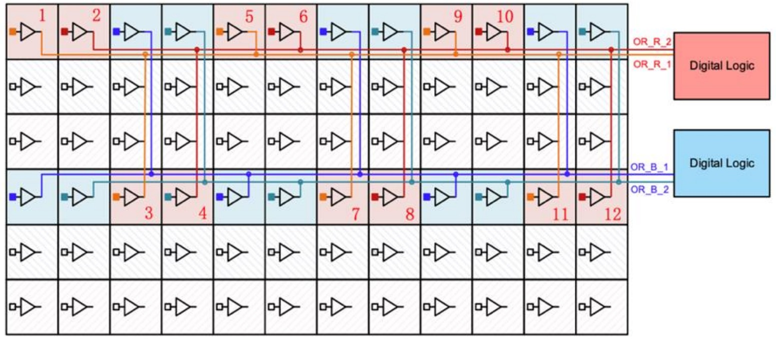


-475 V -2000 V偏压下
的位置测量结果

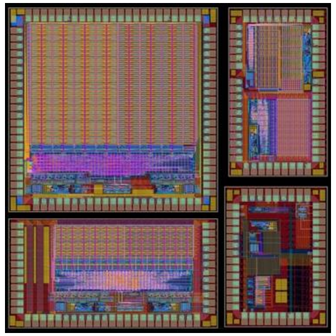
MAPS ITK : MAPS Designs

- **Core target: a low-power MAPS design with moderate position resolution and both timing and charge measurement capabilities.**
- **Low power outweighs position resolution: exploring strip-like or large-size pixel MAPS designs to reduce power.**
- **Exploring a super-pixel design that can provide both high position and high time resolutions for low power consumption.**
- **Various CMOS processes being explored**
  - **Mature technology: 180nm (HR epi)**
  - **Domestic foundries: 90nm (LR epi) , 130nm (HR substrate), 180nm (HR epi)**

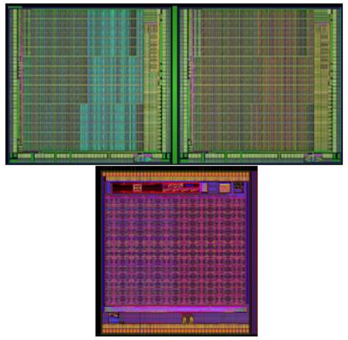




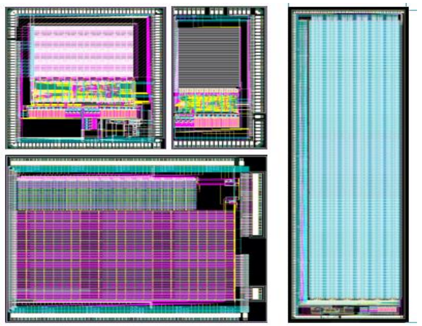
180nm
Chips received, testing underway



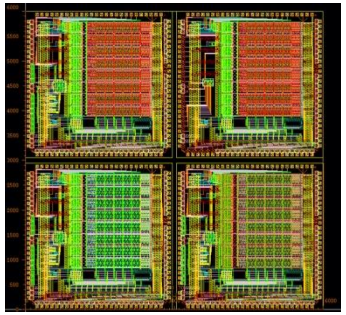
90nm
Chips received, to be tested



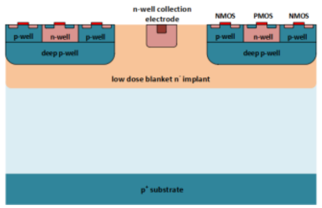
130nm
Chips received, testing underway



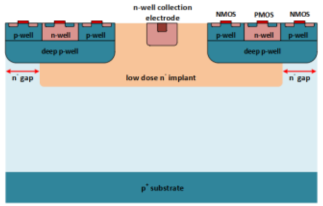
180nm
Supporting quadruple-well with possibility of N-blanket implant and N-gap. Chips received, to be tested



N-blanket implant

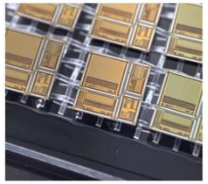


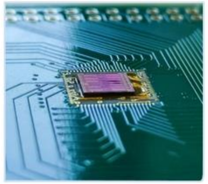
N-gap

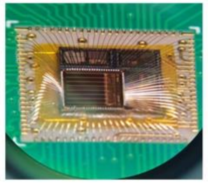


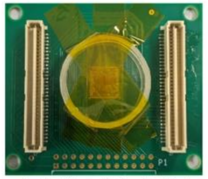
MAPS ITK : MAPS Testing

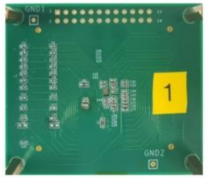
- **Characterized the 180nm and 130nm chips for threshold, noise, fake hit rate and capacitance. Tested the chips with laser and radioactive sources (Fe55 and Sr90) for detection efficiency, charge collection efficiency and time resolution.**

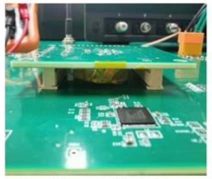

TJ芯片


同尺寸芯片试粘接在绝缘胶上


未划片直接打线

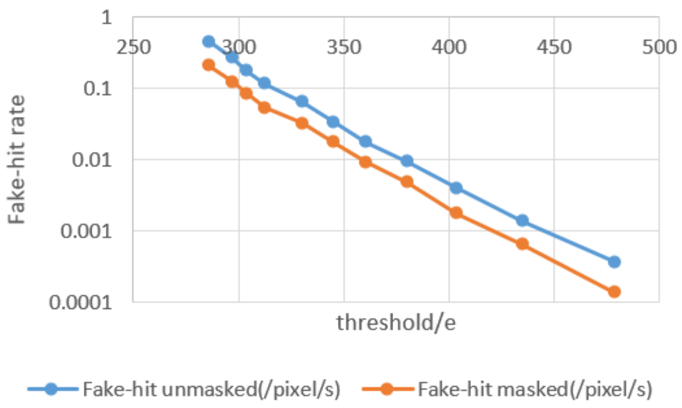

子板背面(芯片+保护壳)

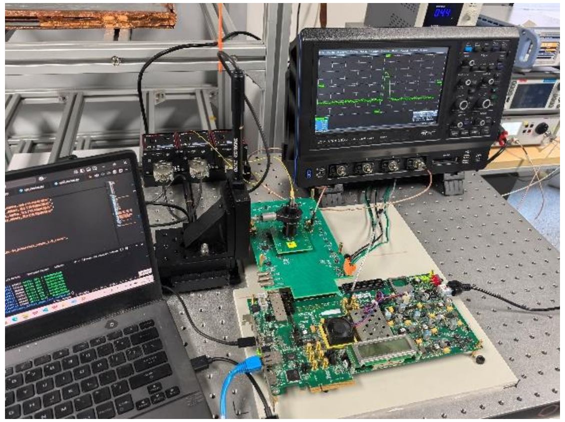

子板正面(绝缘胶挖洞)


子板安装在测试转接板上

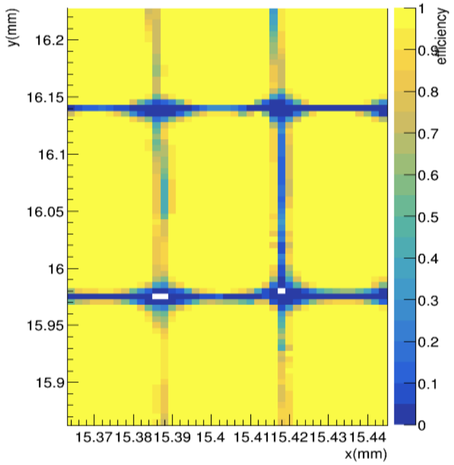
偏压/V	Threshold/e	FPN/e	TN/e	A_{OUT}/mV	基线RMS/mV
-2	268.2	7.15	16.1	523	7.8
-3	234.7	2.75	15.3	477	9.2
-4	212.2	0.82	15.4	417	7.06
-5	178.1	5.32	11.3	348	5.92
-6	182.1	7.11	12.1	292	5.88

Background trigger rate

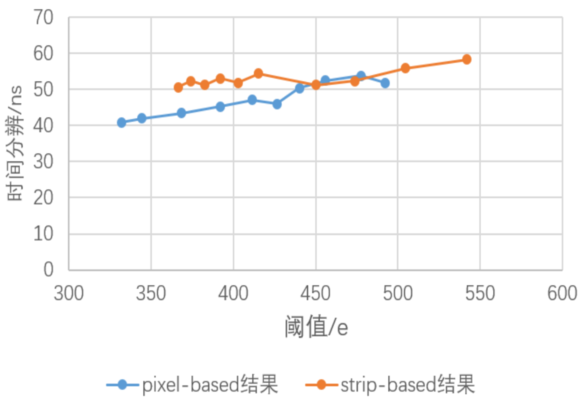




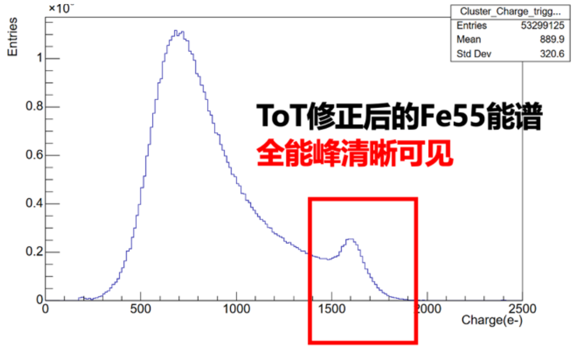
Efficiency



Time resolution (180nm)

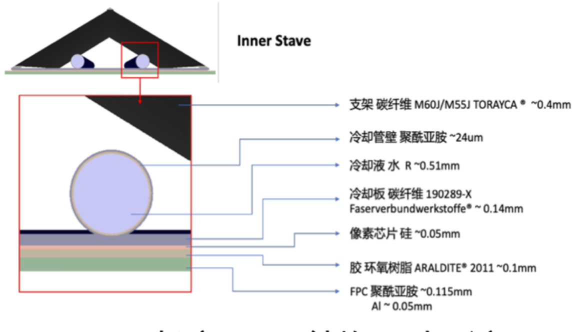


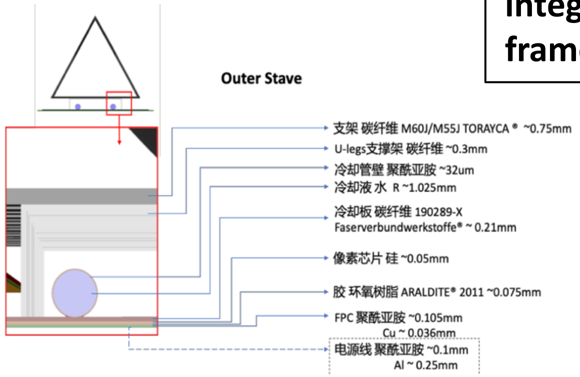
Fe55 energy spectrum (130nm)



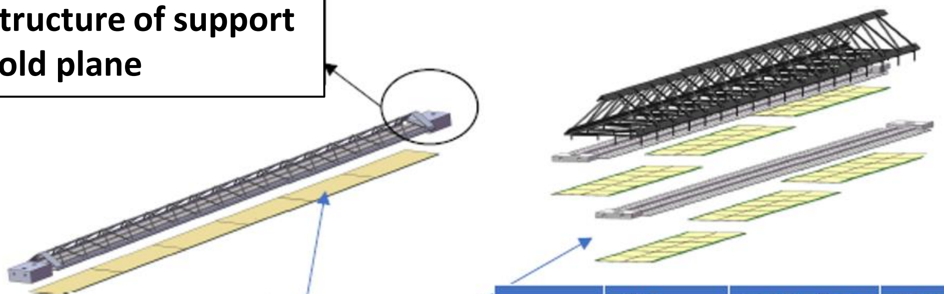
MAPS ITK : Stave Design

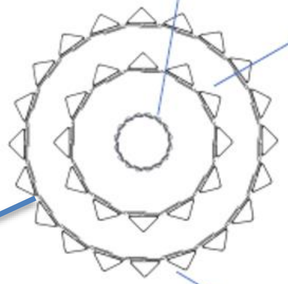
- **Significant progress has been made in detector module (stave) mechanical design**

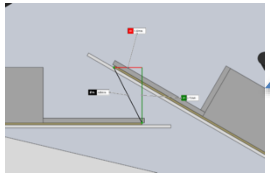




The inner most layer:
integrated structure of support frame and cold plate

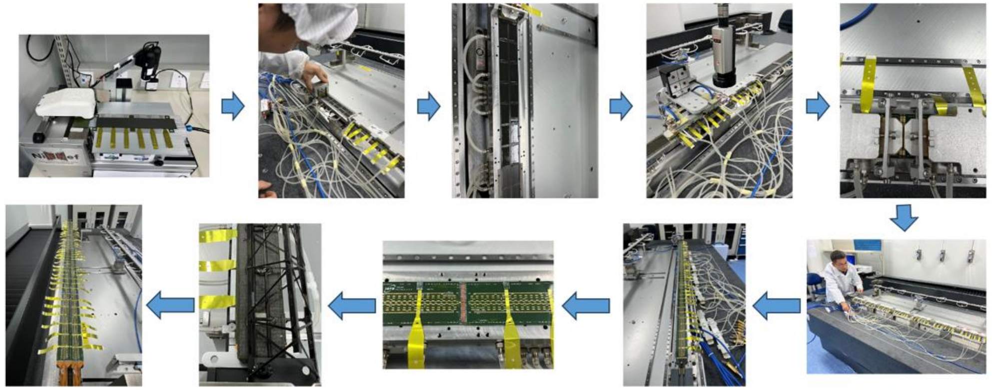


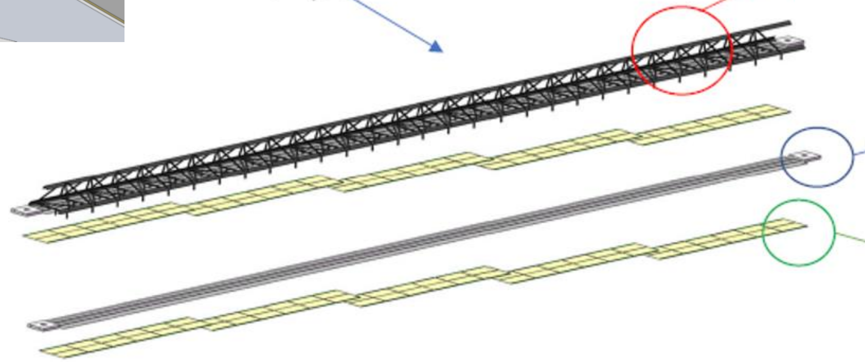




	半径	STAVE数量	STAVE全长
内层	36mm	16	200.75mm
中间层	98mm	12	592.25mm
外层	160mm	20	954.55mm

Stave assembly and integration infrastructure and experience





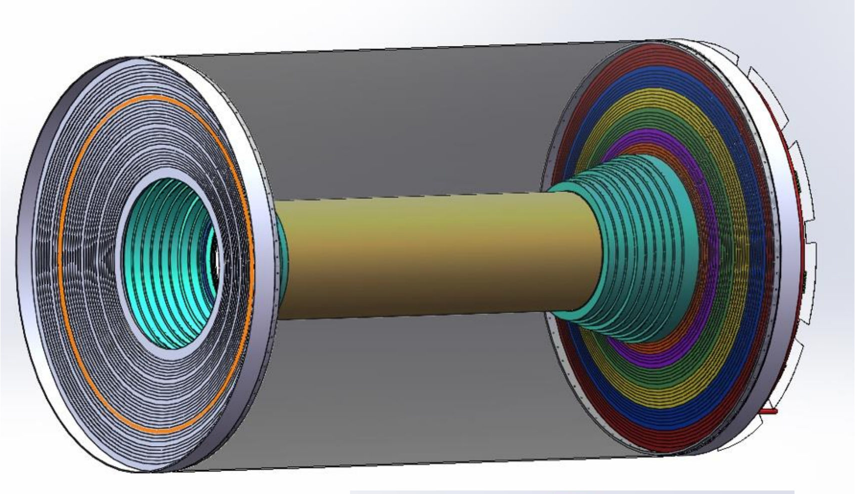
CF support frame

Cold plate

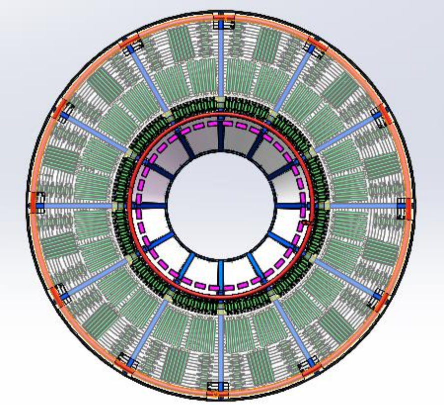
Flex PCB & chips

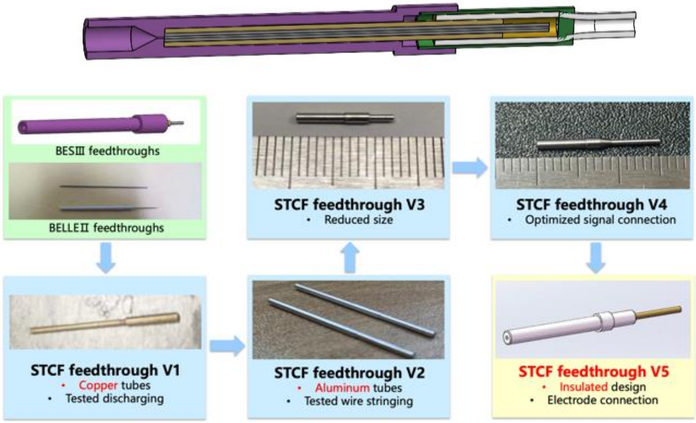
Main Drift Chamber : Detector

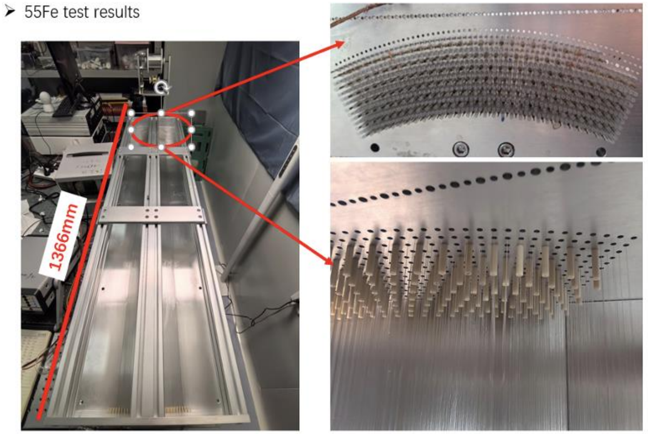
- Endplate structure optimized to simplify the assembly process
- Intensive R&D effort on feedthrough for super-small cells (~5 mm)
- A full-length super-small cell drift chamber prototype is under construction.



Layout of FEE boards

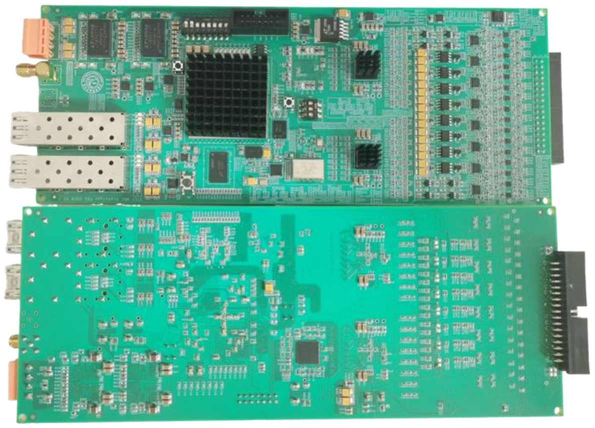


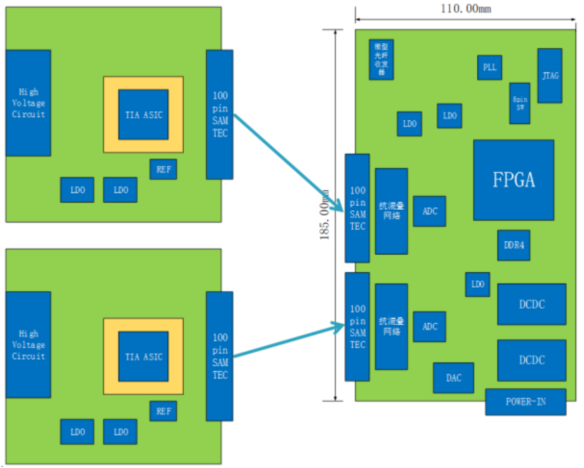


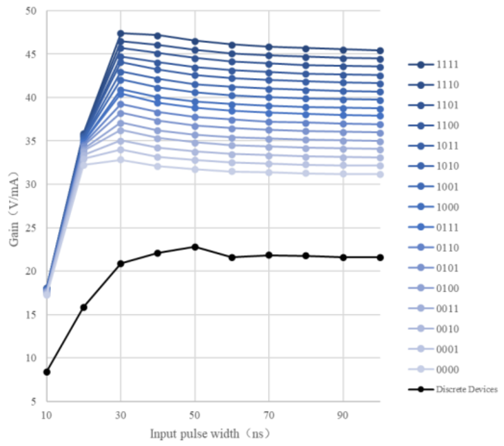


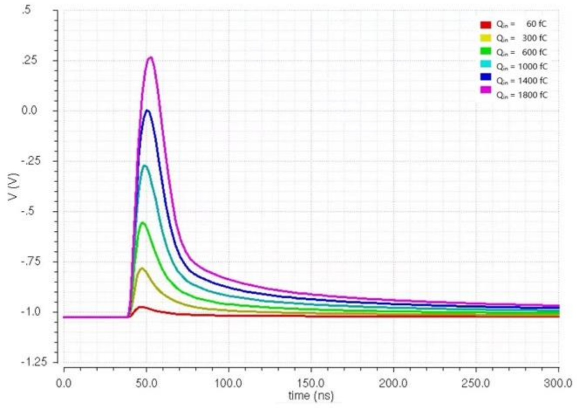
Main Drift Chamber : Electronics

- **The 16-channel electronics board (TIA + shaper + ADC) was updated with new passive components. After passing standalone tests, they are now ready for multi-board integration and testing with a detector.**
- **A new scheme of the electronics system was designed for more integrated layout and less material, separating the Front-End Electronics (FEE) and the waveform digitization board (WDM) on the MDC endplate.**
- **ASIC design is underway. Second version of the analogue part has been taped out and is being tested.**





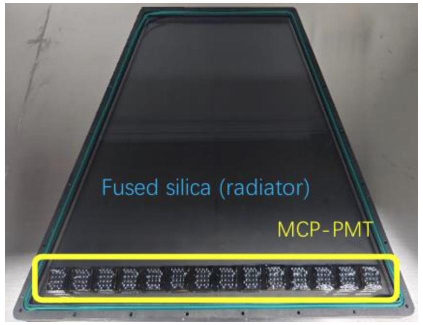


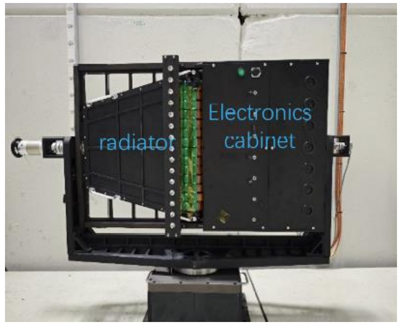


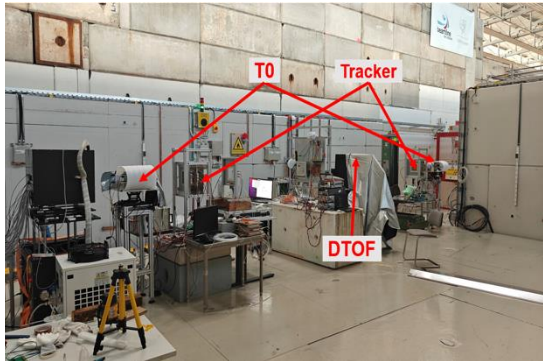
BTOF/DTOF Detectors

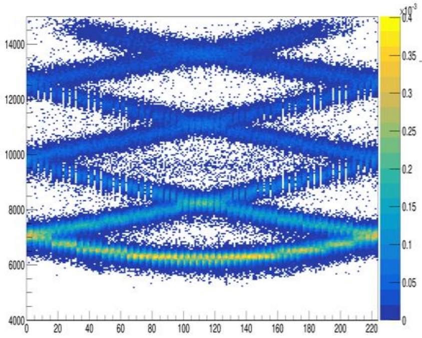
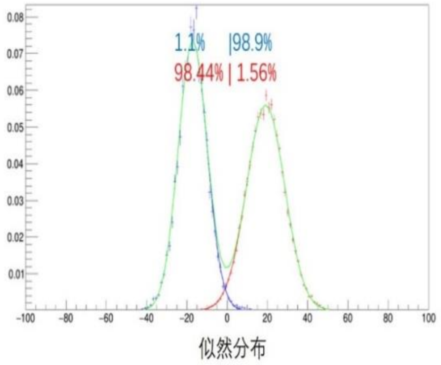
- **A DTOF prototype was built and tested with particle beams at CERN to demonstrate the PID capability of the DTOF detector**

π/K separation >4σ @ 2GeV/c



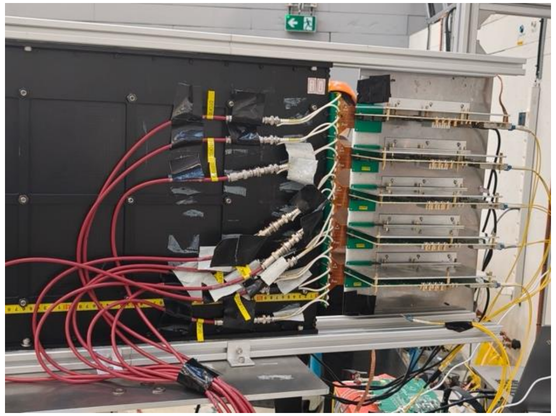




- **A full-length BTOF prototype has been built and tested with particle beams. Data analysis is underway.**





BTOF/DTOF Electronics

➢ ASIC FET v2

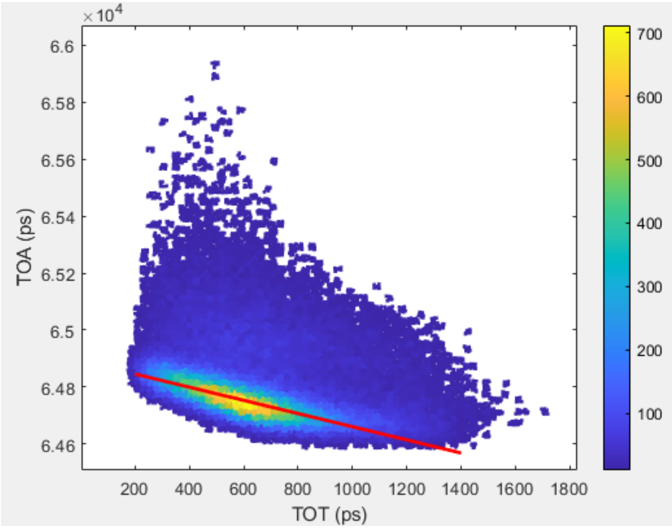
- 8-channel per chip, dynamic range 10 fC – 1 pC
- RMS timing precision < 15 ps
- Single-photon resolution 38–43 ps

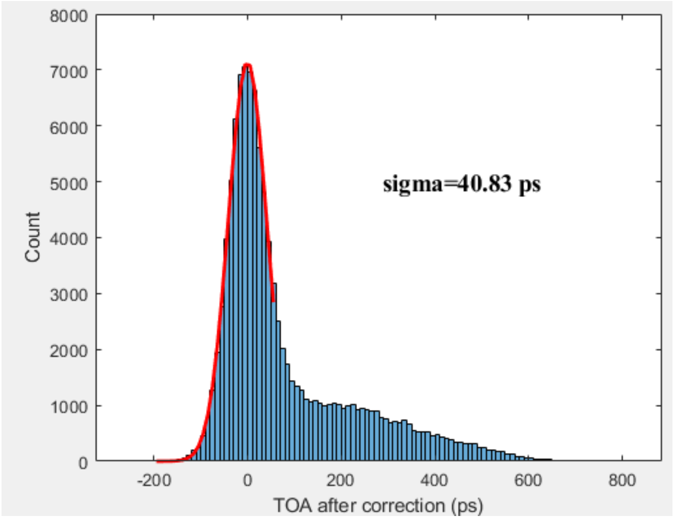
➢ ASIC TDC: MCV-TDC v1

- 160 MHz system clock, LSB = 15 ps
- RMS precision 14 ps
- Event rate 32 MS/s
- Power consumption: 27.76 mW @5 MS/s

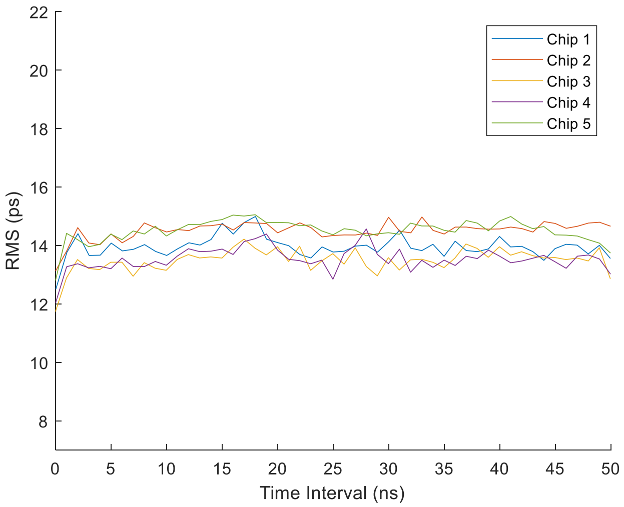
➢ ASIC TDC: DSTA-TDC v2

- Taped out in mid-July 2025
- 8-channel per chip
- TA Gain = 16, LSB = 8 ps
- Adaptive elimination of time amplifier offset; Online calibration

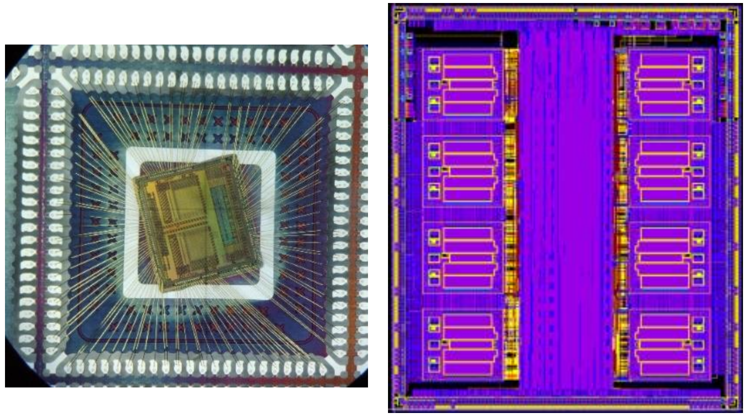




Single-photon time resolution of FETv2



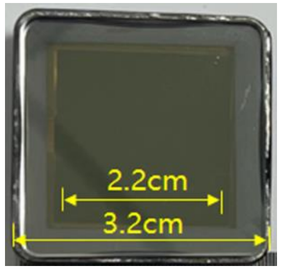
Timing precision of MCV-TDC



MCV-TDC and DSTA-TDCv2

Long lifetime MCP-maPMT

- MCP-maPMT: a critical component of the DTOF technology
- Intensive R&D on techniques (ALD and electron scrubbing) to produce long-life MCP-maPMT (target Q > 10 C/cm^2).
- Designed and produced 1-inch MCP-maPMT prototypes with 16 annodes each.
- Carried out various tests of the MCP-maPMT prototypes
  - TTS<40 ps, QE>20%, G>10^6, Crosstalk < 7%
  - Aging : <50% gain drop when Q>20 C/cm^2

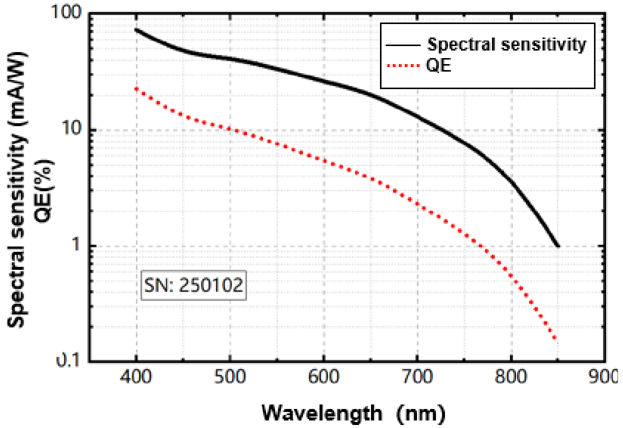


1	2	3	4
5	6	7	8
9	10	11	12
13	14	15	16

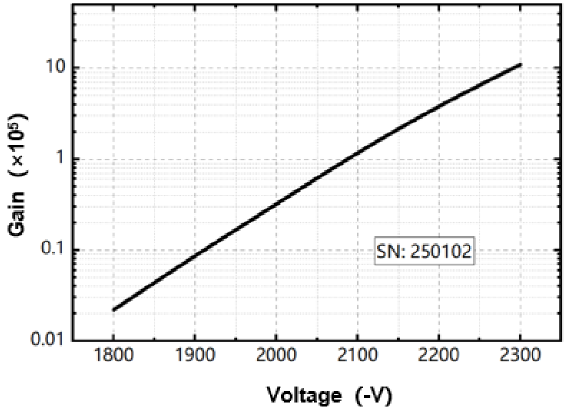
Channel definition

218Hz 1.3nA	17Hz 0.22nA	5Hz 0.07nA	32Hz 0.22nA
26Hz 0.18nA	3Hz 0.07nA	0.4Hz 0.02nA	5Hz 0.1nA
17Hz 0.38nA	3Hz 0.2nA	1Hz 0.13nA	1Hz 0.11nA
675Hz 8.5nA	27Hz 2.6nA	11Hz 0.89nA	12Hz 0.53nA

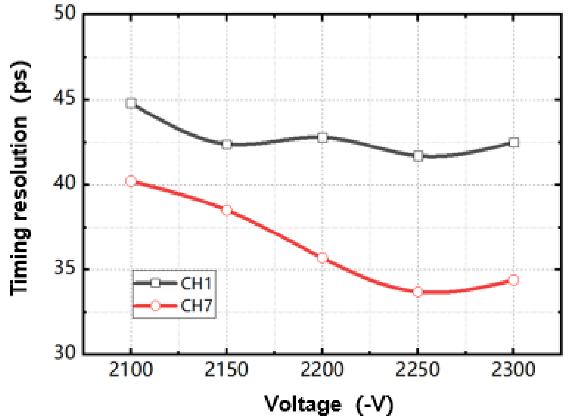
Dark count & dark current



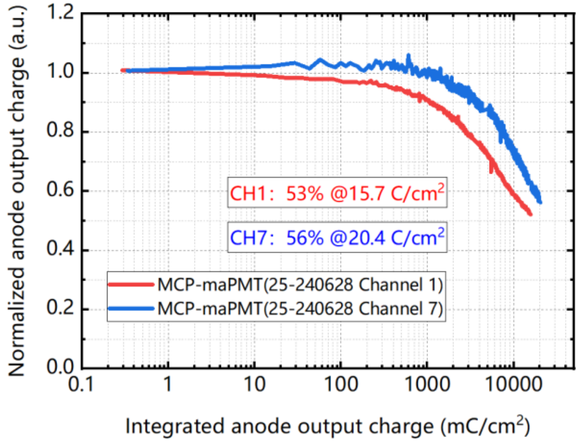
Typical spectral response



Typical Gain



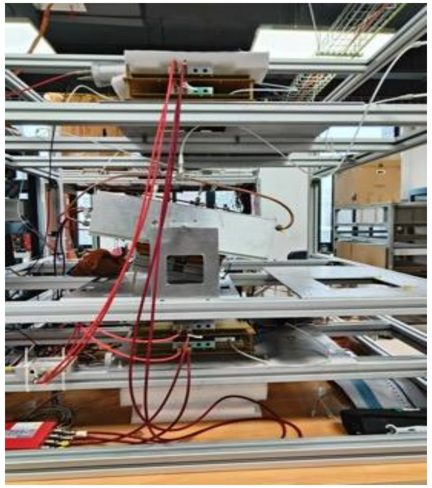
Timing resolution of different channels

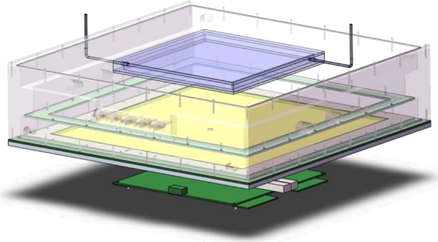


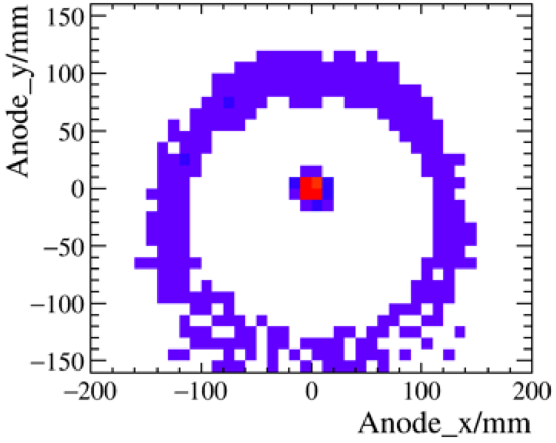
Output drop with IAC

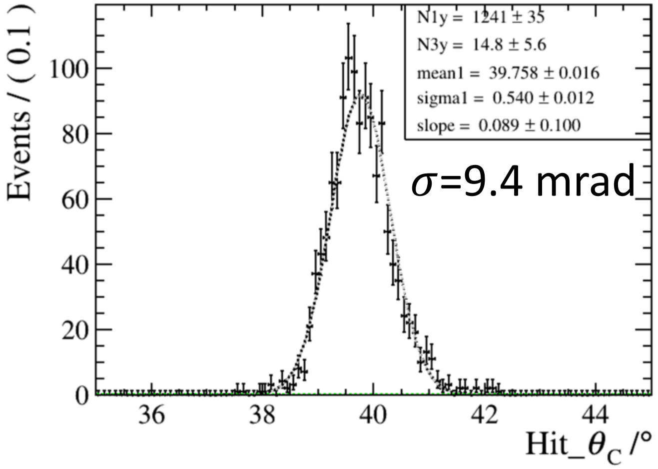
RICH Detector

Cosmic-ray test of a 32×32 cm² RICH prototype with both THGEM+MM and DMM



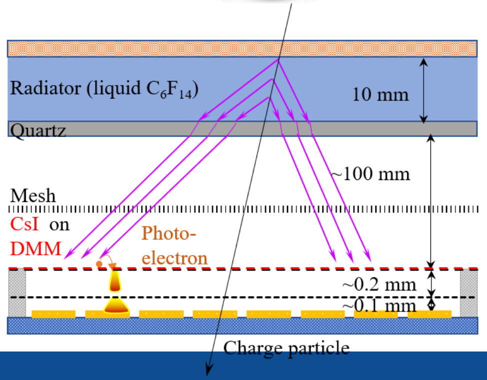


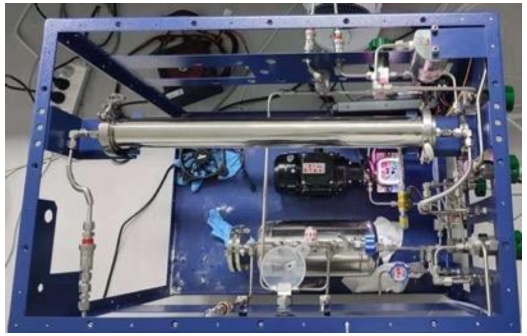


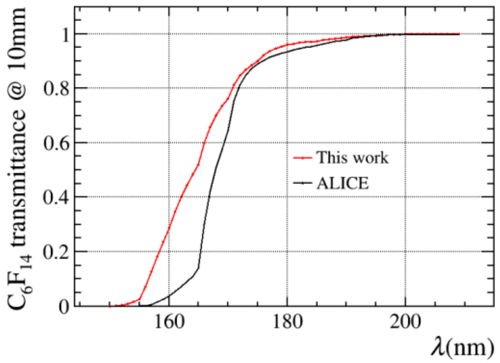


main issue: low photoelectron yield ~2pe/track.

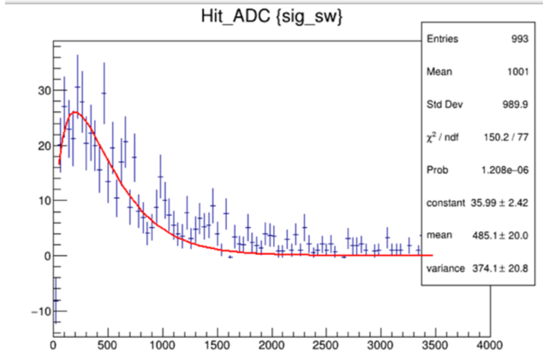
QE of photo cathode needs to be improved !







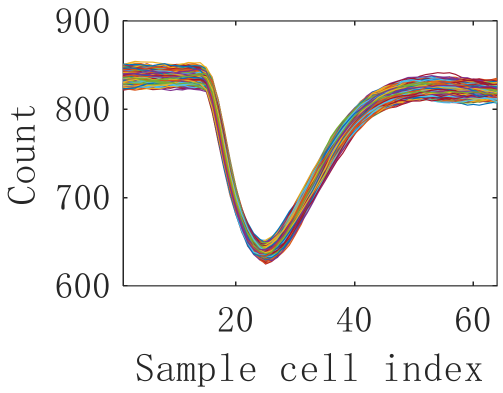
Purifying C_6F_{14} with good transmittance achieved

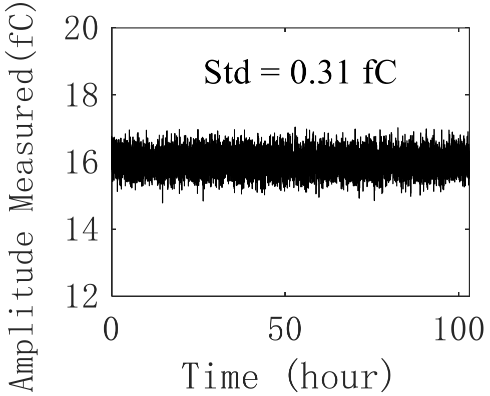


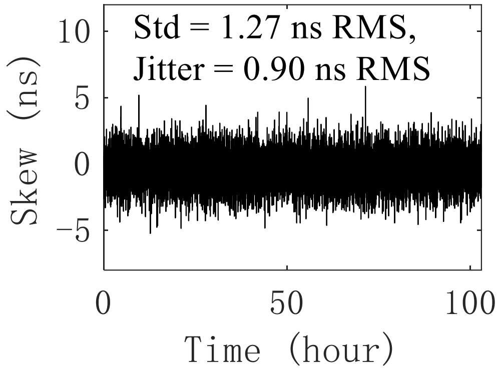
DMM gain 1.2×10^5
THGEM MM gain 0.95×10^5`

RICH Electronics

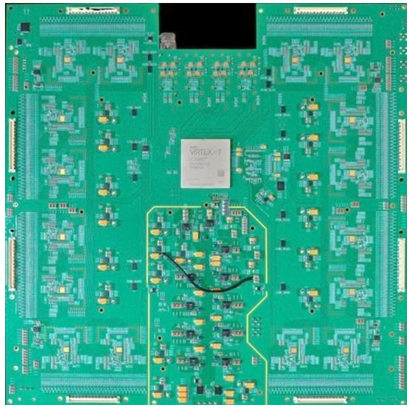
- **Completed the ASIC design and testing for the second-phase development.**
- **Test results show a ENC of better than 0.5 fC and a time resolution of better than 1 ns, meeting the design requirement.**

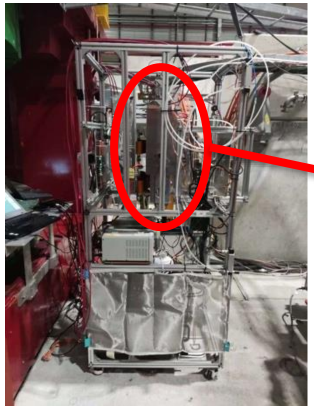


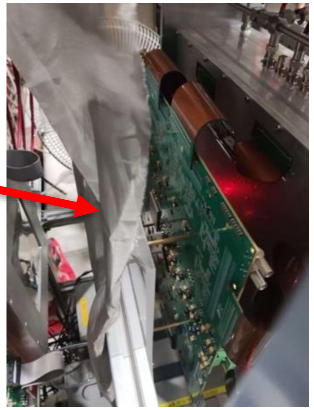




- **Based on the second-phase ASIC, a 1024-channel FEE prototype was designed.**
- **A beam test is ongoing with the detector at CERN's SPS**

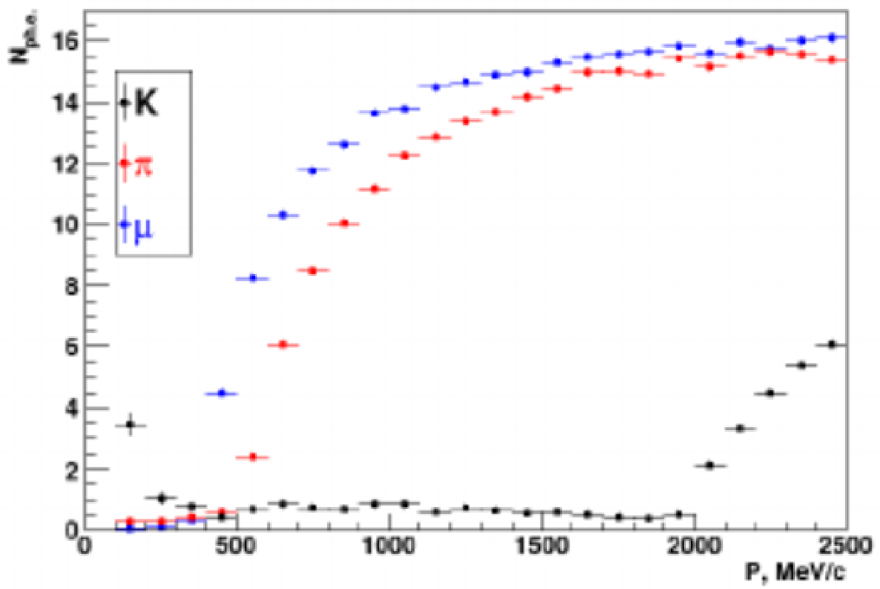




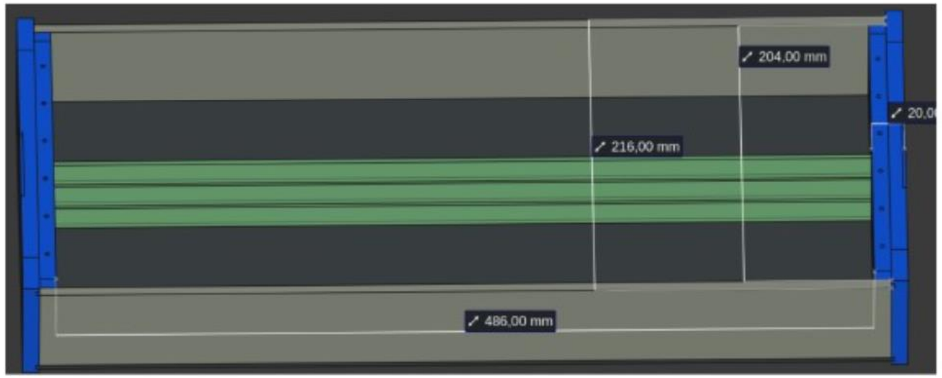


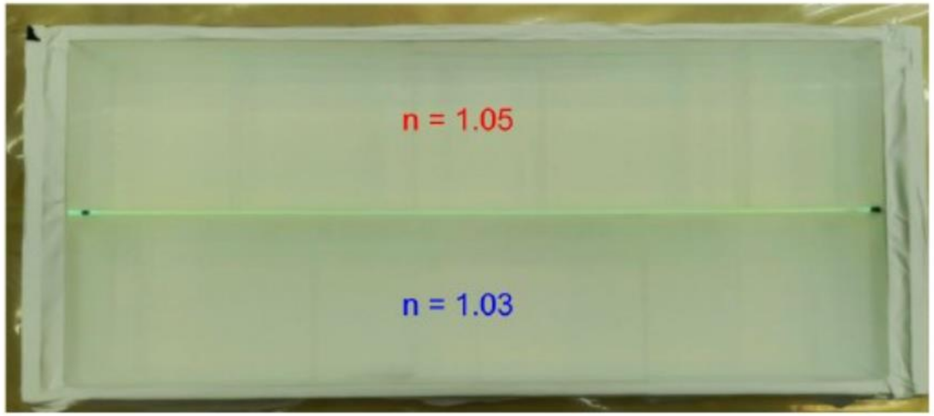
ASHIPH Detector

- Ongoing effort by BINP to use ASHIPH (Aerogel, SHifter, Photomultiplier) Cherenkov counter in STCF as a PID detector.
- Preliminary simulation showed a good pi/K separation up to 2 GeV/c.
- A prototype was built and tested recently.



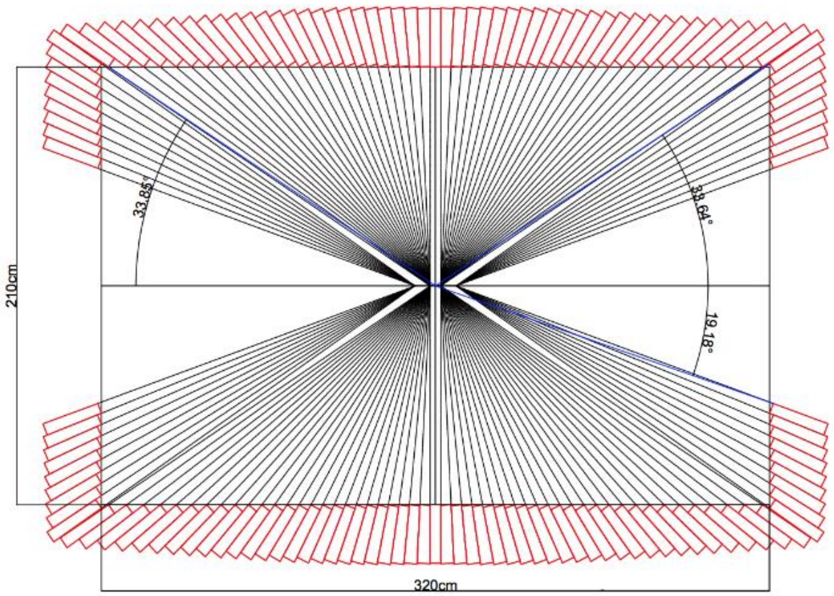
PID performance with threshold of 1 phe



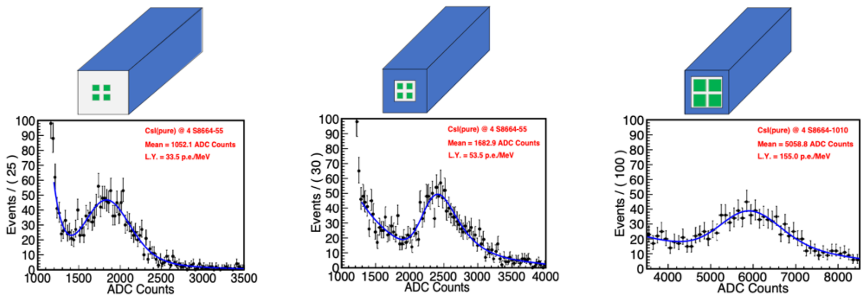


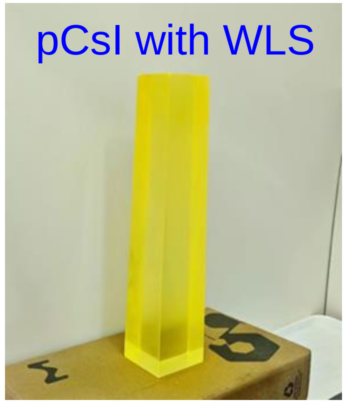
Electro-Magnetic Calorimeter : EMC

- **A crystal calorimeter using pCsI (short decay time of 30ns) to tackle the high background rate (~1 MHz/crystal)**
  - Crystal size: 28cm ($15X_0$), $5\times5cm^2$
  - Defocused layout: 6732 crystals in barrel, 1938 crystals in endcaps
  - 4 large area APDs to address low light yield: $4\times(1\times1cm^2)$



A very low light yield of 3.6% for pCsI → a major R&D task : enhance the light yield of a pCsI unit

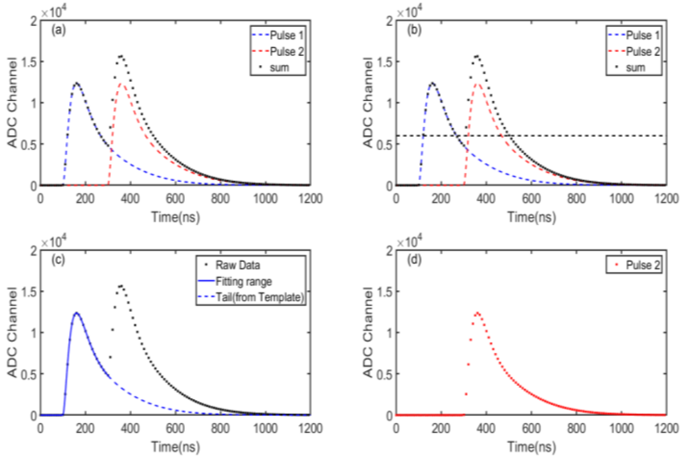


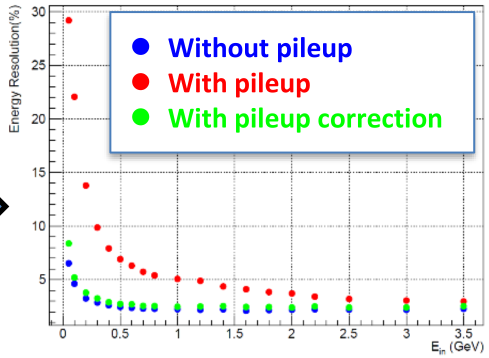


Light yield : 50 p.e./MeV → 300 p.e./MeV

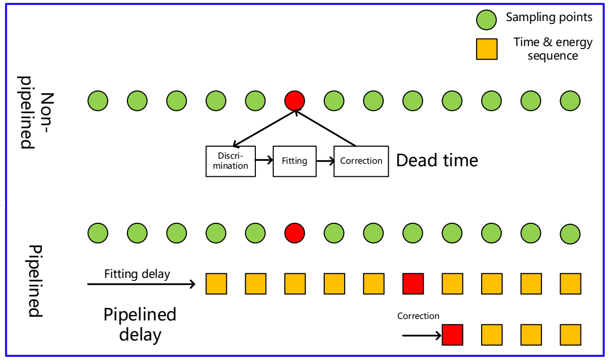
EMC : Pileup Mitigation and Electronics

- **Significant pileup in EMC in the presence of beam background (~1 MHz/ch). A dead-time free pileup correction algorithm involving waveform fitting based on pipelined optimal filtering has been developed and implemented in FPGA**

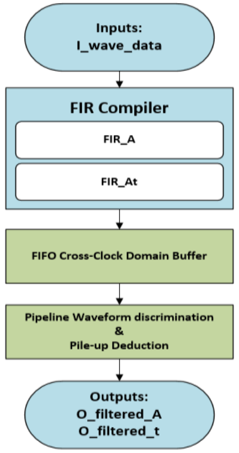




Very effective in mitigating the pileup effect

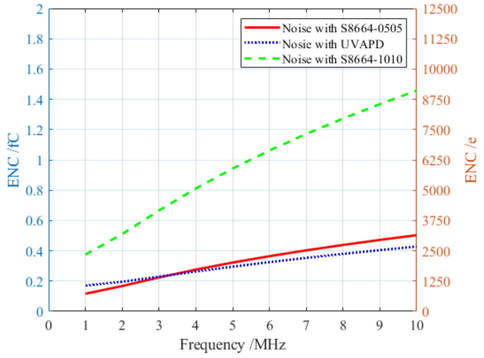


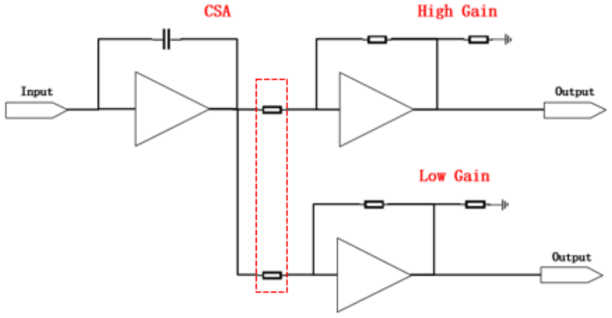
Pipelined correction algorithm



FPGA implementation

- **Development of waveform digitization electronics (CSA + ADC)**



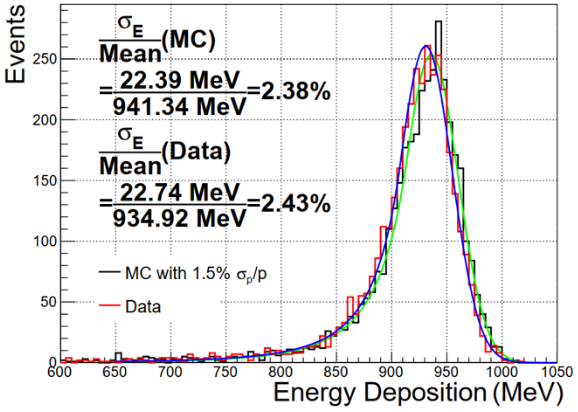


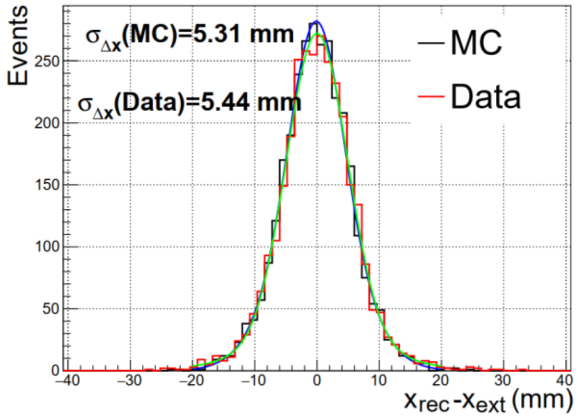
- The dynamic range was improved while maintaining the noise level of the high-gain channel.
- FEM adjustment for waveform consistency between high and low gain channels.

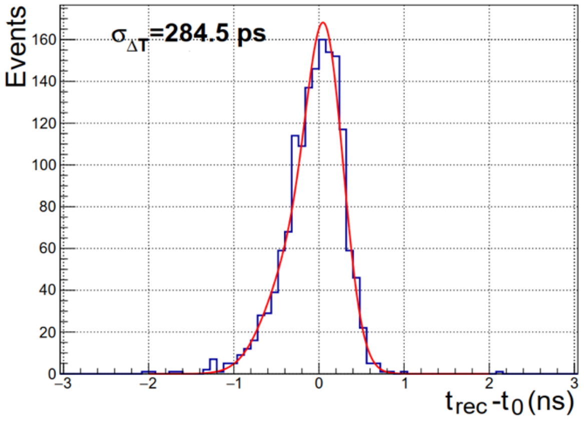
5×5 pCsI EMC Prototype

A pCsI EMC prototype

Performance from a beam test at CERN PS with 1 GeV/c electrons

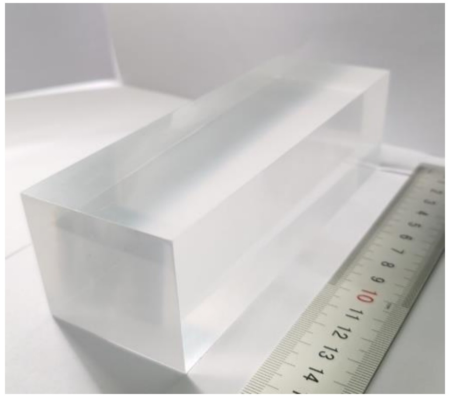


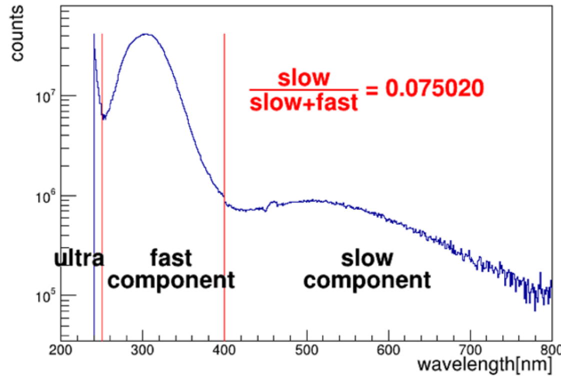




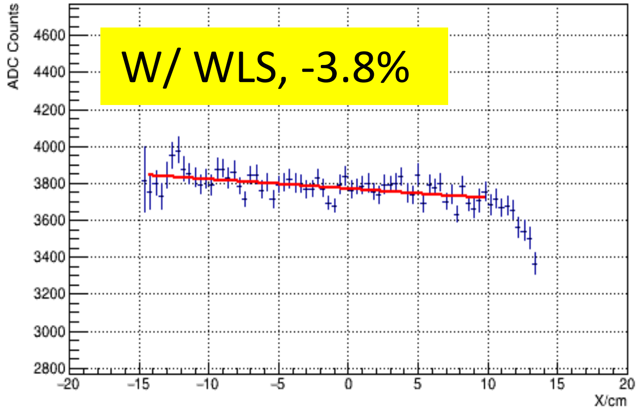
Optimizing the growth process of pCsI

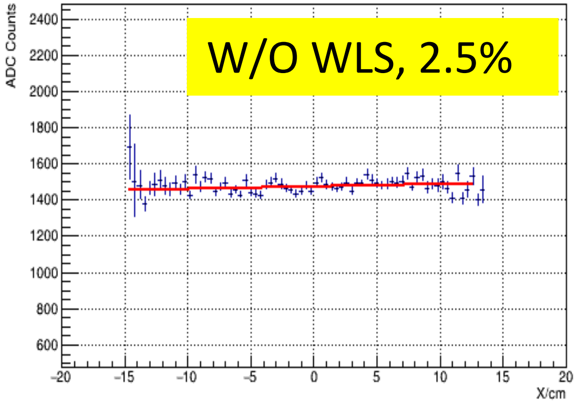
The long wavelength part ratio could be lower than 10%





Light collection uniformity Study

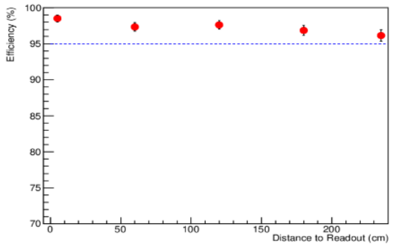


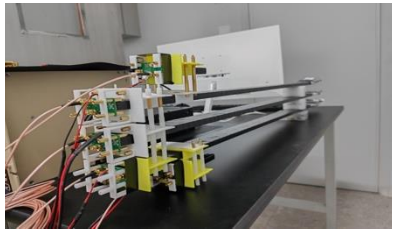


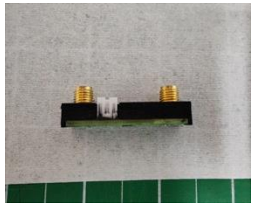
MUD R&D

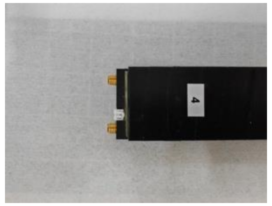
Scintillator strip + WLS + SiPM

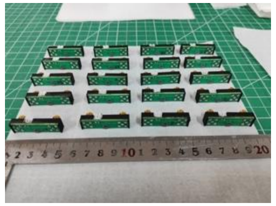
- Design and fabrication of the scintillator unit： reflector, fiber groove, optical coupling, surface processing.
- Fabricated 2.4m long scintillator units (efficiency>95%) and a 50×50 cm^2 scintillator strip array





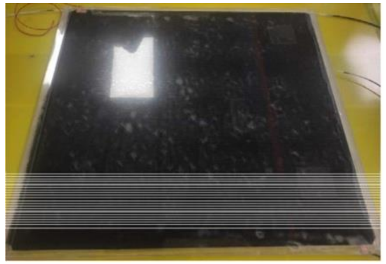


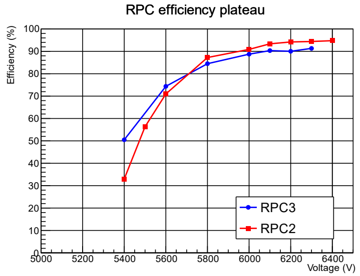




Glass RPC

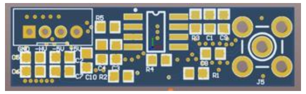
- Developed glass RPC fabrication techniques.
- Built small RPC prototypes (42×30 cm^2) with low-resistivity glass (1.5×10^9 Ω×cm) for high count rate capabilities. (Under test)
- Larger 140×40 cm^2 prototypes are being built.

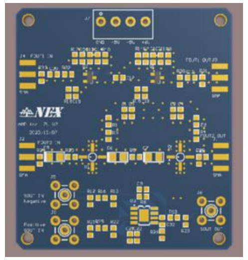


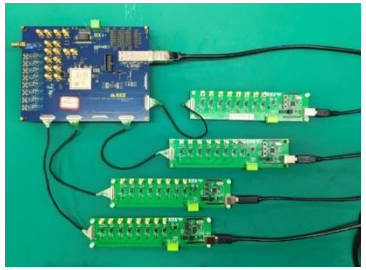


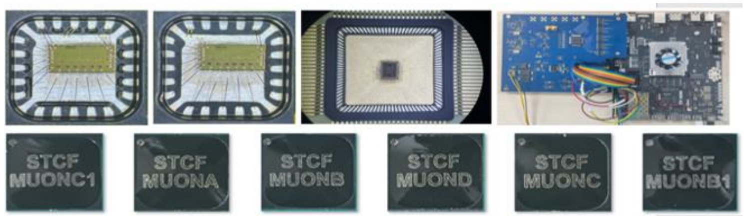
Readout Electronics

- Developed front-end amplifiers and readout boards. Tested with detector prototypes.
- Designed front-end ASICs for different input capacitance and gains. Prototype chips being tested



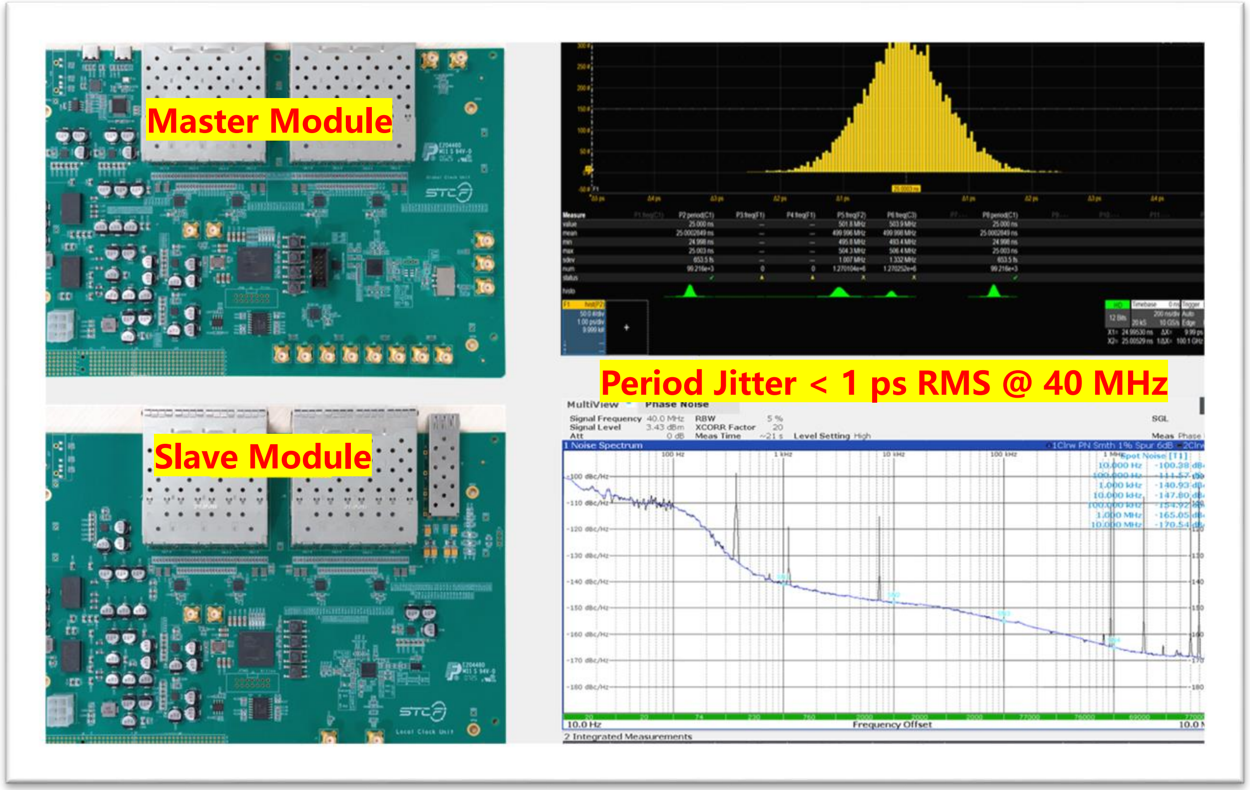


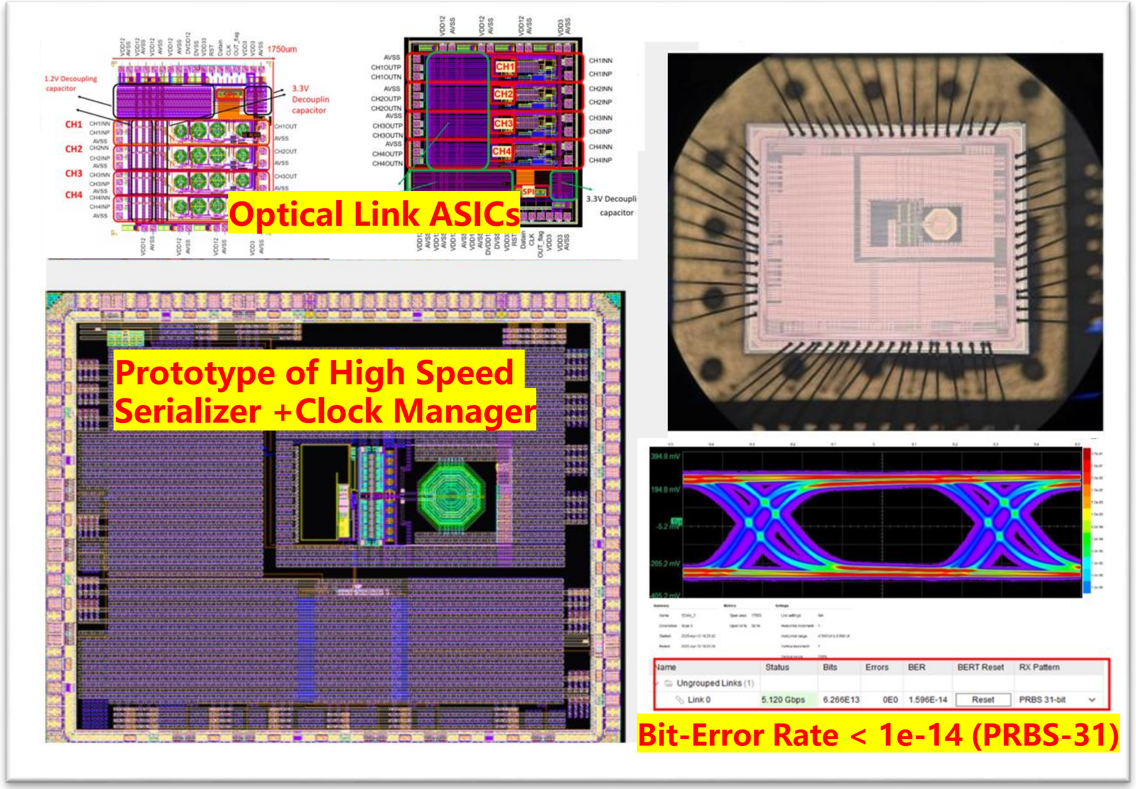




Clock and Data Transmission

- Clock distribution system provides precise and stable clock signals with jitter < 5ps RMS
- High-speed serial data transmission：a GBTx-like ASIC, ADTC, uplink ~5Gbps



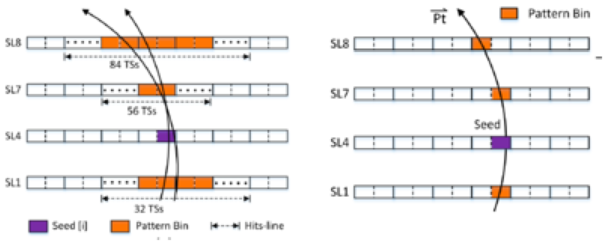


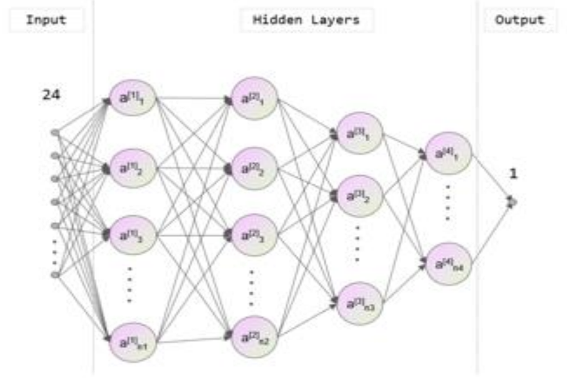
- Completed the design and test of clock distribution modules in a "master-slave" architecture
- Clock jitter tested ~1ps RMS
- joined the upcoming combined beam test

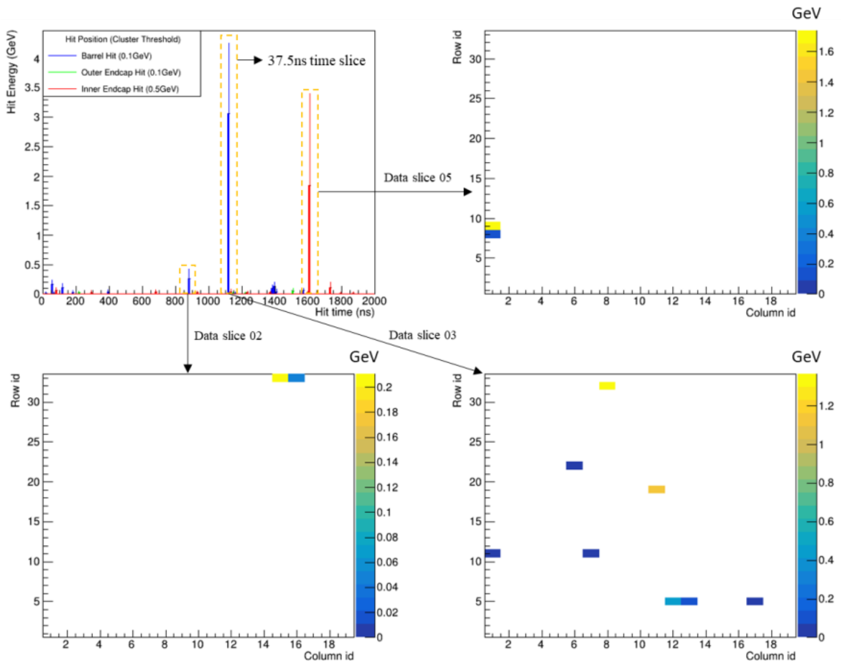
- Designed SerDes and clock managing modules in ADTC, and optical modules. Chips received and tested

Trigger : Algorithms Studies and Development

- **STCF trigger scheme： L1 (MDC, ECAL and global trigger) + HLT**
- **L1-MDC trigger algorithms: 2D track reconstruction (track finding and parameters (pt, θ, ϕ, t) estimation) using pattern matching , 2D short-track reconstruction incorporating stereo layers using NN, Z impact parameter estimation using NN**
- **L1-ECAL trigger algorithms : overlapping events resolving, cluster reconstruction and splitting (E, θ, ϕ, t)**
- **L1 global trigger : track and cluster matching, event T0 estimation, trigger menus for charged and neutral channels**
- **HLT : currently focusing on MDC HLT aiming to remove noise hits and reduce event size**





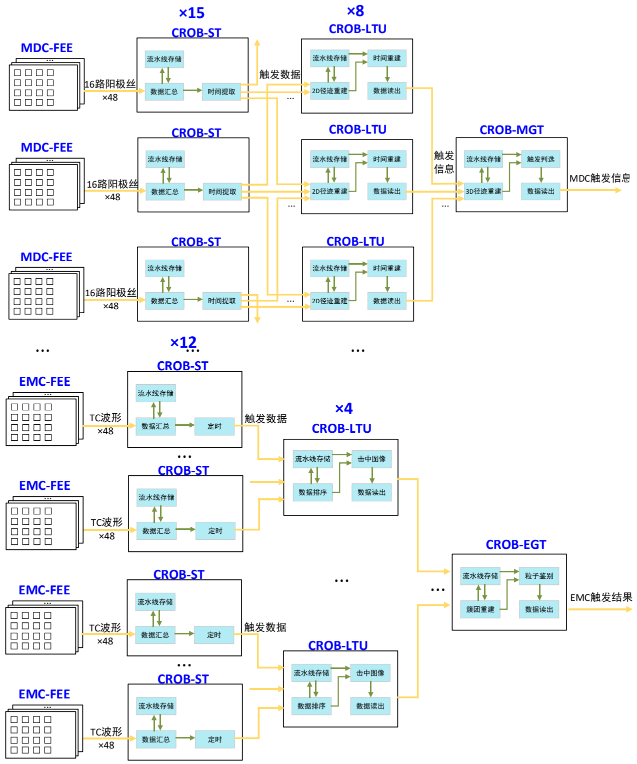


Background trigger rate < 30 kHz

Trigger channel	Physics signal	Energy point	Background trigger rate(kHz)	Signal trigger rate
Charged channel	J/psi -> inclusive	3.097GeV	26.5	98.2%(99.0%)
	e^+e^- -> $\pi^+\pi^-$J/psi Jpsi -> e^+e^-	4.26GeV	18.9	99.4%
	e^+e^- -> $\pi^+\pi^-$J/psi Jpsi -> $\mu^+\mu^-$	4.26GeV	27.4	99.8%
	e^+e^- -> $\tau^+ \tau^-$	4.26GeV	22.8	98.7%
	e^+e^- -> $\pi^+\pi^-$J/psi J/psi -> $\Lambda \bar{\Lambda}$	3.097GeV	18.5	99.3%
	e^+e^- -> $\pi^+\pi^-$J/psi J/psi -> $\Xi \bar{\Xi}$	3.097GeV	26.0	99.1%
	e^+e^- -> K^+K^-J/psi J/psi -> l^+l^-	4.682GeV	18.7	99.9%
	e^+e^- -> $D_0 \overline{D_0}$	3.773GeV	25.2	100%
	e^+e^- -> $D^+ D^-$	3.773GeV	19.3	100%
	e^+e^- -> $D_s^+ D_s^-$	4.04GeV	26.7	100%
Neutral channel	J/psi-> gam invisable	3.097GeV	24.8	99.4%
	e^+e^- -> n nbar	3.097GeV	25.5	97.6%
	e^+e^- -> gam n nbar	3.097GeV	26.0	98.2%
	e^+e^- -> gam n nbar(ISR)	3.713GeV	27.3	98.4%
Luminosity monitor	Bhabha Scattering	4.26GeV	0.63%	97.8%

Trigger : Hardware Development

- Design of trigger hardware architecture. Development of various core trigger hardware components (CROB-ST, CROB-LTU, CROB-MGT/EGT, CTM, FMC …) . FPGA implementation of L1 trigger algorithms.
- A prototype L1 trigger system has been designed and built to demonstrate the trigger system design and its performance. An event simulator has been developed to generate pseudo data for the prototype trigger system.
- The prototype system has participated in the recent combined beam test at CERN

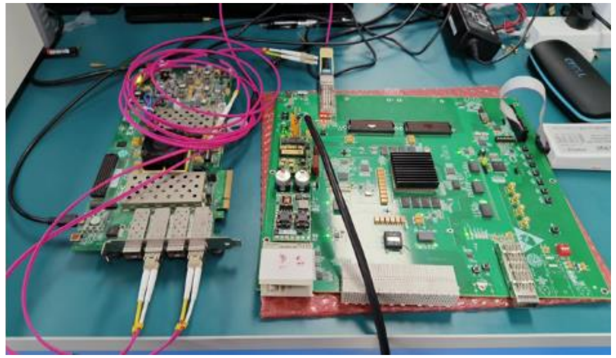


CROB-LTU board

Data processing board

FMC+ board

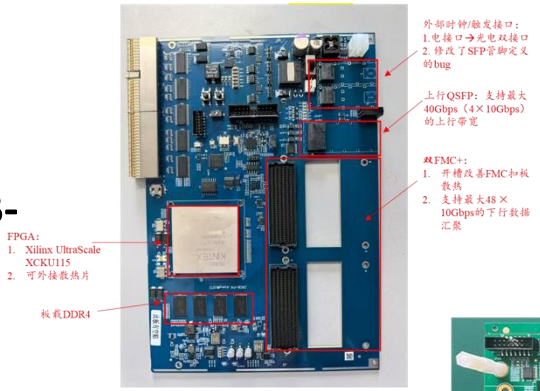
CTM board



DAQ Design and Development

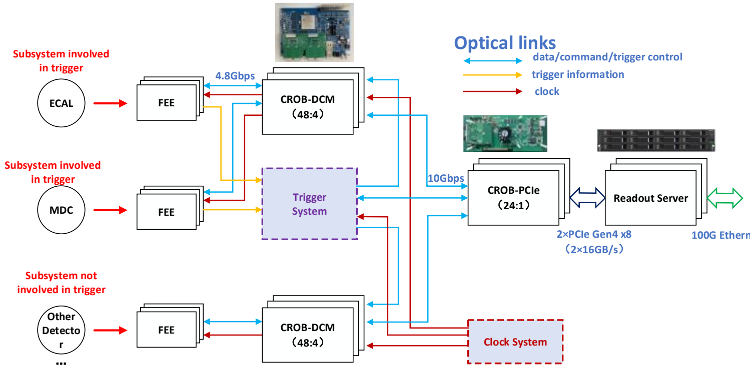
- System architecture based on Data-Matrix: flow processing, heterogeneous computing, standard interfaces and protocols, global pipeline
- Core electronics boards design completed: CROB-PXI V3.0, CROB-PCIe V2.0, FMCP optical interface board
- Software and firmware development completed
- System testing and performance evaluation using simulation data
- A prototype DAQ system has participated in multiple combined beam tests

CROB-PXI board

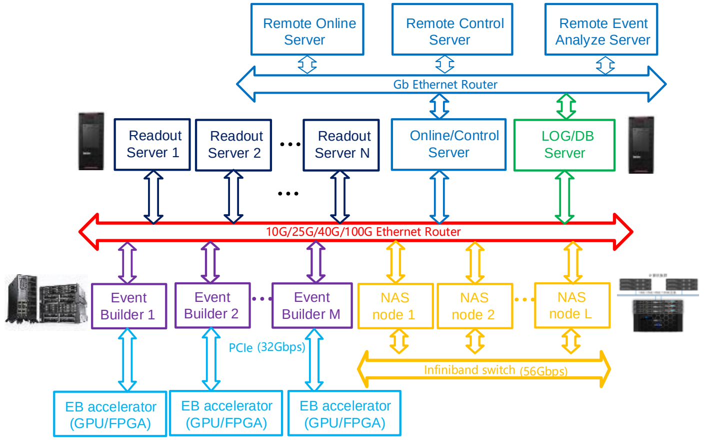


FMCP optical interface board

CROB-PCIe board



FPGA Processing Layer



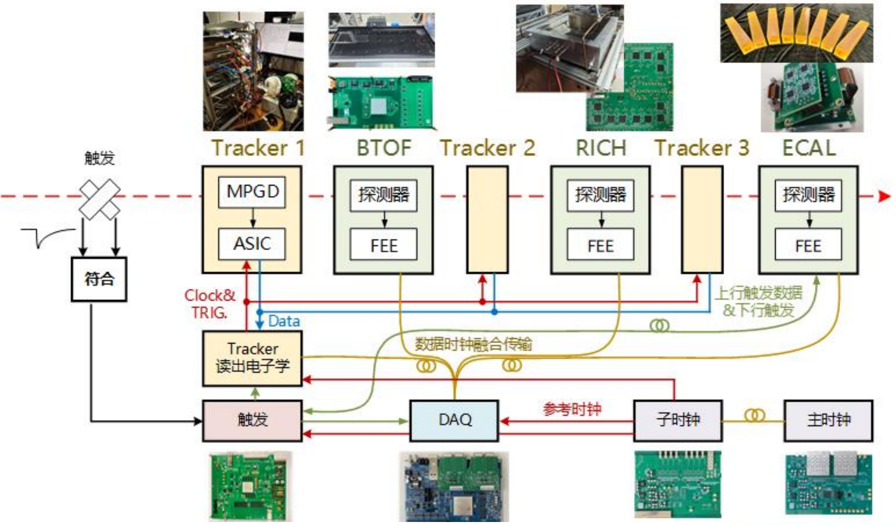
Software Processing Layer

Test of event building

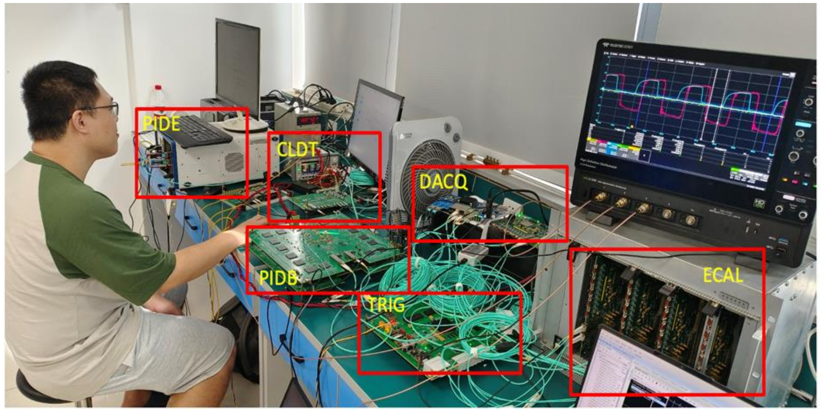
- 12 rack servers
  - 9 servers: readout+ 4 event builders
  - 3 servers: 4 event builders
- 33 simulated data sources
  - 17 big-frame sources: 20~32kB/frame
  - 16 small-frame source: 135 Byte/frame
- Software optimization
  - event building rate: 20 kHz → 90kHz

Second Combined Beam Test

- **Launched the second test beam campaign this year for a large combined system (ITK, RICH, BTOF, EMC, Clock, Trigger, DAQ)**



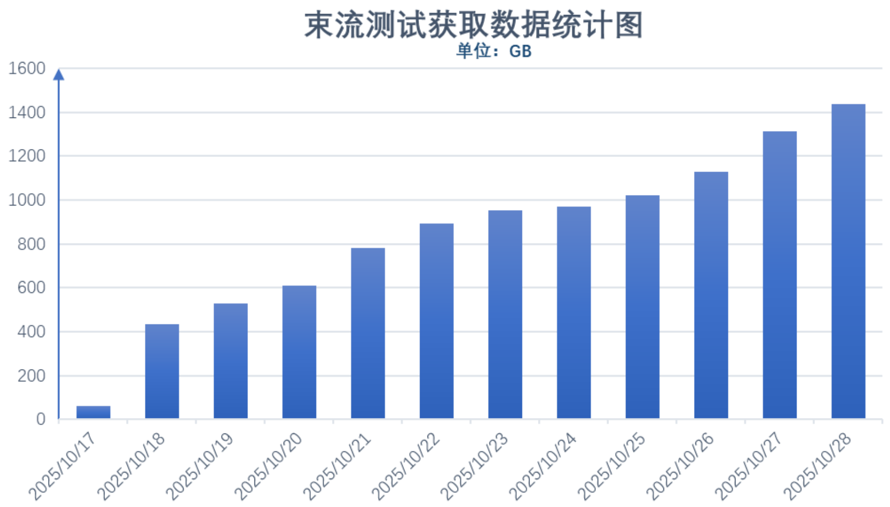
Laboratory test

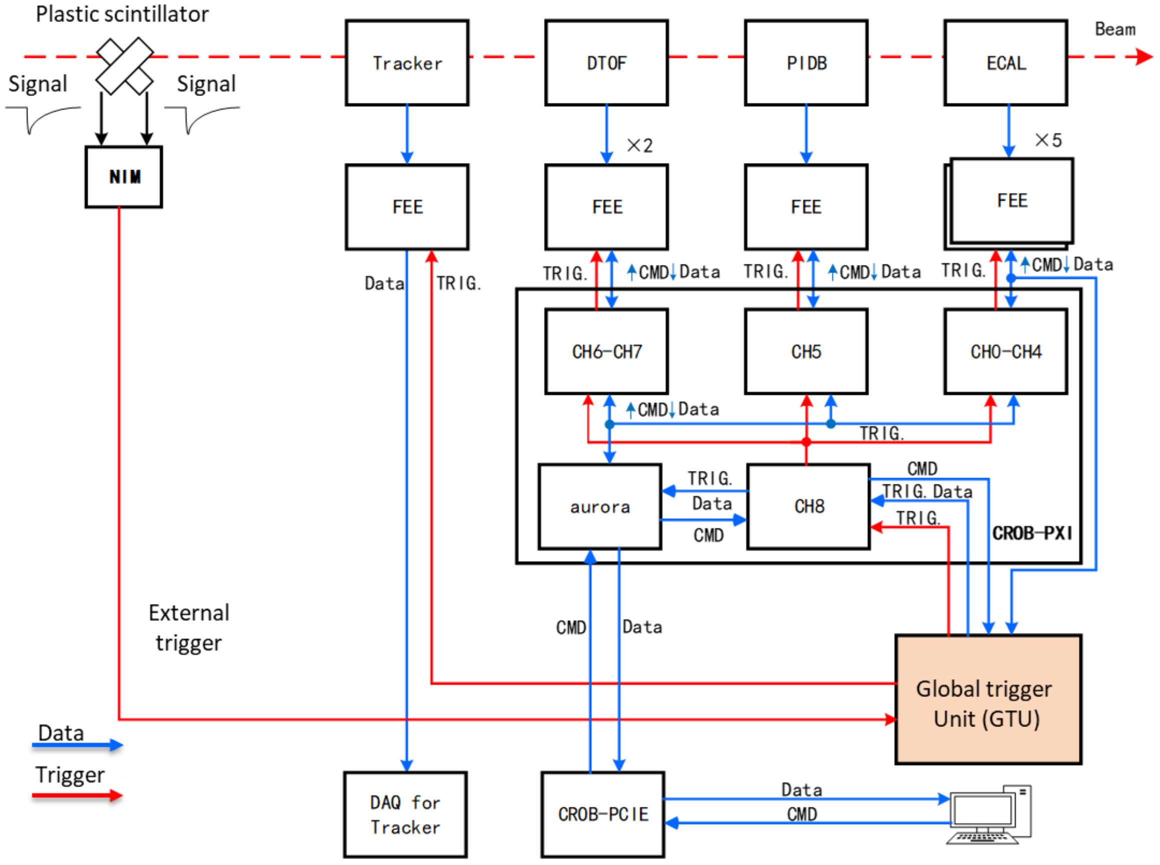


CERN PS T9 in Oct. 2025

Trigger and DAQ in Beam Test

- **Full trigger chain verified with GBT link to RICH, ECAL and DAQ implemented**
- **high ECAL triggering efficiency achieved with a latency of 1.3 µs**
- **DAQ worked well with a total data volume of 1.4 TB accumulated**

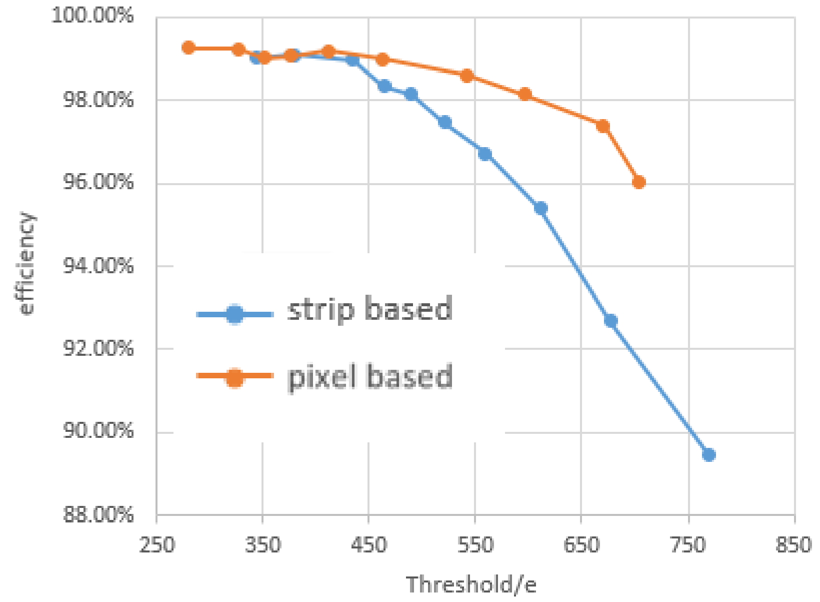




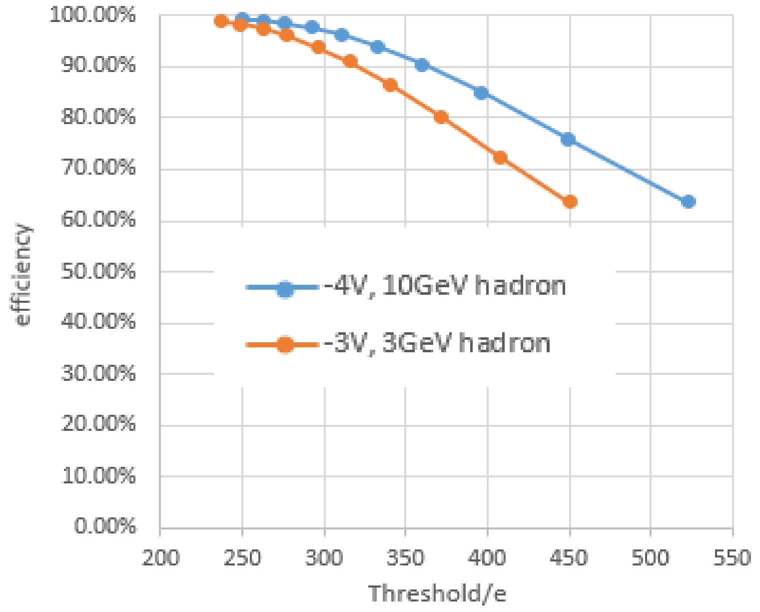
ITKM Preliminary Results

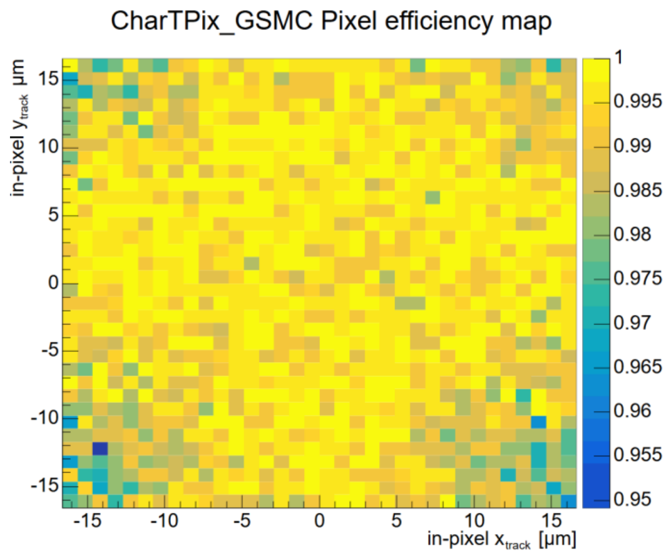
- Track reconstruction and data analysis based on the Corryvreckan software
- Preliminary results on the detection efficiency, spatial and timing resolution

CharTPix-180nm, sub=-6V, 10 GeV hadrons



CharTPix-130nm



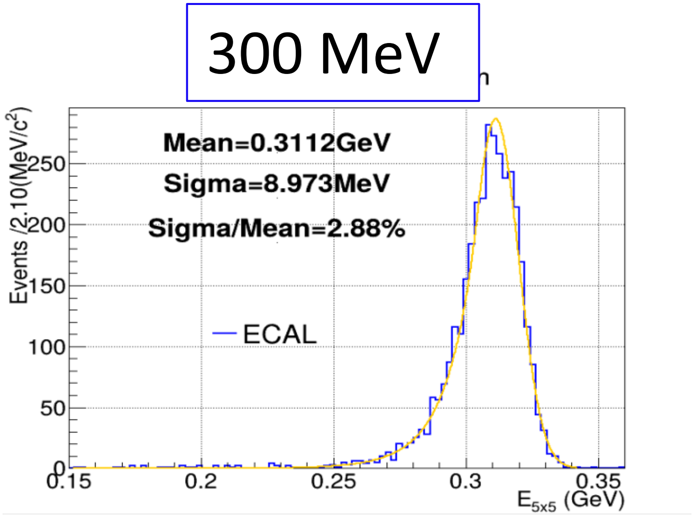


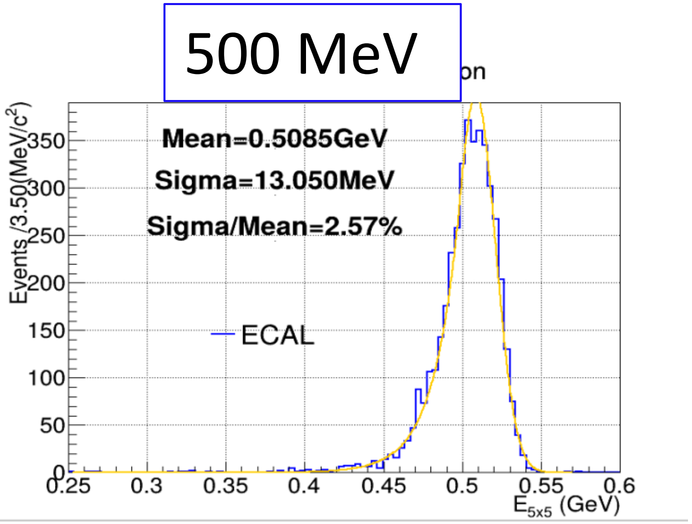
- Efficiency higher than 99% at low thresholds and remains high at higher thresholds
- Spatial resolution: ~50 (10) um in the long (short) pitch
- Timing resolution ~60ns

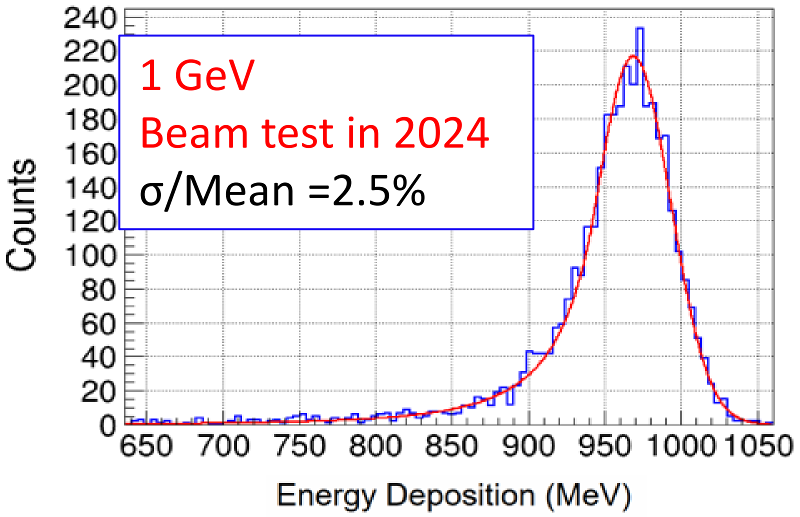
- Efficiency higher than 98% at low thresholds and drops quickly
- Spatial resolution: ~7um

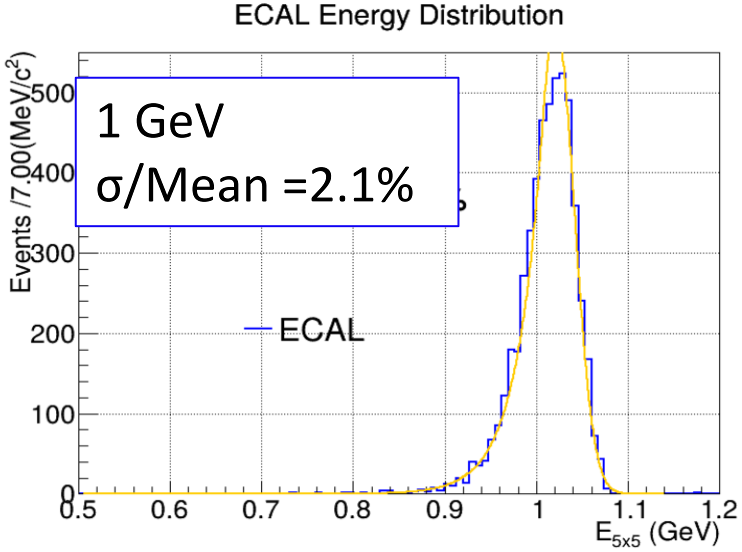
ECAL Preliminary Results

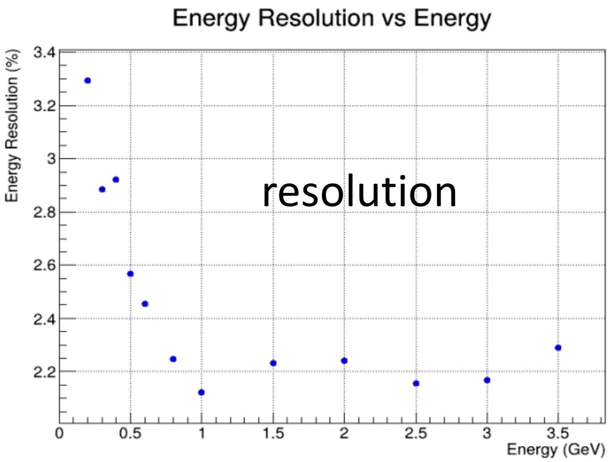
- **Tested using electrons with energy ranging from 200 MeV to 3.5 GeV**
- **Good energy resolution achieved**







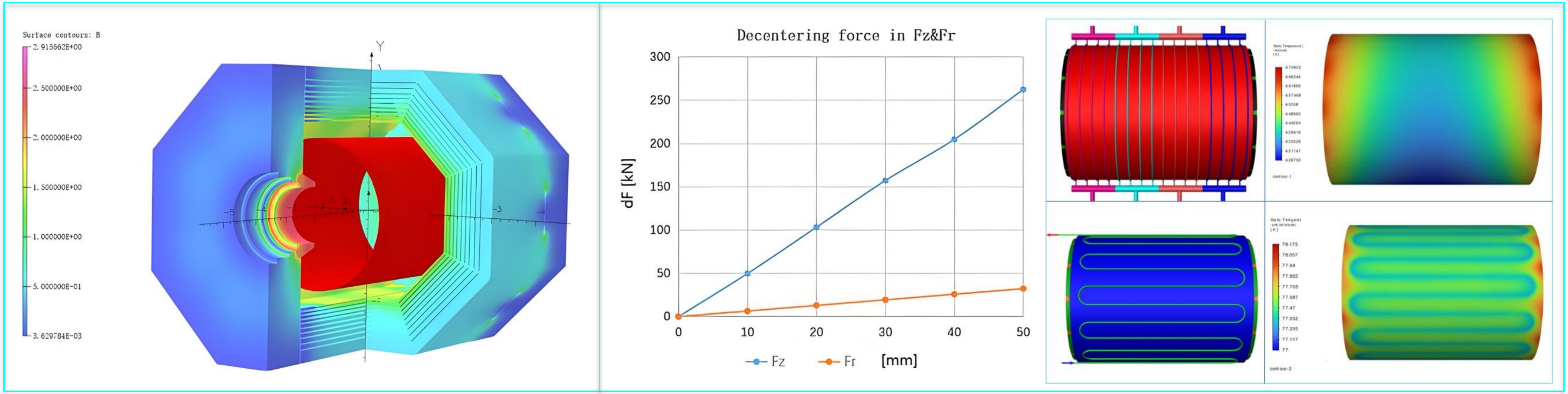




Data analysis is ongoing. More results will come out soon for other detectors

Superconducting Solenoid Magnet

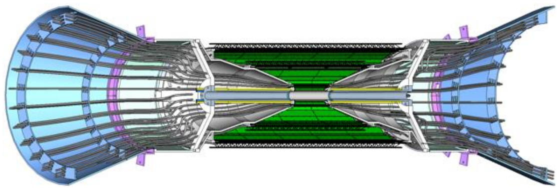
- Optimized the physics design of the magnet by performing FEA of magnet field and decentering forces.
- Studied impact of inhomogeneity of the magnetic field on tracking performance and solutions for shielding stray magnetic fields.
- Designing the magnet support structure using carbon fiber. Investigating heat leakage issue.
- Studying cryogenic forced flow (77K)and thermosiphon (4.2K) schemes with FEA.



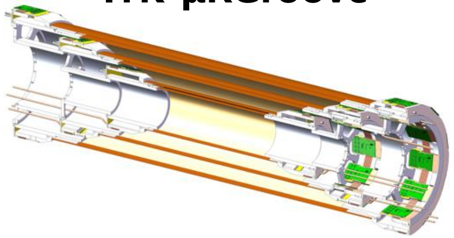
Detector Mechanical Design

- Detector conceptual design has been transferred into engineering drawings
- Engineering design available for each sub-detector or system
- Design studies on detector assembly and installation

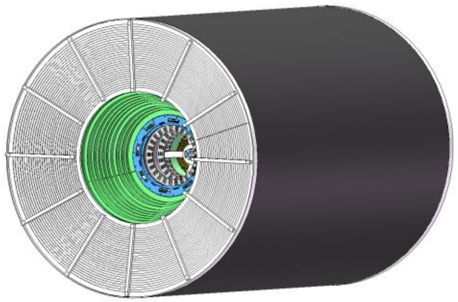
ITK-MAPS



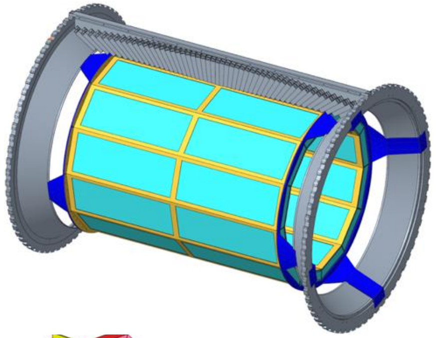
ITK-µRGroove



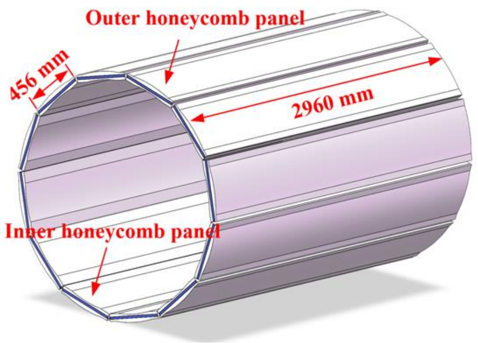
MDC



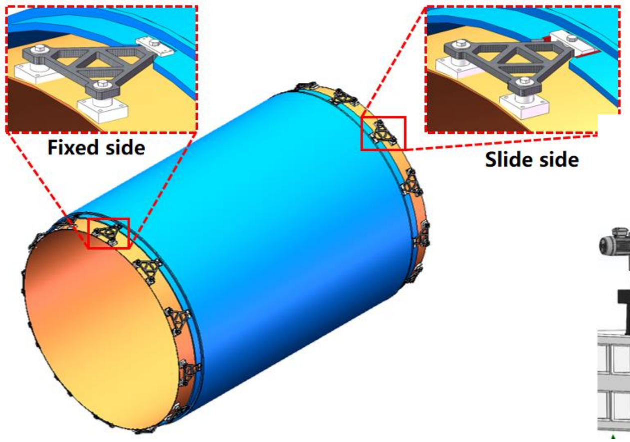
RICH



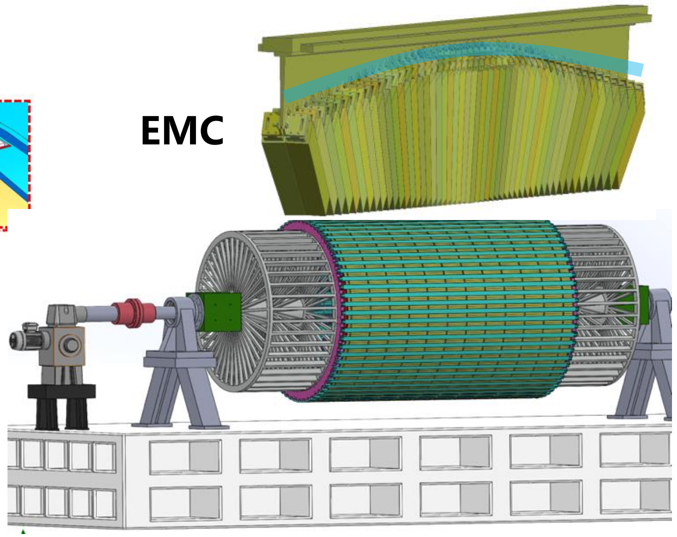
BTOF

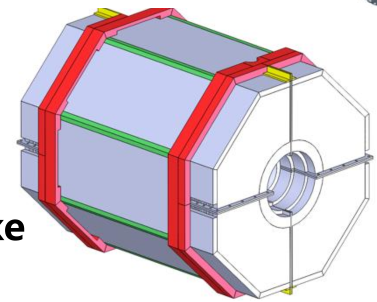


Superconducting magnet

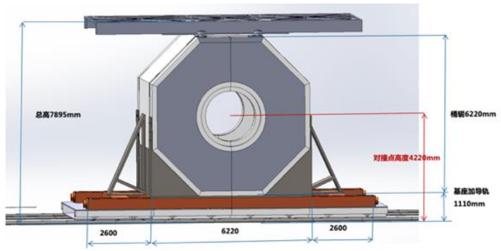


EMC

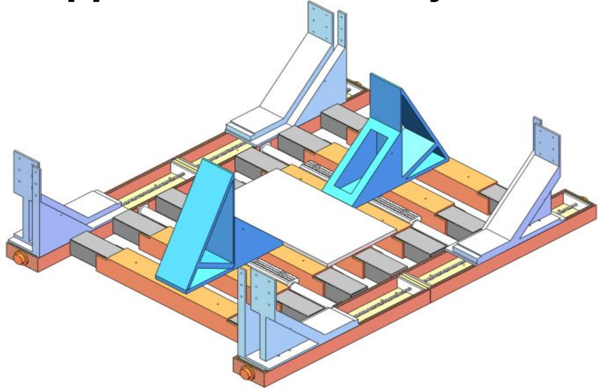




Iron Yoke



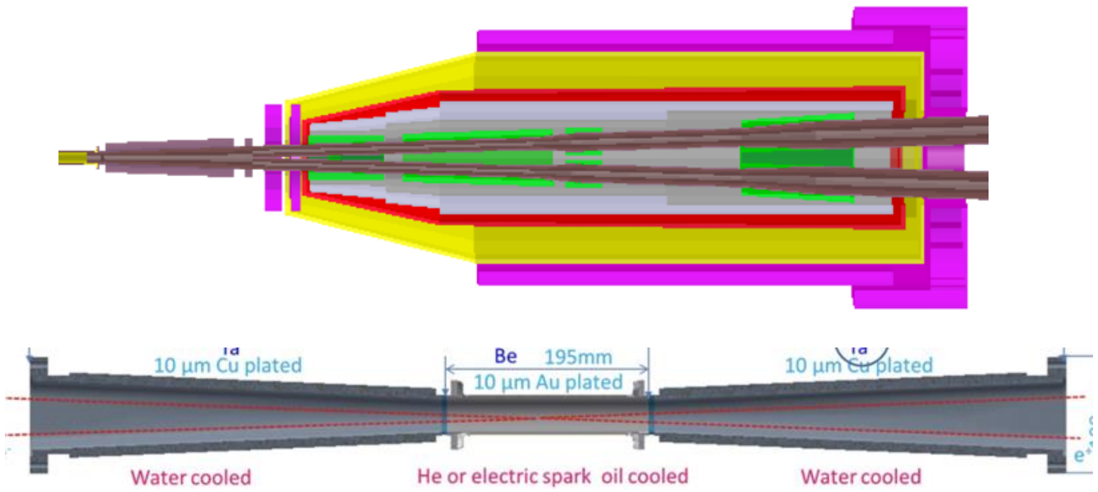
Support and Mobile System

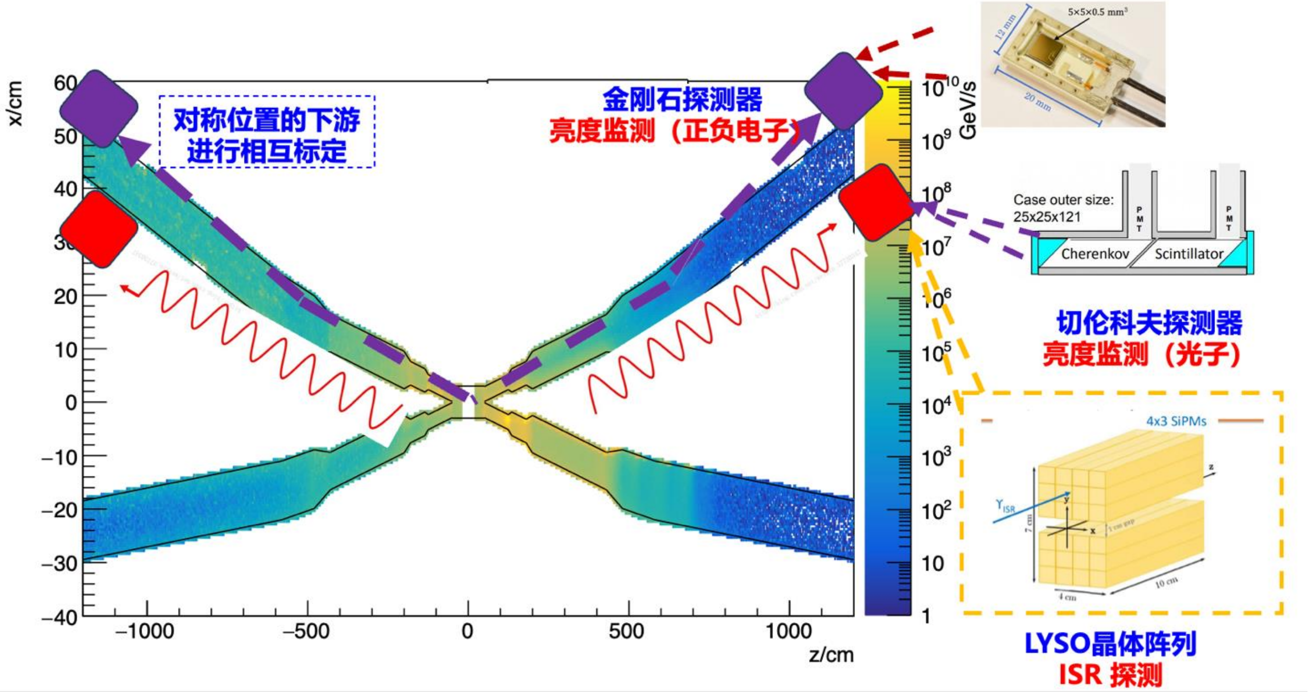


Beam Background and Forward Detectors

- **Keeping up with accelerator design evolution for beam background estimation. Working closely with MDI people to optimize the detector geometry and radiation shielding design in MDI region.**
- **Simulation studies on luminosity detectors (radiative Bhabha) and zero-degree detectors (ISR, two-photon process). Preliminary determination of the sites of these detectors at STCF from these studies.**

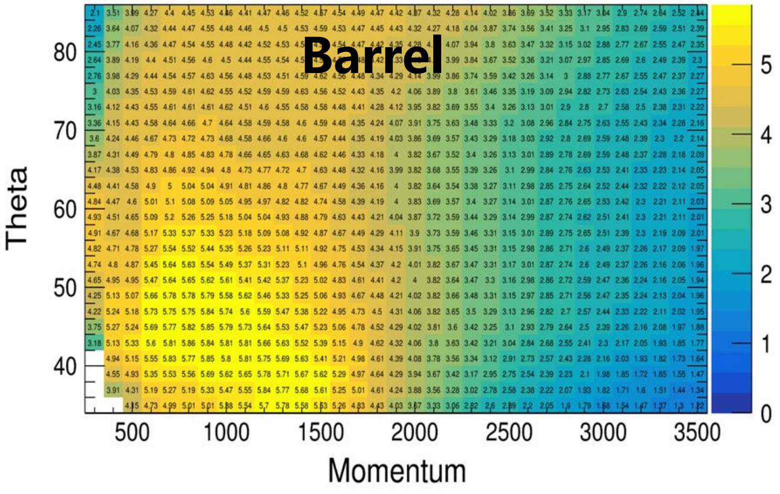
MDI

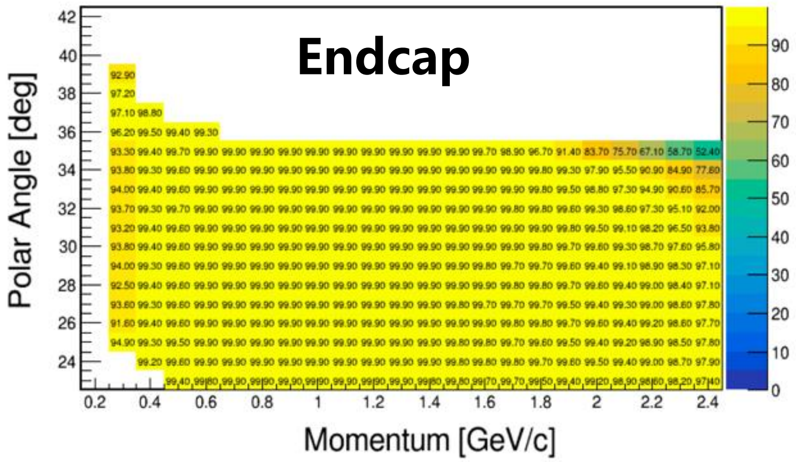




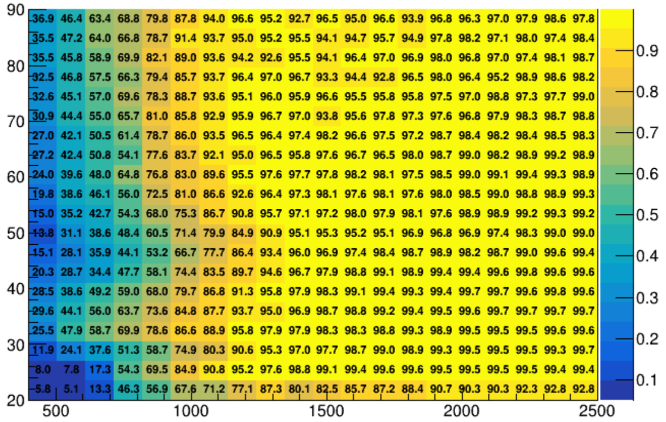
STCF Detector Performance with Full Simulation

PID: π/K ~4σ @ 2 GeV



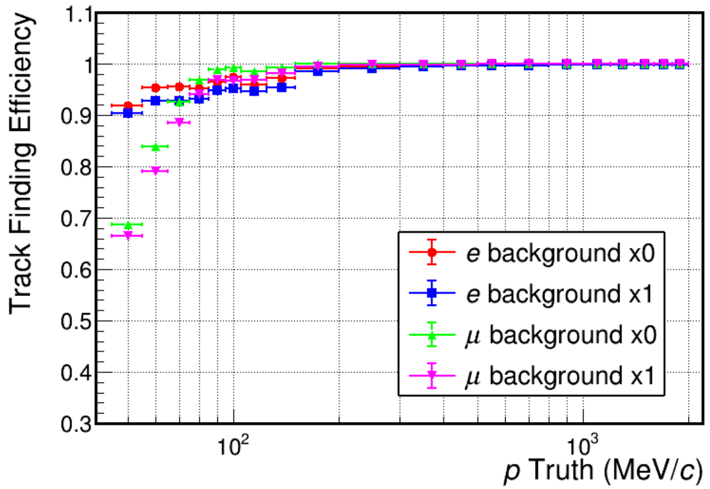


Muon ID eff. @ pi suppression=30

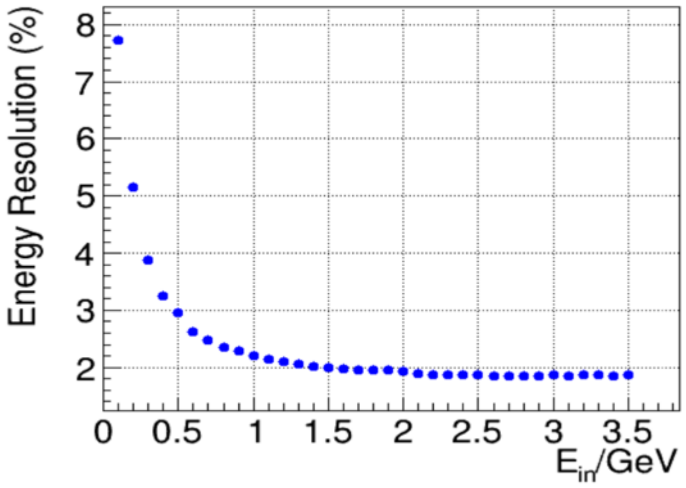


eff. ~> 90% when p ~>1GeV/c

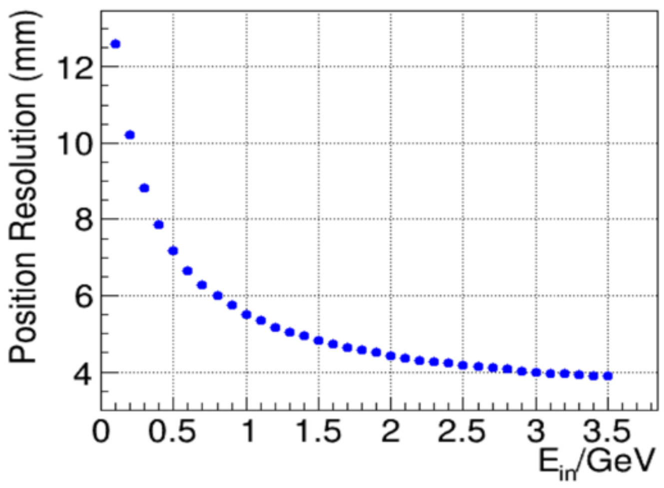
Tracking efficiency



EMC energy resolution

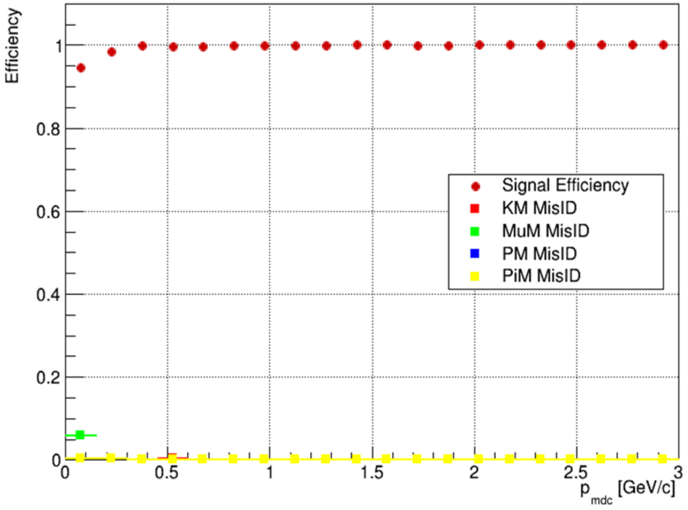


EMC position resolution

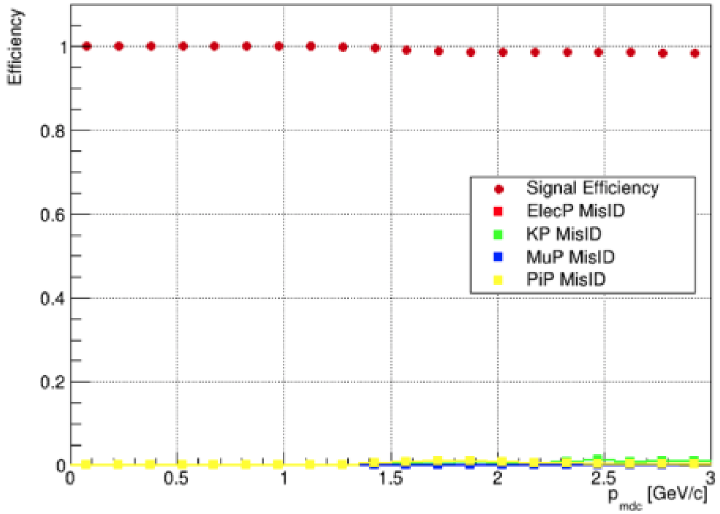


Global PID Performance

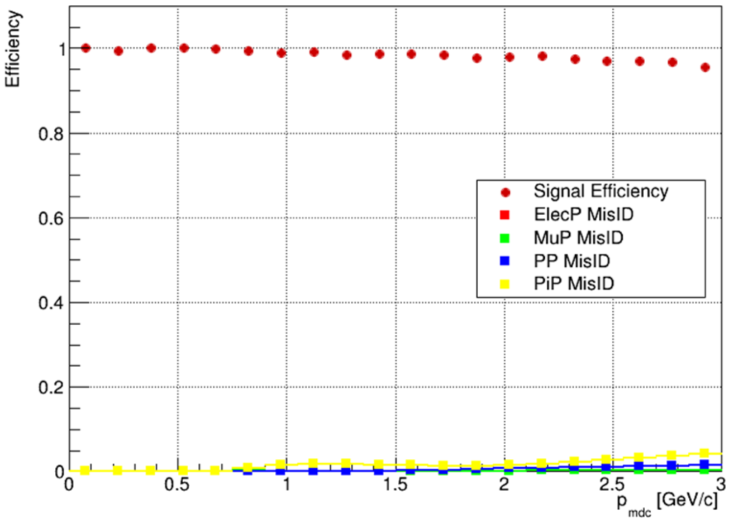
e identification against K/μ/p/π



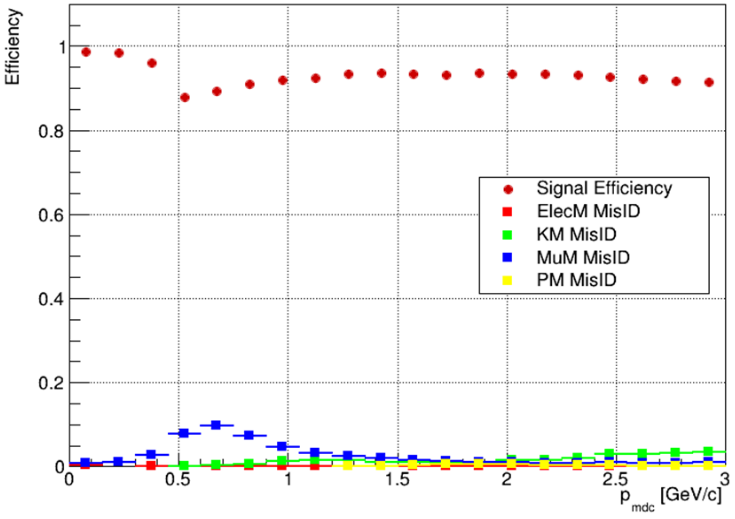
proton identification against e/K/μ/π



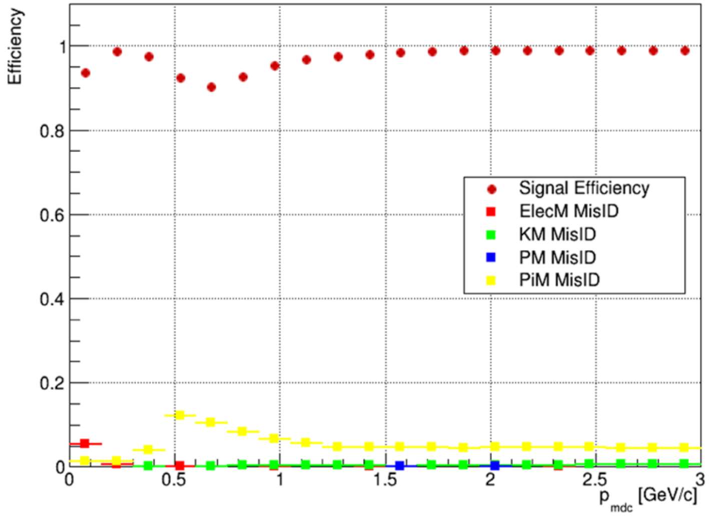
K identification against e/μ/p/π



π identification against e/K/μ/pi



μ identification against e/K/p/pi



Final Remarks

- **A very comprehensive STCF detector R&D project has taken shape and is being vigorously executed.**
- **Enormous progress has been made in many aspects of the project and on many sub-detectors or systems. Some sub-detectors have reached the large-scale prototype level.**
- **A beam test at CERN of a fully integrated system of EMC + BTOF + RICH+ Clock + Trigger + DAQ has been conducted at CERN this October.**
- **Detector performance has been evaluated with full simulation and can meet physics requirements. Many sub-detectors have been optimized with full simulation. More are underway to further enhance the detector capability.**
- **International collaboration has been expanded and substantiated (LHCb-TORCH, BINP-ASHIPH/MDC), and continues to be an important goal of STCF.**
- **STCF detector TDR is in preparation and will come out soon.**