



中国科学技术大学  
University of Science and Technology of China



超级陶粲装置  
Super Tau-Charm Facility

# STCF实验硅像素内径迹探测器 研究进展

宾心瑜

(代表STCF ITK-MAPS工作组)

**超级陶粲装置研讨会**

2025年7月3日 湘潭



❖ 研究背景

❖ STCF MAPS原型芯片设计

❖ TJ第一版MAPS测试

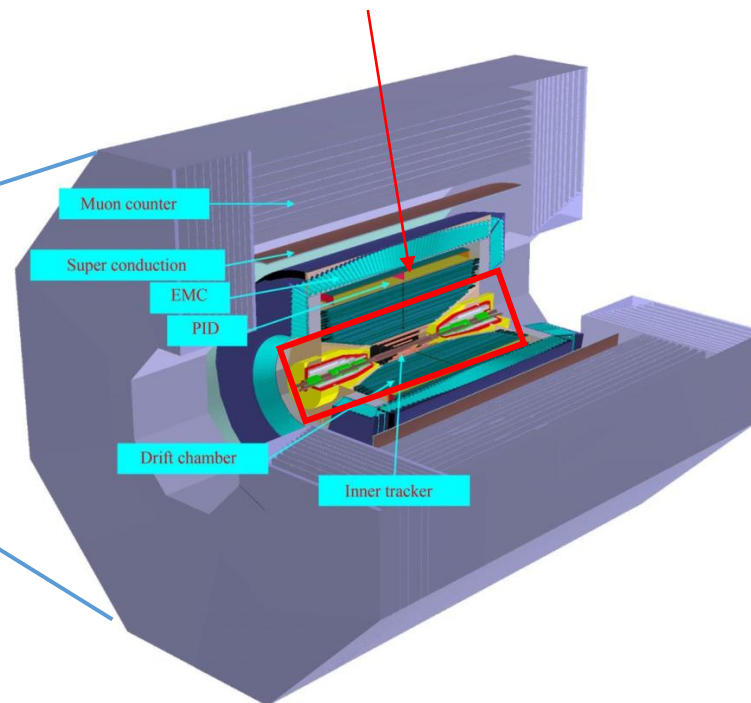
❖ 模块组装设计

## ❖ 超级陶粲装置(Super Tau-Charm Facility, STCF)

- 国内新一代正负电子对撞机
- 质心能量 $2\sim 7$  GeV, 亮度 $>0.5\times 10^{35}\text{cm}^{-2}\text{s}^{-1}$ @4 GeV
- 具备进一步提升峰值亮度和实现束流极化的潜力



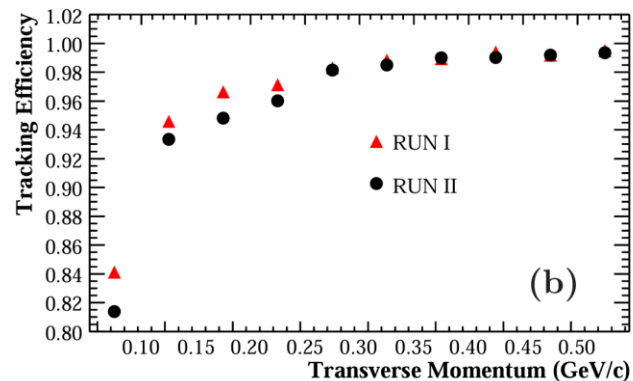
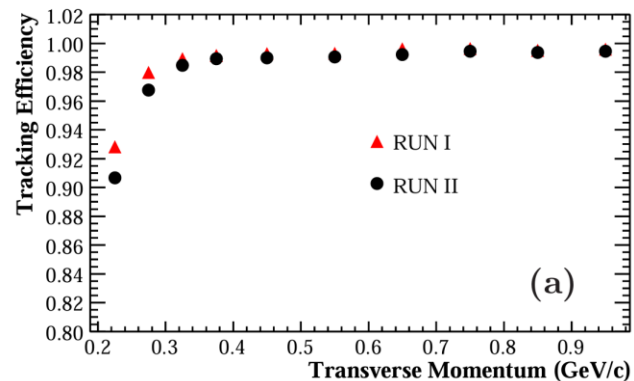
MAPS为STCF ITK方案之一



### ❖ STCF物理目标

Process	Physics interest	Optimized subdetector	Requirements
$\tau \rightarrow K_s \pi \nu_\tau$ ,	$CPV$ in the $\tau$ sector,	ITK+MDC	Acceptance: 93% of $4\pi$ ; Trk. Effi.: <div style="border: 2px solid red; padding: 2px;"> <math>&gt; 99\%</math> at <math>p_T &gt; 0.3 \text{ GeV}/c</math>; <math>&gt; 90\%</math> at <math>p_T = 0.1 \text{ GeV}/c</math>,  <math>\sigma_p/p = 0.5\%</math>, <math>\sigma_{\gamma\phi} = 130 \mu\text{m}</math> at <math>1 \text{ GeV}/c</math> </div>
$J/\psi \rightarrow \Lambda \bar{\Lambda}$ ,	$CPV$ in the hyperon sector,		
$D_{(s)}$ tag	Charm physics		

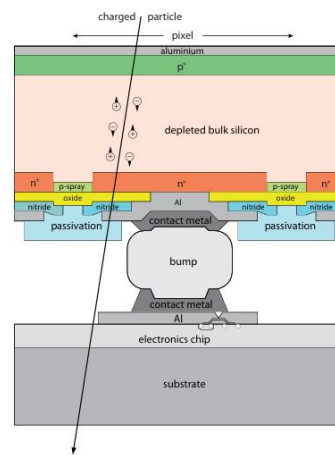
- 低动量能区粒子径迹探测的挑战
  - 多次库仑散射，径迹探测效率低
  - BESIII的径迹重建效率在100MeV迅速降低



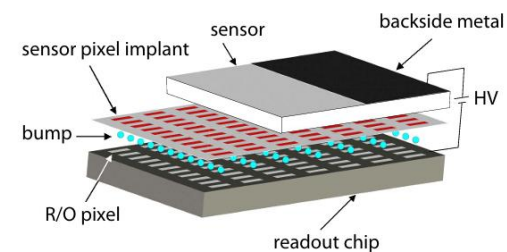
BESIII tracking efficiency,  
Chin.Phys.C 40 (2016) 2, 026201

## ❖ Hybrid

- Sensor和电子学分别优化设计；抗辐照能力强
- ATLAS/CMS采用
- 缺点：物质量大；键合工艺复杂、成本高



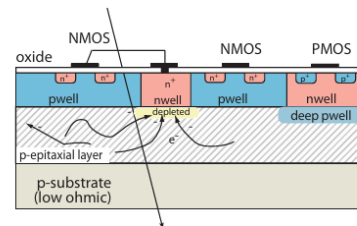
(a) Hybrid pixel



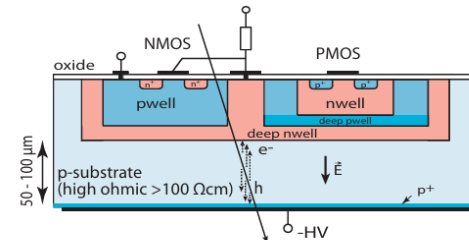
(b) Pixel matrix

## ❖ Monolithic

- 仅需单层硅片，低物质质量
- 易集成，低成本
- STAR/ALICE ITS2采用
- 缺点：抗辐照能力弱、电荷收集时间相对较长



(a) MAPS



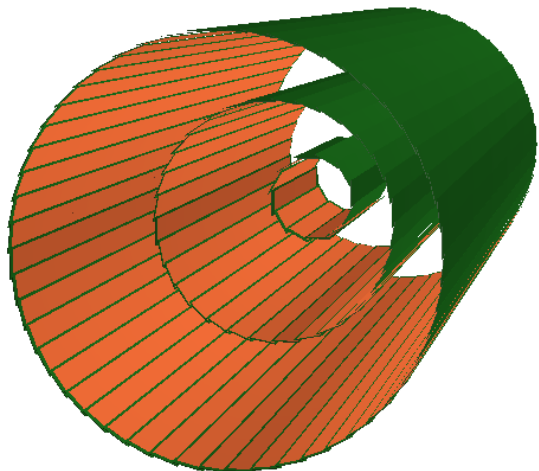
(b) DMAPS

[arXiv:1705.10150](https://arxiv.org/abs/1705.10150)

### 中科大、山大、华师、西工大合作研究

#### ❖ MAPS设计需求

- 位置分辨:  $\leq 100 \mu\text{m}$
- 物质量: 单层 $\leq 0.3\% X_0$
- 功耗:  $\leq 100 \text{ mW/cm}^2 \rightarrow 50 \text{ mW/cm}^2$
- 时间分辨:  $\leq 20 \text{ ns}$  (去堆积)
- 能量测量 (ToT)
  - time walk修正、多次散射修正
- Hit rate  $1\text{MHz/cm}^2$ , TID  $1\text{Mrad/y}$ , NIEL  $1 \times 10^{11} n_{\text{eq}}/\text{cm}^2/\text{y}$



Layer	半径	Stave数量	Stave全长	Chip数量
1	36mm	16	200.75mm	6
2	98mm	12	592.25mm	72
3	160mm	20	954.55mm	120

#### ❖ 探测器结构初步设计:

- 三层探测器
- 接收角度范围 $20^\circ \sim 160^\circ$
- 单芯片尺寸:  $2 \text{ cm} \times 2 \text{ cm}$
- 3360块芯片
- 总面积:  $\sim 1.5 \text{ m}^2$



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## 在四种不同工艺下开展MAPS芯片设计

TJ180nm

国外成熟工艺

低阻衬底+高阻外延 (>1kΩ·cm)

四阱工艺

GSMC130nm

国内工艺

高阻衬底

四阱工艺

BCIS90nm

国内工艺

低阻外延 (<10Ω·cm)

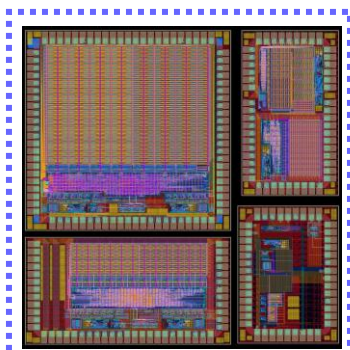
预期实现四阱

IRAY180nm

国内工艺

联系到高阻外延层

预期实现四阱

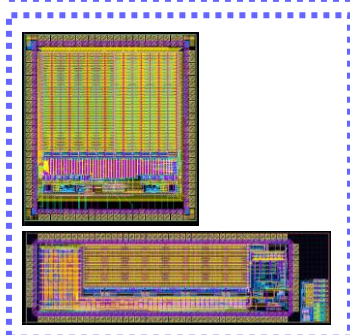


CharTPix-TJ-v0.1  
2024.12回片  
已完成部分测试

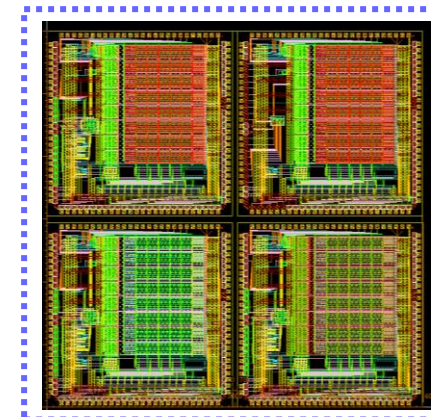
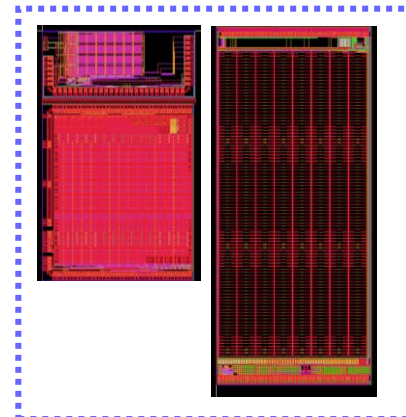
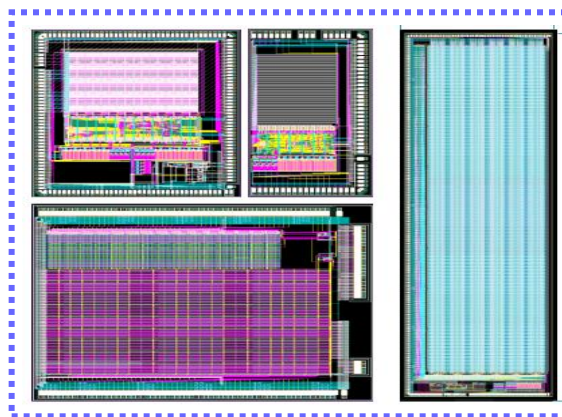
CharTPix-GSMC-v0.1  
2025.6回片  
准备测试中

CharTPix-BCIS-v0.1  
2025.1提交流片  
2025.6回片  
准备测试中

CharTPix-IRAY-v0.1  
2025.5提交流片



CharTPix-TJ-v0.2  
提交中



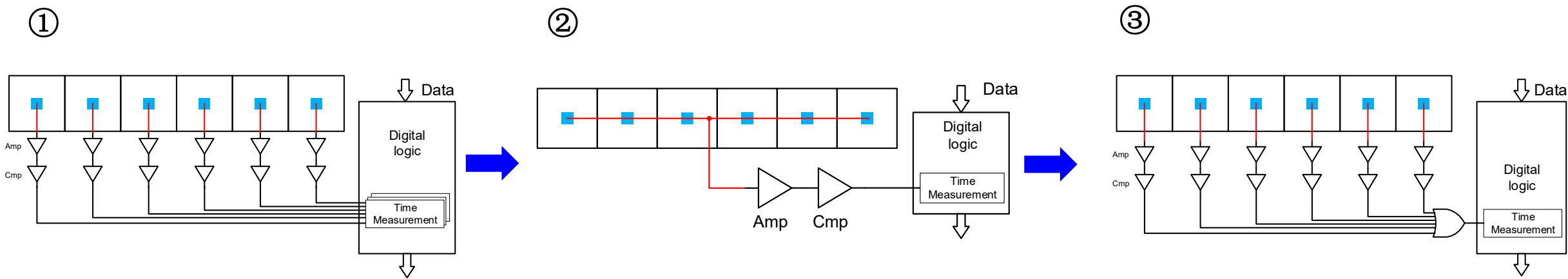




# 精度提升考虑



- ❖ 高精度位置分辨和时间分辨提供更多的可能
- ❖ 提出基于**超级像素**的新型读出架构



## 传统定时MAPS

- ✓ 小像素→定时快、噪声小
- ✓ 读出通道多→功耗高

## TJ & FCIS/BCIS MAPS

- ✓ 大像素→定时较慢、噪声较高
- ✓ 读出通道少→功耗低

## 基于超级像素读出的MAPS

- ✓ 小像素→定时快、噪声小
- ✓ 读出通道少→数字功耗低

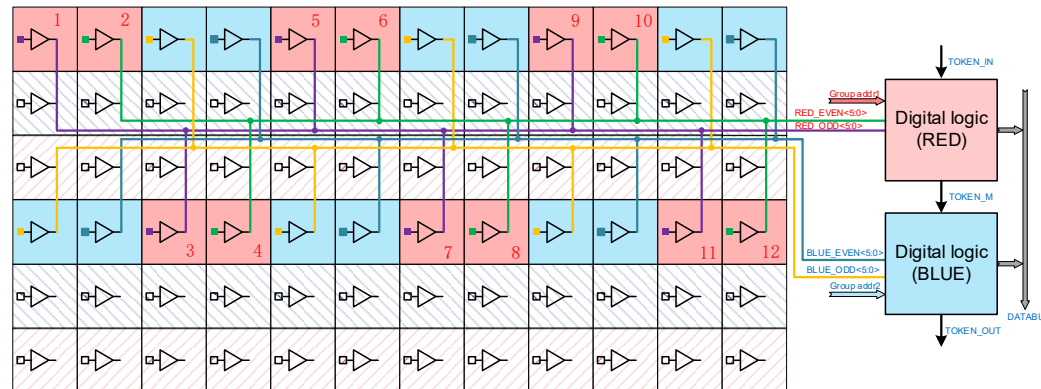
# CharTPix-TJ-v0.2读出电路



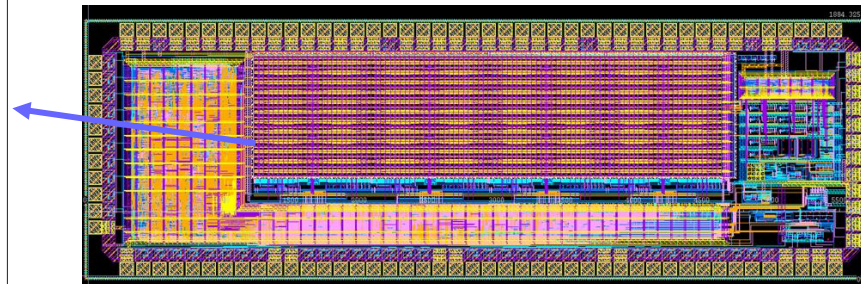
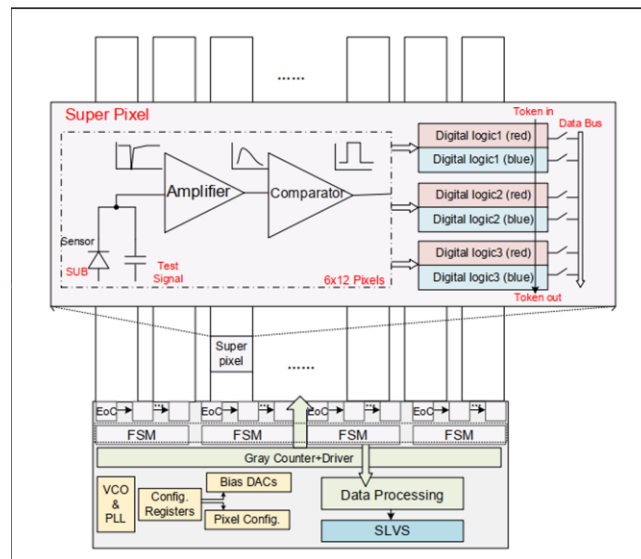
## ❖ Super pixel: 最小可重复Layout单元

- 规模: 6×12 pixels
- Cluster area 小于 3×4 pixels 时, 不损失 hit 信息

同时提供高精度位置分辨和高精度时间分辨

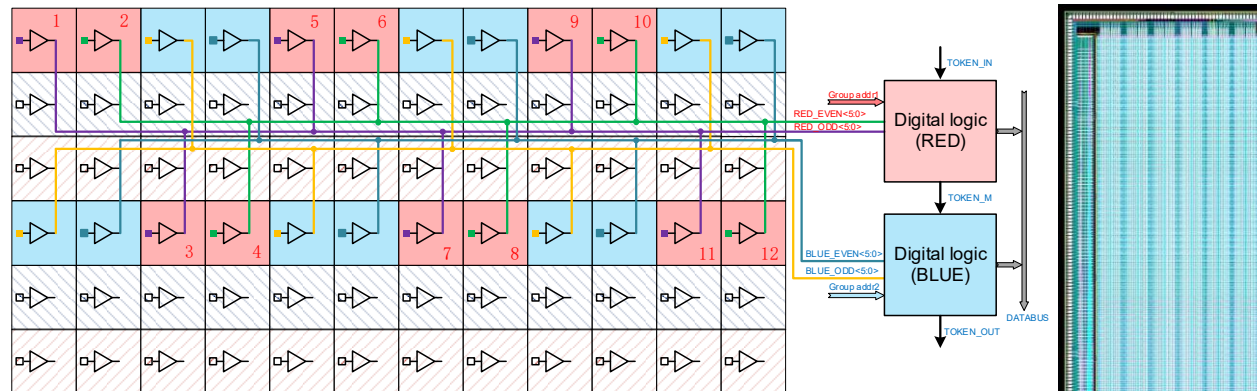


- 芯片尺寸: 6.1 mm×1.7 mm
- 像素尺寸: 36 μm×36 μm
- 仿真阈值~150 e<sup>-</sup>, ENC=5.4 e<sup>-</sup>
- 细时间精度: 500 MHz 启停型VCO
- 仿真功耗: <50 mW/cm<sup>2</sup>

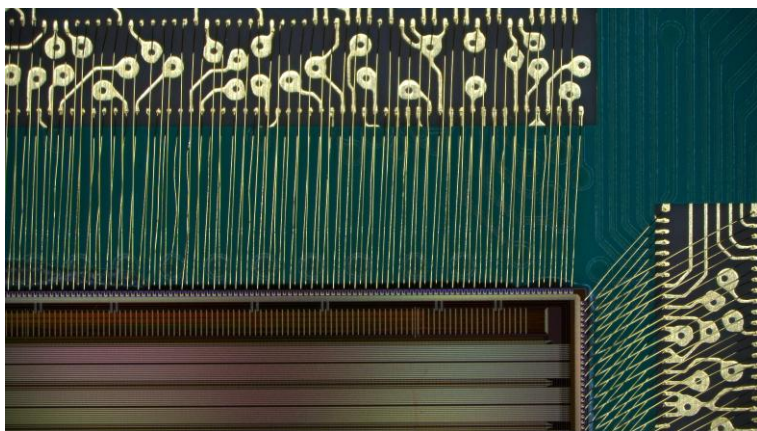


## ❖ Super pixel结构

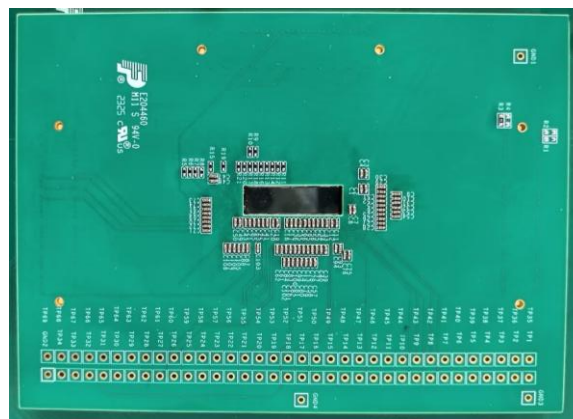
- 芯片尺寸: 6.1 mm×22.0 mm
- 列方向达到全尺寸: 576行



## ❖ 已回片, 准备测试中



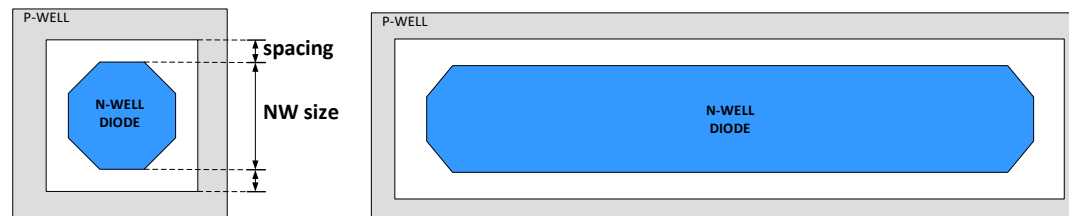
芯片打线



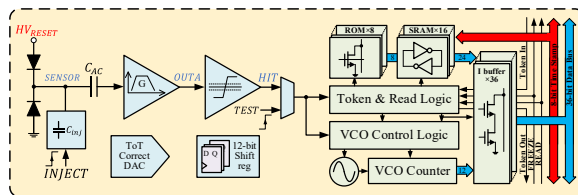
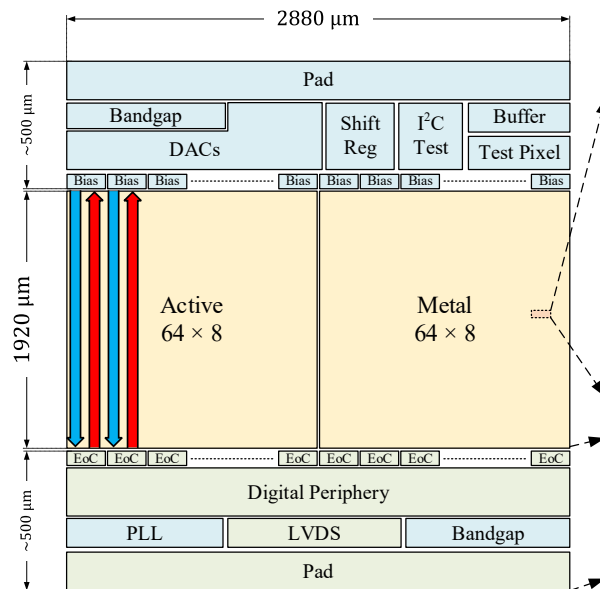
子板正面-芯片封装

## ❖ Sensor纯模拟读出芯片

- 多种像素子阵列
  - 5×5 pixel
  - 大、小像素
  - 收集级尺寸、Pwell间距
  - 复位方式、耦合方式



## ❖ 全功能大像素原型验证芯片



### ➤ 模拟电路

- ✓ 正高压+AC耦合
- ✓ 前放放电时间可调
- ✓ 甄别器阈值可调

### ➤ 数字电路

- ✓ 锁存ToA、ToT时间戳
- ✓ Token读出
- ✓ 500 MHz启停VCO

### ➤ 外围电路

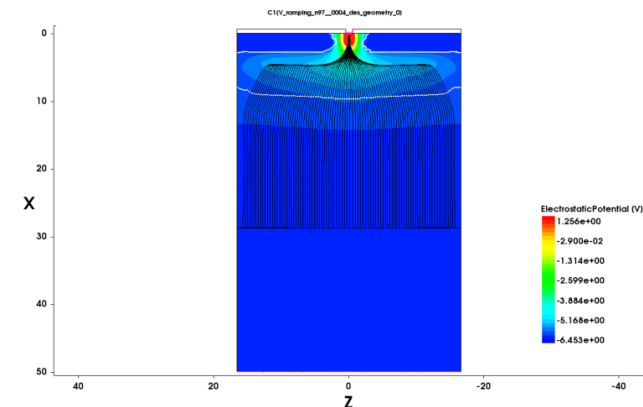
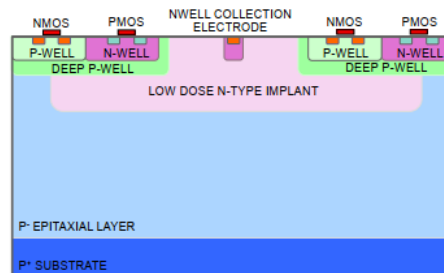
- ✓ Token读出控制电路
- ✓ 数据缓存、汇总、组帧
- ✓ 500 Mbps LVDS×2

### ➤ 时间戳

- ✓ 8 bit格雷码
- ✓ 20 MHz

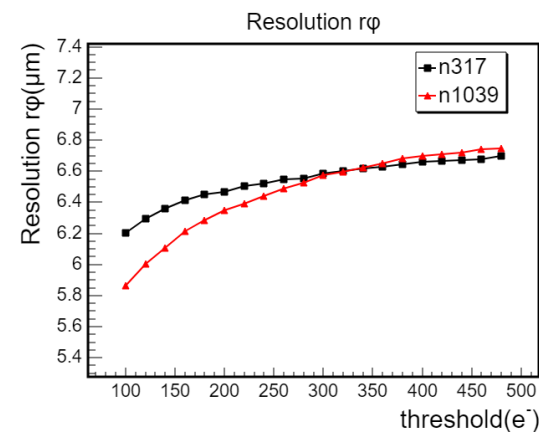
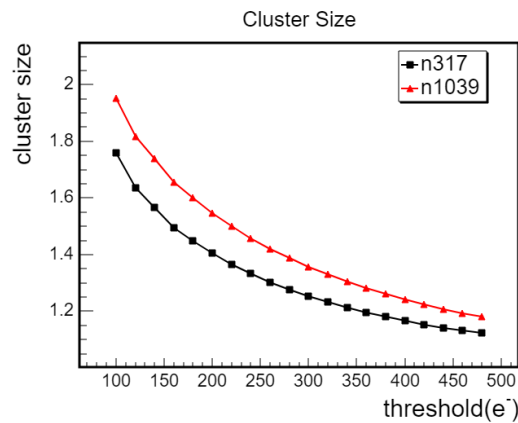
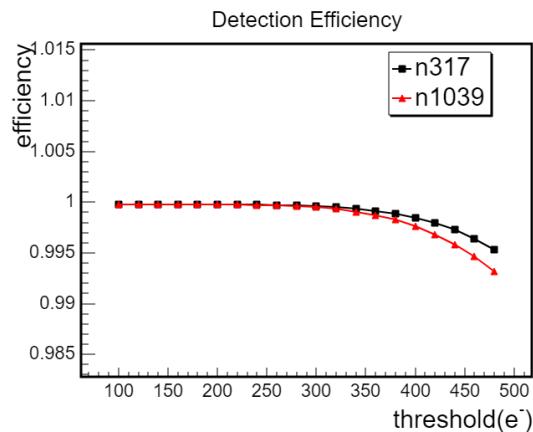
## ❖ Modified with gap sensor

- 像素尺寸:  $33.2 \mu\text{m} \times 33.2 \mu\text{m}$
- N-blanket gap =  $2 \mu\text{m}$



-6V偏压下的modified gap sensor电势分布

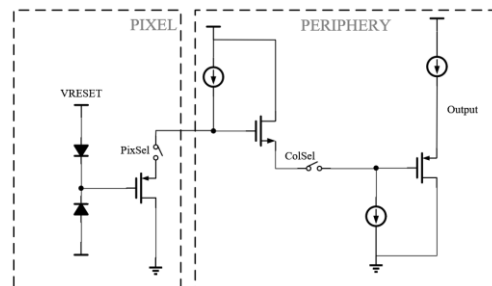
## 两种flow参数下的MIP模拟结果



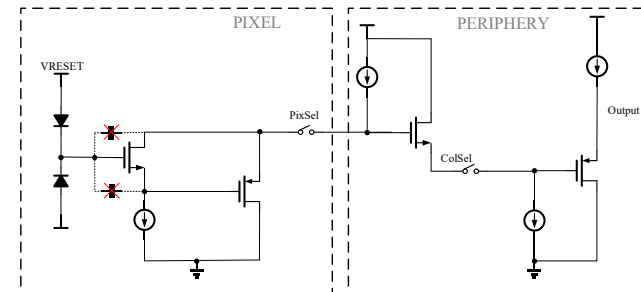
良好的电荷收集性能

## ❖ Sensor纯模拟读出

- 多种像素子阵列
- 优化输入端等效电容/电路增益
- 提高信噪比: 减小信号损失



大像素读出电路

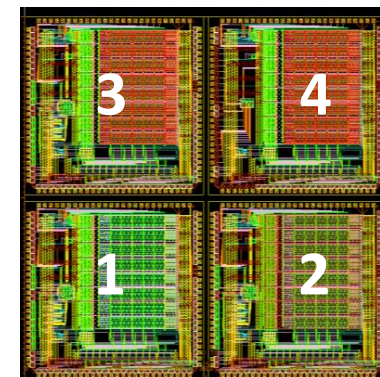


小像素读出电路

## ❖ 模拟前放设计

- 基于传统cascode结构

工艺	TJ180	IRAY180
ENC ( $e^-$ )	5.4	7.7
$\sigma_{Jitter}$ (ns)	1.1 (400 $e^-$ )	2.0 (400 $e^-$ )



## ❖ Chip2-4在Chip1基础上添加N-blanket注入层

	Chip1	Chip2	Chip3	Chip4
Sensor	Standard	Modified	N-gap (= 2.5 $\mu\text{m}$ )	N-gap (= 4 $\mu\text{m}$ )

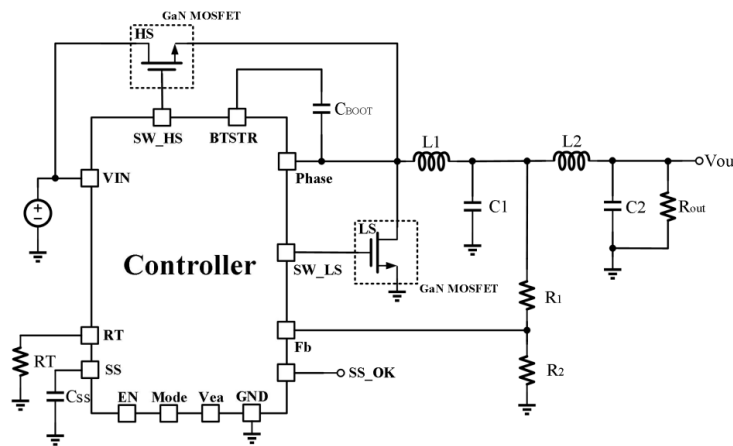
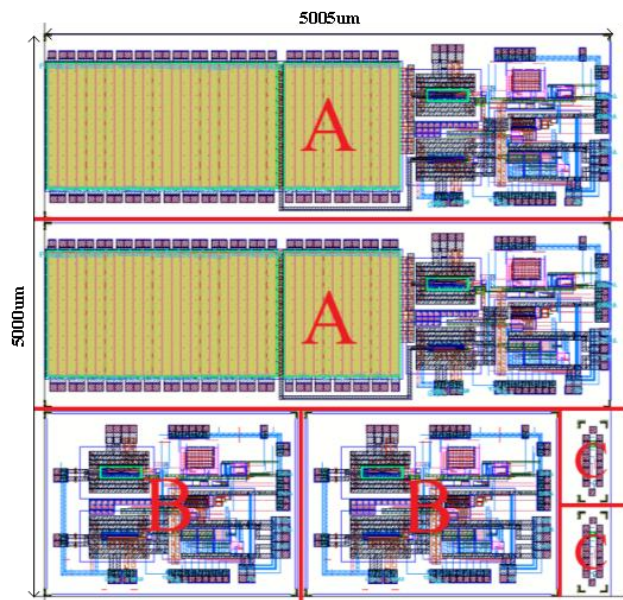
## ❖ 基于SMIC180 BCD工艺的DC-DC电压转换器

✓ 2025.4流片

A: 内置NIdMOS的DCDC Chip

B: DCDC Controller

C: SMIC工艺下的器件辐照测试芯片

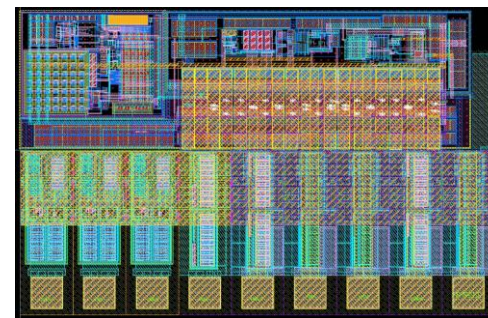


DC-DC系统应用框图

## ❖ 基于TJ180工艺的片上LDO

• 提交中

• 面积: 0.3 mm×0.9 mm







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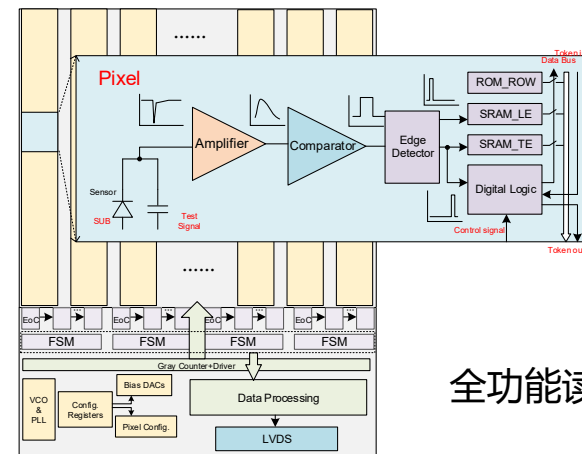
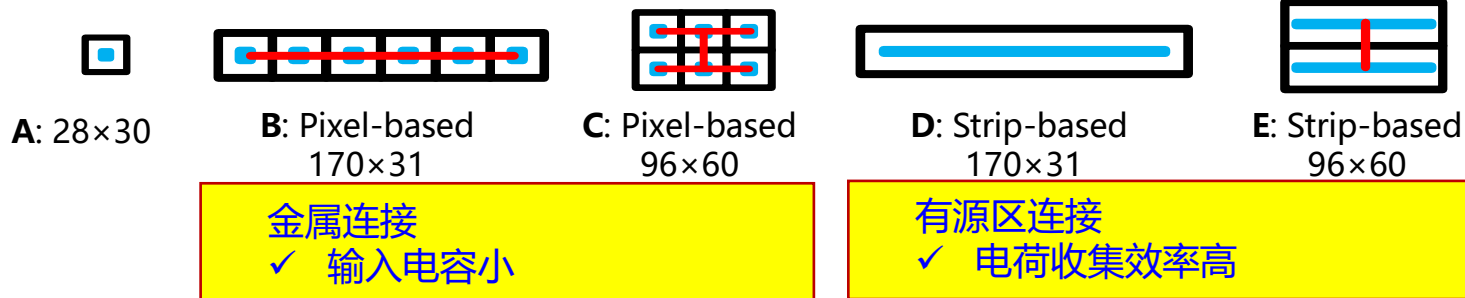
❖ 模块组装设计

# TJ\_v0.1芯片总览



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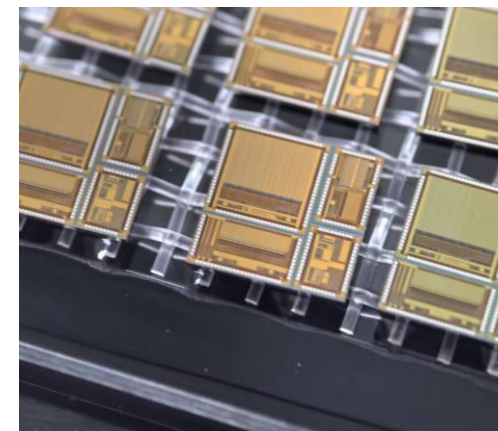
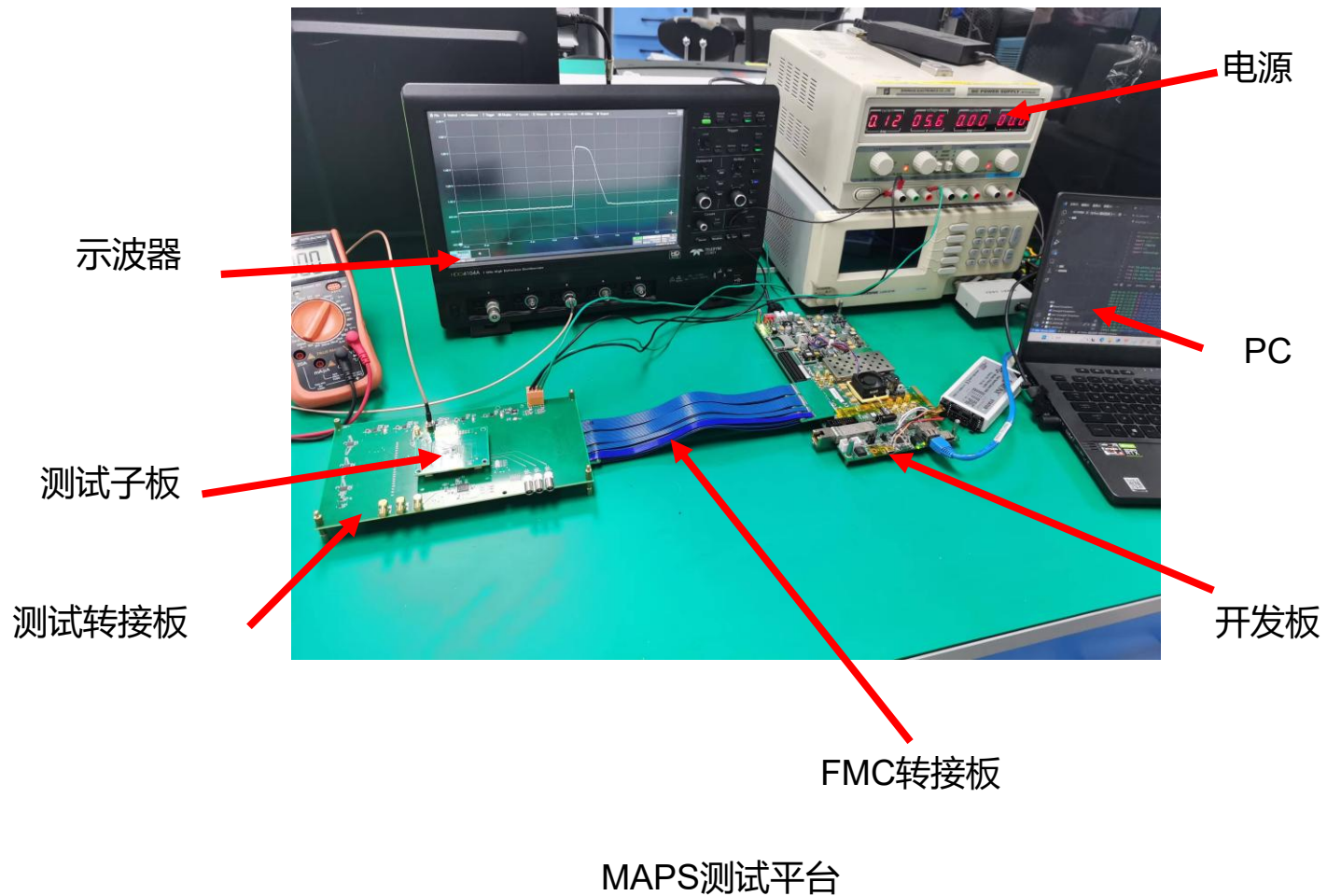
❖ 比较多种模拟连接方式的sensor

❖ 四块原型芯片

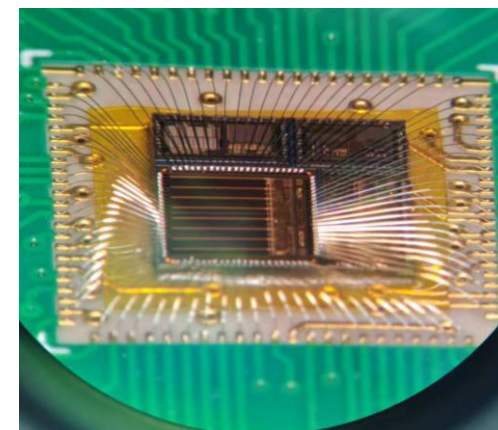
- Chip1: ALPIDE-like小像素, 0/1读出
- Chip2: 大像素 (2×3), ToA&ToT
- Chip3: 大像素 (1×6), ToA&ToT
- Chip4: 模拟读出, 5种sensor

	Chip1	Chip2		Chip3		Chip4
Pixel size (μm×μm)	28.1x30.1	96.4x59.6		170.0x31.0		Mixed
Sensor	A	E	C	D	B	A+B+C+D+E
Pixel array	16x30	8x12	8x12	60x8	60x7	Mixed
Readout	Column-drain	Column-drain		Column-drain		Analog readout
ToA & ToT	X	√		√		X
Chip area (mm <sup>2</sup> )	1.5x1.4	2.5x1.6		2.8x3.1		1.2x1.4

# TJ180测试平台



MAPS芯片



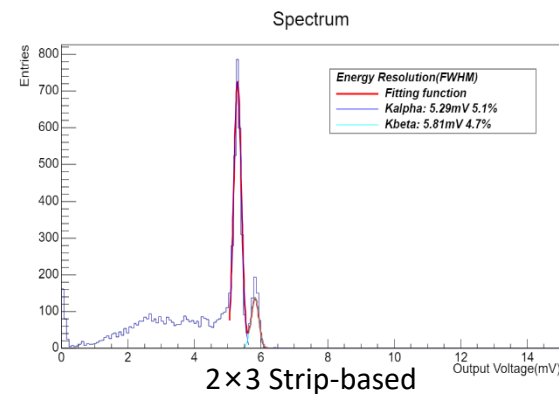
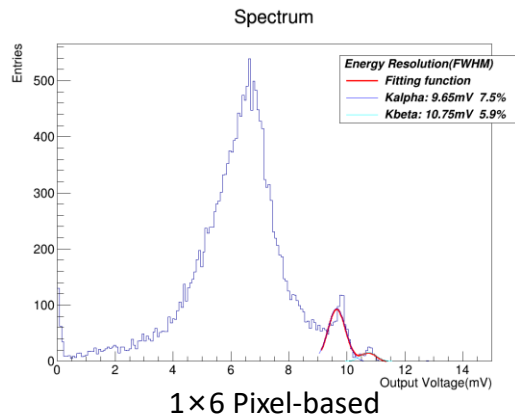
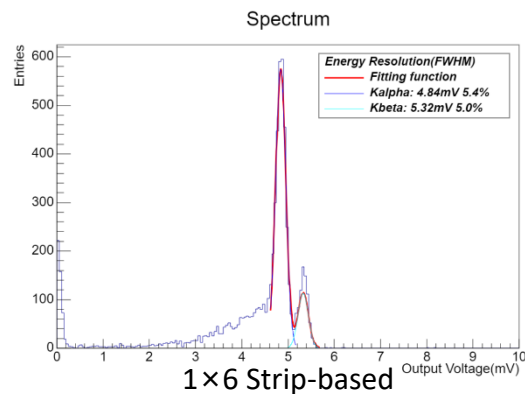
MAPS芯片打线

# Sensor模拟读出芯片测试



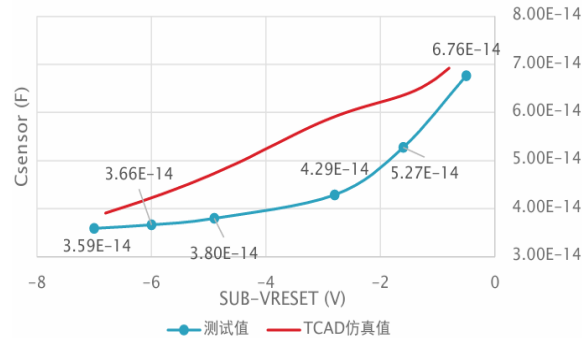
## ❖ Fe55测试

- Strip-based像素观测到明显全能峰→更好的电荷收集效率

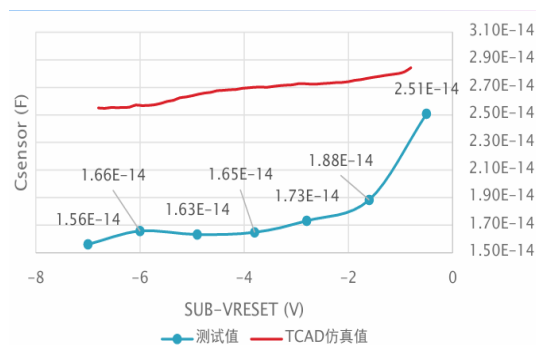


## ❖ Sensor电容

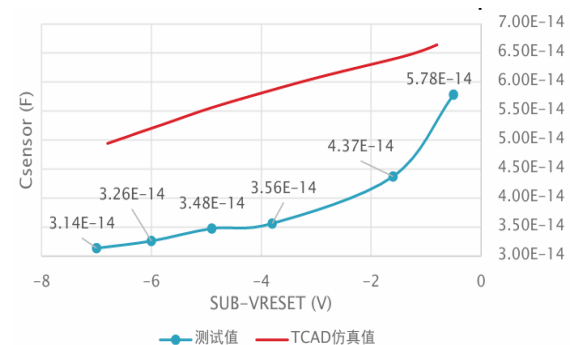
- 通过Fe55能谱标定输入端电容
- 为电路设计提供重要参考



1 × 6 strip-based像素



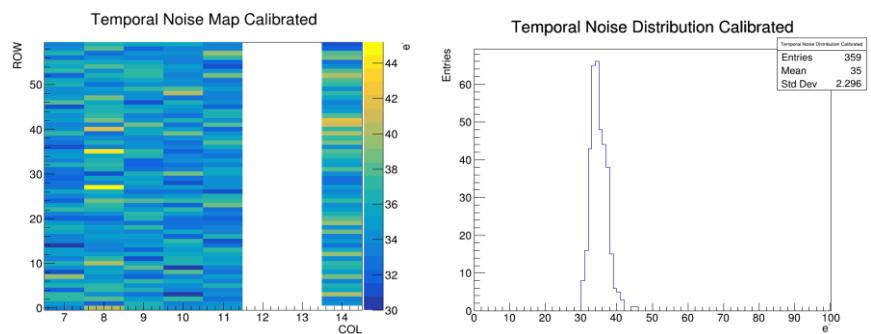
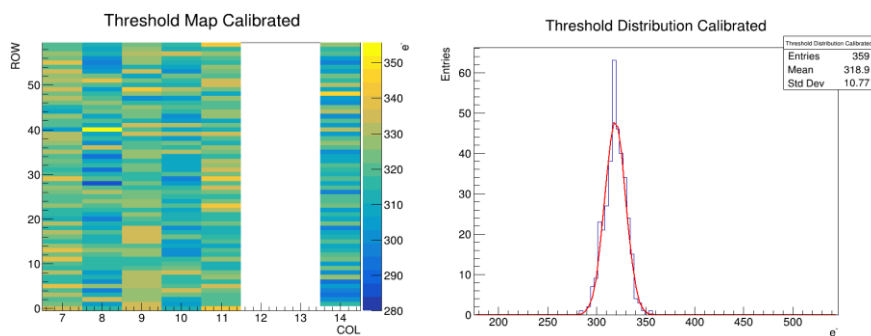
1 × 6 pixel-based像素



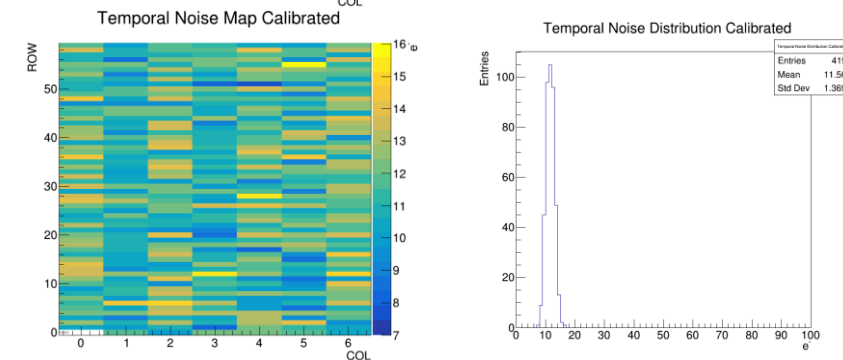
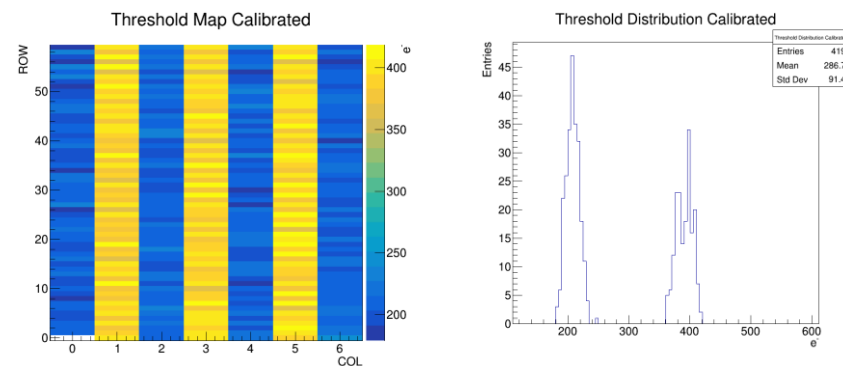
2 × 3 strip-based像素

## ❖ -6V衬底偏压下扫描S-curve

- Strip-based:
  - 阈值均值359 e-, 阈值离散10.8 e-
  - ENC均值35.0 e-, ENC离散2.3 e-



- Pixel-based:
  - 阈值均值207.5 e-, 阈值离散11.0 e- (仅偶数列)
  - ENC均值11.6 e-, ENC离散1.4 e-
  - 奇偶列阈值不一致, 推测是由电荷标定电路的不一致导致



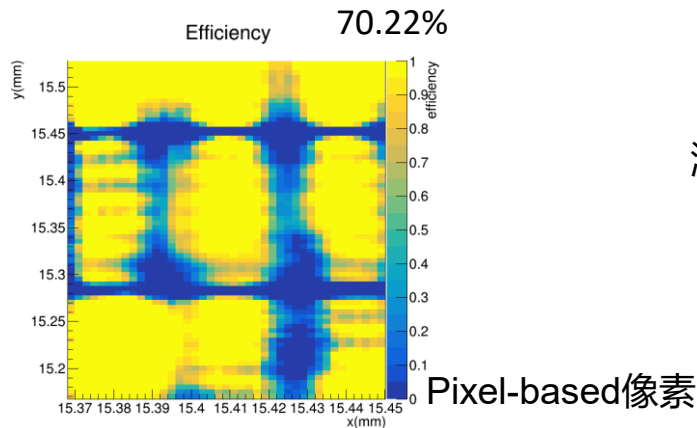
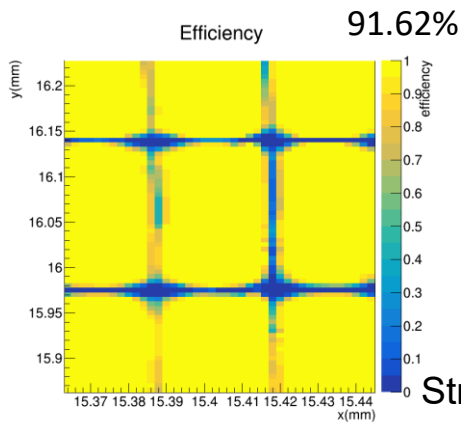
# 激光效率测试



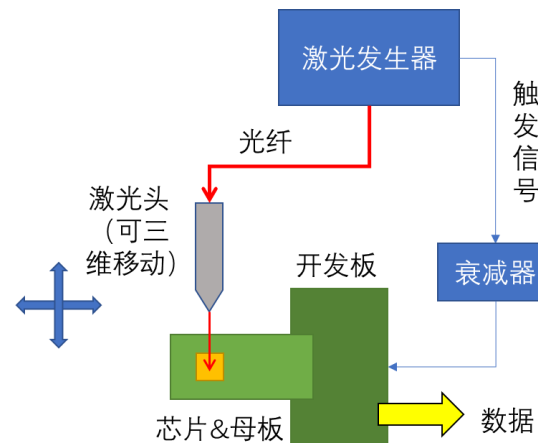
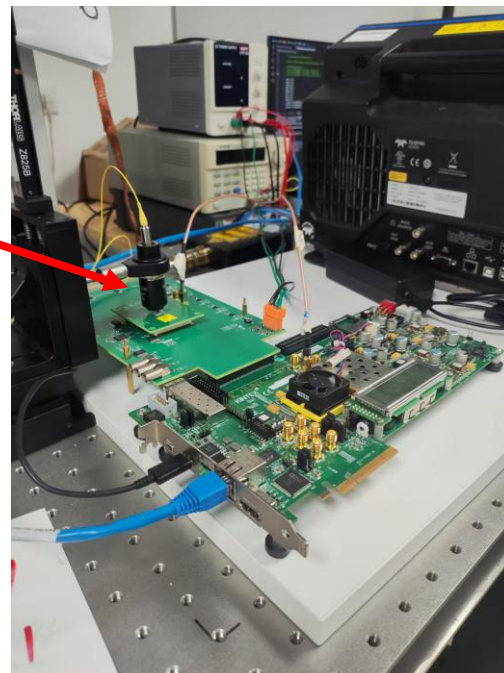
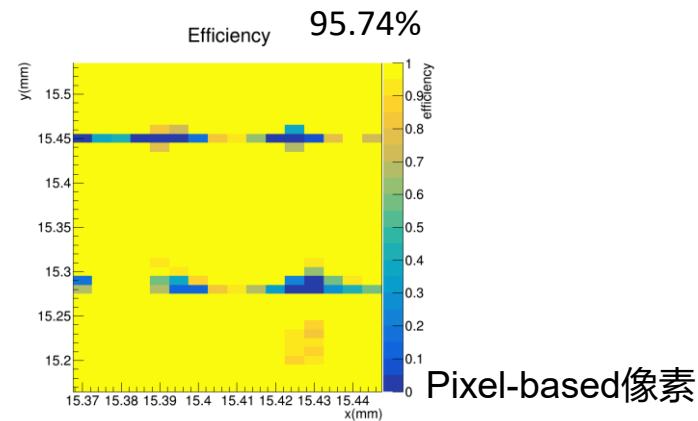
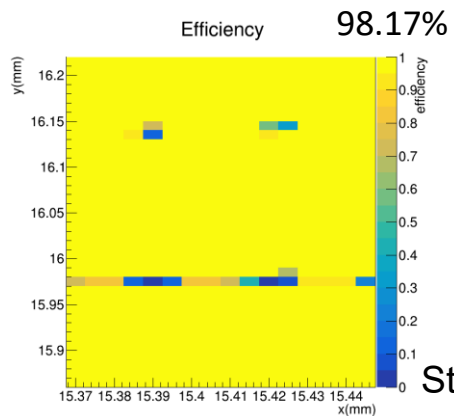
中国科学技术大学

University of Science and Technology of China

利用S-curve标定激光强度, 约为 $600e^-$  ( $<0.375\text{MIP}$ )



激光强度约为 $800e^-$



- Strip-based像素探测性能好于pixel-based像素
- 在 $\sim 1\text{MIP}$ 能量沉积下都能达到99.9%以上探测效率

# Sr90时间精度测试

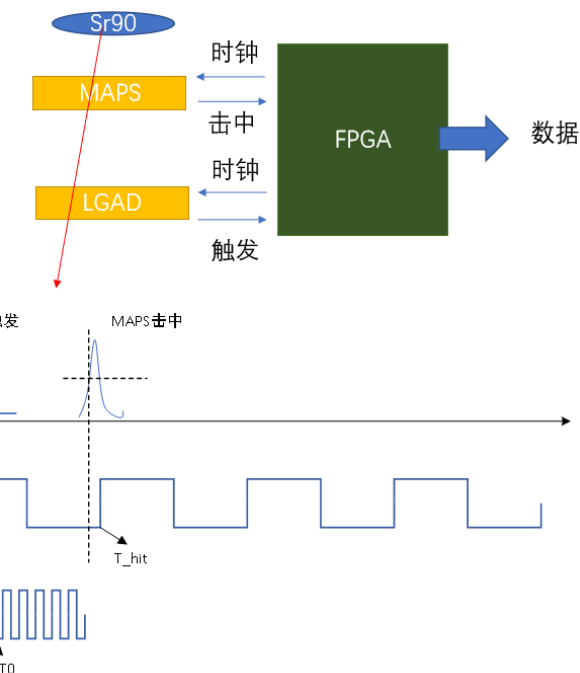
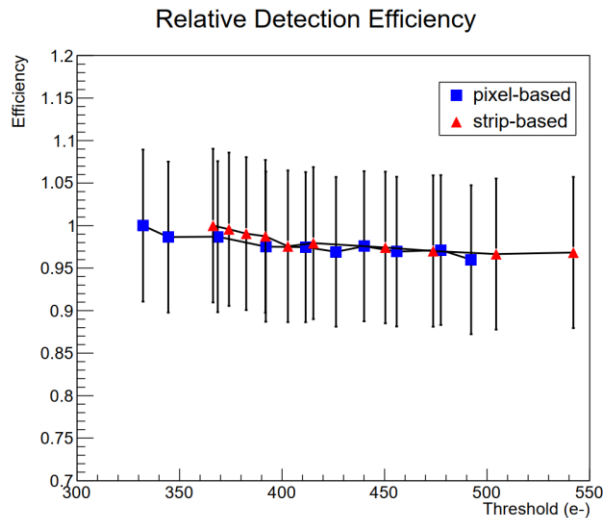
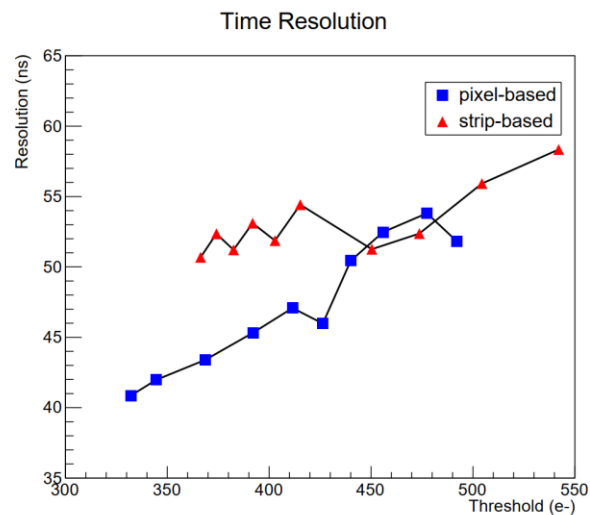
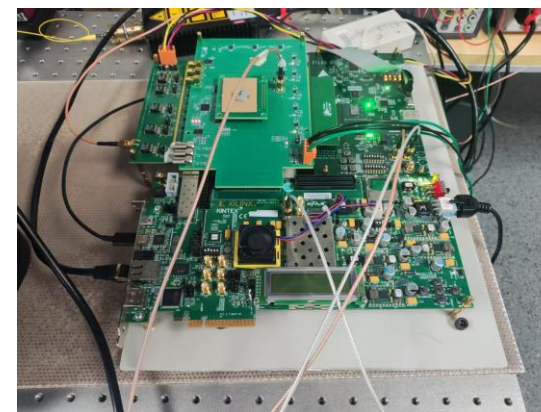


## ❖ 测试方法

- 使用320MHz的高频时钟记录LGAD触发信号的时刻 $T_0$
- 像素被击中时，hit信息会以40MHz系统时钟频率记录下该击中的过阈时刻 $T_{hit}$
- 符合后将两个时刻相减，得到timewalk值
- 在-6V偏压，不同阈值下进行1h的Sr90事例采集

## ❖ 测试结果

- 使用Sr90测得的MAPS时间分辨在 $\sim 50\text{ ns}$ ，如有ToT信息预计可以进一步提升
- 基本达到第一阶段目标





❖ 研究背景

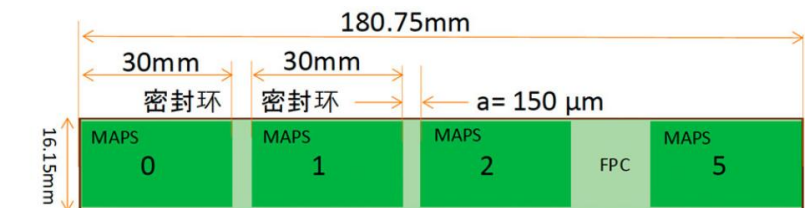
❖ STCF MAPS原型芯片设计

❖ TJ第一版MAPS测试

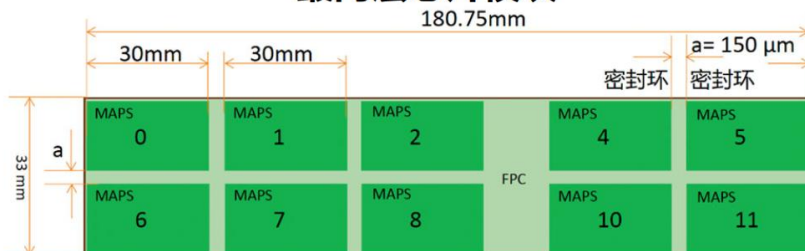
❖ 模块组装设计



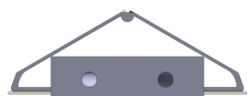
## ❖ STAVE-MAPS模块结构



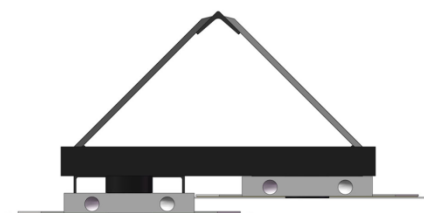
最内层芯片模块



外两层芯片模块

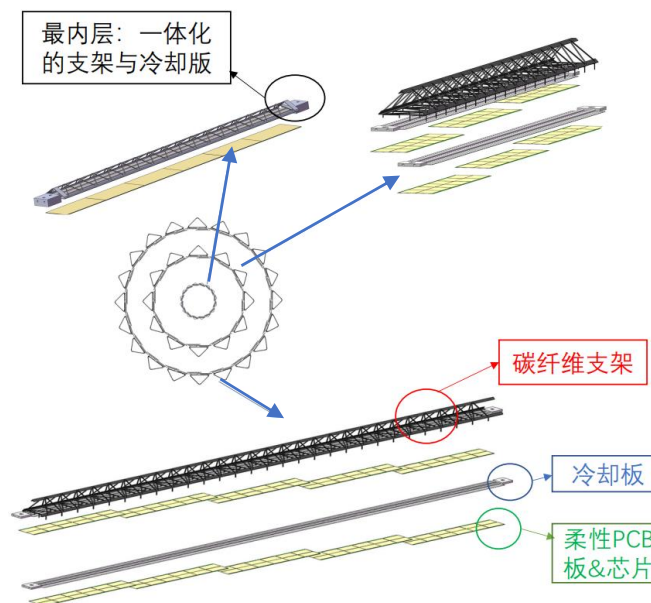


Inner STAVE



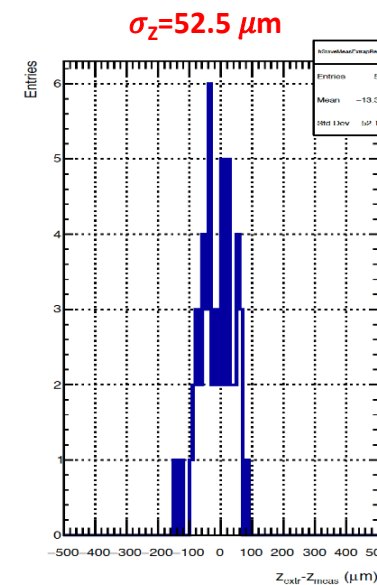
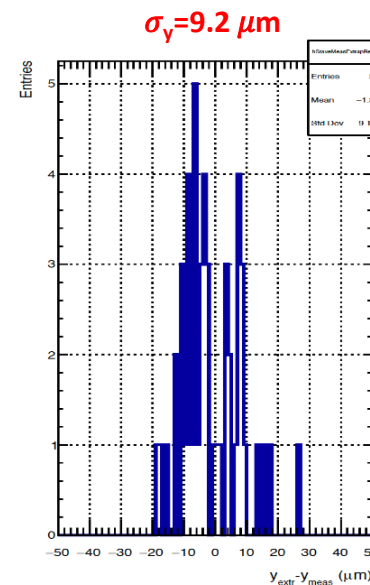
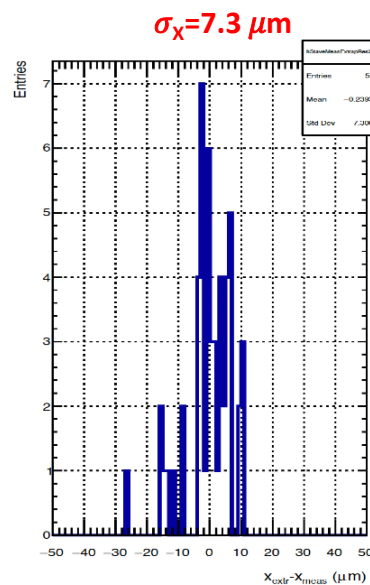
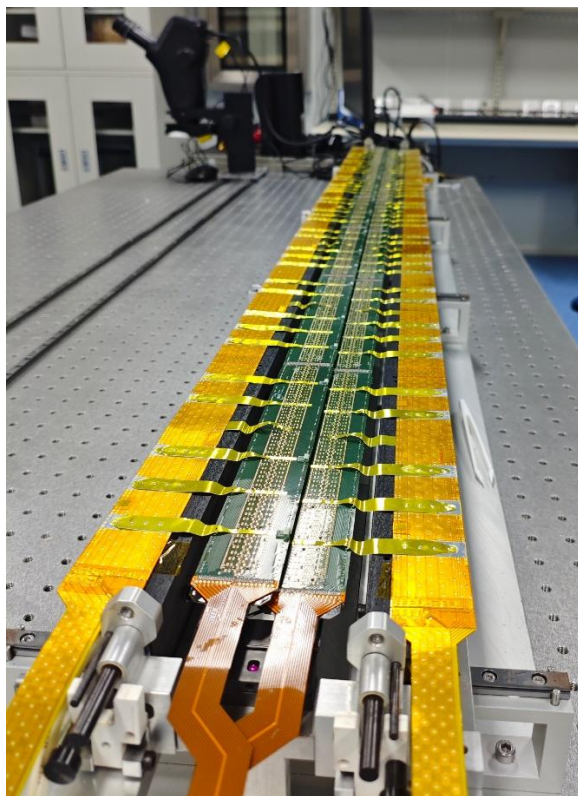
Outer STAVE

Layer	半径	Stave数量	Stave全长	模块数量 /stave
1	36mm	16	200.75mm	1
2	98mm	12	592.25mm	6
3	160mm	20	954.55mm	10

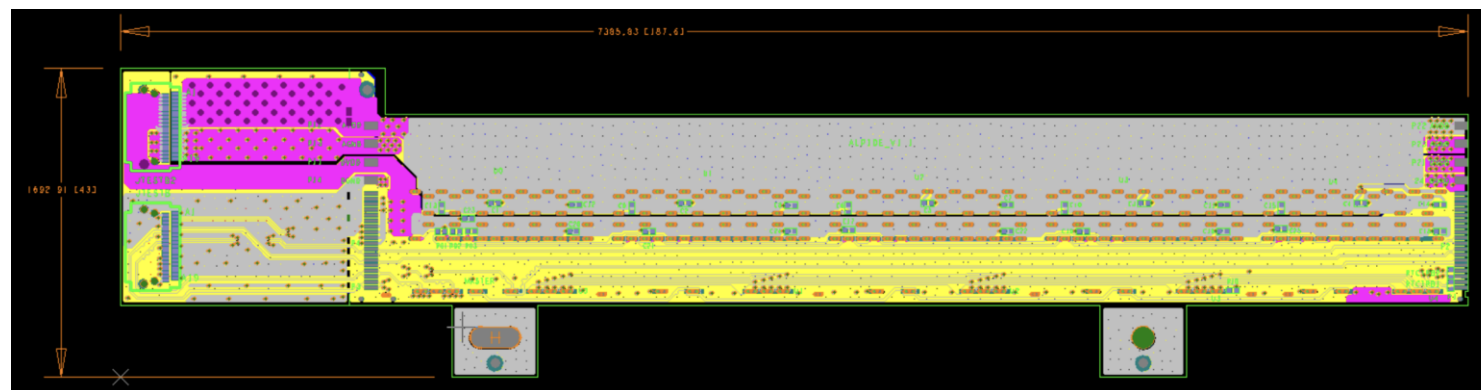
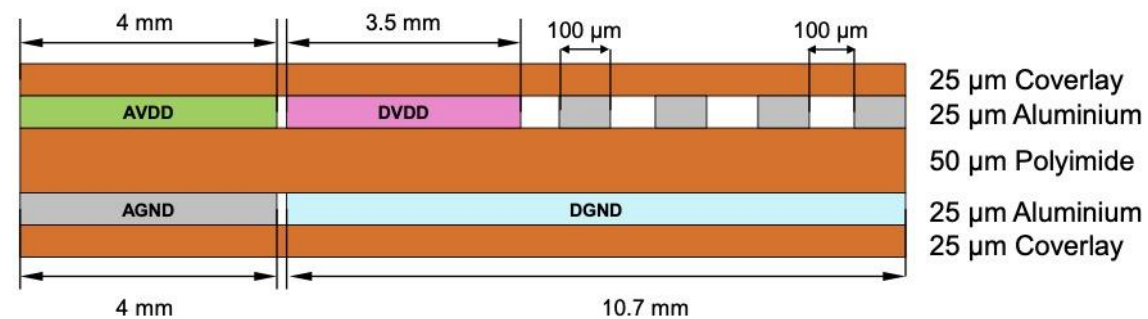


## ❖ 基于ALICE ITS2技术方案，实现stave模块组装与集成精度测试

- 由14个芯片模块与碳纤维机械结构组装而成



- ❖ ALICE ITS2采用镀铝的柔性PCB，以减少质量
- ❖ 基于ALICE ITS2的FPC设计做了简化，提交给工厂做试制



## ❖ MAPS探测器是STCF ITK方案之一，要求同时实现位置、时间和电荷测量

- 位置分辨 $\leq 100 \mu\text{m}$
- 时间分辨 $\leq 50 \text{ ns} \rightarrow 20 \text{ ns}$
- 功耗 $\leq 100 \text{ mW/cm}^2 \rightarrow 50 \text{ mW/cm}^2$
- 单层物质质量 $< 0.3\% X_0$
- Hit rate  $1 \text{ MHz/cm}^2$ , TID  $1 \text{ Mrad/y}$ , NIEL  $1 \times 10^{11} n_{\text{eq}}/\text{cm}^2/\text{y}$

## ❖ MAPS设计进展

- 基于TJ180工艺完成第二版原型验证芯片设计 (CharTPix-TJ-v0.2)，正在提交流片
  - 超级像素方案：高空间分辨、高时间精度；大像素方案优化
- 基于GSMC130工艺原型芯片 (CharTPix-GSMC-v0.1)，已回片
- 基于BCIS90完成原型验证芯片设计 (CharTPix-BCIS-v0.1)，已于2025.6回片
- 基于IRAY180完成工艺评估芯片设计 (CharTPix-IRAY-v0.1)，并于2025.5提交流片
- 开展了抗辐照电源设计工作，DC-DC已提交流片，LDO正在提交中

## ❖ TJ第一版原型芯片测试

- Fe55能谱标定sensor电容
- 时间精度 $\sim 50 \text{ ns}$ ，基本达到第一阶段目标

## ❖ 模块组装设计

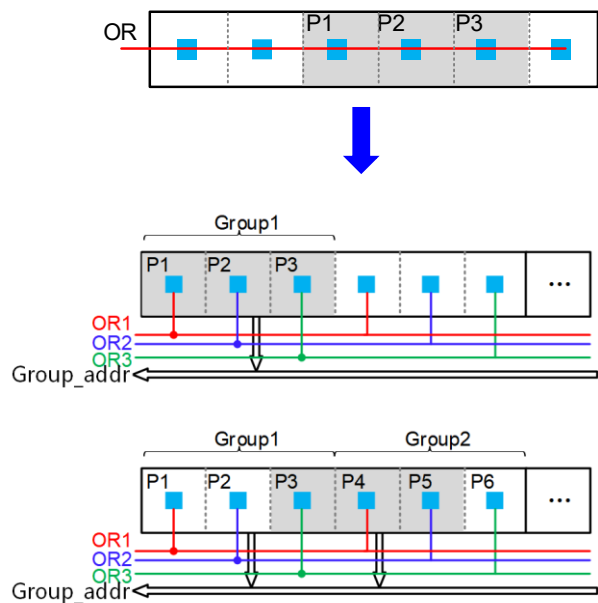
- 开展了stave机械结构设计
- 基于ALICE ITS2技术方案，实现Stave模块组装和集成精度测试
- FPC试制

谢谢！



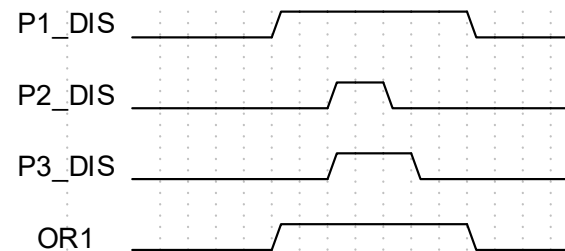
# 补充材料

# 方案优化



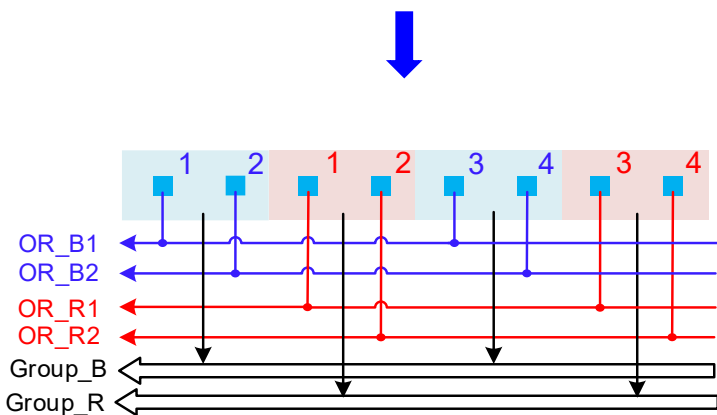
相邻像素做“OR”

- ✓ 小信号像素的ToT丢失 (Cluster>1时)



错位像素做“OR”

- ✓ 避免小信号ToT丢失(Cluster>1时)
- ✓ 读出有效Group地址
- ✓ 多个Group同时有效时, 位置信息丢失

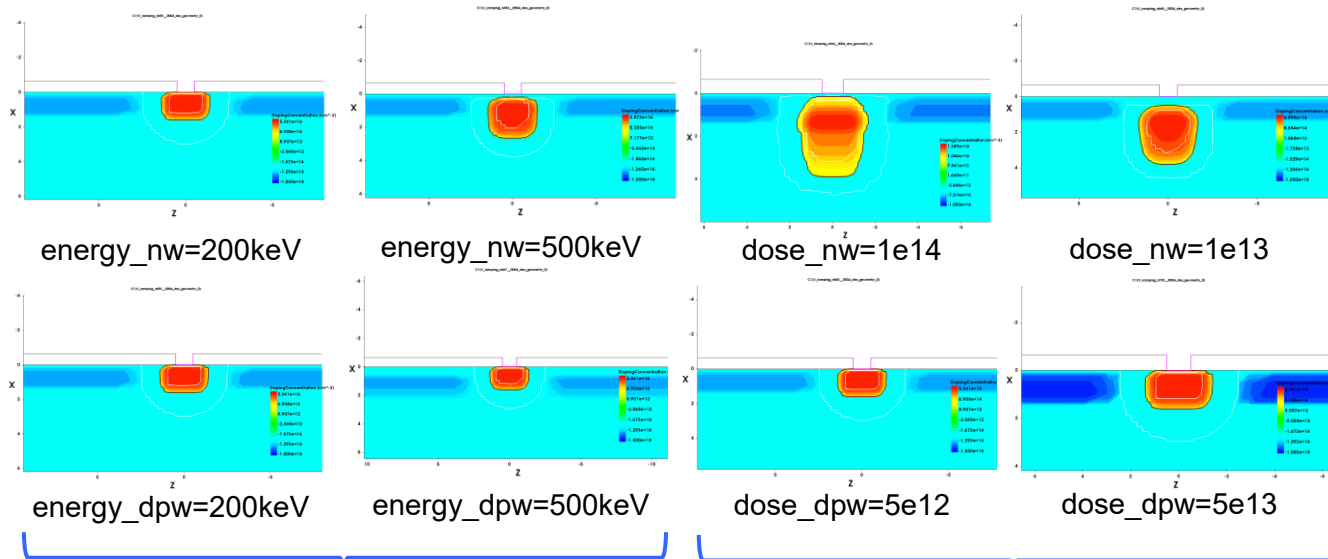


错位像素做“OR”、错位摆放Group

- ✓ 避免小信号ToT丢失
- ✓ 避免位置信息丢失
- ✓ 进一步减小数字功耗

## 结合仿真定制特殊工艺层

特殊掺杂NW  
(收集diode)

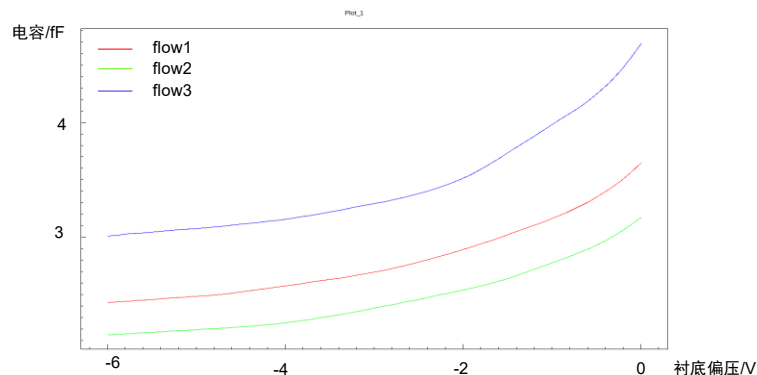


DPW

将尝试多种工艺参数

不同注入能量

不同掺杂浓度



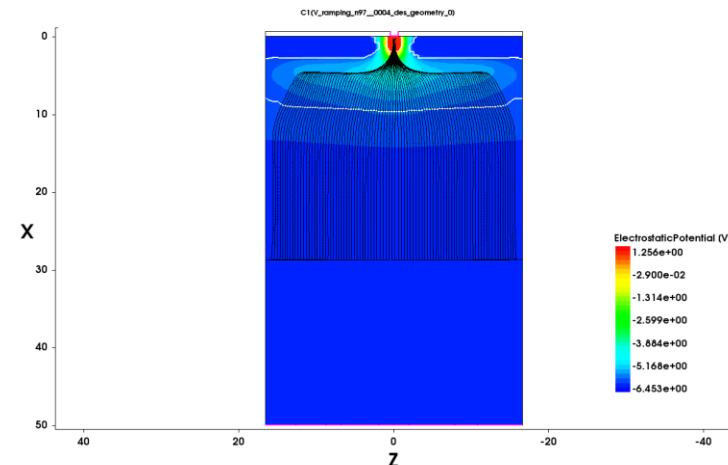
flow	0V下电容/fF	-6V下电容/fF
1	3.65	2.43
2	3.18	2.15
3	4.69	3.02

❖ 尝试高阻外延层

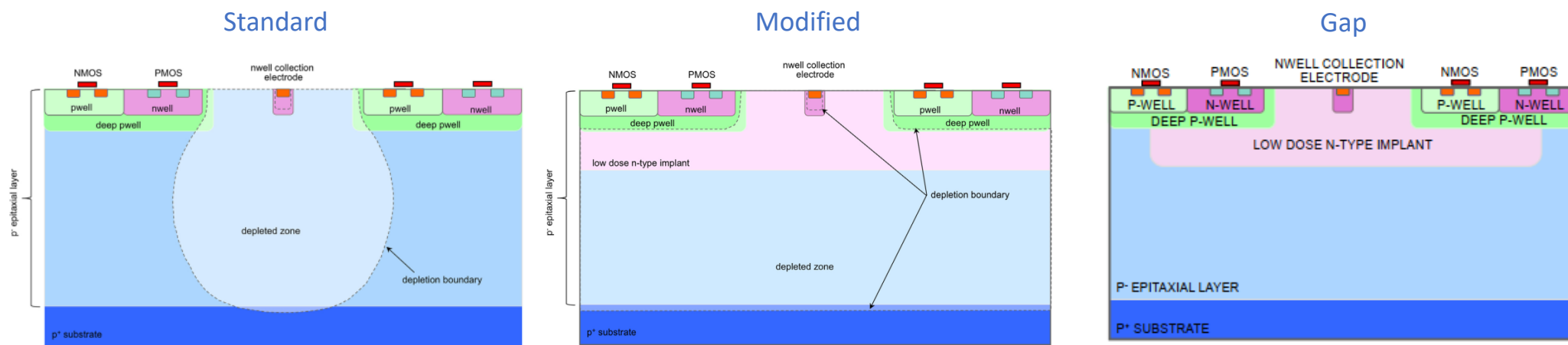
❖ 工艺流程

- N-blanket注入、退火
- DPW注入、退火
- 收集极NW注入、退火
- 氧化、金属化

❖ 通过TCAD仿真提供多种注入参数选择



-6V偏压下的modified gap sensor电势分布



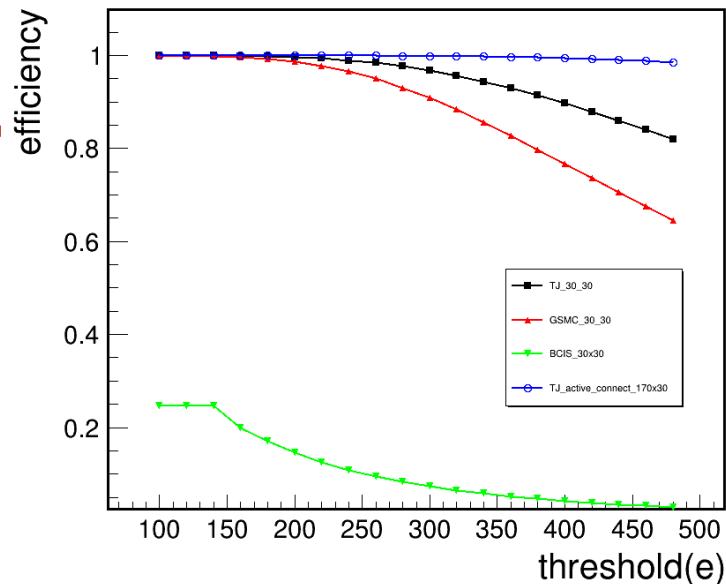


# MIP模拟

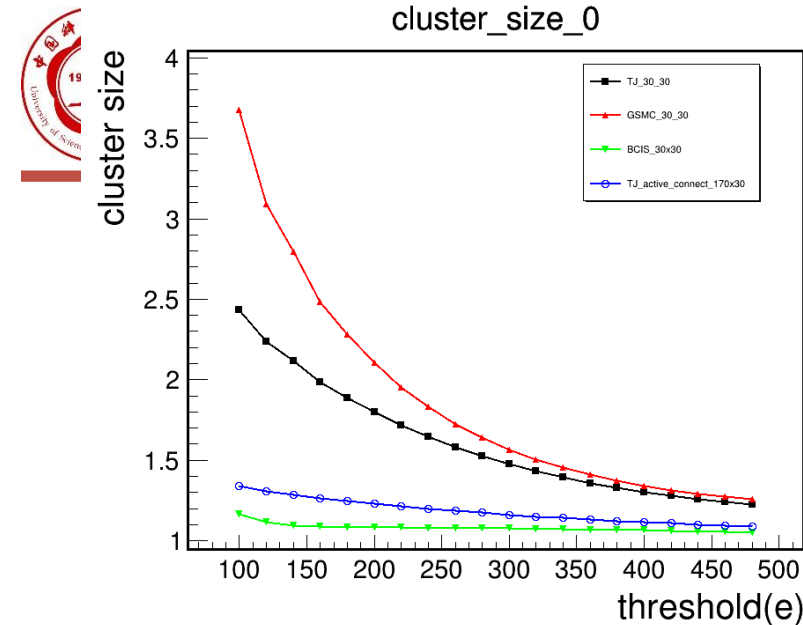
各项指标随像素阈值的变化

- TJ工艺长条型像素的探测效率最高，其次是TJ工艺小像素和GSMC工艺小像素
- 除BCIS工艺之外，其余工艺的位置分辨均随着阈值增加先变差后基本不变（或略有变好），与ALPIDE测试结果趋势接近

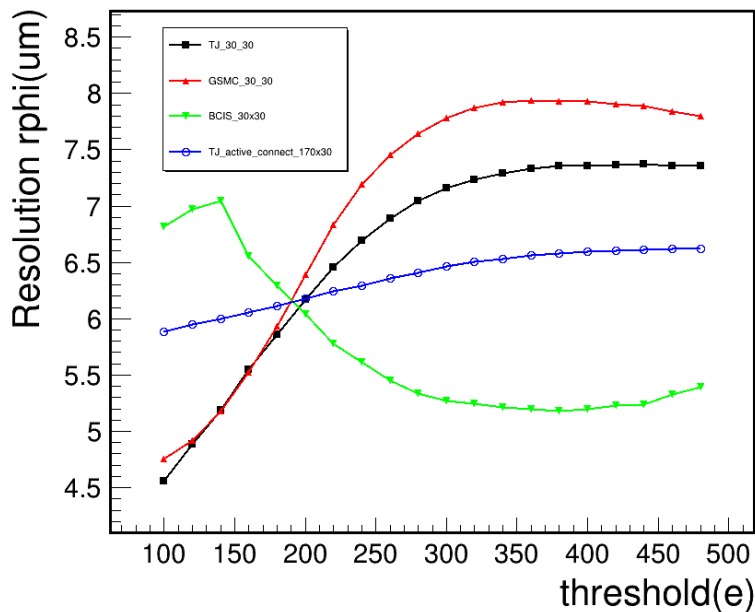
detection\_efficiency\_0



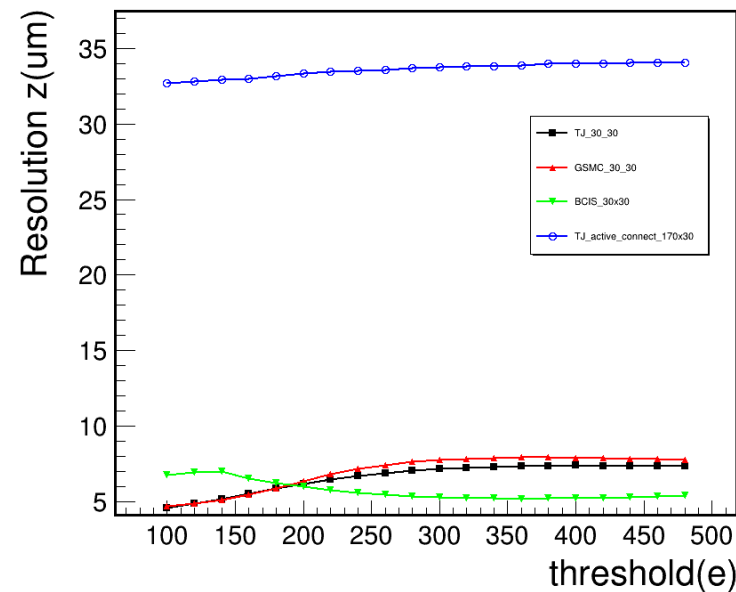
cluster\_size\_0



Resolution\_rphi\_0



Resolution\_z\_0



- 所有位置探测效率在99.9%以上

## xy方向扫描-1600e

