JadePix-3 CMOS 像素探测器的性能测试

胡珈豪[1]，张睿洋[1]，陈智良[1]，徐来林[1]，卢云鹏[2]

1 中国科学技术大学

2 中国科学院高能物理研究所

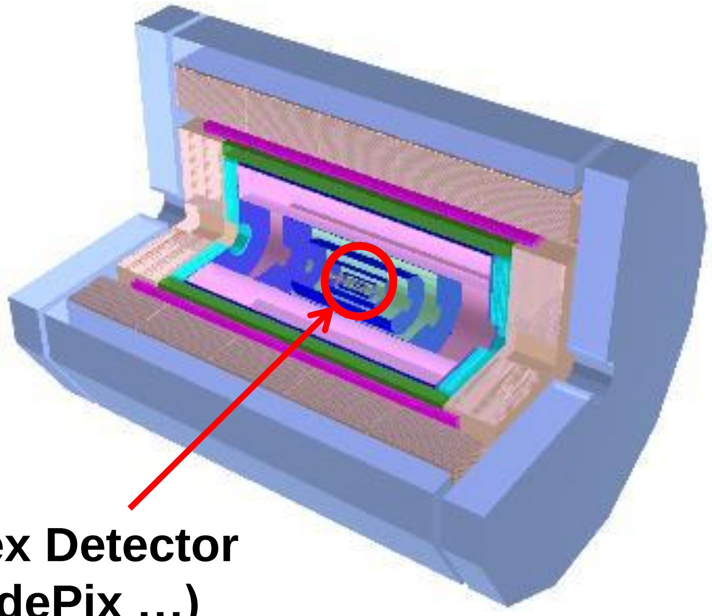
第五届半导体辐射探测器研讨会

4/19/2025

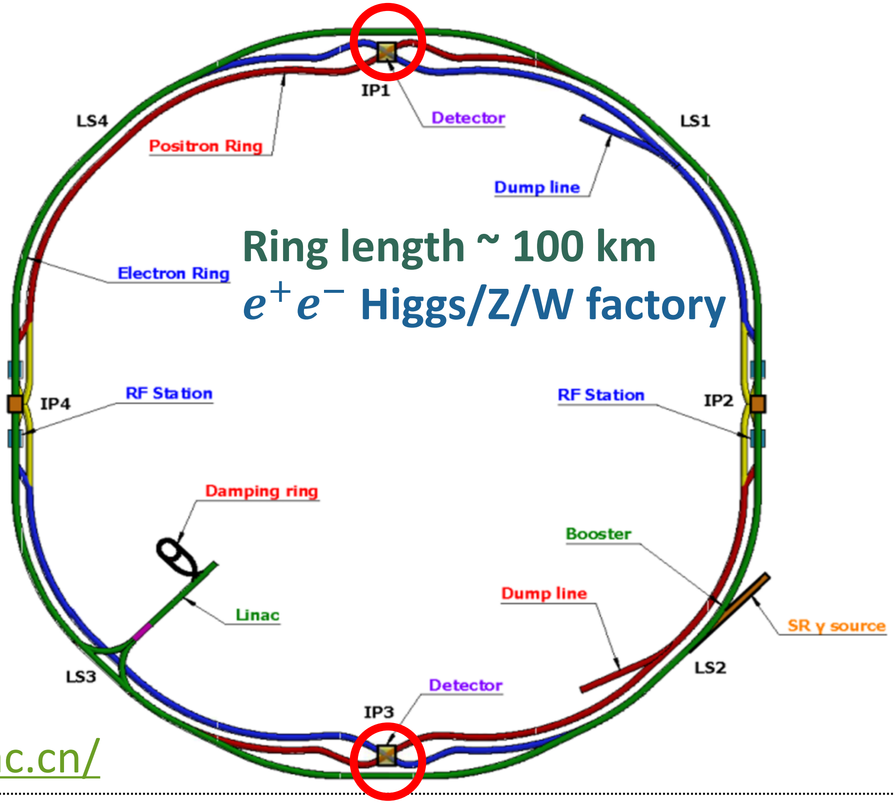
Outline

- **Requirements & Design**
  - **R&D background of JadePix-3**
  - **Design specifications of JadePix-3 MAPS**
- **Performance Test @USTC**
  - **Motivation for substrate reverse bias test**
  - **Test result**
- **Summary & Outlook**

- The **CEPC** was proposed in 2012 right after the Higgs discovery. It aims to start operation in 2030s, as an e^+e^- Higgs / Z / W factory.
- The **JadePix-3** sensors are orientated to the vertex detector for the experiments at the proposed future CEPC for precise measurement of Higgs boson.



Vertex Detector (JadePix …)



http://cepc.ihep.ac.cn/

R&D background of JadePix pixel chip

Impact parameter resolution	Vertex detector specs	Pixel sensor specs

Measurement of ***Br(H→bb/cc)*** strongly depends on vertex detector parameter:

$$\sigma_{r\phi} = 5\mu m \oplus \frac{10}{p(GeV)\sin^{3/2}\theta}\mu m$$

JadePix-3

$\sigma_{s.p.}$ ~ 2.8um → **Small pixel** ~ 16um

Material budget ~ 0.15% X_0/layer → **Thinning to** ~ 50um

→ **low power** ~ 50mW/cm^2

r of Inner most layer ~ 16mm → **fast readout** ~ 1us

JadePix-4

→ **radiation tolerance** ~

$\leq 3.4\ Mrad/year$

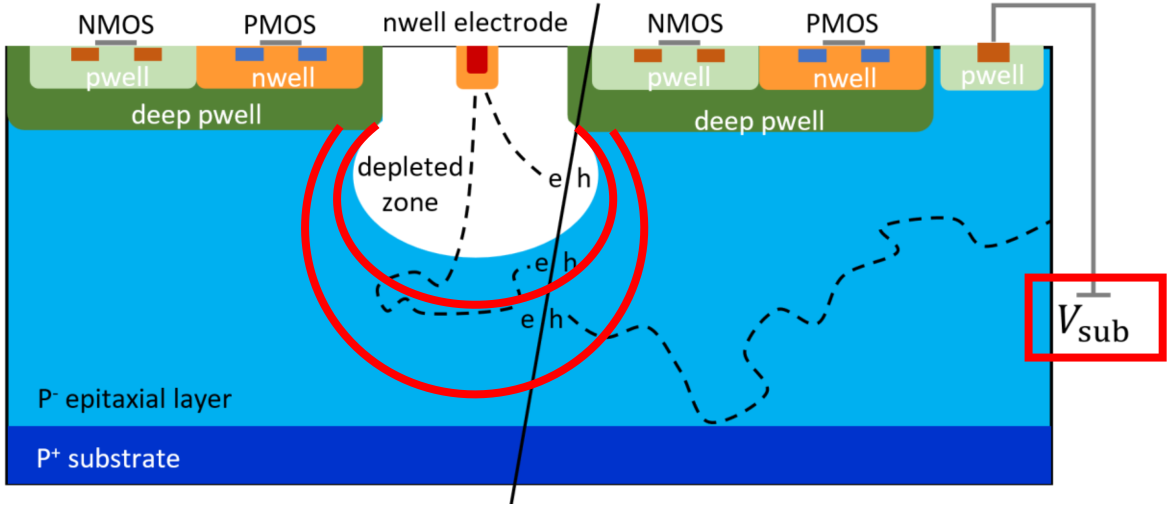
$\leq 6.2\times10^{12} n_{eq}/(cm^2 year)$

- **JadePix-3 CDR: (Requirements)**
  - **Small pixel + Thin chip + Low power**
  - **Only MAPS technology can meet these requirements**

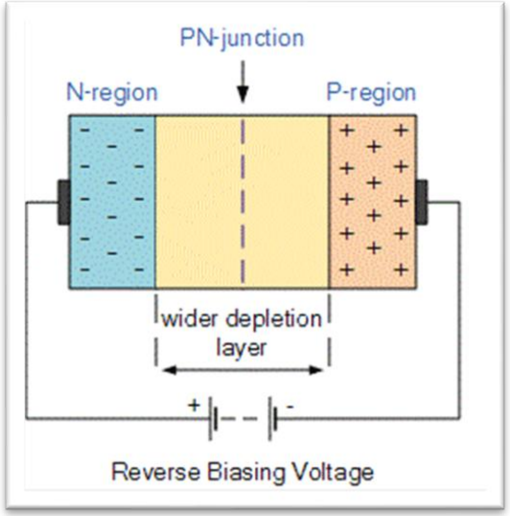
  - **What is MAPS?**

Monolithic Active Pixel Sensors
MAPS

- It is called Monolithic technology because **sensors** and **readout electronics** are integrated on one chip.
- Advantages:
  - **Smaller Pixel Size** and **Low material budget**
  - **Lower Costs** : implemented in standard commercial CMOS processes
  - **Bias Voltage**: added to substrate to improve performance by expanding *depleted zone*



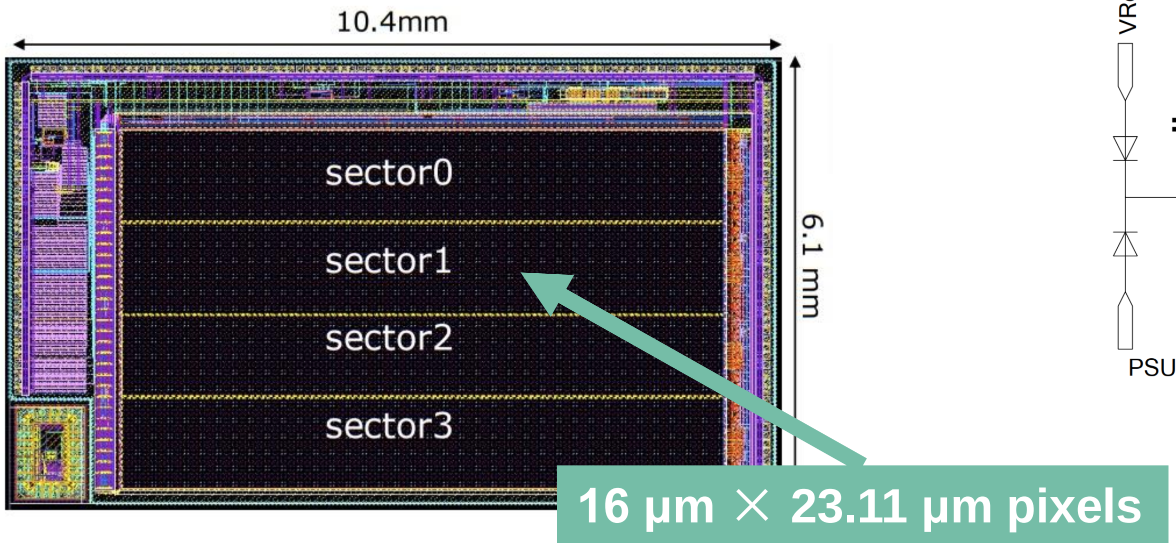
Sensing diode of JadePix-3
(High-resistivity CMOS)



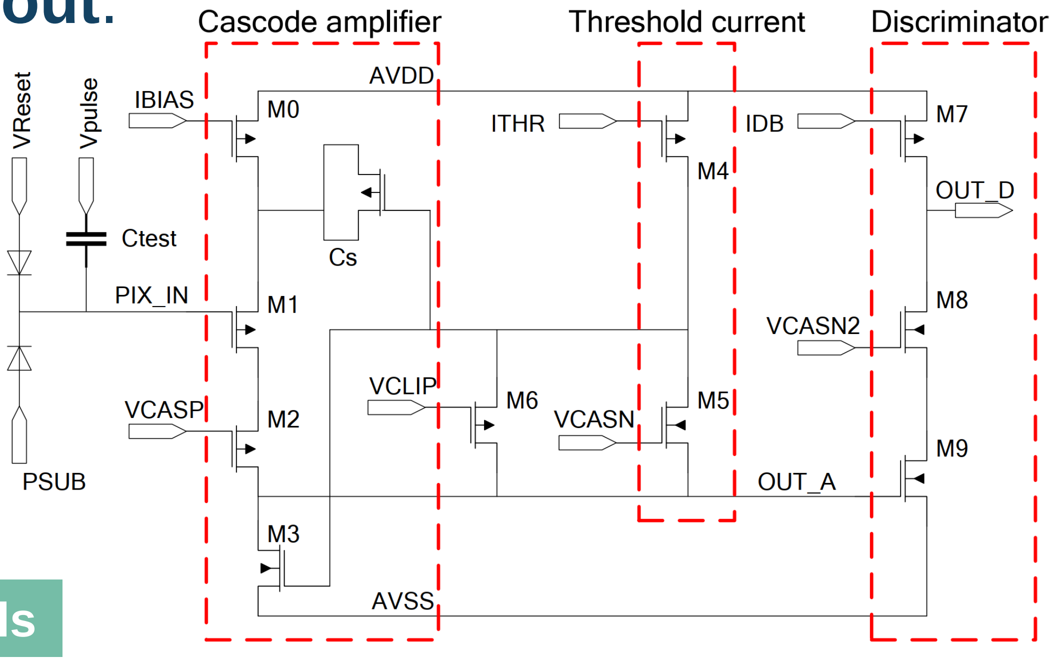
Design specs of JadePix-3 MAPS

P. Yang, Y. Zhang, Y. Zhou, L. Xiao, L. Zhang, Z. Shi, D. Guo, Z. Wu, Yunpeng LU

- JadePix-3 optimized for position resolution and low power consumption with Tower Jazz 180nm process.
  - Minimum pixel size: **16 μm × 23.11 μm**
  - Matrix readout time: **98.3 μs/frame**
- ALPIDE-like front-end with **binary readout**.



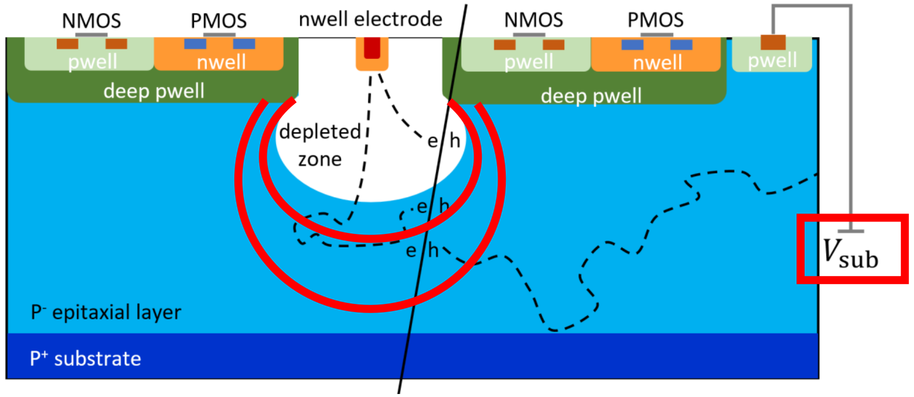
Layout of the JadePix-3 sensor



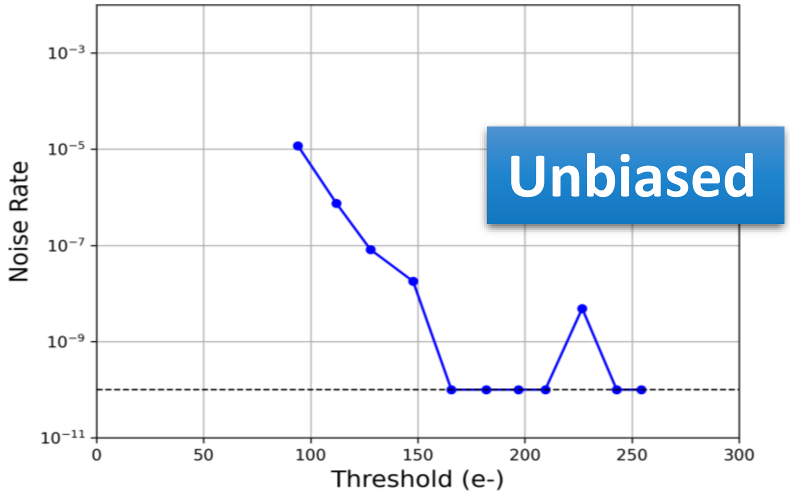
Analog front-end of the sensor

Motivation

- Bias Voltage added to the substrate should **improve** performance metrics:
  - (front-end) Noise, Input Capacitance
  - (detection) Detection Efficiency, Charge Collection Efficiency
  - Radiation Tolerance
  - ……
- Unbiased test done previously @NIMA 1048 (2023) 167967



sensing diode of JadePix-3

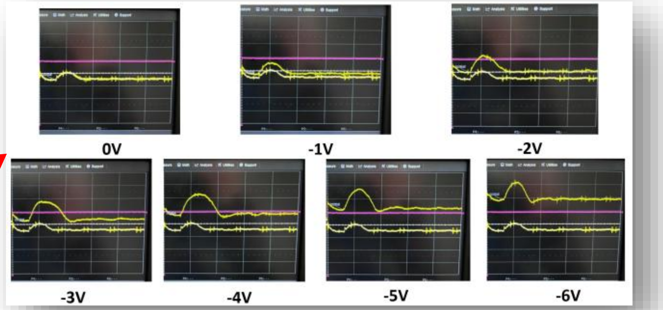


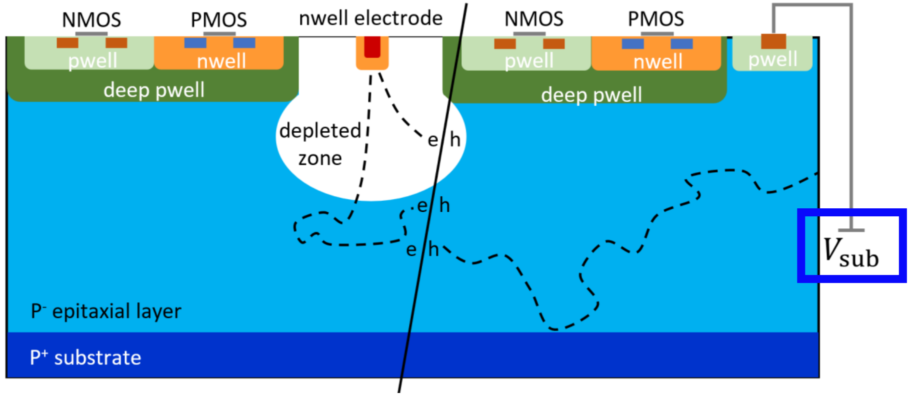
Previous Noise test

- Bias Voltage test need to be operated!

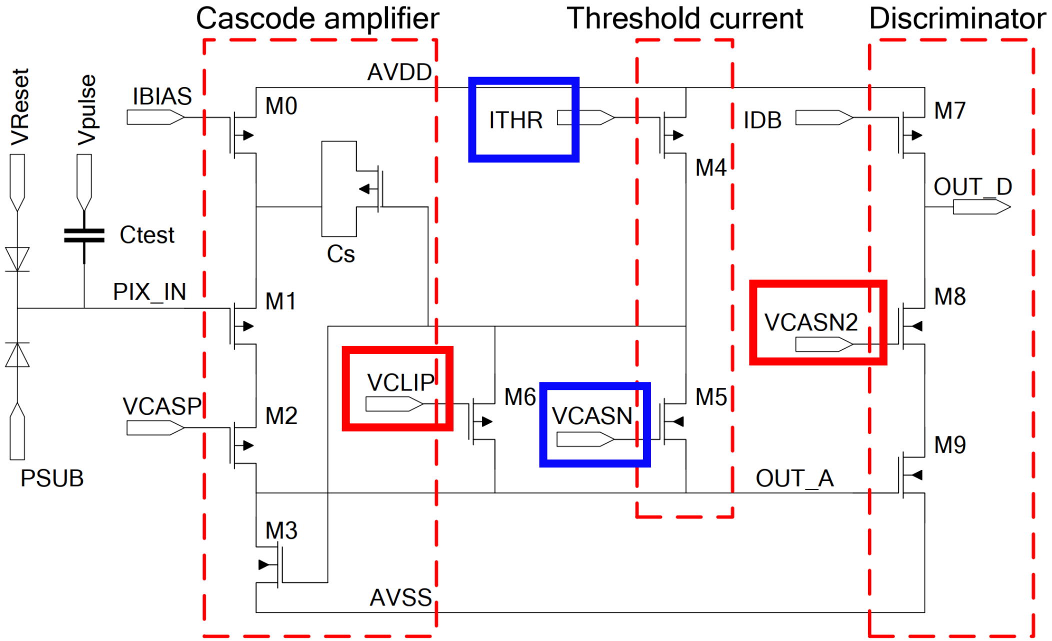
Searching Work-points under Bias

- Designed operating state cannot support all bias V_{sub} levels.
- Work-point Selection from V_{sub}=0~ -6V
  - VCLIP, VCASN2 adjustment
  - Adjusting VCASN and V_{sub} to keep threshold ≃ 210 e^-
  - ITHR scan to achieve distinct thresholds 100~270 e^-





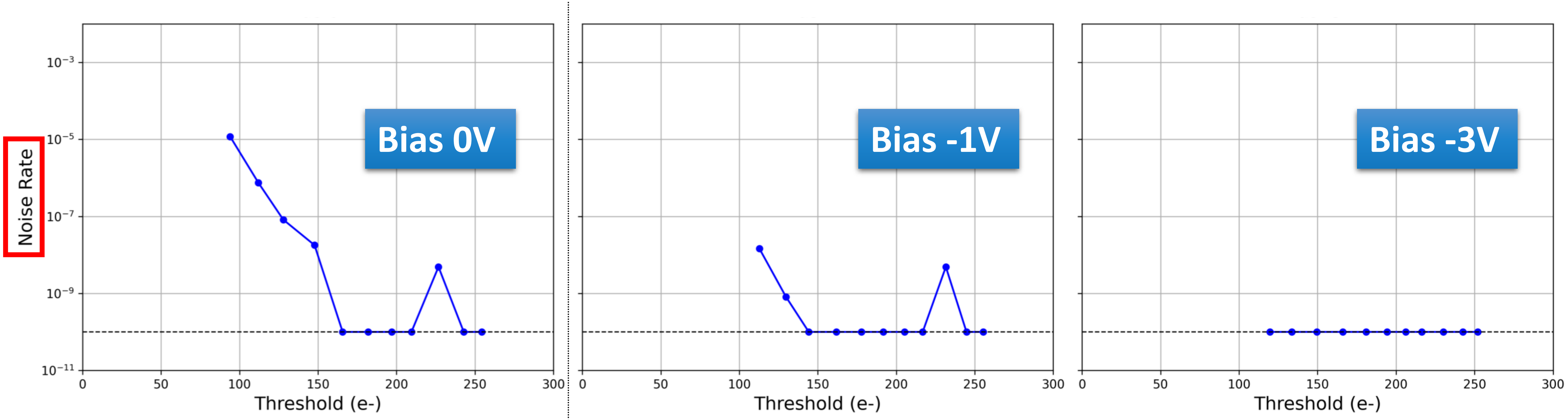
sensing diode of JadePix-3



Analog front-end of the sensor

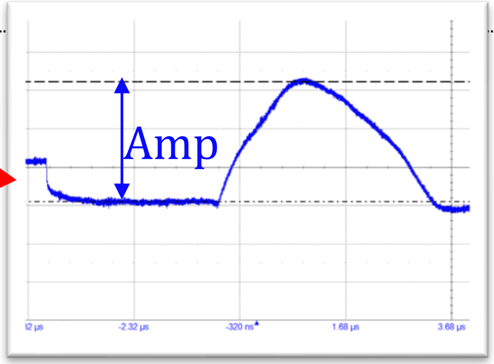
Noise

- Noise Rate represents the possibility of a pixel hit without any particle interactions
  - $R = \frac{\text{Noise Hit Counts}}{\text{Pixel Number} \times \text{Time}}$
- Noise reducing as the threshold increasing
- Noise reducing to **ZERO** as Bias Voltage increasing
  - Bias Voltage improves Noise performance

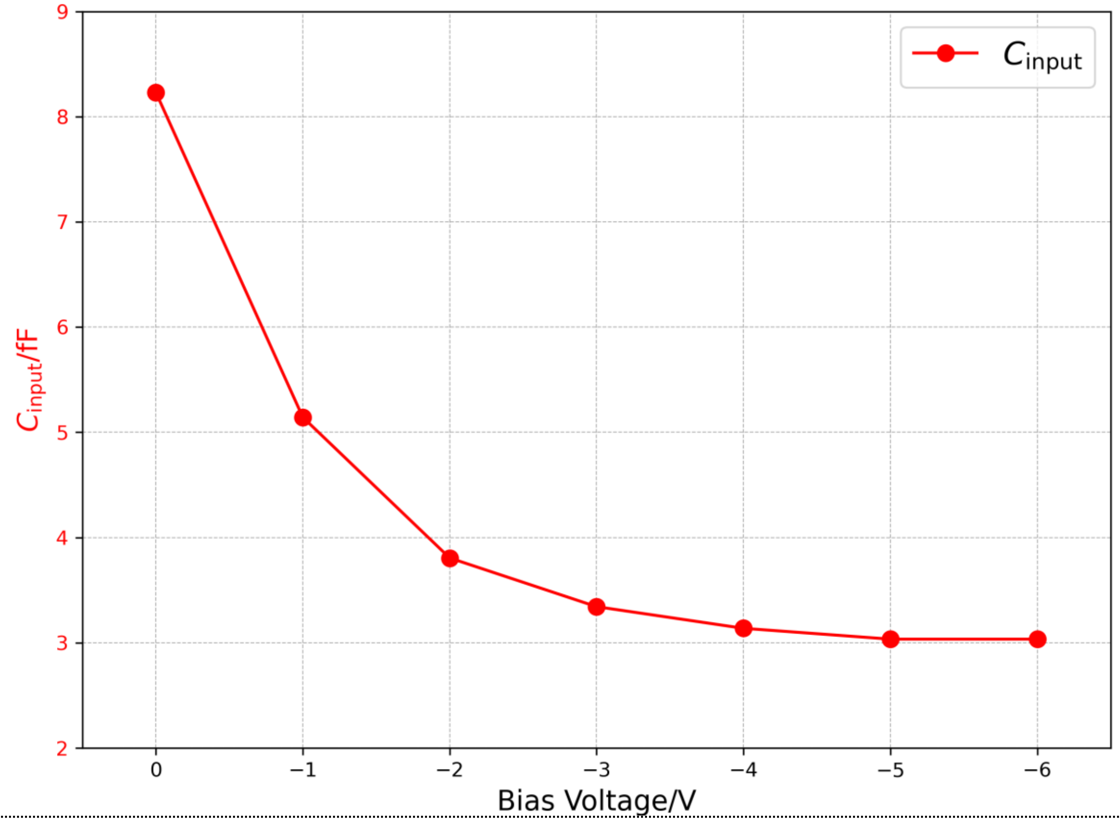


Input Capacitance

- Input Capacitance, C_{input} accessed by calculating analog response
- Smaller $\boldsymbol{C}_{\text{input}}$ increase voltage excursion and improves the SNR
- $\boldsymbol{C}_{\text{input}}$ reduced nearly **65%** as Bias Voltage increasing!

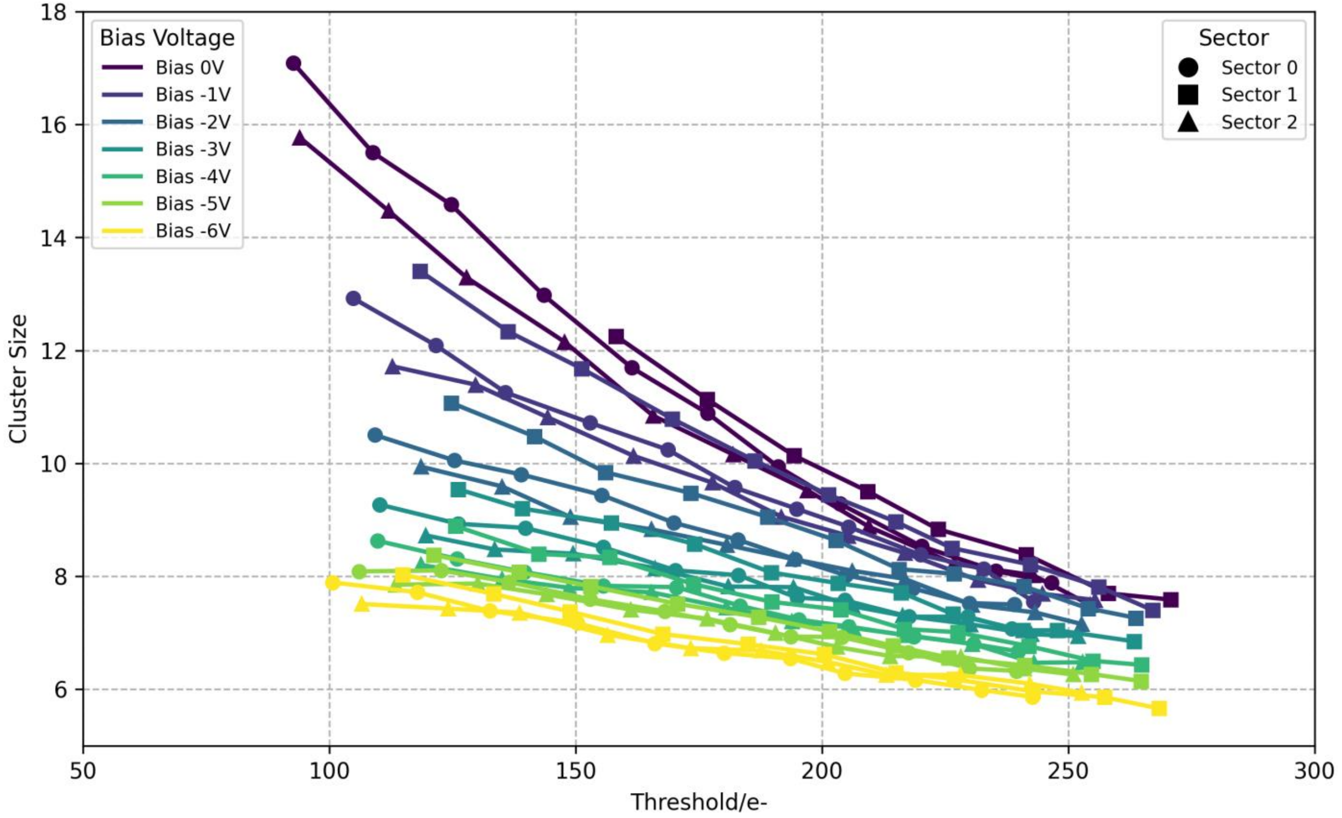


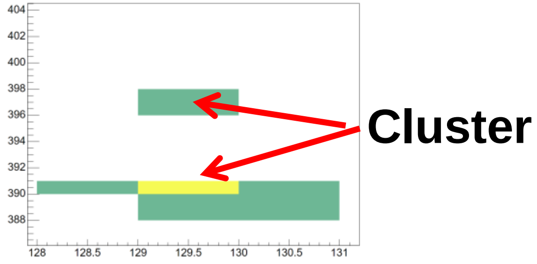
$$\text{Amp} = \frac{Q_{inject}}{\boldsymbol{C}_{\text{input}}} \cdot f_{gain} \cdot f_{sf}$$

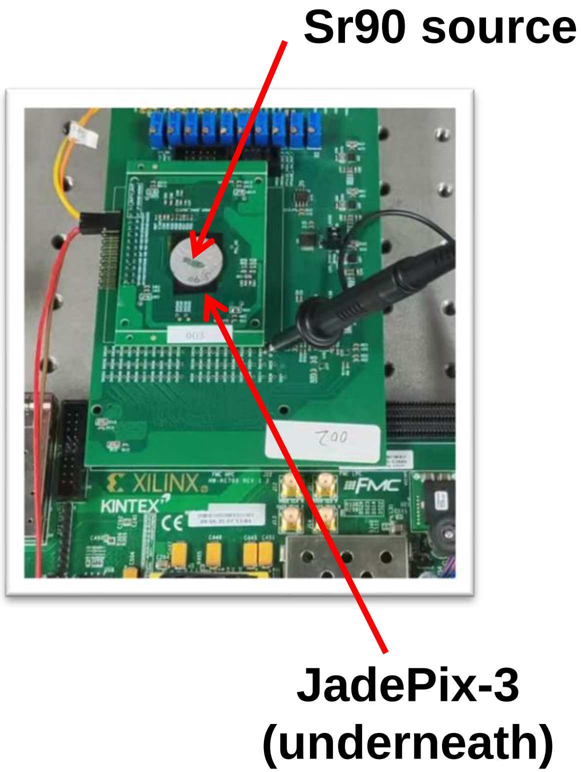


Charge Collection Ability

- JadePix-3 exposed to a Sr90(β) source with activity~1200 Bq
- Cluster Size reflects charge collection & localization ability
- Average Cluster Size reduced nearly **25%** as Bias Voltage increasing
  - Bias Voltage improves charge collection ability!



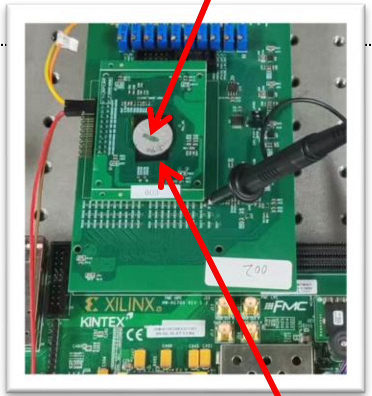




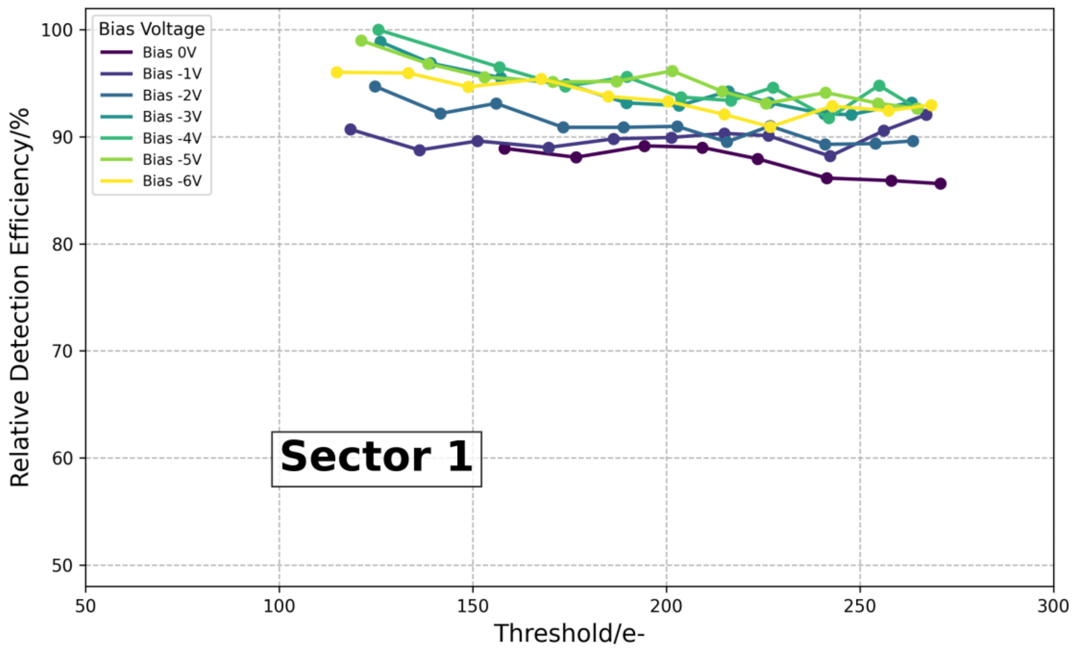
Relative Detection Efficiency

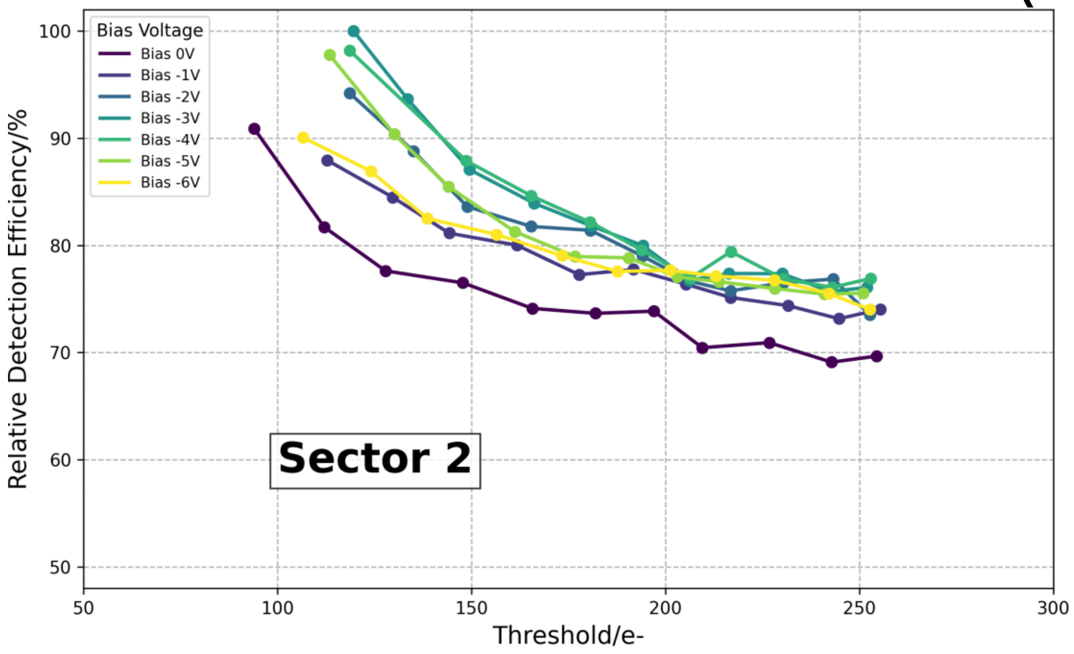
- JadePix-3 exposed to a Sr90(β) source with activity~1200 Bq
- **Relative** Detection Efficiency is proportional to cluster numbers accumulated
- Efficiency improved by **10%** from Bias Voltage 0V to -5V
  - Bias Voltage improves detection efficiency!
  - Sector 1(D-flipflop) exceeds Sector 2(RS-flipflop)

Sr90 source



JadePix-3 (underneath)

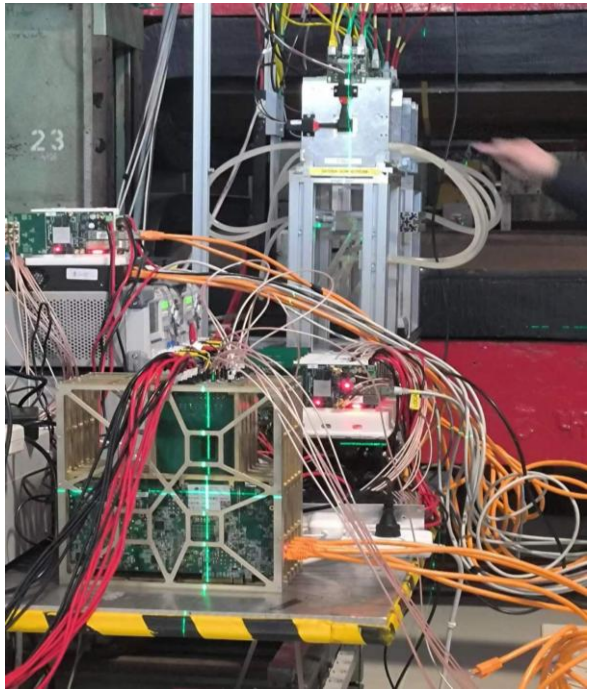




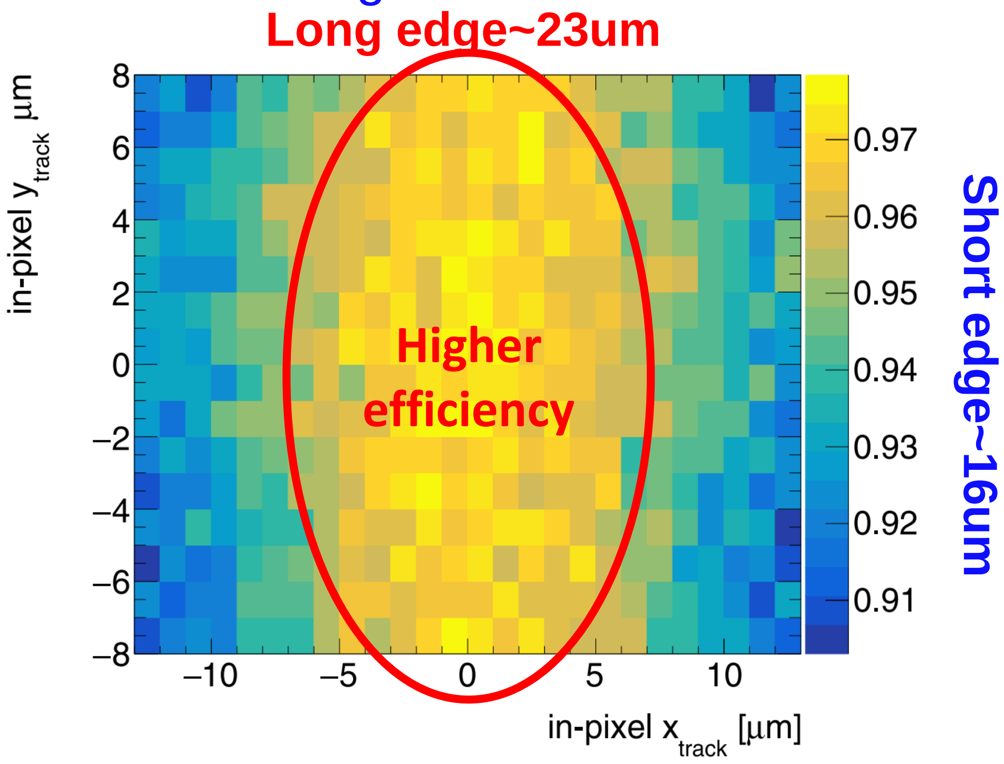
Previous Beam Test @DESY TB21

Sheng DONG, Jia ZHOU, Zhiliang CHEN, Yunpeng LU

- JadePix-3 exposed particle beam, up to 1000 particles per cm² and energies from 1 ~ 6 GeV
- In-pixel detection efficiency plot
  - Efficiency ~ 98%, Position Resolution ~ 5 μm
  - higher efficiency at the long edge center to the short edge center



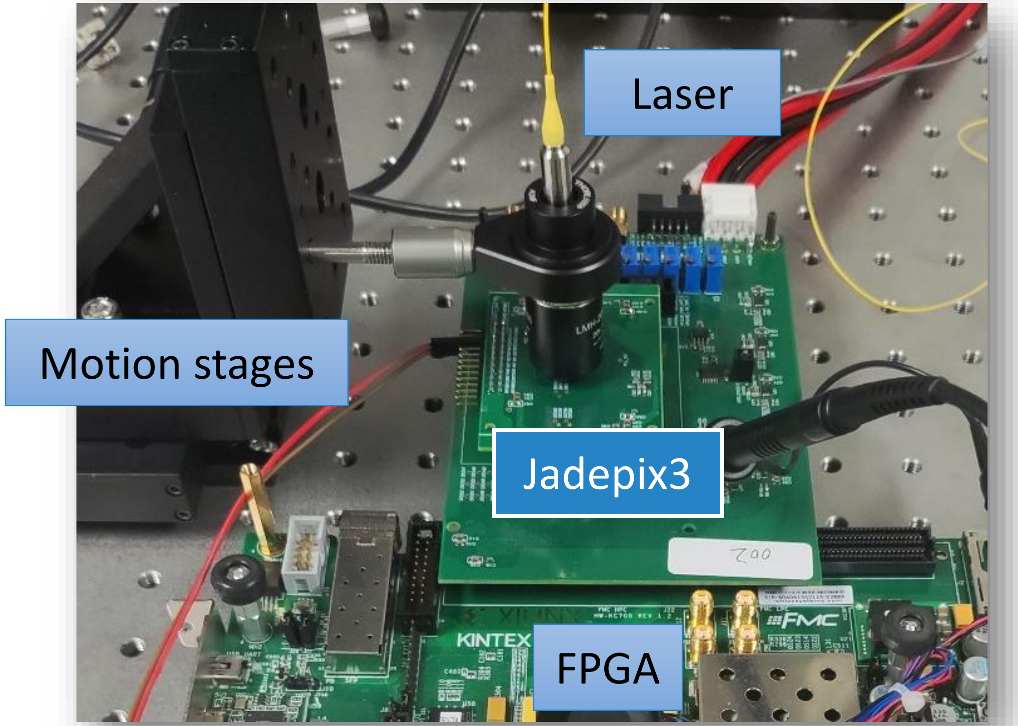
Test Setup @DESY Dec.2022



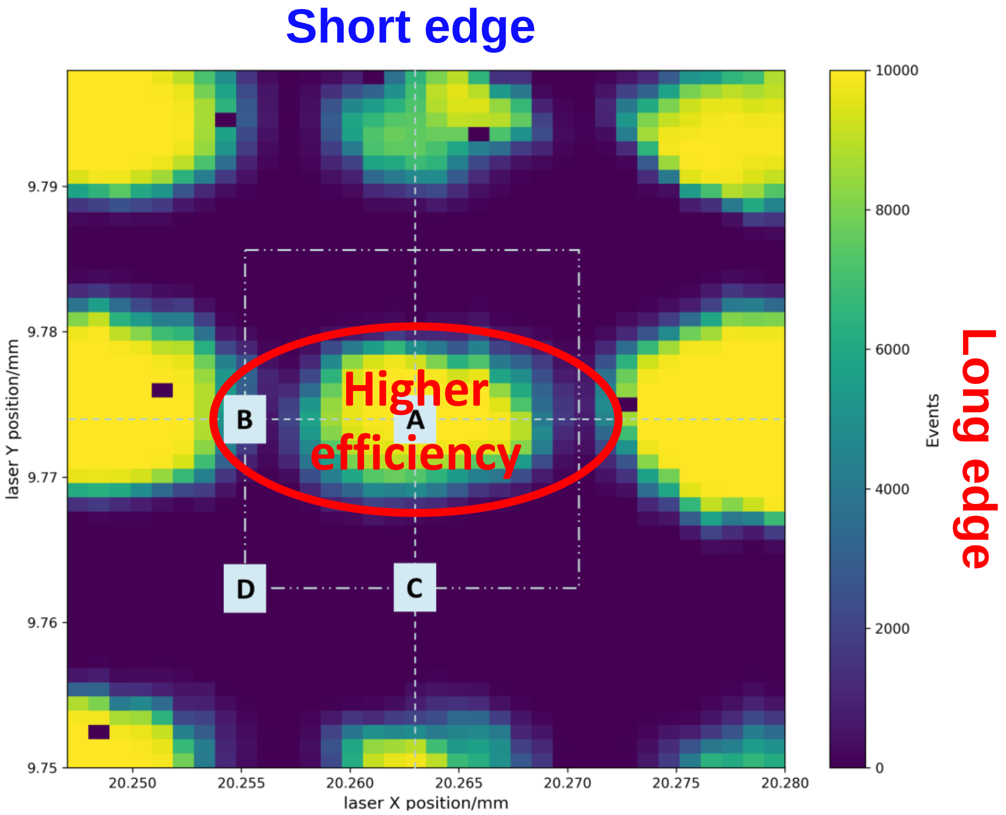
Beam test detection efficiency

Infrared Laser Test

- JadePix-3 exposed to laser beam with 1064nm wavelength
- X-Y scan performed @zero bias
  - Higher hit counts at the long edge center to the short edge center
  - Consistent with beam test



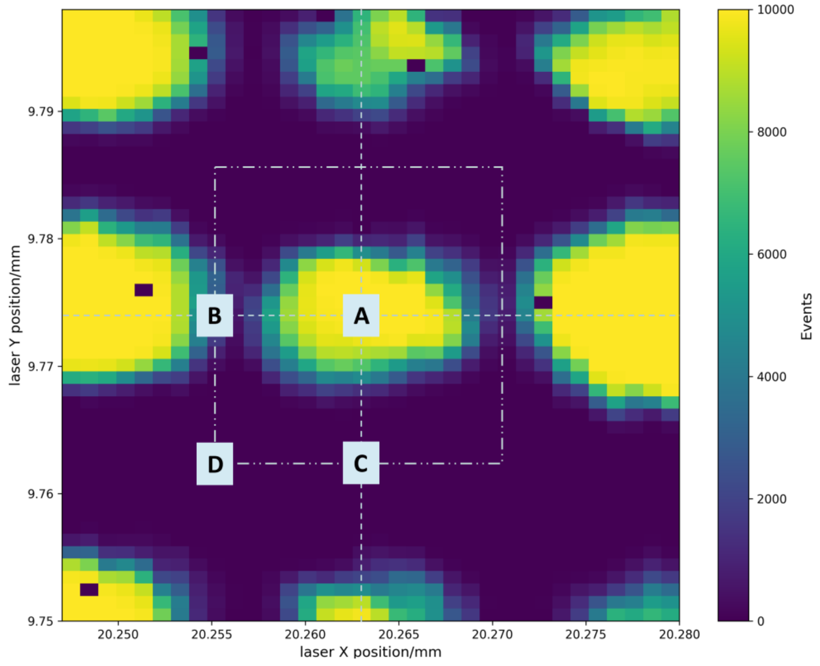
Laser Test Setup



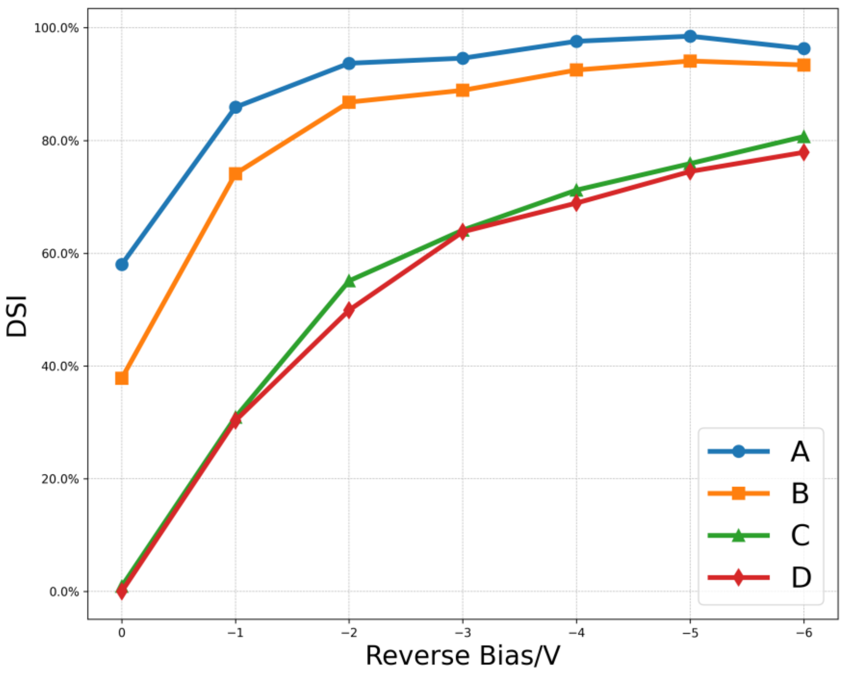
Laser scan

Infrared Laser Test

- **Detection Sensitivity Index (DSI), quantifying pixel sensitivity to laser**
  - **DSI** = Laser attenuation value where hit counts drop to half the maximum
  - Bias Voltage significantly improves overall detection efficiency to laser!



Laser scan



DSI vs. Bias Voltage

Summary

- JadePix-3 is designed for CEPC vertex detector
  - Optimized for high resolution, low power, low mass budget

- Performance enhanced under Bias condition:

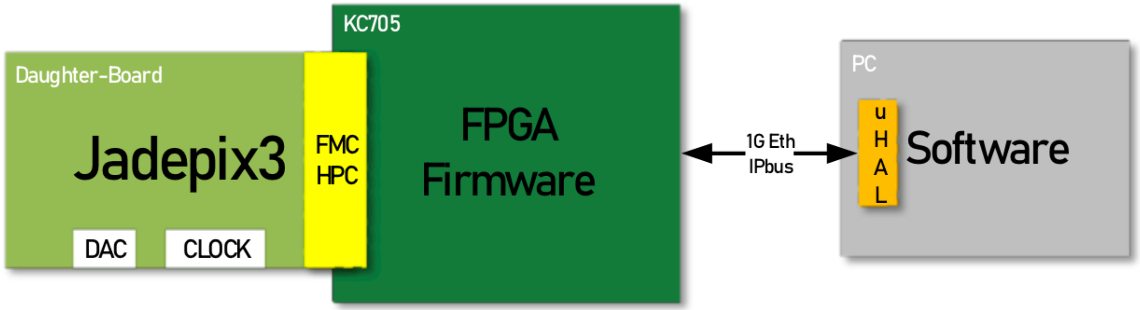
Noise	Input Capacitance	Charge Collection	Efficiency	Other performance
Reduce to ZERO	Reduced 65%	Improve 25%	Enhanced 10%	……

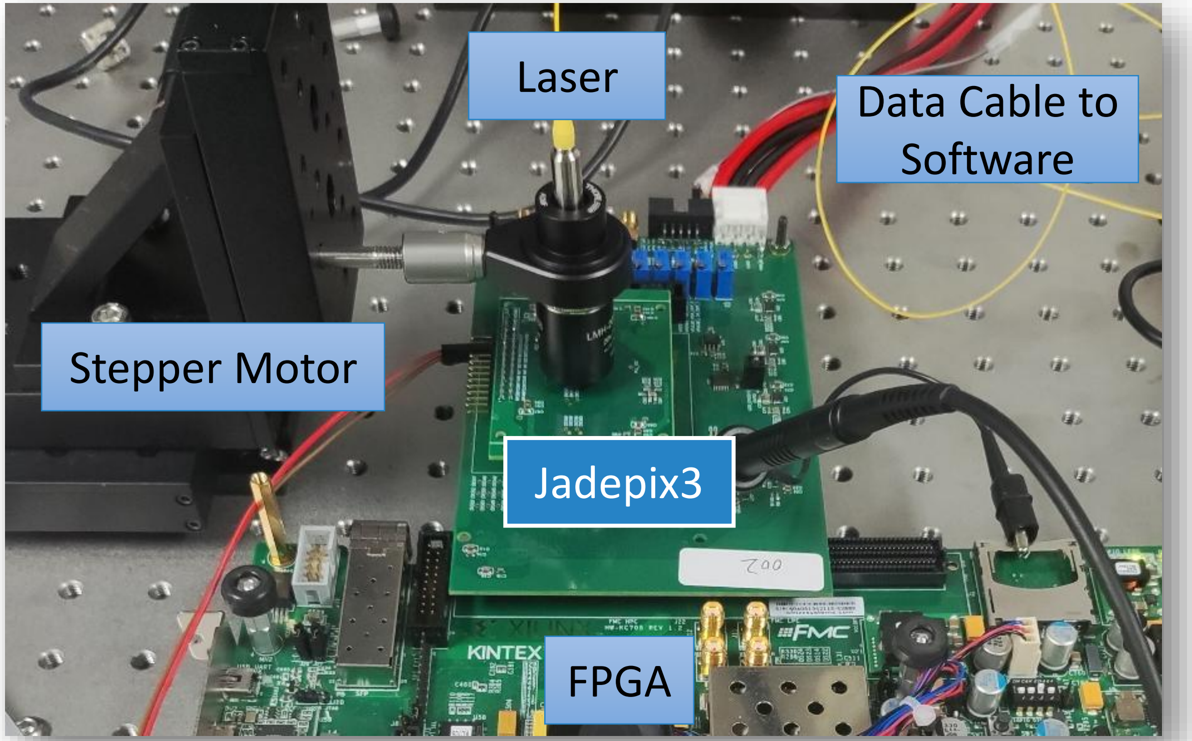
- Beam Test in preparation

感谢高能所卢云鹏老师提供的支持！

Back up

Test System Setup@USTC

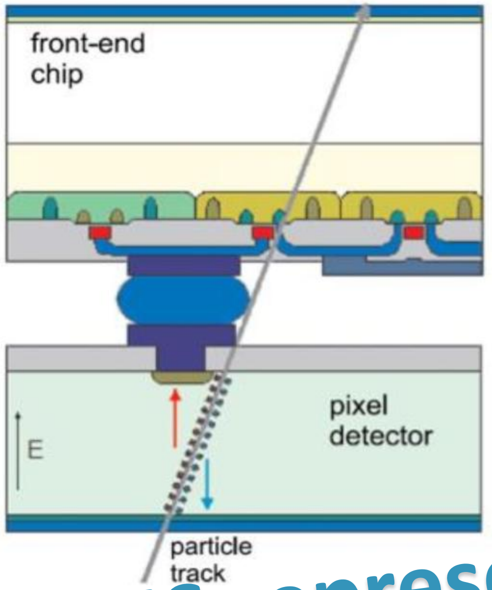




Silicon pixel detector

Hybrid

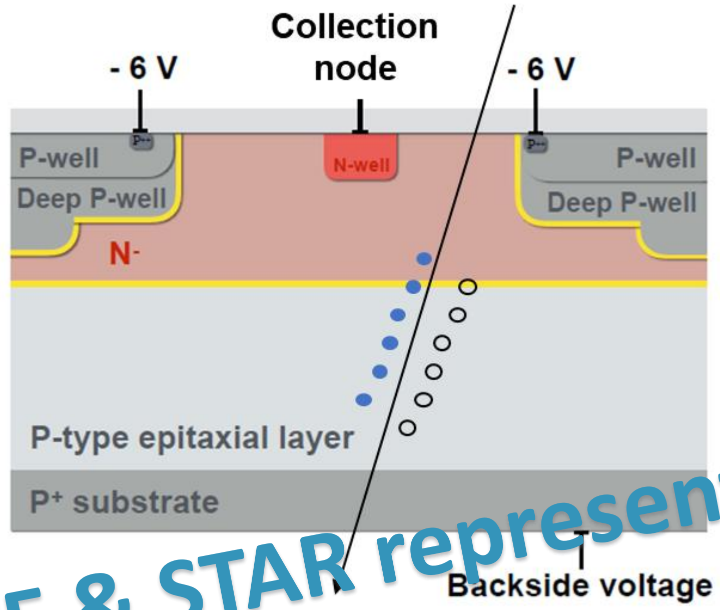
- Separately optimize sensor and FE-chip for very high radiation environment
- Fine pitch bump bonding to connect sensor and readout chip



ATLAS & CMS representative

Monolithic

- Charge generation volume **integrated** into the ASIC, but many different variants!
- Thin monolithic CMOS sensor, on-chip digital readout architecture

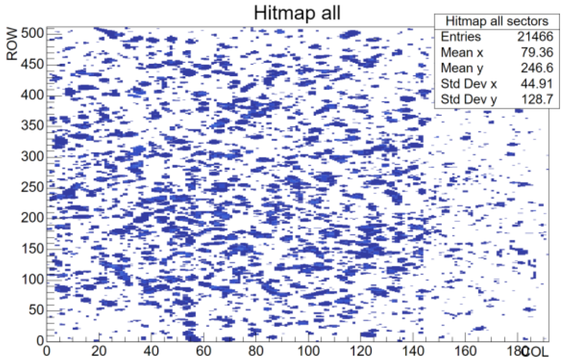


ALICE & STAR representative

Rolling Shutter(RS) Mode in JadePix-3

- Hit registered in each pixel has to be processed **fast**
  - Hit position (col. and row address) encoded
  - Time stamp attached
  - Register reset for the next hit

✓ Rolling Shutter Mode deployed
  - ✓ row address encoding
  - ✓ iterate over all rows → Take a shutter
  - ✓ Multiple frames → Long exposure



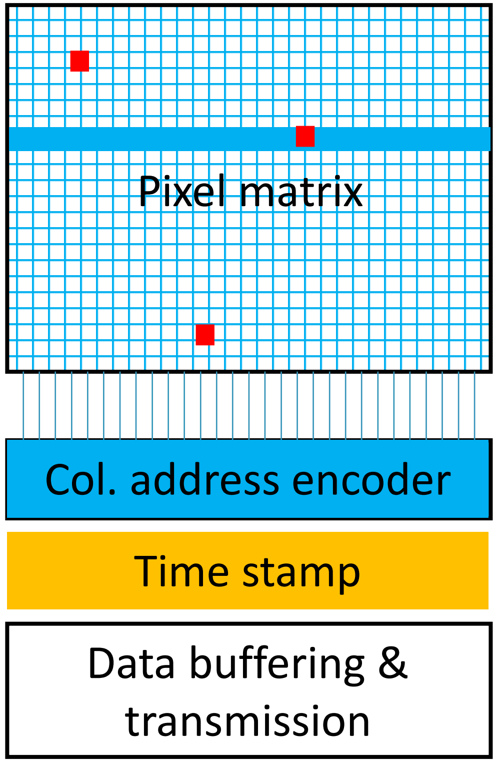
'Photo' took by RS under radio-source for 10,000frames

JadePix-3 flow

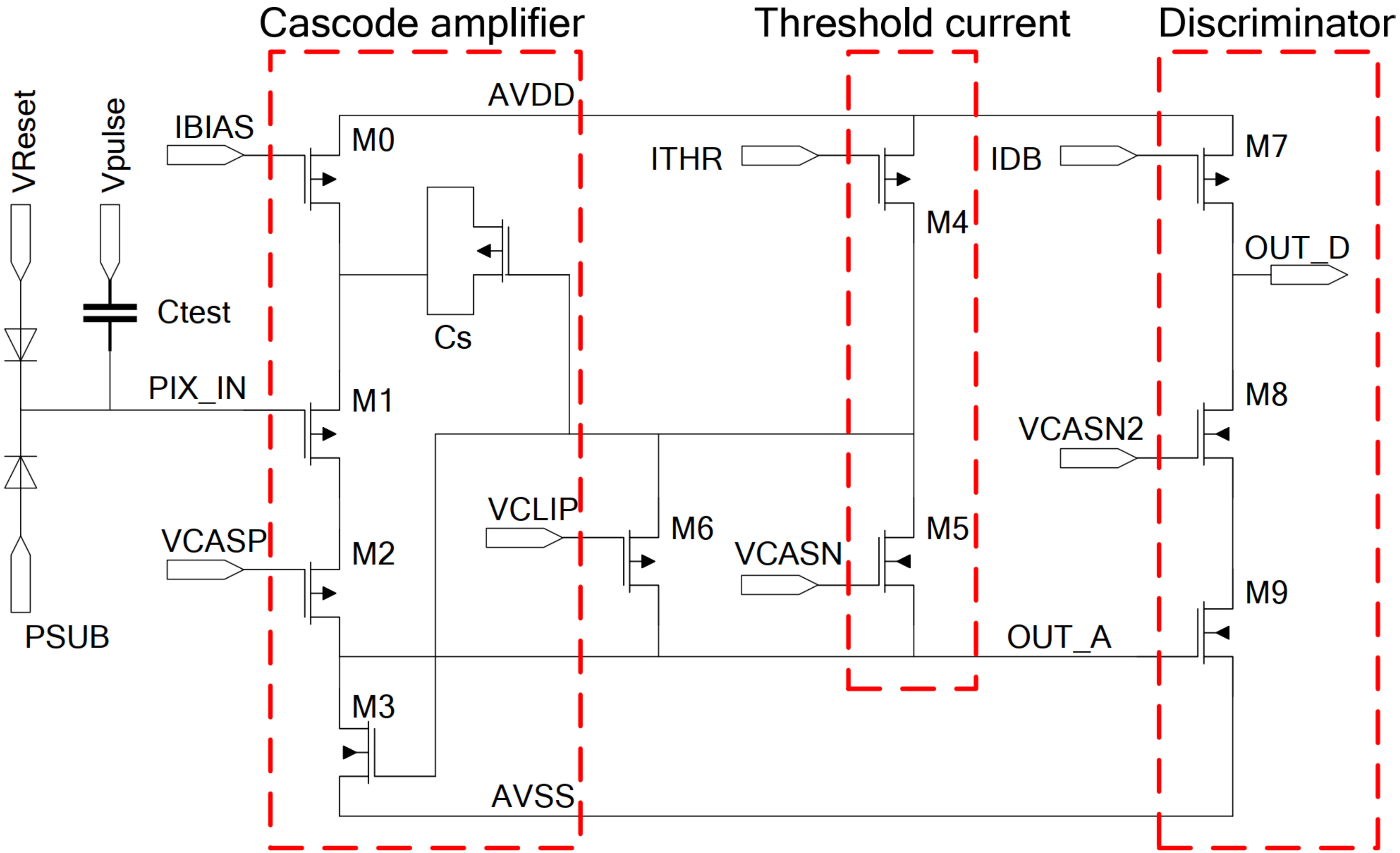
row address information extracted from the row selecting sequence (RS) →

col address encoded at the end of columns →

Time stamp attached to the generated hit address →



Front-end Circuit

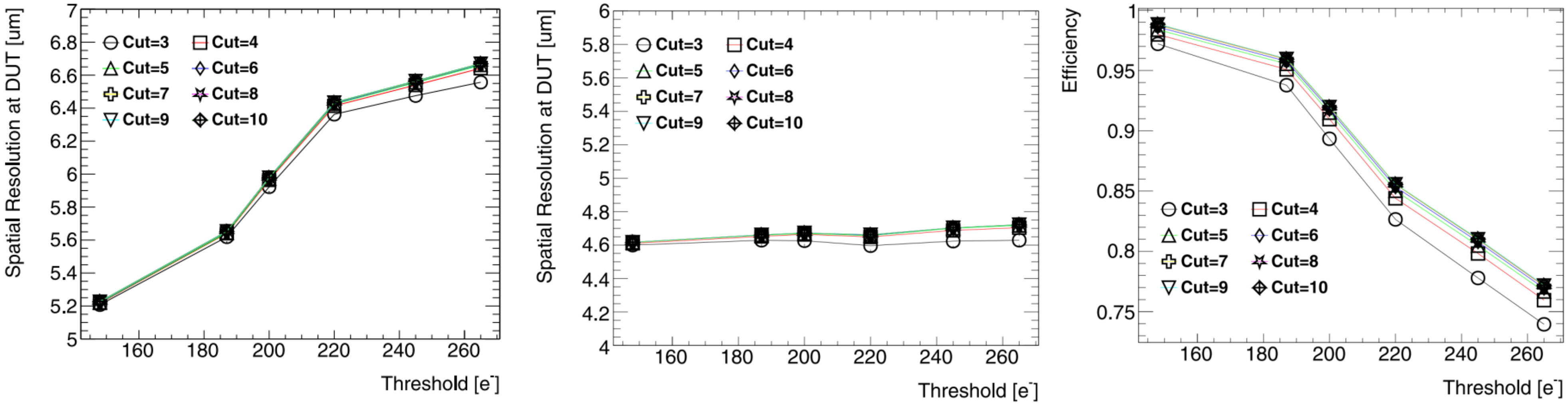


Beam Test Result

@DESY

Sheng Dong, Zhiliang Chen

- Electron beam energy = 5.8GeV
  - Demonstrated excellent spatial resolutions of 5.2 & 4.6 μm in two dimensions.
  - Threshold scan performed below:



X resol. vs. threshold **Y resol. vs. threshold** **Efficiency vs. threshold**

Requirement of Vertex detector @ CEPC

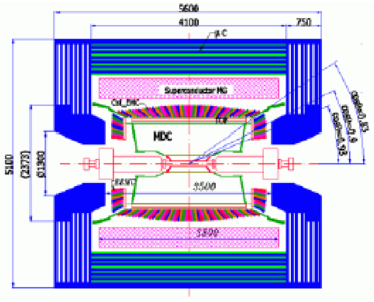
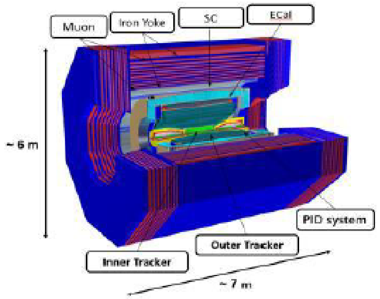
- Physics goals @ **CEPC**
  - Identify b/c quarks and tau leptons from Higgs
  - Perform a precise measurements of the Z boson

- Require a 3 μm spatial resolution
- Fast readout speed of 20 μs
- Very low mass budget (<0.15% X_0 / layer)
- Adequate radiation tolerance

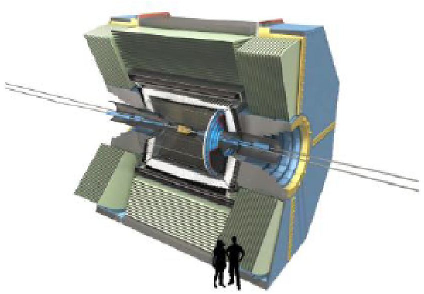
JadePix
MAPS

Requirements for e^+e^- @ different energy regions

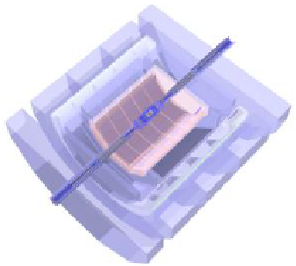
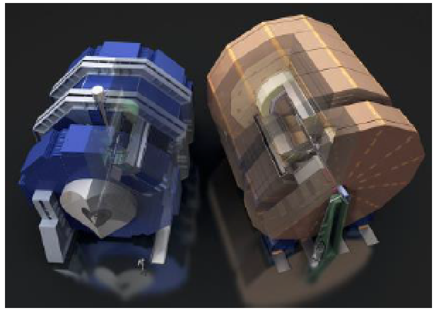
- Monolithic detector can meet different experimental needs
  - Design & optimize pixel chips for specific experimental needs

Charm: 2-7 GeV
BESⅢ upgrade / STCF
Sensitive to mass budget



Bottom: ~10.58 GeV
BELLEⅡ upgrade
Highest luminosity

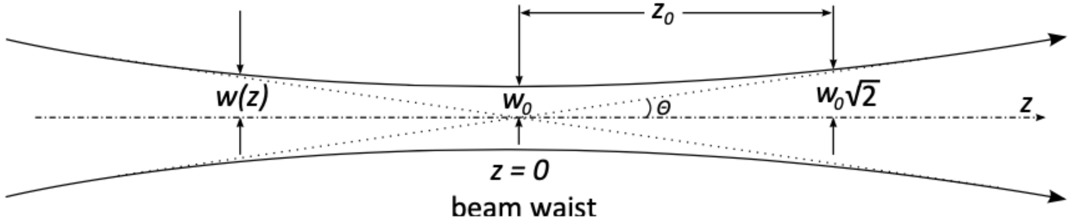



Higgs: 240-250 GeV
CEPC / ILC
Highest precision

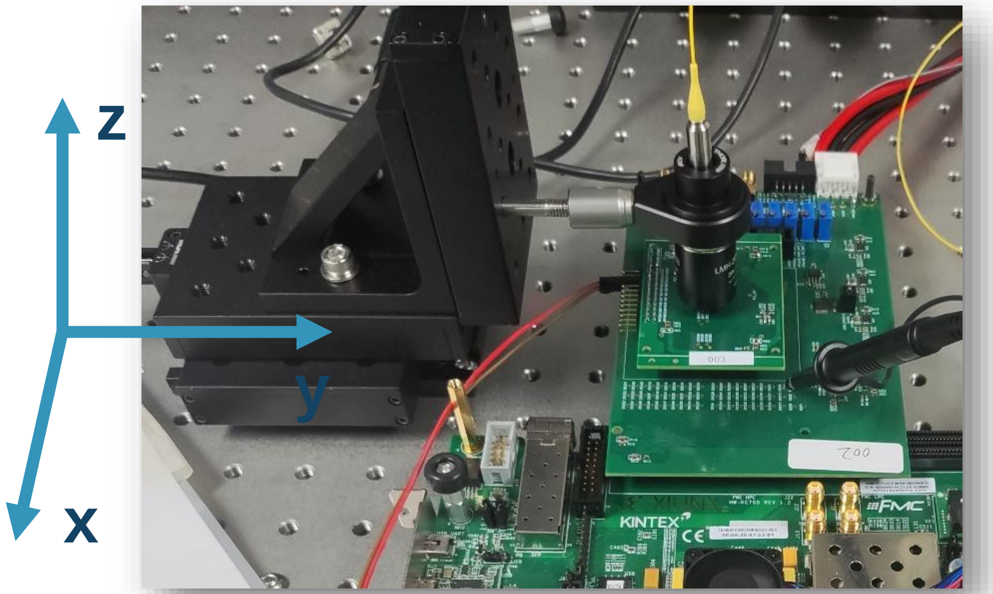
High precision, fast readout,
low power, low mass budget ← **MAPS**

Infrared Laser Test

- Test procedure
  - 1.Scan in z-direction, zero bias to determine the position of beam waist.
  - 2.Scan in xy-direction, 0V/-1V/-2V bias and tune 95%/99%.
  - 3.*Residual=Reconstruct - Motor*
    - Gauss fit
    - Case-by-case statistics
    - Point-by-point statistics



Laser Beam



Laser Test Platform

Infrared Laser Test

Bias(V),Tune	Point-by-point statistics		Case-by-case statistics	
	Column Resolution/um	Row Resolution /um	Column Resolution/um	Row Resolution /um
0,95%	**1.92**	**1.68**	3.26	3.21
0,99%	**4.16**	**1.97**	4.67	3.36
-1,95%	**2.33**	**1.75**	3.13	2.74
-1,99%	**2.05**	**2.29**	2.96	3.20
-2,95%	**3.24**	**1.76**	3.71	2.63
-2,99%	**2.49**	**1.78**	3.11	2.65