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The progress of the MTCA.4 based LLRF system in LUTF

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Outline

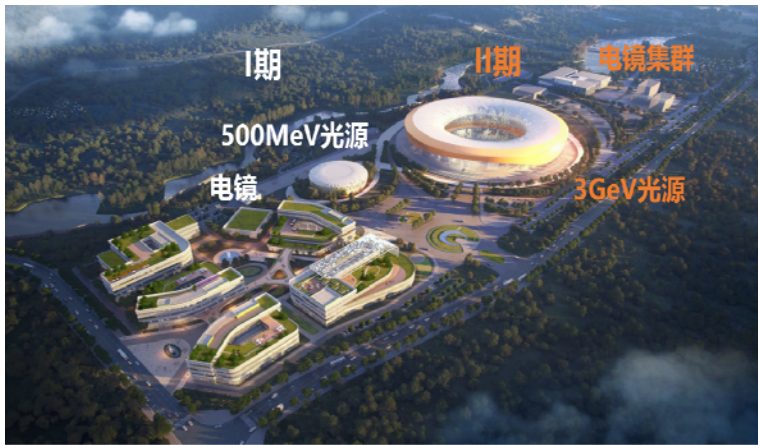
1. Brief introduction of LUTF
2. The progress of LLRF
 - 2.1 LLRF
 - 2.2 SSA, CLK&LO
 - 2.3 Timing system
 - 2.4 Klystron acceptanc
3. Summary

1. Brief introduction of LUTF

Laboratory for Ultrafast Transient Facility (LUTF) is composed of a synchrotron radiation light source and an electron microscope.

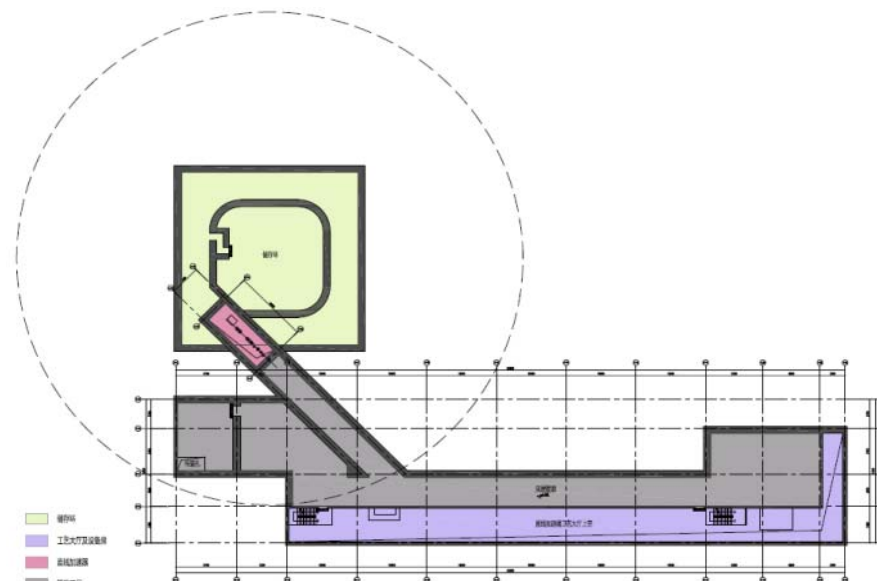
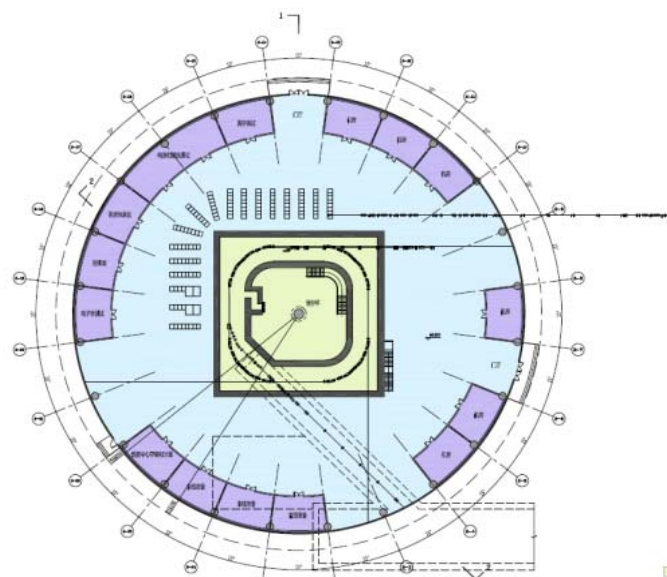
LUTF is developed in 2 phases, phase I is a pre-research project, including a 500MeV light source and an electron microscope platform; phase II including a 3GeV light source and an electron microscope cluster.

Project duration: 2023.5~2026.5

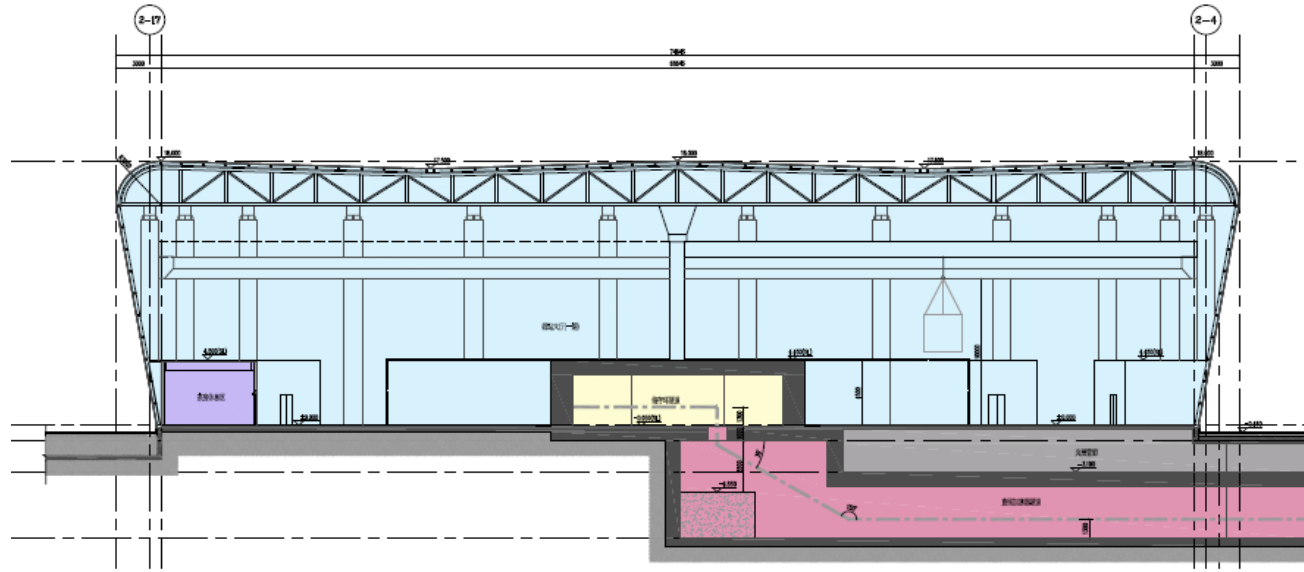


Parameters of 500MeV ring

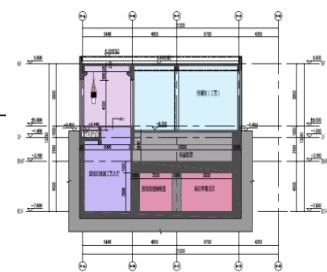
Parameters	Value	Unit
Energy	0.5	GeV
Ring circumference	76.78	m
Beam current	0.5~1	A
Focusing type	QBA	
Natural emittance	8.56	nm rad
Working point (x, y)	6.198, 3.357	-
Length of straight section	8*4	m
Working frequency	499.8	MHz
Energy loss per turn	4.34	keV
Natural energy spread	0.37×10^{-3}	

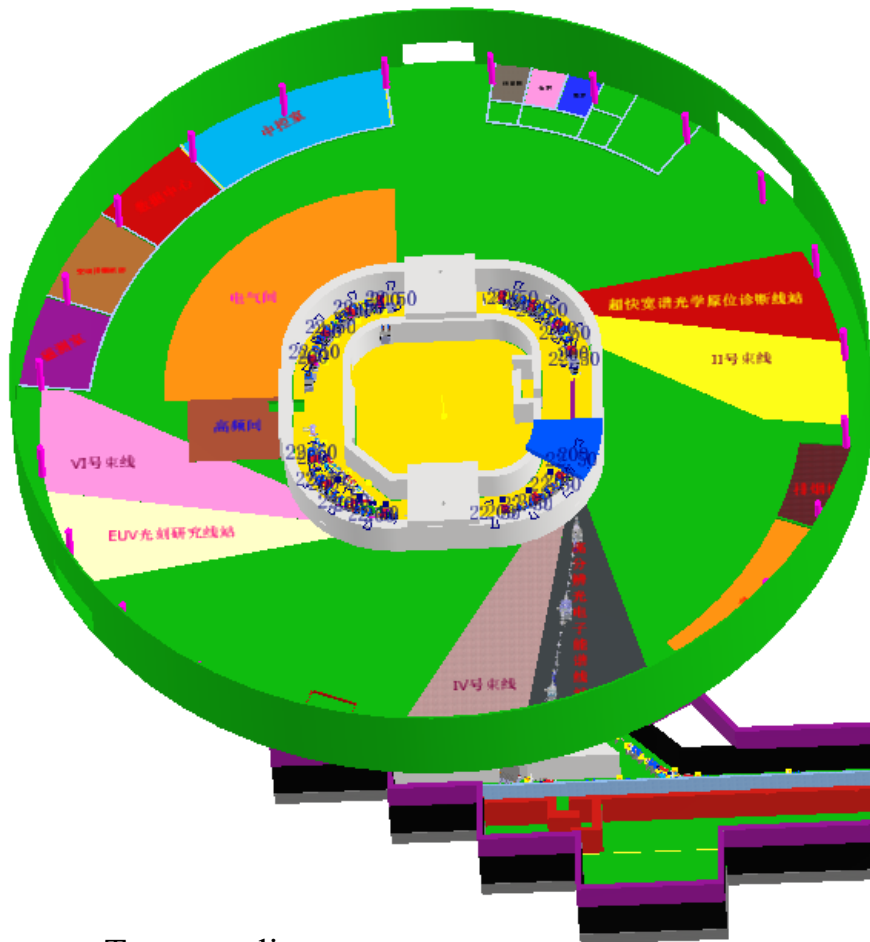


- 展览厅
- 工业材料及设备库
- 基础及结构
- 结构



2-2剖面图





Storage ring:

76.78m,

500MeV,

4 focusing sections (QBA) ,

4 straight sections,

6 beam extraction ports,

multipole kicker injection (1 Septum and 1 NLK)

1st beamline: ARPES(Angle resolved photoemission spectroscopy)

Transport line:

A climbing section

Linac:

500MeV,

7.6m underground,

a thermionic cathode electron gun,

S band accelerating structure,

Timeline of LUTF:

2024/04

Facility construction starts

2025/01

Linac starts install

2025/04

Storage ring starts install

2026/05

Project completed



Test platform(2024.09.14)



Research building (2024.7.17)

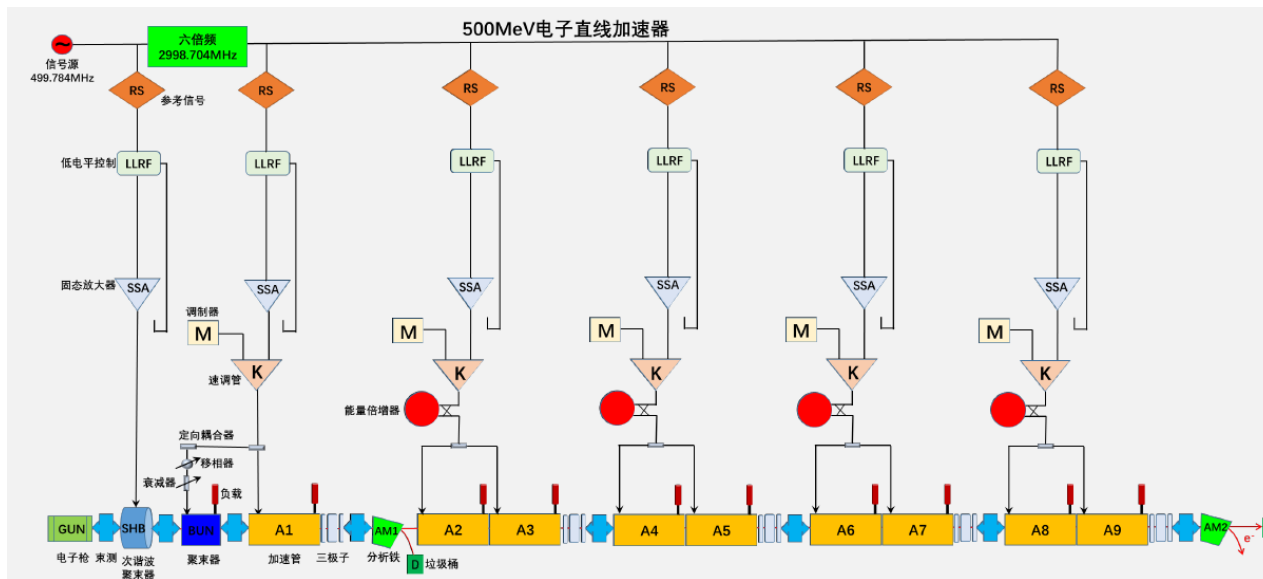


Powerhouse(2024.7.17)



Linac (2024.7.17)

2.The progress of LLRF



The layout of the Linac

Parameters of 500MeV Linac

Parameters	value	unit
Beam energy	500	MeV
Beam charge	≥ 1	nc
Beam length	≤ 1	ns
Energy spread	≤ 0.5 (rms)	%
Normalized emittance	≤ 50 (rms)	mm.mrad
Repetition rate	2	Hz
Working frequency	2998.704	MHz

2.1 LLRF



NATIVE-R2



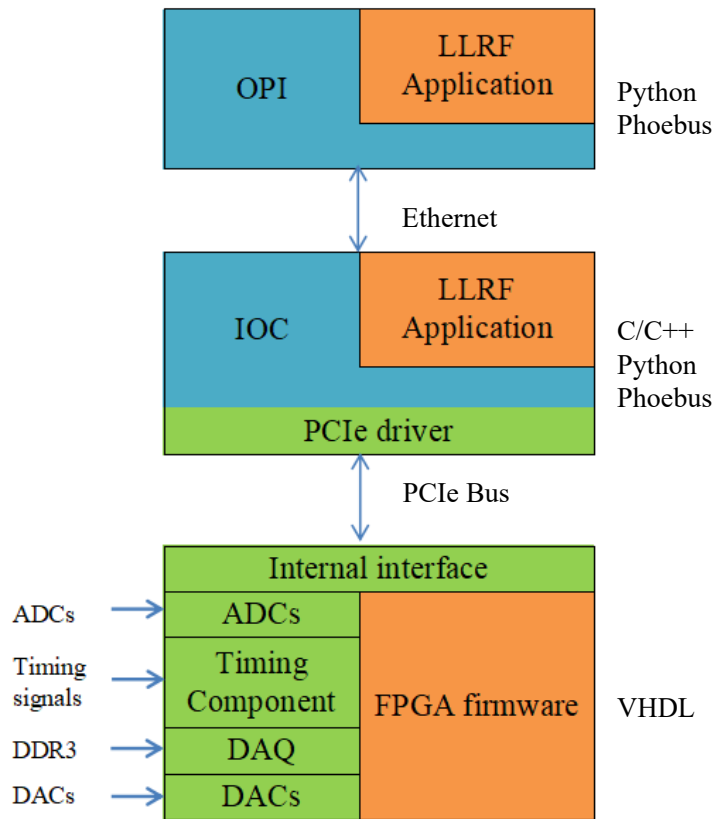
DWC8VM1



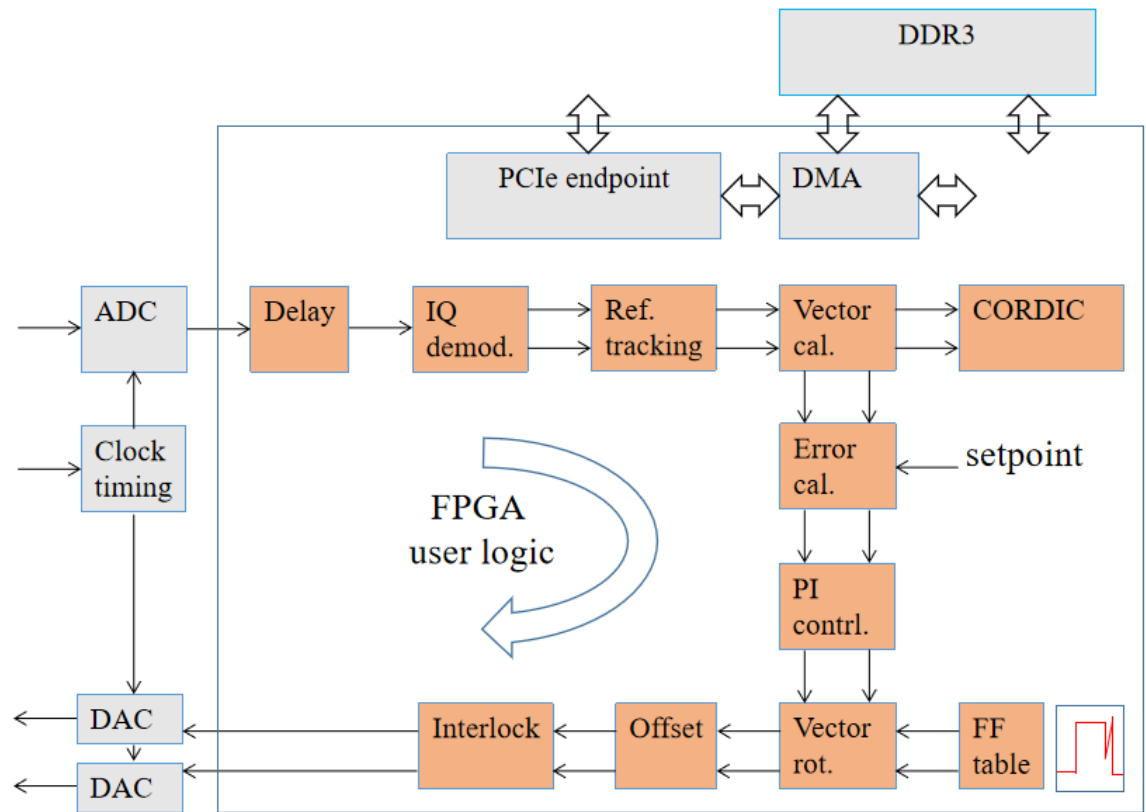
SIS8300KU

SIS8300-KU Properties

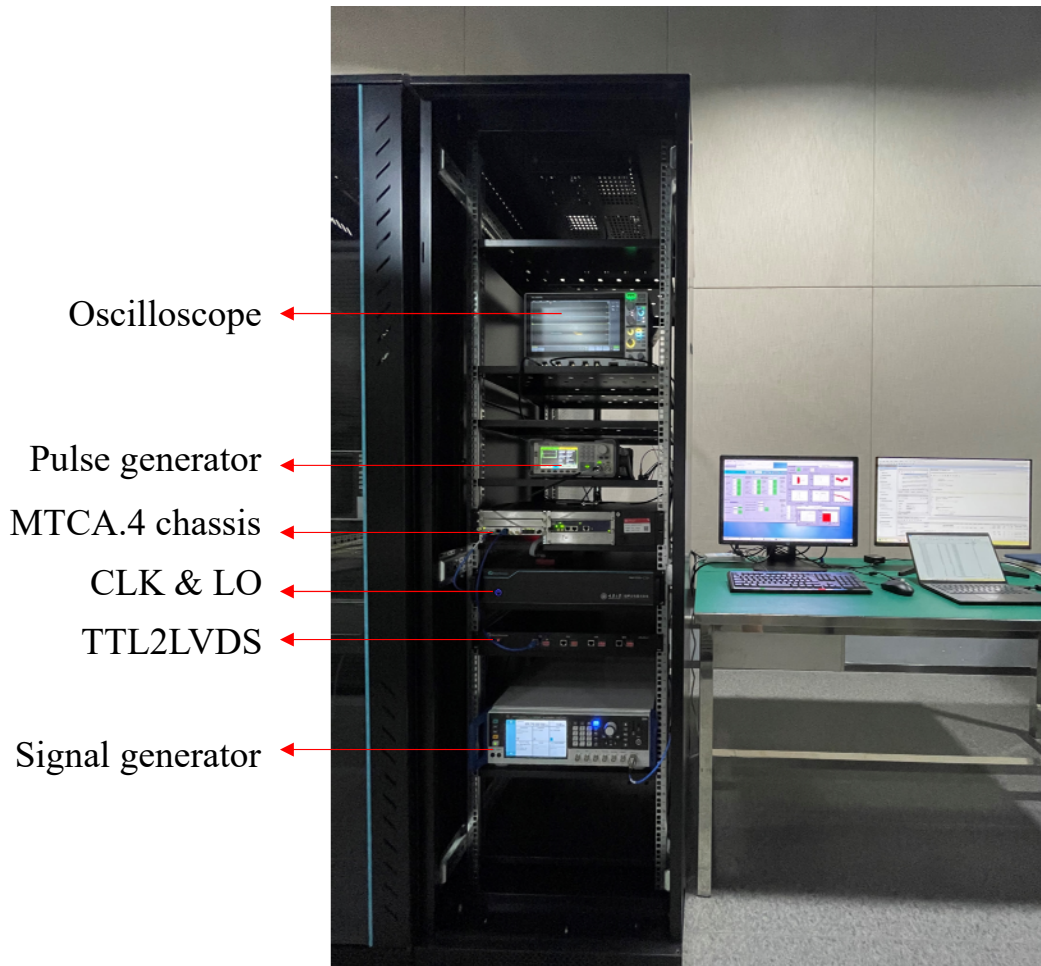
- 10 Channels 125 MS/s 16-bit or 250 MS/s 14-bit ADC
- 10 MS/s to 125 MS/s Per Channel Sampling Speed
- AC or DC Input Stage
- Internal, Front Panel, RTM and Backplane Clock Sources
- Two 16-bit 250 MS/s DACs for Fast Feedback Implementation
- High Precision Clock Distribution Circuitry
- Programmable Delay of Dual Channel Digitizer Groups
- Multi Gigabit Link Port Implementation to Backplane
- Twin SFP+ Card Cage for High Speed System Interconnects
- **White Rabbit Clock Option for SFP+ Ports**
- **Two RJ45 Connectors** (One Clock + 3 Data or 4 Data In/Out)
- **XCKU040-1FFVA1156C Kintex Ultrascale FPGA**
- 2 GByte DDR4 Memory (flexible partitioning scheme)
- 4 lane PCI Express Gen3 Connectivity
- Dual boot
- MMC1.0 under DESY license LV91
- In Field Firmware Upgrade Support
- **Vivado Project for Custom Firmware Development**
- Zone 3 class A1.0, A1.0C or A1.1CO Compatible



Software and firmware



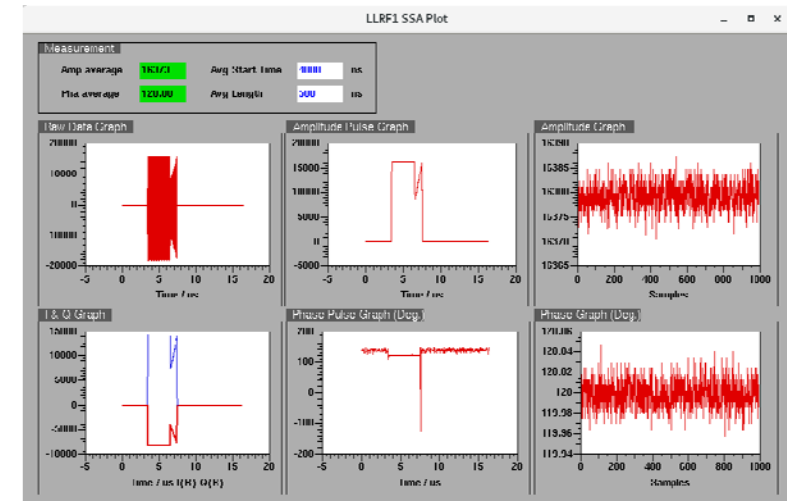
Firmware of SIS8300KU



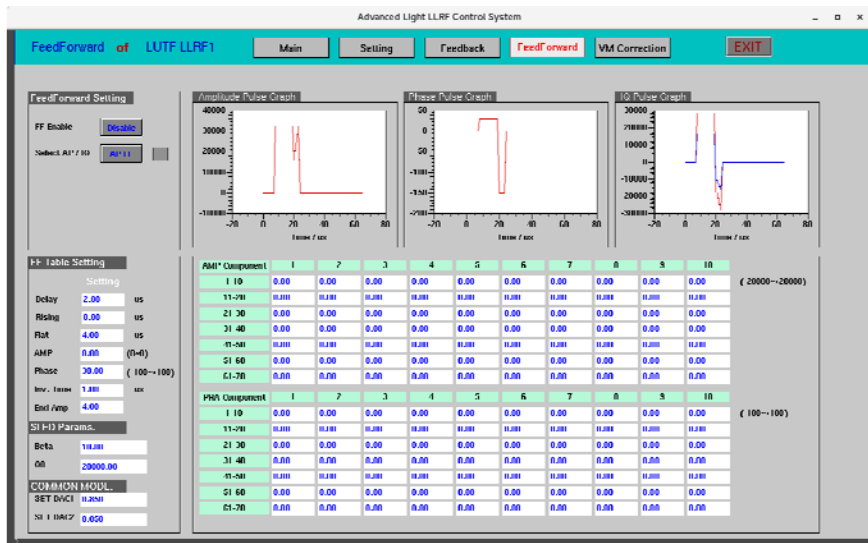
LLRF platform

LUTF frequencies

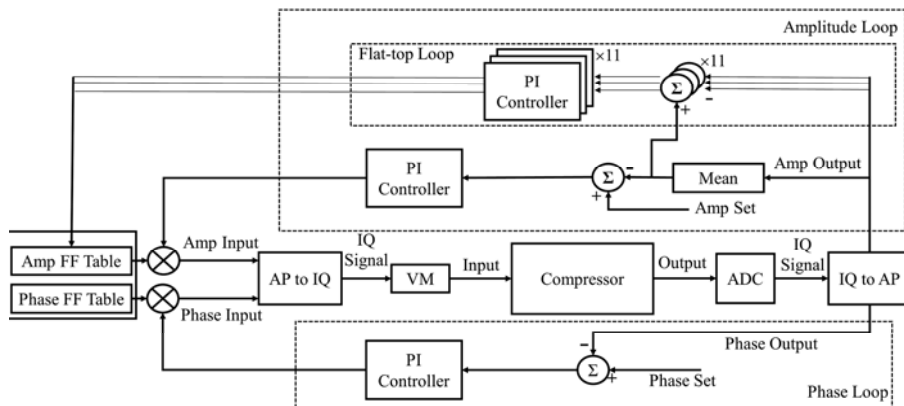
No.	Items	Frequency
1	Main RF	499.79/2998.74MHz
2	LO	474.80/2973.75MHz
3	IF	24.99MHz
4	ADC Clock	124.95MHz



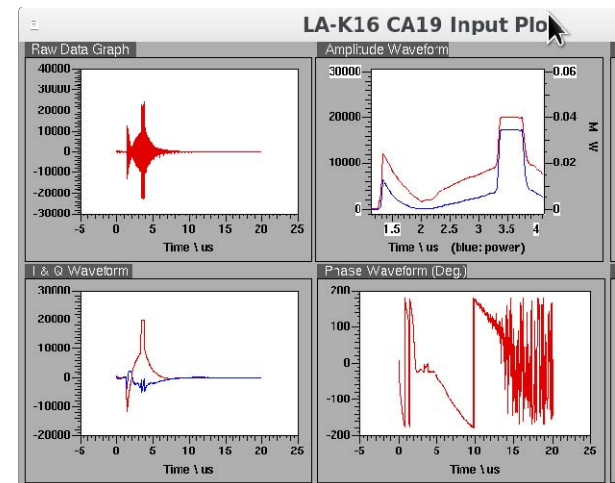
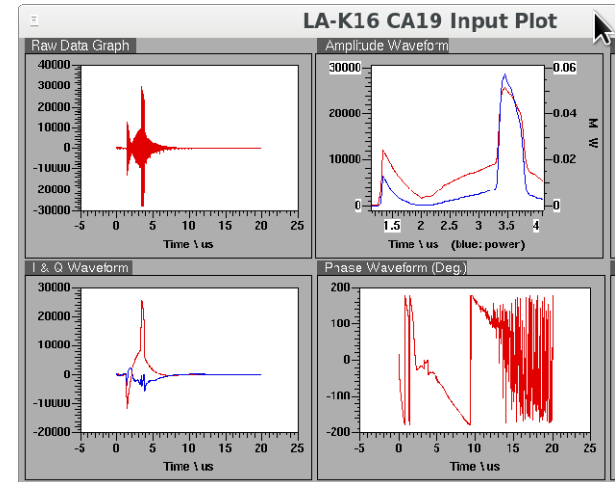
Amplitude and phase stability:
0.01% (rms) , 0.01° (rms)



Interface of FF table



The feedback algorithm of amplitude modulation



Amplitude modulation

2.2 SSA, CLK&LO

1. Working frequency: 499.790/2998.74MHz
2. Input power (CW) : 0-3dBm
3. Ref. signal power (CW) : $\geq 15\text{dBm}$
4. LO signal power (CW) : $\geq 15\text{dBm}$
5. Clock signal power (CW) : $\geq 15\text{dBm}$
6. LO phase noise: $< 50/36\text{fs} @ [10\text{Hz}, 10\text{MHz}]$
7. Harmonic suppression: $> 50\text{dBc}$
8. Spurious noise suppression: $> 65\text{dBc}$
9. Power stability: $< \pm 0.1\text{dB} (1\text{min})$

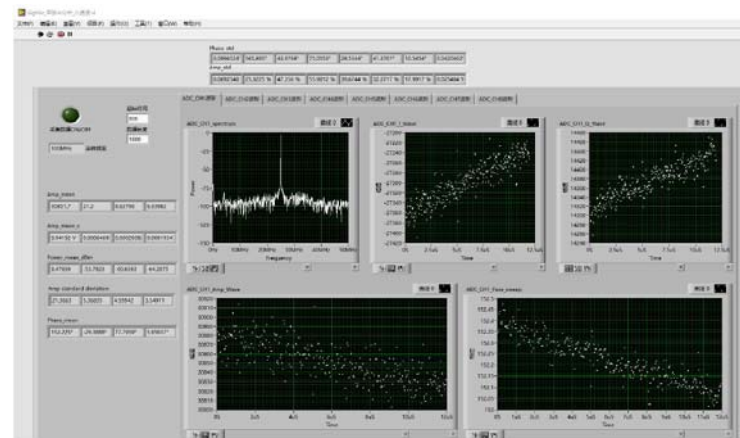
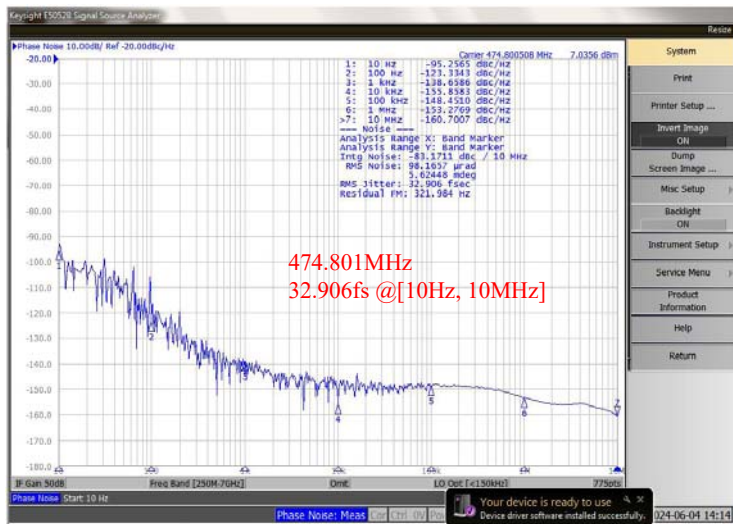


CLK & LO

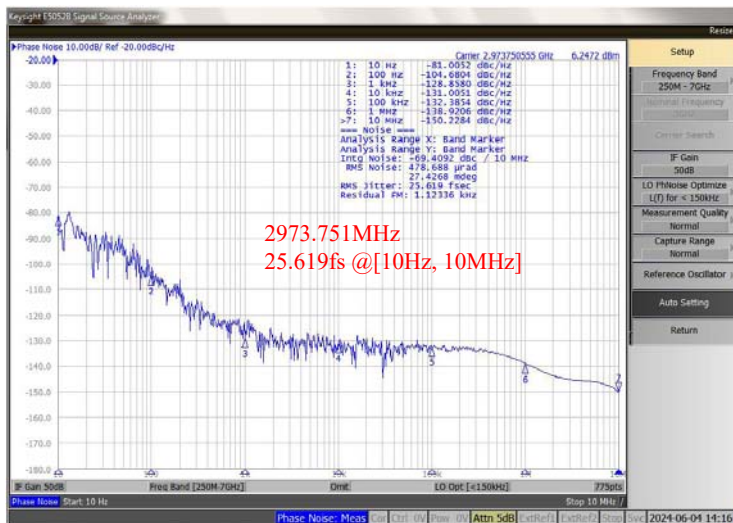
1. Working frequency: 499.784MHz/2998.704MHz
2. Bandwidth: $\geq \pm 2.5\text{MHz}@1\text{dB}$
3. Pulse width: 0.5-30 μs /0.5-4 μs
4. Repetition rate: 1-50Hz
5. Output power: $\geq 2000\text{W}/1000\text{W}$
6. Rising edge/Falling edge: $\leq 0.1/0.1\mu\text{s}$
7. Rising edge jitter: $\leq 5\text{ns}$
8. Pulse flatness: $\leq 0.2\% (\text{rms})$
9. Pulse phase shift: $\leq 1^\circ (\text{rms})$
10. Amplitude stability: $\leq 0.02\% (\text{rms})$
11. Phase stability: $\leq 0.02^\circ (\text{rms})$



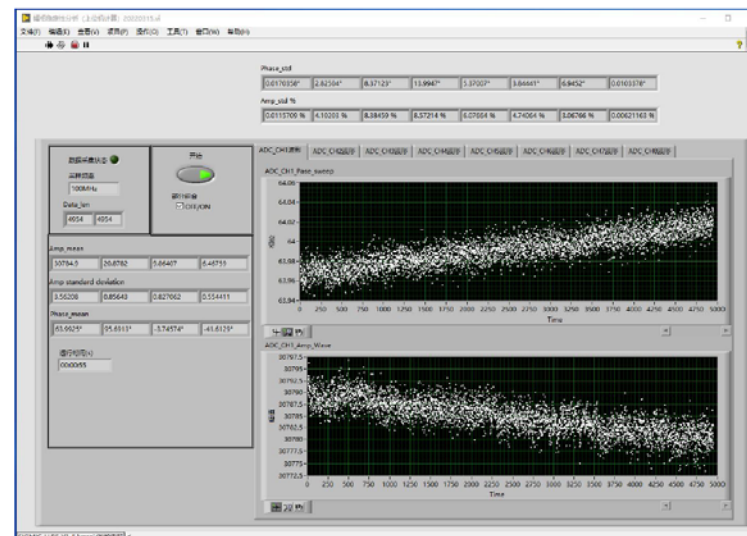
Solid state amplifier



Pulse flatness and phase shift



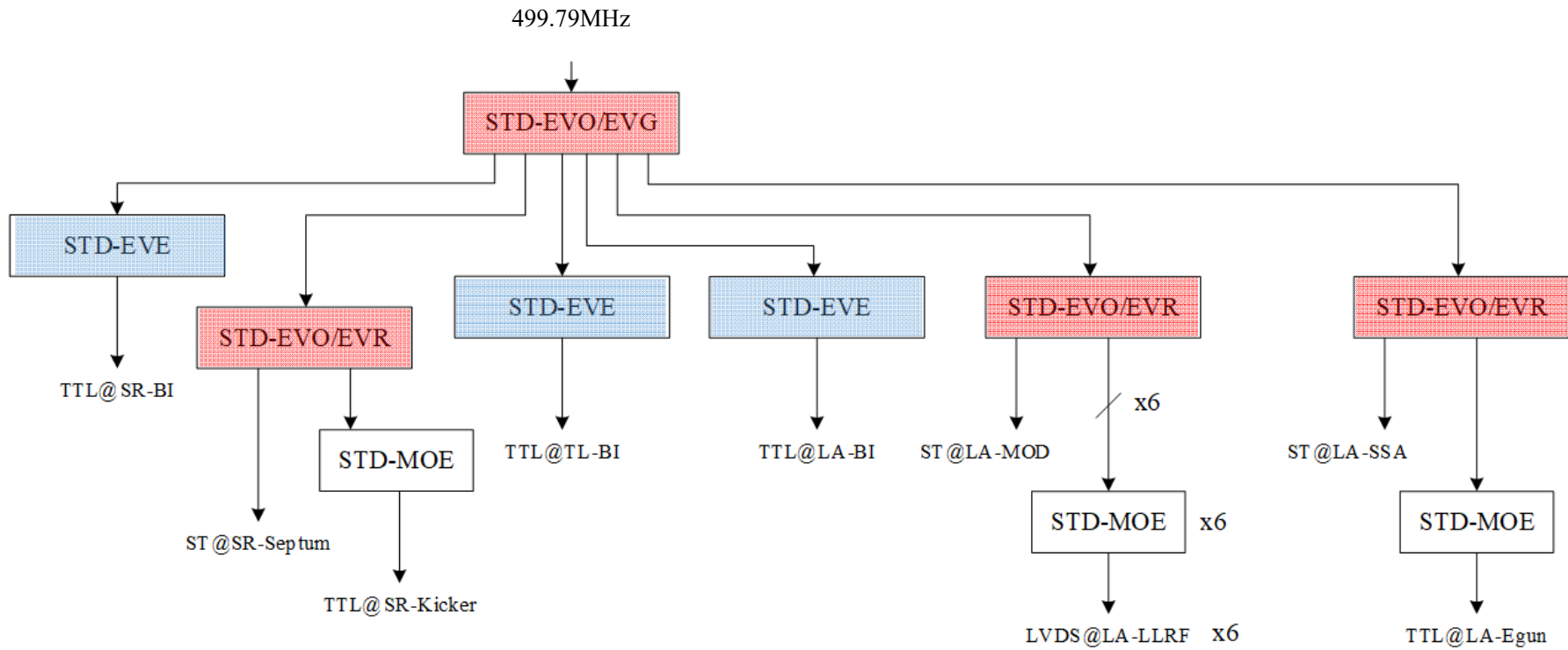
The phase noise of LO signals



Amplitude and phase stability

2.3 Timing system

Facility	Equipment	Num.	Pulse width	Delay step	Jitter(RMS)	Connector
Linac	E-gun	1	1ns	5ps	30ps	BNC
	Modulator	5	4 μ s	10ns	150ps	ST
	Solid state amplifier	6	4 μ s	10ns	150ps	ST
	LLRF	6	4 μ s	10ns	150ps	*RJ45
	Beam inspection	3	4 μ s	10ns	150ps	SMA
Transport line	Beam inspection	3	4 μ s	10ns	150ps	SMA
Storage line	LLRF	2	4 μ s	10ns	150ps	SMA
	Septum	1	60 μ s	10ns	150ps	ST
	NLK	1	0.5 μ s	5ps	150ps	BNC
	Beam inspection	9	4 μ s	10ns	150ps	SMA
	Beam inspection	7	4 μ s	10ps	150ps	SMA
	Beam line					



The layout of timing system



STD-EVO

19 inches 1U standard chassis,

110/220V 50-60Hz AC power supply

- Configured as EVR, EVG and FANOUT by software
- event clock delay, 1/20 event clock delay, 5ps/step delay
- event clock frequency range is 60 – 135MHz
- RF clock frequency range is 60 – 500MHz,
- Support cascaded EVG function with different event clock frequency
- Embedded IOC installed (uclinux 2.6.30.4)

In front panel:

- 1 RF clock input (0–10dBm)
- 1 interlock / AC-line input (TTL)
- 1 fiber input (SFP module)
- 8 fiber output (SFP module)

In rear panel:

- 1 10/100Mbit Ethernet port
- 10 optic trigger output (HFBR-1414/ST)



STD-EVE

19 inches 1U standard chassis,

110/220V 50-60Hz AC power supply

- event clock delay, 1/20 event clock delay, 5ps/step delay
- recovery RF clock frequency range is 60 – 500MHz,
- Embedded IOC installed (uclinux 2.6.30.4)

In front panel:

- 1 RF clock output (-3dBm)
- 1 interlock input (TTL)
- 1 fiber input (SFP module)
- 8 TTL output (SFP module)

In rear panel:

- 1 10/100Mbit Ethernet port
- 12 TTL trigger output (8 NIM trigger output optional)

STD-MOE



19 inches 1U standard chassis

110/220V 50-60Hz AC power supply

In front panel:

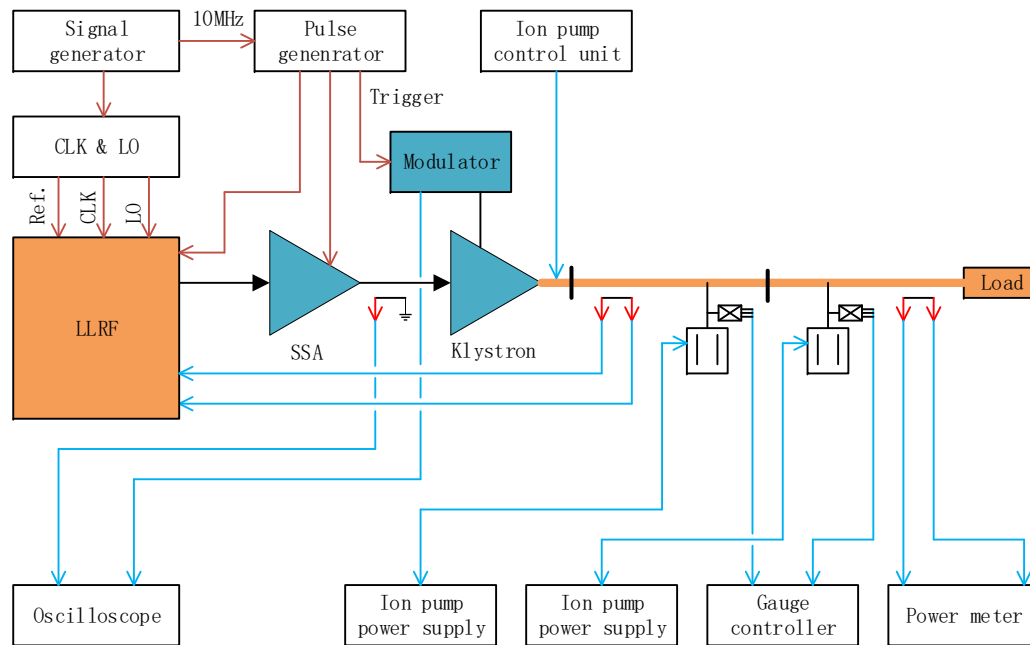
- 4 fiber inputs (SFP module)
- 4 TTL outputs

In rear panel:

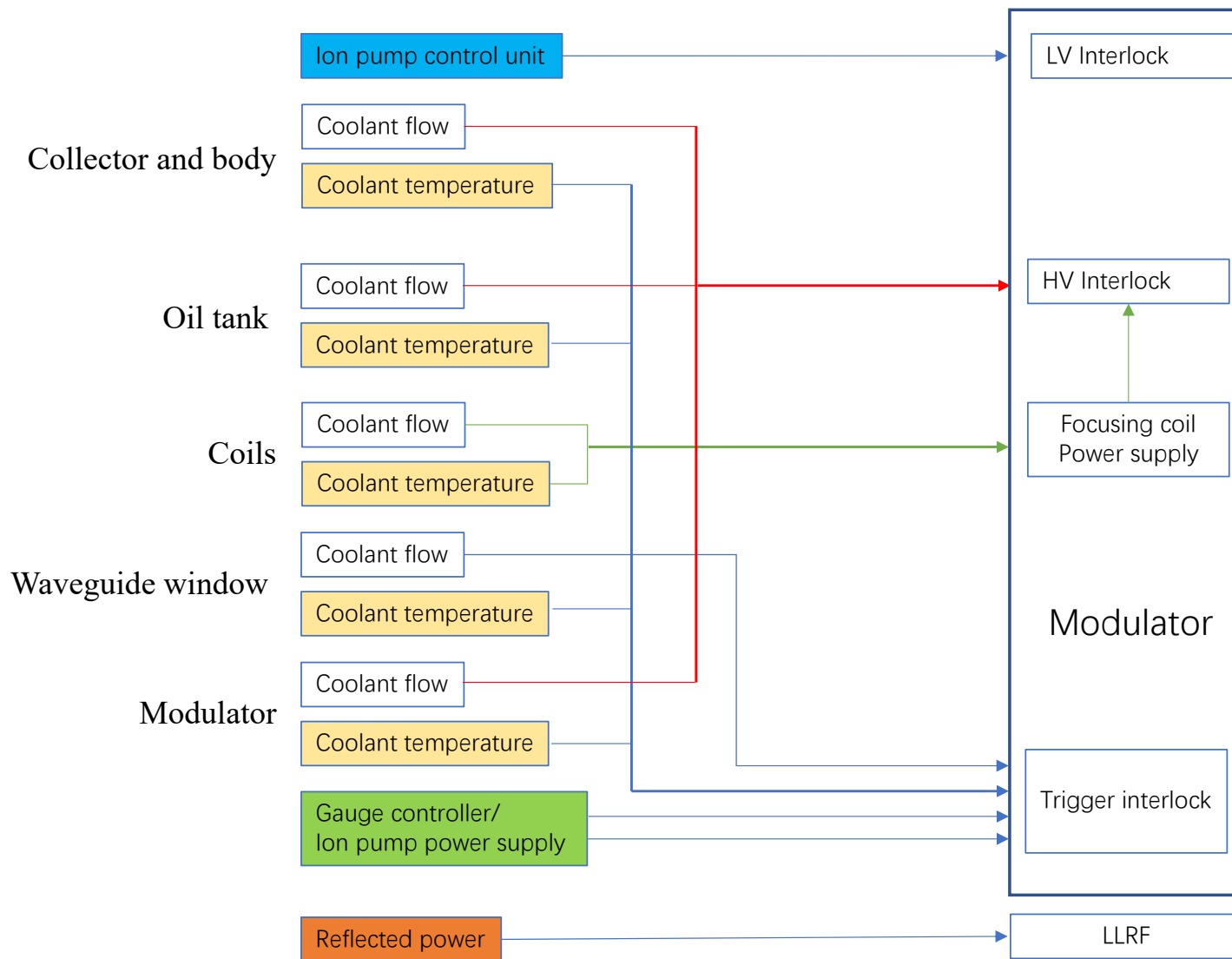
- 4 interlock inputs (1 interlock input/channel)

2.4 Klystron acceptance

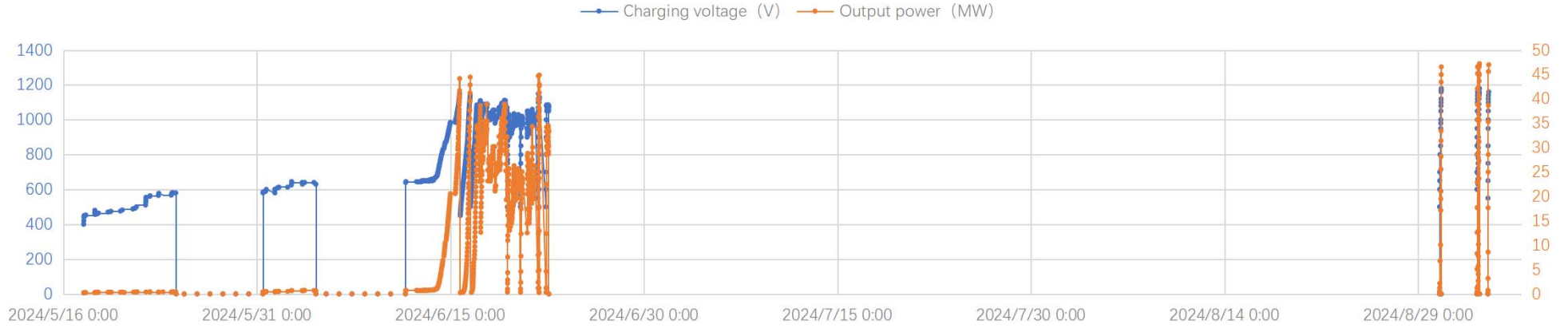
Klystron
E37302A
45MW
2998MHz
Canon electron tubes & devices Co., LTD



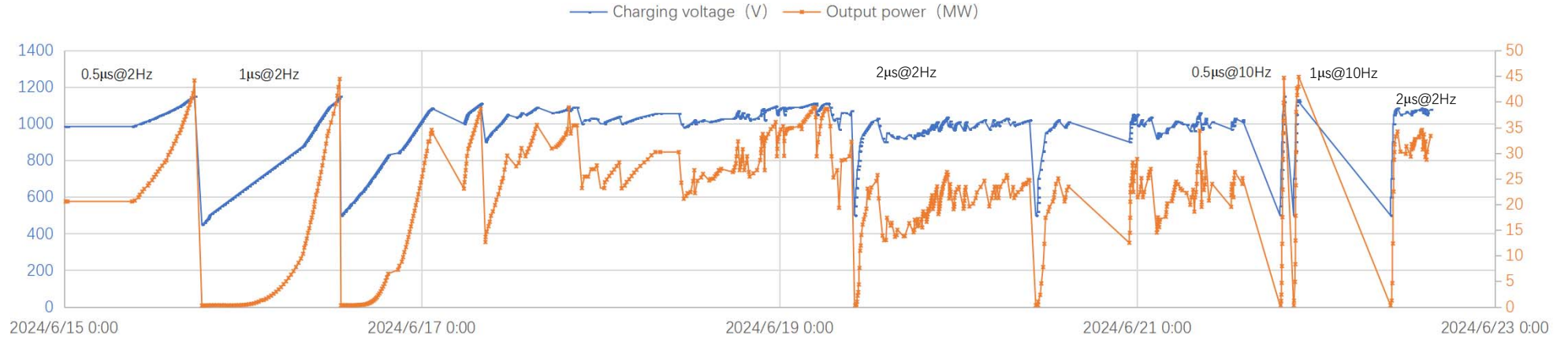
Testing and acceptance platform for klystron



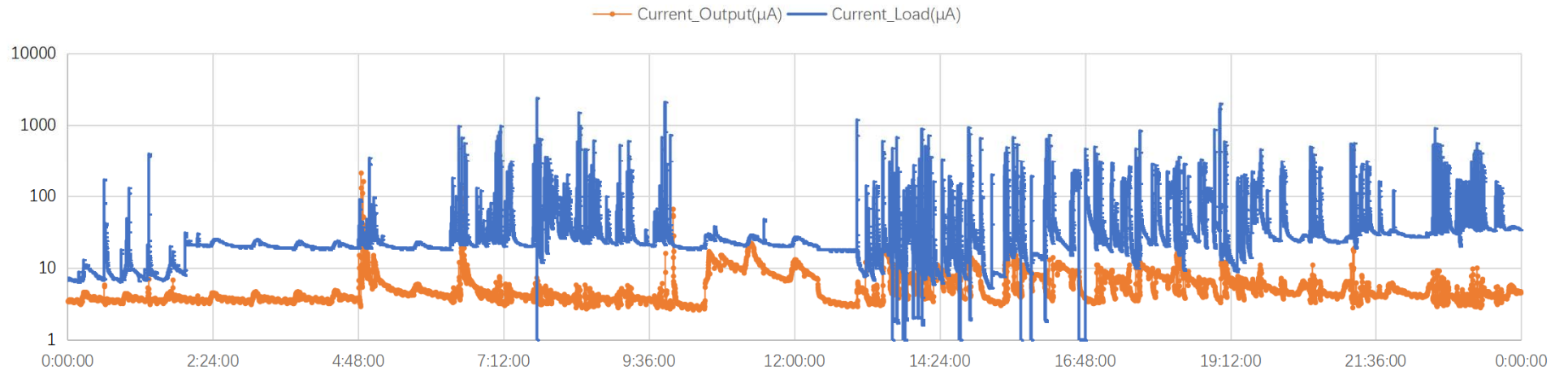
Acceptance testing of klystron



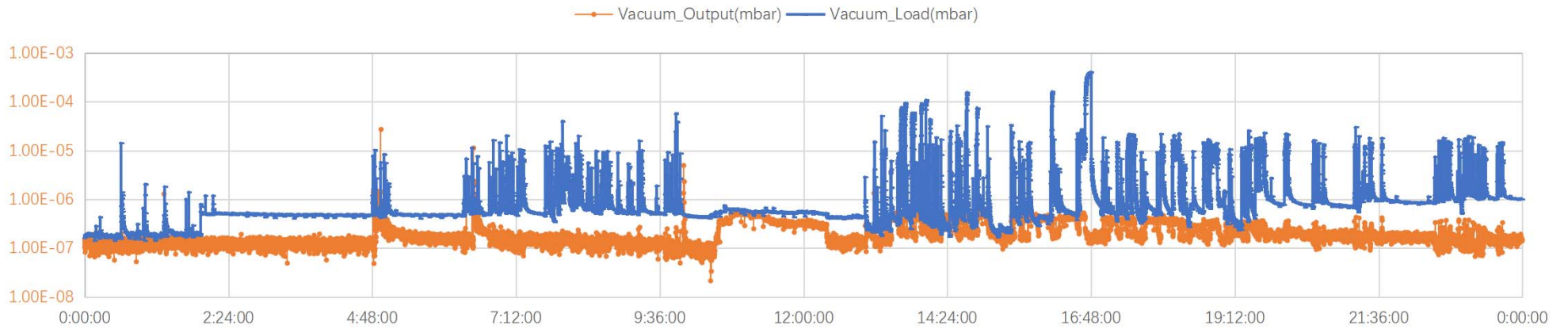
2024.06.15-2024.06.22



Ion pump power supply



Gauge controller



Vacuum data @ 2024.06.19

3. Summary

1. Facility construction is going smoothly as expected.
2. MTCA.4 based LLRF is under developing, the performance meets our requirements.
3. Many equipments are under testing and acceptance.

Thanks for your attention

