



Progress on the MDC Track Reconstruction for STCF L1 Trigger Pre-Research

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On behalf of STCF Trigger Working Group

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Outline

1. **STCF trigger system preliminary design**
2. MDC track reconstruction algorithm
 - 2D tracking and reconstruction
 - Time reconstruction
 - 3D reconstruction
3. Summary



STCF overview

□ Super Tau-Charm Facility:

- A new generation of **high-luminosity electron-positron collider**
- Center-of-mass energy: **2-7 GeV**
- Peak luminosity: **$>0.5 \times 10^{35} \text{ cm}^{-2}\text{s}^{-1}$ at 4 GeV**
 - **Two orders of magnitude higher than BEPCII**
- Collision data: more than **1 ab⁻¹/y**
- With potential to further **increase luminosity and beam polarization**

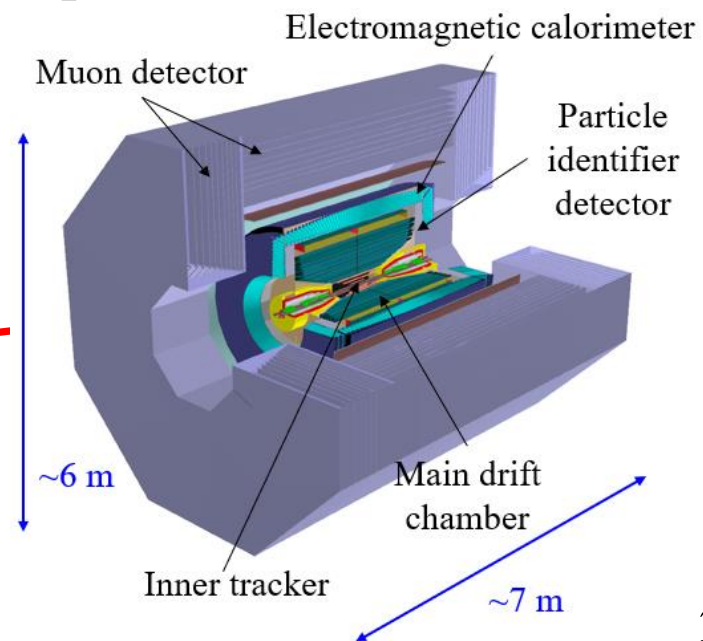


Fig: Concept Design Diagram



Requirements for trigger system

High trigger rate (~ 1 MHz)

Low latency

Maintain the long-term stable operation of experiment

Good background suppression capability

Distinguish of multi-physics events in 1 trigger window

□ High luminosity in STCF generates:

- **High physics event rate:** over **400 kHz**
- **Large data size:** **30 GB/s at 1 times background** raw data
- **High background:** \sim **400 kHz/channel** in MDC
 \sim **1 MHz/channel** in ECAL

□ Trigger system:

- Identifying physics events from massive background
- Ensure very high physics event trigger efficiency : $>99\%$
- Reducing the pressure in data acquisition and transmission



STCF trigger system preliminary design

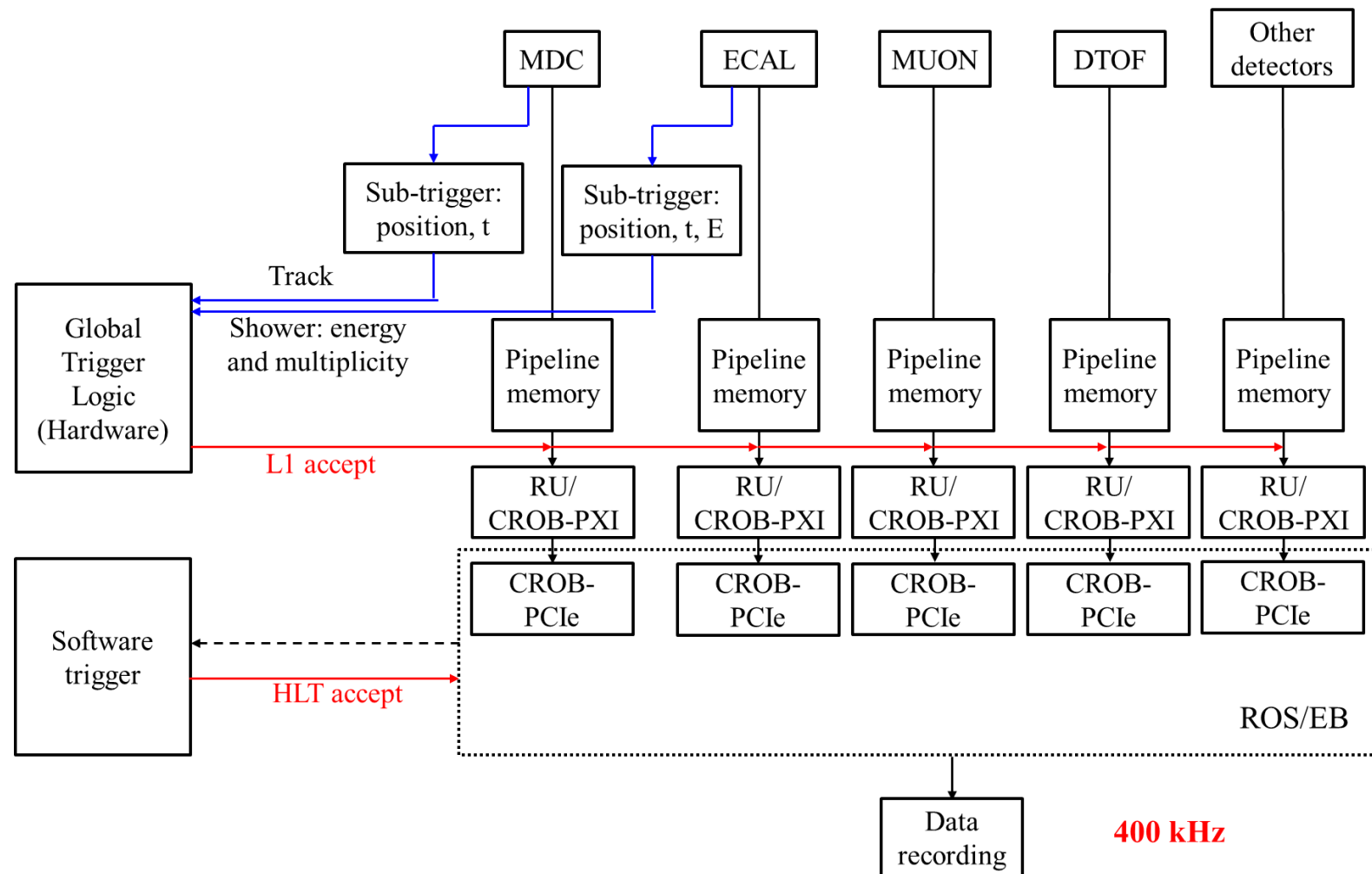
Two-stage trigger system:

Level 1 Trigger:

- Identifying physics events window
- Based on FPGA platform
- Latency $\sim 5 \mu\text{s}$

High Level Trigger (HLT):

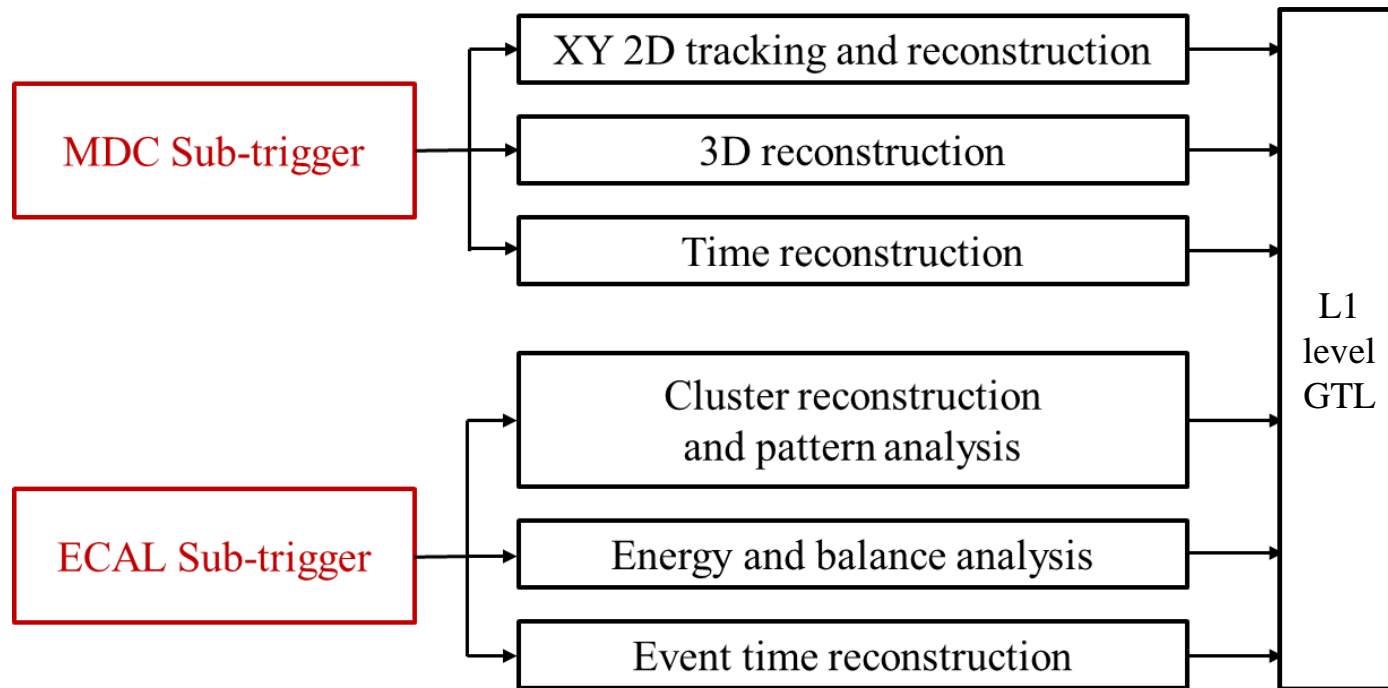
- Suppressing backgrounds in each time window
- Based on server cluster





Preliminary design of L1-level trigger

- **ITK**: high background
- ✓ **MDC**: key tracking detector
- **RICH**: complex Cherenkov ring reconstruction
- **DTOF**: auxiliary in Endcap
- ✓ **ECAL**: key calorimeter, fast response
- **MUON**: auxiliary for $\mu/\pi/n/K_L$



MDC sub-trigger

□ Baseline design:

- 48 layers of small cell
- 1,4,7,8---axial superlayers
- 2,3,5,6---stereo superlayers

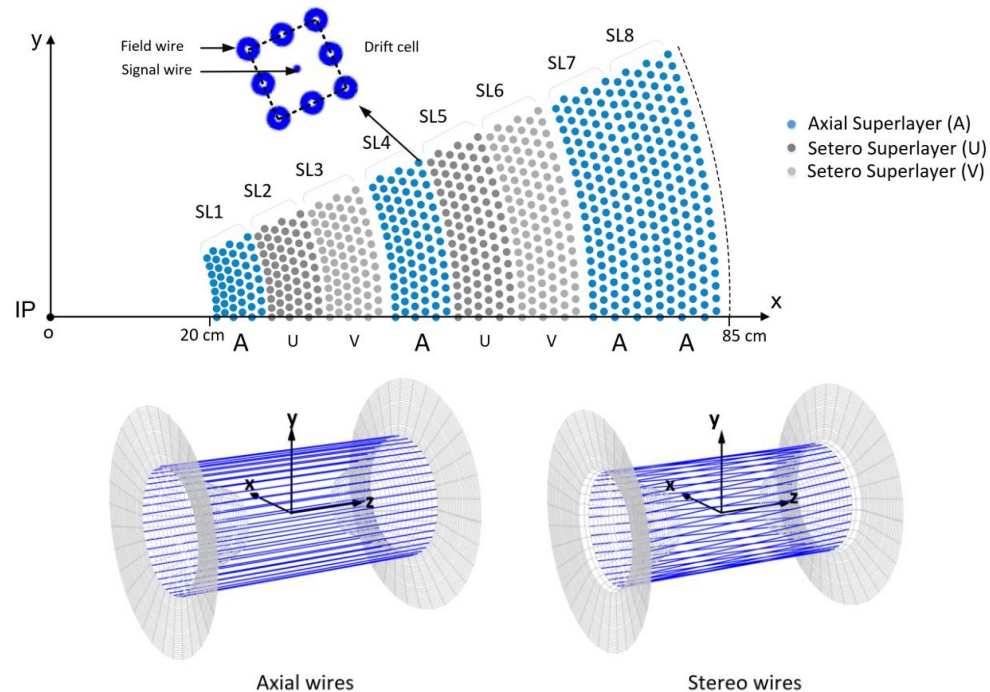


Fig.1: Layout of the MDC signal wires.

□ Region division:

- Barrel & Endcap
- Long track: Exits after passing through the Barrel.
- Short track: Exits at the Endcap.

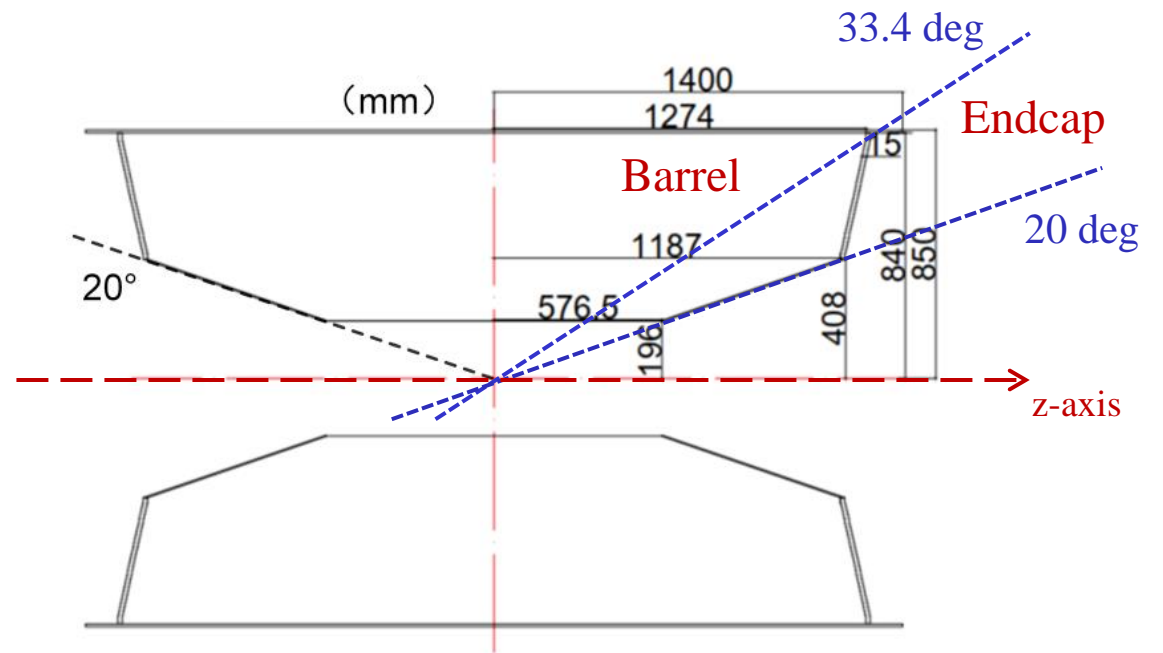


Fig.2: MDC geometric structure



MDC sub-trigger

Requirements for the MDC trigger algorithm:

Challenges:

- High background
- Coordination between sub-detectors

Needs:

- Information of charged particles : $p_T, \Phi, \theta, \rho, z\text{-vertex}$
- Time at which particles hit MDC: t_s

Implementation:

- 2D tracking and reconstruction & 3D reconstruction
- Time reconstruction

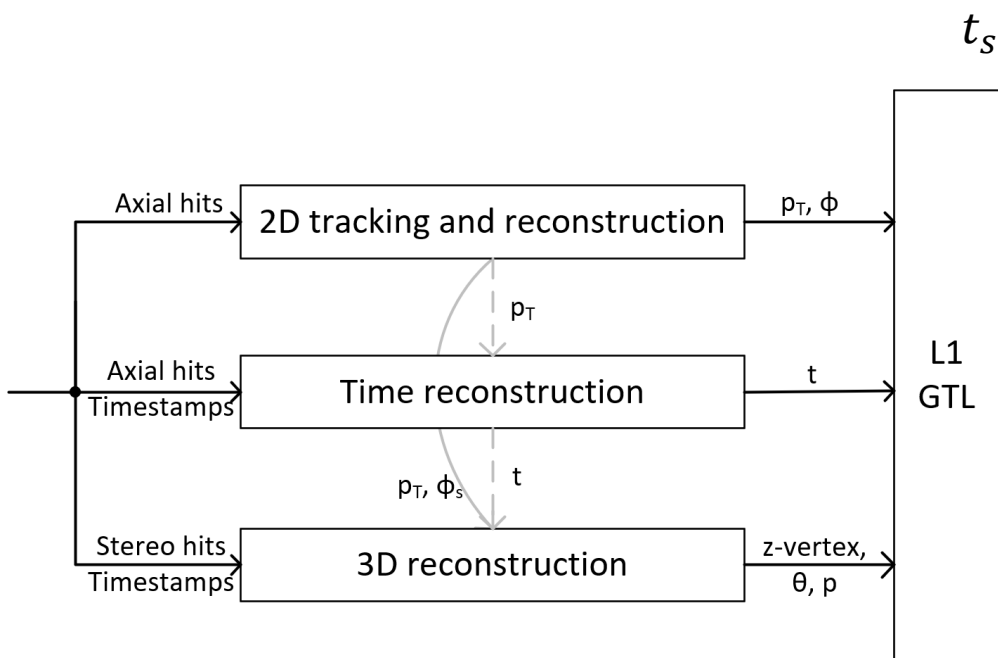


Fig: Data flow of MDC sub-trigger.

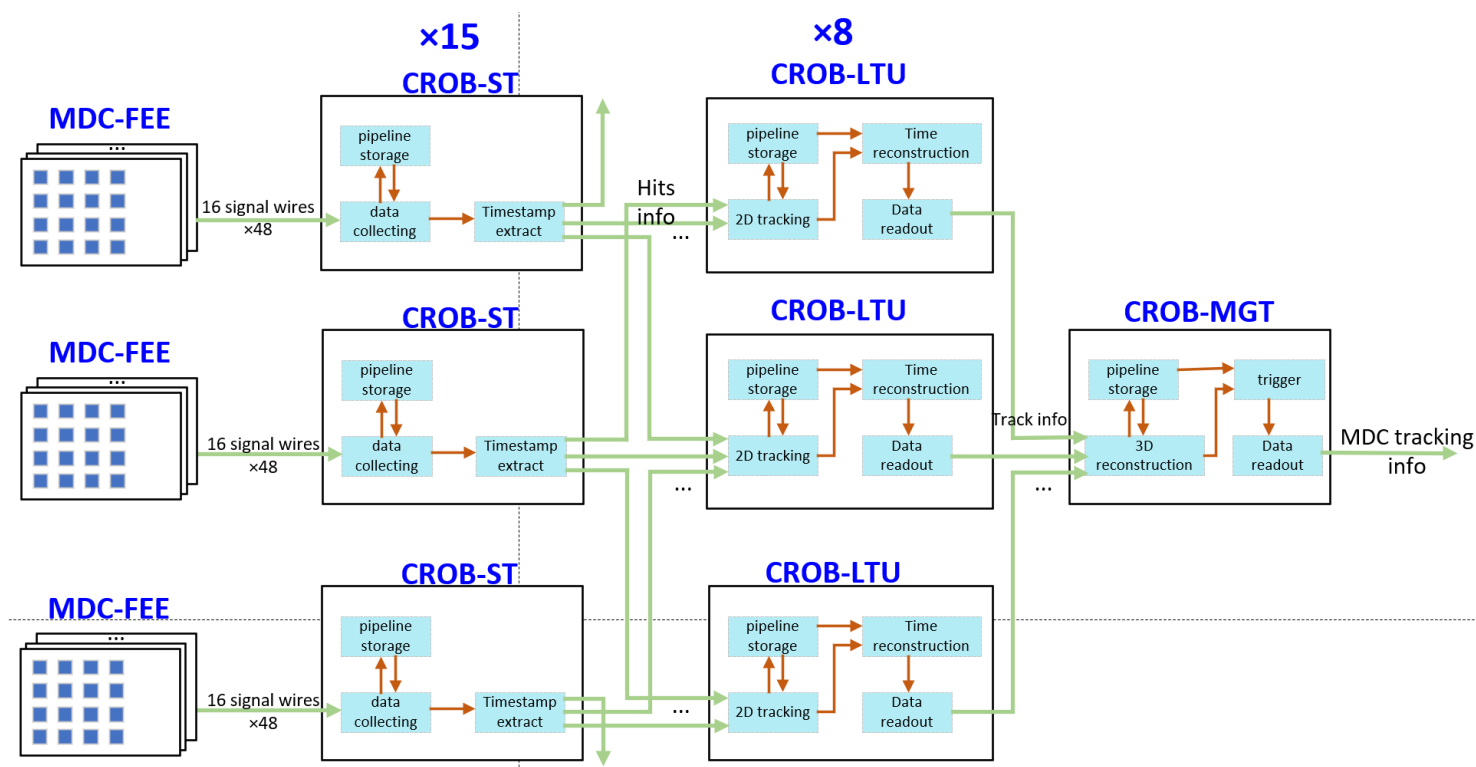


Fig: a schematic diagram of the hardware structure



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2D tracking and reconstruction

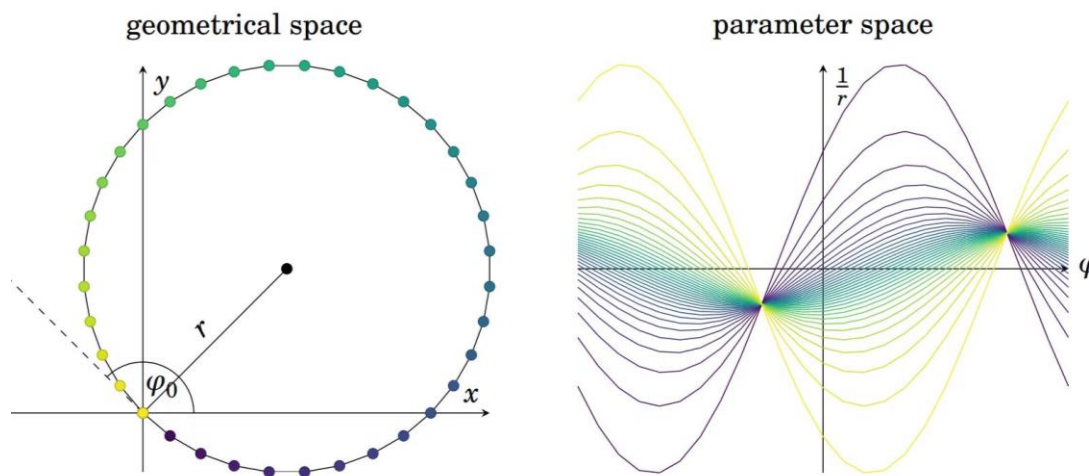
□ Method selection:

➤ Hough transform:

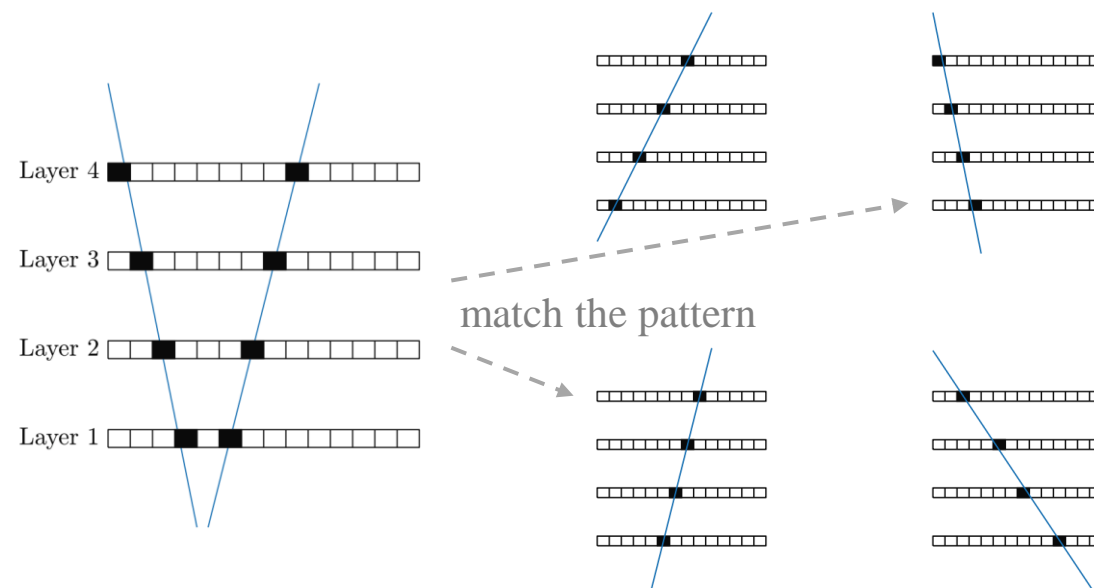
- Complex calculations
- Cannot achieve Track trigger logic $< 1 \mu\text{s}$

➤ Pattern matching:

- ✓ Simple and easy to implement
- ✓ **achieve Track trigger logic $< 1 \mu\text{s}$**



replace





2D tracking and reconstruction

□ Pattern matching operation:

- **Generate pattern banks** through simulated data
Write into distributed storage units on the FPGA
- **Match event data** with the patterns
Implement high-speed parallel processing with FPGA logic

□ Three stages:

- **Track segment (TS) finding:** reduce the input, reject background hits
- **Track finding:** pattern matching---fast but sketchy
- **Estimation of track parameters:** matching with an accurate pattern bank

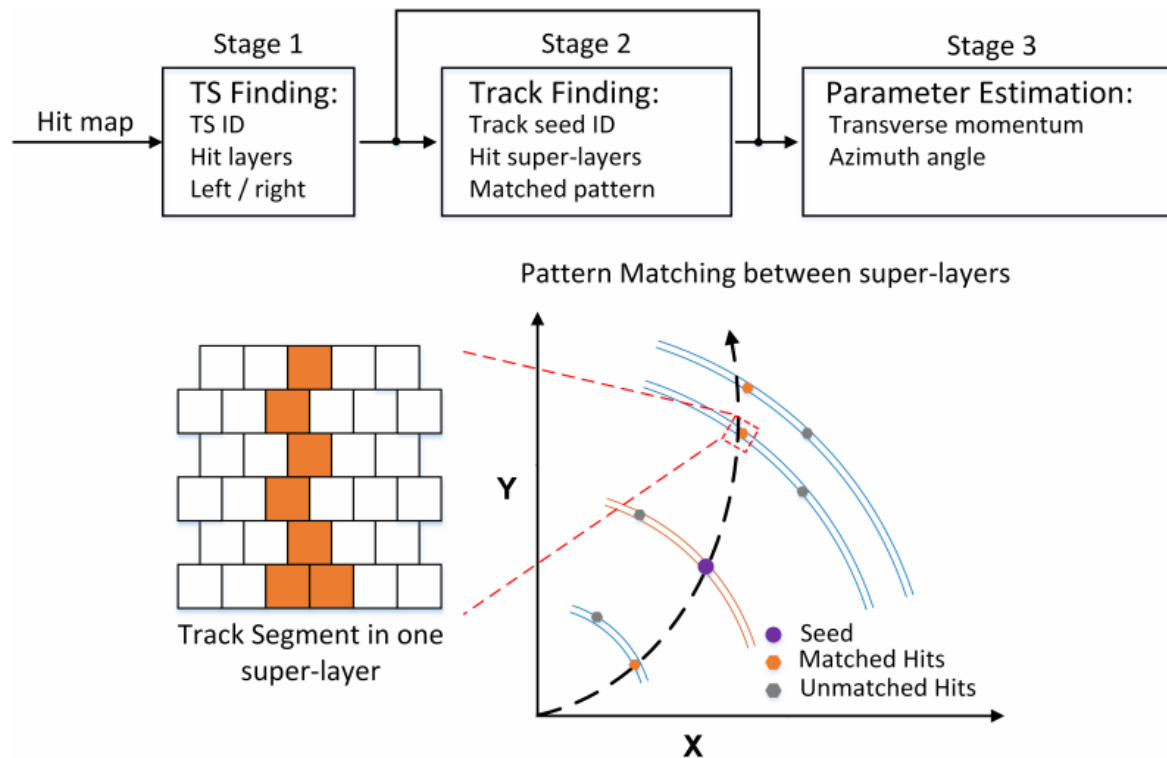


Fig: The components and process of the track reconstruction algorithm.

2D tracking and reconstruction

Track segment finding:

- **Undivided TS:** for track finding
- **Divided TS:** for parameter estimation

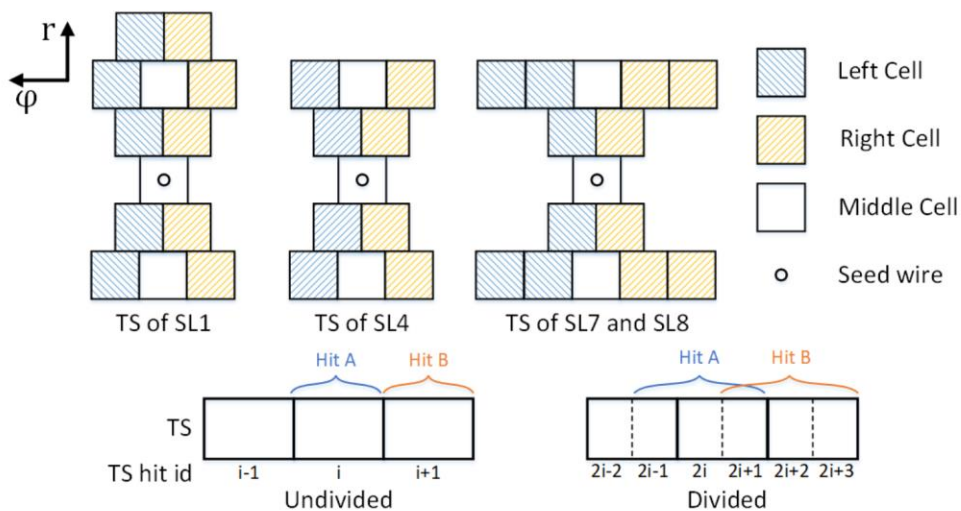


Fig.1: Configurations of three types track segments in different super-layers.

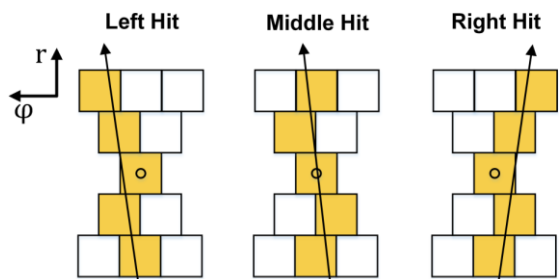


Fig.2: Three examples of segment hits classified by passing side.

Pattern matching

- Track finding: merged patterns for fast tracking
total number: **784**
- Track reconstruction: accurate patterns
 - total number: **~7800**
 - $p_T > 170 \text{ MeV}$

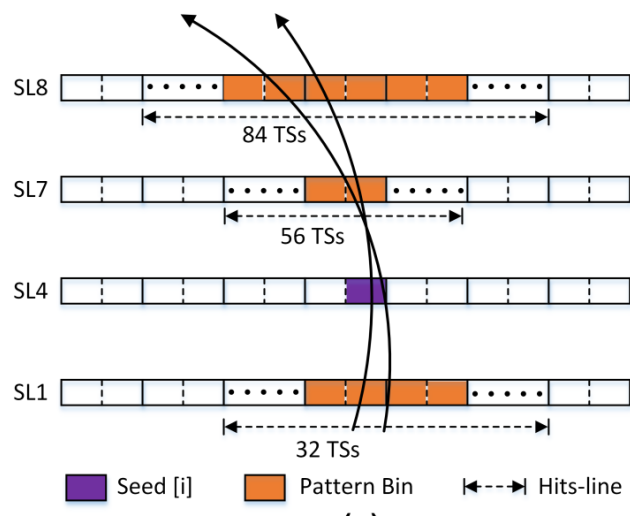


Fig.3: The granularity of patterns in track finding.

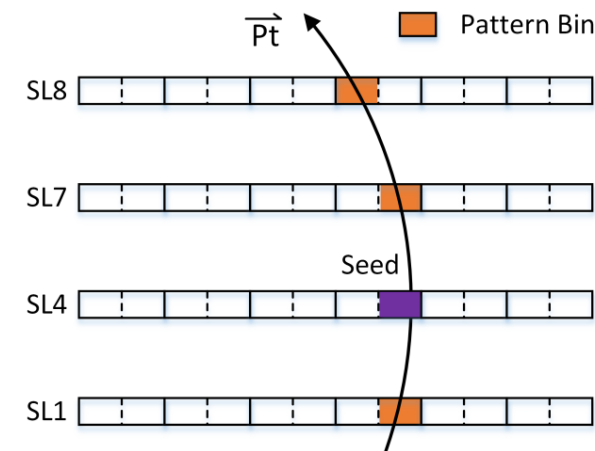


Fig.4: The granularity of patterns in p_t reconstruction.



2D tracking and reconstruction

□ Track efficiency

- Single track
 - Track finding: $p_T > 130\text{MeV}$ $\theta > 30^\circ$
 - Parameter estimation: $p_T > 170\text{MeV}$ $\theta > 30^\circ$
 - $\Delta p_T / p_T^2 \sim 0.1$
- Physics event
 - The cut of θ : reason for 90% lost events

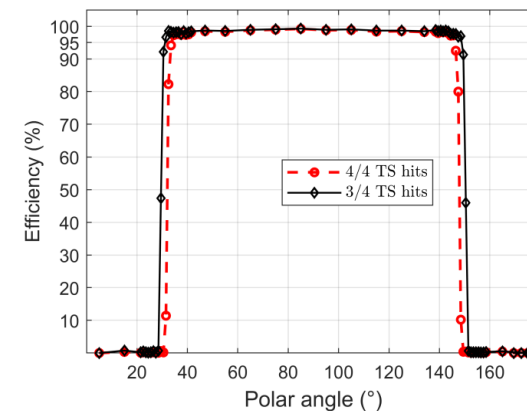
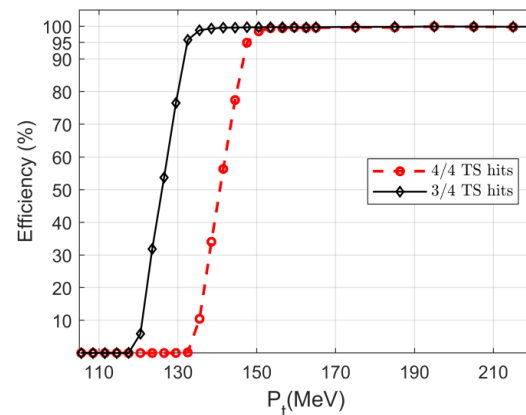


Fig.1: The track finding efficiency in different thresholds.

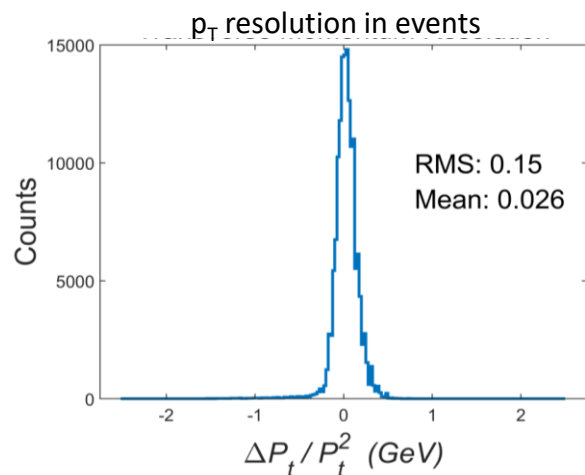


Fig.3: p_T resolution of track reconstruction in physics events

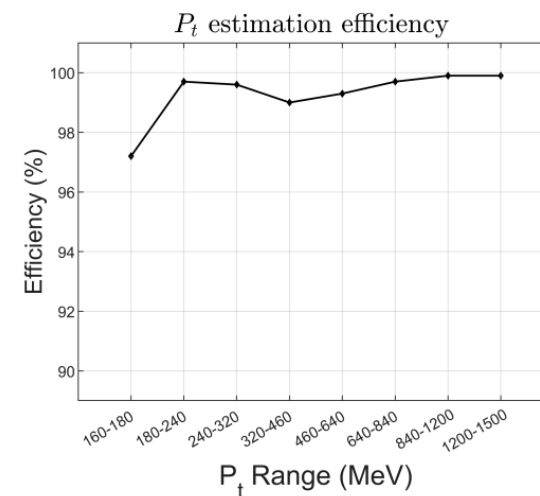
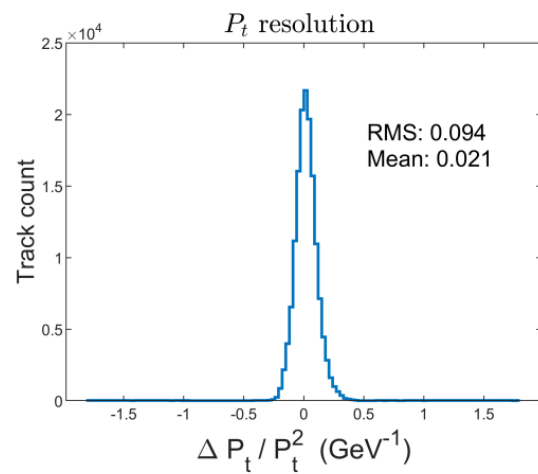


Fig.2: p_T resolution and reconstruction efficiency for single track



2D tracking and reconstruction

➤ Track efficiency - The cut of θ : reason for 90% lost events

□ Optimization: Short Track Reconstruction

- For data with hits only in the first and fourth superlayers
- Introduce hits from the second and third superlayers to select short tracks (hits account for the θ error caused by the z-vertex offset)
- Still under development
- Preliminary tracking results:
 - Single track: Efficiency ~ **98%** (1505/1540)
 - Background in physics events: Misidentification rate ~ **41%** (1829/4463)

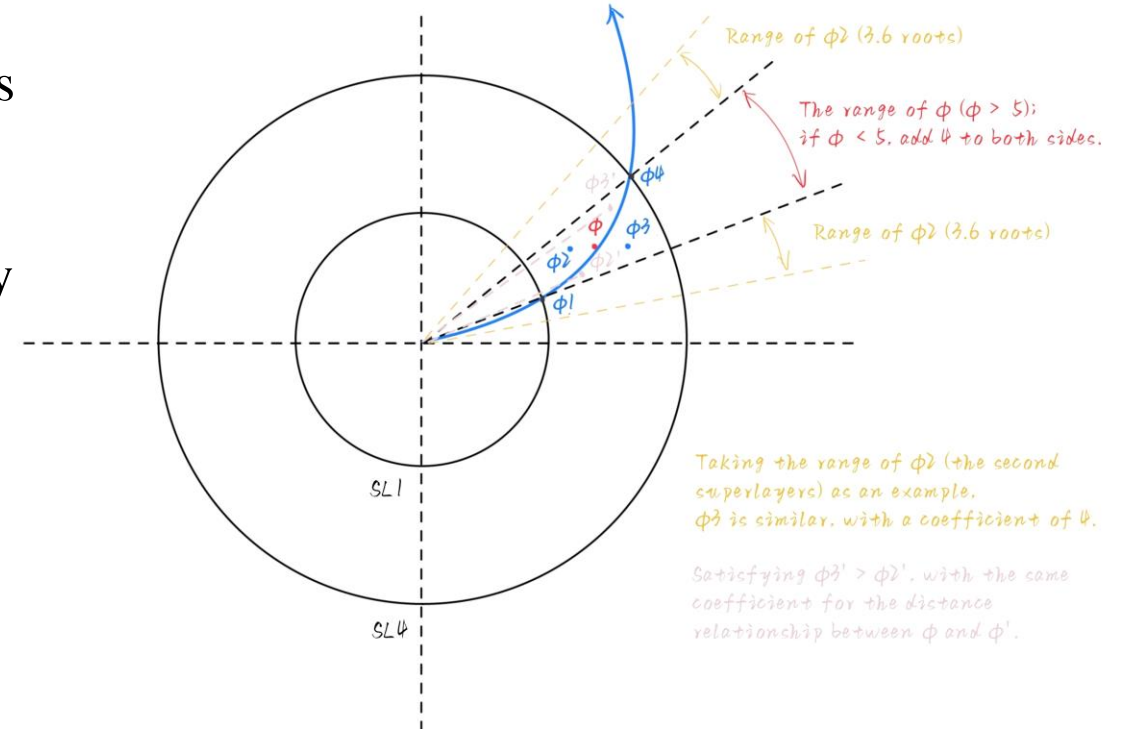


Fig: Track finding rules



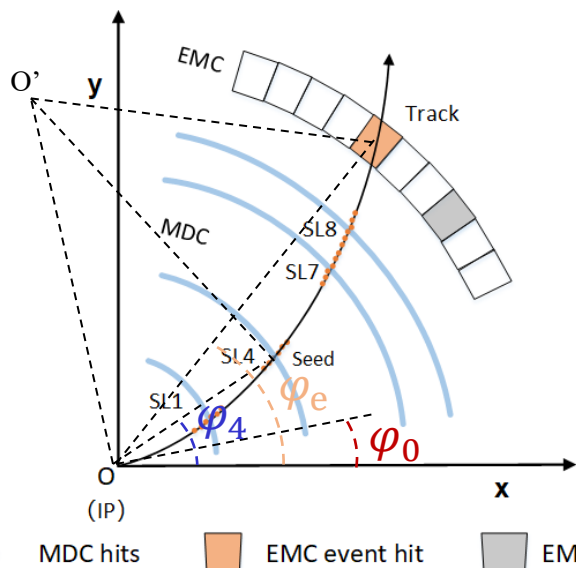
2D tracking and reconstruction

□ φ reconstruction

IP: $\varphi_0 = \varphi_4 - \arcsin\left(\frac{r_4}{2\rho}\right)$

EMC: $\varphi_e = \varphi_4 - \arcsin\left(\frac{r_4}{2\rho}\right) + \arcsin\left(\frac{r_e}{2\rho}\right)$

$$\rho = \frac{p_t(\text{Gev})}{0.3B} \text{ (m)}$$



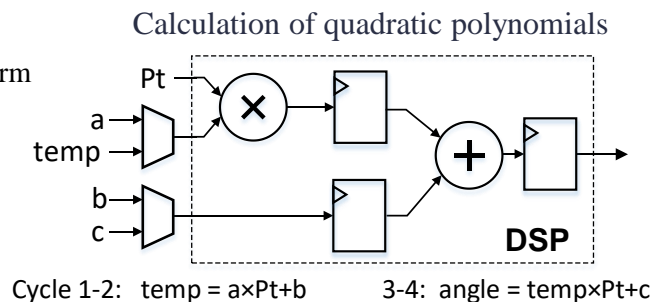
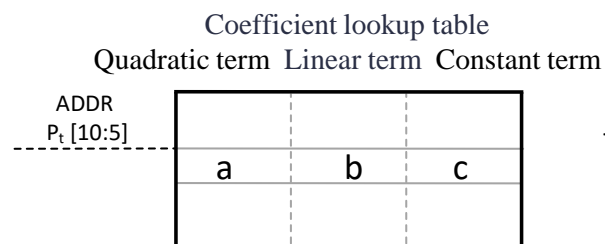
Piecewise interpolation

□ FPGA implementation

$$\varphi = \varphi_4 + \Delta\varphi$$

Resource friendly

$$\Delta\varphi = a \times p_t^2 + b \times p_t + c$$



➤ precision

- For tracks with $p_t > 180 \text{ MeV}$, $\Delta\varphi_e < 20 \text{ mrad}$
- For track matching with EMC, 50 mrad is OK

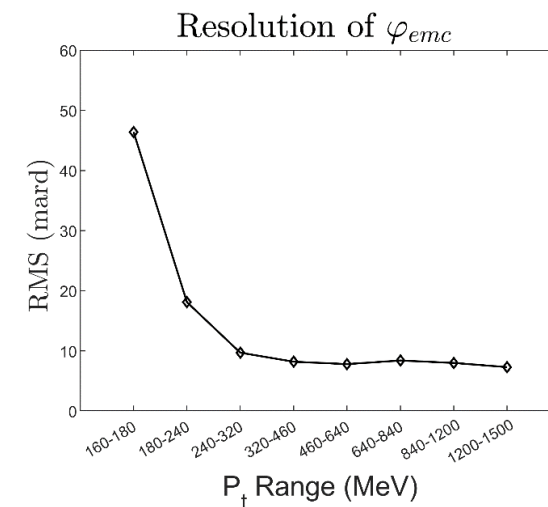
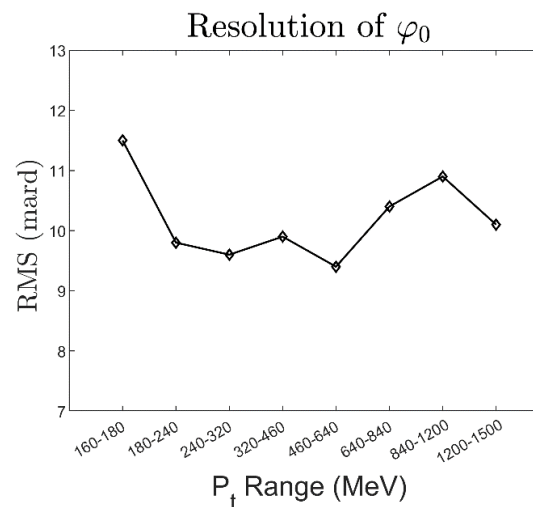


Fig.1: Calculating the φ by the seed location and estimate of p_t .

Fig.2: φ resolution for single track



Time reconstruction

□ Purpose of time reconstruction:

- TS generation time t_s + drift time t_{drift} = single wire hit time T
- suppress background
- Distinguish adjacent physics events

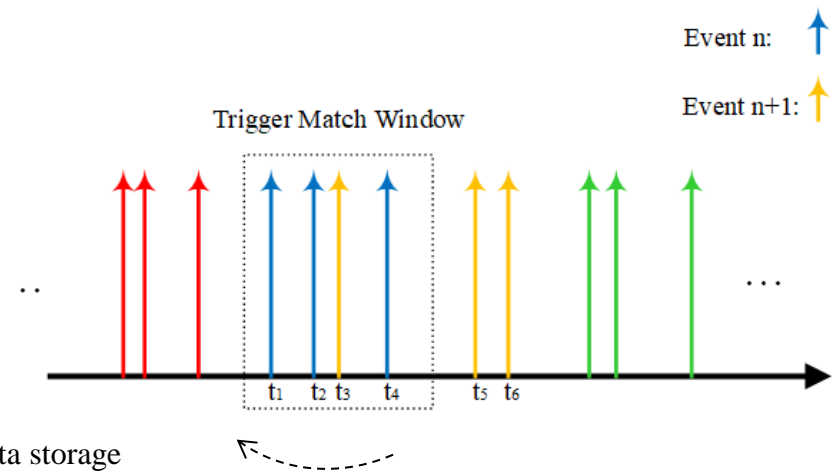
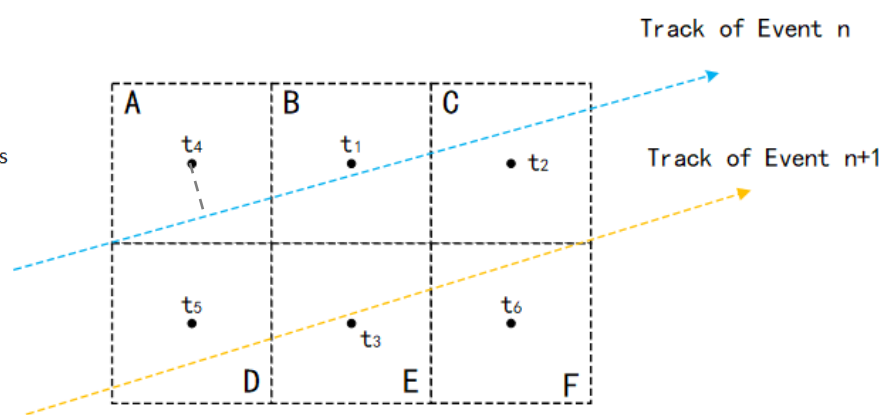
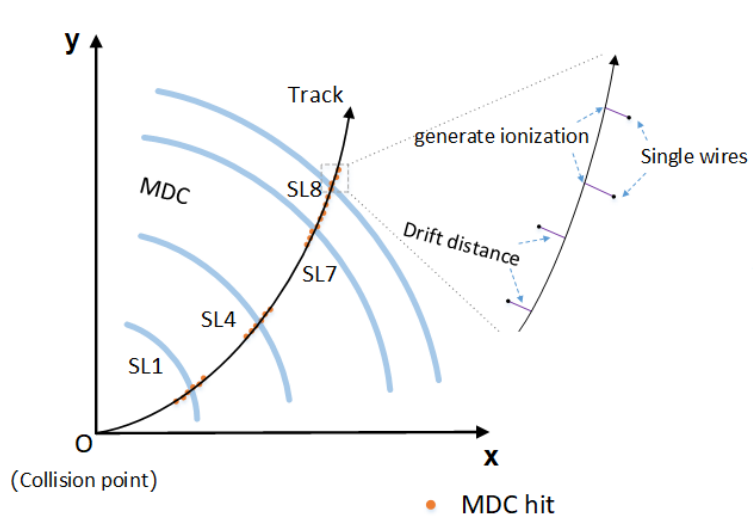
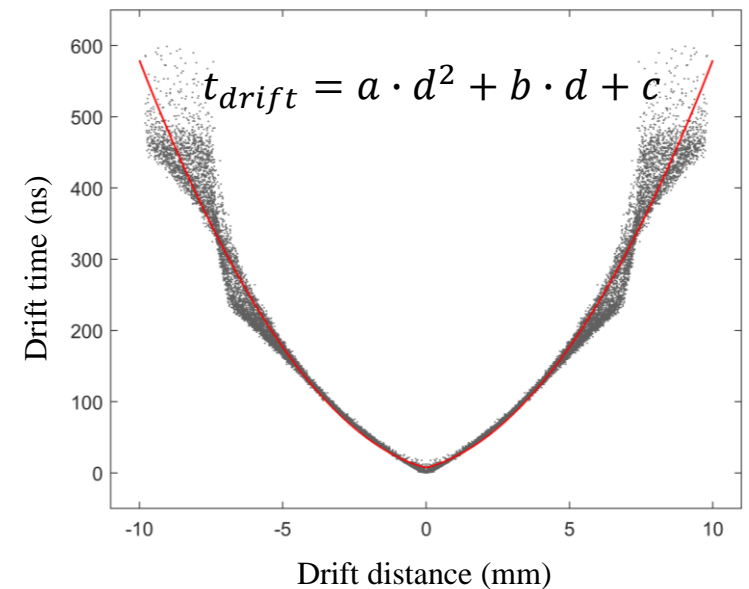
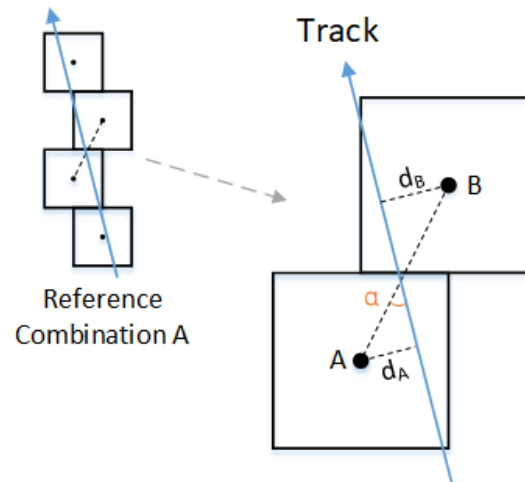
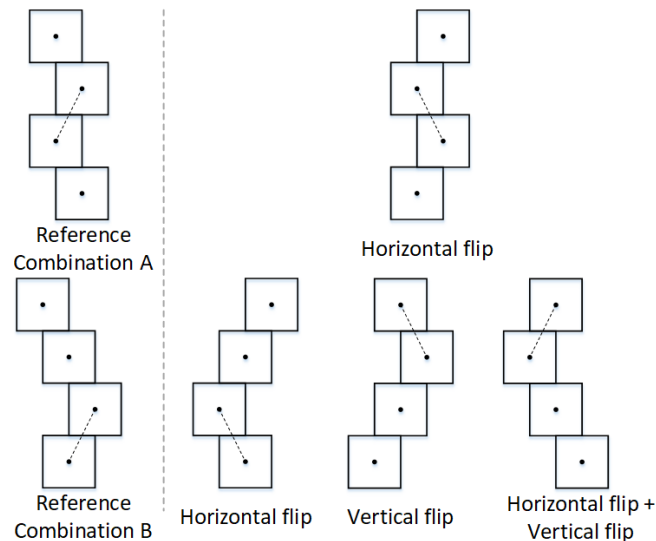


Fig: Misaligned data storage

Time reconstruction

□ Reconstruct the hit time using track parameters

- Estimate the track segment as a **straight line**
- Calculate the drift distance based on the reconstructed track parameters, and then **obtain the drift time**
 - FPGA pipeline computation
- Combine the timestamp to calculate the **generation time of the track segment**
- The track time is **the average value** of the times of each track segment





Time reconstruction

□ Track time reconstruction

- Calculate the median
- Abandon TS whose time deviates significantly from the median
- Test with single tracks
 - For tracks with $p_T > 180$ MeV: efficiency $> 80\%$, $\Delta t < 8$ ns

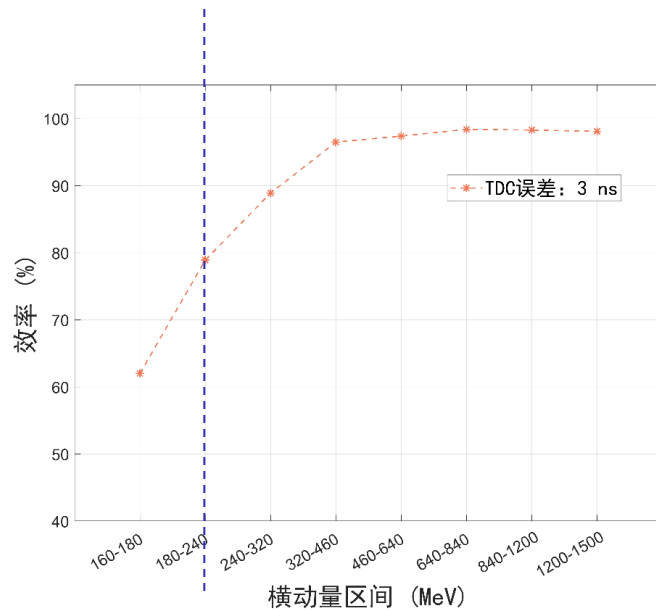


Fig.1:Reconstruction efficiency of single track.

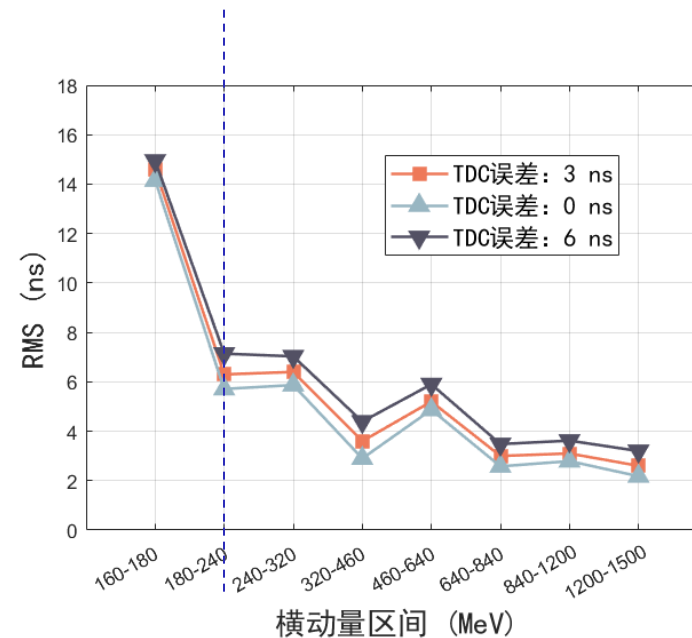


Fig.2:resolution of single tracks.



3D reconstruction

□ Main content of 3D reconstruction

✓ Z-vertex reconstruction

- Resolution of about 3 cm
- Support for $|z| < 10$ cm truncation, and an error of $\pm 3\sigma$
- **over 97% of background tracks can be eliminated**

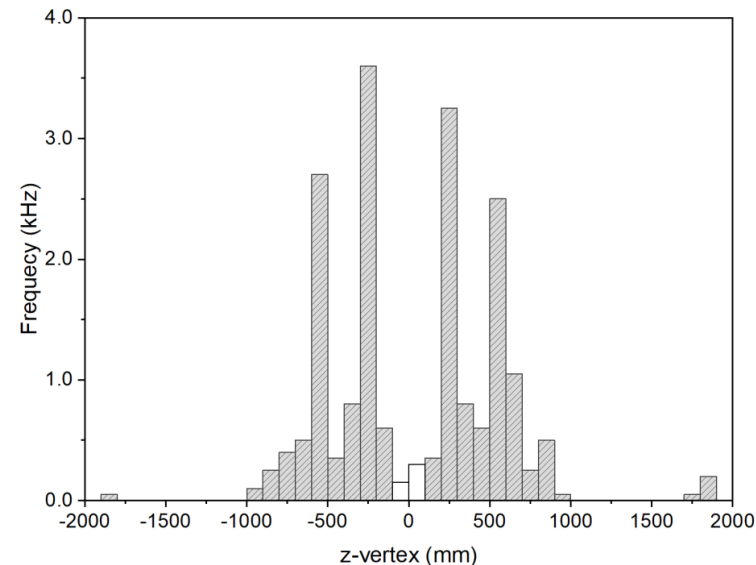


Fig: The z-vertex distribution of background tracks selected by the two dimensional reconstruction algorithm.



Z-vertex reconstruction

□ Stereo TS finding

- 1 superlayer ---2 seed wires

Position + timestamp

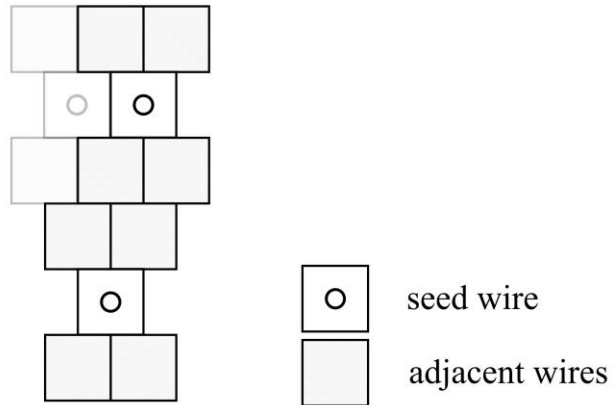
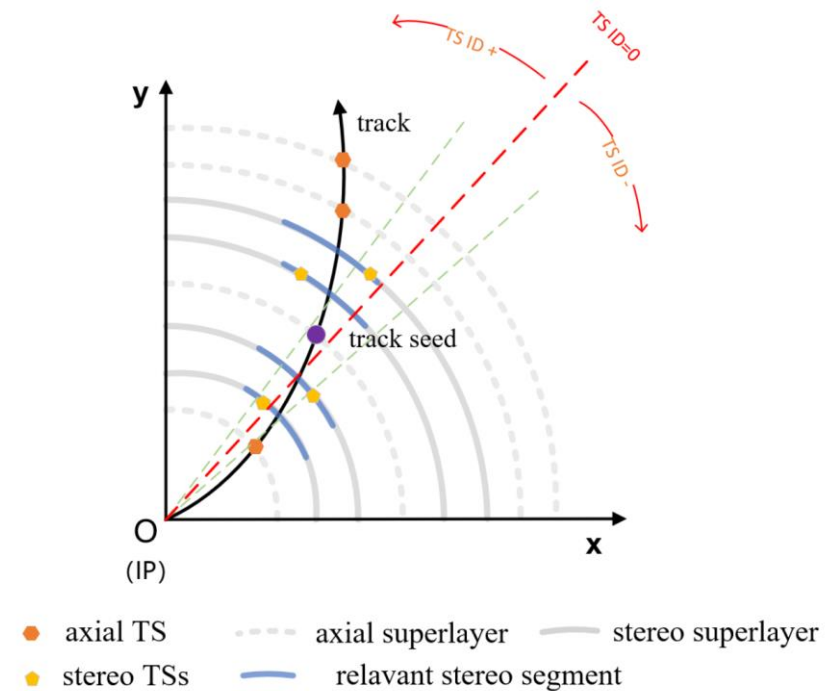


Fig: Stereo SLs

□ Track finding

- Matching stereo TS with an existing track
- Sectorization and Normalization



Z-vertex reconstruction

MLP training

Multi-layer fully connected neural network

(MLP)

- Input: track segment numbers and timestamps for 8 superlayers
- Output: z-vertex in various p_t regions

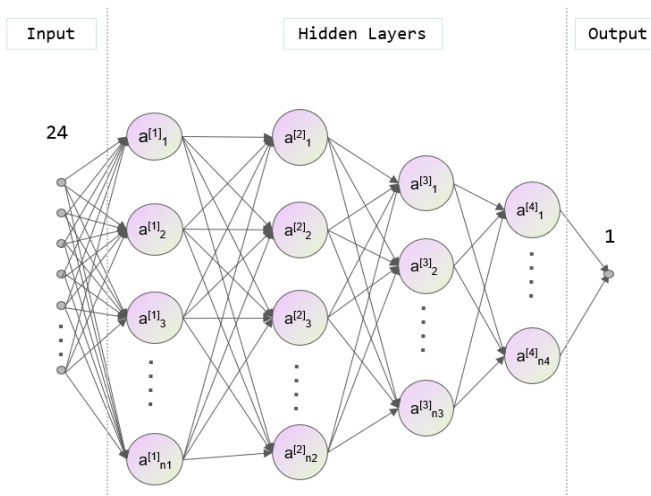


Fig.1: The basic structure of an MLP model.

Quantization & FPGA resource optimization

- Qkeras

Model bitwidth and z-vertex resolution

bitwidth*	8_1	12_4	16_6	20_8
$\Delta z/cm$	2.93	2.84	2.53	2.51

*W_I represents 'ap_fixed(W, I)', indicating a W-bit fixed-point number with I integer bits (including one sign bit).

- Pruning

Model size and resolution of z-vertex

Structure	Sparsity	NNZ Params	$\Delta z/cm$
A^1	0	2.53k	2.43
	0.2	2.04k	2.46
	0.4	1.52k	2.56
	0.6	1.06k	2.90
	0.8	0.58k	5.05
B^2	0.4	2.11k	2.31

¹24-32-32-16-8-1.

²24-48-32-16-8-1.

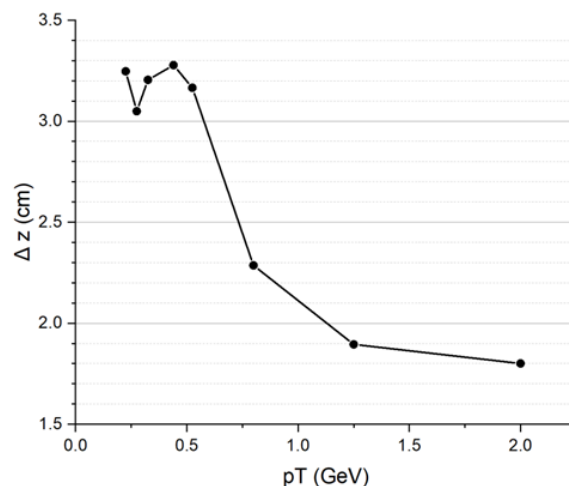


Fig.2: Z-vertex resolution at different p_t



Z-vertex reconstruction

□ Further resource optimization

- 1 MLP for all tracks
- Training with **High Granularity Quantization (HGQ)**
 - Certain parts of the network can accommodate lower precision without compromising performance.
 - Fine-tune the per-weight and per-activation precision.

- Latency: 60 clk
- Interval (Dead time): 2 clk
- FPGA resource:

DSP: 71%

FF: 29 %

LUT: 19%



- Latency: 40 clk
- Interval (Dead time): 1 clk
- FPGA resource:

DSP: 4%

FF: 4%

LUT: 17%



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Algorithm Summary

1. 2D tracking and reconstruction ($J/\psi \rightarrow$ anything)

- $\Delta p_T / p_T^2 \sim 15\%$

Latency = 339 ns

2. Time reconstruction (single track)

- $\Delta t < 16$ ns

Latency = 207 ns

3. Z-vertex reconstruction (clear single track)

- $\Delta z \sim 3$ cm

Latency (MLP) = 125 ns



Further Work Plan

□ Algorithm Optimization

- Un-identification of high- p_t track in Endcap
 - 3 hits tracking as a complement to 4 hits tracking requiring further optimization
- Continue advancing short track reconstruction.
- Distinguish of cross tracks

□ Engineering Principle Prototype Testing

- Port the FPGA GBT protocol and establish the data link.
- Validate the MDC hardware reconstruction algorithm.
 - 2D reconstruction algorithm
 - 3D reconstruction algorithm
 - Time reconstruction algorithm
- Purpose:
 - Conduct on-board hardware logic test to verify the reliability of timing.
 - Ensure consistency between actual test results and simulated behavior.



Thanks