STCF Trigger Design and R&D Progress

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On behalf of STCF TRIG group

21/11/2024

Outline

1. STCF and Trigger system
2. L1 trigger algorithm progress
3. L1 trigger hardware platform R&D
4. HLT study
5. Summary

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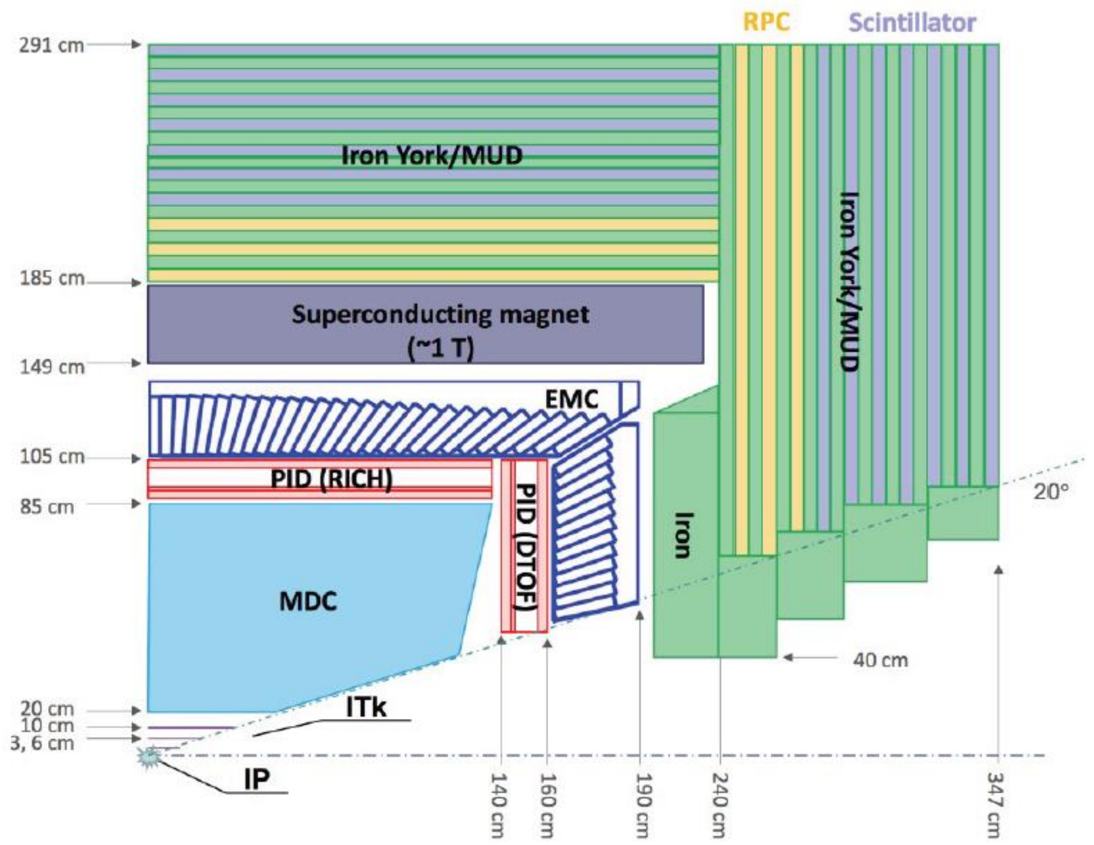
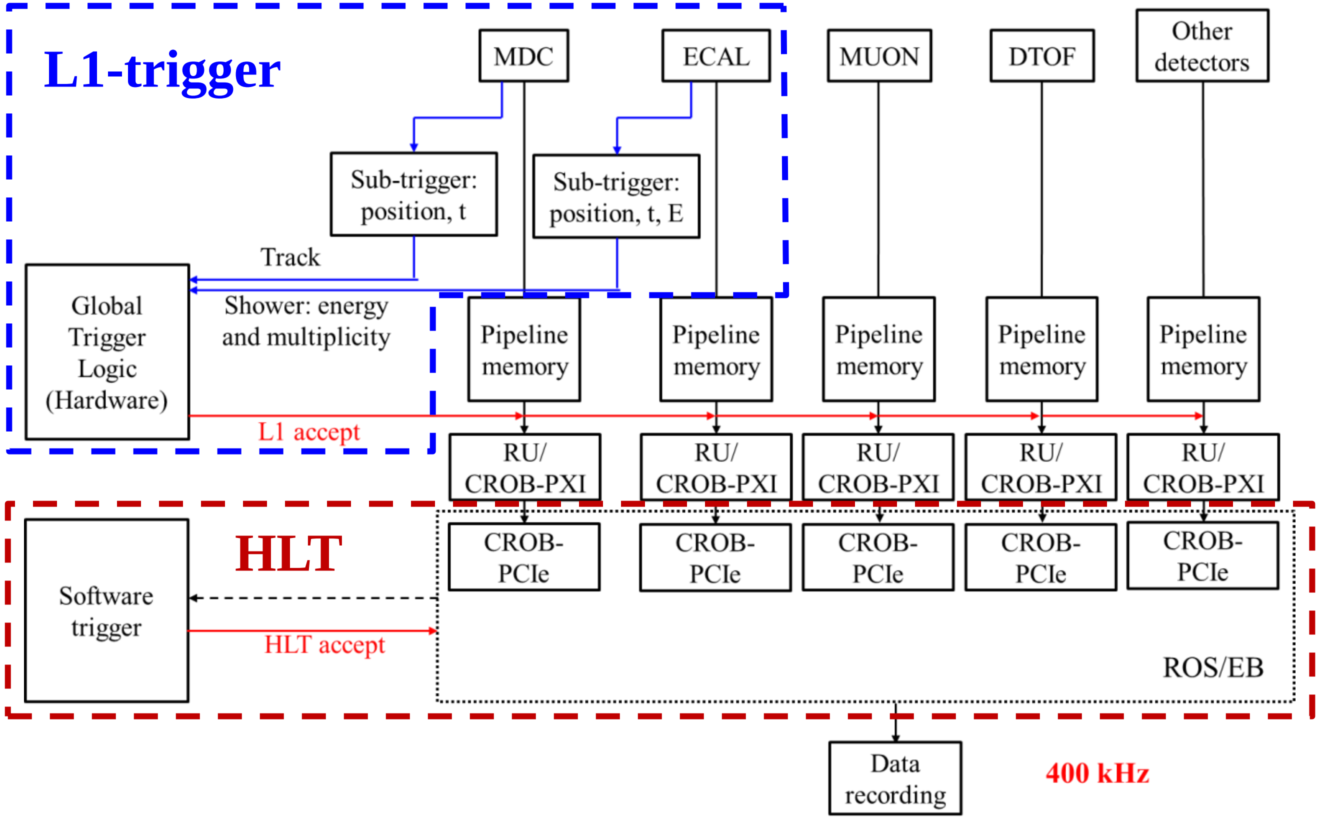
STCF and trigger system

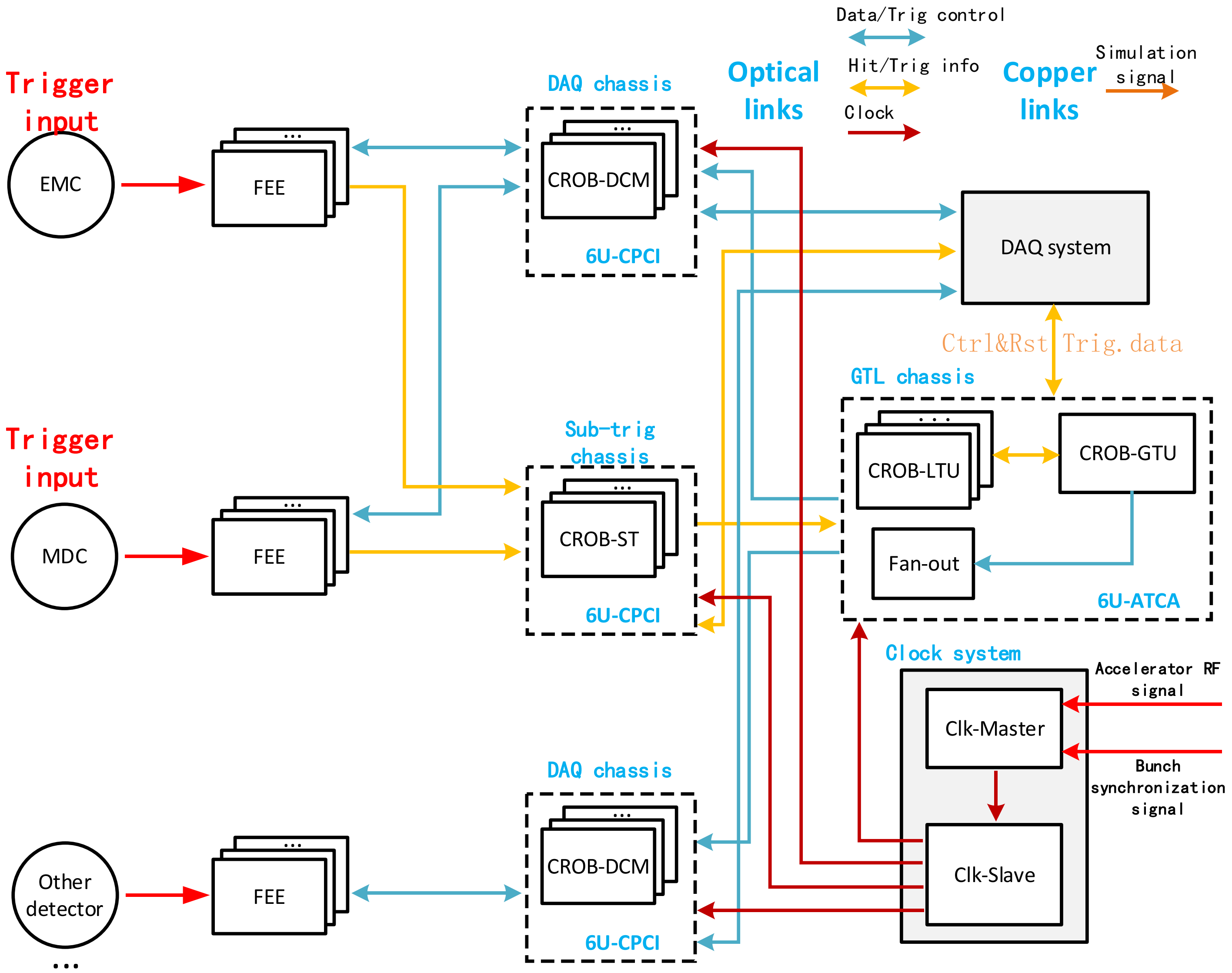
STCF detector spectrometer cross section



Flowchart of STCF TRIG system



L1 trigger hardware framework



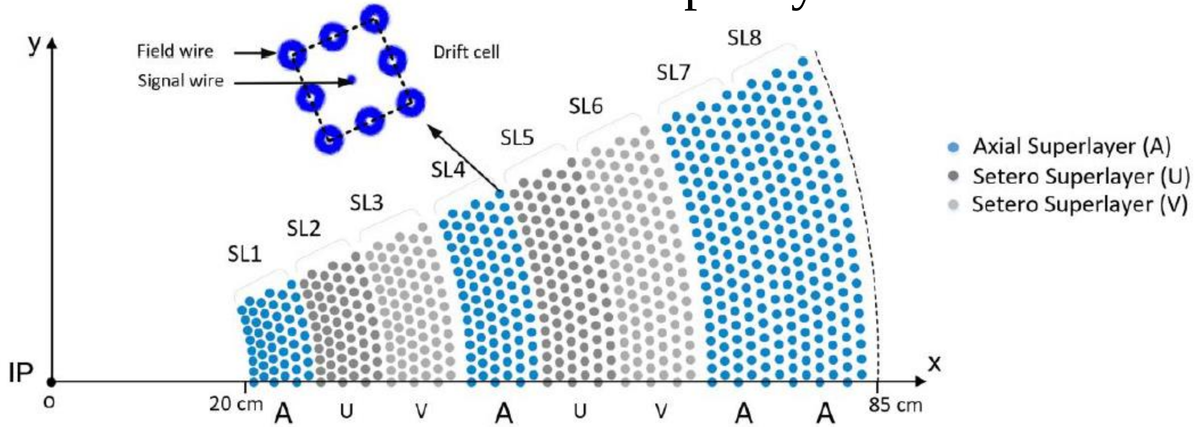
- Separated L1 trigger and DAQ system
- **CROB-DCM** for data collection for DAQ system
- **CROB-ST** for data collection for L1 trigger
- Delivery L1 trigger decision by **DAQ chassis to FEE**
- CROB-DCM/ST： CPCI chassis
- CROB-LTU/GTU： ATCA chassis
- Global clock: 40MHz

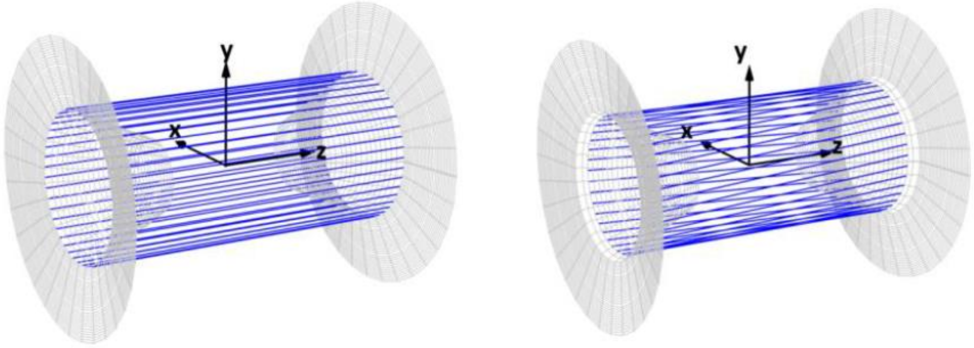
Outline

MDC sub-trigger R&D

□ MDC structure

- 4 × axial wire superlayer
- 4 × stereo wire superlayer

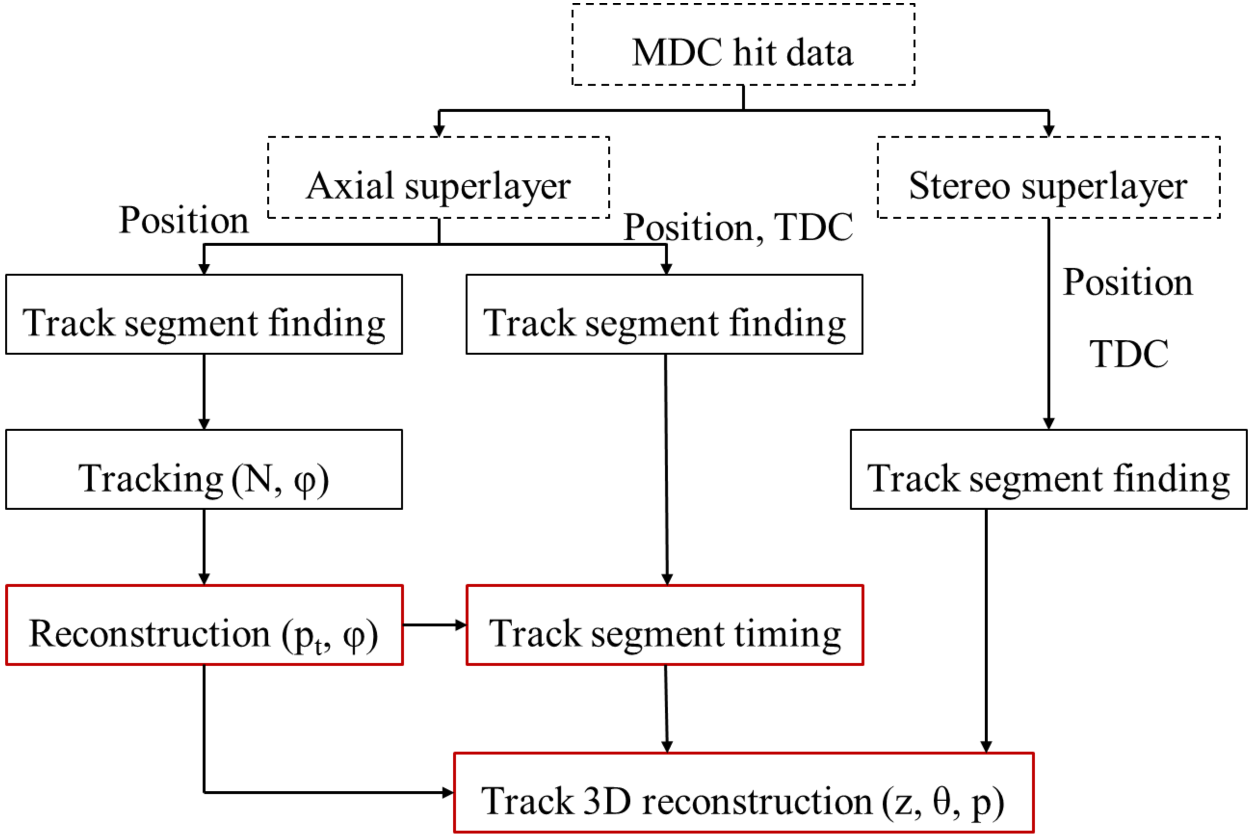




Axial wires

Stereo wires

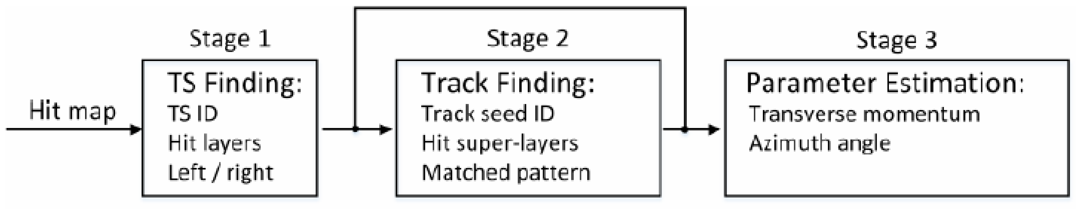
□ MDC algorithm

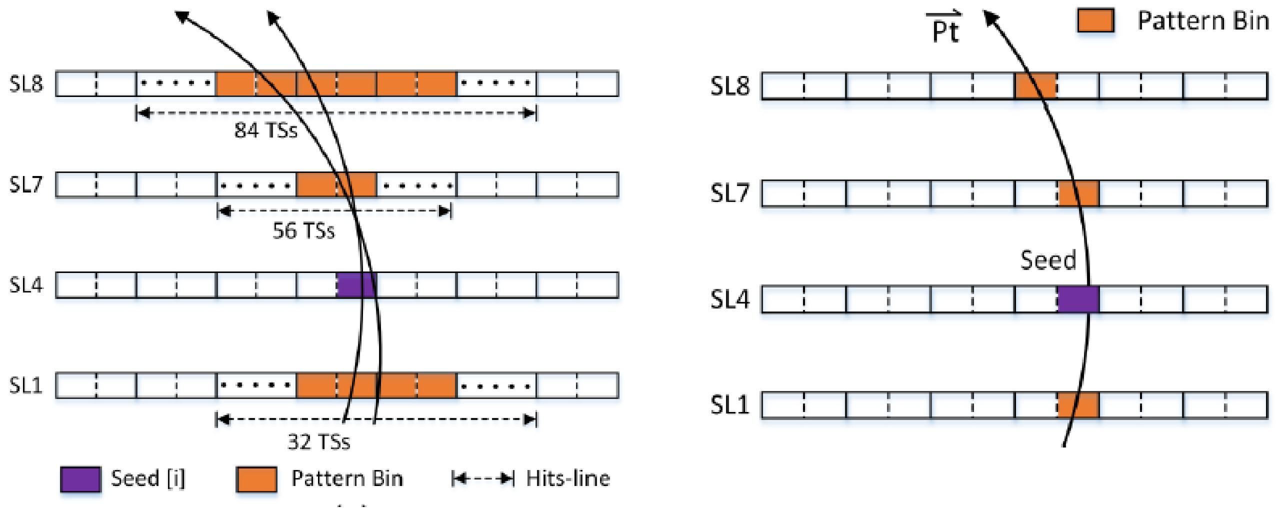


MDC sub-trigger R&D

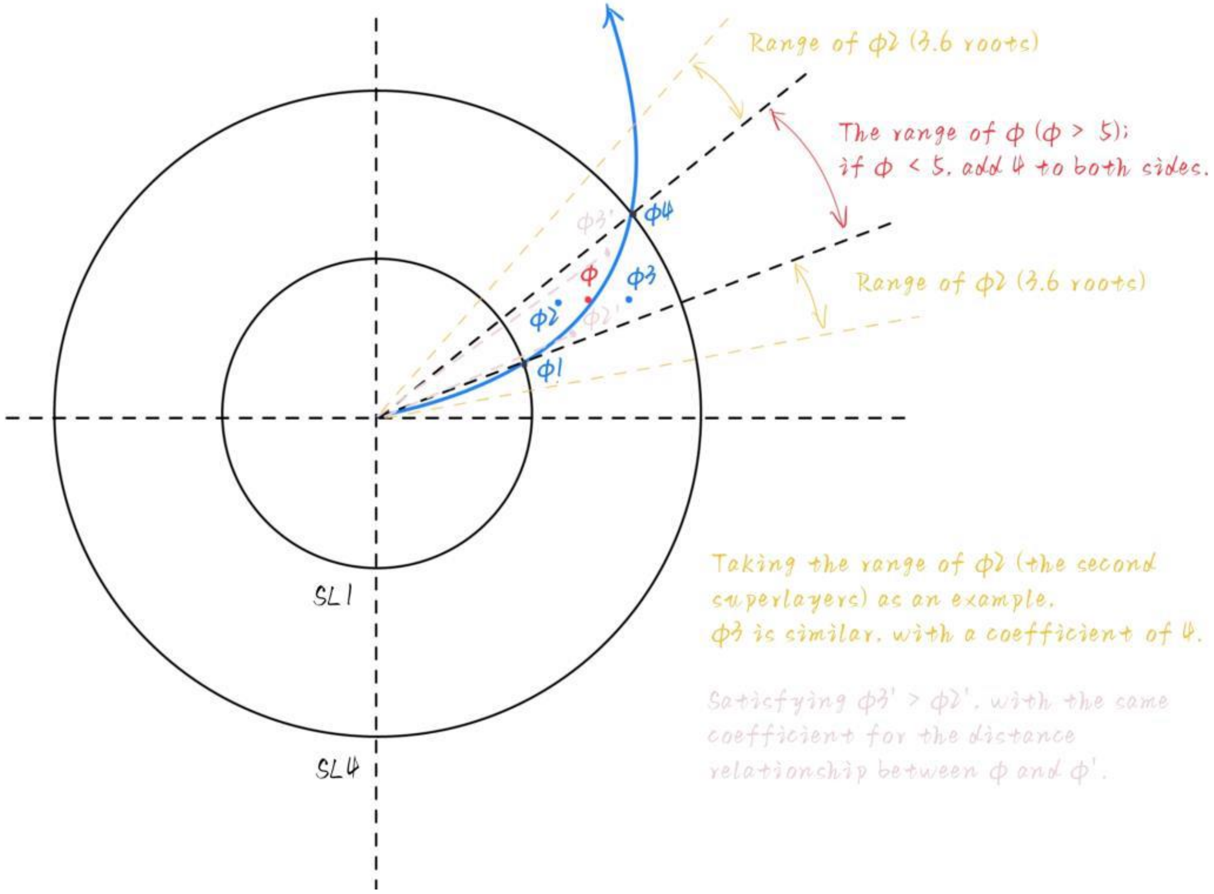
☐ XY 2D tracking and reconstruction

Long track: axial superlayers





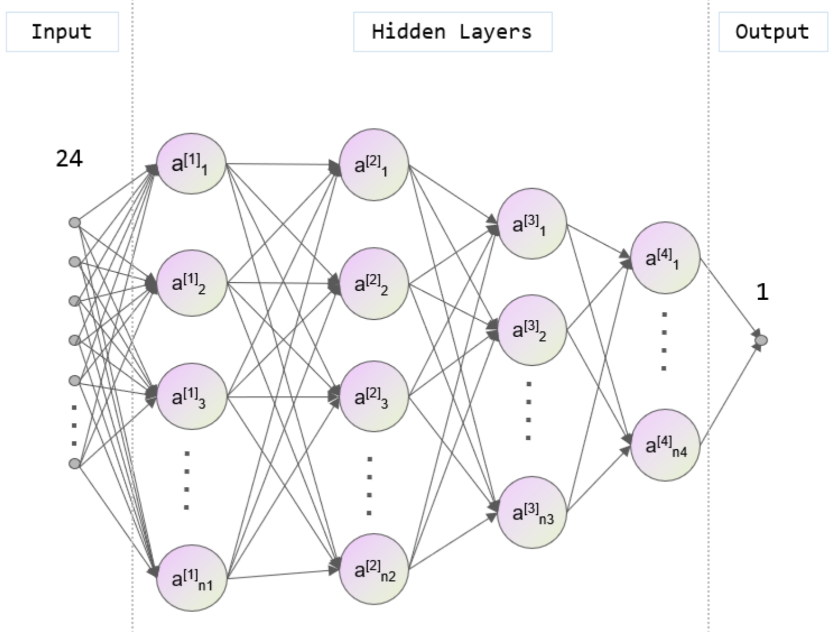
Short track: axial + stereo superlayers



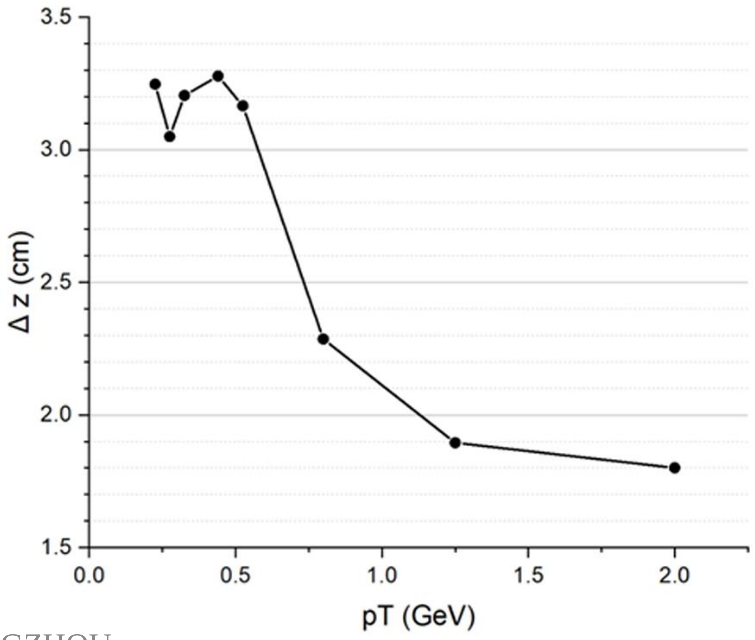
MDC sub-trigger R&D

☐ XY 3D reconstruction

- **Multi-layer fully connected neural network (MLP)**
- Input: TS numbers and TDC for 8 superlayers
- Output: z-vertex in various p_t regions

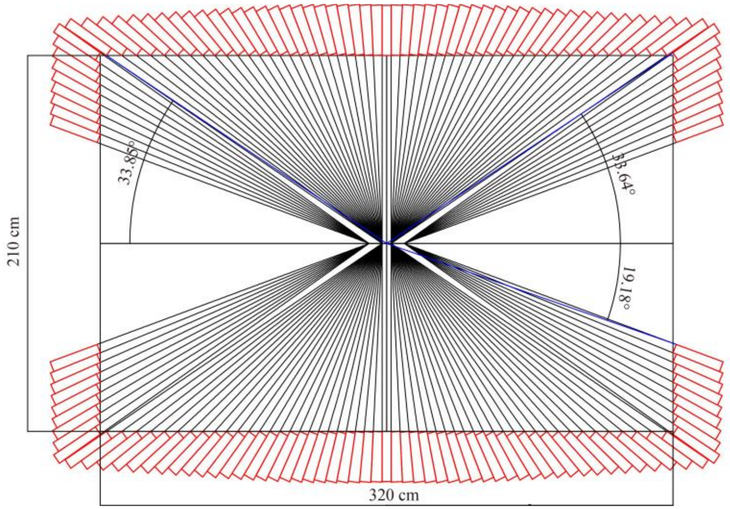


- Using **pruning** method and **High Granularity Quantization (HGQ)**
- DSP: 71% → **4%**
- FF: 29 % → **4%**
- LUT: 19% → 17%



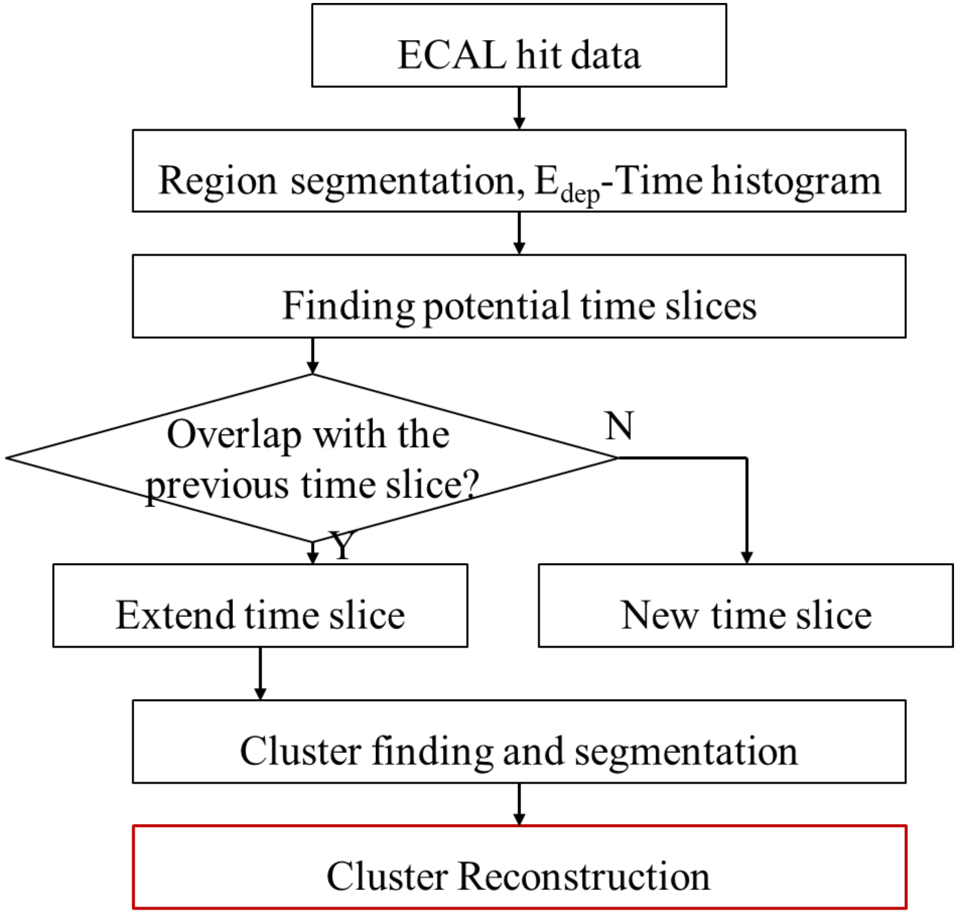
ECAL sub-trigger R&D

ECAL structure

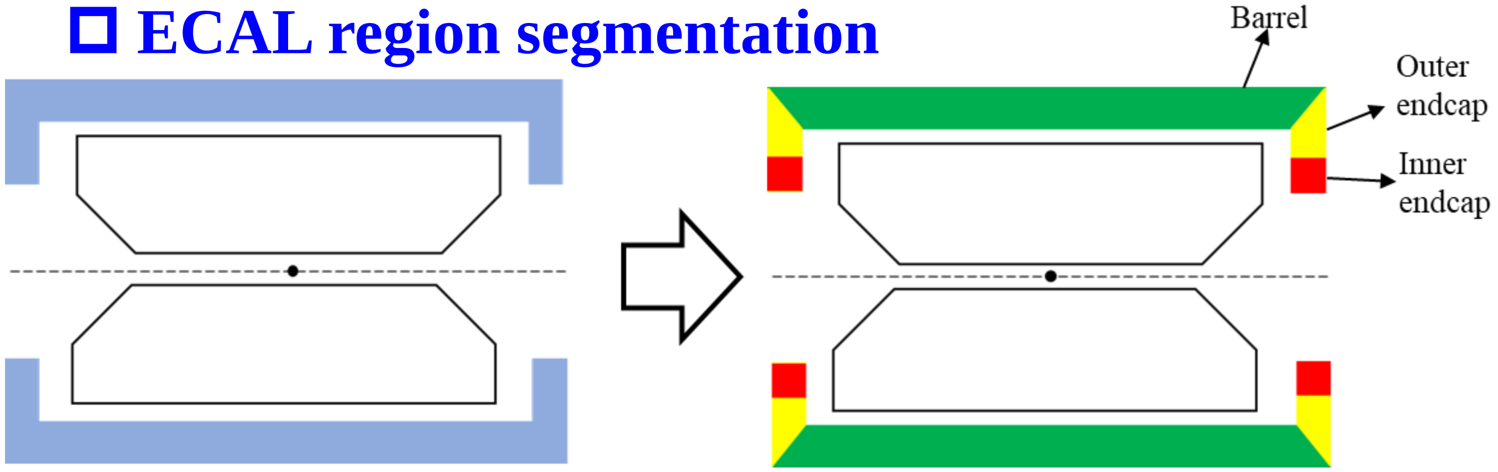


- Trigger cell:
- Barrel: 4×4 or 3×4
- Endcap: 3×5 or 4×5

ECAL algorithm

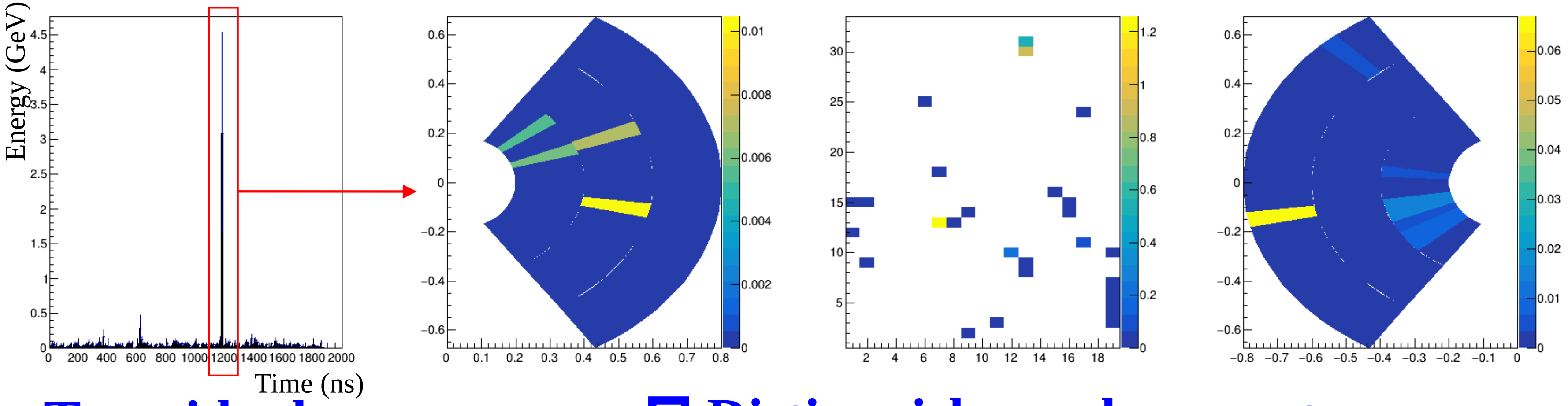


ECAL region segmentation

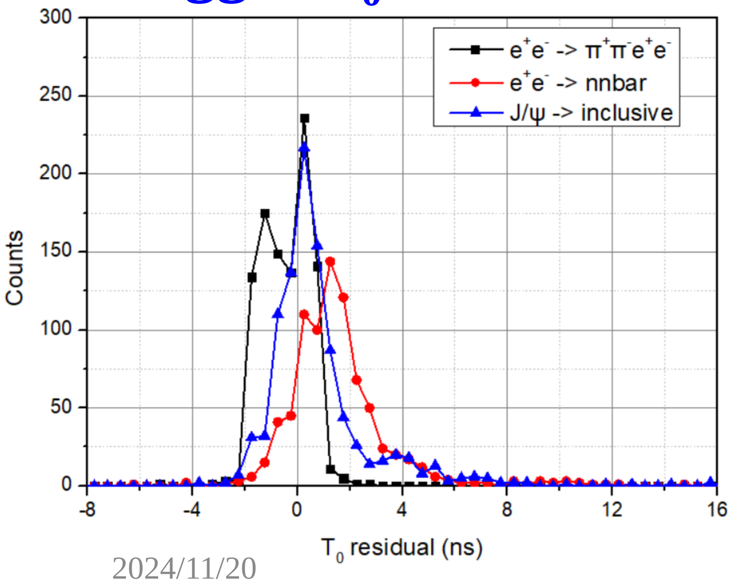


ECAL sub-trigger R&D

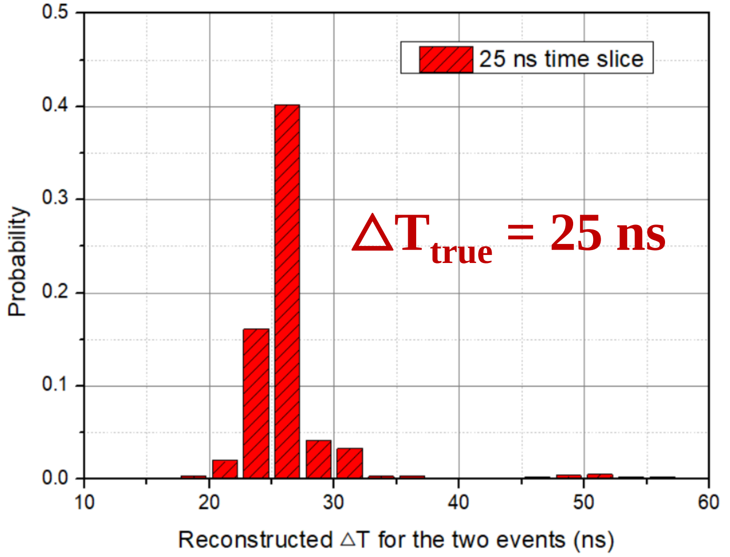
Time slice selection and cluster mapping in ECAL

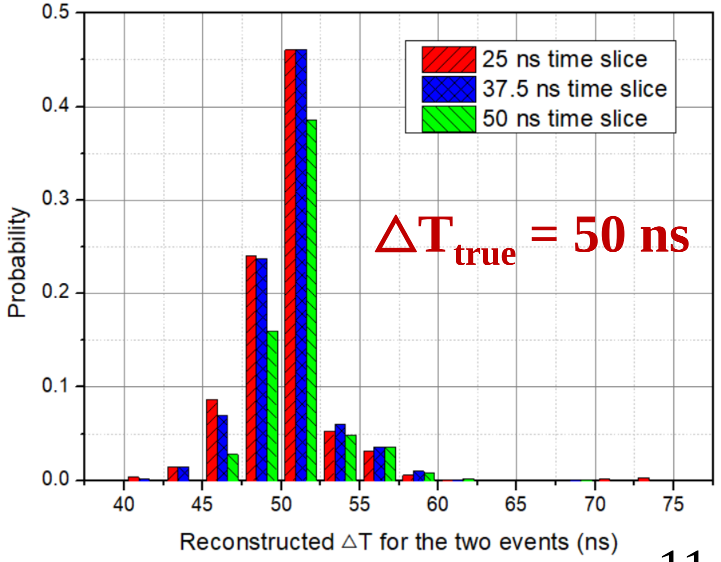


Trigger T_0 residual



Distinguish overlap events

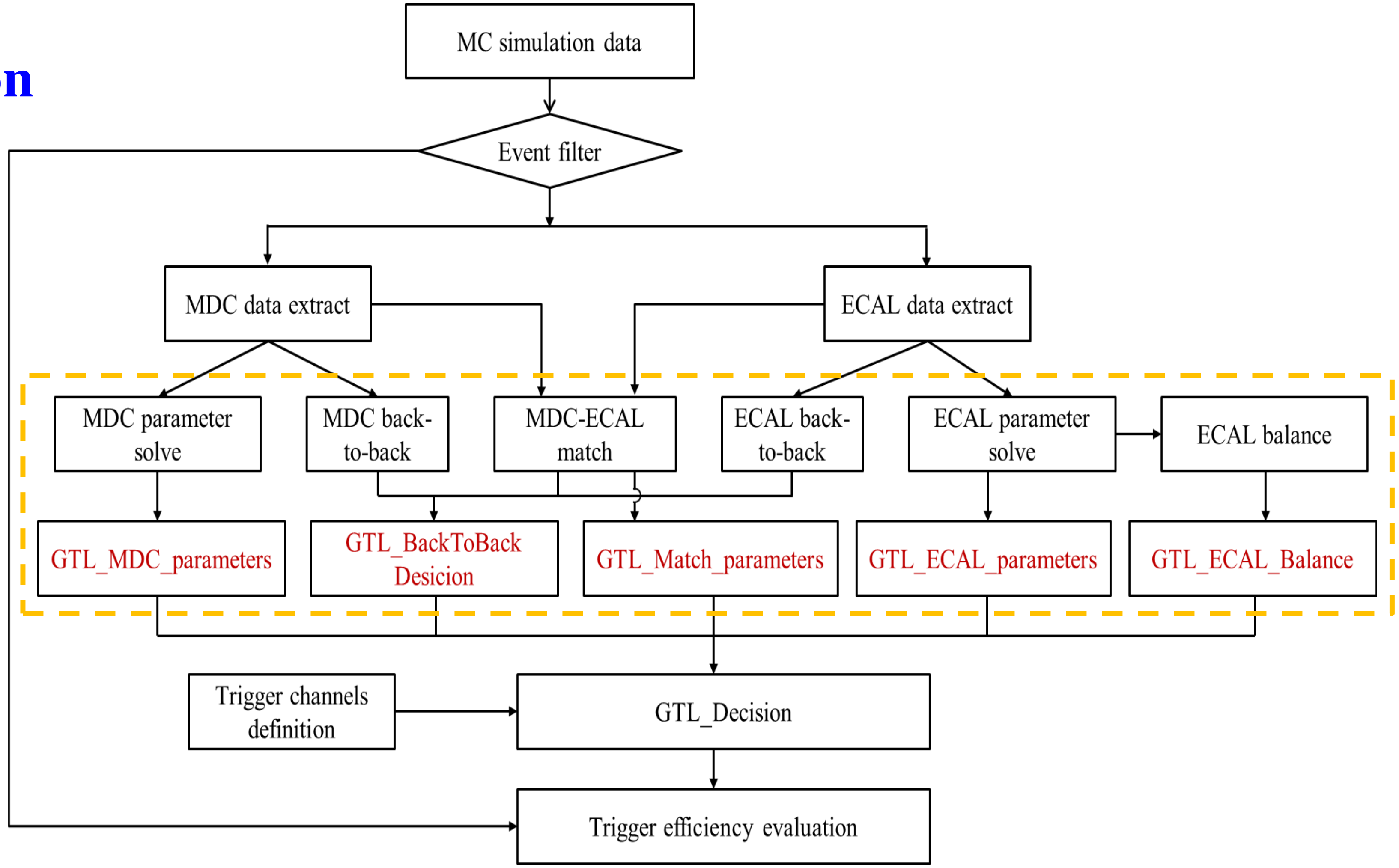




L1 trigger GTL R&D

L1 trigger GTL optimization

- Frame design
- Algorithm development
- Trigger table design
- Performance evaluation



Current trigger table

- 4 charged channels
- 1 neutral channel
- 1 luminosity monitor channel

Large trigger table

		1	2-1	2-2	2-3	2-4	3-1	3-2	3-3	4-1	4-2	4-3	5-1	5-2	5-3	5-4	6	7	8	9-1	9-2	10-1	10-2	10-3	10-4	11	12	13	14	15	16	17
L. M.	1-1									Y			Y													Y		Y				Y
	1-2									Y			Y													Y			Y			
	1-3									Y			Y													Y				Y		
Charged	2-1	N		Y							Y						Y						Y			N					Y	
	2-2	N		Y							Y							Y	Y				Y			N					Y	
	2-3	N		Y							Y		Y										Y			N					Y	
	3-1	N	Y			N	Y		N	Y				Y		Y	Y								N							
	3-2	N	Y			N	Y		N	Y				Y		Y		Y	Y						N							
	3-3	N		Y		N	Y		N	Y			Y			Y					Y		Y		N							
	3-4	N	Y			N	Y		N	Y				Y		Y				Y		Y			N							
	3-5	N	Y			N		Y	N	Y				Y			Y								N							
	3-6	N	Y			N		Y	N	Y				Y				Y	Y						N							
	3-7	N		Y		N		Y	N	Y			Y								Y		Y		N							
	3-8	N	Y			N		Y	N	Y				Y						Y		Y			N							
	4-1	N			Y	N						Y			Y		Y					Y										
	4-2	N			Y	N						Y			Y			Y	Y			Y										
	4-3	N			Y	N						Y		Y							Y	Y		Y								
	5-1	N				Y											Y					Y										
	5-2	N				Y												Y	Y			Y										
	5-3	N													N		Y					Y										
	5-4	N													N			Y	Y			Y										
Neutral	6-1	N		Y																						N	Y					
	6-2	N		Y																				Y		N						
	6-3	N	Y	N																			Y			N						
Random	7																						N									

L1 trigger performance

- **False trigger rate <30 kHz** @ charged channels; **<70 kHz** @ neutral channels

Trigger channel	Physics signal	Energy point	No. of tracks should(is) matched	No. of matched tracks in Endcap	No. of matched tracks in Barrel	Signal trigger rate	Background false trigger rate (kHz)	Signal trigger rate
Charged channel	$e^+e^- \to \pi^+\pi^-$Jpsi; Jpsi -> e^+e^-	4.26GeV	3550 (3230)	448 (226)	3102 (3004)	948/952 (≥3)	24.5	99.6%
	$e^+e^- \to \pi^+\pi^-$Jpsi; Jpsi -> $\mu^+\mu^-$	4.26GeV	3518 (3191)	452 (203)	3066 (2988)	945/948 (≥3)		99.7%
	$e^+e^- \to \tau^+ \tau^-$	4.26GeV	1717 (1600)	186 (88)	1531 (1512)	867/879 (≥2)		98.6%
	$e^+e^- \to \pi^+\pi^-$Jpsi; Jpsi -> $\Lambda \bar{\Lambda}$	3.097GeV	2550 (2348)	220 (129)	2330 (2219)	903/918 (≥3)		98.4%
	$e^+e^- \to \pi^+\pi^-$Jpsi; Jpsi -> $\Xi \bar{\Xi}$	3.097GeV	2713 (2864)	198 (148)	2515 (2716)	913/922 (≥5)		99.0%
	$e^+e^- \to K^+K^-$Jpsi; Jpsi -> l^+l^-	4.682GeV	3515 (3144)	365 (182)	3150 (2962)	954/964 (≥3)		99.0%
	$e^+e^- \to D_0 \bar{D_0}$	3.773GeV	3387 (3160)	312 (170)	3075 (2990)	953/954 (≥3)		99.9%
	$e^+e^- \to D^+ D^-$	3.773GeV	4031 (2707)	274 (64)	2640 (2643)	980/983 (≥3)		99.7%
	$e^+e^- \to D_s^+ D_s^-$	4.04GeV	4770 (4258)	462 (263)	4308 (3995)	932/936 (≥5)		99.6%
Neutral channel	J/psi-> gam invisable	3.097GeV	-	-	-	542/546 (≥1&&gam_momentum>=1)	69.0	99.3%
	e+e- -> n nbar	3.097GeV	-	-	-	565/575 (≥2&&Nbar≥1&&EDep≥0.5)		98.3%
	e+e- -> gam n nbar	3.097GeV	-	-	-	753/756 (≥2&&Nbar≥1&&EDep ≥1)		99.7%
	e+e- -> gam n nbar(ISR)	3.713GeV	-	-	-	427/435 (≥2&&Nbar≥1&&EDep≥0.7)		98.2%
Luminosity monitor	RBB	4.26GeV	382	96	286	188/191		98.4%

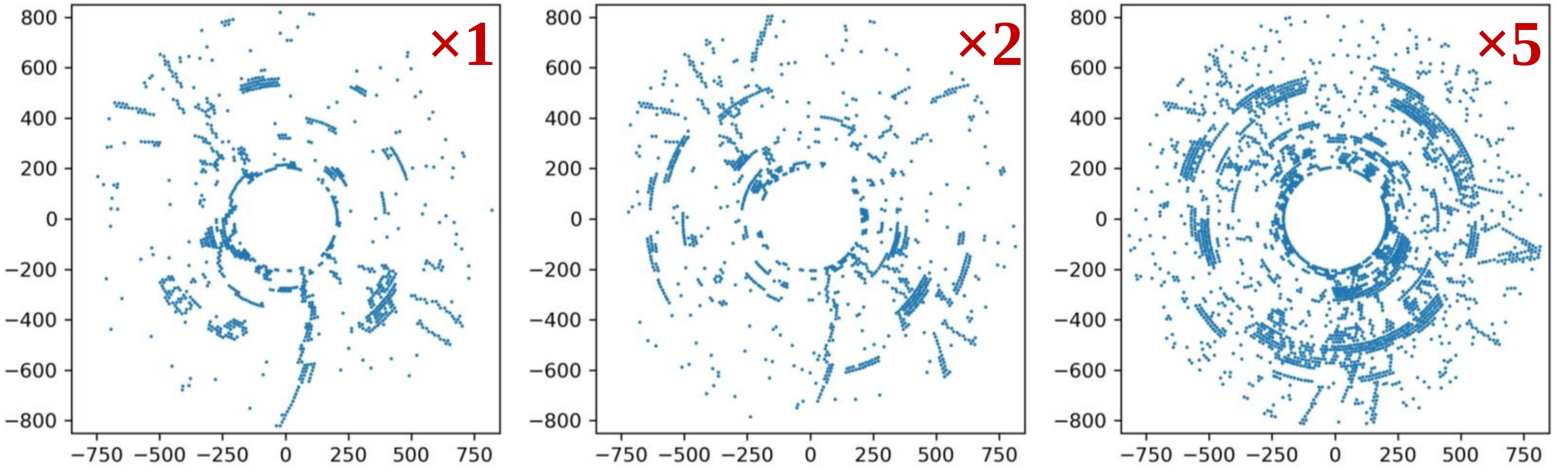
L1 trigger performance

☐ Multi-BKG trigger

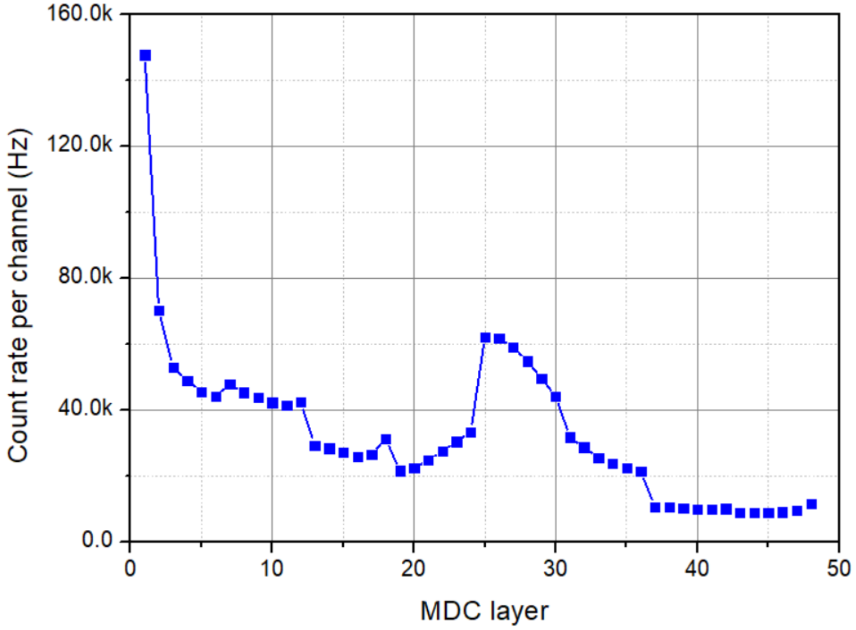
- $e^+e^- \to \pi^+\pi^- J/psi,$
  $J/psi \to e^+e^-$

Background factor	×1	×2	×5
Trigger rate	99.7%	99.2%	58.3%
False trigger (kHz)	21.3	56.7	178.6

☐ MDC hitting map for a same event with various background level



☐ MDC background count rate

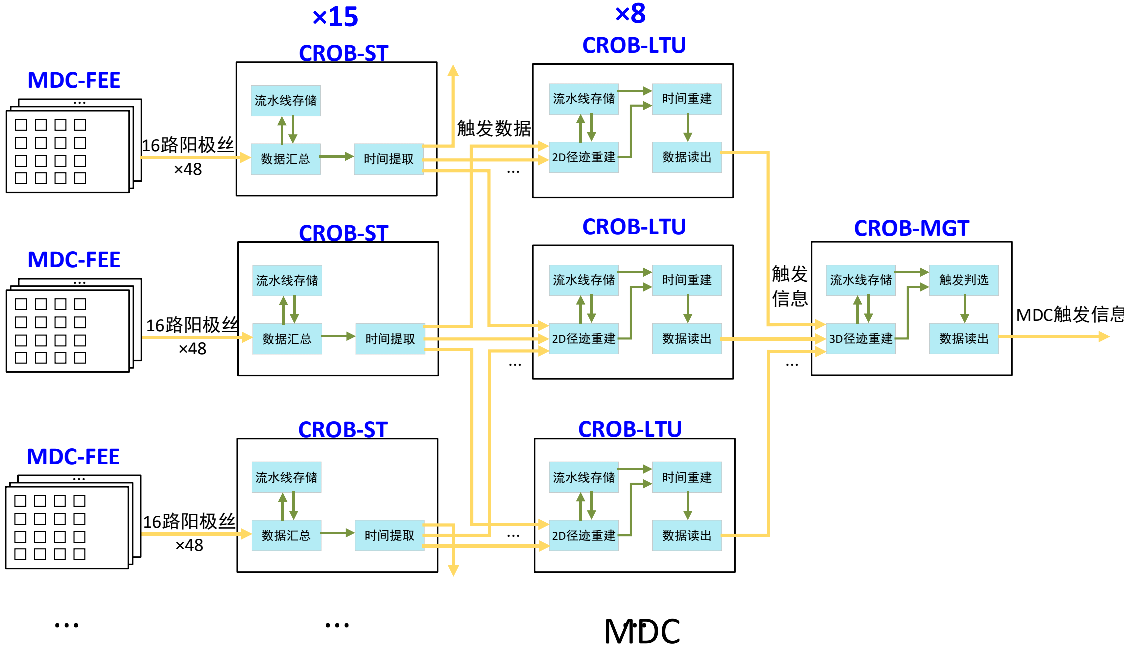


Outline

1. STCF and Trigger system
2. L1 trigger algorithm progress
3. **L1 trigger hardware platform R&D**
4. HLT study
5. Summary

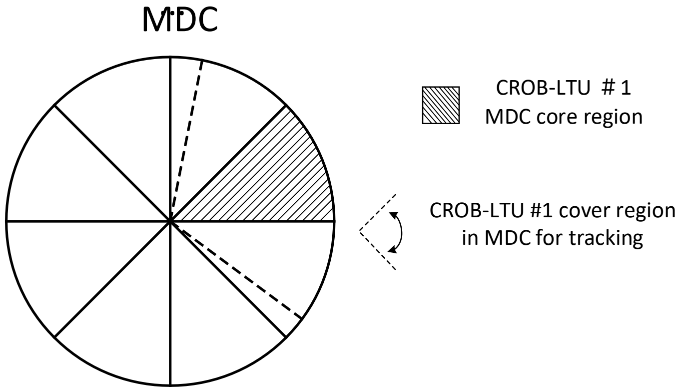
FPGA-based hardware platform for L1 trigger

▢ MDC sub-trigger

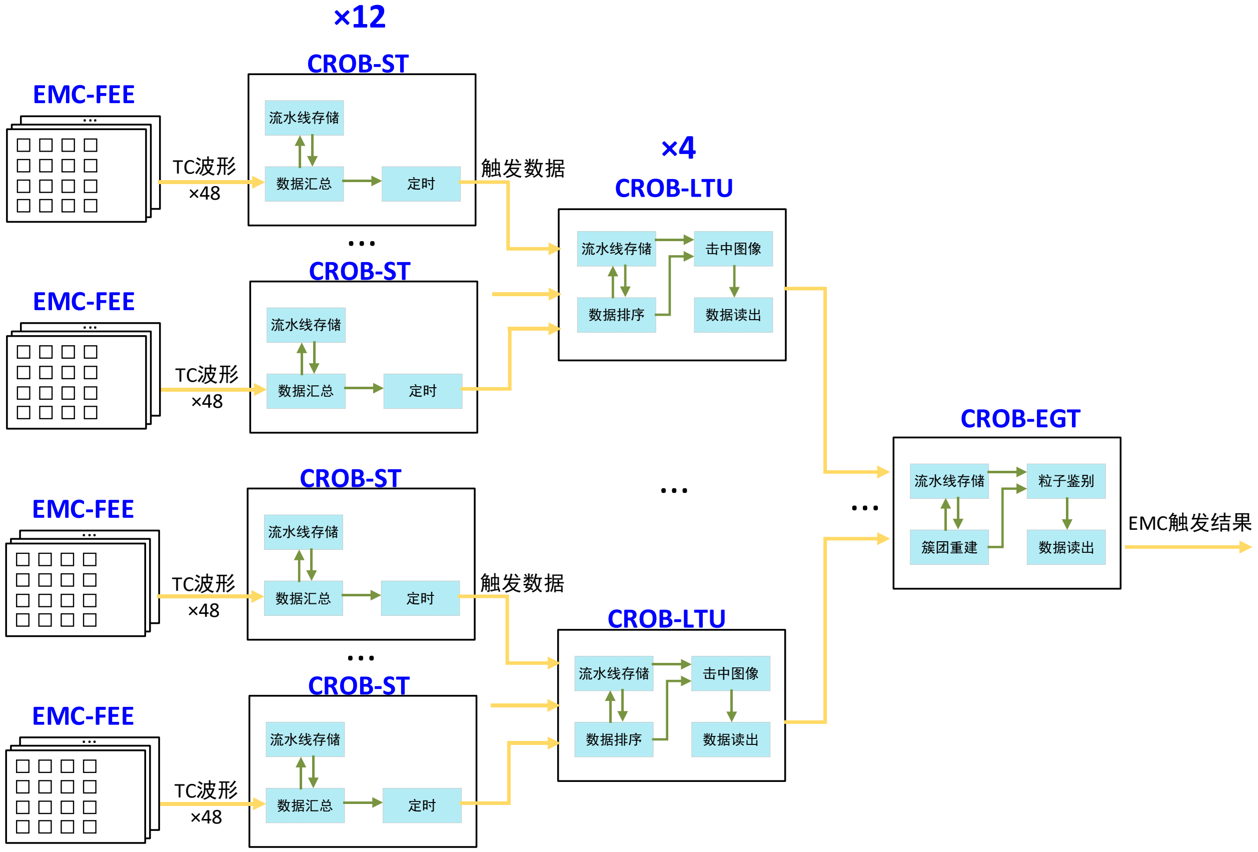


Cover range of each LTU

in MDC sub-trigger

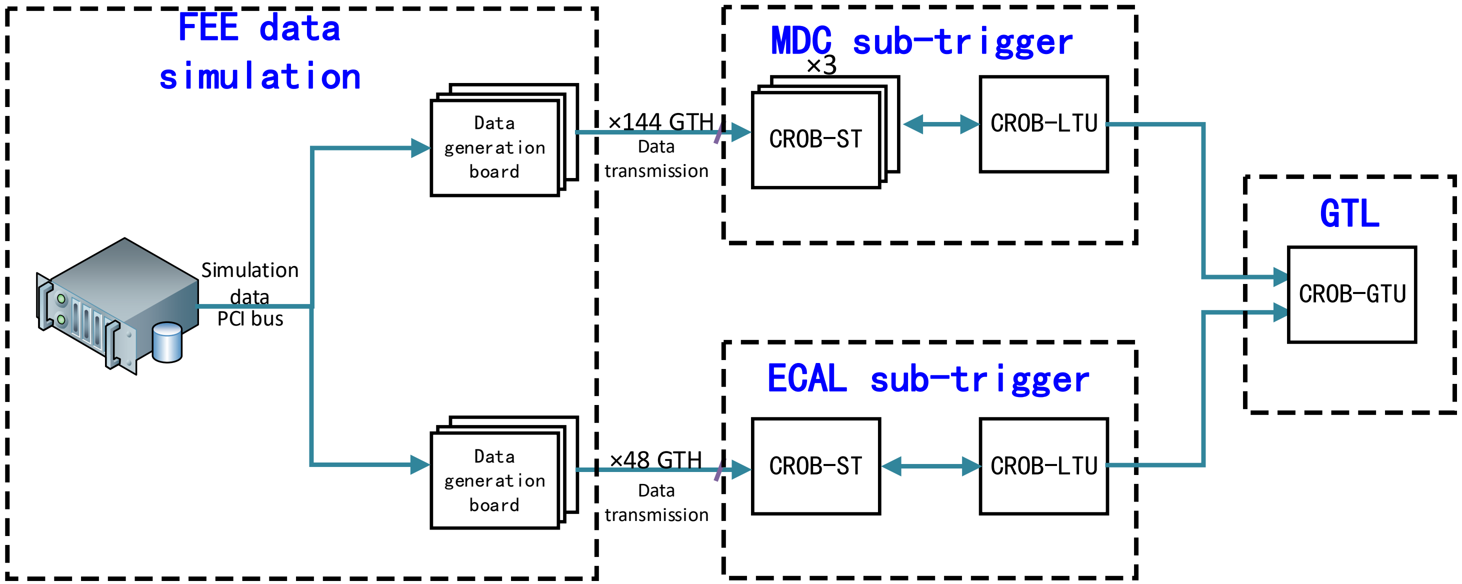


▢ ECAL sub-trigger

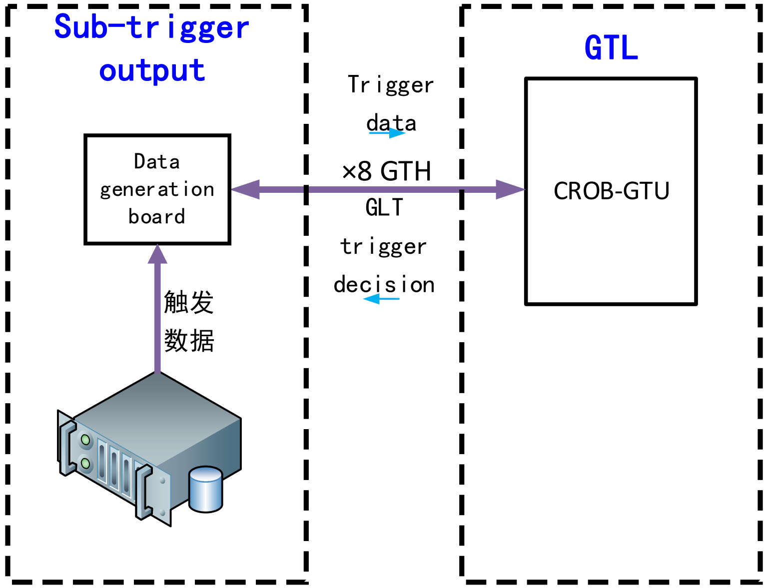


Prototype for L1 trigger

◻ Test for frame and sub-trigger algorithm



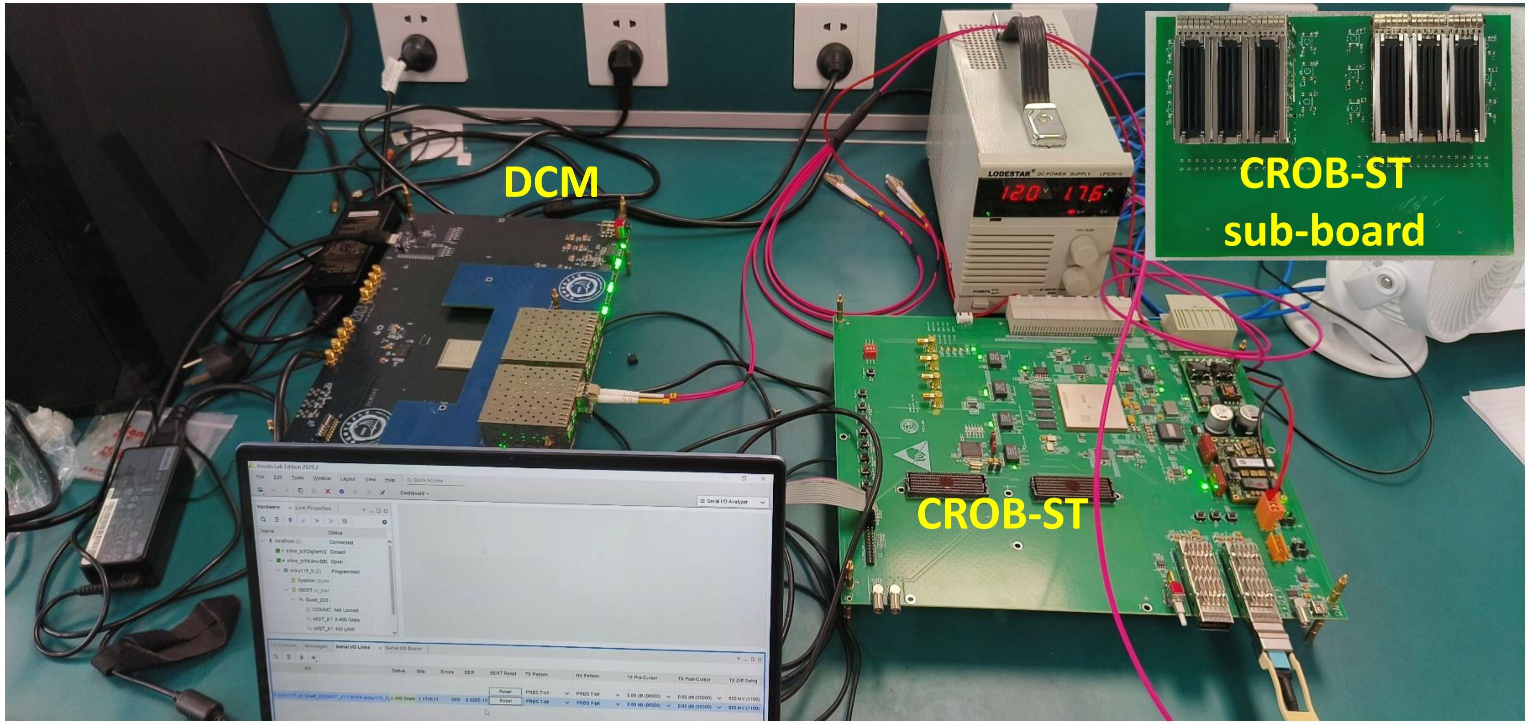
◻ GTL test



- Prototype: **1/8 MDC (cover 1/3 of MDC)**、**1/4 ECAL**
- Frame verification: data transmission, latency
- Sub-trigger algorithm performance evaluation
- GTL performance evaluation

Key board R&D

□ Test of 1st version of key boards

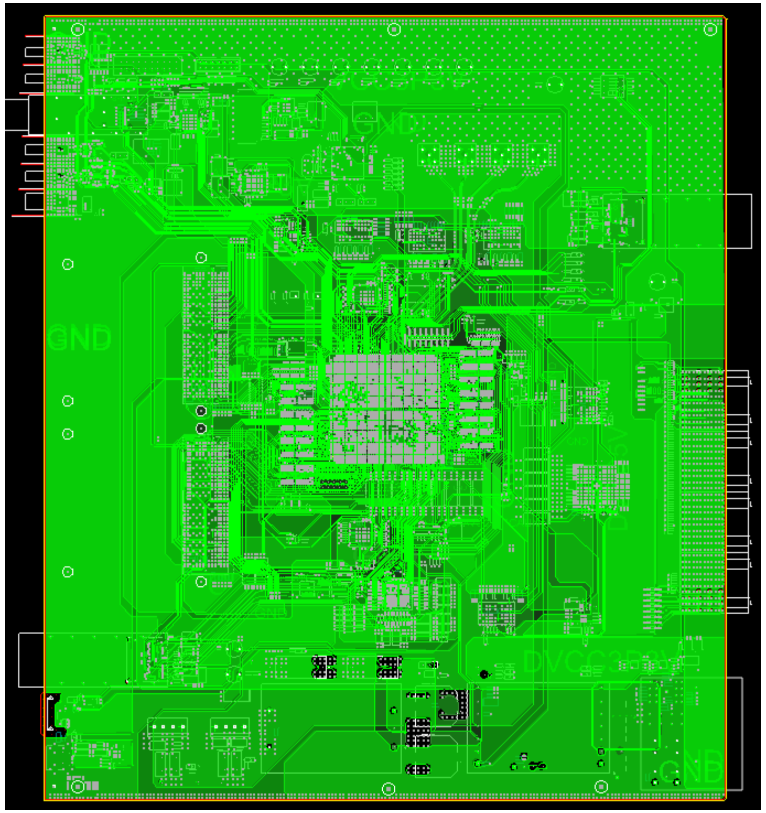


- □ **CROB-ST board test**
  - ✓ Power supply
  - ✓ FPGA
  - ✓ DDR4
  - ✓ SCM
  - ✓ Sub-board
  - × GTH
- □ Running MDC sub-trigger algorithm

Key board R&D

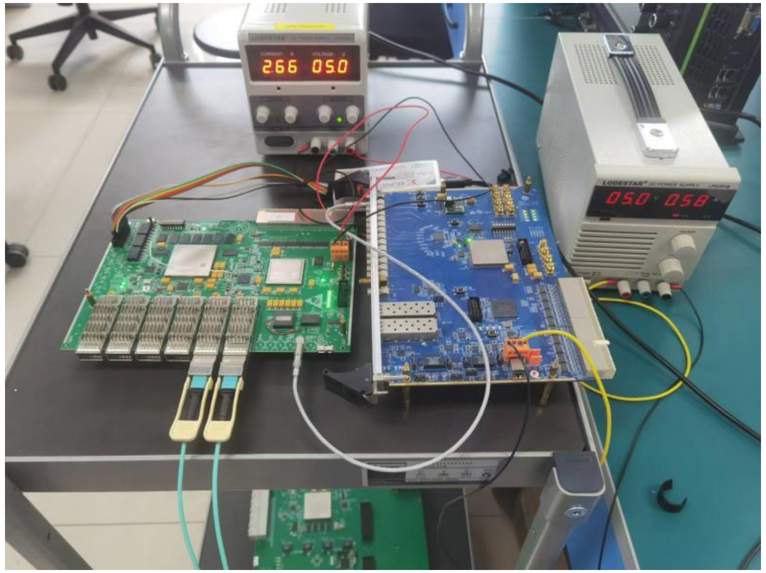
New version of CROB-ST

- ✓ Meet the multi-system beam test requirement

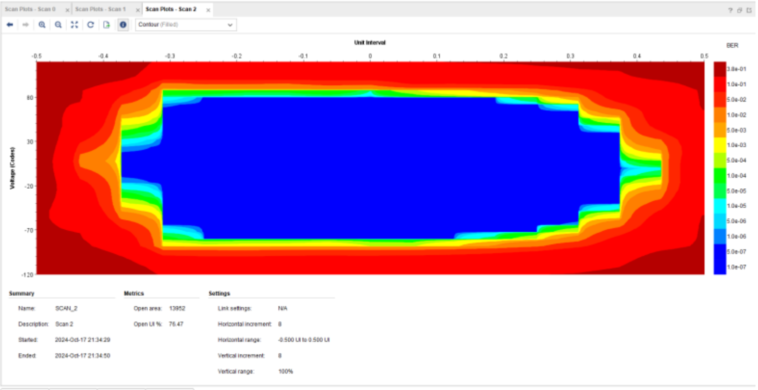


Data Generation Board

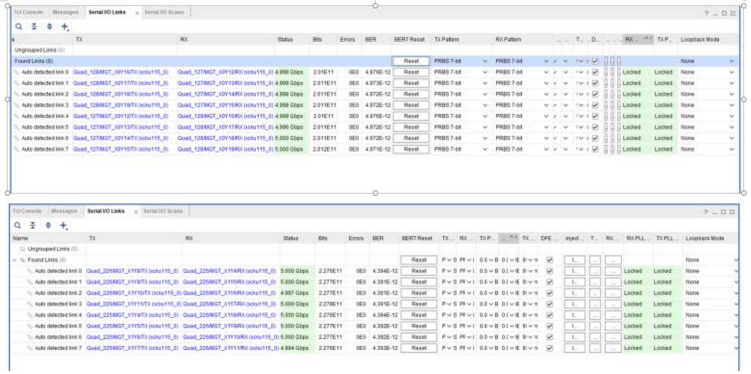
✓ Power	• DDR4
✓ FPGA	• Chassis
✓ Optical port	• PLL



Eye map of optical port



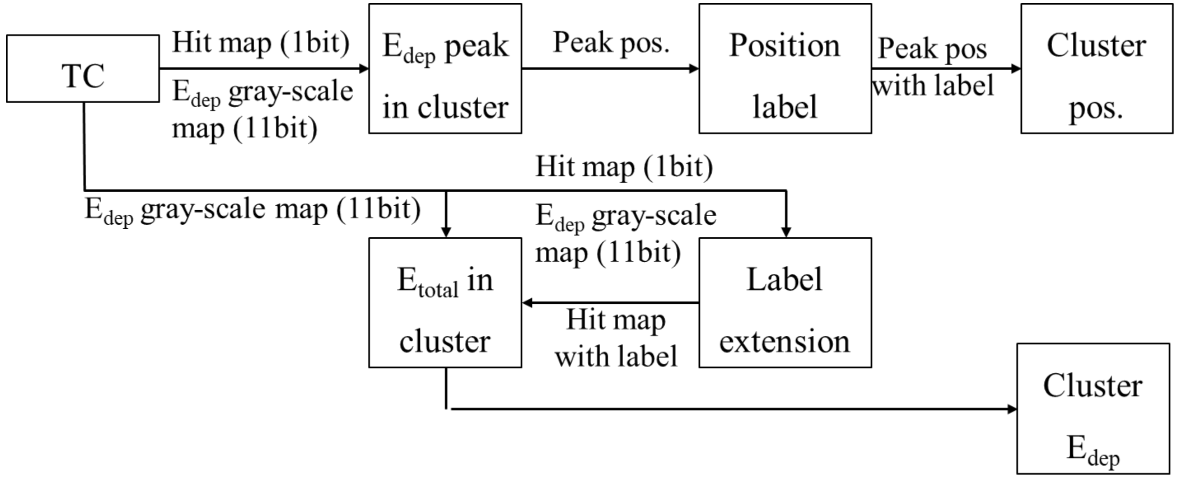
Link test for optical port



Hardware algorithm implementation

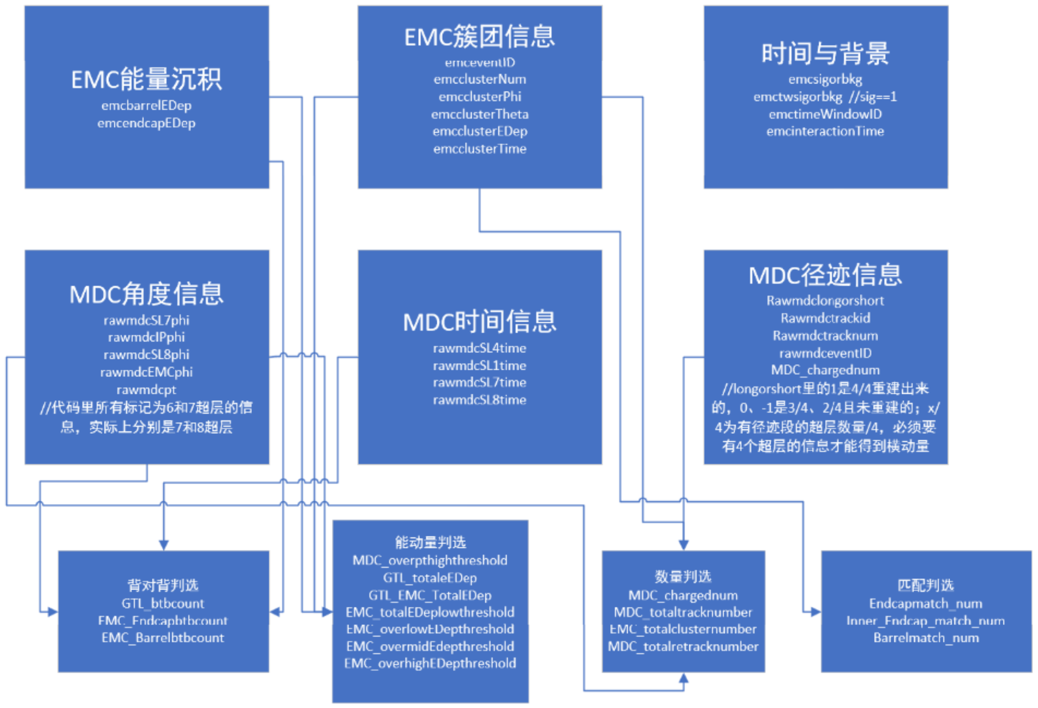
☐ ECAL cluster segmentation

- Finding peak, segmenting cluster based on gray-scale map
- Control the number of cycles
- Test the extremes



☐ GTL hardware algorithm

- ➢ Matrix calculation for loop computation
- ➢ Computing source evaluation



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3. L1 trigger hardware platform R&D
4. **HLT study**
5. Summary

Routes for HLT

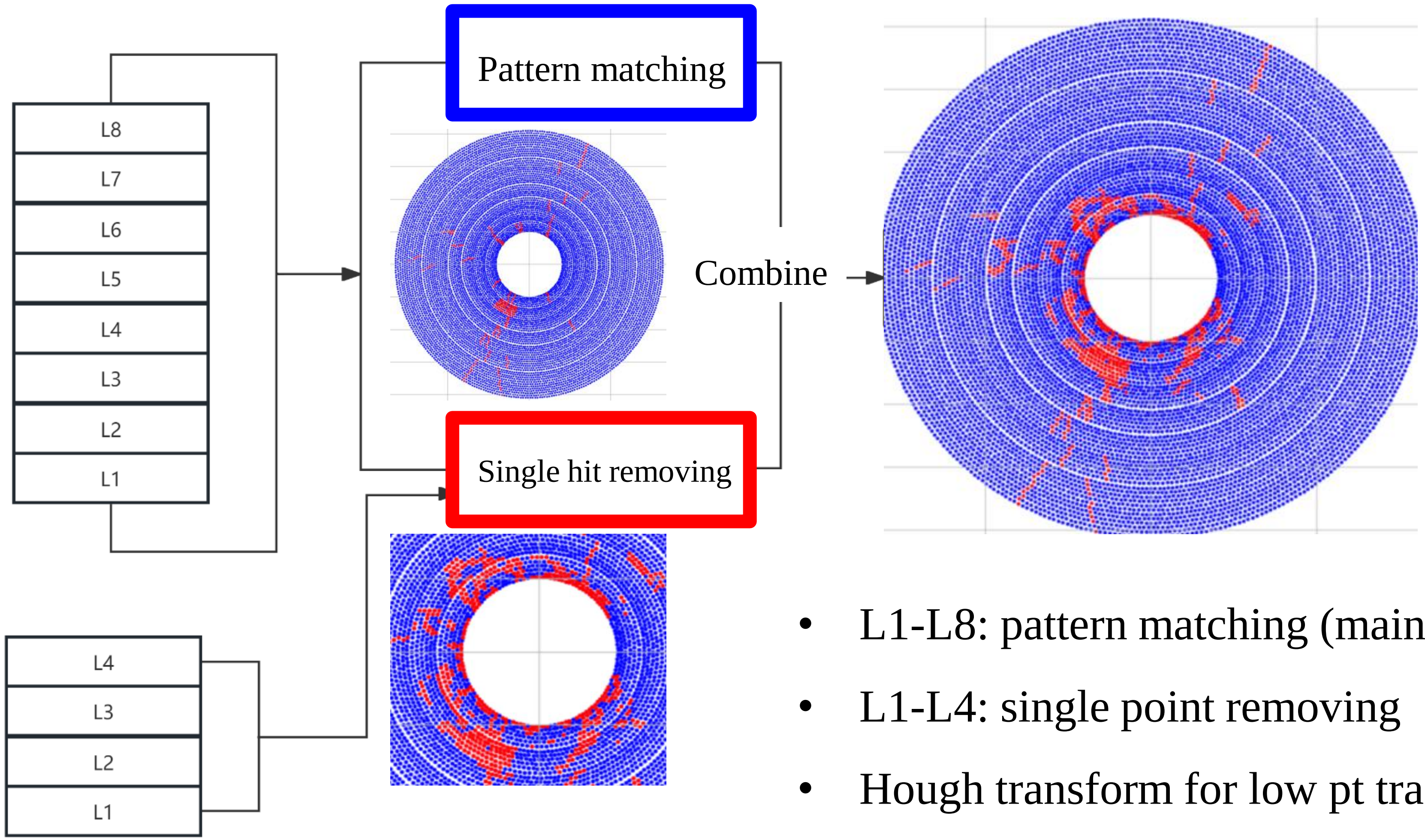
- **HLT: Reduce data size**
  - Based on server cluster (CPU + GPU ?)
  - Identify and remove background hits
  - (Using offline reconstruction algorithm or develop a simpler one?)

- Peak physics event rate ~ 400 kHz
- Normal physics event rate ~ 50 kHz
- L1 background false trigger ~ 40 kHz

- **Preliminary HLT routes** for each detector:
  - **ITK**: hit reconstruction
  - **MDC**: Single hit removing,
    Hough transform/pattern matching
  - **PIDB & PIDE**: T_0 reconstruction
  - **ECAL**: cluster-level analyzing
  - **MUON**: global analyzing / no HLT

MDC HLT study progress

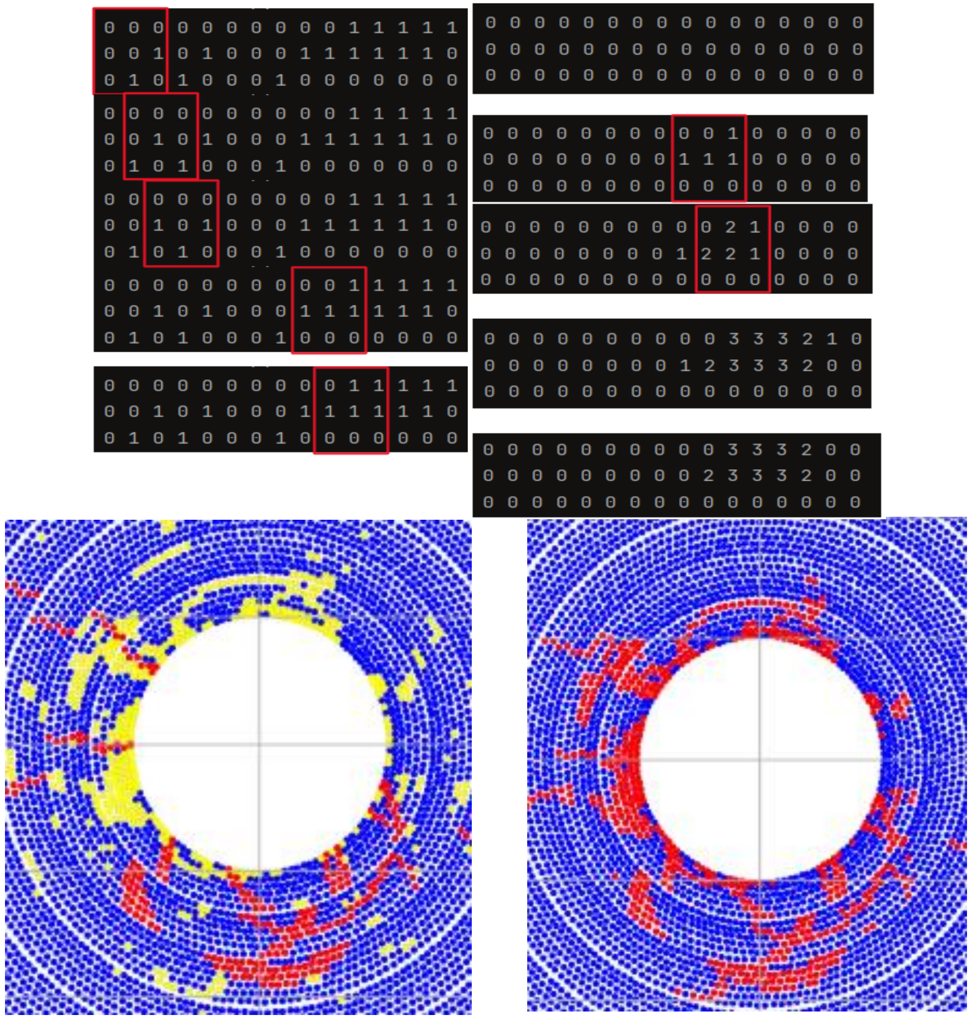
New algorithm for MDC HLT



- L1-L8: pattern matching (mainly for L5-L8)
- L1-L4: single point removing
- Hough transform for low pt track

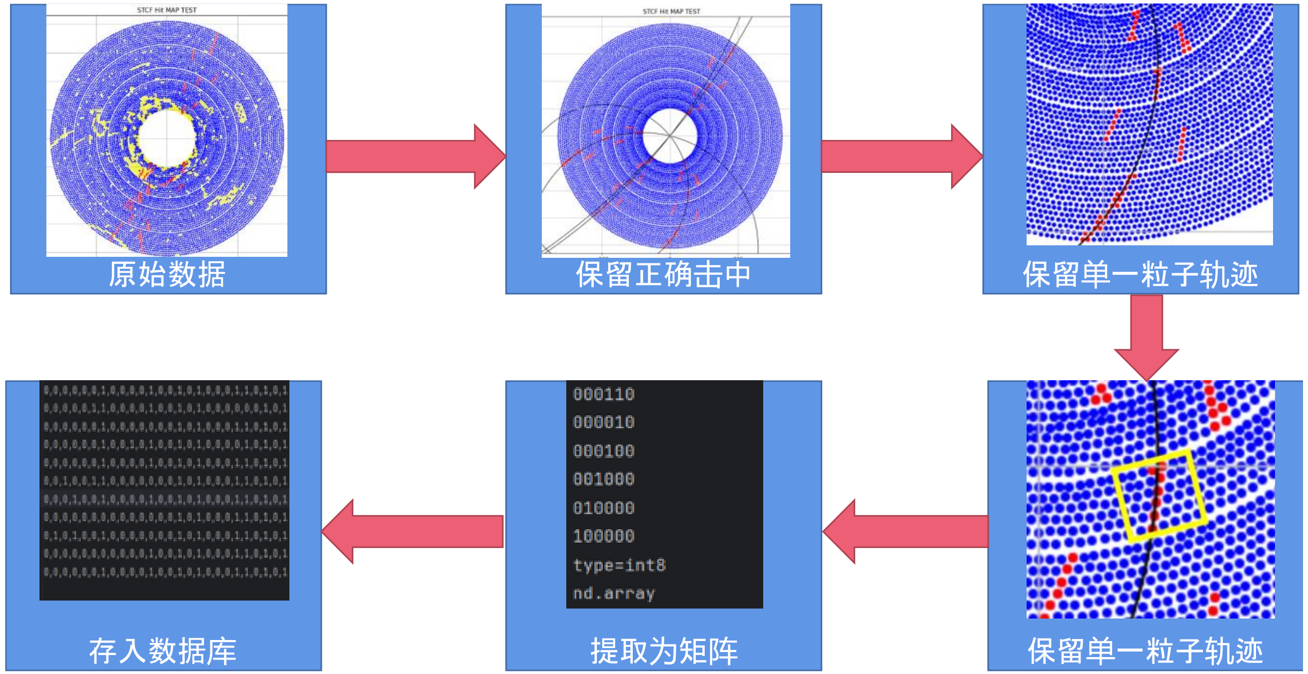
MDC HLT study progress

◻ Single hit removing: accuracy >99%



◻ Pattern matching

- Target: track pt > 250 MeV/c
- Efficiency highly depends on the pattern bank



Outline

Summary

- **L1 trigger algorithm:**
  - ✓ Trigger efficiency to typical charged physics channel: **99%**
  - ✓ Background trigger rate: **< 30 kHz** @ charged channels; **< 70 kHz** @ neutral channels
- **Hardware platform and prototype:**
  - ✓ Design and test of 2^{nd} version of boards
  - ✓ MDC latency test: **340 ns** (2D) **+ 210 ns** (timing) **+ 125 ns** (3D) **= 675 ns**
  - ➢ Hardware algorithm implementation
- **HLT:**
  - ➢ Preliminary HLT routes design for detectors
  - ➢ MDC HLT study

Thanks~

Back up

<table>
<tr><th>No</th><th>触发道类型</th><th>触发道设置</th></tr>
<tr><td>1</td><td>RBB道</td><td>(EMC_Endcapbtbcount==1||EMC_Barrelbtbcount==1||MDC_RBBcount==1)&&MDC_chargednum<=4&&MDC_totaltracknumber>0&&MDC_totalretracknumber<4&&GTL_totaleEDep>=3</td></tr>
<tr><td>2</td><td>带有背靠背特征的末态带电道</td><td>IfRBB==0&&GTL_btb==1&&(((EMC_totalclusternumber>=2&&MDC_totaltracknumber>=2)&&(Barrelmatch_num>=1||(Endcapmatch_num>=1&&Endcapmatch_num<=2&&Inner_Endcap_match_num<1)))||(MDC_totalretracknumber<=1&&EMC_totalclusternumber>=2))&&EMC_TotalClusterEDep>=0.4&&GTL_totaleEDep<3</td></tr>
<tr><td>3</td><td>少量末态带电径迹道</td><td>IfRBB == 0 && ((EMC_totalclusternumber>=1&&EMC_totalclusternumber<=6 && ((EMC_overlowEDepthreshold>=1 && MDC_totalretracknumber<=EMC_overlowEDepthreshold+1) || EMC_overmidEDepthreshold>=1)) && (MDC_totaltracknumber>=1&&MDC_totalretracknumber<=3)) && (Barrelmatch_num>=1 || (Endcapmatch_num>=1 && Endcapmatch_num<=2 && Inner_Endcap_match_num<=1) || (Match_Info[0].size() == 0 && GTL_EMC_TotalEDep>=EMC_totalEDepmidthreshold && MDC_totalretracknumber<=1 && EMC_totalclusternumber>=2) || (Match_Info[0].size()>=2 && GTL_EMC_TotalEDep>=0.1)) && GTL_EMC_TotalEDep<EMC_totalEDephighthreshold && EMC_overhighEDepthreshold<=1</td></tr>
<tr><td>4</td><td>中量末态带电径迹道</td><td>IfRBB==0&&((EMC_totalclusternumber>=3&&EMC_totalclusternumber<=7)&&(MDC_totaltracknumber>=3&&MDC_totalretracknumber<=7))&&(Barrelmatch_num>=1||(Endcapmatch_num>=1&&Endcapmatch_num<=2&&Inner_Endcap_match_num<=1)||(Match_Info[0].size()==0&&(GTL_EMC_TotalEDep>=0.6)&&MDC_totalretracknumber<=4&&EMC_totalclusternumber>=3))&&GTL_EMC_TotalEDep>=EMC_totalEDeplowthreshold</td></tr>
<tr><td>5</td><td>大量末态带电径迹道</td><td>IfRBB == 0&&(EMC_totalclusternumber>=7||MDC_totalretracknumber>=7)&&(Barrelmatch_num>=1||(Endcapmatch_num>=1&&Endcapmatch_num<=2&&Inner_Endcap_match_num<1))&&GTL_EMC_TotalEDep>=EMC_totalEDeplowthreshold</td></tr>
<tr><td>6</td><td>中性道</td><td>IfRBB==0&&((EMC_totalclusternumber>=2&&(EMC_BarrelEDep>=0.4||GTL_EMC_TotalEDep>=0.6))||(EMC_totalclusternumber==1&&GTL_EMC_TotalEDep>=0.4))&&GTL_totaleEDep<3</td></tr>
<tr><td>7</td><td>随机触发</td><td></td></tr>
</table>

No	EMC触发条件	定义
2	EMC_totalclusternumber	EMC时间片段中的总簇团数量>=1, >=2, >=3, >=7
3	EMC_overEDepthreshold	EMC时间片段中分别过簇团低阈0.1GeV(>=1)、中阈0.24GeV(>=1)、高1.3GeV阈(>=1)的簇团数量
10	EMC_TotalClusterEDep	EMC时间片段中的总簇团能量沉积大小，低(除少径迹道0.1外其他均为0.28)，中1(0.4)，中2(0.6)，高(3.5)四个阈值
12	EMC_BarrelEDep	桶部簇团能量沉积的大小，中性道专用，0.4GeV
13	EMC_Endcapbtb	EMC端盖位置的簇团是否满足背靠背条件
14	EMC_Barrelbtb	EMC桶部位置的簇团是否满足背靠背条件
11	EMC_TotaleEDep	EMC中能量沉积超过1GeV的簇团能量沉积之和，用以代替电子的能量沉积之和，阈值为3GeV

- 存在多个子条件时按照本页表中出示的顺序依次标记为No-1……No-n
- 特殊*的含义是利用本底时间片段中多只有一个簇团的特点，设置MDC_totalretracknumber≤EMC_overEDepthreshold+1条件，可以以此令部分簇团能量沉积少的事例通过触发，后续可能会删除

No	MDC触发条件	定义
4	MDC_totaltracknumber	MDC事例中识别径迹的数量>=1,>=2, >=3
5	MDC_totalretracknumber	MDC事例中重建径迹的数量<=1,<=4,<=7,特殊*
15	MDC_RBB	MDC事例中径迹能否满足背靠背判选条件
17	MDC_chargednum	MDC带电径迹数量

No	GTL触发条件	定义
6	Barrelmatch_num	桶部完成了匹配的簇团和径迹数量
7	OuterEndcapmatch_num	外端盖完成了匹配的簇团和径迹数量
8	InnerEndcapmatch_num	内端盖完成了匹配的簇团和径迹数量
9	Match_num	总的匹配数量>=2,==0
16	GTL_btb	是否在MDC和EMC中均能满足背靠背判选且能够完成匹配
1	IfRBB	是否满足RBB道触发条件

	1	2-1	2-2	2-3	2-4	3-1	3-2	3-3	4-1	4-2	4-3	5-1	5-2	5-3	5-4	6	7	8	9-1	9-2	10-1	10-2	10-3	10-4	11	12	13	14	15	16	17
1-1									Y			Y													Y		Y				Y
1-2									Y			Y													Y			Y			
1-3									Y			Y													Y				Y		
2-1	N		Y							Y						Y						Y			N					Y	
2-2	N		Y							Y							Y	Y				Y			N					Y	
2-3	N		Y							Y		Y										Y			N					Y	
3-1	N	Y			N	Y		N	Y				Y		Y	Y								N							
3-2	N	Y			N	Y		N	Y				Y		Y		Y	Y						N							
3-3	N		Y		N	Y		N	Y			Y			Y					Y		Y		N							
3-4	N	Y			N	Y		N	Y				Y		Y				Y		Y			N							
3-5	N	Y			N		Y	N	Y				Y			Y								N							
3-6	N	Y			N		Y	N	Y				Y				Y	Y						N							
3-7	N		Y		N		Y	N	Y			Y								Y		Y		N							
3-8	N	Y			N		Y	N	Y				Y						Y		Y			N							
4-1	N			Y	N						Y			Y		Y					Y										
4-2	N			Y	N						Y			Y			Y	Y			Y										
4-3	N			Y	N						Y		Y							Y	Y		Y								
5-1	N				Y											Y					Y										
5-2	N				Y												Y	Y			Y										
5-3	N													N		Y					Y										
5-4	N													N			Y	Y			Y										
6-1	N		Y																						N	Y					
6-2	N		Y																				Y		N						
6-3	N	Y	N																			Y			N						