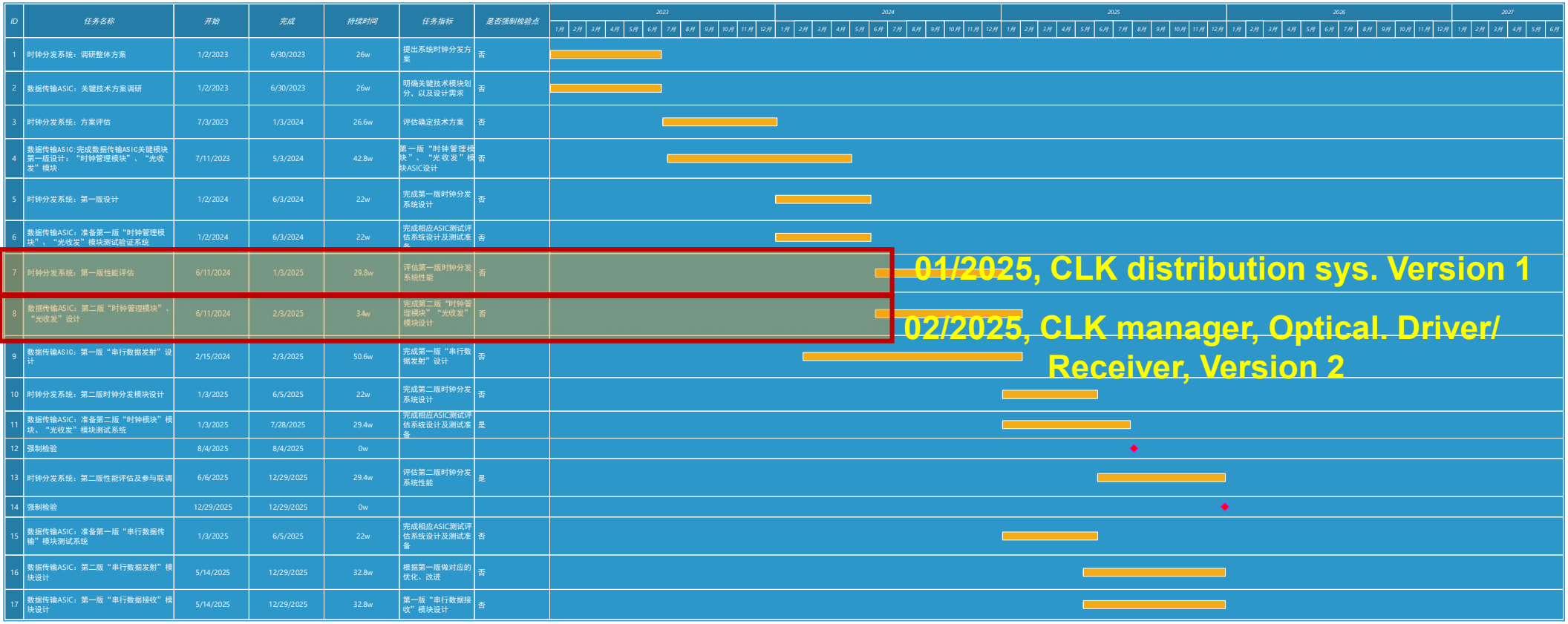
R&D Progress of the STCF CLock & Data Transmission System

Jinhong Wang, on behalf of the CLDT team

Nov. 20, 2024

I Progress Overview

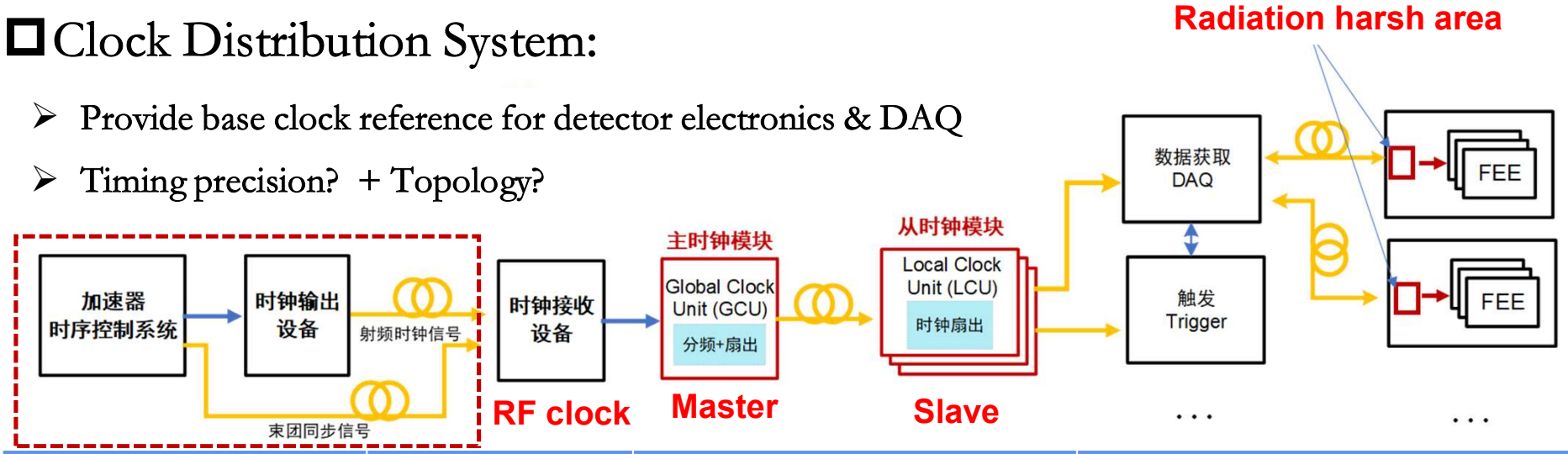
ID	任务名称	开始	完成	持续时间	任务指标	是否强制检验点
1	时钟分发系统：调研整体方案	1/2/2023	6/30/2023	26w	提出系统时钟分发方案	否
2	数据传输ASIC：关键技术方案调研	1/2/2023	6/30/2023	26w	明确关键技术模块划分，以及设计需求	否
3	时钟分发系统：方案评估	7/3/2023	1/3/2024	26.6w	评估确定技术方案	否
4	数据传输ASIC：完成数据传输ASIC关键模块第一版设计：“时钟管理模块”、“光收发”模块	7/11/2023	5/3/2024	42.8w	第一版“时钟管理模块”、“光收发”模块ASIC设计	否
5	时钟分发系统：第一版设计	1/2/2024	6/3/2024	22w	完成第一版时钟分发系统设计	否
6	数据传输ASIC：准备第一版“时钟管理模块”、“光收发”模块测试验证系统	1/2/2024	6/3/2024	22w	完成相应ASIC测试评估系统设计及测试准备	否
7	时钟分发系统：第一版性能评估	6/11/2024	1/3/2025	29.8w	评估第一版时钟分发系统性能	否
8	数据传输ASIC：第二版“时钟管理模块”、“光收发”设计	6/11/2024	2/3/2025	34w	完成第二版“时钟管理模块”“光收发”模块设计	否
9	数据传输ASIC：第一版“串行数据发射”设计	2/15/2024	2/3/2025	50.6w	完成第一版“串行数据发射”设计	否
10	时钟分发系统：第二版时钟分发模块设计	1/3/2025	6/5/2025	22w	完成第二版时钟分发系统设计	否
11	数据传输ASIC：准备第二版“时钟模块”模块、“光收发”模块测试系统	1/3/2025	7/28/2025	29.4w	完成相应ASIC测试评估系统设计及测试准备	是
12	强制检验	8/4/2025	8/4/2025	0w		
13	时钟分发系统：第二版性能评估及参与联调	6/6/2025	12/29/2025	29.4w	评估第二版时钟分发系统性能	是
14	强制检验	12/29/2025	12/29/2025	0w		
15	数据传输ASIC：准备第一版“串行数据传输”模块测试系统	1/3/2025	6/5/2025	22w	完成相应ASIC测试评估系统设计及测试准备	否
16	数据传输ASIC：第二版“串行数据发射”模块设计	5/14/2025	12/29/2025	32.8w	根据第一版做对应的优化、改进	否
17	数据传输ASIC：第一版“串行数据接收”模块设计	5/14/2025	12/29/2025	32.8w	第一版“串行数据接收”模块设计	否



II Design Introduction

Clock Distribution System:

- Provide base clock reference for detector electronics & DAQ
- Timing precision? + Topology?



Experiments	Scale	Timing Precision	Topology
BESIII	x100 m	~ 10 ps RMS	Master/Slave+fanout
CEE	x100 m	~ 5 ps RMS	Master/Slave+fanout
LHC/ATLAS	x1000 m	~ 7 ps RMS	Timing Encoding+fanout
STCF	**x100 m**	**~ 5 ps RMS**	Master/Slave+fanout

http://cicpi.ustc.edu.cn/indico/conferenceDisplay.py?confId=6373

II Design Introduction

Requirement on the overall clock timing precision: ~ 5 ps RMS

- Take the requirement from DTOF for an example:

Single-photon transit time spread: TTS

Time reconstruction uncertainty of the DTOF det.

$$\sigma_{tot}^2 \approx \sigma_{trk}^2 + \sigma_{T_0}^2 + \left(\frac{\sigma_{elec}}{\sqrt{N_{PE}}}\right)^2 + \left(\frac{\sigma_{TTS}}{\sqrt{N_{PE}}}\right)^2 + \left(\frac{\sigma_{det}}{\sqrt{N_{PE}}}\right)^2$$

Track reconstruction: ~10 ps

Event reference: ~40 ps

- N_{PE} = 17, **three effects contribution ~20 ps**
- $\propto \frac{1}{N_{PE}}$

DTOF Electronics: 20-30 ps RMS → 10 ps RMS for clock is adequate

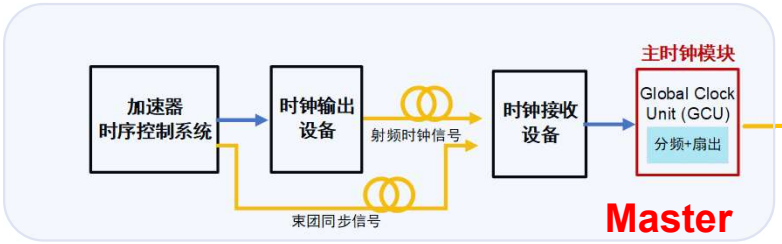
Target: ~ 5 ps RMS, → more contingency

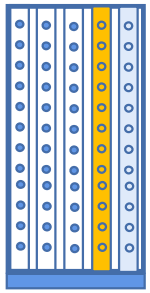
II Design Introduction

Topology: "STAR" distribution, Master/Slave + fanout

Synchronized with the beam control of the collider

- **~ 500 MHz → 40 MHz**

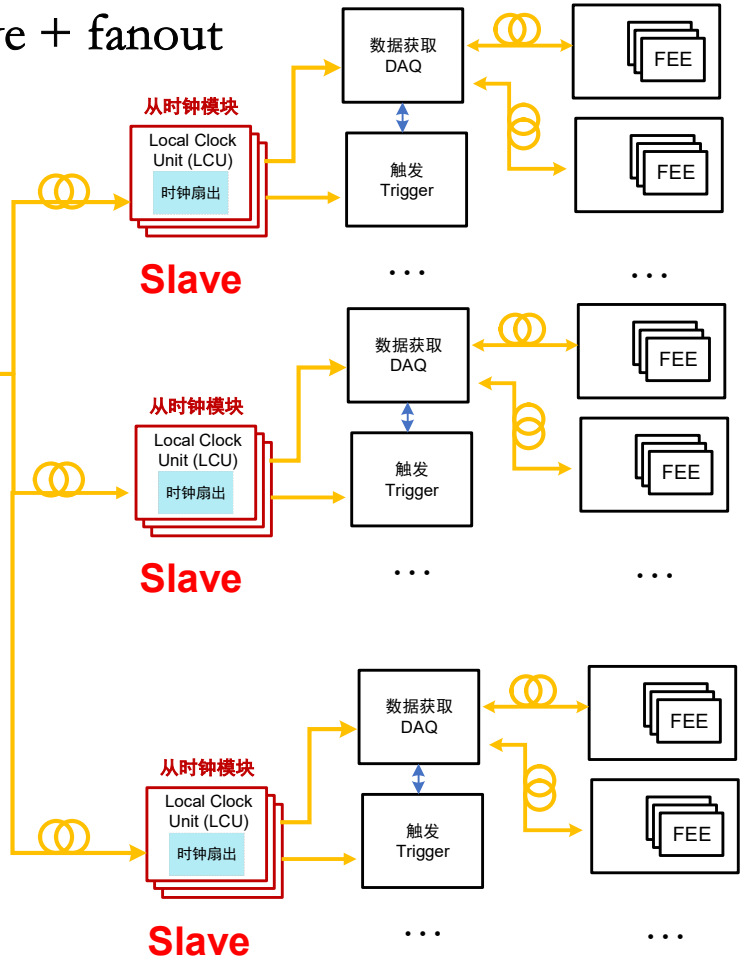




Fanout
(optical)

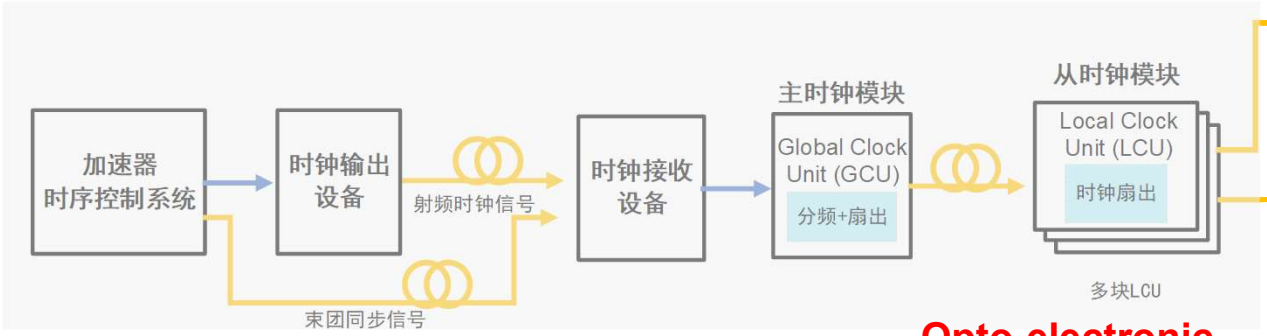
Standard crate

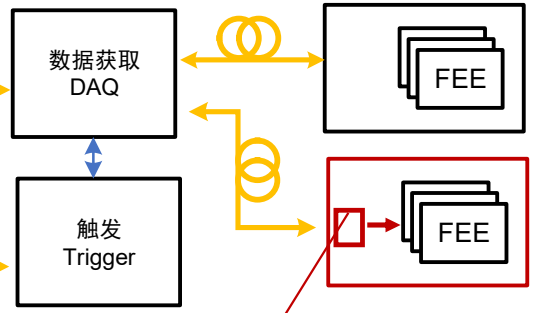
~100 m fiber!



II Design Introduction

☐ High-speed Data Transmission: ~ 5 Gbps (uplink) + Rad. harden



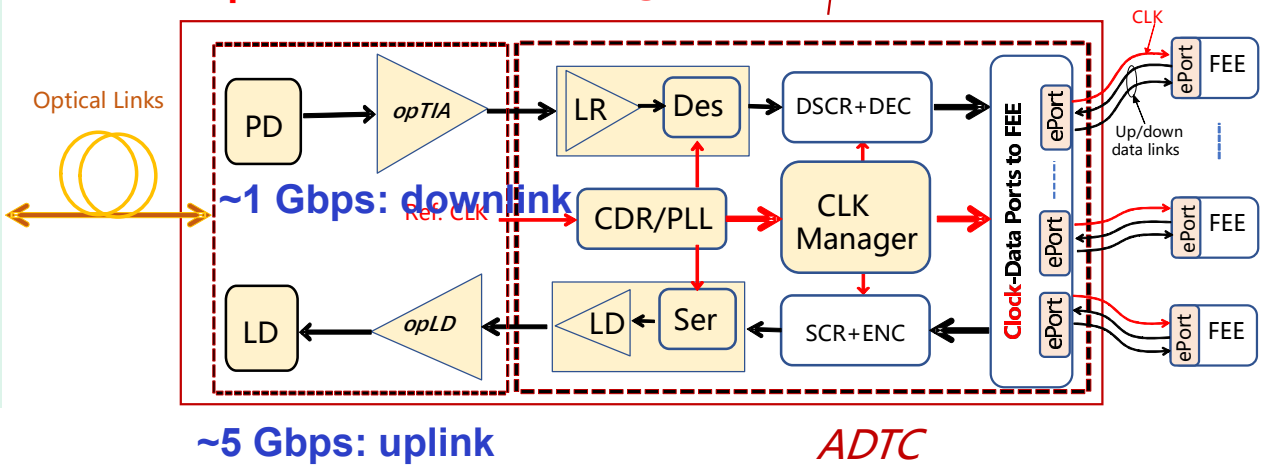


Opto-electronic

High-speed serial Transmission

Four key blocks:

- → **Clock manager**
  - CDR, PLL, DLL, phase-shifter, noise /spur suppression etc.
- → **Serializer- uplink**
  - SCR+ENC, SER, LD, opLD
- → **Deserializer - downlink**
  - PD, opTIA, DES, DSCR, DEC
- → **Service unit: data interface (ePort), slow control, function monitoring…**



II Design Introduction

☐ Line rate on the up/down links: ~ 5 Gbps-uplink, ~ 1 Gbps-downlink

- STCF data rate estimation from each detector

Component	Num. of channels	Readout time	Event size (B)	Total (B/s)	Avg. rate per **1000** chnl (Gbps)
ITK (Silicon)	50M	200 ns	3290	1.32G	⟷ 211 Kbps
ITK (μRWELL)	11380	400 ns	11753	4.69G	⟷ 3.3 Gbps
MDC	11520	1 μs	15300	6.12G	⟷ 4.25 Gbps
PID (RICH)	698880	200 ns	1835	734M	⟷ 8.4 Mbps
PID (DTOF)	6912	200 ns	1440	576M	⟷ 667 Mbps
EMC	8670	1 μs	15000	6.00G	⟷ 5.54 Gbps
MUD	40840	300 ns	373	149M	⟷ 29.2 Mbps
Total	20.8M	–	45.7k	18.3G	**~5 Gbps suffices for uplink**

- Downlink is for: configuration, slow-control ← very limited data rate within limited time frame

~1 Gbps is adequate for the downlink

- Line rates of the CERN GBT chips:
  - → GBT: uplink 4.8 Gbps, downlink 4.8 Gbps
  - → lpGBT: uplink 10.24 Gbps (max), downlink 2.56 Gbps (max)

II Design Introduction

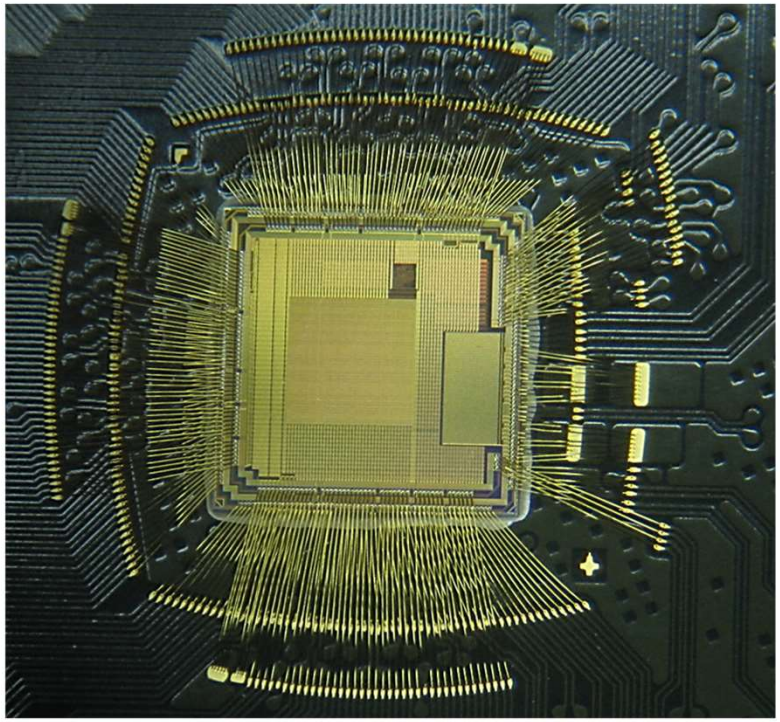
Radiation tolerance for the ASICs

Detector	Highest TID value per pixel (Gy/y)	Highest NIEL damage per pixel (1 MeV neutron/cm^2/y)	Highest count rate per channel (Hz/channel)
Silicon-inner-1	3488.3	1.75×10^{11}	2.61×10^{2}
Silicon-inner-2	320.4	3.72×10^{10}	2.74×10^{1}
Silicon-inner-3	149.9	2.68×10^{10}	8.51×10^{0}
μRWELL-inner-1	117.8	1.12×10^{10}	3.35×10^{5}
μRWELL-inner-2	61.8	1.46×10^{10}	1.63×10^{5}
μRWELL-inner-3	38.6	5.67×10^{10}	1.61×10^{5}
MDC	60.5	4.87×10^{10}	4.00×10^{5}
PID-Barrel (RICH)	4.25	1.07×10^{10}	1.71×10^{4}
PID-Endcap (RICH)	44.3	1.98×10^{10}	1.20×10^{5}
EMC-Barrel	21.1	1.76×10^{10}	9.00×10^{5}
EMC-Endcap	45.1	1.88×10^{10}	1.50×10^{6}
MUD-Barrel-RPC	0.093	3.74×10^{11}	1.54×10^{1}
MUD-Barrel-Scintillator	0.047	4.88×10^{11}	2.15×10^{1}
MUD-Endcap-RPC	0.37	1.22×10^{10}	2.72×10^{2}
MUD-Endcap-Scintillator	0.24	2.79×10^{12}	9.01×10^{2}

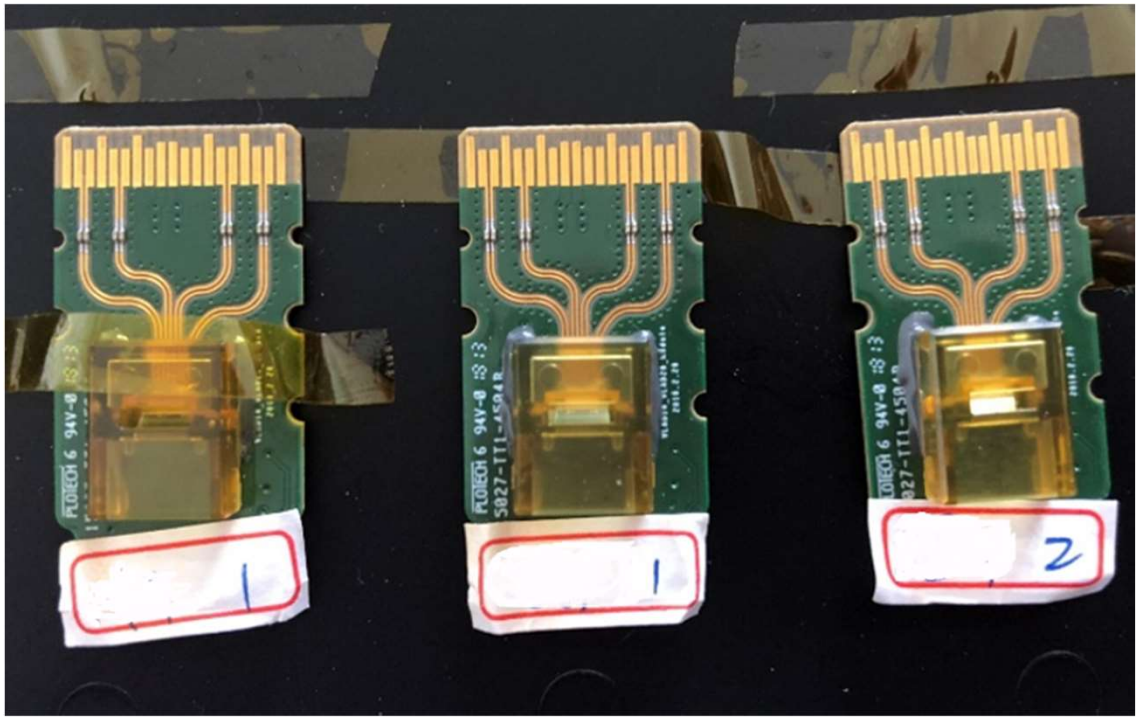
- **TID is not significant: ~ 3.5 Mrad for 10 years**

II Design Introduction

- IC tech. node： 130nm CMOS → 65/55 nm CMOS
  - Higher integration, lower power, and longer life-cycle



~ 5 Gbps serializer in 130nm CMOS

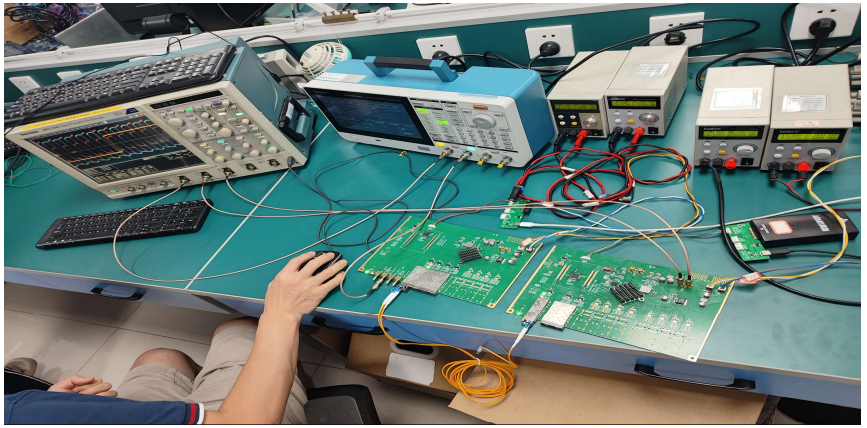


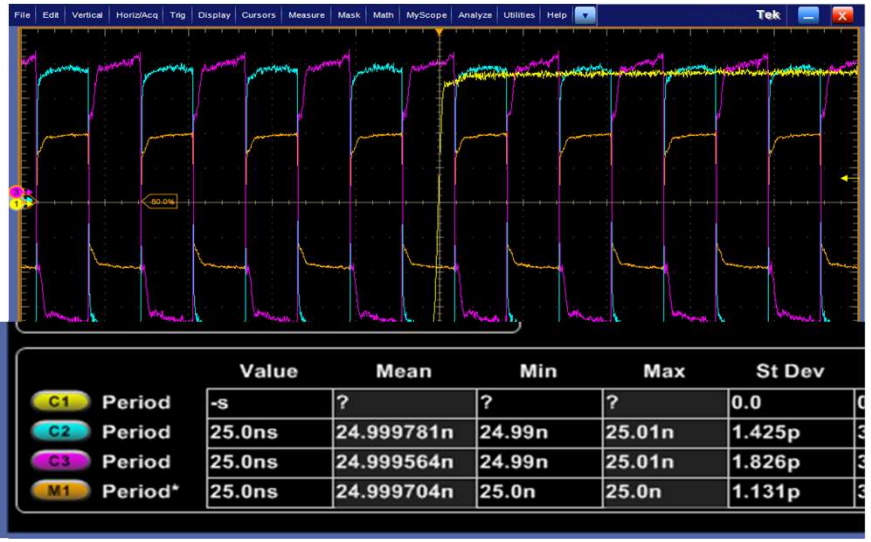
Custom opto-modules in 55nm CMOS

III Progress: CLK distribution system

Evaluation of version 1 performance

- setup: Tektronix AFG31000
  Tektronix DPO7354C @ HUST
  Color chip 10G SFP
  SR Optical Transceiver
- A complete signal chain evaluation with ~ 2 m fiber.





Period Jitter < 2 ps

C1	2MHz for synchronization
C2	40 MHz output P
C3	40 MHz output N
M1	Difference P-N

III Progress: CLK distribution system

Further evaluation @ USTC with HUST

时钟分发板的测试报告

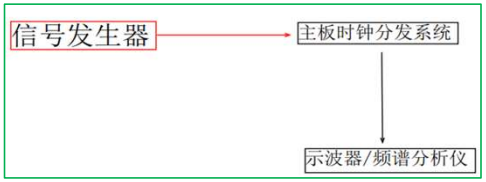
陈鑫 武一鸣 王进红 彭亮

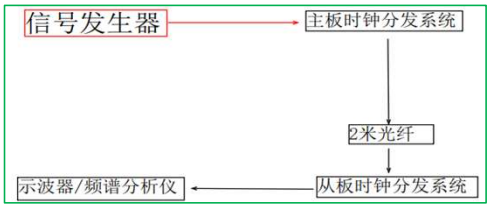
Final Report

中国科技大学

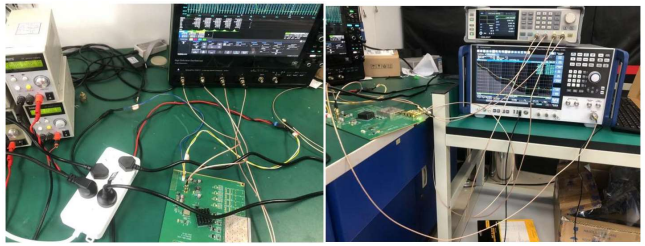
湖南科技大学

目录



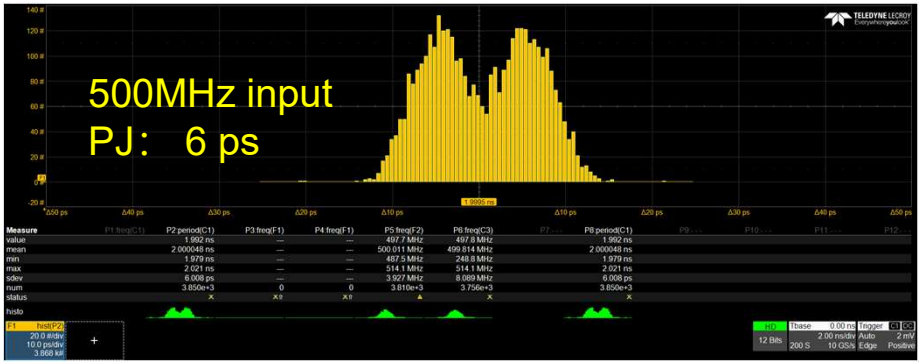


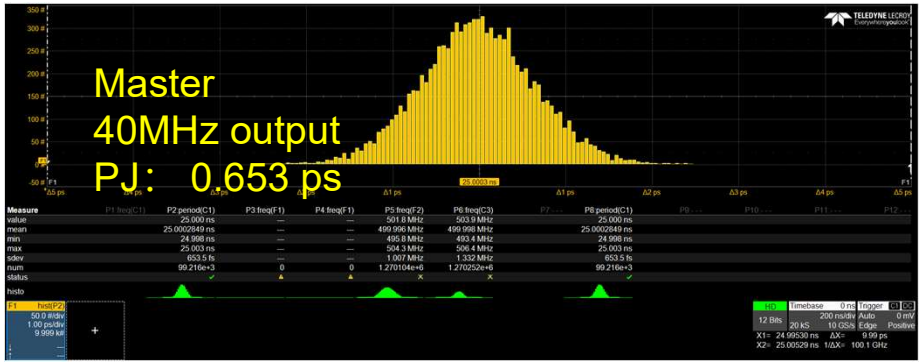
Evaluation setup



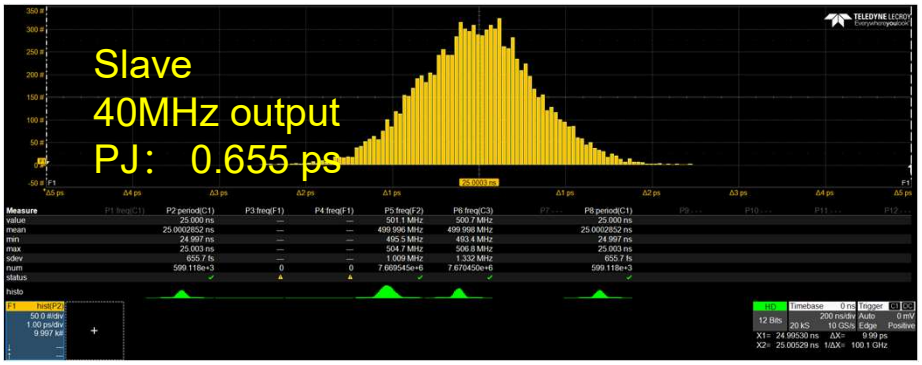
III Progress: CLK distribution system

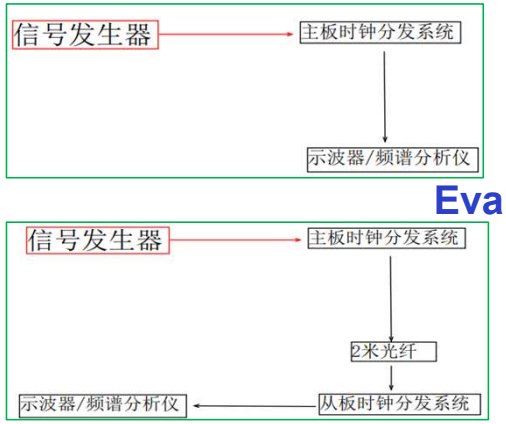
- Further evaluation @ USTC with HUST





Jitter cleaners are the key!

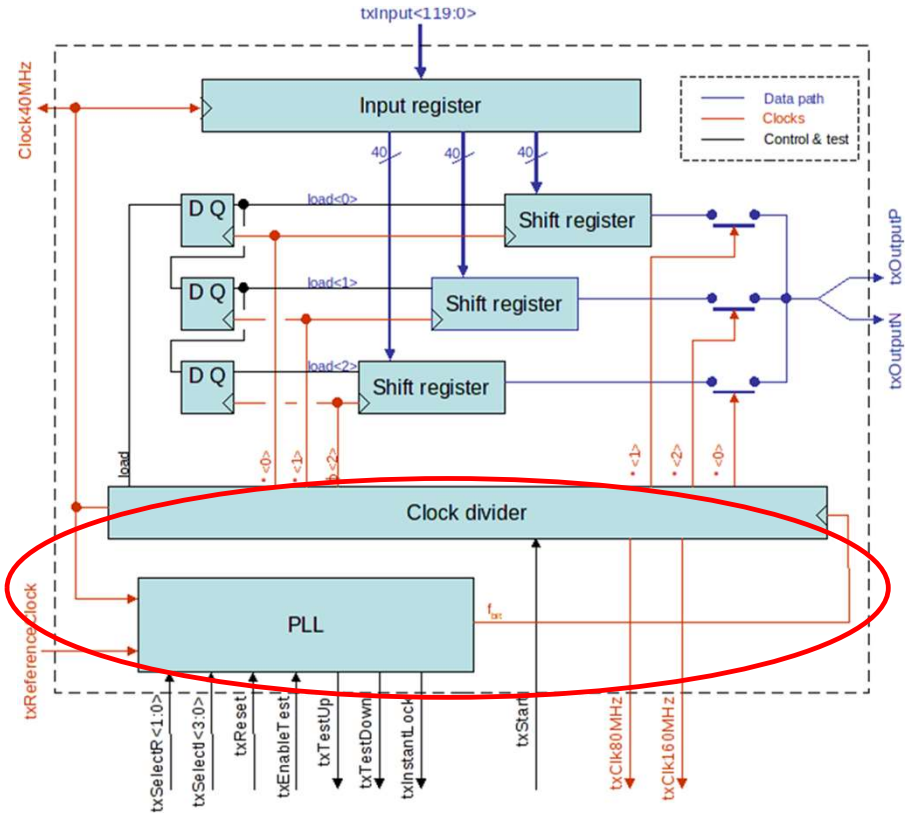




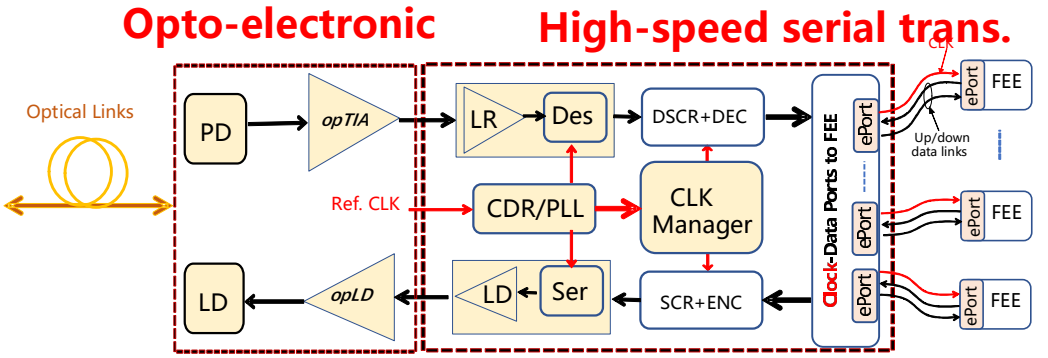
Evaluation setup

III Progress: High-speed data transmission

➢ Prototype for the key functional blocks



The GBT SER.



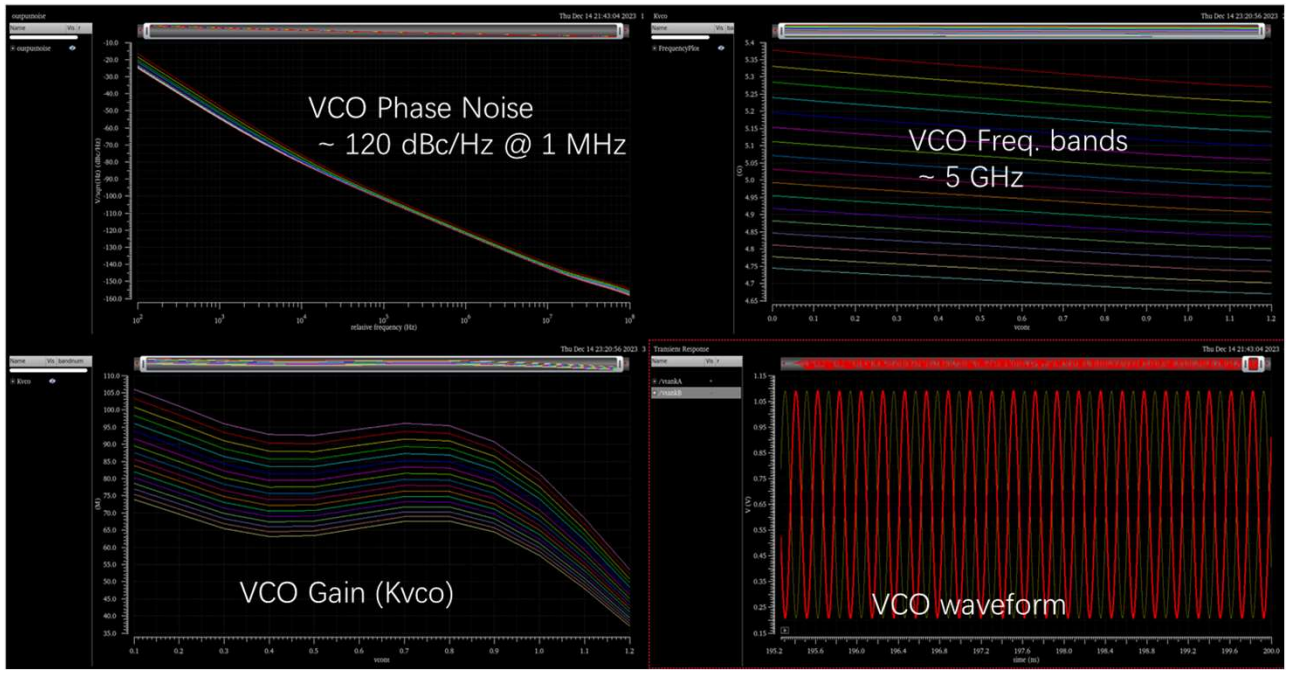
- **Clock manager**
  - → ~5 GHz PLL single phase or ~2.5 GHz with dual phase
  - → LC VCO
- **Serial transmission: uplink**
  - → ~5 Gbps, 2/1 MUX or 3/1 MUX
- **Serial transmission: downlink**
  - → ~1 Gbps
  - → Possible clock conditioner

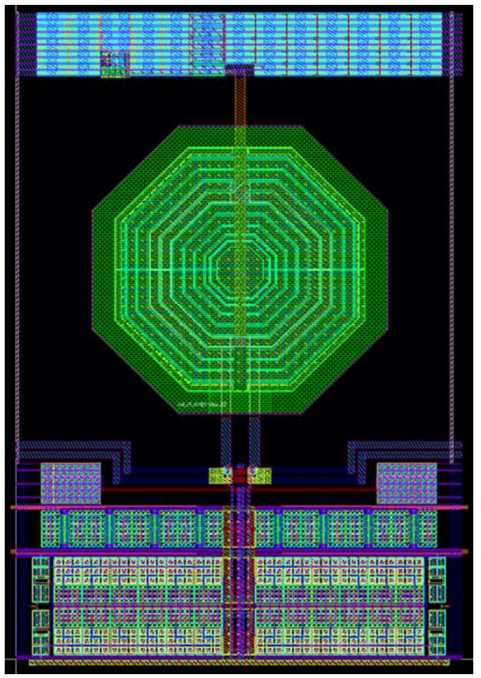
- E-Links
  - → SLVS/LVDS IO
- CML IO

- Enc. & Dcode.
  - → SCR +ENC
  - → DSCR +ENC
- Test utilities
  - → PRBS generator

III Progress: High-speed data transmission

➢ Clock manager： VCO+ FBDiv

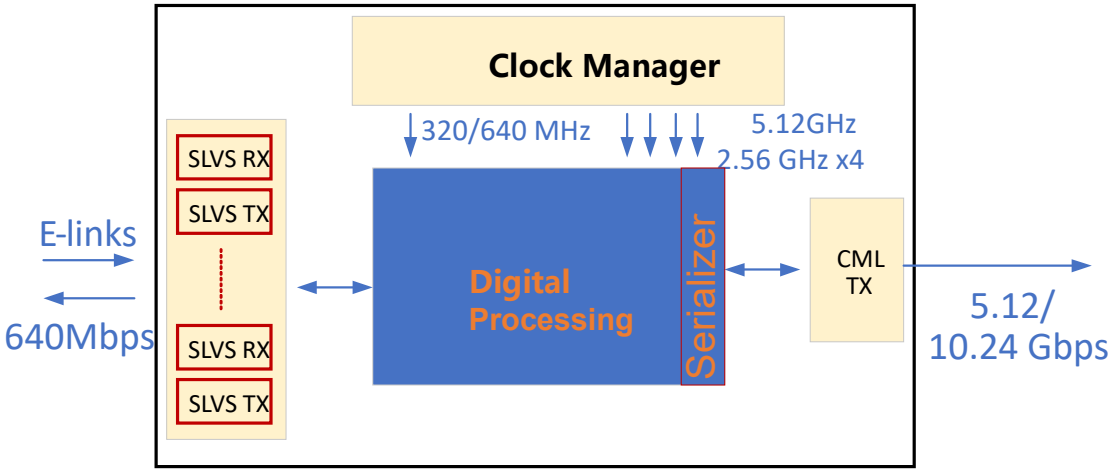


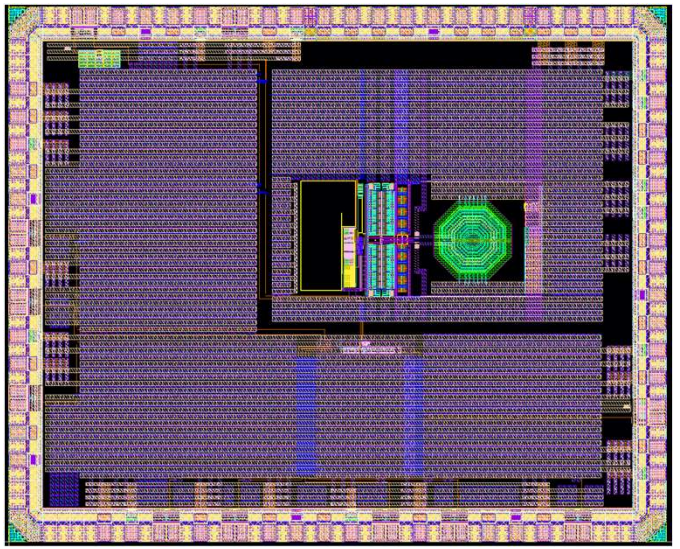


- LC-VCO ， central frequency ~ 5 GHz (4.6 -5.3 GHz)
  - → With four phases of 2.56 GHz outputs: 0/90/180/270
  - → Multiple frequency available: 1.28GHz/640MHz/320MHz/160MHz/80MHz

III Progress: High-speed data transmission

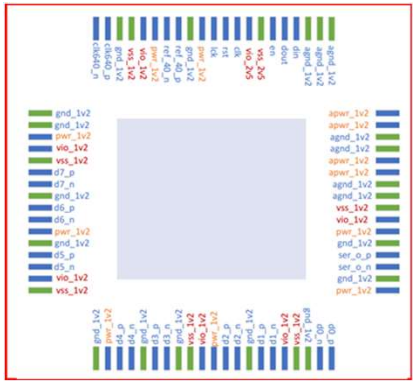
➢ Uplink blocks (MPW in Oct. 2024)





- Clock manager:
  - → four phases of 2.56 GHz (0/90/180/270)
  - → Available also 320/640MHz/1.28 GHz
- *Digital Processing:*
  - →*data flow control, frame builder etc.*
- Serializer:
  - → 8/1 from 640 Mbps → 5.12 Gbps

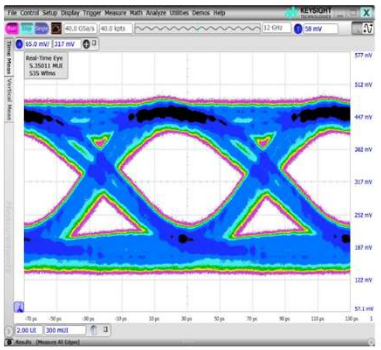
- E-links: for FEE
  - → SLVS TX/RX
  - → 160/320/640Mbps
  - → 1.28 Gbps
- CML: for DAQ
  - → 5-10 Gbps

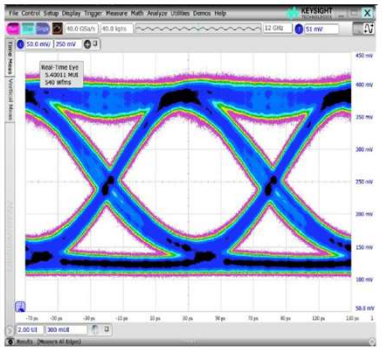


- Package + Evaluation brd under design

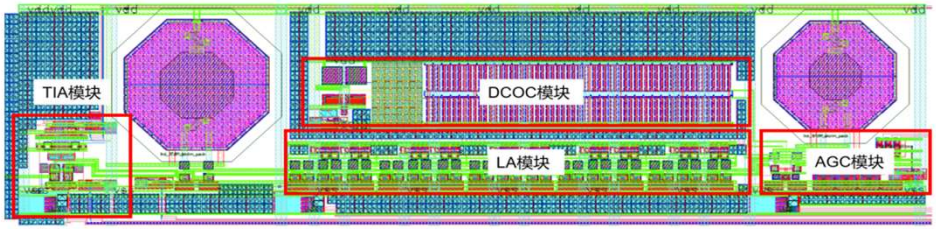
III Progress: High-speed data transmission

- Custom TIA & LD from CCNU
  - All in 55nm CMOS
  - Uplink: Tx supports 5 Gbps up to 10 Gbps
  - Downlink: Rx operates up to 5 Gbps

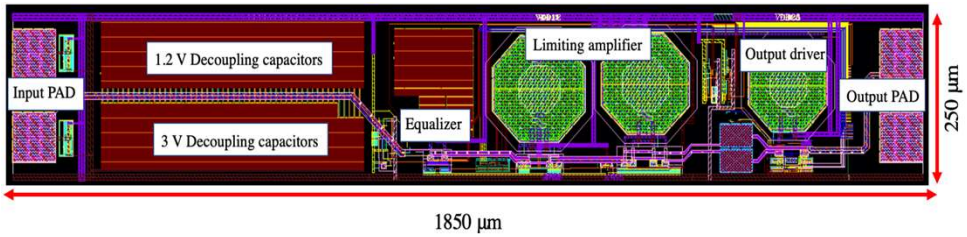


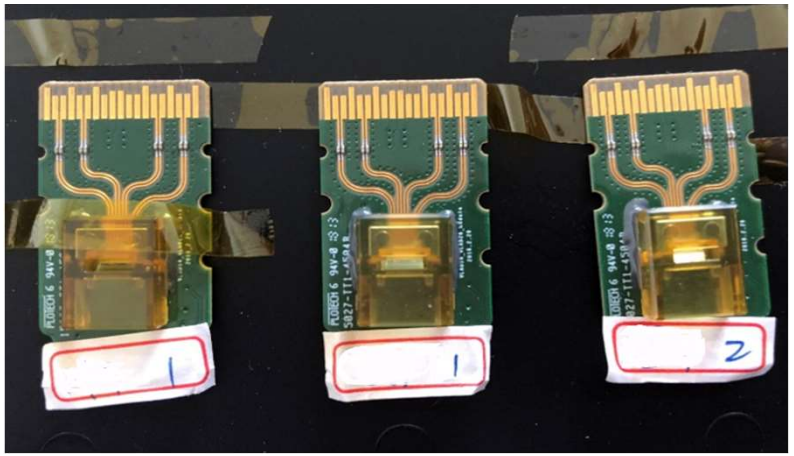


TIA



Laser Driver





Custom opto-modules in 55nm CMOS

IV Summary & Outlook

- Summary
  - Clock Distribution System V1 done, timing performance meets requirements.
  - 1st prototype of the uplink key blocks submitted in Oct. 2024.

- Outlook:
  - Clock Distribution System V2 in consideration, for preparation in joint tests.
  - Packaging and evaluation boards are in preparation for the ASIC prototypes.