中国科学技术大学
University of Science and Technology of China

Development of TDC ASIC for the STCF Endcap PID Detector

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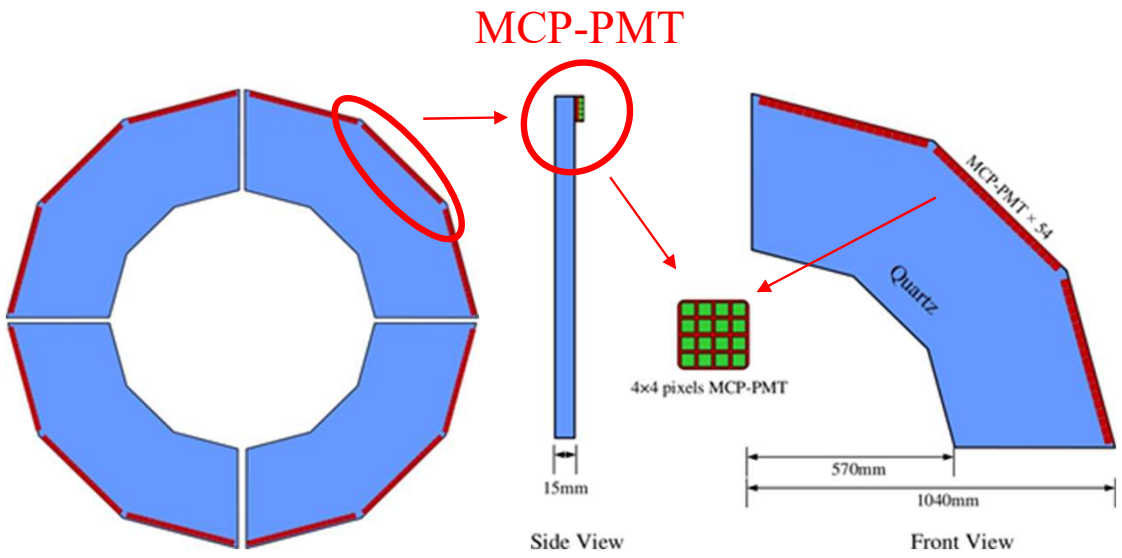
#01

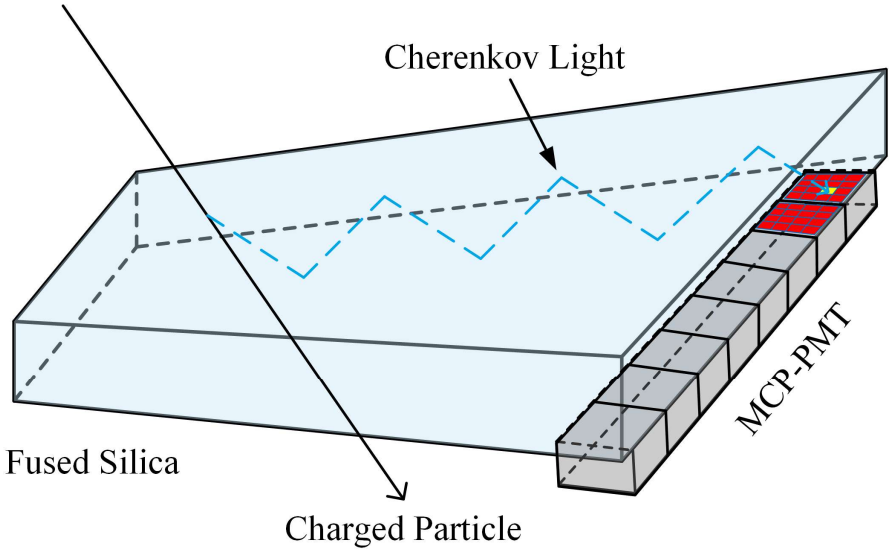
DTOF Readout Electronics

Dirc-like TOF Detector for Endcap PID at STCF

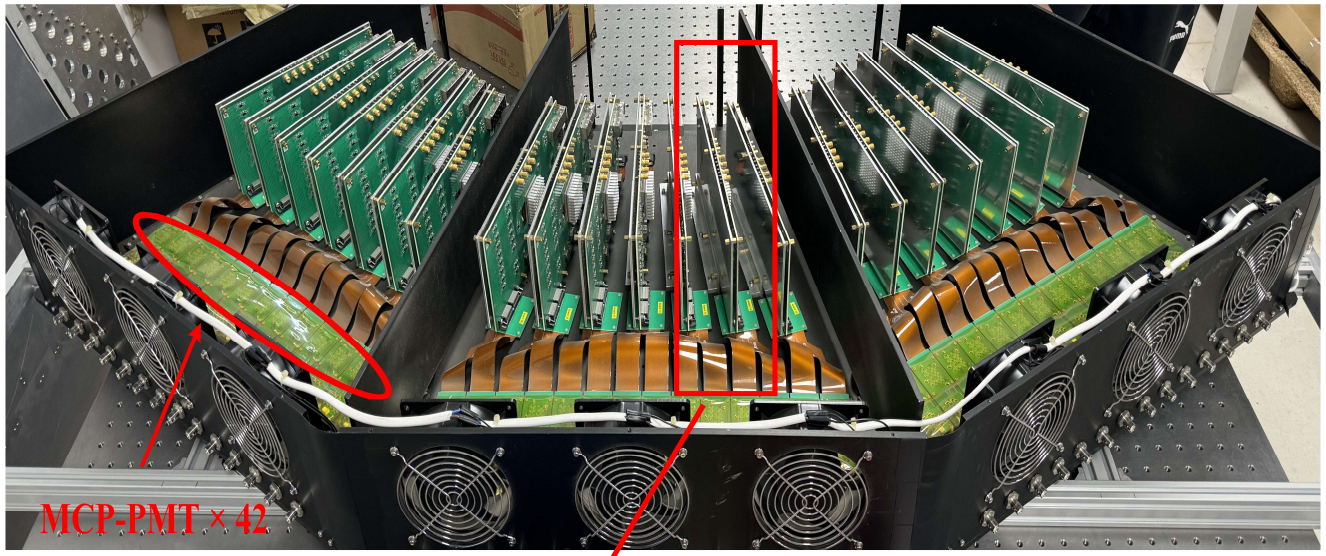
Dirc-like time-of-flight (DTOF) detector: the endcap particle identification (PID) device at STCF.

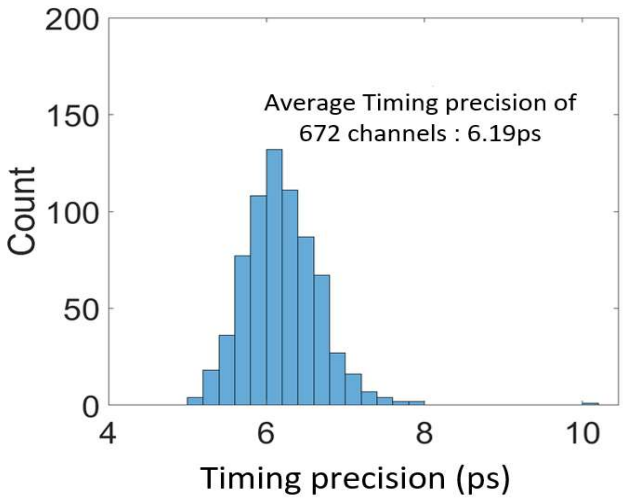
- Using the detection of internally reflected Cherenkov light (DIRC) to measure the time of flight (TOF) and separate different particles
- Expectation: achieving a 4σ π/K separation at 2 GeV/c momentum
- Requirements: intrinsic time resolution of the DTOF: $\sigma_{DTOF} < 30\ ps$



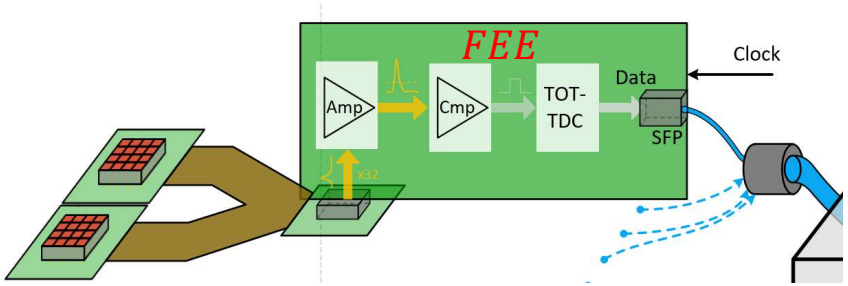


672-channel electronics for DTOF prototype





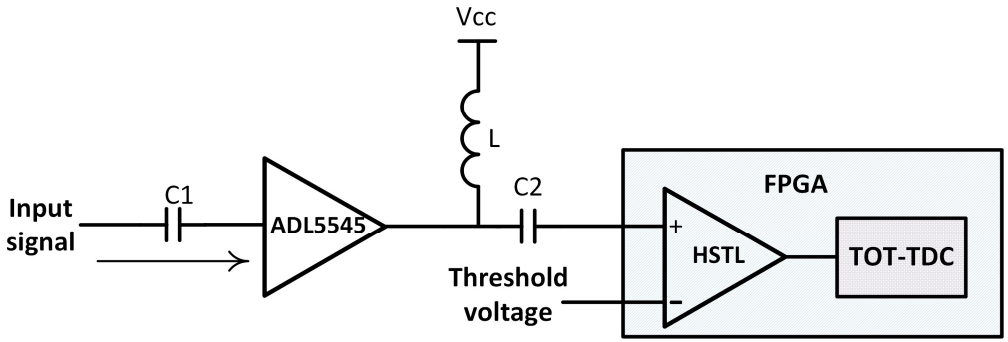
- Inherent electronics timing precision: < 10 ps
- Fully meet the timing requirement



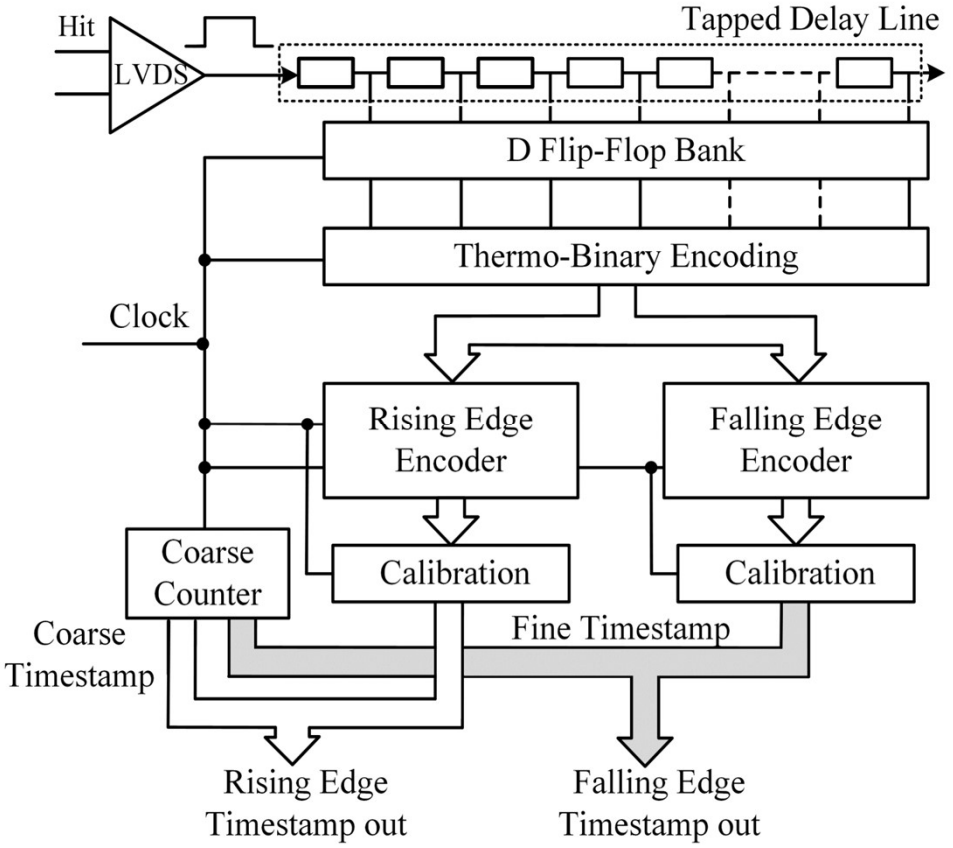
- Leading edge discrimination (LED)
- LED correction with time-over-threshold (TOT)
- FPGA-based time-to-digital converter (TDC)

672-channel electronics for DTOF prototype

- LED circuit based on discrete devices
  - Broadband RF amplifier
  - Using FPGA HSTL IO for discrimination
- FPGA-based TDL-TDC
  - Tapped delay line constructed by CARRY chain
  - Time resolution: ~ 7 ps
  - Time interval measurement precision: ~ 6 ps

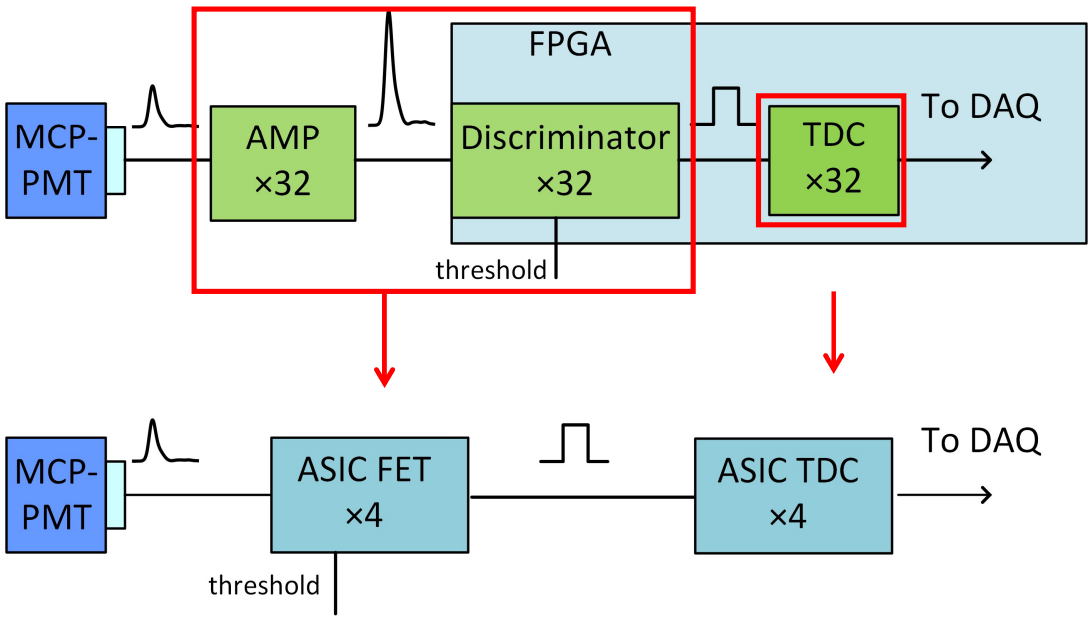


LED circuit with discrete devices



FPGA-based TDL-TDC

From Discrete Devices to ASIC



(At least 8 channels within each FET or TDC chip)

- The prototype achievements
  - Timing resolution (electronics): < 10 ps
  - Channel number: 627
  - Power comsumption: ~380 mW/ch
  - Demonstrate the feasibility
- Challenges to integrate final ~7k channels
  - High power consumption of both the RF AMP and the TDC (cooling)
  - Low integration with discrete devices (space)
  - Lack of customization (radiation hardness)
- Step to ASIC
  - Front-end timing (FET) ASIC
  - TDC ASIC
  - ≥ 8 channels
  - Timing resolution (electronics): < 30 ps
  - Power consumption: < 150 mW/ch

#02

ASIC TDC for DTOF Detector

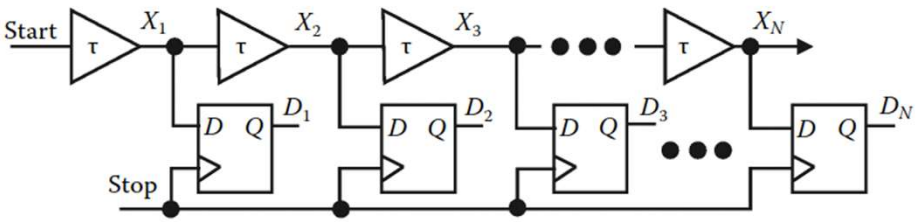
DTOF Requirements on TDC ASIC

- Timing Precision:
  - RMS precision (single channel) < 20 ps
  - Better precision is preferred, giving margin to system design
- Power: < 30 mW/ch
- Integration: ≥ 8 channels (TOT) on one chip
- Sample rate:
  - At least 5 MS/s (< 200 ns conversion time)
  - Higher rate means better efficiency
- TOT measurement:
  - For LED timing correction
- Possibility to be integrated with FET ASIC on one chip
- 130 nm CMOS

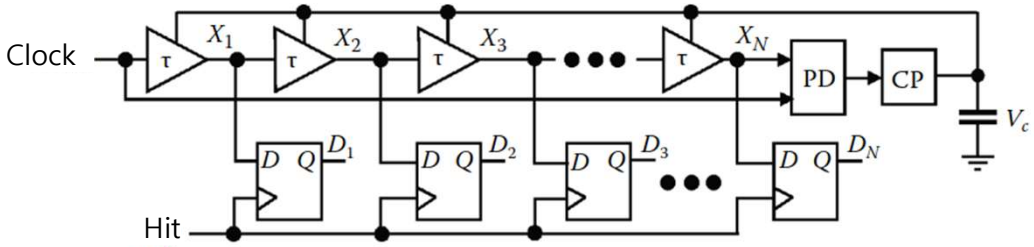
Typical TDC Implementations in ASIC

Simple One-step TDC:

- Tapped delay line (TDL) TDC



- Multiphase clock TDC



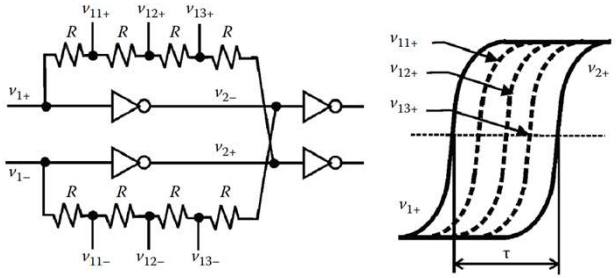
- **Considerations:**
  - Simple circuits and structures
  - Beginner friendly
  - Their resolution is limited by the minimum gate delay, which strongly depends on the technology node.
  - High resolution needs advanced technologies.

    → High R&D costs

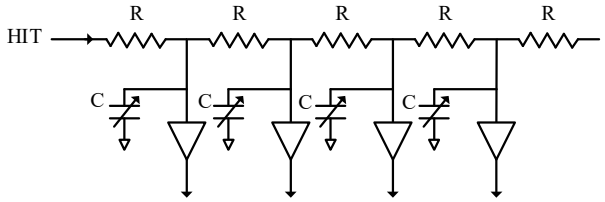
Pursuing Sub-gate Delay Resolution

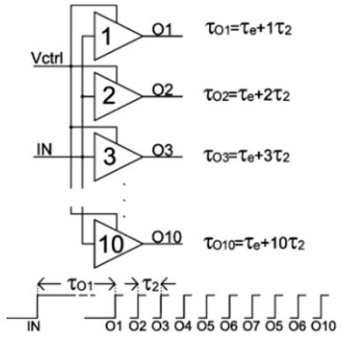
Interpolation:

- Local passive interpolation: create intermediate signal transitions using resistor chain



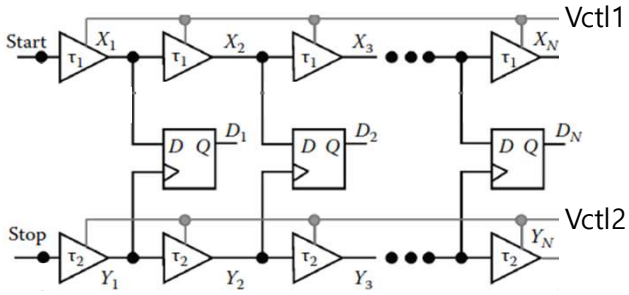
- Parallel interpolation: sampling in parallel at time intervals with sub-gate delay





- For our first ASIC attempt, a simpler structure and robustness are preferred.

Vernier TDC: simple Vernier structure has the disadvantage of long conversion time and limited measurement range.



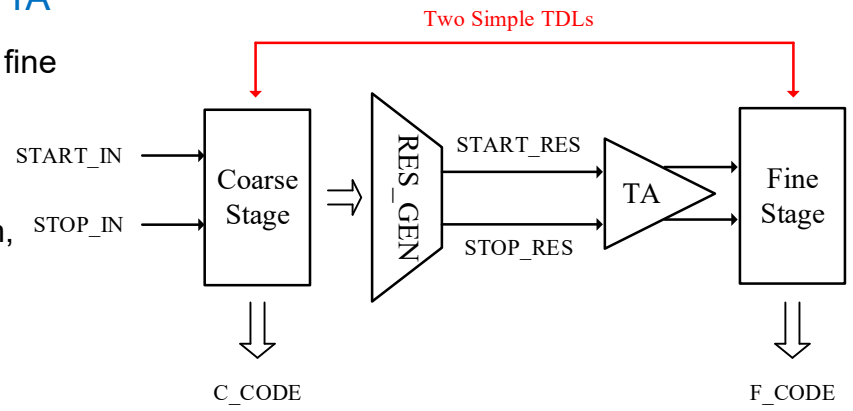
Two-step TDC: coarse-fine structure

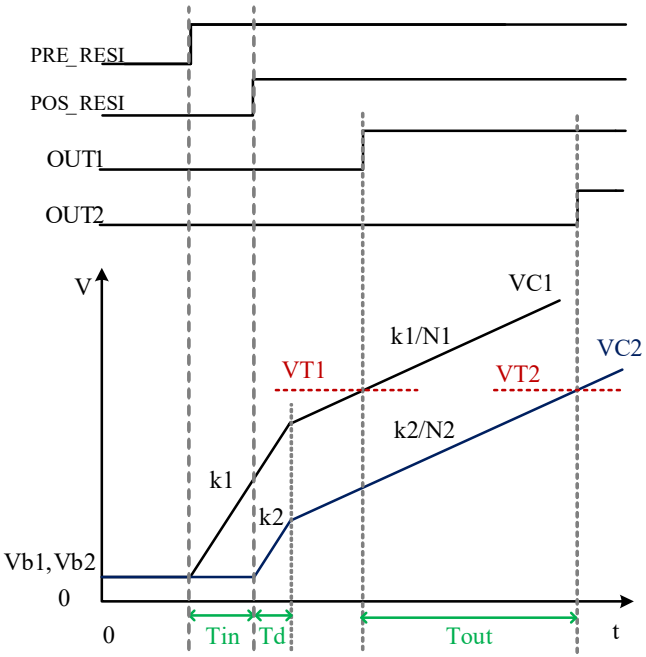
- Two simple stages are cascaded ✓
  - Moderate measurement range, conversion time, power, area
  - Significant resolution improvement
  - Low power
- Vernier for the fine stage: robust control of delay difference
- Time amplification (TA) between coarse and fine stages: one simple TDC can be reused in two stages

Two Designs Are Studied and Tried Out

1. Two-step TDL-TDC with a Dual-slope TA

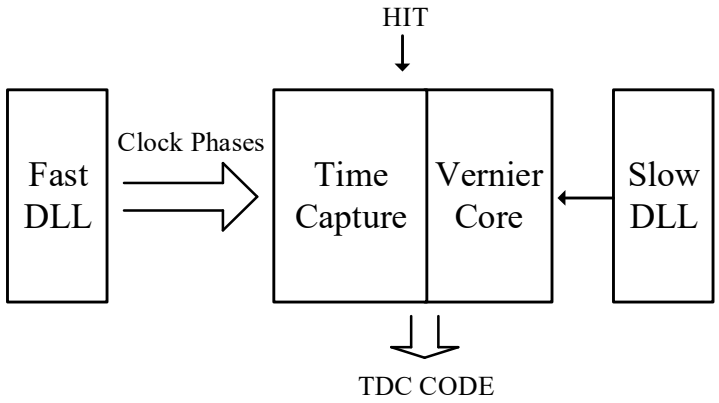
- Two simple TDLs used as coarse and fine stages
- Fast residue extraction
- Dual-slope TA: high linearity, high gain, offset adjustable
- Low-power, startup-free DLL





2. Multiphase clock Vernier hybrid TDC

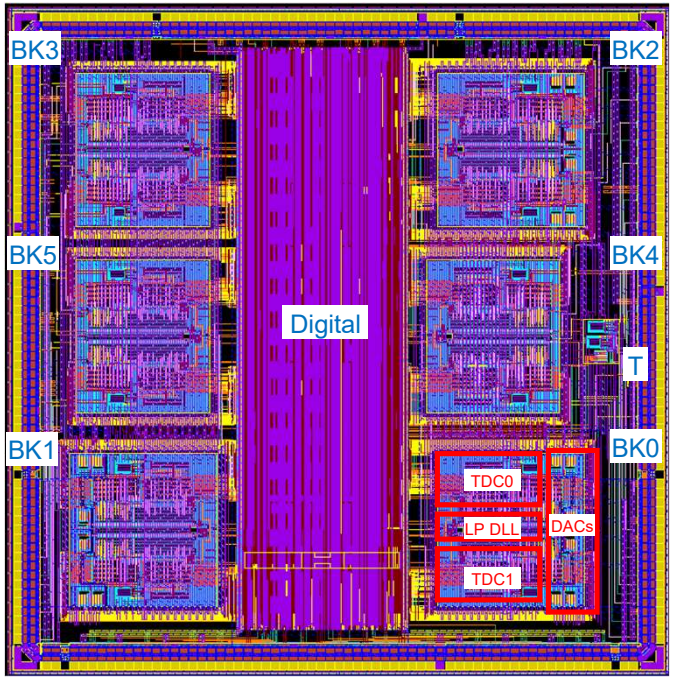
- Fast DLL generates multiple clock phases
- Slow DLL controlled Vernier core
- Time capture is driven by the input HIT
- Optional low power mode



Progress

➢ Dual-slope TA-TDC

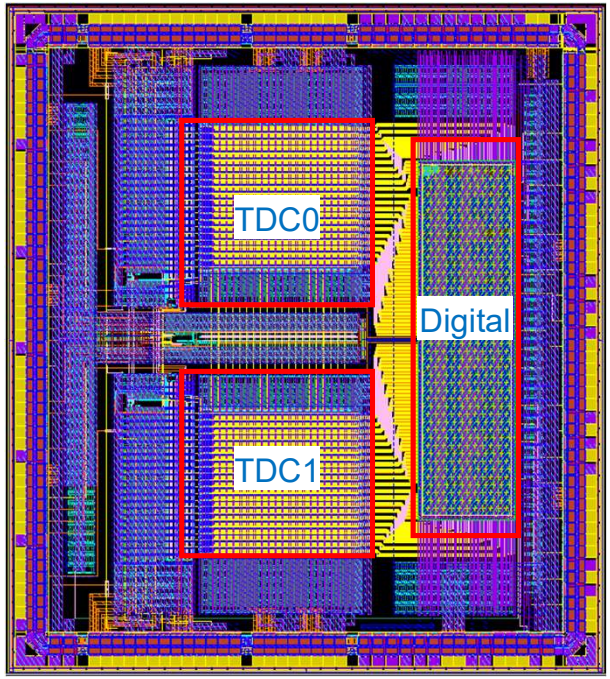
- First version prototype has been taped out in March 2024
- Evaluation board completed
- COB packaged
- Preliminary test results available



The following section will only show preliminary test results of the **Dual-slope TA-TDC**.

➢ Multiphase clock Vernier hybrid TDC

- First version prototype has been taped out in July 2024
- Evaluation board design undergoing
- QFN package undergoing
- To be evaluated soon

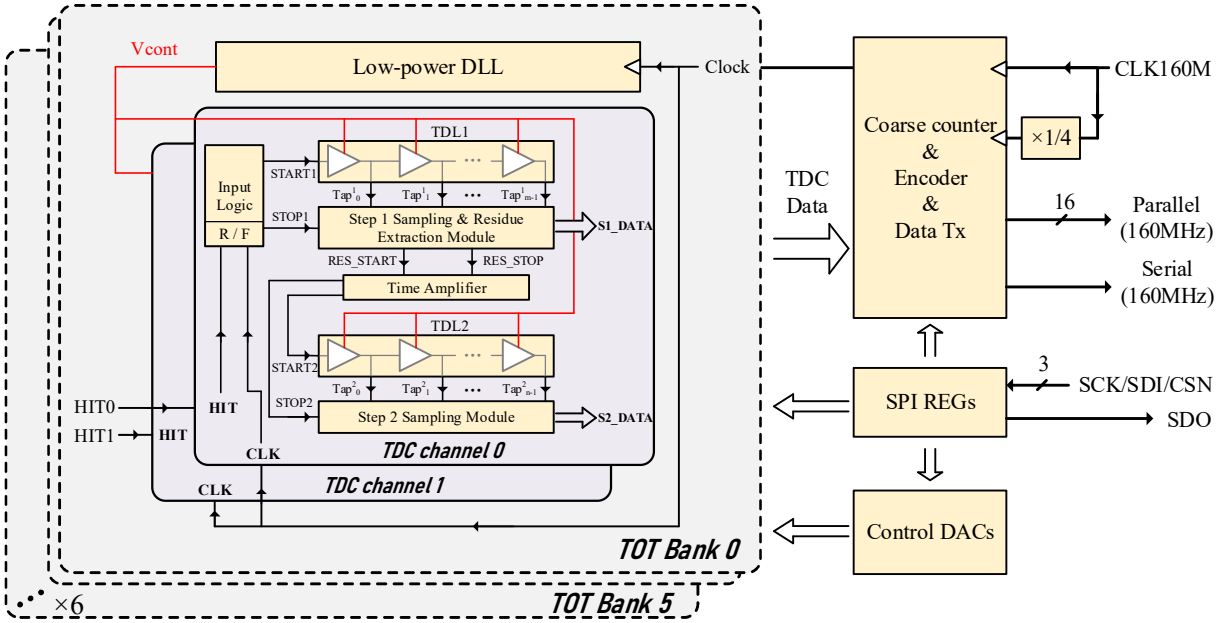


#03

Test Results

—— Dual-slope TA-TDC

TA-TDC Design Overview



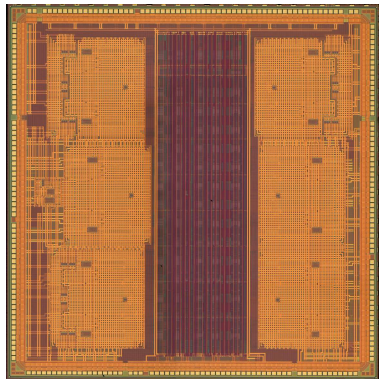
TOT Bank	Comment	DAC Power
0	Combined Input + Built-in DAC + TA_B	Individual
1	Separate Inputs + Built-in DAC + TA_B	Individual
2	Separate Inputs + Built-in DAC + TA_B	From TDC Power
3	Separate Inputs + External DAC + TA_A	--
4	Combined Input + External DAC + TA_B	--
5	Separate Inputs + External DAC + TA_B	--
T	Test DAC, TA_A, and TA_B	Individual

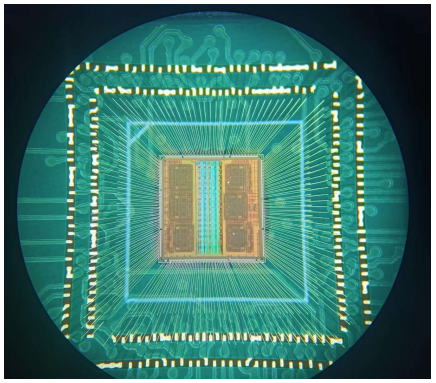
- First prototype for silicon validation
- 6 TOT banks (12 TDC channels): designed different in part of unit circuits to validate our understanding of the circuits

- LSB = 8.7 ps
- Conversion time < 50 ns
- Low power consumption
  - TDC core < 0.5 mW/ch
  - Digital core < 1 mW/ch

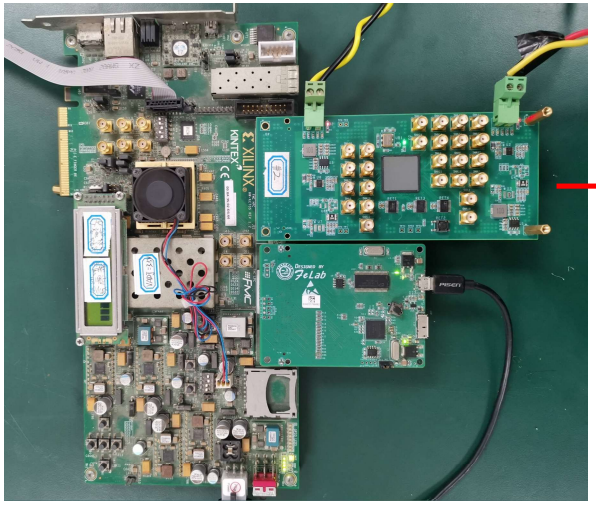
Evaluation Setup

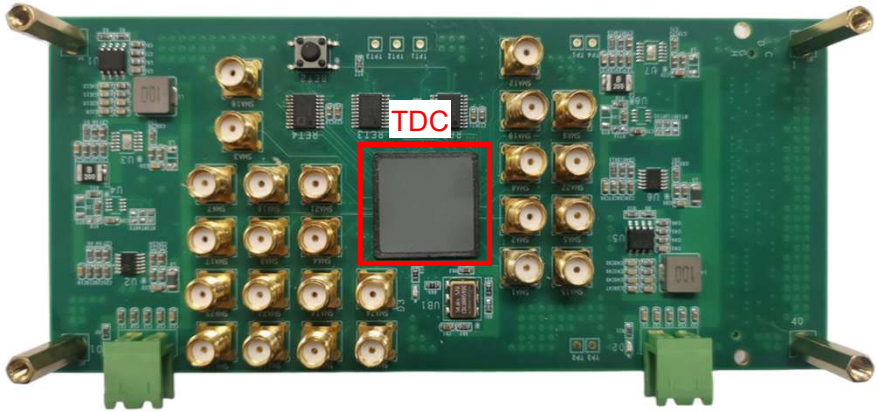
- Tests undergoing
  - All functions works correctly.
  - Some preliminary results available





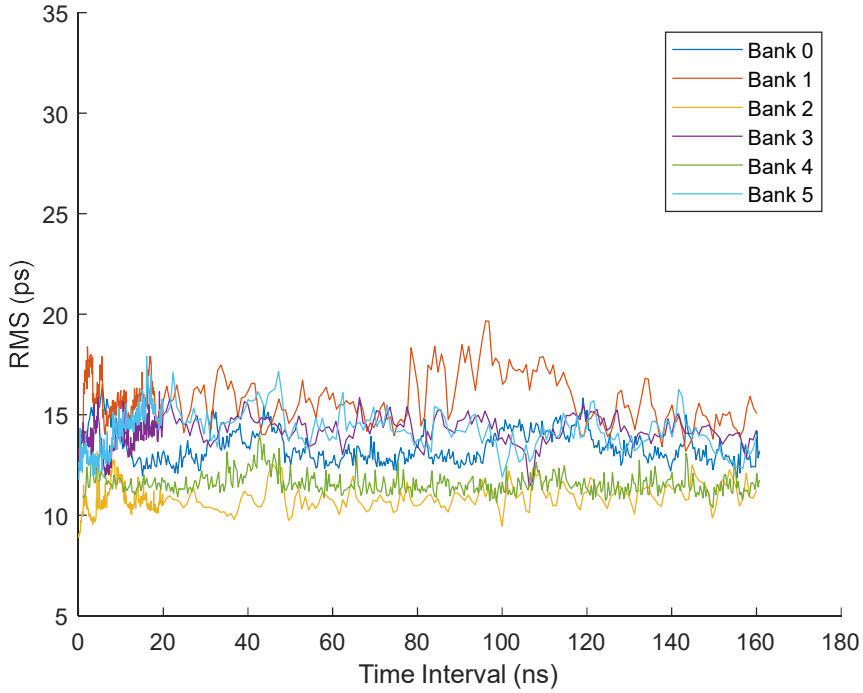
- Evaluation setup:





Precision

- INL correction adopted
- The average RMS precision of all TDC channels are below 11.2 ps (15.8 ps /$\sqrt{2}$)
  - Timing performance variations between channels are observed
- Fulfill the timing resolution requirement of DTOF detector (< 20 ps).



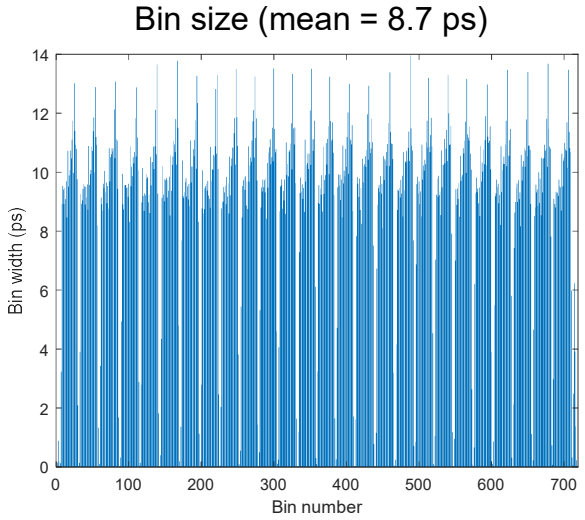
RMS precision of TDC banks with respect to measured time interval

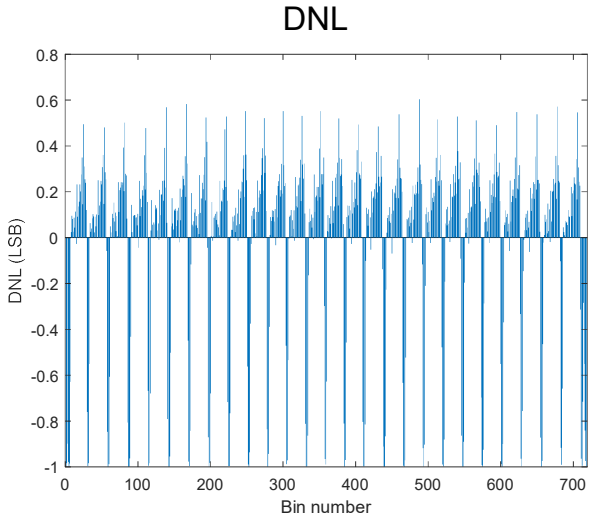
TOT Bank	Time Interval RMS Precision
0	13.4 ps
1	15.8 ps
2	10.8 ps
3	14.1 ps
4	11.6 ps
5	14.2 ps

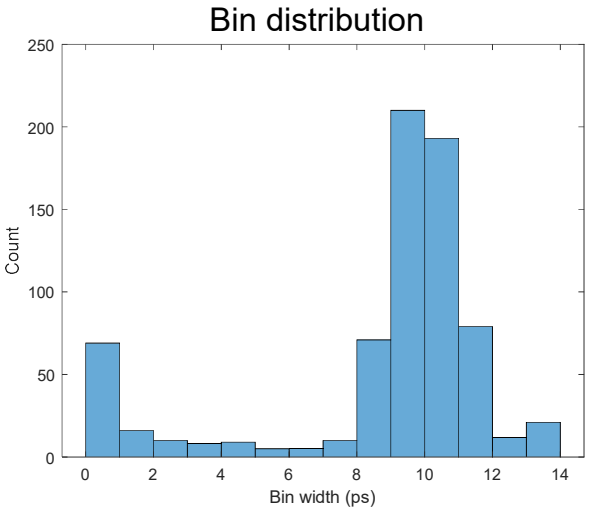
Average RMS precision of all TDC banks

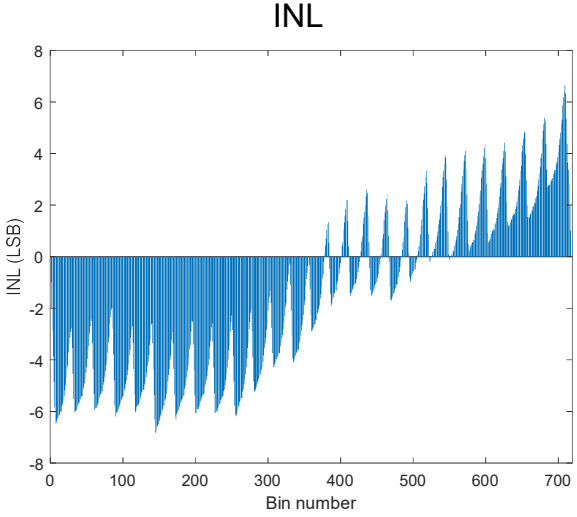
Bin Size, DNL and INL

- Averaged bin size of 8.7 ps
- **Small bins** appear every ~ 200 ps (the coarse stage bin size).
- Leading to:
  - Periodic large DNL error
  - Significant INL error
- It's due to:
  1. Offset misalignment between coarse and fine stages.
     - Static effect
     - Can be corrected by LUT
  2. Noise interference
     - Dynamic effect
     - Hard to correct
     - Degrade the TDC precision



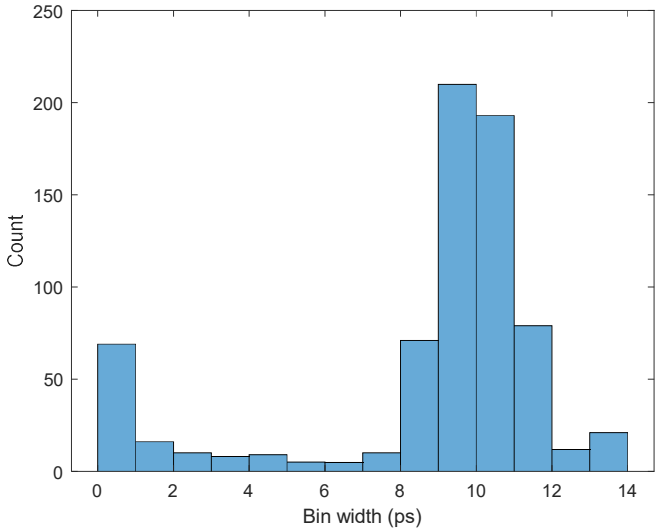




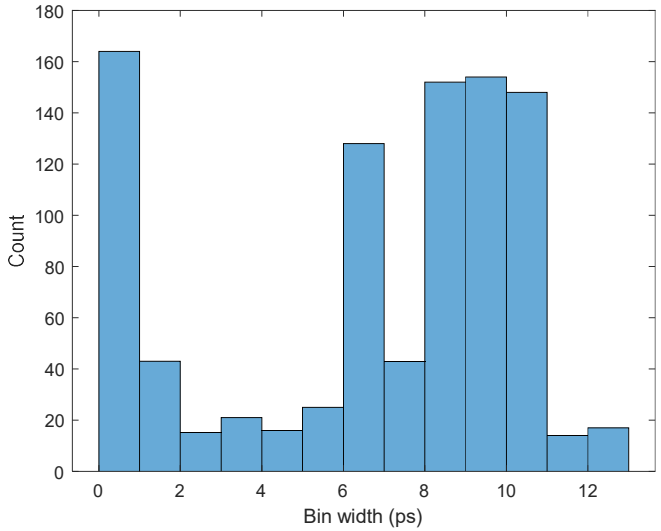


Noise

- The number of small bins is normally around twice of the coarse stage bin number (~ 2 × 30 = 60).
- Too many small bins mean **noise** interference.
- Possible noise sources:
  - Insufficient power integrity of the evaluation PCB → to be optimized
  - On-chip noise from the digital blocks.



Bin distribution of bank 2
(best precision)

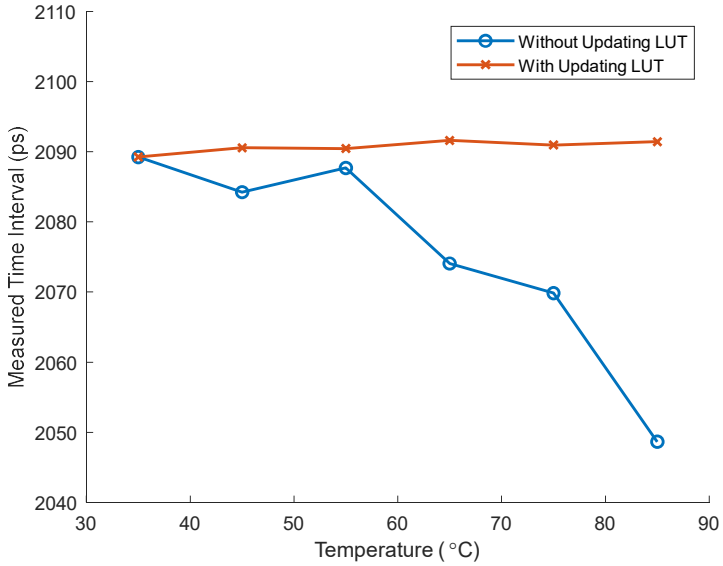


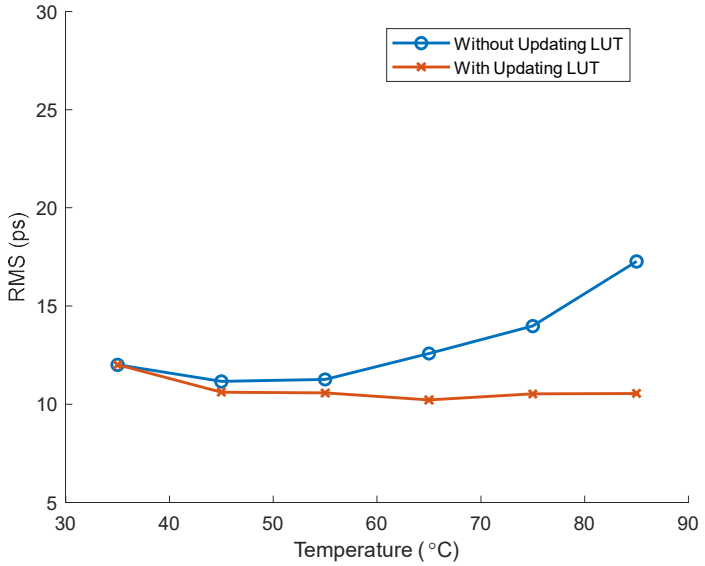
Bin distribution of bank 1
(worst precision)

Sample rate and temperature effect

- Sample rate:
  - Checking the maximum input frequency where the measured TOA sequence loss its continuity
  - Sample rate reaches 7 MS/s
  - Limited by the data acquisition process (100 ns)

- With 50 ℃ temperature change
  - TDC measurement result drifts ~ 2%.
  - TDC precision keeps good (below 20 ps).
  - Updating LUT significantly suppresses the temperature effect.





#04

Summary

Summary

Summary

- Two TDC ASIC designs are taped out for the DTOF detector at STCF.
- Preliminary test results available for the dual-slope TA-TDC
  - The basic requirements are satisfied
  - Further investigation required to figure out unexpected results and for optimization

Undergoing

- Further comprehensive evaluation of the two ASICs
- Comparison and trade-off between the two designs
- Preparing for the next ASIC iteration

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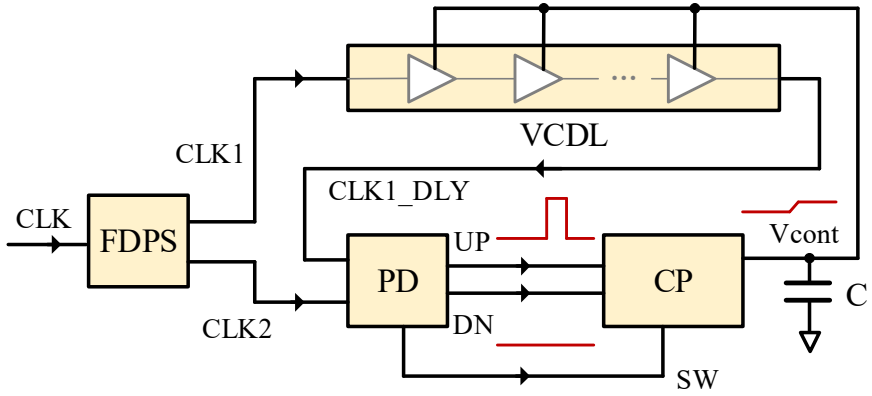
THANKS

For Your Attention

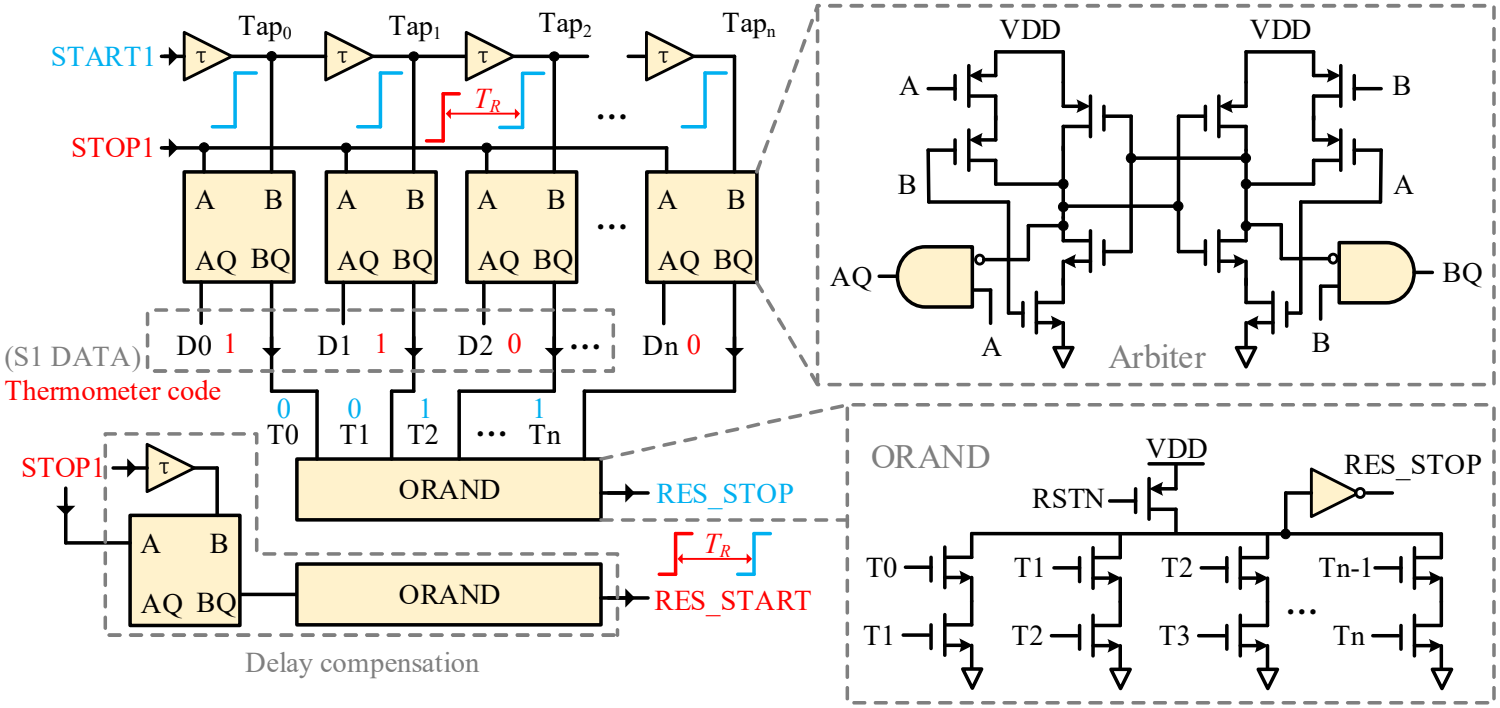
Backup

- Low-power DLL
  - One LP DLL for each TOT bank against intra chip variation
  - Frequency divider and phase shifter
  - Slow down the VCDL nodes switch
  - Start-up free
  - Only one of UP and DN valid in each phase comparison cycle



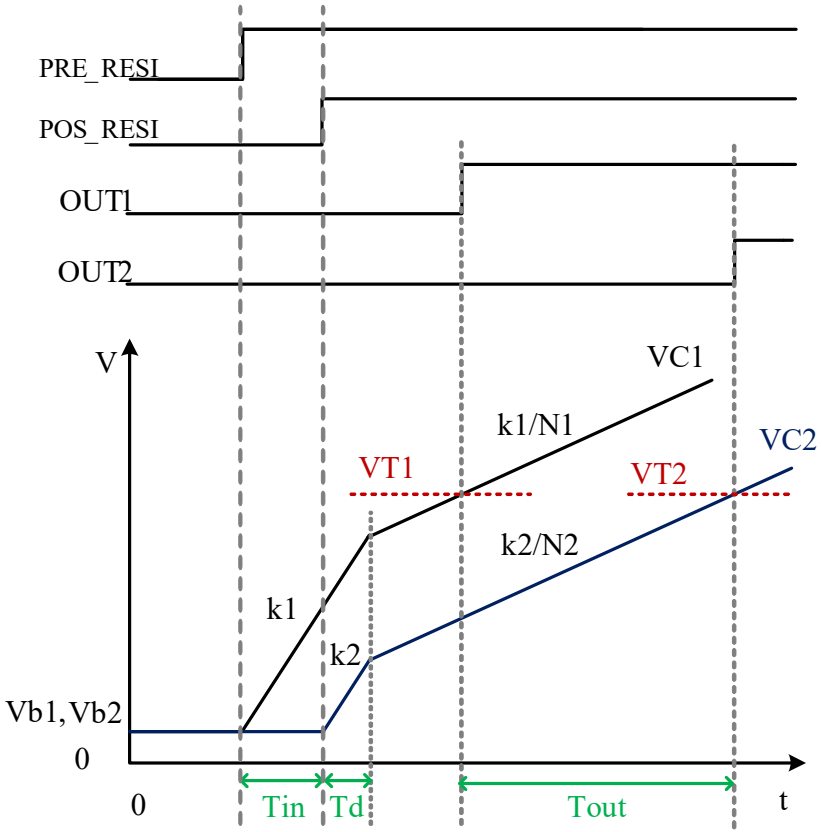
Backup

- Fast residue extraction
  - DFFs are replaced by Arbiters.
  - Half of the arbiter outputs represent the interpolation result.
  - The other half generates RES_STOP.
  - No TA duplication or delay insertion to wait for decoding



Backup

- Td is required for good TA performance with small input.



- Type A (TA_A)
  - Switch the two branches to the slow slew rate Td after the later coming input.
  - Wide input range for both input sequences
  - Gain difference between two input sequences due to mismatch

① $\mathrm{Tin} < 0$:

$$T_{out} = \frac{V_{T2} - V_{b2} - k_2(T_d - T_{in})}{k_2 / N_2} - \frac{V_{T1} - V_{b1} - k_1 T_d}{k_1 / N_1}$$

$$= N_2 T_{in} + (N_1 - N_2)T_d + \frac{N_2(V_{T2} - V_{b2})}{k_2} - \frac{N_1(V_{T1} - V_{b1})}{k_1}$$

② $\mathrm{Tin} > 0$:

$$T_{out} = N_1 T_{in} + (N_1 - N_2)T_d + \frac{N_2(V_{T2} - V_{b2})}{k_2} - \frac{N_1(V_{T1} - V_{b1})}{k_1}$$

- Type B (TA_B)
  - Switch the two branches to the slow slew rate Td after POS_RESI.
  - Limited input range for $\mathrm{Tin} < 0$
  - Better gain matching for both input sequences

$$T_{out} = N_1 T_{in} + (N_1 - N_2)T_d + \frac{N_2(V_{T2} - V_{b2})}{k_2} - \frac{N_1(V_{T1} - V_{b1})}{k_1}$$