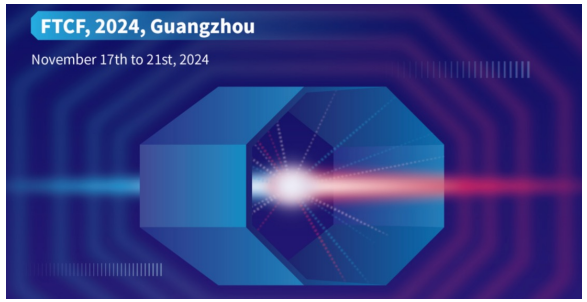
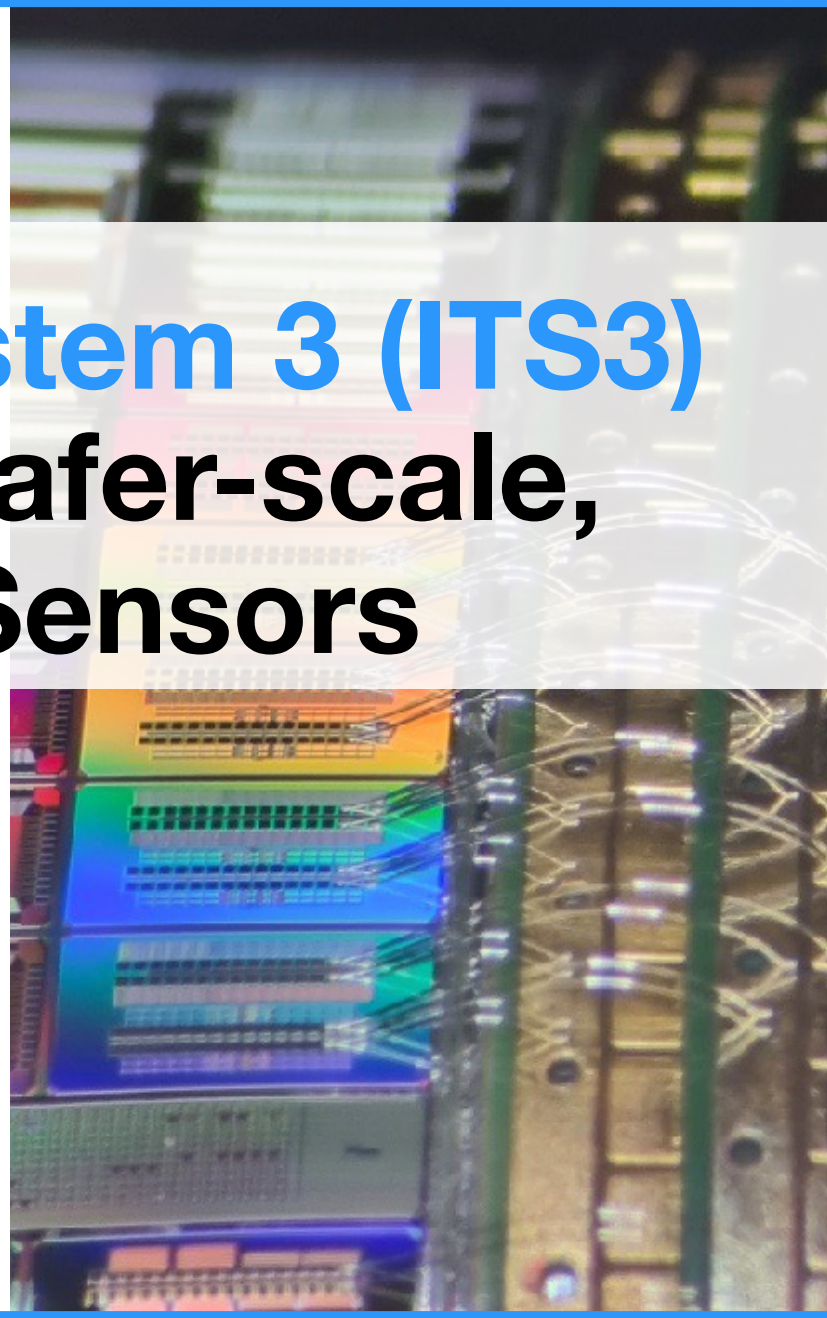
The ALICE Inner Tracking System 3 (ITS3)
a vertex detector based on wafer-scale, bent Monolithic Active Pixel Sensors

Francesca Carnesecchi

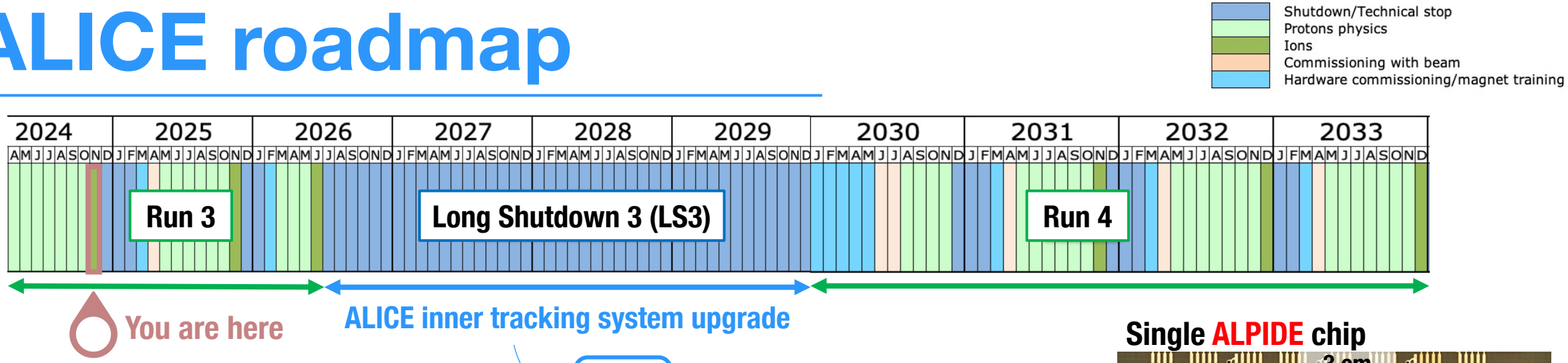
On behalf of the ALICE collaboration

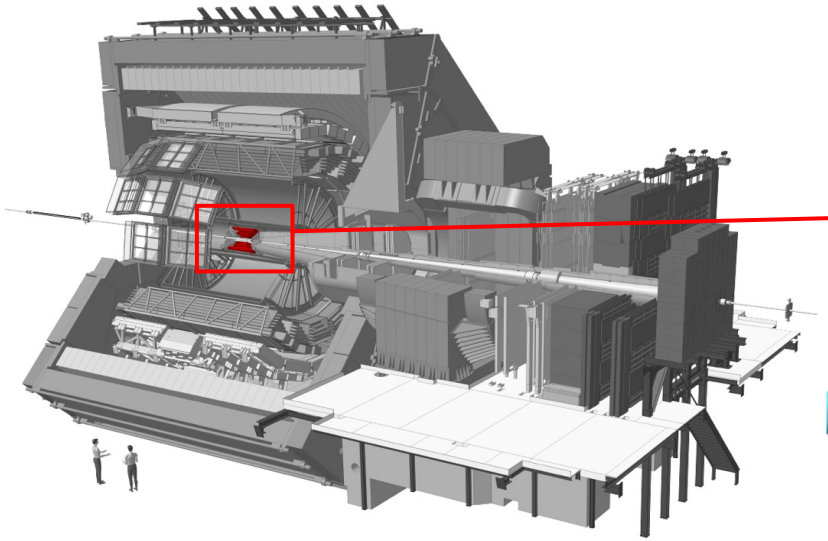




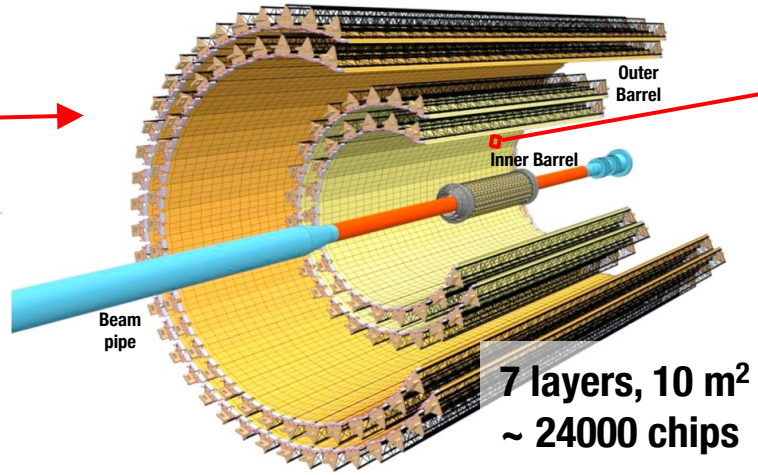
19th November 2024, Guangzhou, China

ALICE roadmap



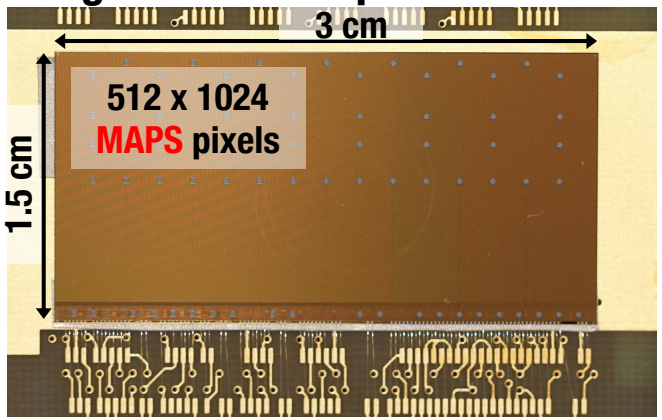


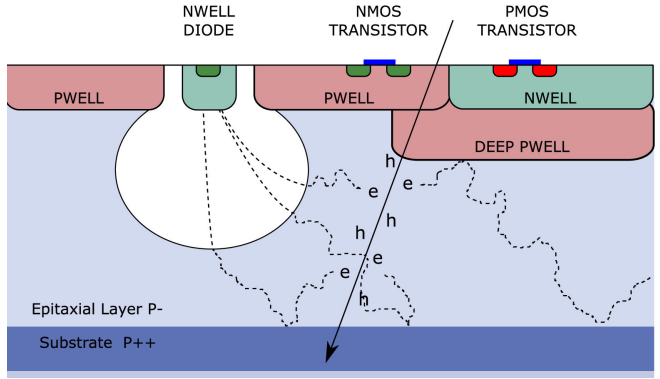
ITS2 → ITS3



7 layers, 10 m²
~ 24000 chips

Single ALPIDE chip



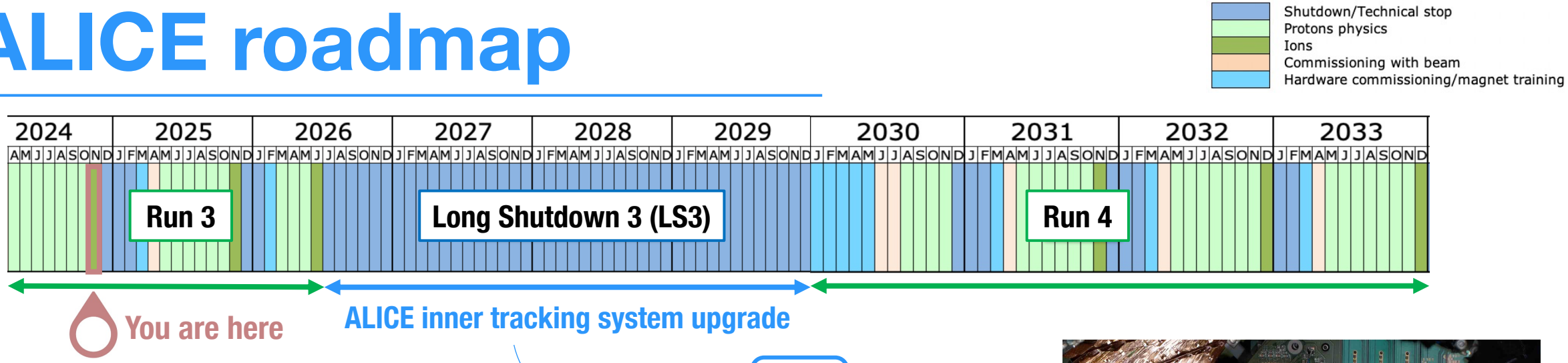


ITS2, Closer, thinner, better:

- 23 mm from IP
- 0.36% x/X_0 per layer, Inner Barrel
- 1.14% x/X_0 per layer, Outer Barrel
- pixel size ~ 27x29 μm²

In-pixel:
amplification, discrimination and multi event buffer

ALICE roadmap

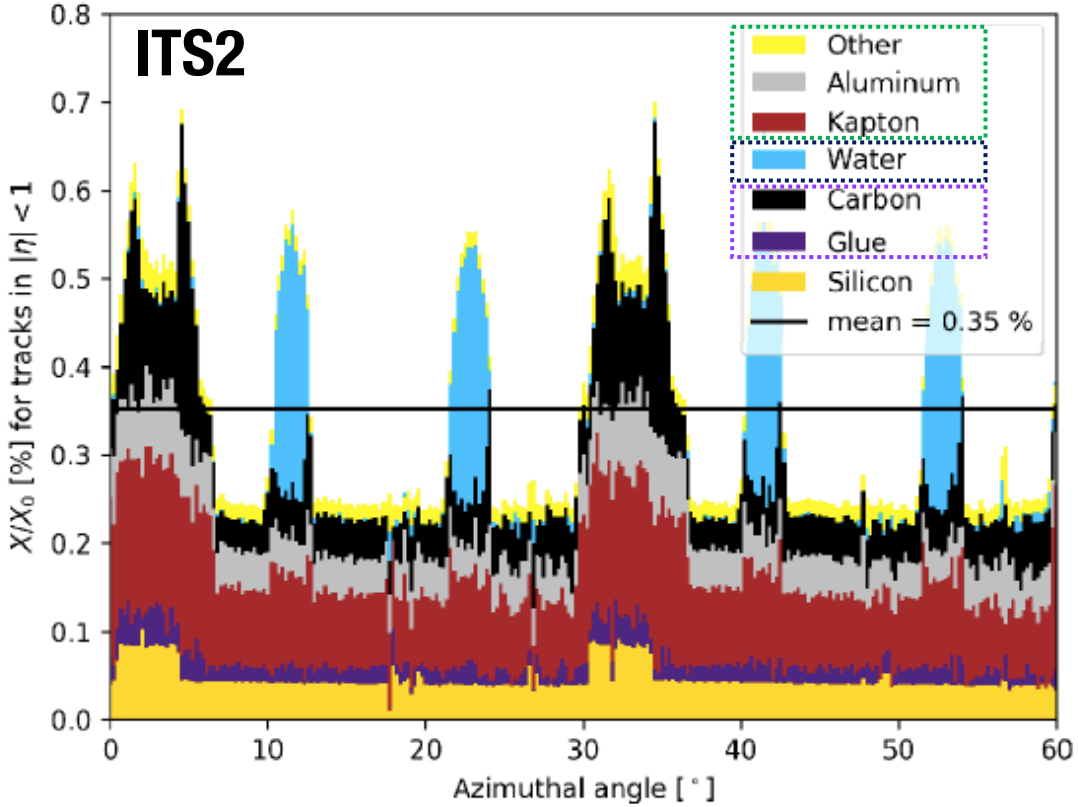


How can we further improve the ITS2 performance? → **Replacing the 3 innermost layers** with new ultra-light, truly cylindrical layers

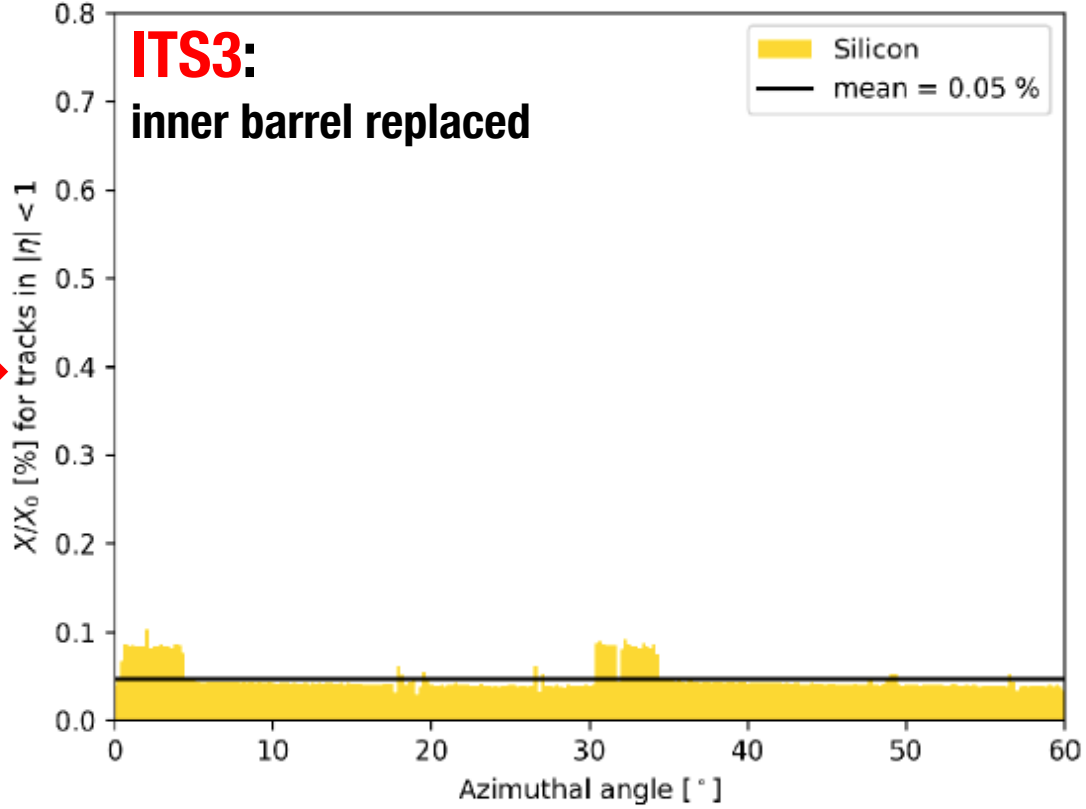
Idea – reduce material budget

How can we further improve the ITS2 performance?

Replacing the 3 innermost layers



x 1/7



- Removal of **circuit board** → possible if integrated in circuit (stitching)
- Removal of **water cooling** → possible if power consumption < 40 mW/cm^2
- Removal of **mechanical support** → possible if self supporting arched structure (benefit from increased stiffness by rolling silicon wafers)

How – ITS3 concept

ITS3 TDR, CERN-LHCC-2024-003, https://cds.cern.ch/record/2890181

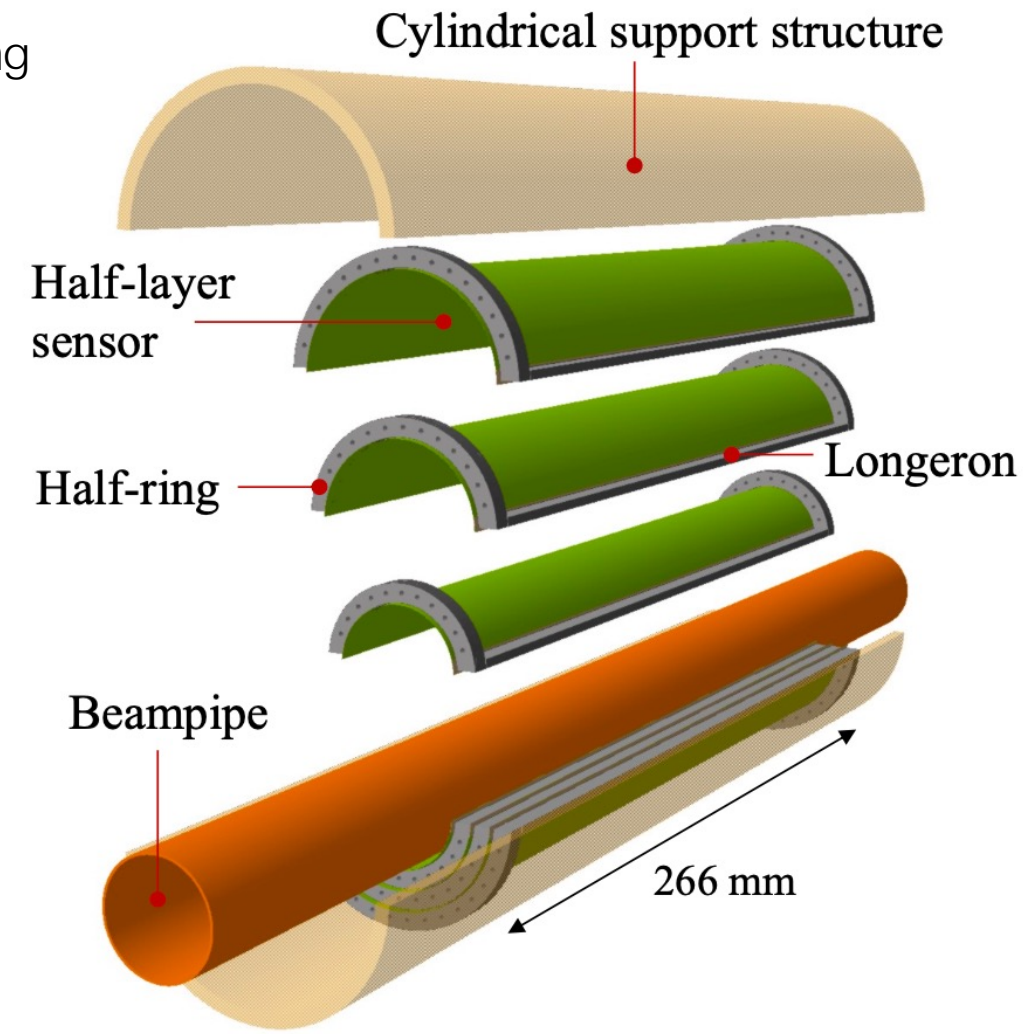
From 432 to 6 bent sensors

ITS3: an ultra-light, truly cylindrical layers made of wafer scale 65 nm MAPS

Key ingredients:

- **300 mm wafer-scale MAPS sensors**, fabricated using stitching
- **thinned down** to 50 μm, making them flexible
- **bent** to the target radii
- mechanically held in place by carbon foam ribs
- cooled down by air

Layer parameters	Layer 0	Layer 1	Layer 2
Radial position (mm)	19	25.2	31.5
Length (sensitive area) (mm)		259.992	
Sensor azimuthal width (mm)	58.692	78.256	97.820
Total sensor thickness (um)		≤ 50	



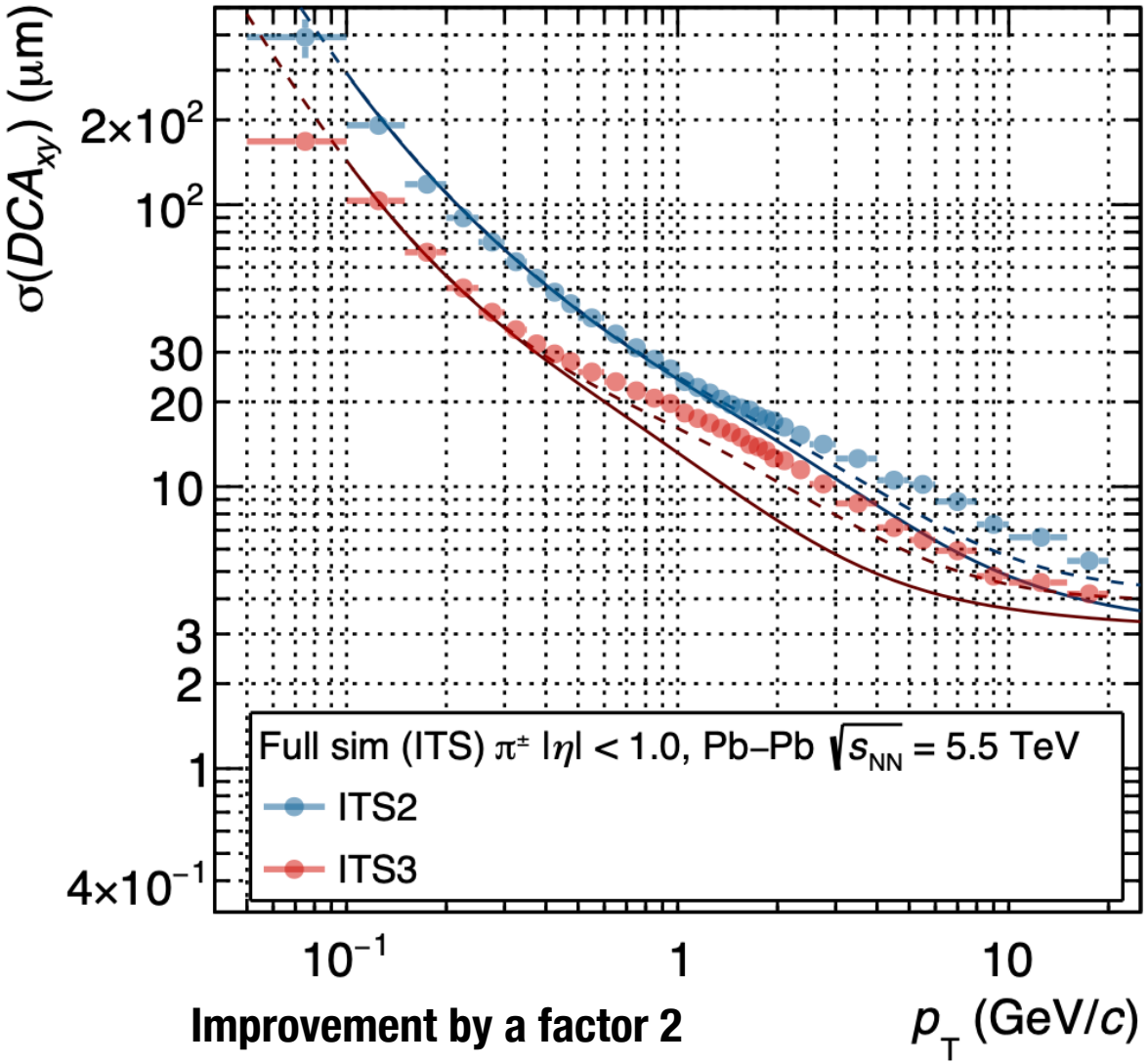
ITS3 – Performance

ITS3 TDR, CERN-LHCC-2024-003, https://cds.cern.ch/record/2890181

Improvement of **pointing resolution**:

- Reduction of **material budget** (0.36 → 0.07 X_0/layer)
- **Closer** to interaction point (23 → 19 mm)
- Smaller and thinner **beam pipe** (18 → 16 mm, 700 → 500 μm)

→ **boost of the ALICE core physics program**, largely based on low momenta and secondary vertex reconstruction



ITS3 - roadmap and main challenges

Outline

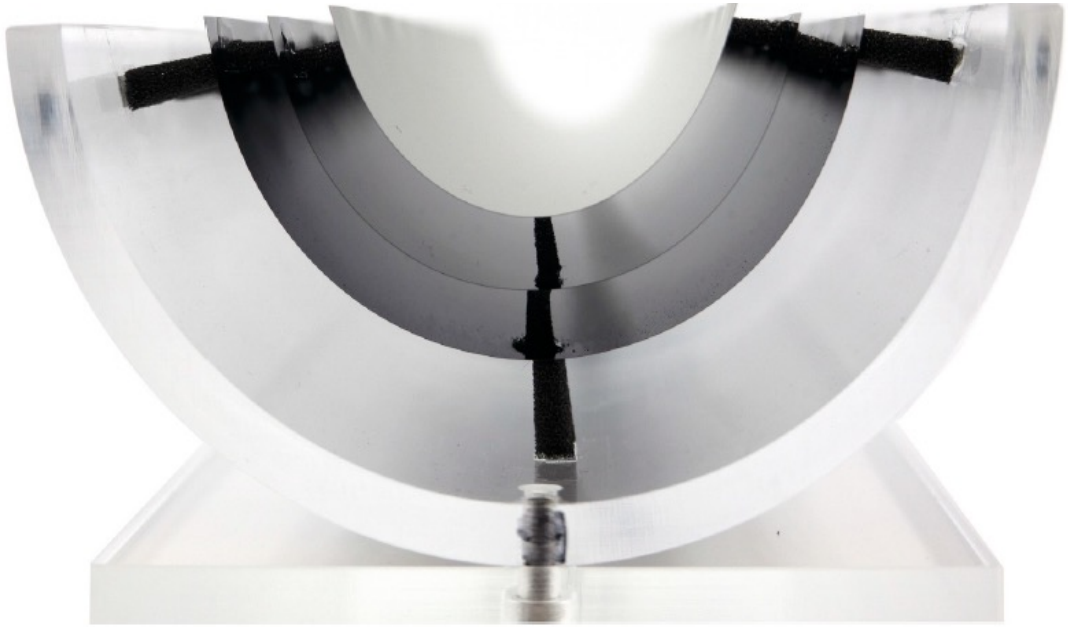
Support with carbon foam ribs (handling ultra thin structures) and air for cooling
Several mechanical prototypes manufactured, procedures to handle large thin chips and thermal tests done

Silicon flexibility and bending: ultra-thin, bent Monolithic Active Pixel Sensors
Proof of concept demonstrated for both 180 nm and 65 nm, performance of bent silicon at different target radii done

Sensor design: 65 nm CIS process of TPSCo
Qualification done

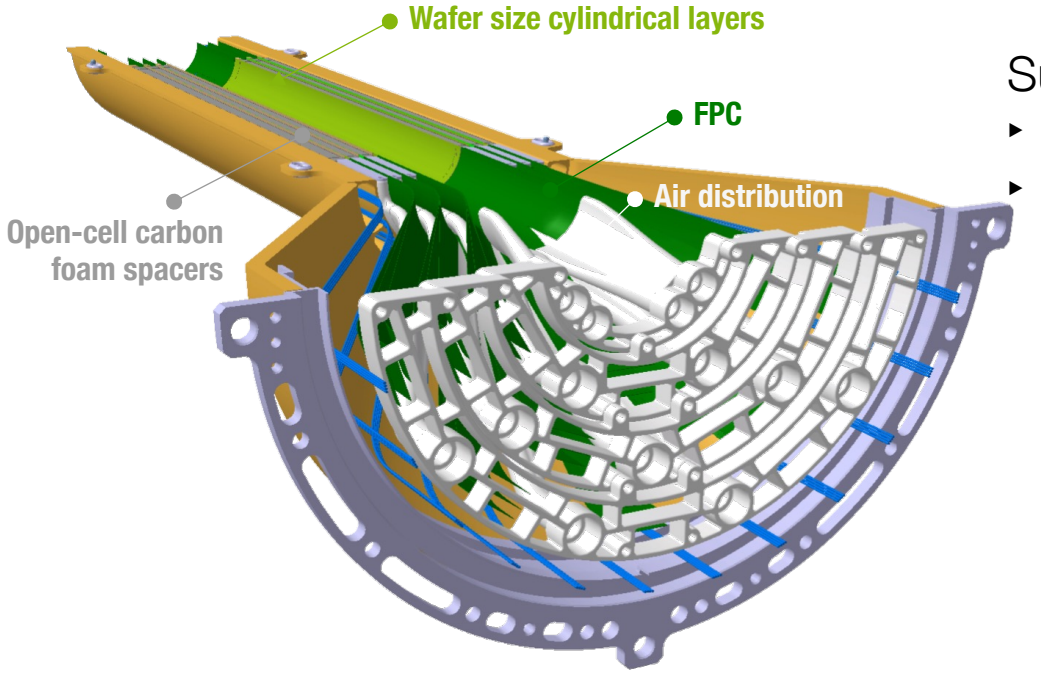
Stitching of wafer scale-chips
Production and test of first stitched done, 26 cm-long MAPS

Final sensor prototype
Design almost finished, to be submitted by early 2025



Engineering Model 1

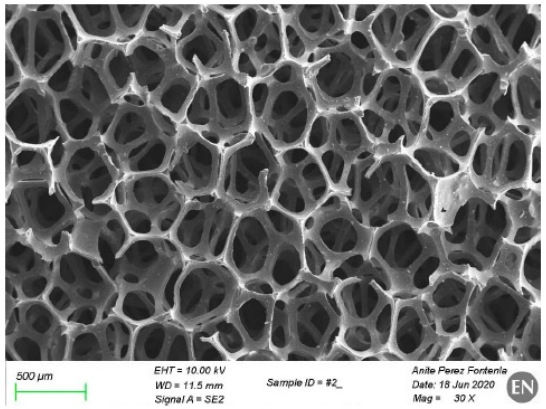
Support and cooling



Support and cooling optimization, maintaing the low material budget

- carbon foam as **spacers**
- optimezed/improved for amount of glue and distortion

ERG Carbon
@Duocel
ρ = 50 kg/m^3
K = 0.05 W/m·K



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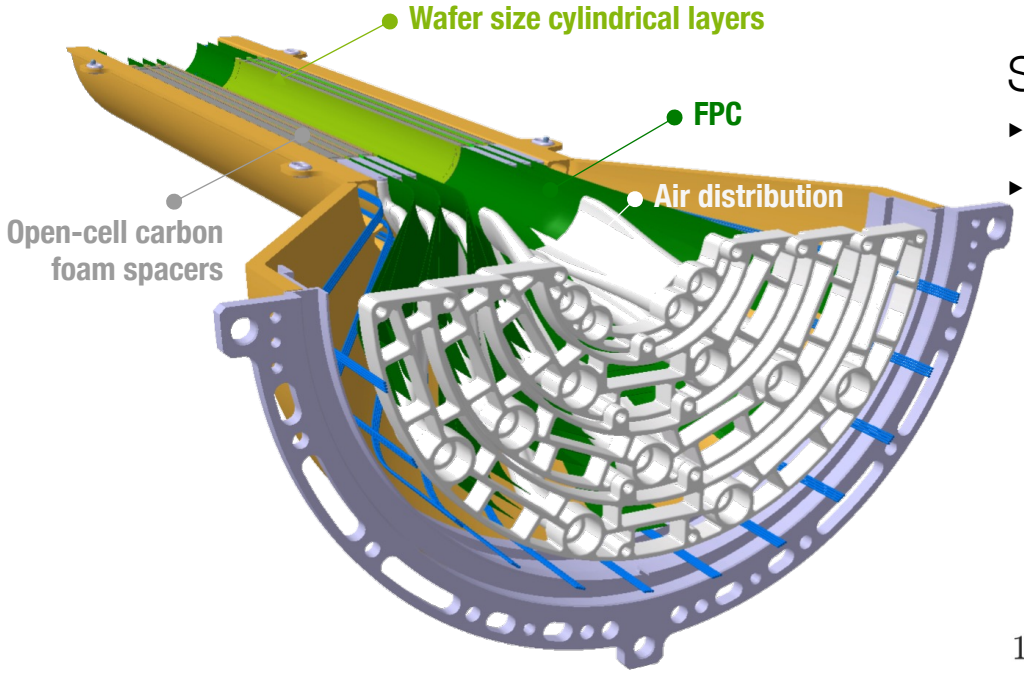

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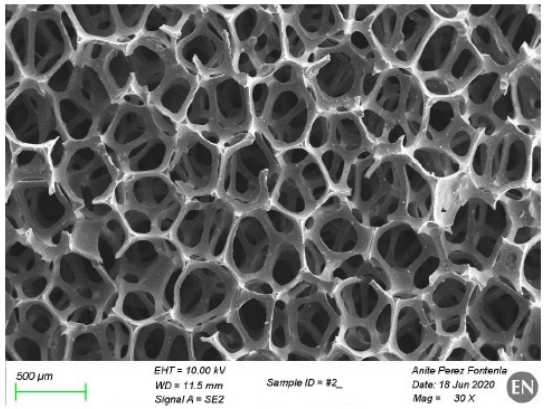
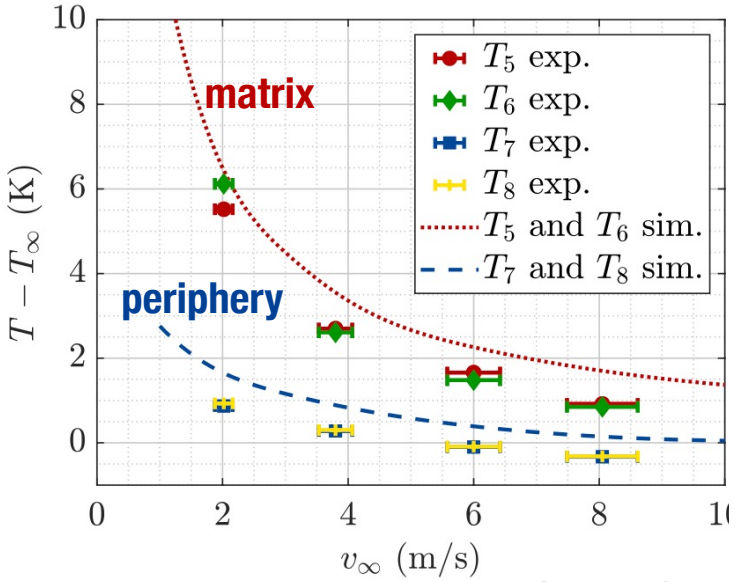


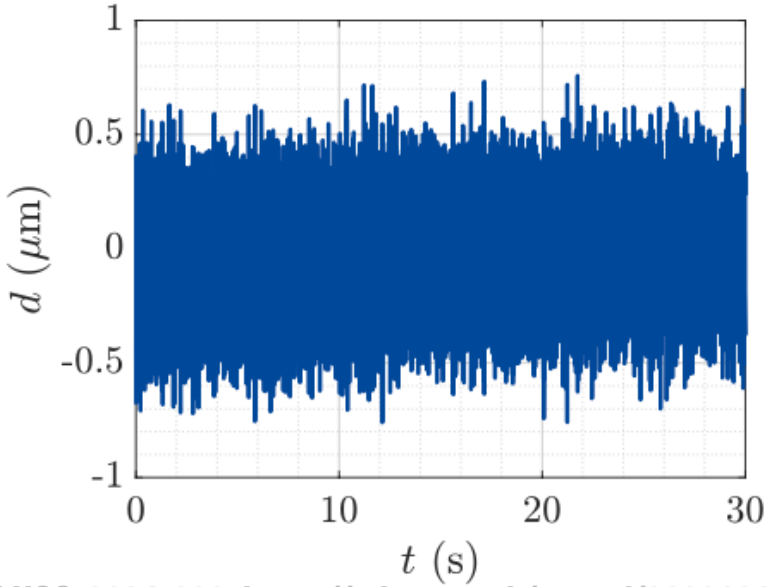
Air cooling, thermal and stability test:

- A set of bread board models based on heating elements
- Placed in a custom wind tunnel, thermal and mechanical properties studied

Temperature variation



Vibrations, center (8 m/s)



ITS3 TDR, CERN-LHCC-2024-003, https://cds.cern.ch/record/2890181

Sensor design: MLR1

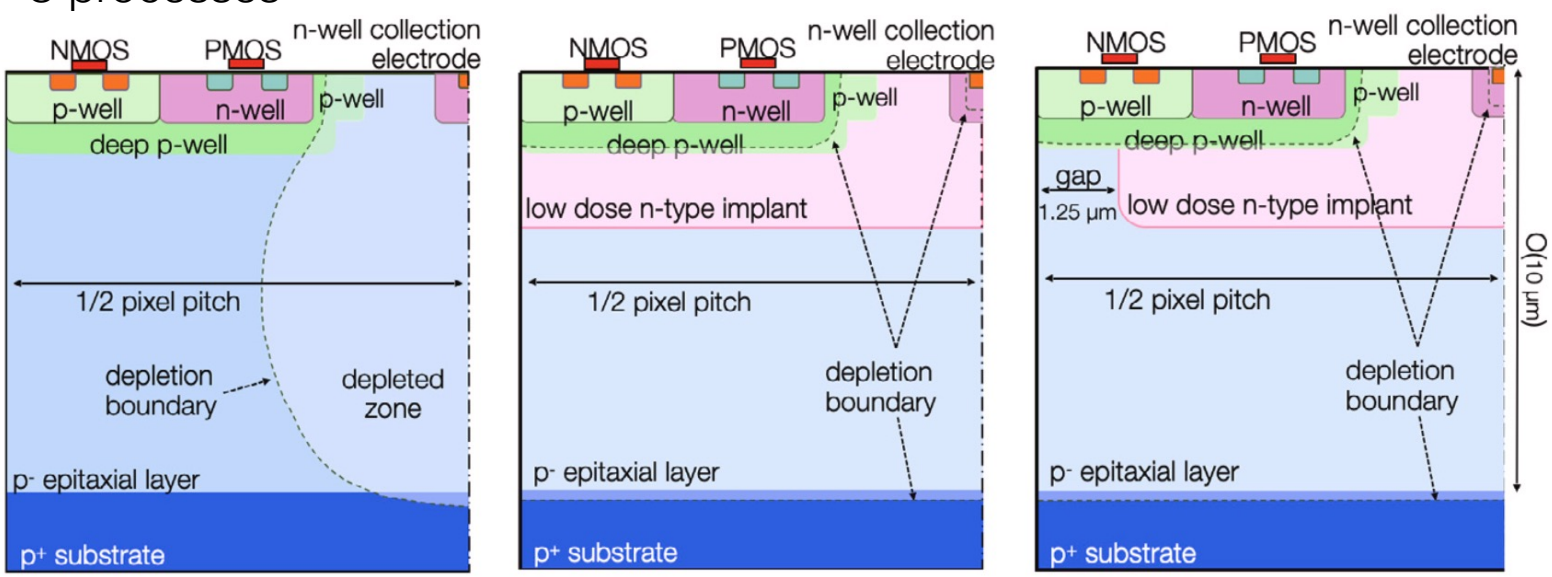
Multi Layer Reticle 1

First submission in the Tower Partners Semiconductor (TPSCo) **65 nm technology**
Multi Layer Reticle 1: received in 09/2021

Benefits:

- larger wafers: 300 mm (instead of 200 mm), single “chip” is enough to equip an ITS3 half-layer
- smaller structure sizes:
  - lower power consumption
  - improve spatial resolutions
  - increase in-pixel circuitry
  - increase yield

3 processes



Standard **Modified** **Modified with gap**

Charge Collection efficiency and speed

Charge sharing

Sensor design: MLR1

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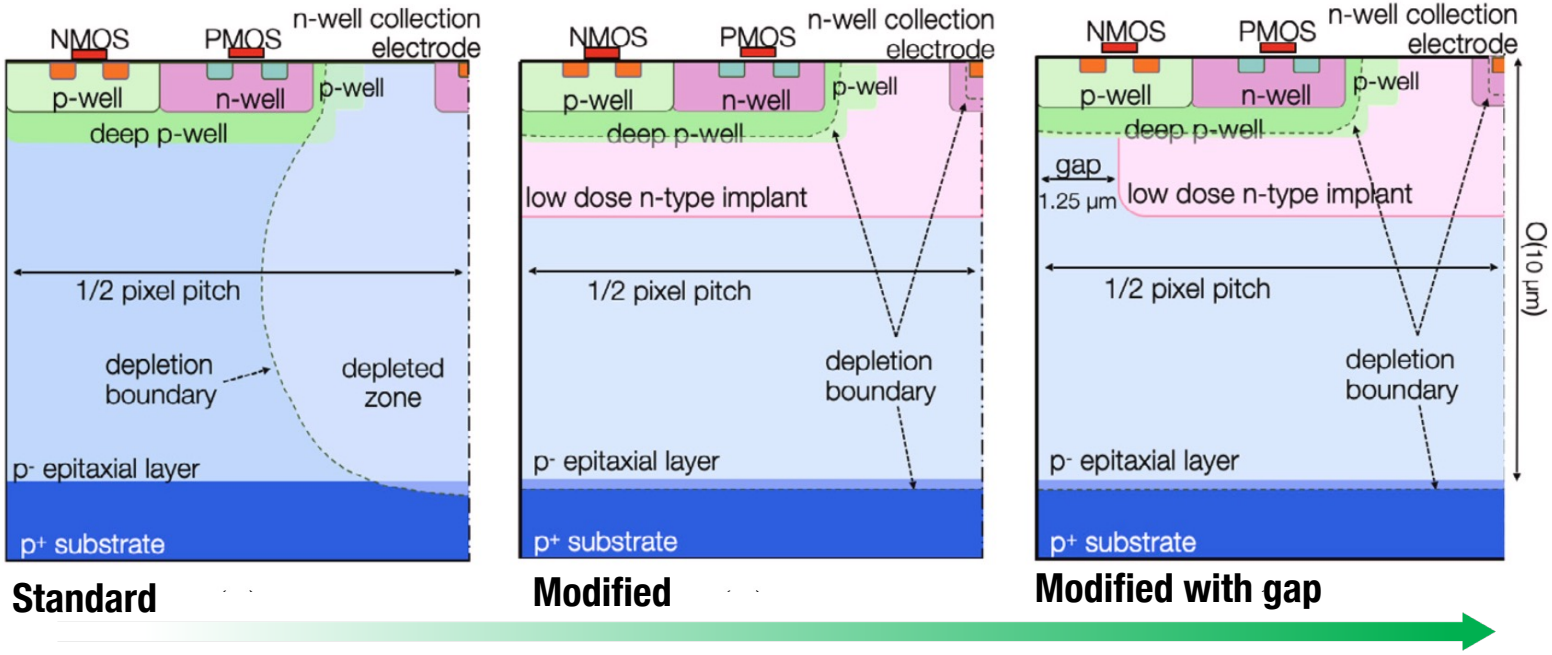
  - improve spatial resolutions
  - increase in-pixel circuitry
  - increase yield
- **55 prototype chips**
  - With various differences, among others: processes, pitches
- **verification of the technology done,** for charge collection efficiency, detection efficiency, radiation hardness
- **technology explored far beyond the requirements of ITS3** in terms of radiation hardness and time resolution

3 processes



Sensor design - performance

https://doi.org/10.1016/j.nima.2024.169896

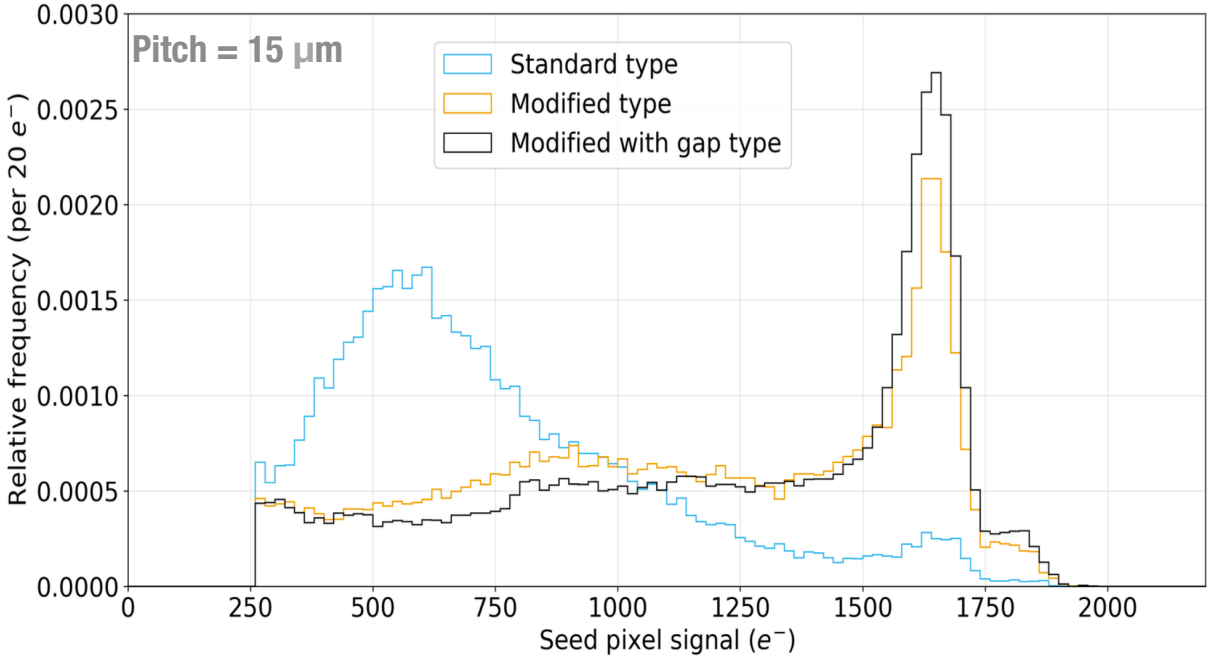
Fe-55 radioactive source

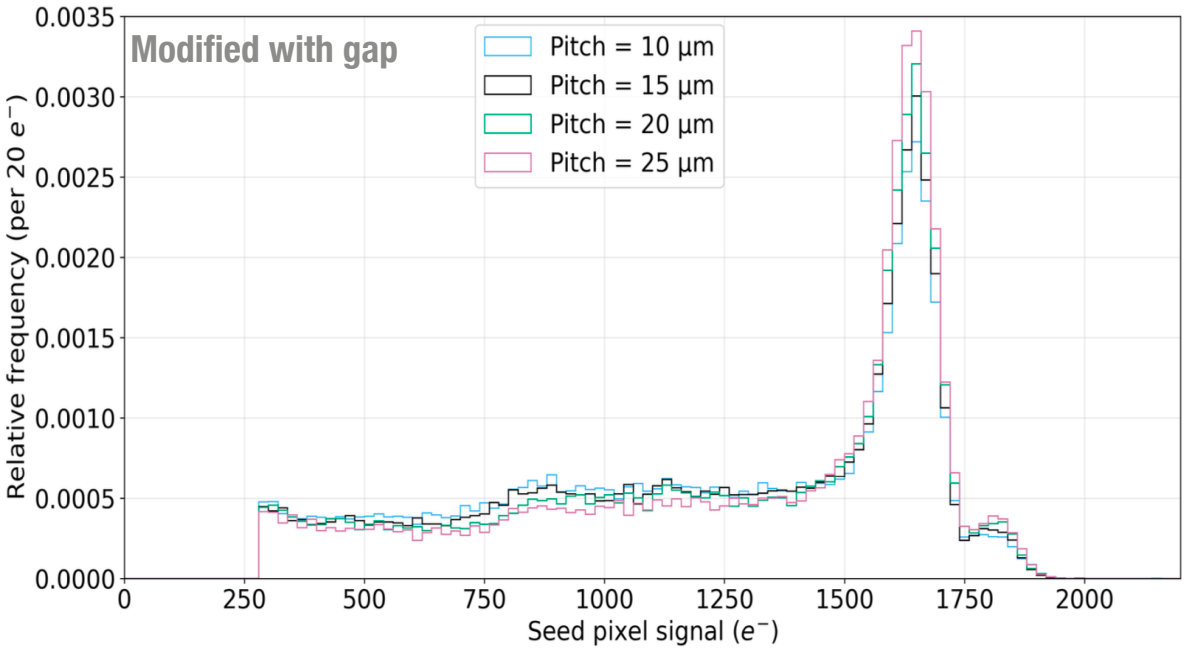
For the modified process:

- full depletion of sensors
- electric field pointing to collection electrodes

For different pitches, 10 to 25 μm:

- similar results
- allows to choose optimal pitch





- Demonstrated also an excellent detection efficiency over large threshold range for modified processes, for all pitches

Sensor design - performance

Process: modified with gap

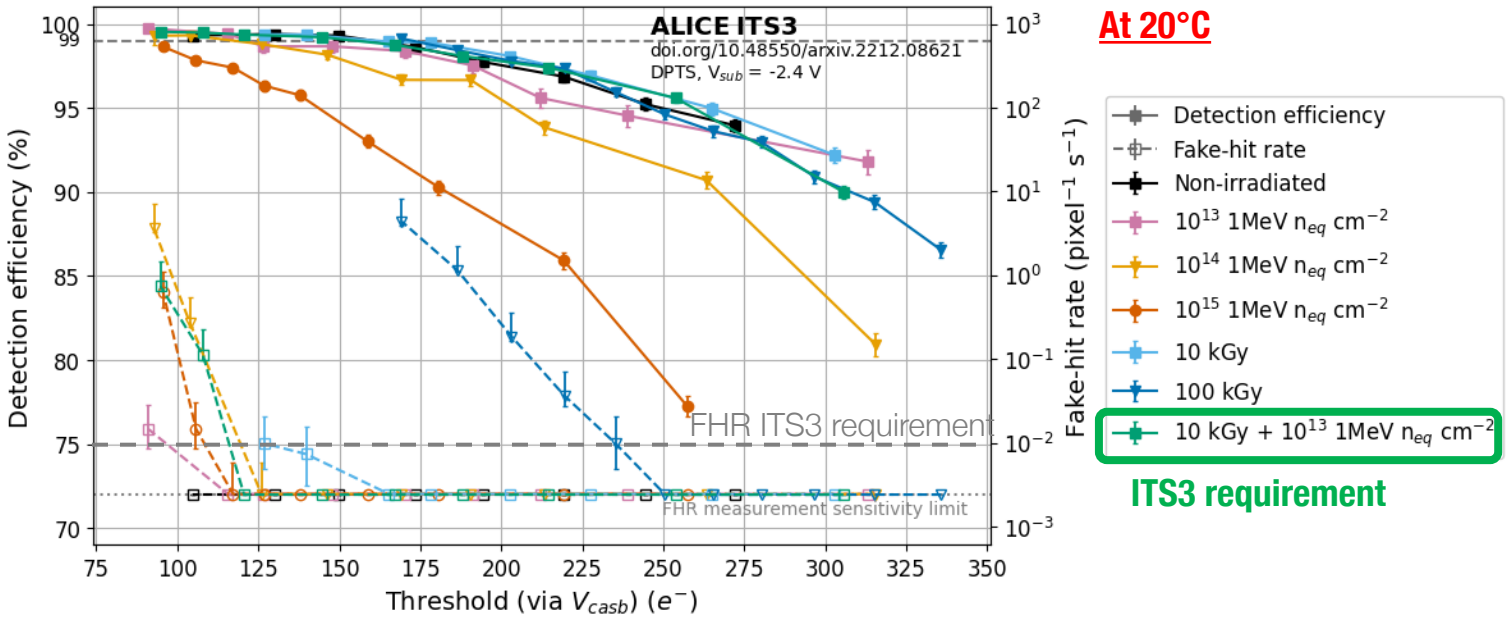
https://doi.org/10.1016/j.nima.2023.168589
https://doi.org/10.1016/j.nima.2024.170034

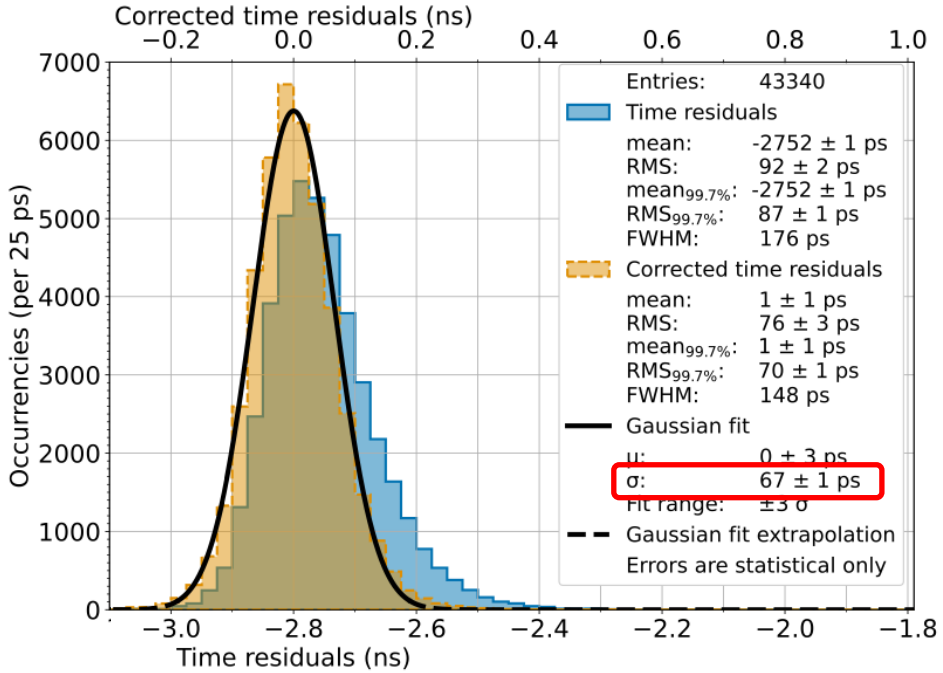
Efficiency and FHR:

- At ALICE-ITS3 requirements irradiation level slightly larger fake rates, but still largely operational
- At 10^{15} n_{eq}/cm^2 → ~99% efficiency reached at 20°C

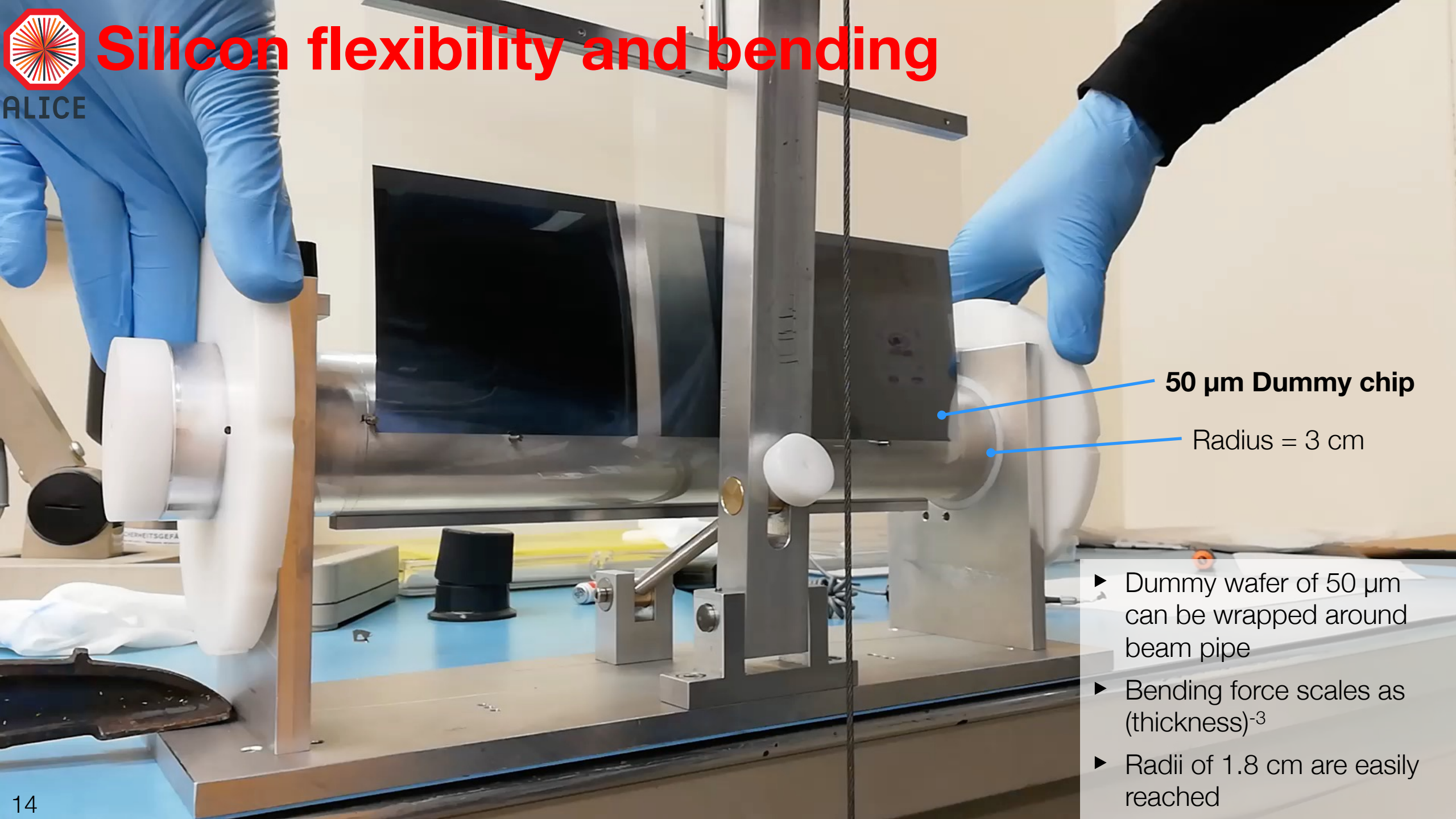
Time resolution:

- For a 10 μm pitch, 67 ps reached





Silicon flexibility and bending



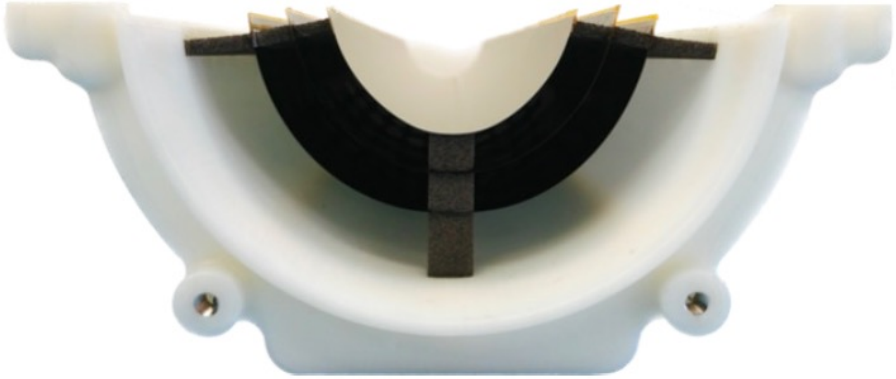
- Dummy wafer of 50 µm can be wrapped around beam pipe
- Bending force scales as $(\text{thickness})^{-3}$
- Radii of 1.8 cm are easily reached

Silicon flexibility and bending

Mechanical mockup of 3 truly cylindrical dummy layers
- Several mockups done

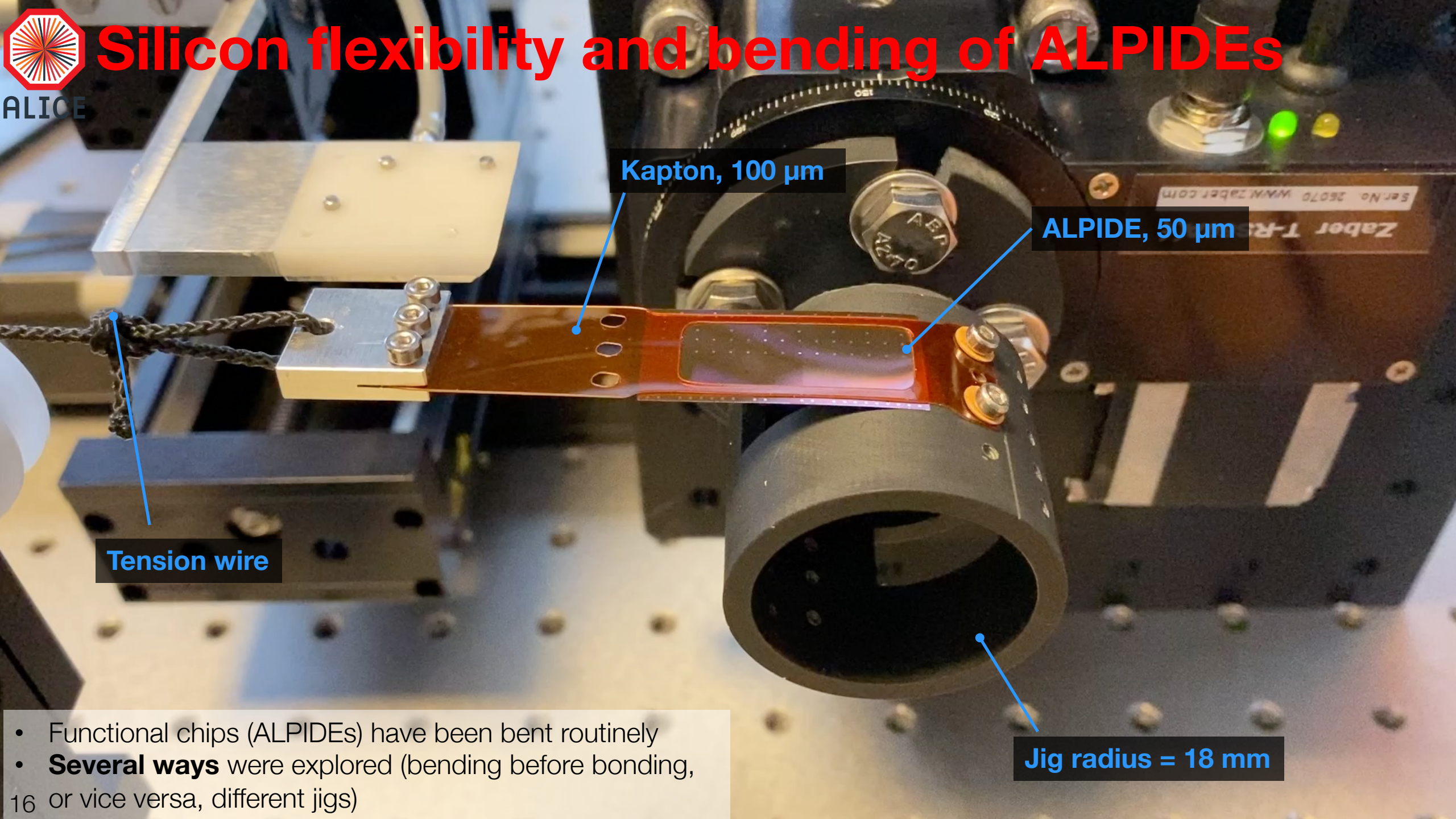
Engineering Model 2:
40 µm, 280 mm long

front



back

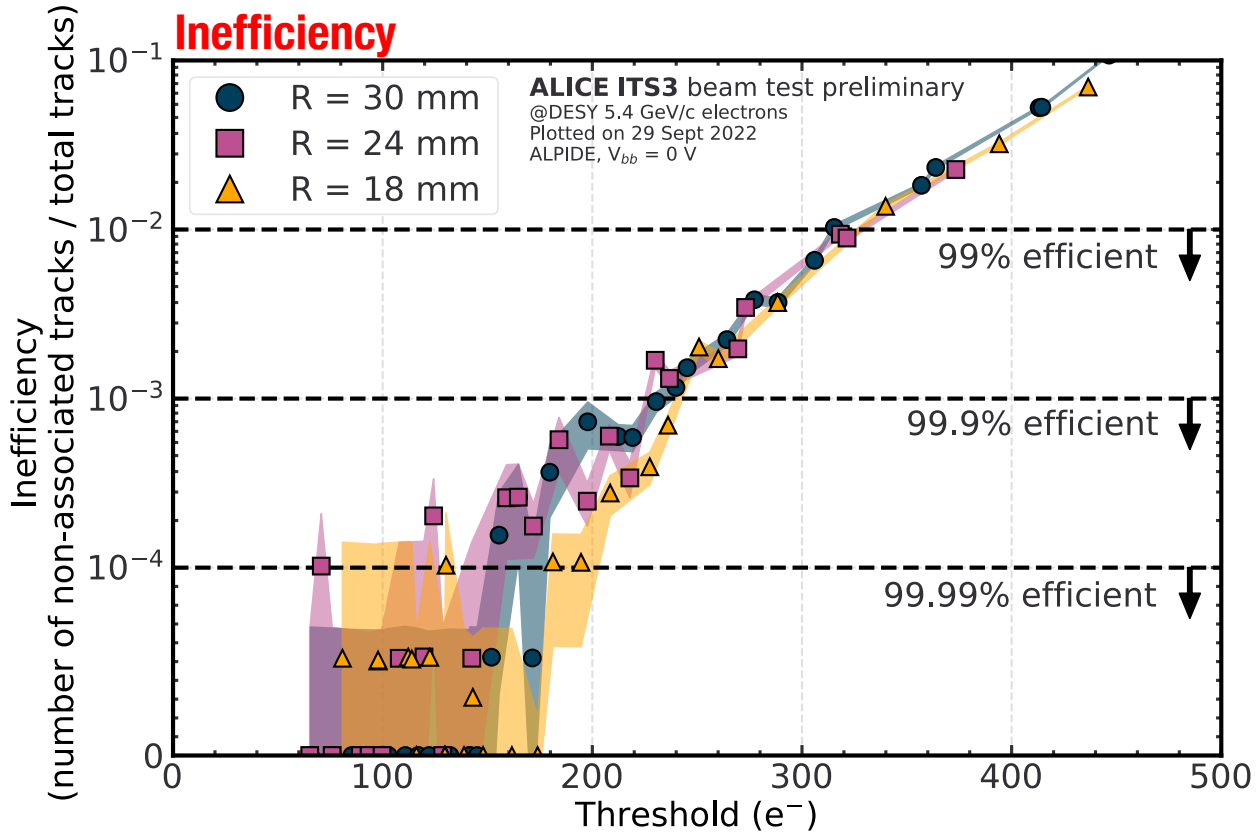
Silicon flexibility and bending of ALPIDEs



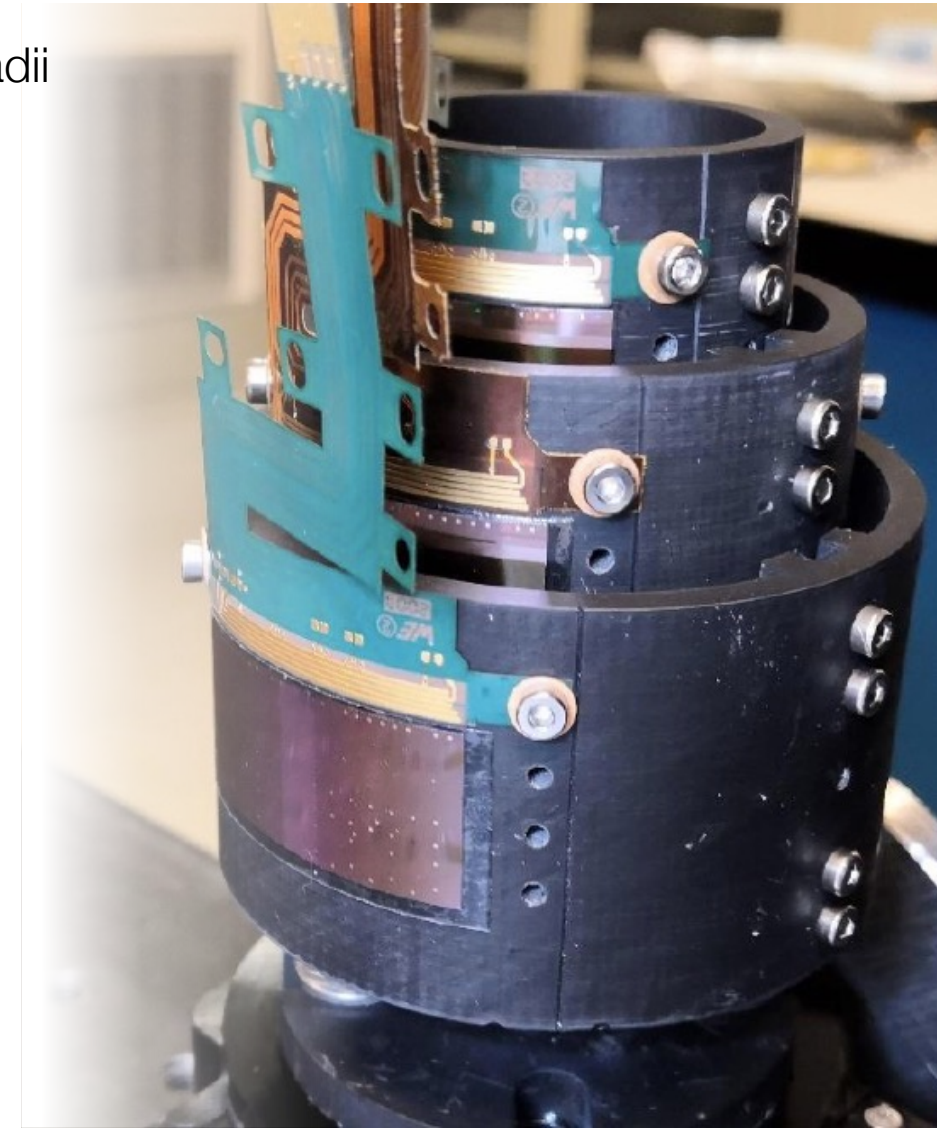
- Functional chips (ALPIDEs) have been bent routinely
- **Several ways** were explored (bending before bonding, or vice versa, different jigs)

Silicon flexibility and bending of ALPIDEs

- **The chips continue to work**
  https://doi.org/10.1016/j.nima.2021.166280
- Full mock-up called "**μITS3**": 6 ALPIDE chips, bent to ITS3 target radii
  - **Beam test** on μITS3: **uniform** among different radii

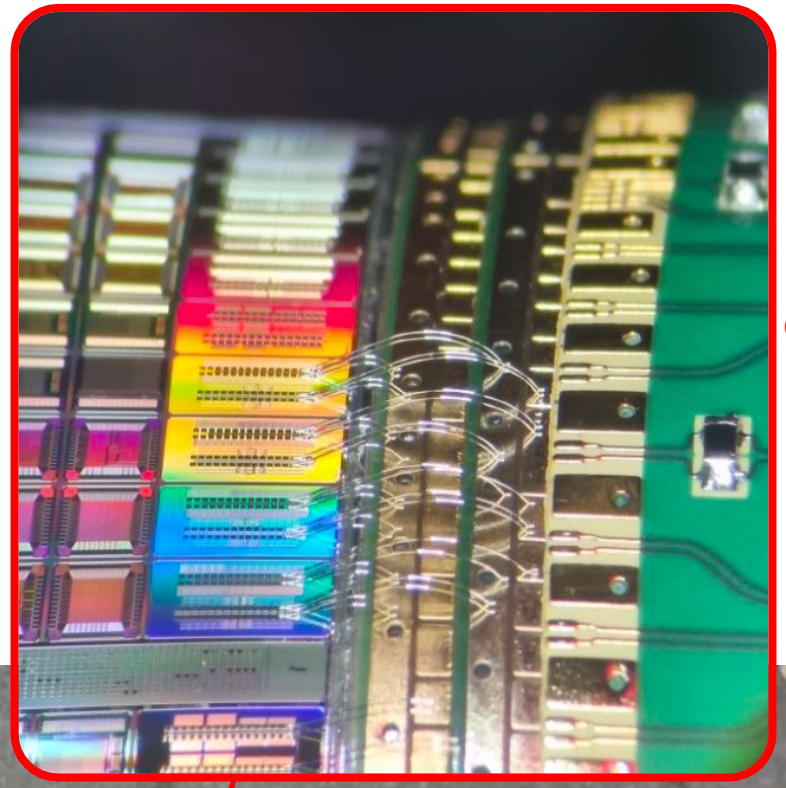


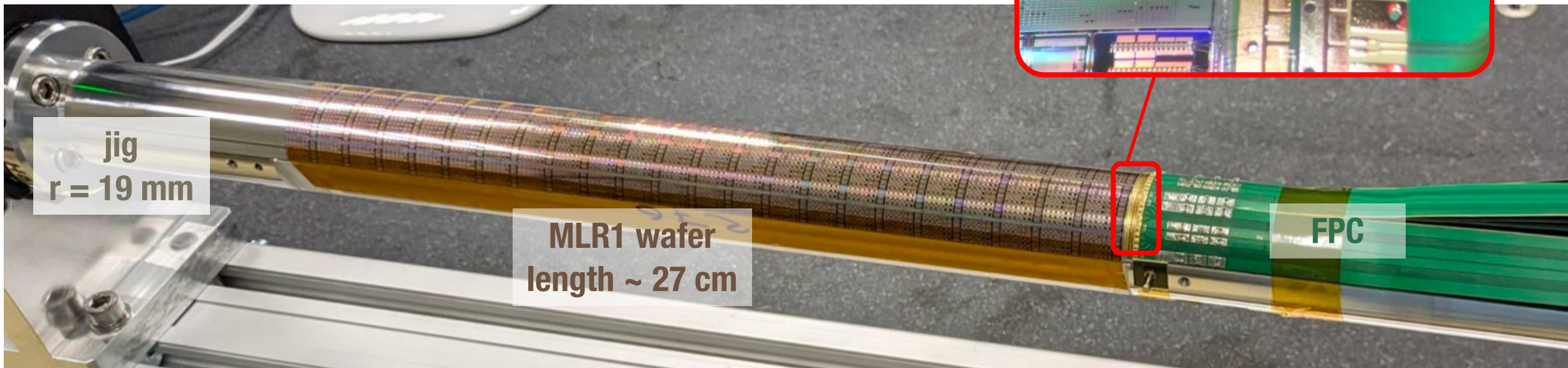
μITS3: 6 ALPIDEs bent



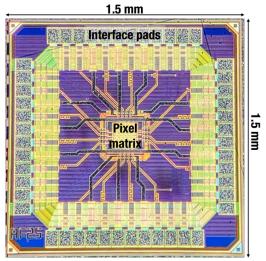
Silicon flexibility and bending of MLR1

- special boards developed to **bond and test** MLR1 structure
  - measurements confirm no performance degradation
- **bending and assembly of full L0** using MLR1 wafers
  - wirebonded to an FPC

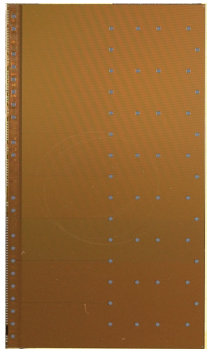




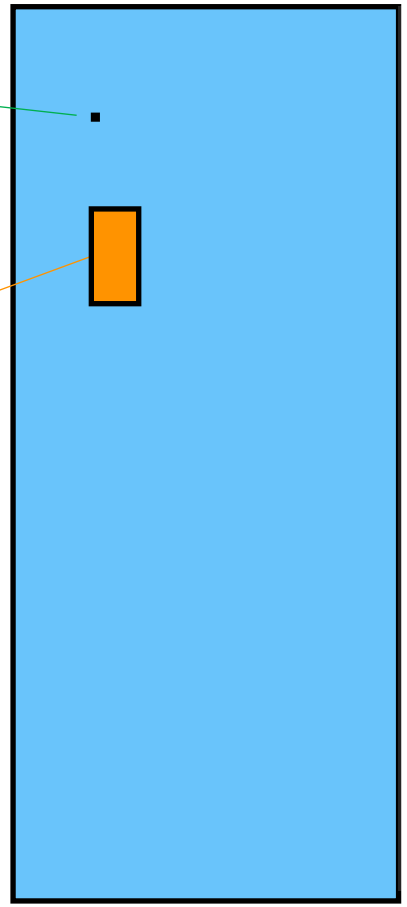
Stitching – a wafer scale sensor



MLR1
1.5 x 1.5 mm



ALPIDE
30 x 15 mm
limited by reticle size

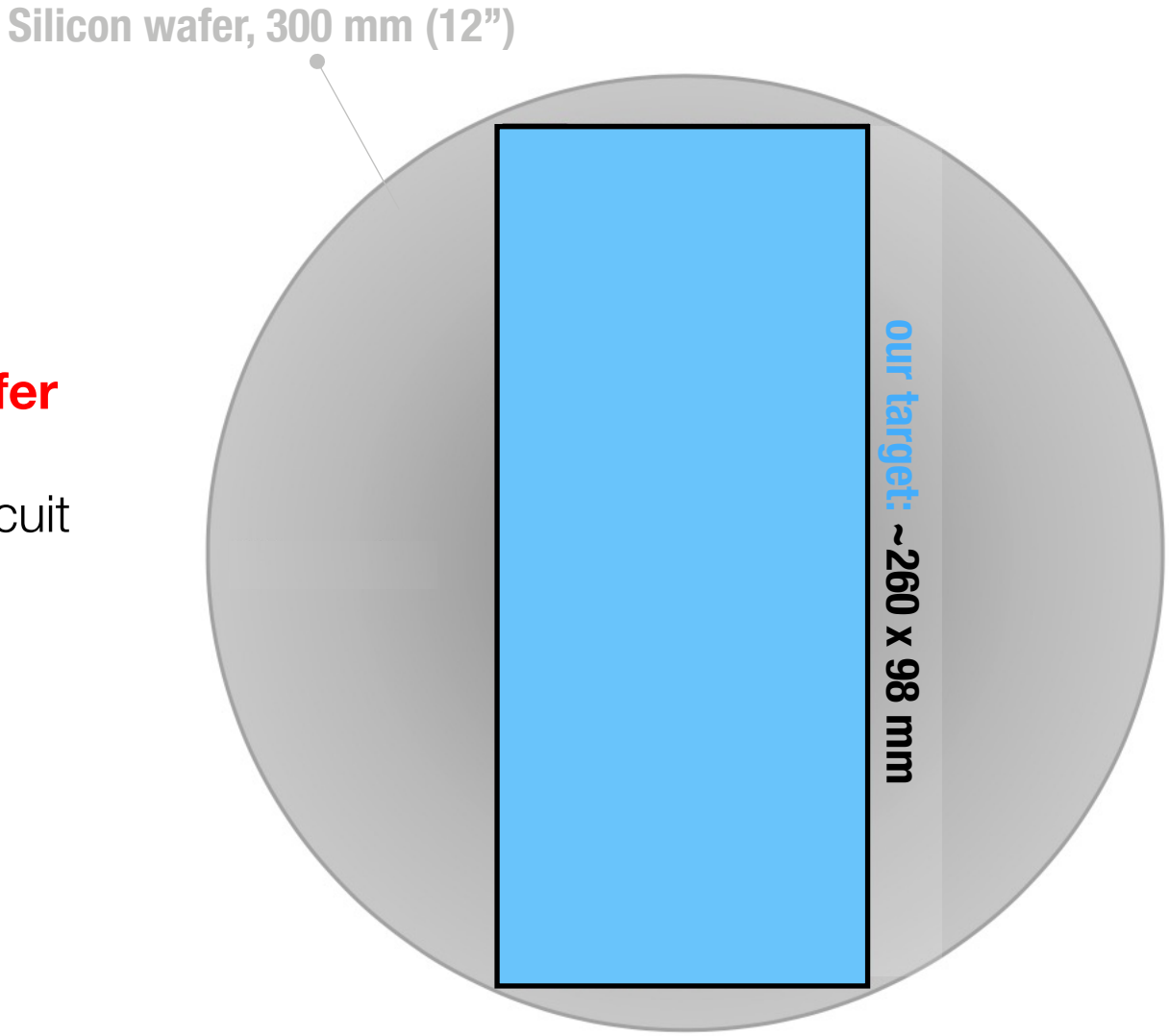


our target: ~260 x 98 mm

Stitching – a wafer scale sensor

For such large area → stitching needed:

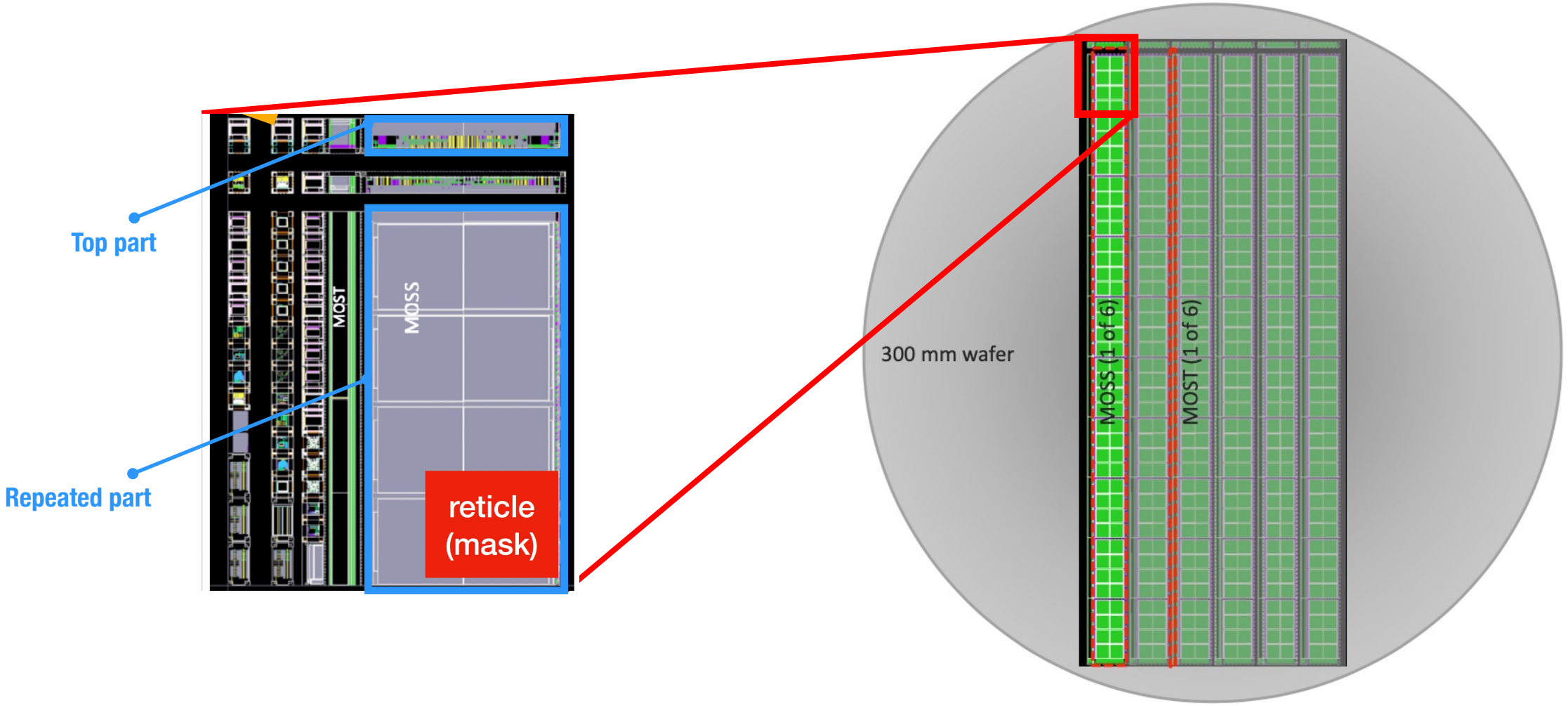
- aim at a realization of **a true single wafer scale sensor**
- eliminates the need of tiling chips on circuit boards



Stitching

What we designed…

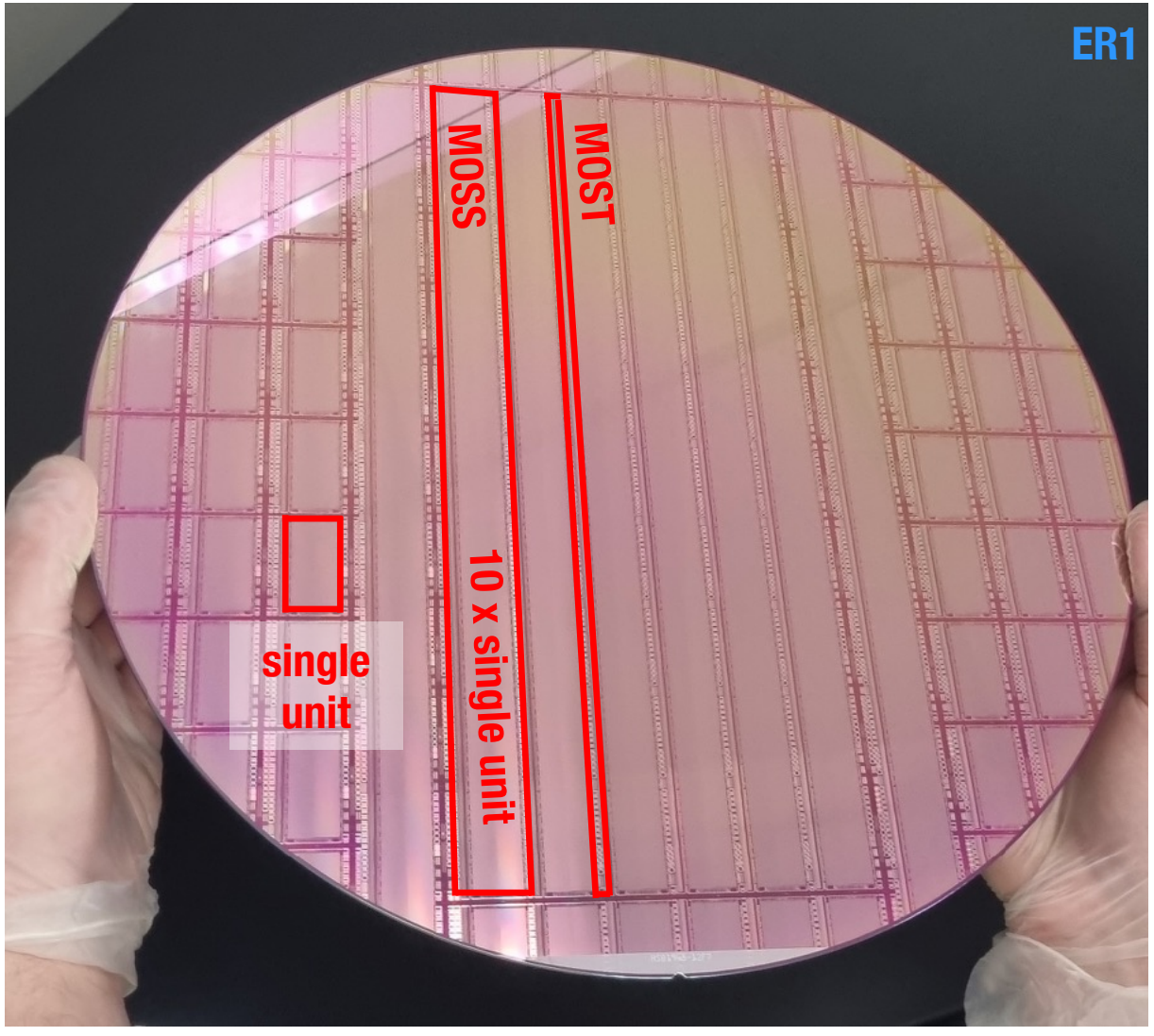
…what we want to fabricate



ER1: stitched wafer-scale MAPS in 65 nm

Engineering Run 1 (ER-1), received in 05/2023

- First MAPS for HEP using stitching
  - one order of magnitude larger than previous chips
  - based on TPSCo 65 nm, MLR1
- **MOSS**: 14 x 259 mm, 6.72 MPixel
  - MOnolithic Stitched Sensor
  - 2 different pitches
- MOST: 2.5 x 259 mm, 0.9 MPixel
  - 18 x 18 μm^2
  - more dense design, different power granularity
- Single unit → Baby-MOSS (~ reticle-sized)
- Plenty of small chips (like MLR1)



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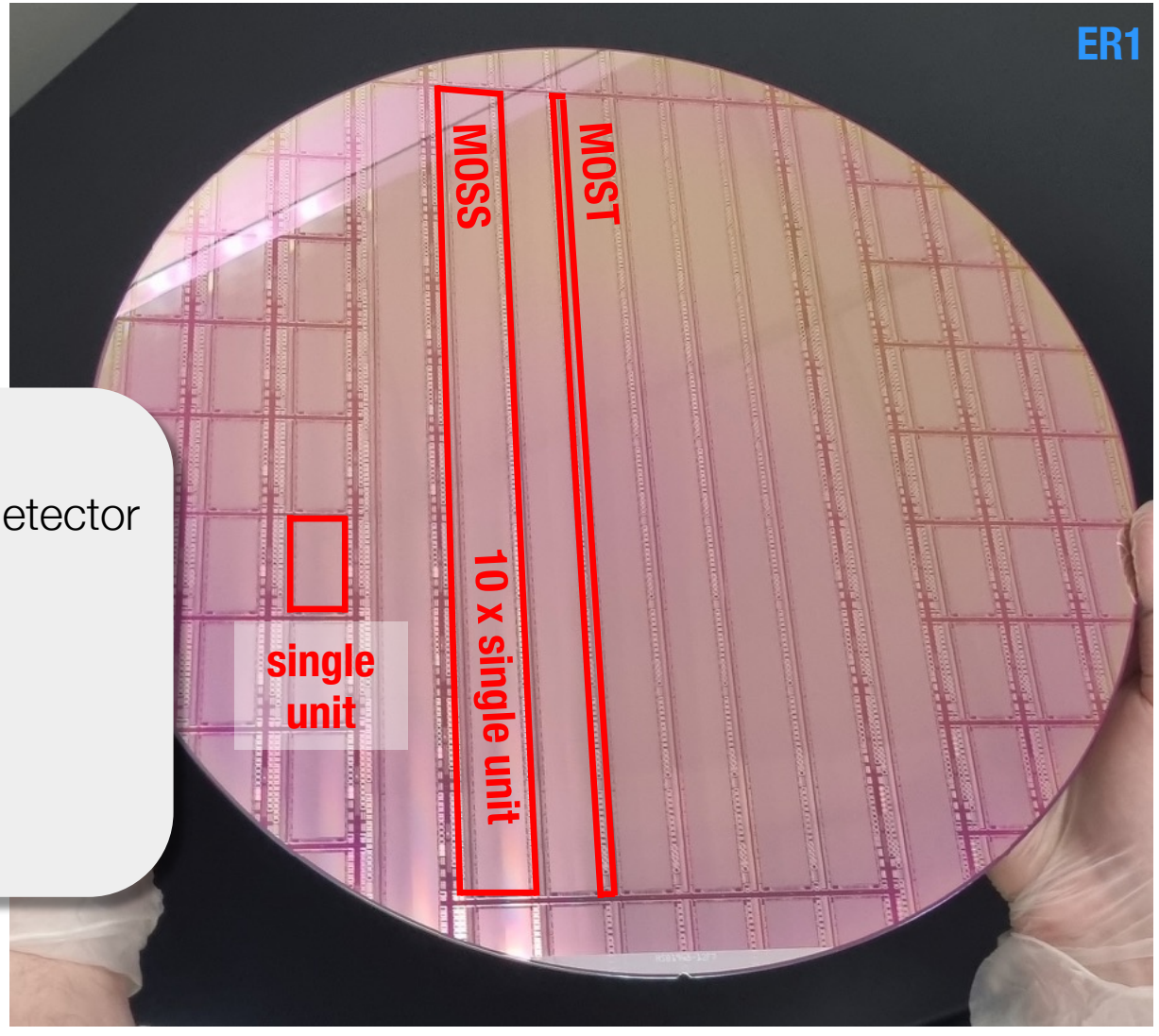
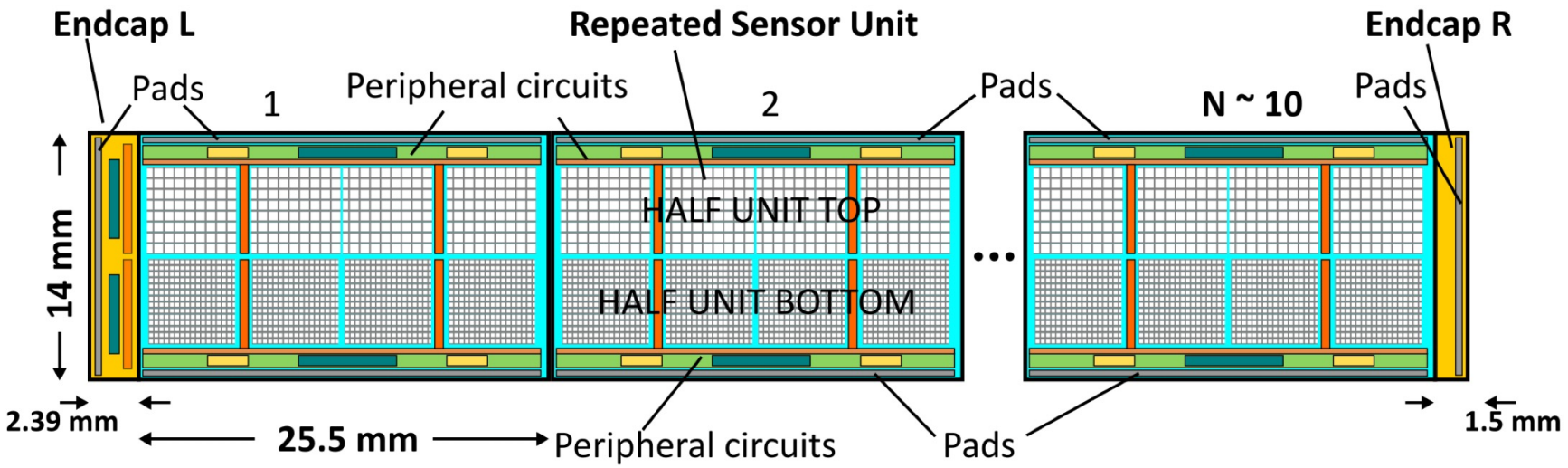
  - 18 x 18 μm^2
  - more dense design, different power granularity
- Si
- P

Required dedicated design effort:
- understanding **stitching** rules to make a particle detector
- redundancy, fault tolerance

Crucial exercise to understand:
- **yield**
- **possible defects**
- **uniformity**



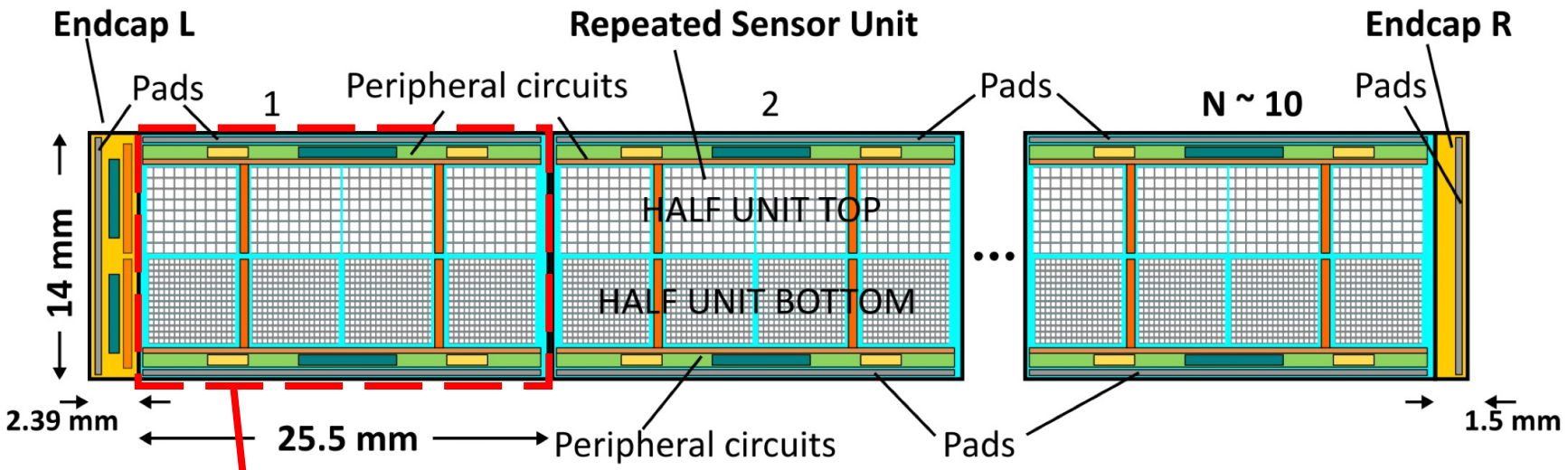
MOSS



10 Repeated Sensor Units (**RSUs**).
For every RSU:

- **Top and bottom** halves with **different pitches**
  - 22.5 μm → less compact layout, 256x256 pixels
  - 18 μm → compact layout, 320x320 pixels
- For every half, **4** different regions with **different designs**

MOSS



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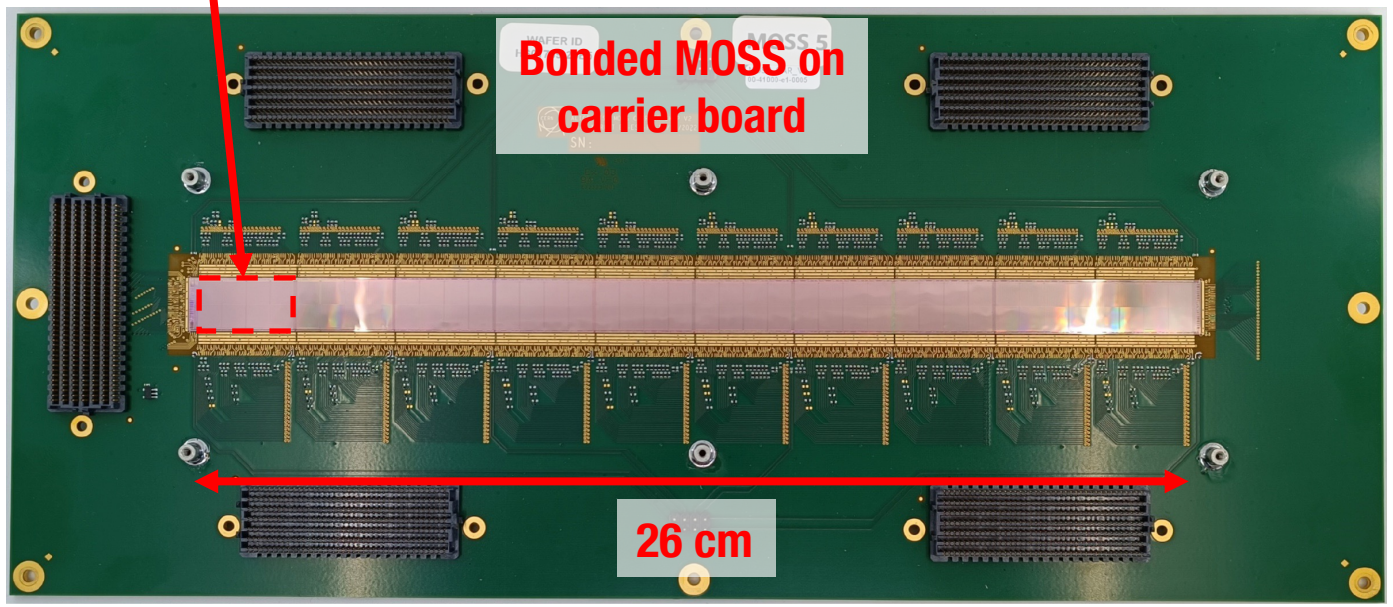


- Handling and picking understood for such a large chip
- 82 MOSS bonded on carrier board

MOSS – testing campaign

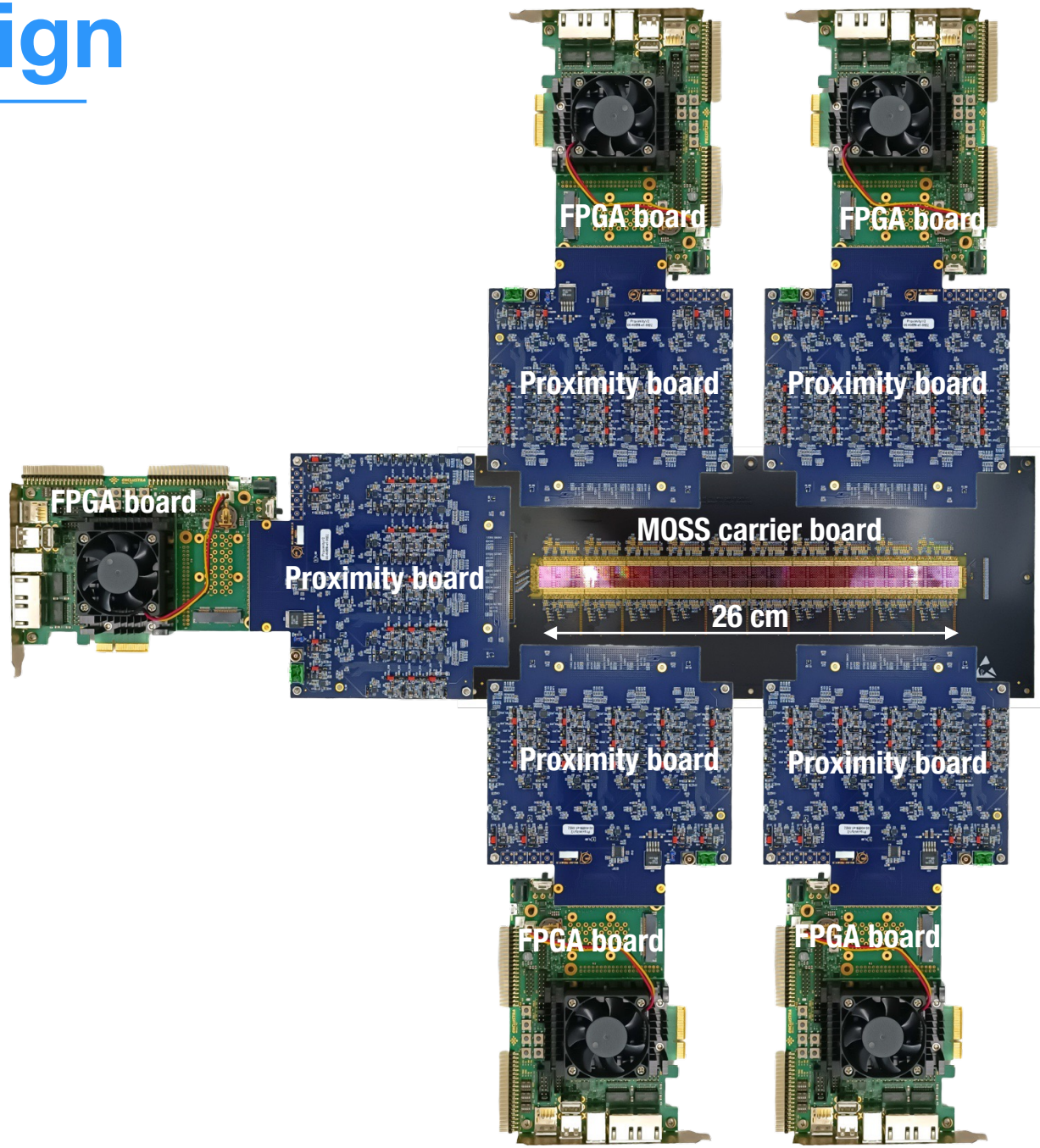
Comprehensive test of several sensors

Before picking and bonding on carrier:
- Wafer-probing

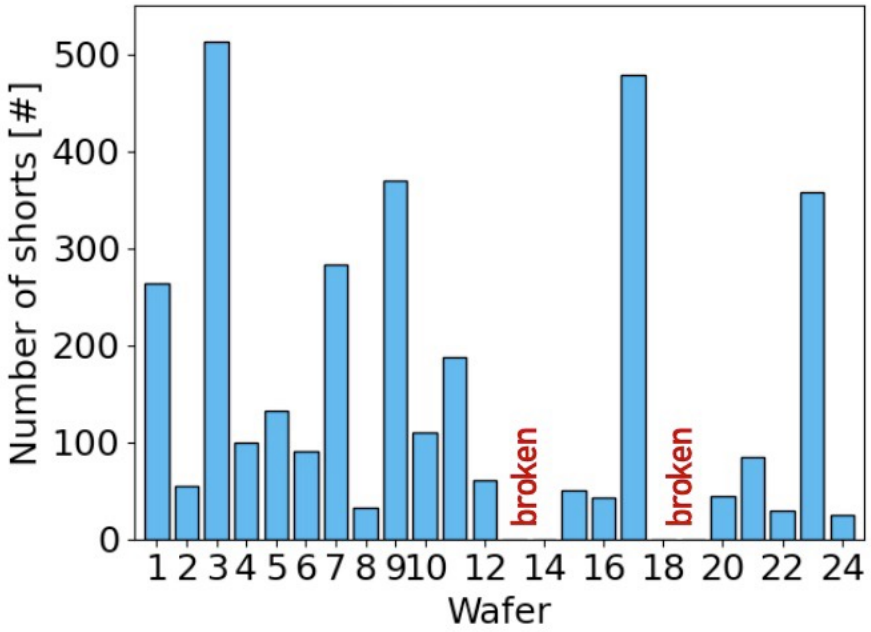
In laboratory, 3 main steps:
- Impedance tests between power nets
- Power ramp (slowly by domain) → using a thermal camera
- Functional tests

→ All to get yield, uniformity and performance

In beam tests:
- Performances in terms of efficiency and FHR



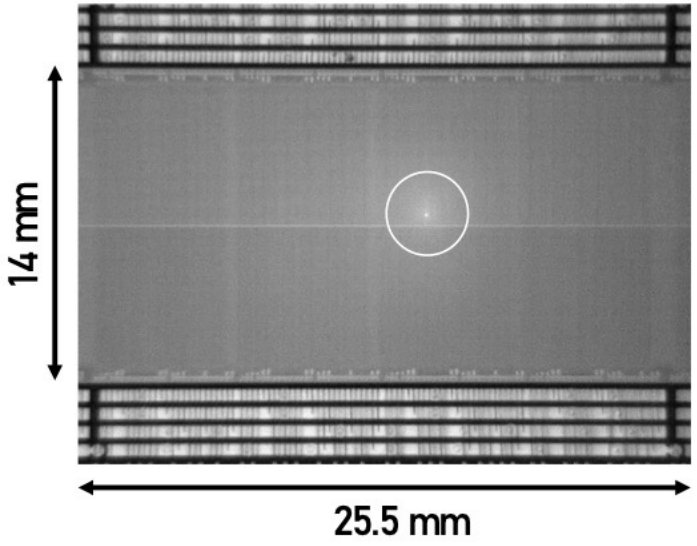
MOSS – powering yield



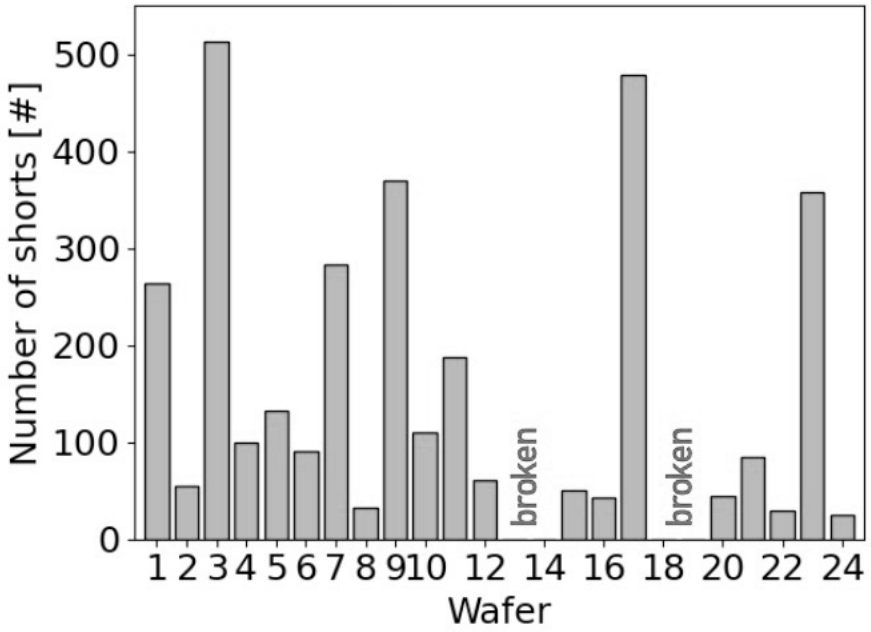
Large number of **shorts** observed during ramping:

- **Hotspot** appear
- Often they **disappear** after some time or voltage
- Position reconstructed O(50-100 μm)

Typical thermal camera image of an hotpsot



MOSS – powering yield



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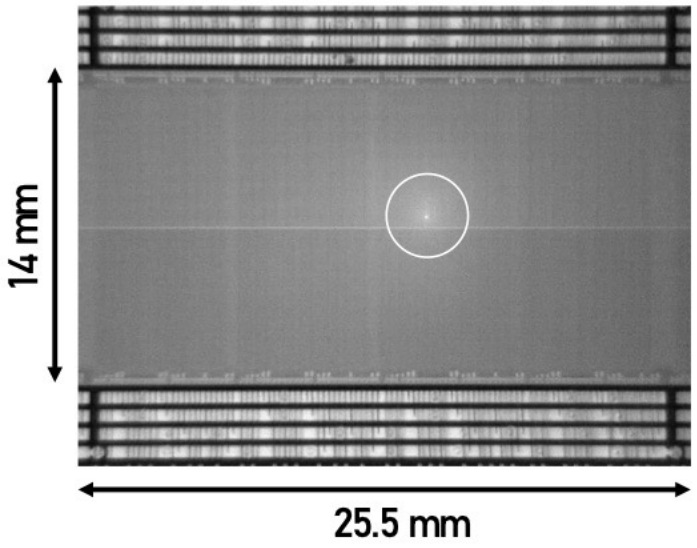
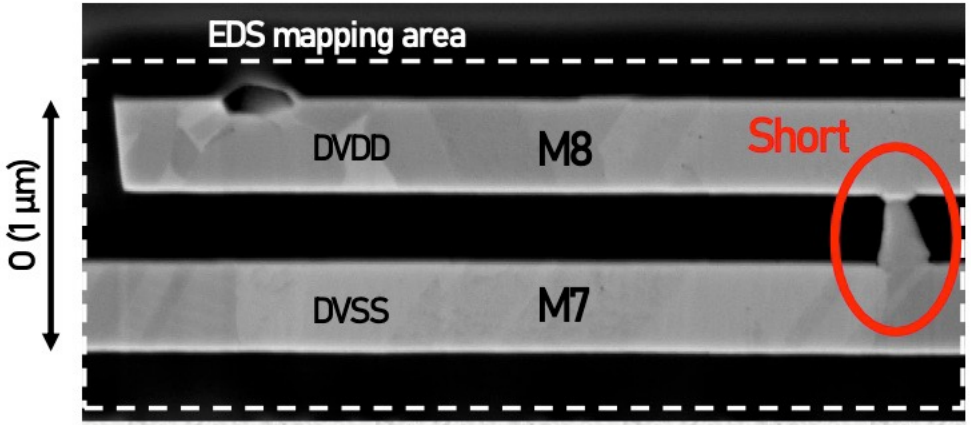




SEM cross section of the top two metal layers

Reason **understood**:

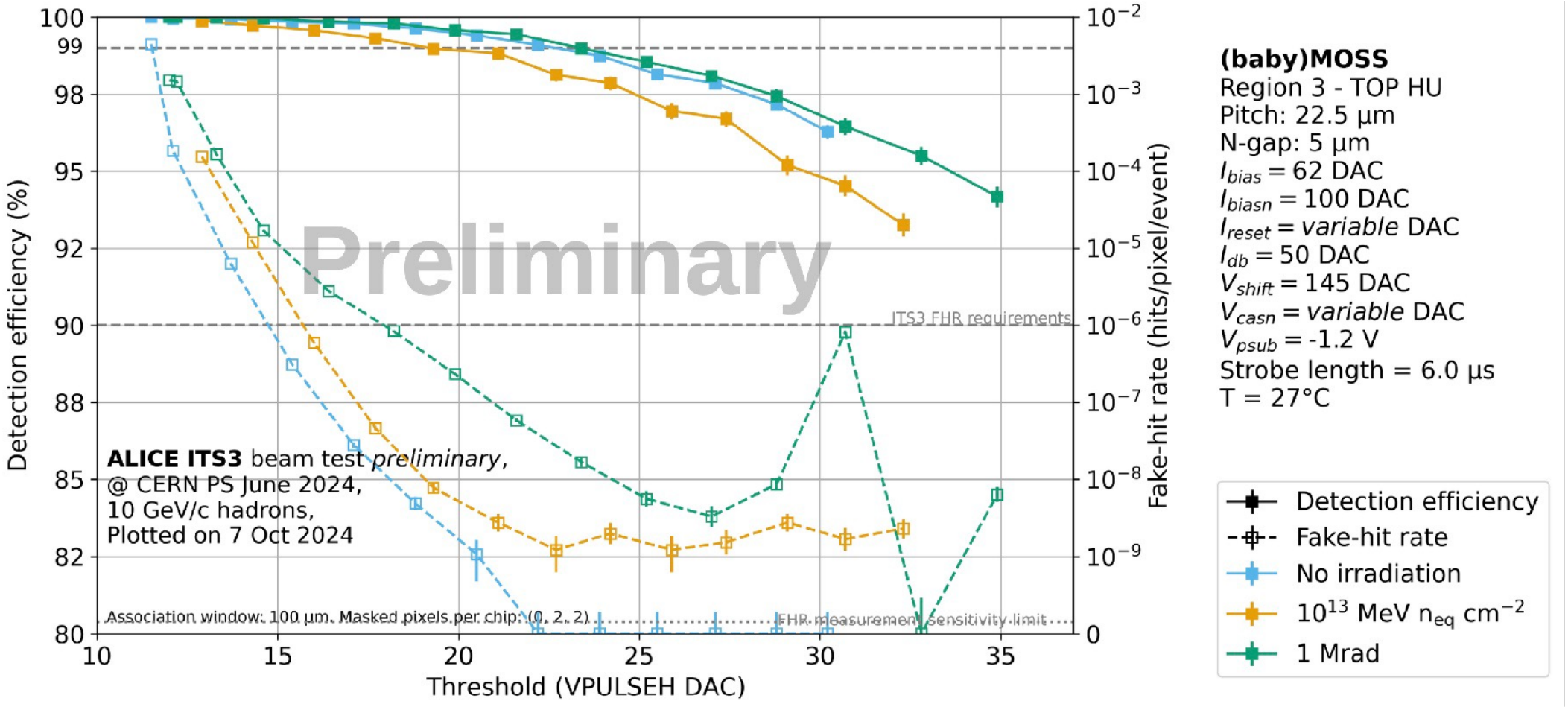
- Correlated with crossing of metal lines (design files) on the top two metal
- Communicated to foundry that confirmed the issue
- Will be fixed for future sensors

→ **Very important finding for the next submission in terms of yield!**

MOSS – beam test

Efficiency and FHR:

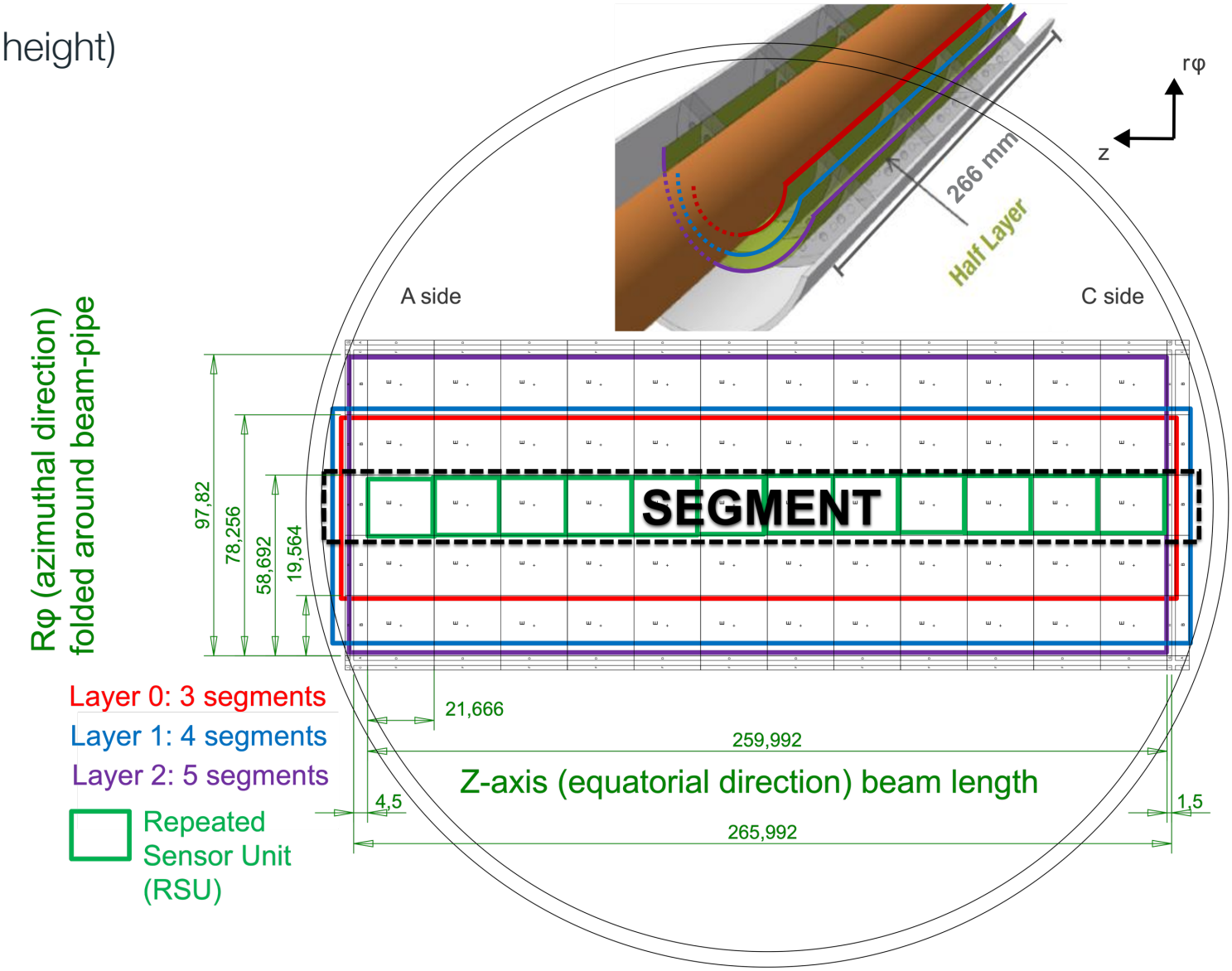
- Confirmation of expected performance from small-scale prototypes (MLR1)



MOSAIX: the final stitched wafer scale prototype

Engineering Run 2 (ER-2)

- Sensor divided in segments (20 mm sensor height)
- Pixel pitch: 20.8 x 22.8 μm^2
- 12 RSU per segment
- 12 different pixel/matrix variants per RSU
  - to fine tune operational margins
- Increased granularity of power network to selectively switch of malfunctioning parts
  - 144 units per segment (12x12)
  - for MOSS there were 20
- Submission foreseen for beginning of 2025



Conclusions

Upgrade of the ALICE Inner Tracking System, ITS3. Aim at truly cylindrical wafer-scale MAPS sensors
Ultimate vertex detector. Installation of new inner layers for LHC LS3 in 2026-2029.

Ultra light detector mechanics and cooling estabilished
Using carbon foam for support and air cooling

65 nm sensor design validated
Improved charge collection efficiency with new design, 100% detection efficiency reached and radiation hardness higher than what needed

Silicon flexibility and bending proved
Full mock-up of the final ITS3 done, uniform performances among different radii

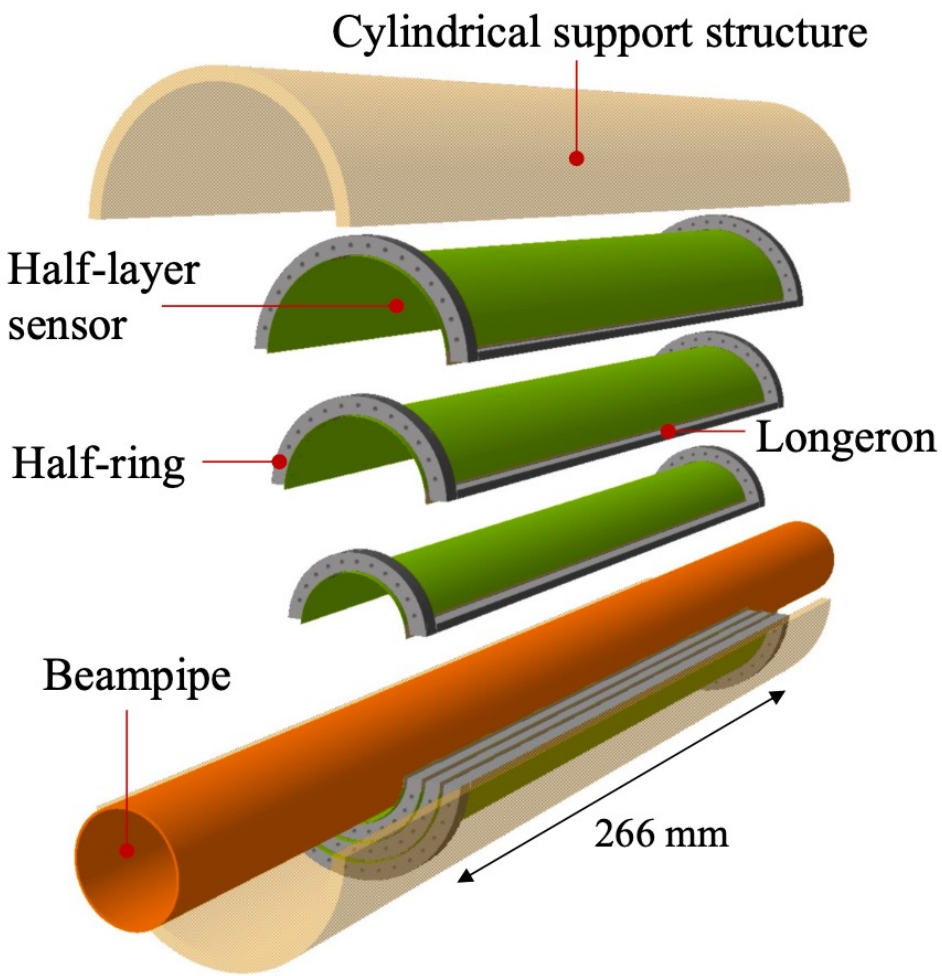
First stitched MAPS in 65 nm done. The chips work and the performance met the requirements
Yield studied and faulty found and understood, test beam performance excellent. Fundalmental step for increasing yield in next submission

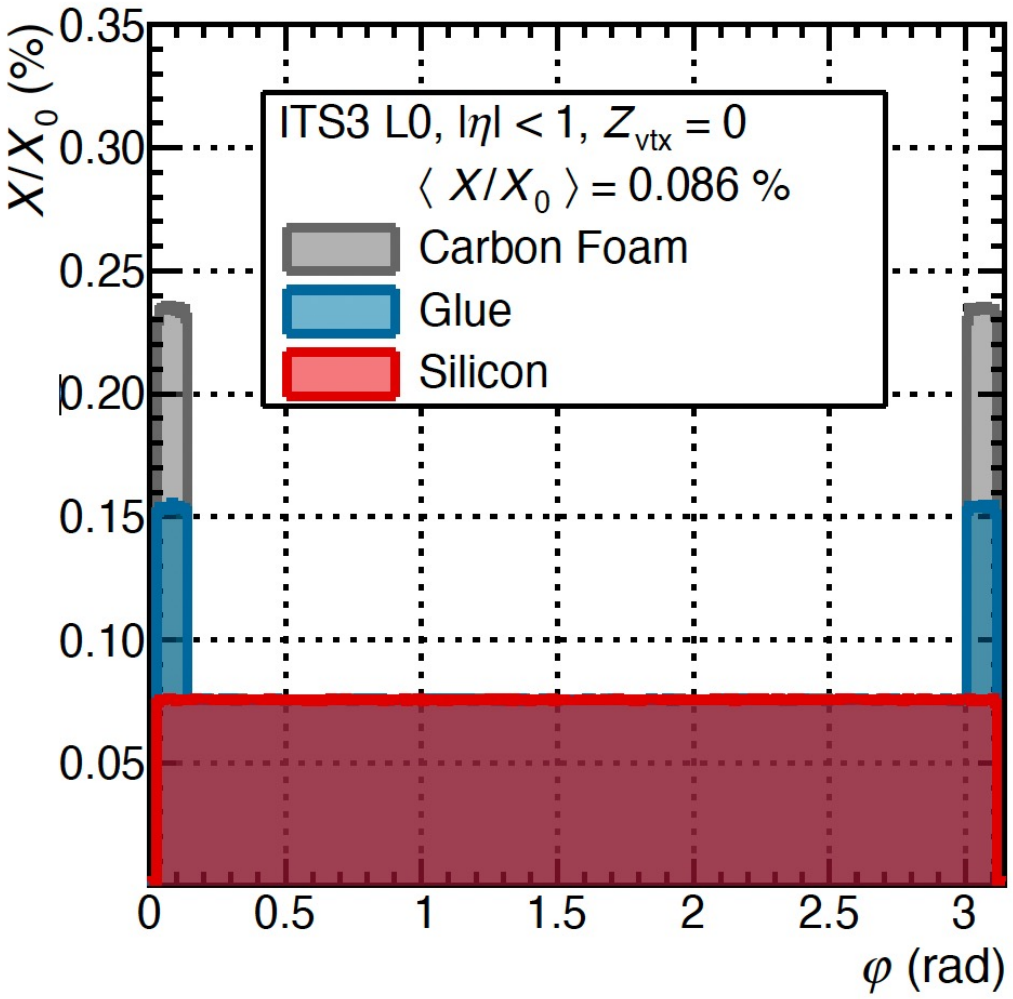
Next step: MOSAIX, the final sensor prototype for ITS3
Sensor expected for summer 2025

Backup

Material budget

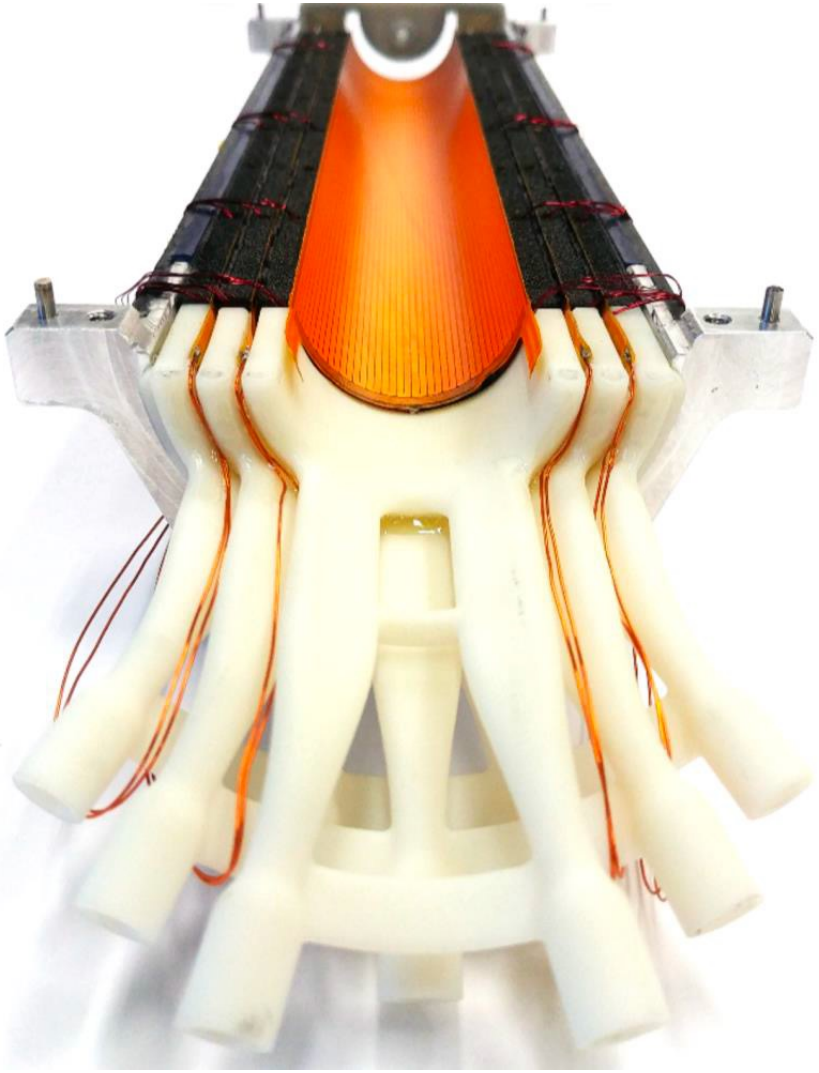
ITS3 TDR, CERN-LHCC-2024-003, https://cds.cern.ch/record/2890181

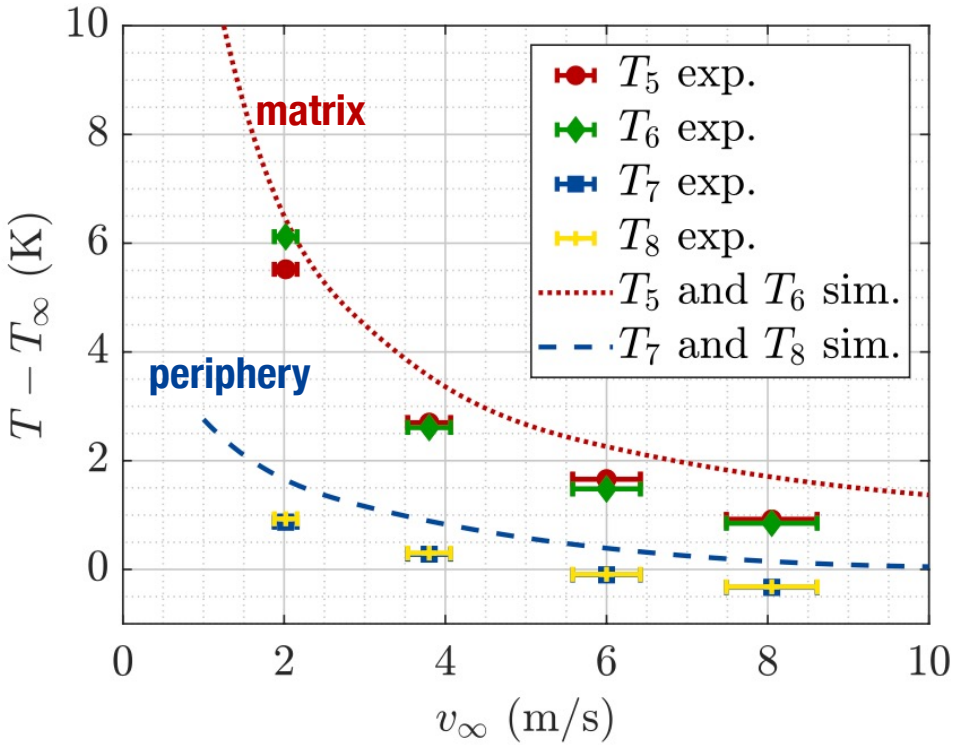




Air cooling – Thermal performance

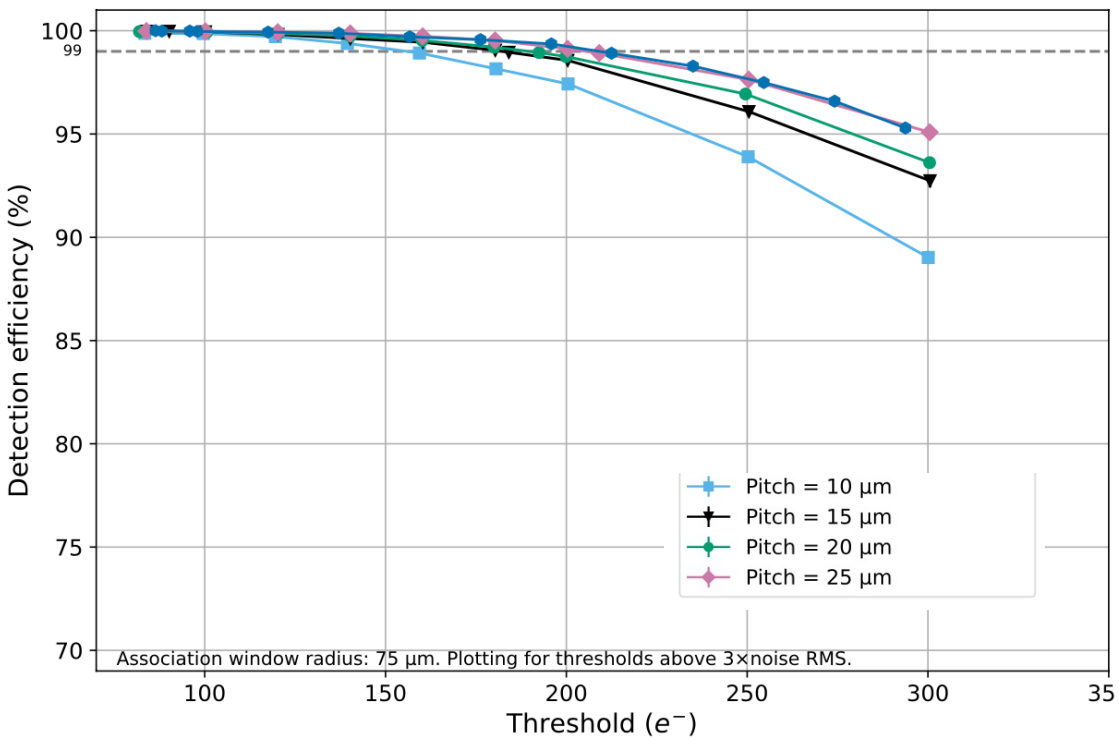
Si and Polyimide sandwich
copper serpentines embedded

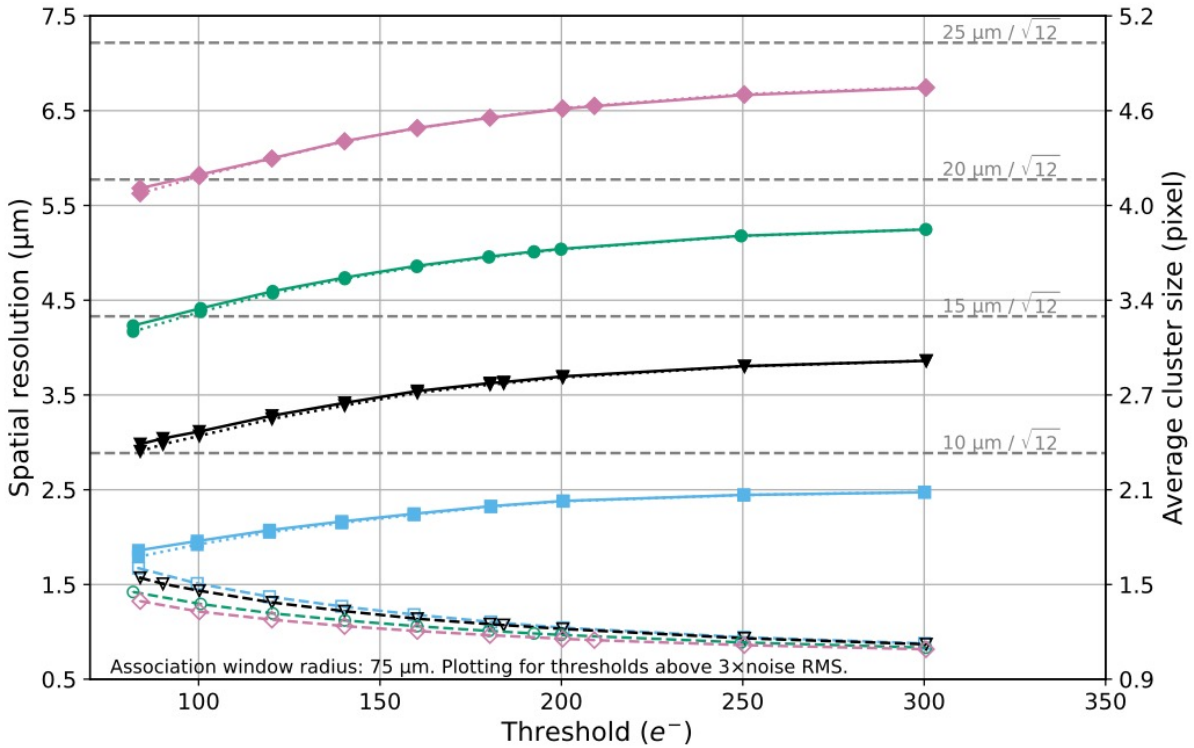




MLR1 efficiency – Modified with gap

https://doi.org/10.1016/j.nima.2024.169896





ITS3 - Flexibility of silicon

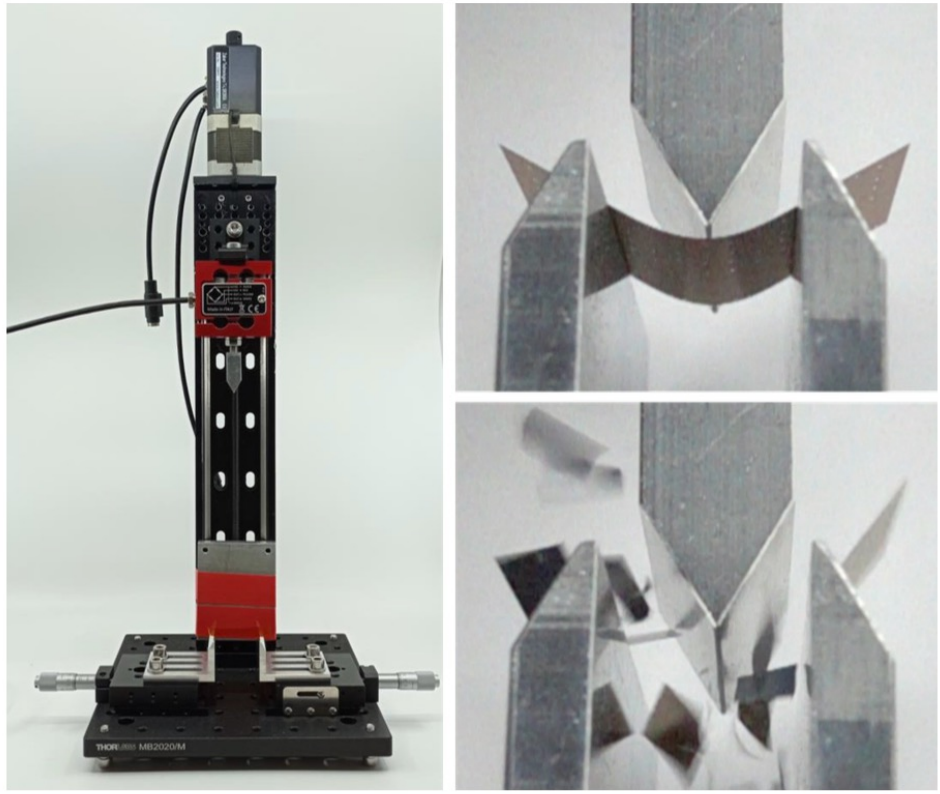
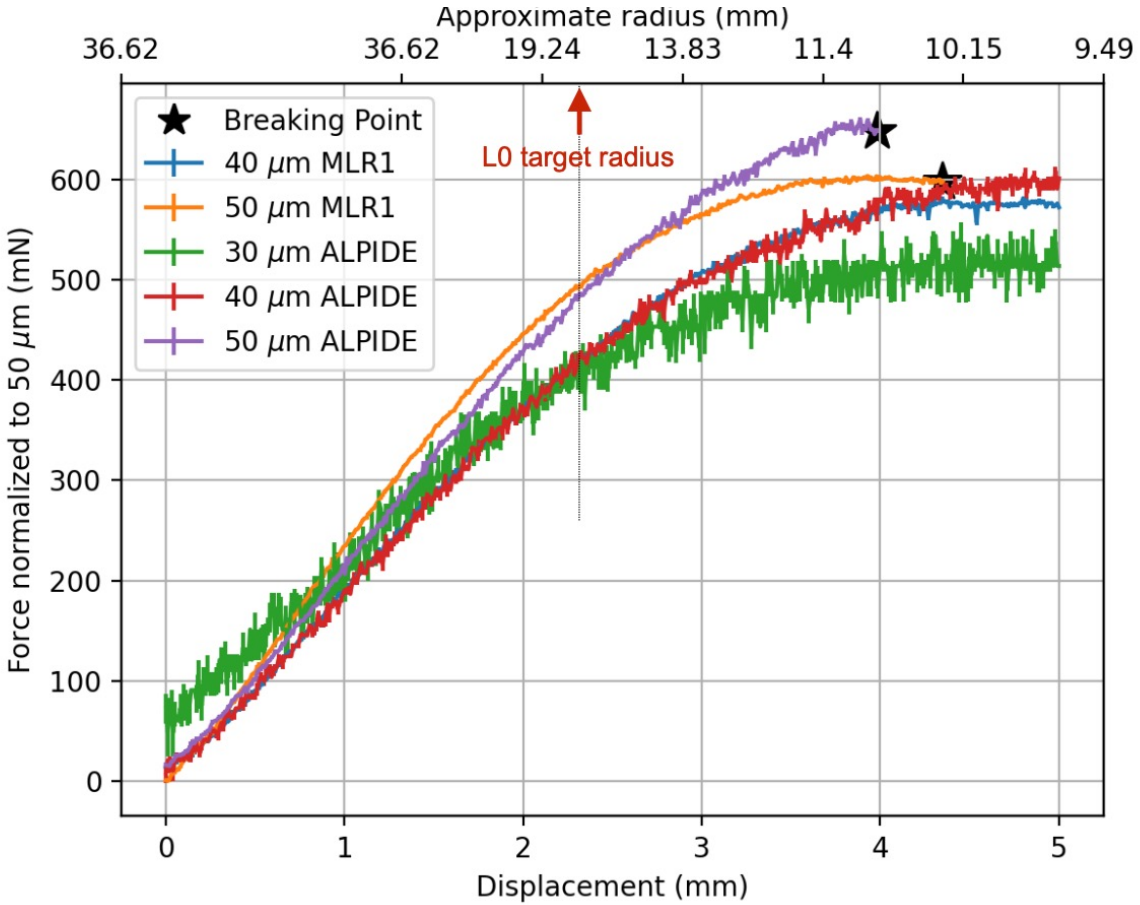


Figure 4.40 Setup for the bending strength measurements



- Bending force scales as (thickness)$^{-3}$
- Radii of 1.8 cm are easily reached

Physics Performance

ITS3 Physics Performance study, https://cds.cern.ch/record/2868015

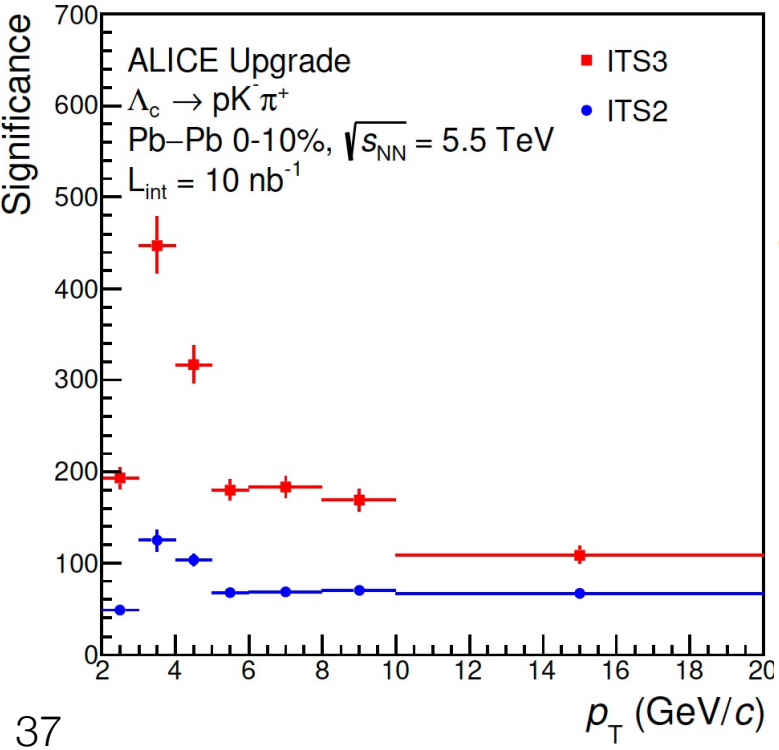
ITS3 TDR, CERN-LHCC-2024-003, https://cds.cern.ch/record/2890181

- Pointing resolution improved of a factor 2 → improved separation of secondary vertex

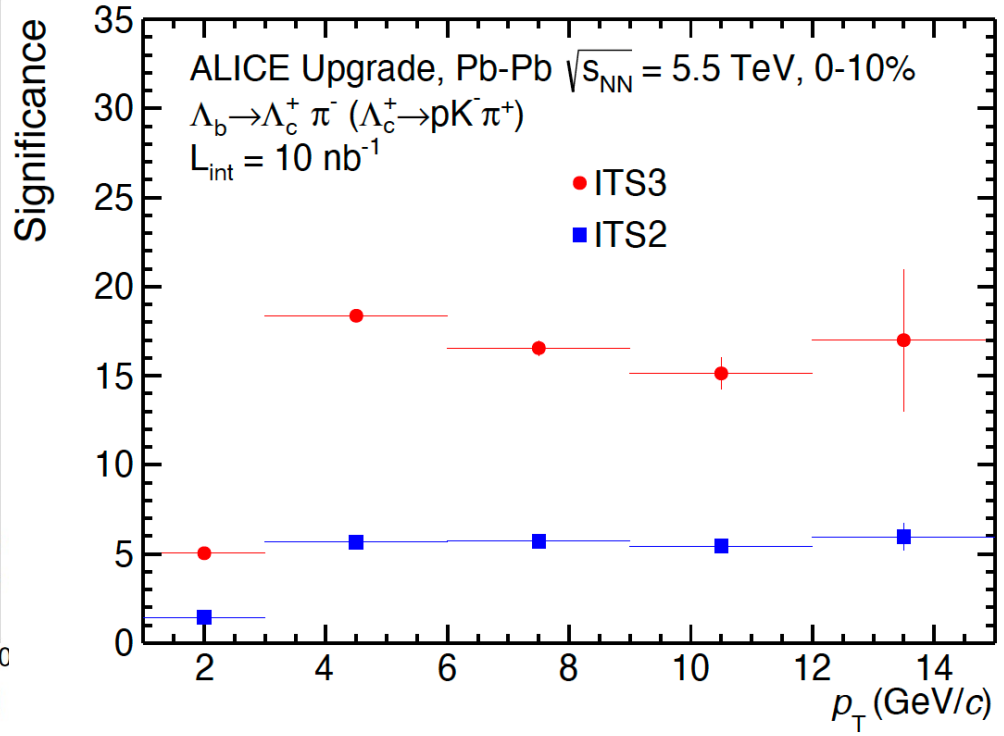
- Many observable strongly benefit or becoming in reach:
  - Charmed and beauty baryons
  - Low-mass di-electrons
  - Full topological reconstruction of B_s

Red = ITS3
Blue = ITS2

Λ_c significance



Λ_b significance



B^0_S significance