Upgrade of the Belle II Vertex Detector with Depleted Monolithic CMOS Active Pixel Sensors

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on behalf of the Belle II VTX collaboration

6th International Workshop on Future Tau Charm Facilities (FTCF2024-Guangzhou)
November 19, 2024

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Outline

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2. The current Vertex Detector (VXD)
3. The VTX Upgrade Proposal
4. The TJ-Monopix2 chip
5. The OBELIX sensor : **O**ptimized **Belle**2 p**IX**el sensor
6. Conclusions

VTX collaboration

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IPMU, Kashiwa
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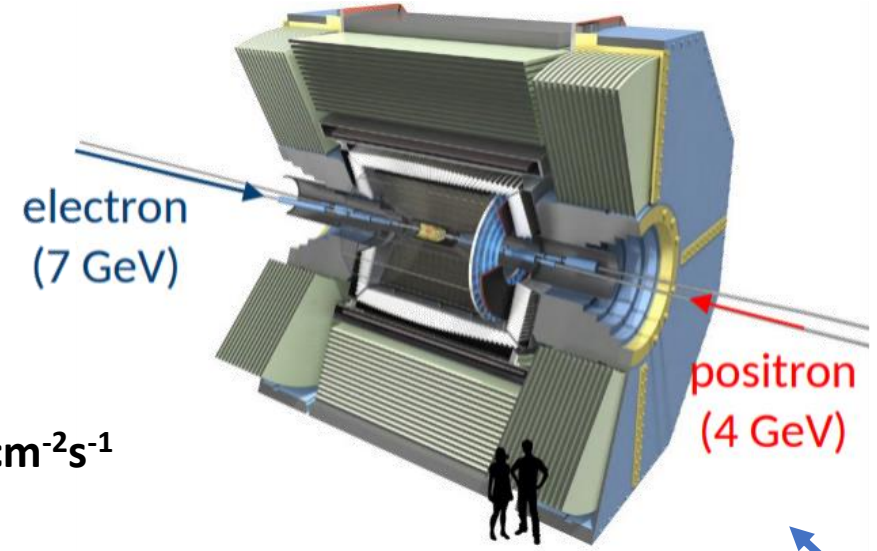
IGFAE, Barcelona
University of Bergamo
University of Bonn
University of Dortmund
University of Göttingen

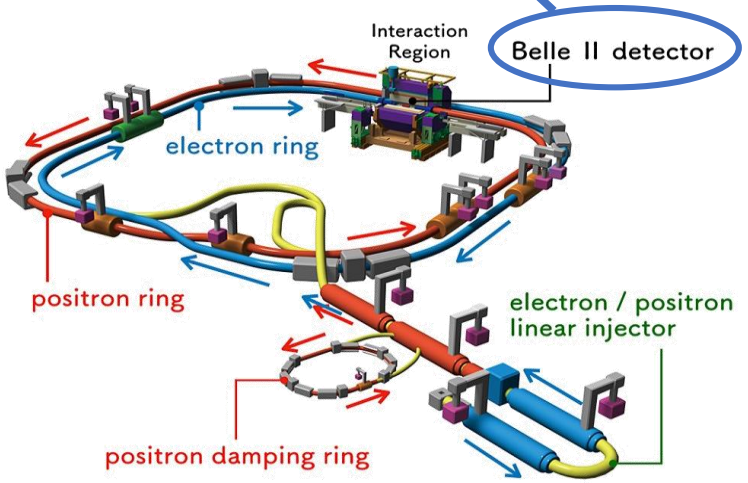
IJCLab, Orsay
RAL, Oxford
INFN & University of Pavia
INFN & University of Pisa
IFCA (CSIC-UC), Santander

IPHC, Strasbourg
University of Tokyo
KEK, Tsukuba
IFIC (CSIC-UV), Valencia
HEPHY, Vienna

The Belle II Experiment

- Located at the SuperKEKB collider in Tsukuba,Japan
- Asymmetric e^+- e^- collider at 4 / 7 GeV and $\sqrt{s}$ = 10.58 GeV
- Luminosity frontier experiment, exploring new physics
- Target instantaneous luminosity of **6×10^{35} cm^{-2}s^{-1},** currently **0.47×10^{35}cm^{-2}s^{-1}**
- Target integrated luminosity of **50 ab^{-1},** currently **0.43 ab^{-1}**
  - Machine related beam background will increase with high luminosity
  - Efficiency, resolution and performance of data tracking could degrade with higher occupancy from background
  - Extrapolation to this target luminosity has large uncertainty and limited safety margins





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The Belle II Upgrade Motivations

- An upgrade of the machine elements and the detector's **interaction region (IR)** is required:
  - To cope with the higher luminosity provided by the SuperKEKB accelerator
  - To improve detector robustness against high backgrounds
  - To provide larger safety factors for running at higher luminosity
  - To increase longer term subdetector radiation resistance
  - To improve overall physics performance
- A **long shutdown** is foreseen around early 2030 and provides the opportunity to install an upgraded detector

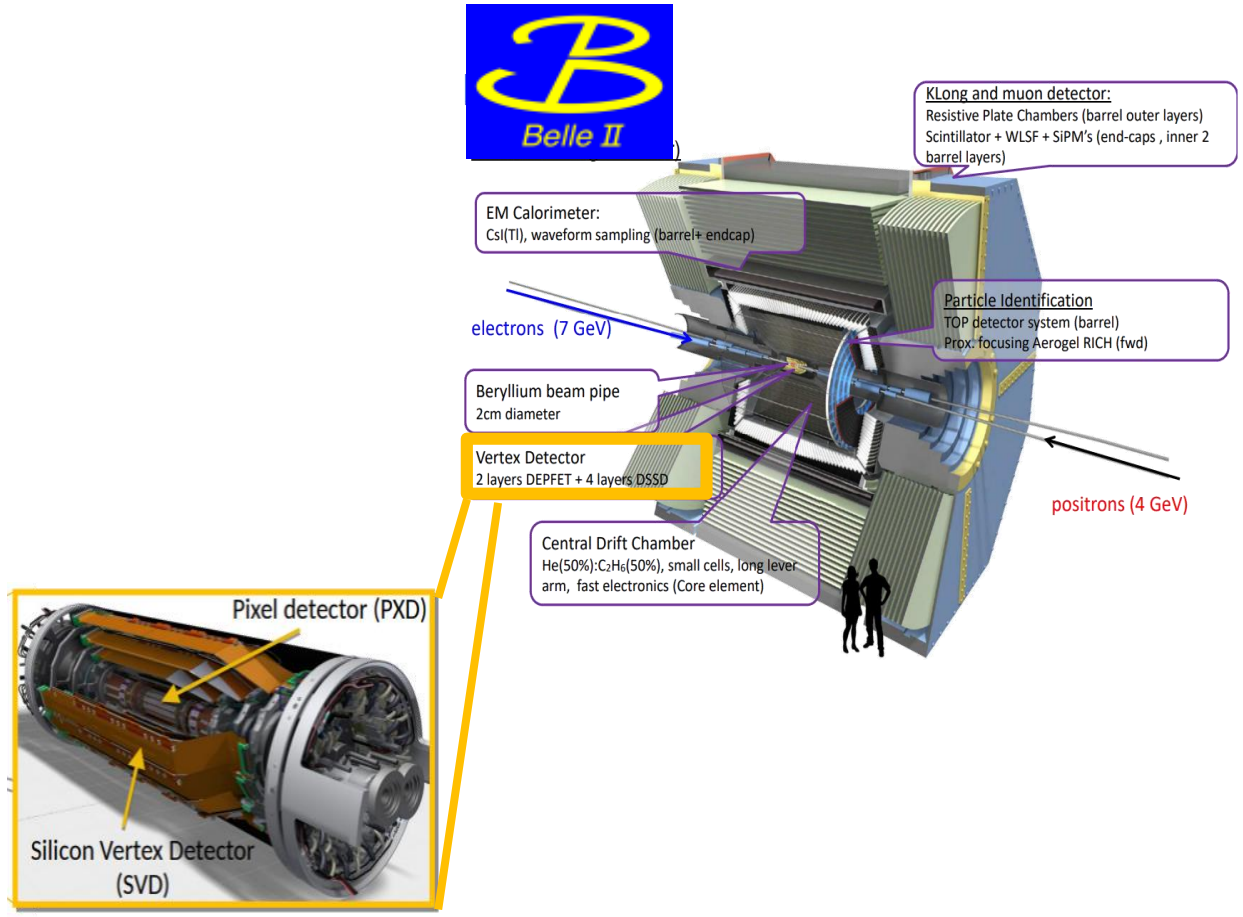
➡ **A new vertex detector concept VXD is proposed**

The Current Vertex Detector (VXD)

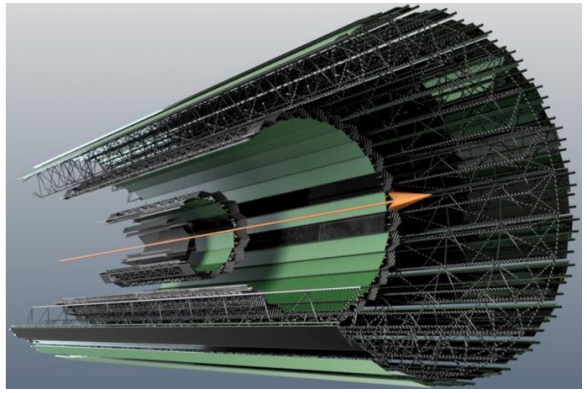
- Current VXD performance good and operating with low background occupancy < 1 %
  - Well below limits: PXD~3%, SVD~5%

- Two different technologies compose the VXD:
  - Pixel Detector (**PXD**)
    - Two layers of DEPFET pixel sensor
    - Material budget: 0.25 % X0 / layer
    - Pixel pitch: 50 to 75 µm
    - Integration time of 20 µs

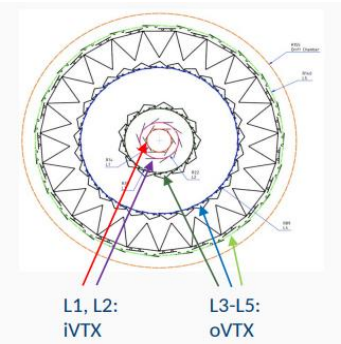
  - Silicon Vertex Detector (**SVD**)
    - Four layers of double sided silicon strip sensor
    - Material budget: 0.75 % X0 / layer
    - Up to 12 cm long strips
    - Time resolution of 3 ns



The VTX Upgrade proposal



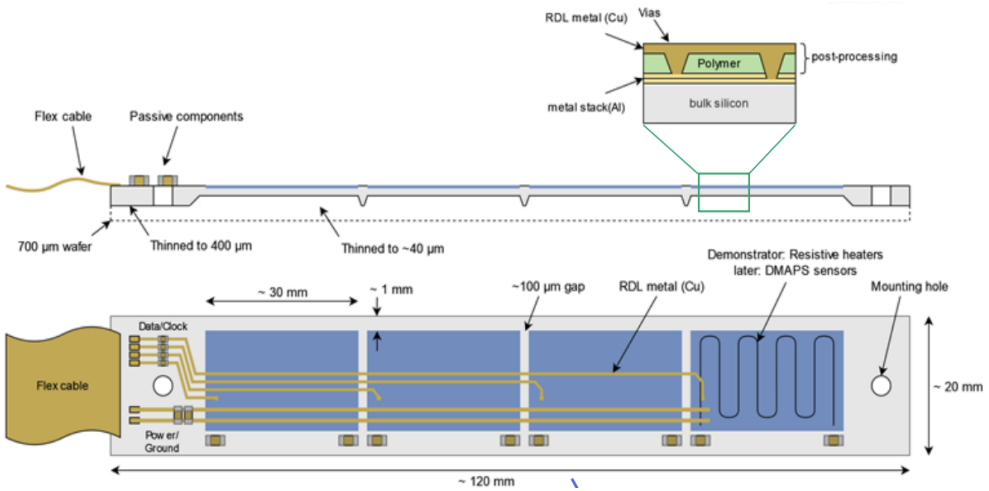
- A new fully pixelated CMOS detector to replace the VXD ➡ VTX
- Improved tracking resolution and space-time granularity
- Reduced material budget ≈ 2%X0 instead of 3.8%X0 (sum of all layers)
- 5-6 straight layers with **D**epleted **M**onolithic **A**ctive CMOS **P**ixel **S**ensors (**DMAPS**) process
- L1 and L2 (iVTX)
  - All silicon ladders
  - Air cooling (constrains power)
- L3 to L5 (oVTX)
  - Carbon fiber support frame
  - Cold plate with liquid cooling



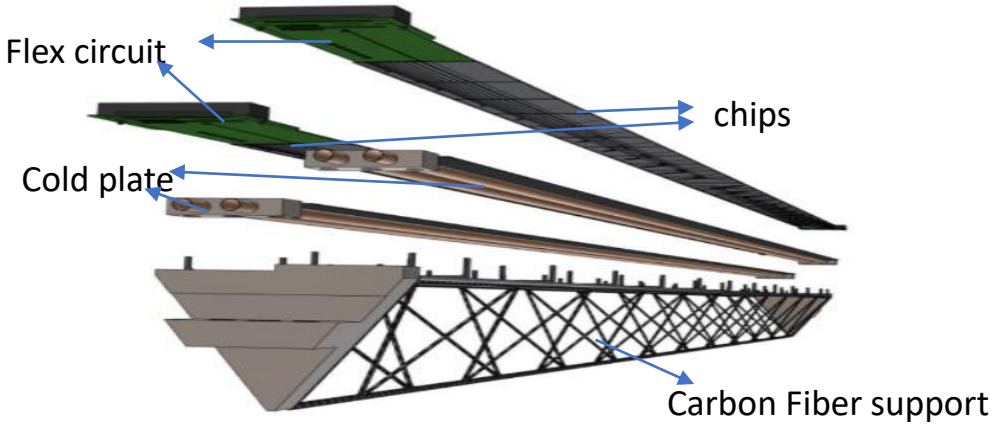
	L1	L2	L3	L4	L5	Unit
Radius	14.1	22.1	39.1	89.5	140.0	mm
# Ladders	6	10	17	40	31	
# Sensors	4	4	7	16	2 x 24	per ladder
Expected hitrate*	19.6	7.5	5.1	1.2	0.7	MHz/cm^2
Material budget	0.2	0.2	0.3	0.5	0.8	% X_0

The VTX detector mechanics

- iVTX Inner Layers Concept:
  - 4 contiguous sensors diced as a block from the wafer
  - Flex print cables
  - Redistribution layer for interconnection
  - Heterogeneous thinning for thinness and stiffness



Schematic view of the iVTX ladder design

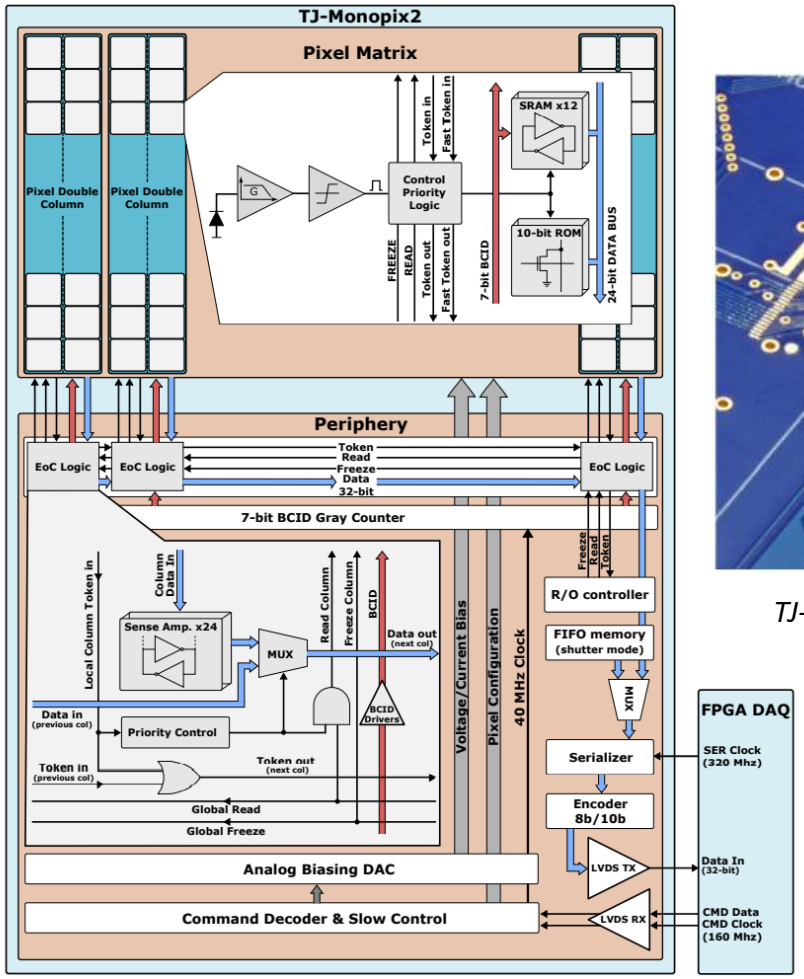


Exploded view of the oVTX

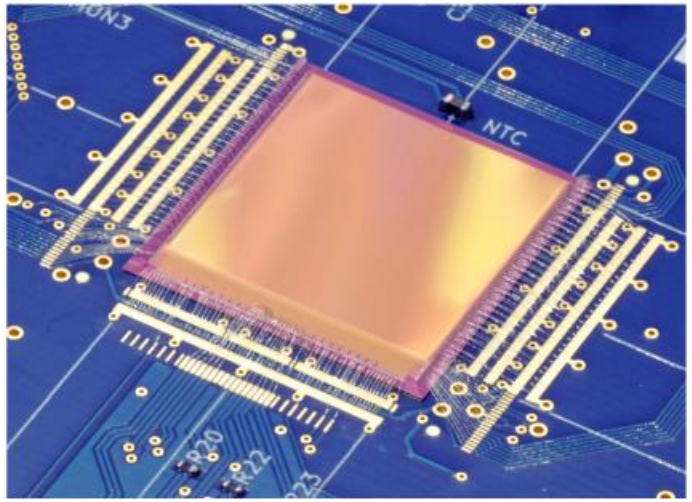
- oVTX Outter Layers Concept:
  - Ladder structure design inspired by ALICE ITS2, composed of:
    - Carbon Fiber support structure (truss)
    - Cold-plate with pipes for liquid coolant circulation
    - Chip and Flex circuit for power and signal glued on top

- A same monolithic CMOS pixel sensor chip for all layers : **Optimized Belle II pIXel sensor (OBELIX)**

The TJ-Monopix2 (TJM2) as prototype



Chip architecture of TJM2



TJ-Monopix2 sensor bonded on a test board

- Developed for ATLAS experiment
  - FE derived from ALPIDE
  - 4 FE flavors
  - Column-drain R/O architecture
- DMAPS **Tower Semiconductor 180 nm CMOS**
- 2×2 cm² chip: 512×512 pixels
- Pixel pitch: 33.04×33.04 µm²
- Expected from design (simulations):
  - ~ 100 e− min. threshold
  - 5-10 e− threshold dispersion (tuned)
  - >97% efficiency at 10^{15} n_{eq}/cm²
  - ~ 5 e− noise
  - Fully efficient with hit rate 120 MHz/cm²
  - Power: ~ 1 µW/pixel

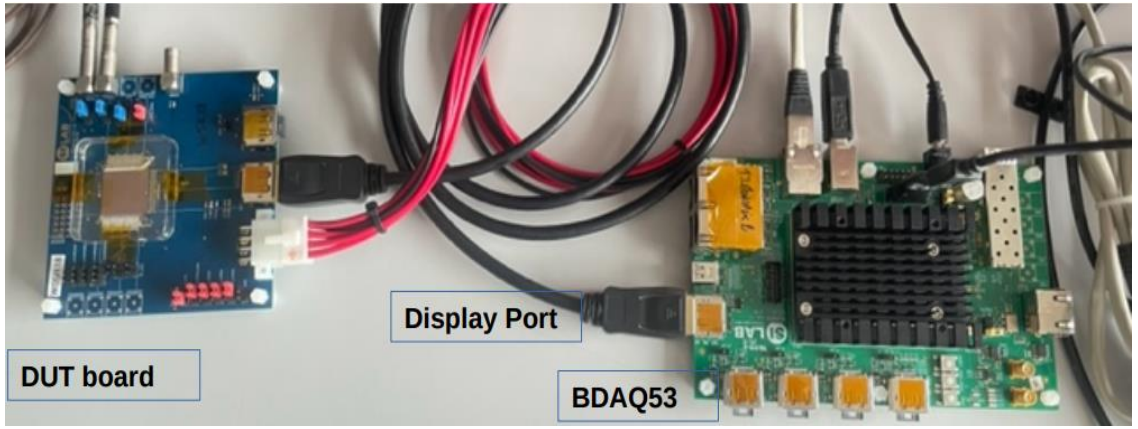
Base-line option for OBELIX design

The TJM2 Testing

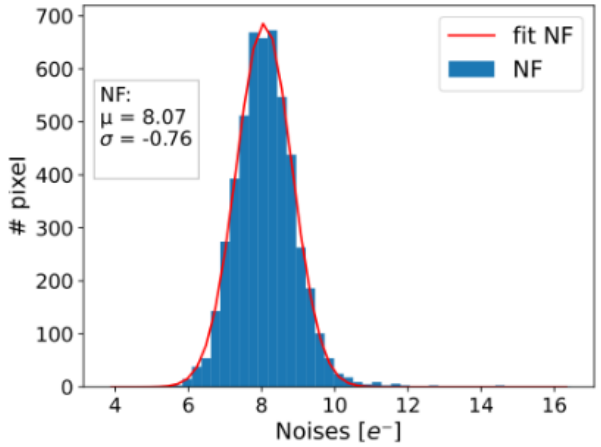
- Characterisation of TJ-Monopix2 (all FE) to validate key performance crucial for OBELIX design

- **Full characterisation** on bench:
  - Threshold scans (lowest value, dispersion)
  - Noise testing
  - ToT (Time Over Threshold) calibration

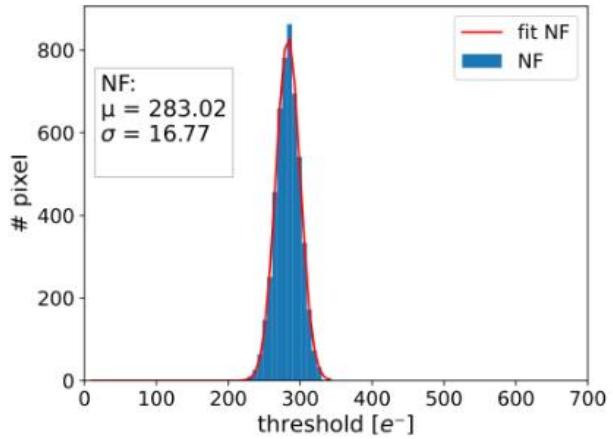
- Control and data acquisition system based on the BDAQ53 setup



TJM2 setup DAQ inherited from RD53 collaboration



Noise distribution



Threshold distribution.

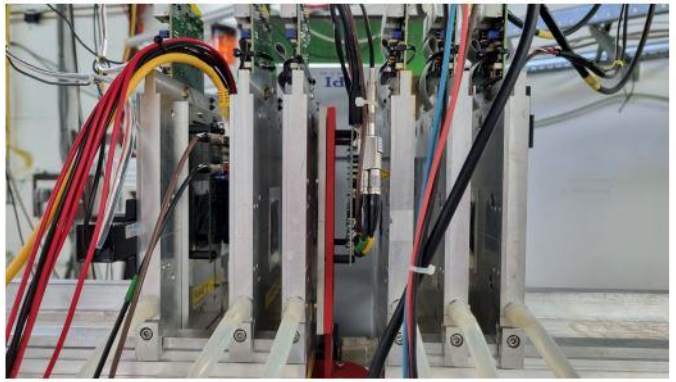
- Typical settings for operational threshold:
  - Thresholds between 200 to 300 e−
  - Average noise varies from 7 to 8 e−

- Time Over Threshold (ToT) calibration, Fe55

- Comparison with measurement and simulations
  - Measurement from monitoring pixels of the analog output signal after the FE amplifier

The TJM2 Testing

- **Full characterisation@DESY**:
  - Efficiency/Resolution measurements
  - Radiation hardness (NIEL and TID irradiation campaigns in progress)



Setup for testbeam – @Desy

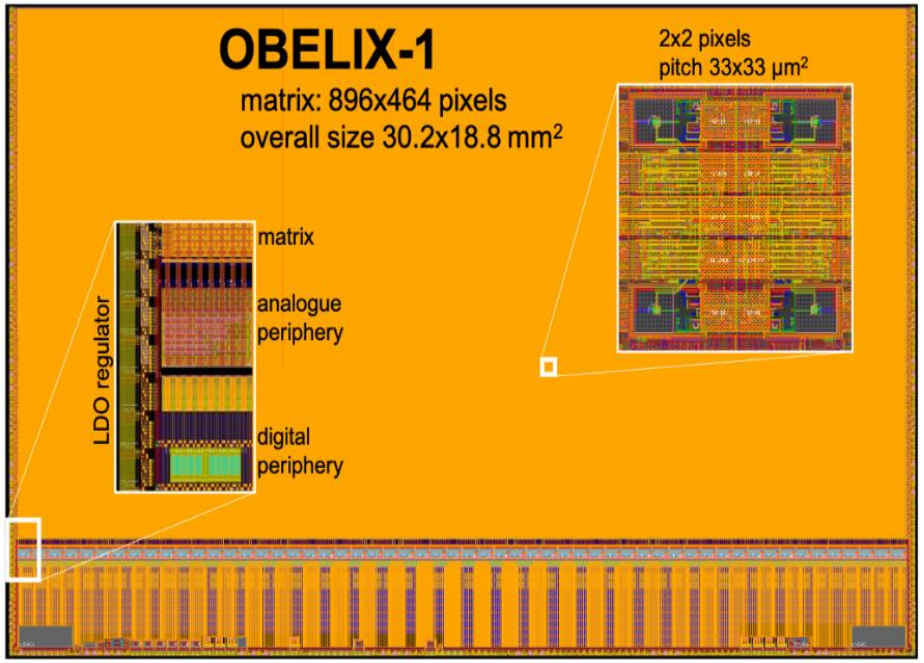
- **Several test beam campaigns (3-5 GeV e-)**
  - **July 2022:** Non-irradiated chips
    - High threshold (500 e-)
    - Hit efficiency ~ 99.54%, Cluster position residuals ~ 9 µm
  - **July 2023:** Irradiated chips at $5x10^{14}$ n_{eq}/cm^2
    - Lower threshold ~ 250-300 e-
    - Good performance and high efficiency
  - **July 2024:** Irradiated chips at $5x10^{14}$ n_{eq}/cm^2, TID of 100 Mrad
    - Good efficiency but temperature influence

Another test beam planned for 2025

The OBELIX Sensor

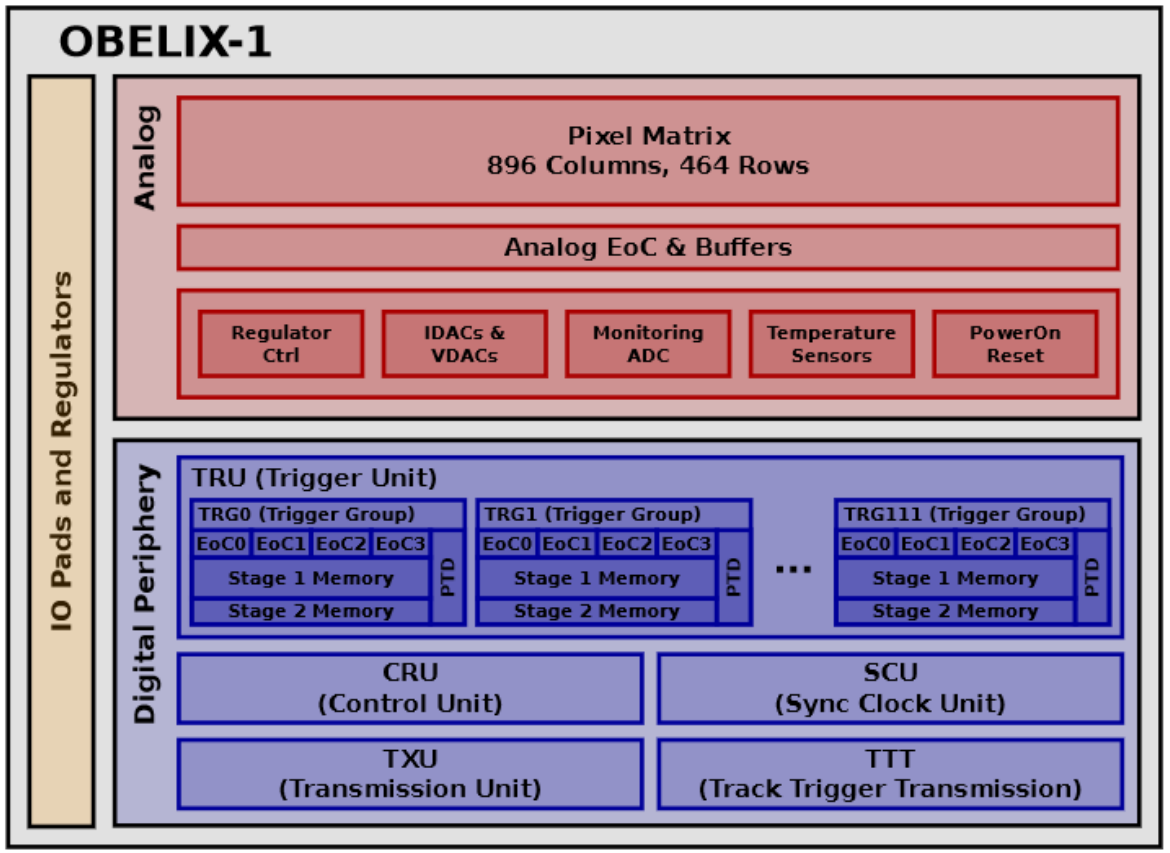
Sensor specifications:

- Tower Semiconductor 180 nm CMOS
- Hit rate up to 120MHz/cm²
- TID tolerance: 100 MRad
- NIEL tolerance: $5x10^{14}$ $n_{eq}/cm^2/year$
- Spatial resolution < 15µm
- Power < 200 mW/cm²
- Time precision < 100 ns
- Trigger at 30kHz average frequency with 5-10 µs latency



- 464 rows and 896 columns
- Overall sensor dimensions around 30.2x18.8 mm²
- Pixel pitch 33x33 µm²
- Main design is based on the **TJM2** chip

The OBELIX Block Diagram



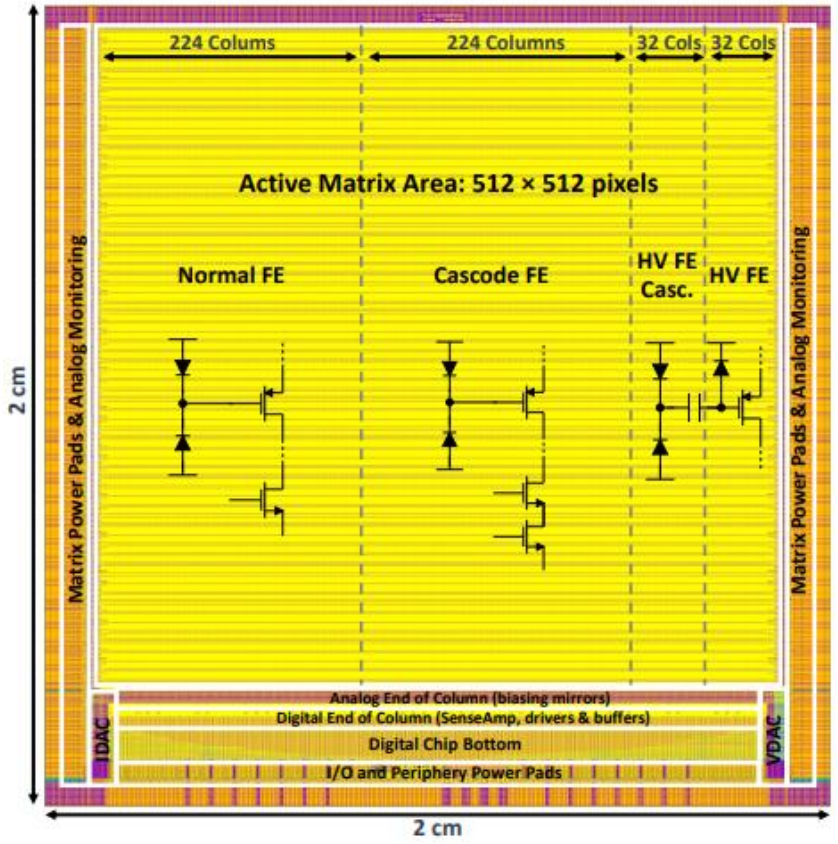
Analog
- Pixel matrix adapted from **TJM2**
- Column drain architecture
- Monitoring ADC
- Temperature sensors

Power pads
- Power regulators added
- Simplified system integration

Digital Periphery
- Main clk-in: 170MHz
- New end-of-column adapted to Belle II trigger
- Timestamped hits stored in memories
- Read-out when timestamp matched with trigger
- Single output at 340 MHz average bandwidth
- RD53 control/readout protocol

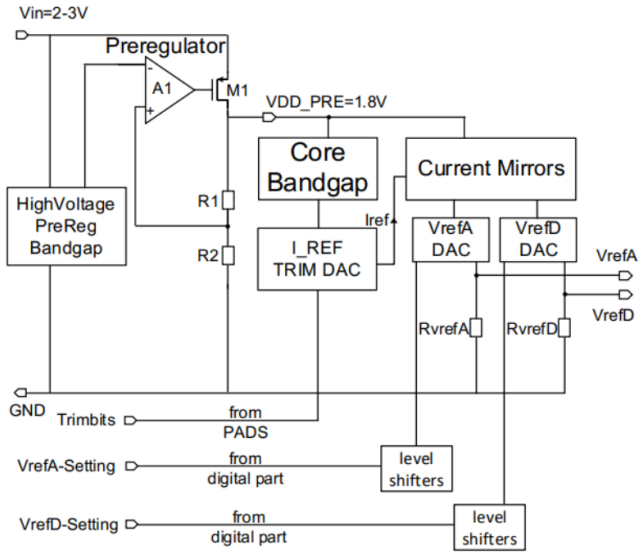
The pixel matrix of OBELIX

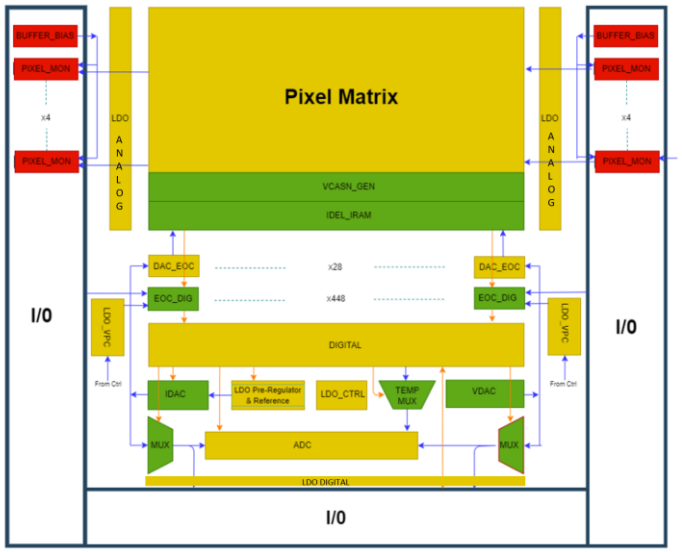
- The OBELIX sensor inherits the performance of the pixel matrix from TJ-Monopix2 sensor
- The same pitch, 33 × 33 µm², with the same layout for the analog and digital parts
- The Matrix pixel of TJ-Monopix2 is composed of 4 pixel flavors with differences in the Front-End (FE) amplifier and detector input coupling (AC or DC):
  - Normal FE / Cascode FE
  - HV Cascode FE / HV FE
- **Based on current characterization and simulation results, 2 FE flavors are chosen for OBELIX on equal area:**
  - **Cascode FE**
  - **HV Cascode FE**



Floorplan of TJM2 sensor

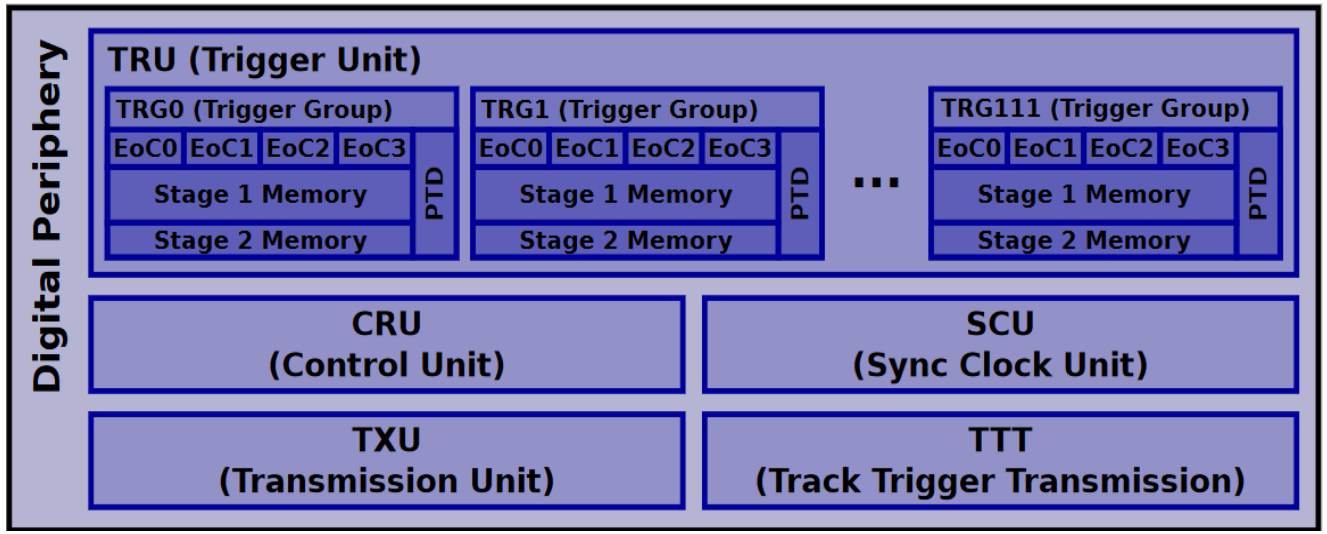
The OBELIX Power management





- Power distribution is a major concern as OBELIX is larger than TJ-Monopix2, leading to performance degradation
- Long linear ladders ⇒ voltage drop across ladder
- On chip regulators are being developed in OBELIX to compensate the voltage drop and minimize the material budget dedicated to power distribution:
  - Two analog **LDO (Low Dropout)** regulators will be implemented to supply the matrix from both sides
  - A digital LDO in the bottom side of the chip to supply the digital blocs
  - A preregulator to supply LDO references generator
  - A VPC (Voltage pre-charge) LDO to reset and recharge bit-lines between each read cycle
- The LDO generates the output voltage of 1.8 V ± 10% necessary for the technology to power the chip
- Wide input supply voltage range of 2V to 3 V

The Digital periphery of OBELIX



- Module division: 4 main parts
  - **SCU – sync & clk divider**: digital clk divider, synchronize circuit & clk divider, RxDat format conversion, main function: clock divider, Rx_data SIPO synchronization
  - **CRU – Control Unit**: Implementation RD53B interface, which almost keeps the same design as TJM2, main functions: command decoder, global configuration
  - **TRU – Trigger Unit**:Manage pixel data from the matrix-EOC and wait for the trigger to pick them for output
  - **TXU – TX Unit**: generate output data and sequential output, main functions: data framing, serializer

- New modules related to the Belle II trigger:
  - **TRU:** The Trigger Unit
    - Pixel readout, trigger processing
    - PTD: Periphery Time to Digital
  - **TTT:** The Track Trigger Transmission
    - Fast transmission in parallel to the Belle II trigger system

Conclusions

- The SuperKEKB collider is considering a major upgrade to reach a high luminosity
- Reaching the target peak luminosity requires an upgrade of the interaction region and the Vertex Detector
- A new DMAPS VTX is foreseen to improve the performance of the Belle II vertex detector
- The OBELIX sensor based on TJM2 chip with TJ180 nm technology is under development with additional features (all on-chip):
  - Voltage regulators
  - ADC and temperature sensors
  - Trigger logic, up to 10 µs latency at 120 MHz/cm²
  - Precision timing module
  - Fast transmission for trigger contribution
- Lab testing and TB campaigns on TJM2 to validate key performance crucial for OBELIX design
- Development and verification of OBELIX are entering the final stages
- Aiming submission of first version of OBELIX sensor in Spring 2025

Thanks for your attention

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