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R&D Progress of STCF MAPS-based Inner Tracker

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Outline

- MAPS-based Inner Tracker for STCF
- R&D of MAPS
  - Prototype chip design
  - Simulation of MAPS & ITKM
- Detector Module & Mechanics
- Conclusions

Super Tau-Charm Facility

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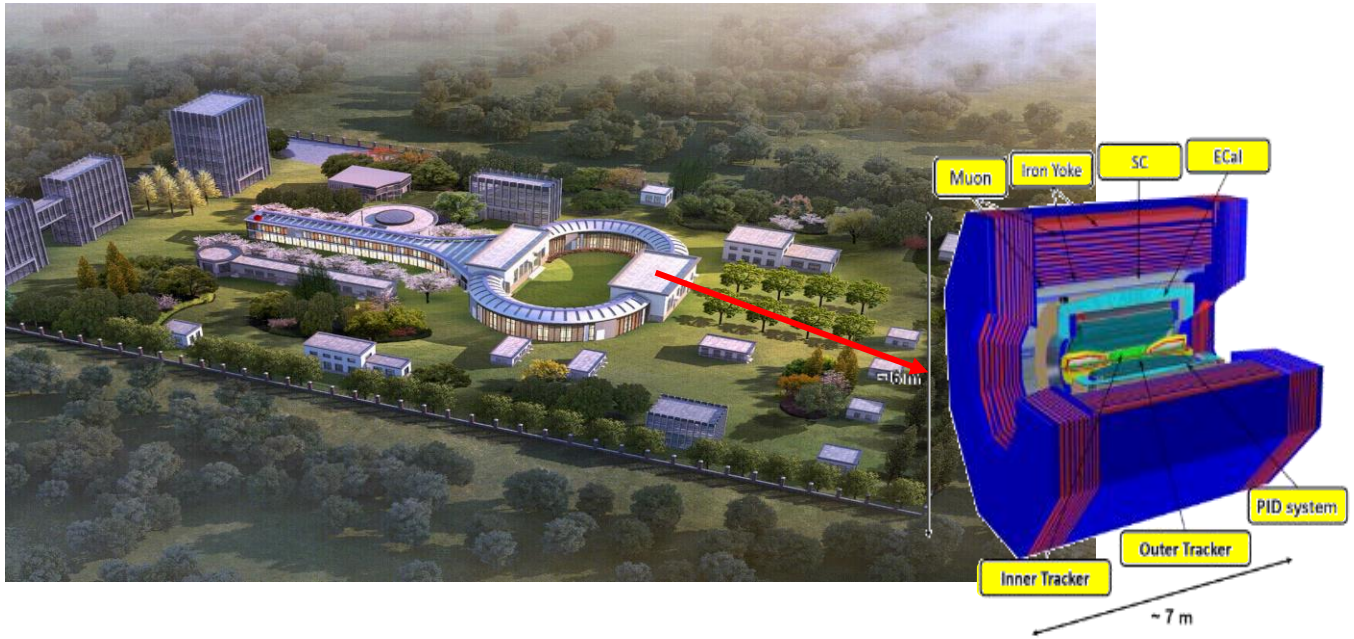
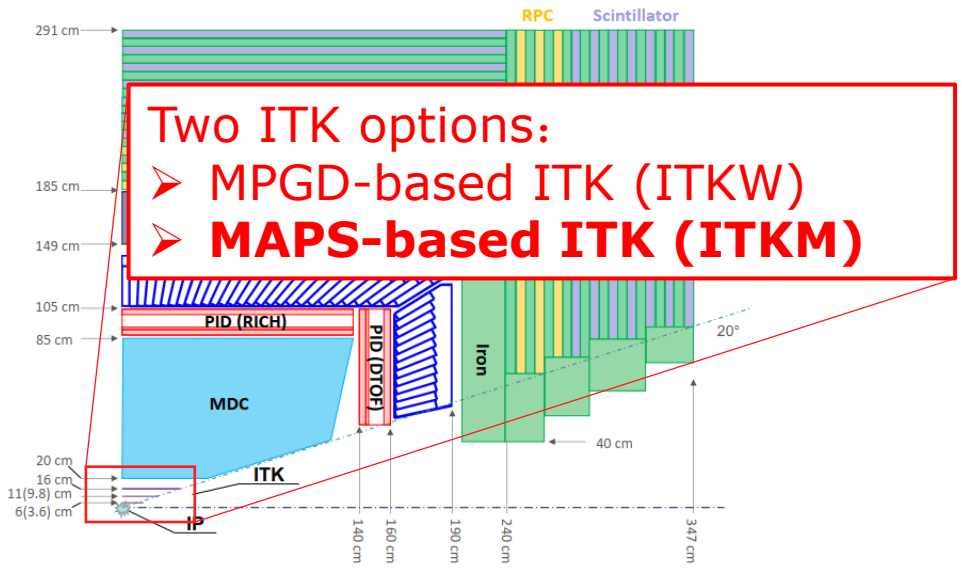
- **STCF: next generation e^+e^- collider in China**
  - Detailed study of τ-c physics
  - Precise tests to the SM
  - Searching for new physics
- E_{cm}=2~7 GeV
- Peaking luminosity >0.5×10^{35} $cm^{-2}s^{-1}$

High luminosity brings challenges to all detectors, especially the Inner Tracker

- Extremely low material budget
- High event rate capability
- Good radiation tolerance





MAPS-based Inner Tracker for STCF

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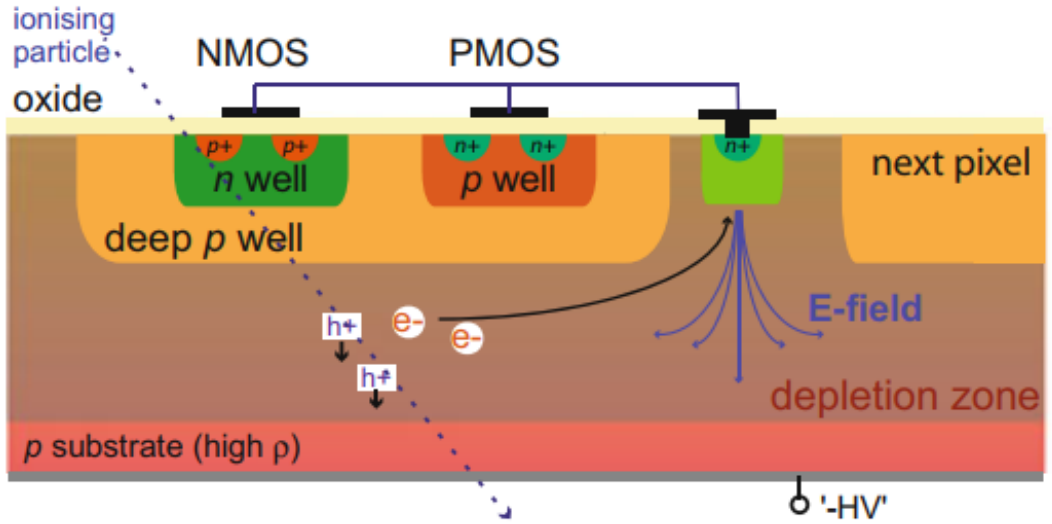
Requirements for Inner Tracker

- ~0.3% X_0 per layer
- $\sigma_{r\varphi}$<100μm
- Tracking efficiency >90% @100MeV/c
- Hit rate 800kHz/cm^2, TID 0.6Mrad/y, NIEL $3.5\times10^{10}n_{eq}$/cm^2/y

Requirements for MAPS

- Power consumption <100mW/cm^2
- Moderate position resolution
- Good timing of ~50ns
- Detection of energy deposition



Monolithic **A**ctive **P**ixel **S**ensor
- ✓ Mature CMOS technology
- ✓ Highly integrated
- ✓ Small pixel pitch
- ✓ Low material budget
- ✓ High SNR
- ✓ …

small collection electrode MAPS chosen as baseline design for ITKM

Conceptual design of ITKM

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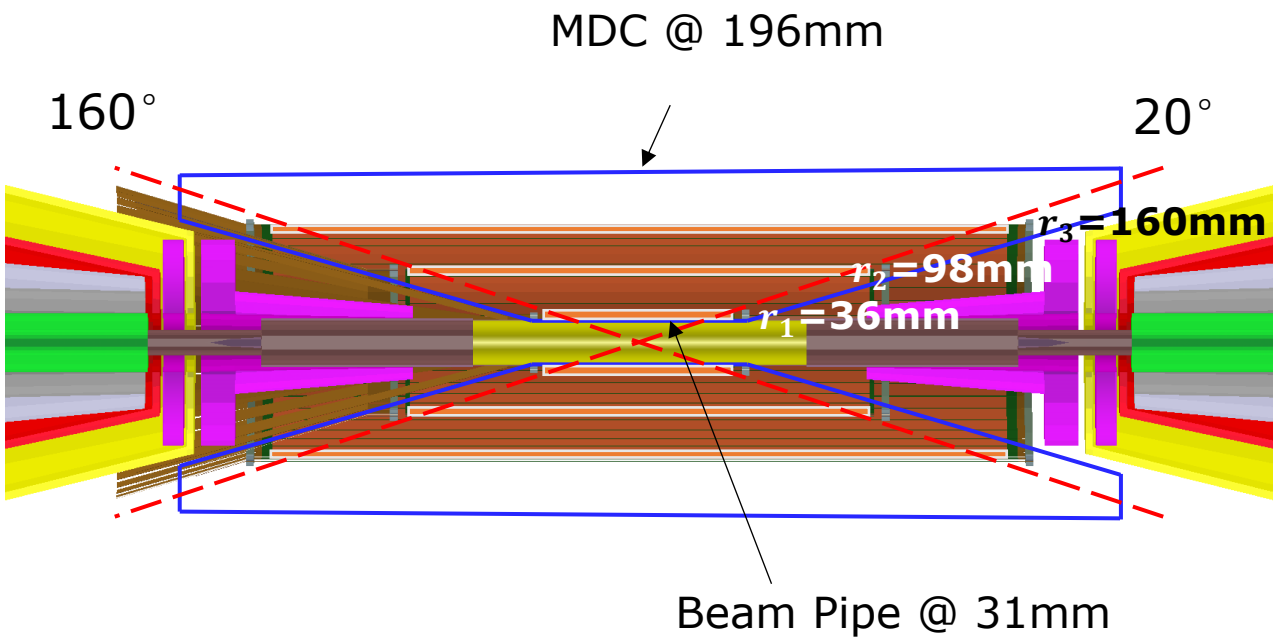

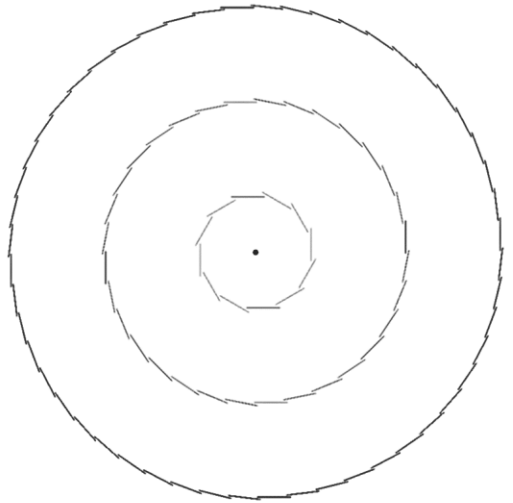

	Min radius/mm	stave no.	chip no.	Area/cm²
ITKM1	36	12	12	583.9
ITKM2	98	32	30	3892.7
ITKM3	160	52	48	10120.9

- A three layer design at present
- Single chip size **~2cm×2cm**
- Covering polar angle **20° -160°**
- Total area: 15000cm²
- 3600 chips

Chip design overview

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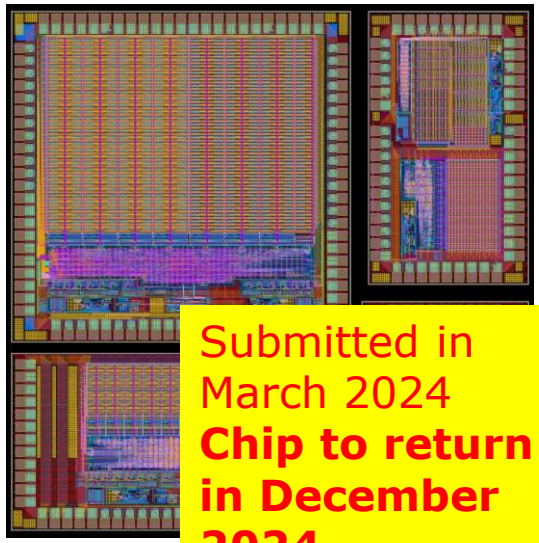
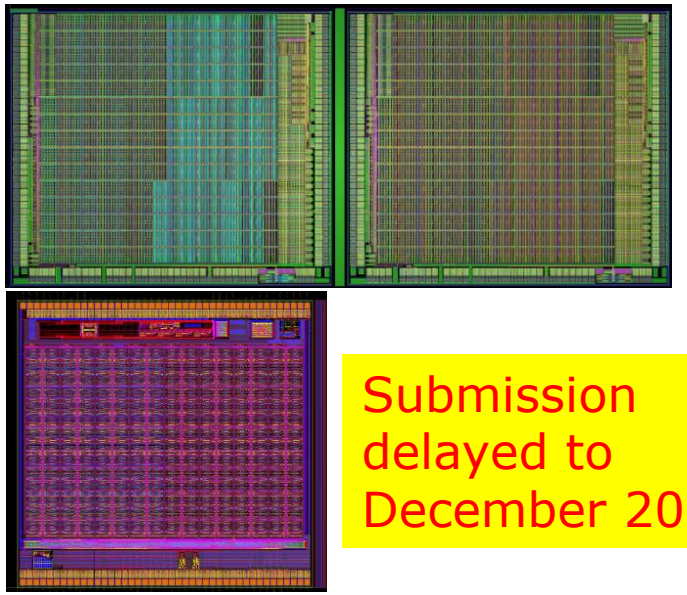
Prototype MAPS design under three different technologies

TJ180nm
- Mature process in HEP (ALPIDE, TJ-Monopix)
- **Baseline techno**
- Low res substrate + high res (>1kΩ·cm) EPI



Submitted in March 2024
Chip to return in December 2024

BCIS90nm
- **Domestic techno**
- Low res EPI (10Ω·cm)



Submission delayed to December 2024

GSMC130nm
- **Domestic techno**
- High res substrate, no EPI

Submitted in September 2024
Chip to return in March 2025

TJ180-Chip Overview

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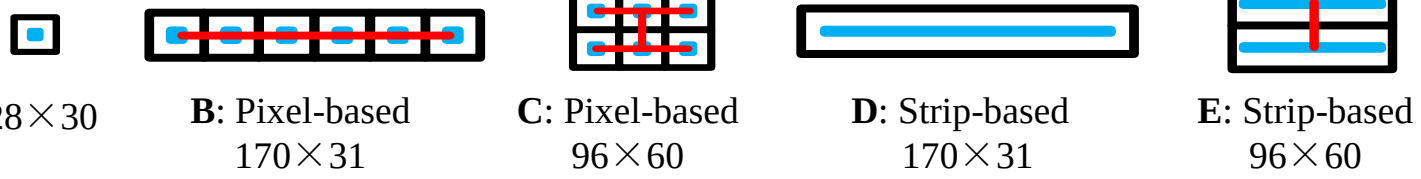
- Compare different pixel geometry & connection



A: 28×30

B: Pixel-based
170×31

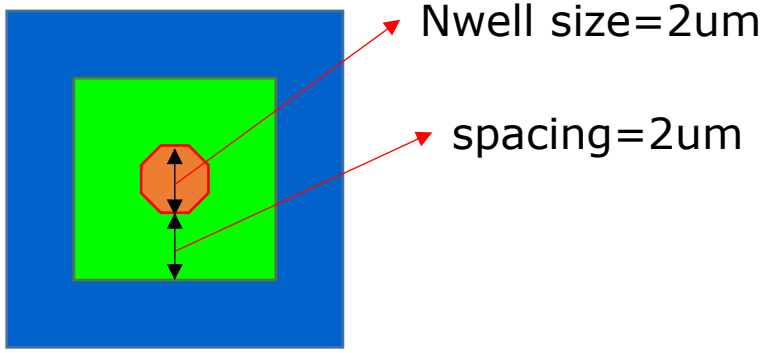
C: Pixel-based
96×60

D: Strip-based
170×31

E: Strip-based
96×60

Metal line connected
✓ small input capacitance

Nwell (active) connected
✓ faster charge collection



Four flavors of prototype chips:
- **Chip1**: Small pixel, Low power consumption
- **Chip 2 & 3**: Enlarged pixel size, timing with TOA, TOT
- **Chip 4**: Analog readout for sensor performance comparison

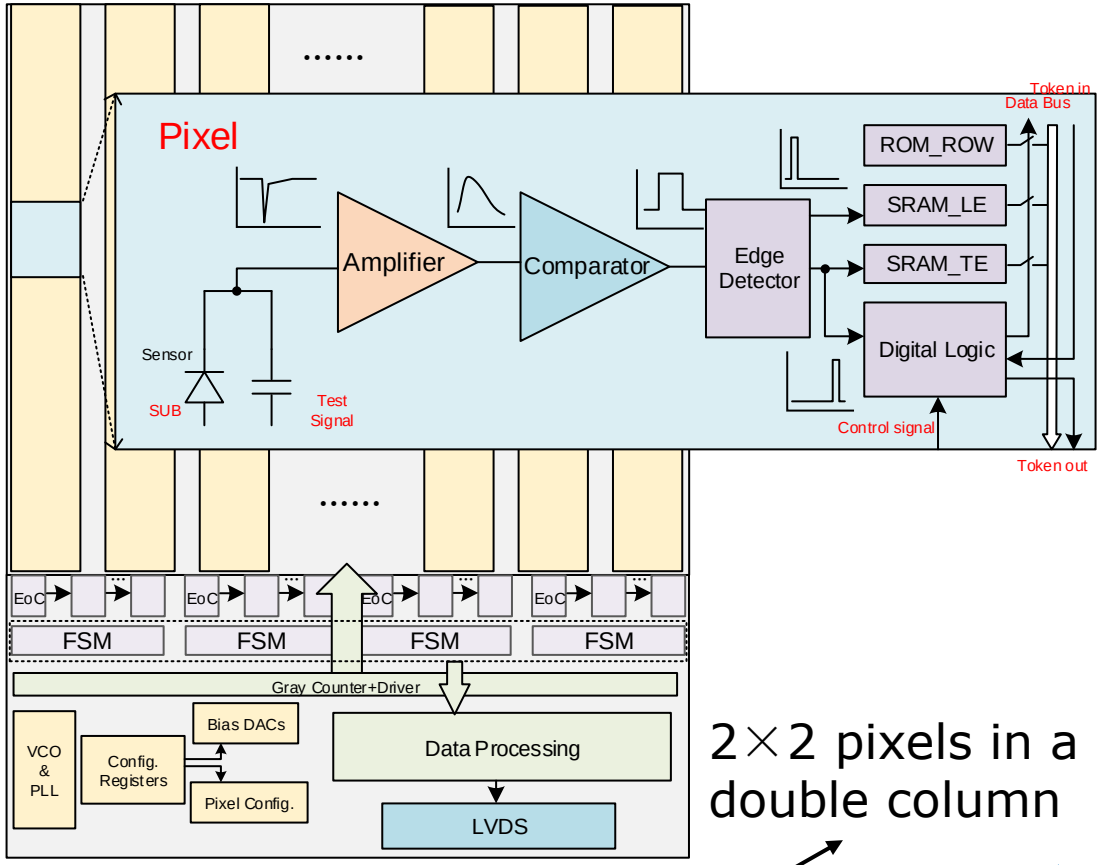
	Chip1	**Chip2**		**Chip3**		**Chip4**
Pixel size (μm×μm)	28.1×30.1	96.4×59.6		170.0×31.0		Mixed
Sensor	A	E	C	D	B	A+B+C+D+E
Pixel array	16×30	8×12	8×12	60×8	60×7	Mixed
Readout	Column-drain	Column-drain		Column-drain		Analog readout
ToA & ToT	×	✓		✓		×
Chip area (mm^2)	1.5×1.4	2.5×1.6		2.8×3.1		1.2×1.4

TJ180-Full functional chip

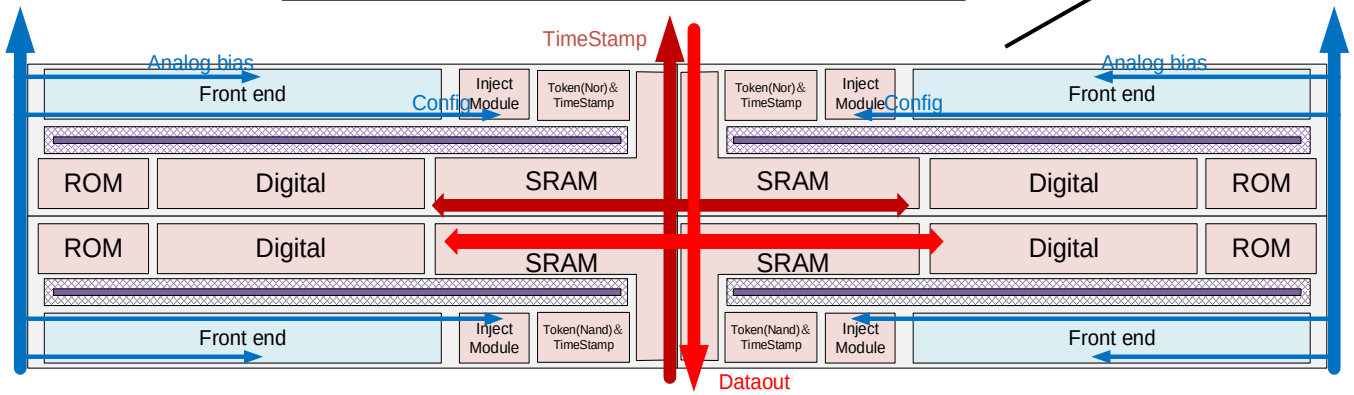
Chip 2 & 3

- Column-drain readout
- 20MHz clock distributed to the pixel array
- LE & TE timestamp recorded (8+8 bits)
- Power consumption estimation for 2×2 cm^2 chip
  - Metal line connected: 46.2mW/cm^2
  - Nwell connected: 55.7mW/cm^2
- >99% readout efficiency @8.72MHz/cm^2
- Timing ability σ_{ele}~22.0ns
  - σ_{Jitter}~8.1ns (Q_{inj}=600e^-)
  - σ_{TDC}~14.4ns
  - σ_{TW}~14.5ns (Q_{inj}=600e^-)

Lailin Xu, 2024FTCF-Hefei



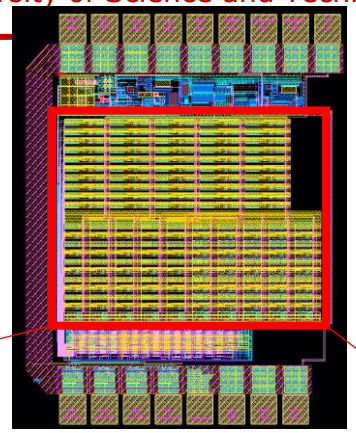
2×2 pixels in a double column

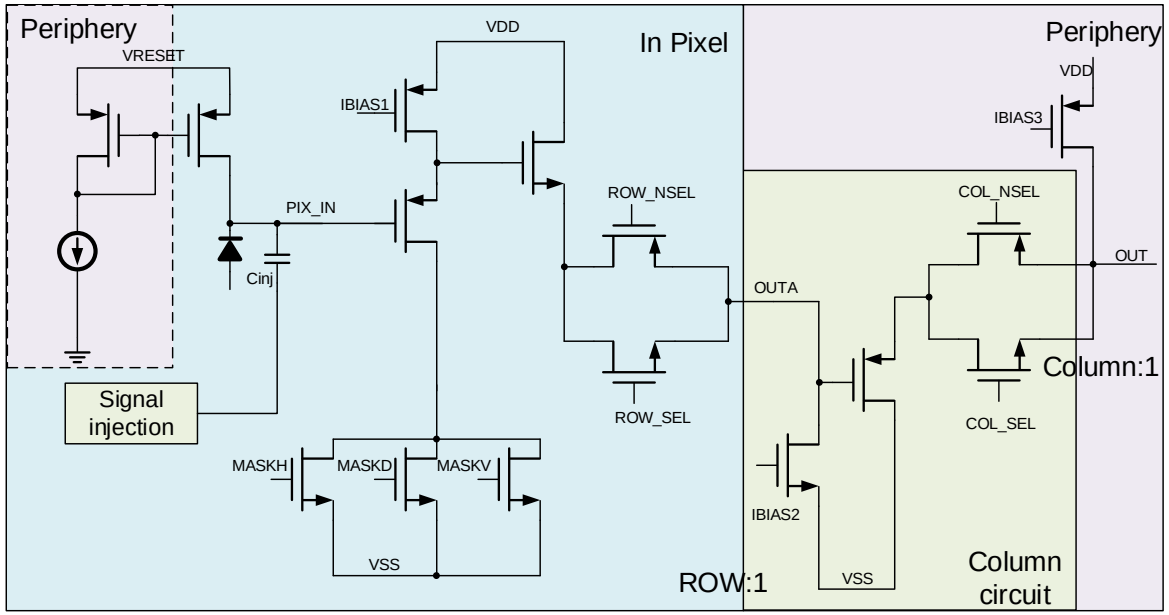


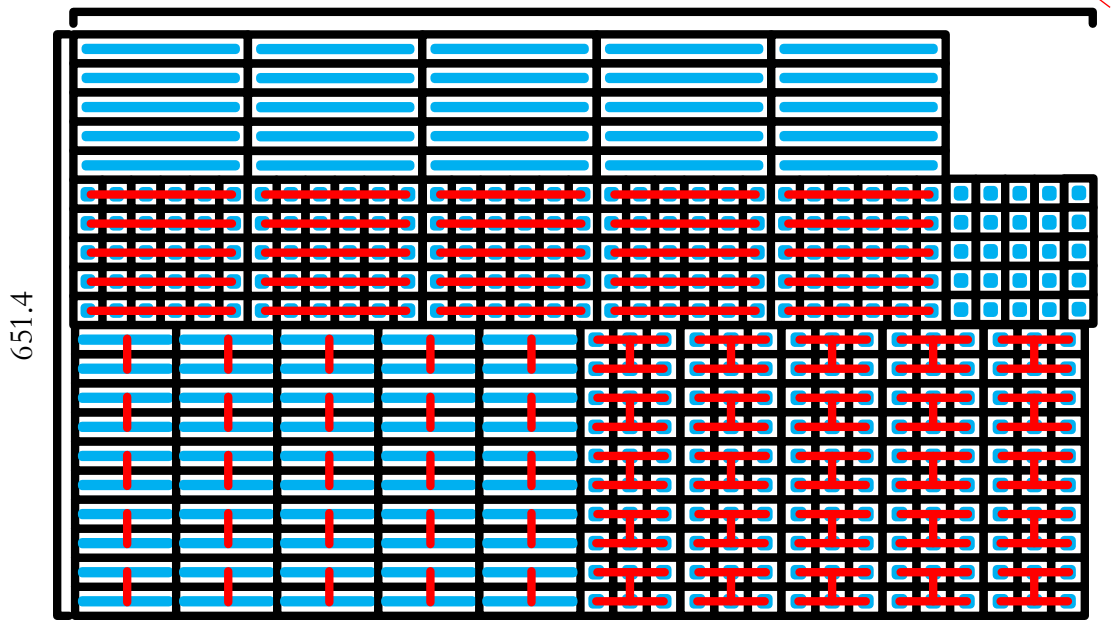
TJ180-Characterization chip

Chip 4

- To study performance of different pixel layout
- 5×5 array for each type of pixel
- Pure analog readout: source follower + matrix parallel readout







BCIS90-Chip Overview

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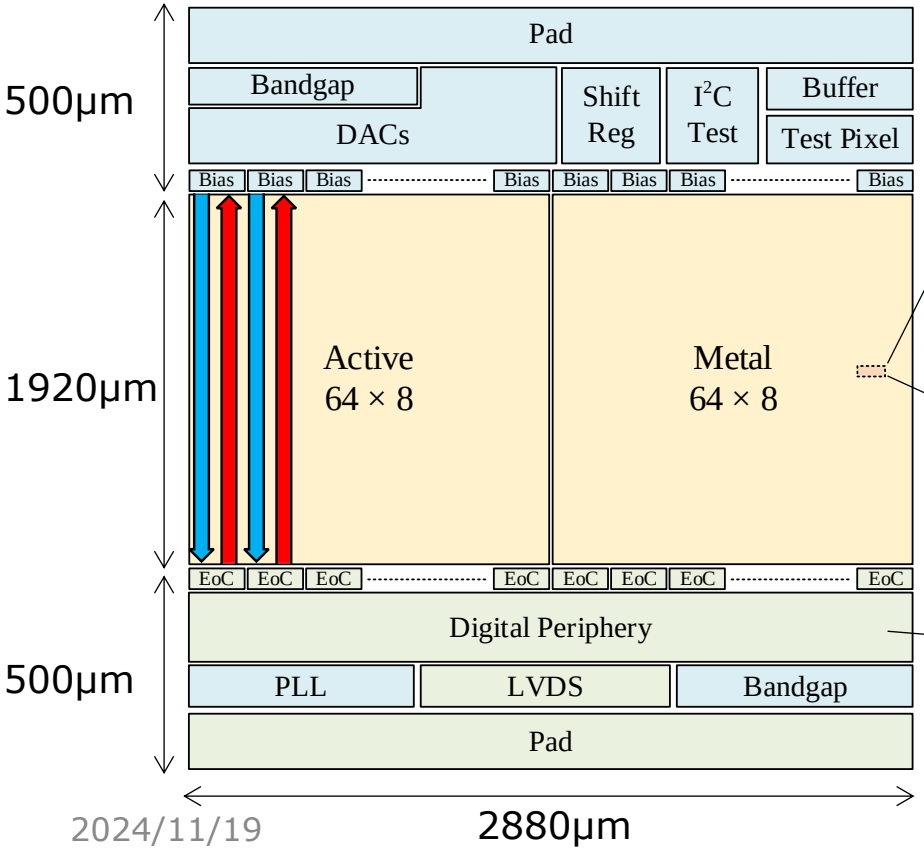
- Two flavors of prototype chips
  - **Full-function chip**
  - Pure analog readout chip

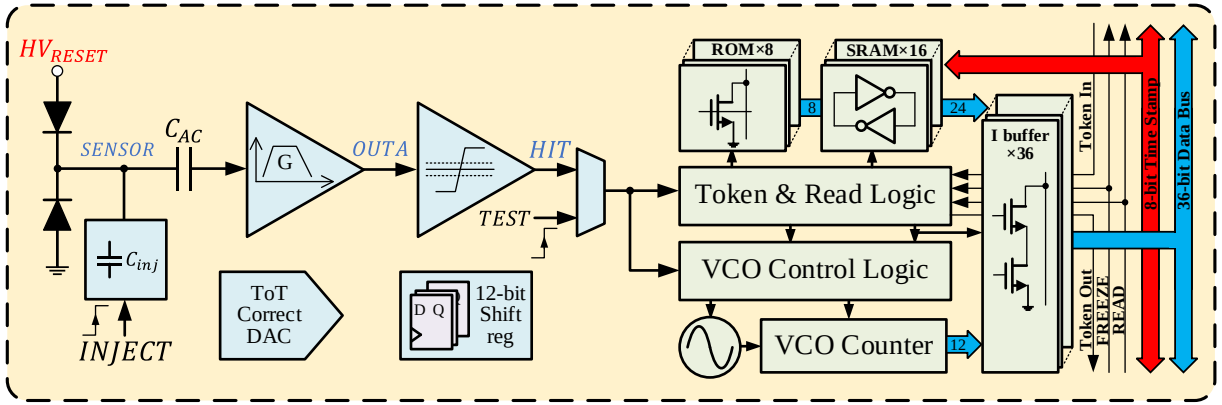


Analog

- Pixel size 180×30 μm²
- AC-coupling, diode positive voltage
- Independently adjustable pixel threshold & discharge time

Digital

- TOA & TOT
- Column drain
- 500MHz in-pixel VCO for fine LE timing
- VCO frequency calibration



Periphery

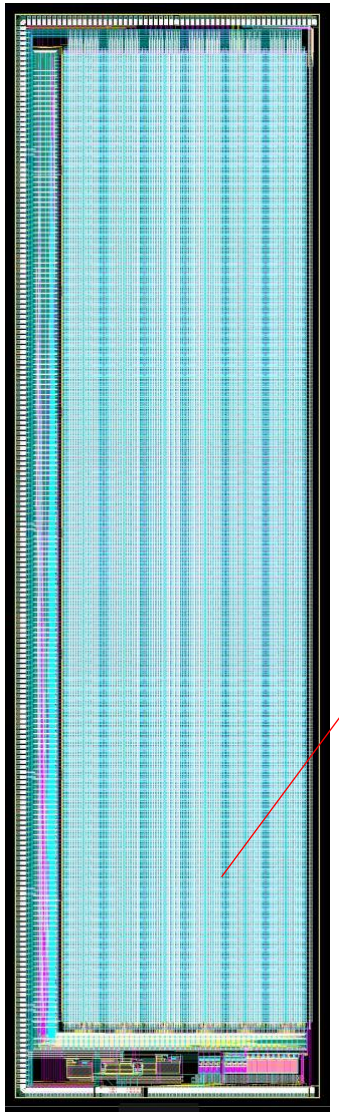
- Token readout control
- Data assembly
- 500Mbps LVDS

Time stamp

- 20MHz
- 8-bit Gray code

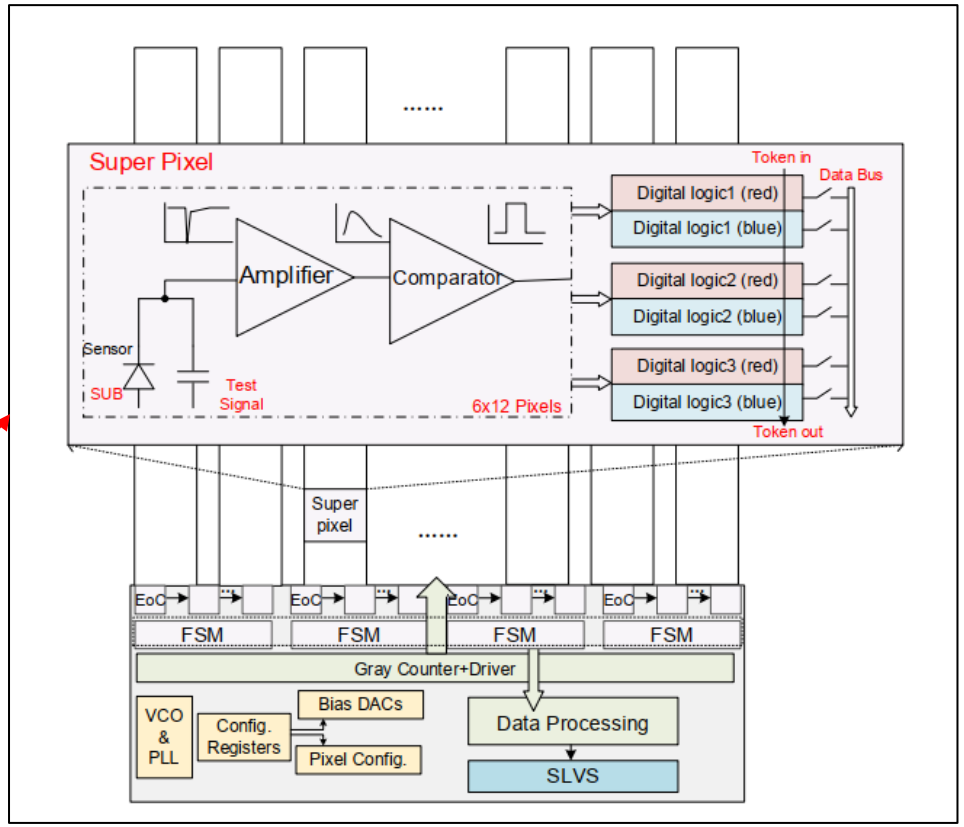
GSMC130-Chip Overview

	Chip1		Chip2	Chip3	Chip4
Pixel size (μm×μm)	170×30		30×28	Mixed	33.2×33.2
Sensor	B	C	A	A+B+C	D
Pixel array	60×8	60×8	60×48	Mixed	576×144
Readout	Column-drain		Column-drain	Analog	Column-drain (Super pixel based)
ToA & ToT	✓		×	×	✓
Chip area (mm^2)	5.25×4.4		4.3×2.2	4.2×4.9	21.0×6.0



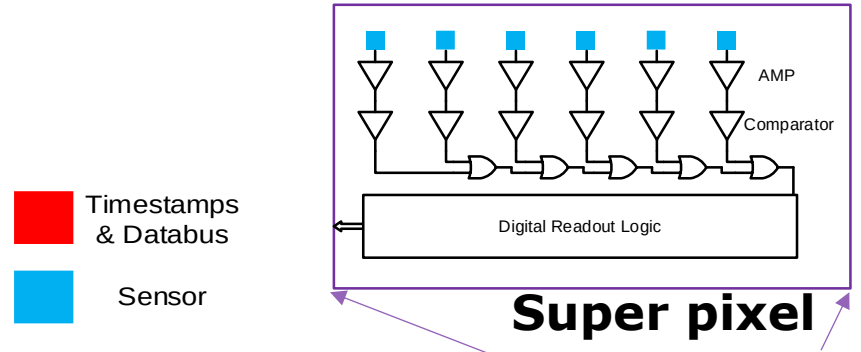
Chip4

- **Novel super pixel design**
- 33×33 μm^2 pixel
- 500MHz VCO for fine LE timing
- Expected power consumption ~40mW/cm^2

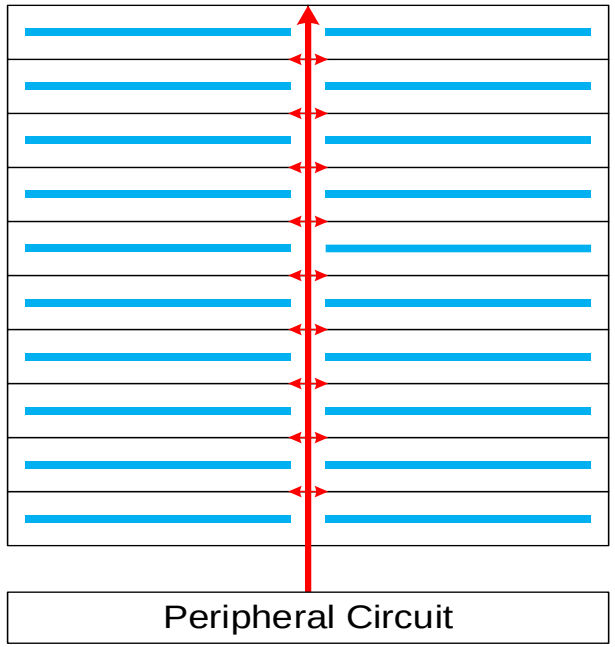


GSMC130-Design concept

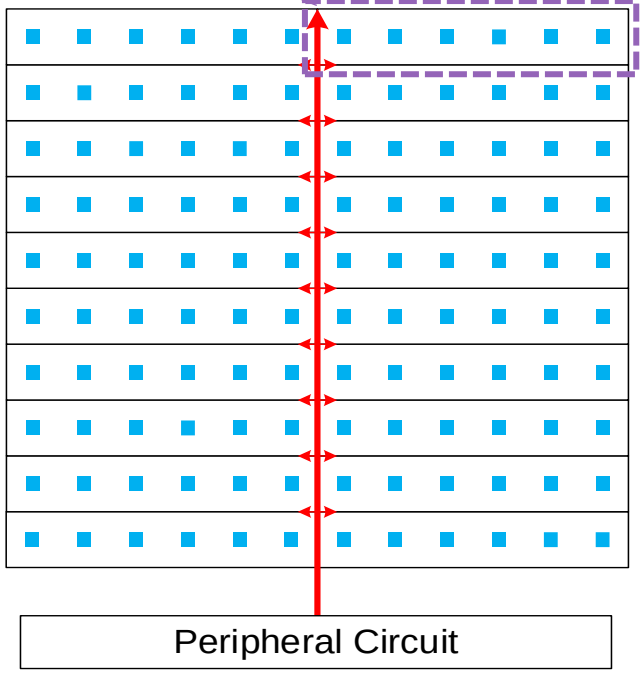
- **Towards finer timing & higher spatial resolution with low power consumption**
- How is that possible?
- Super pixel design!



- ✓ Reduced readout channel → low power consumption
- ✓ In pixel VCO → fine timing
- ✗ Large pixel → high noise, low spatial resolution

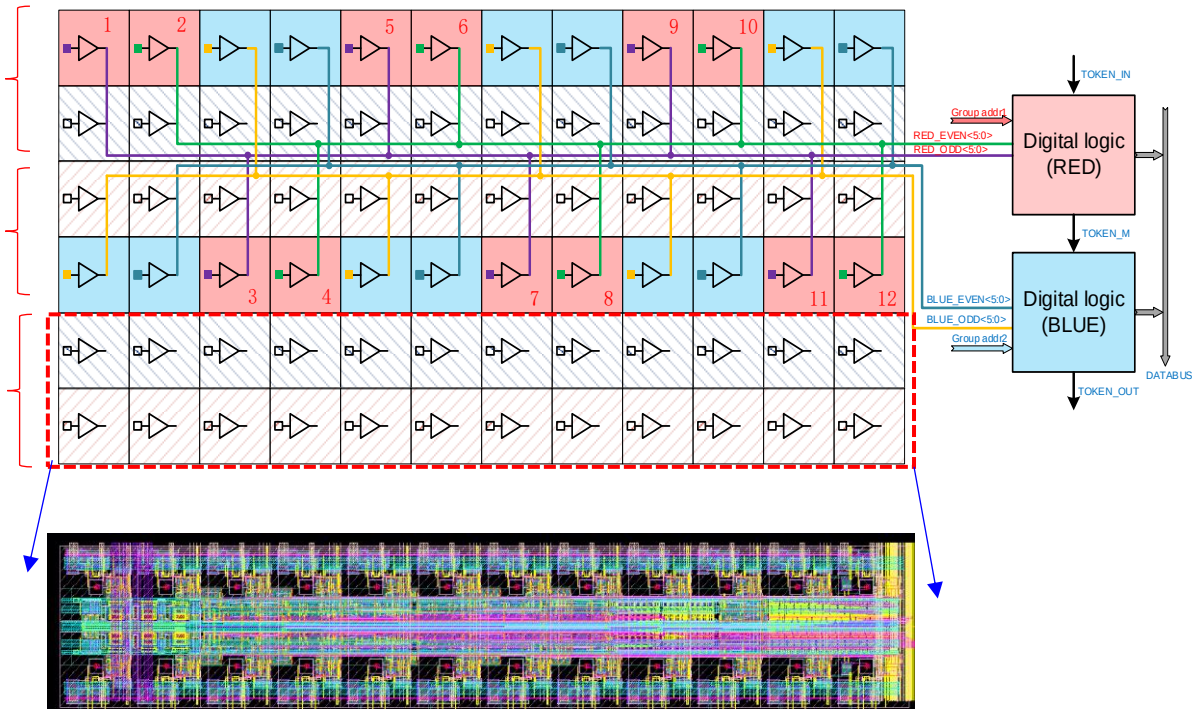


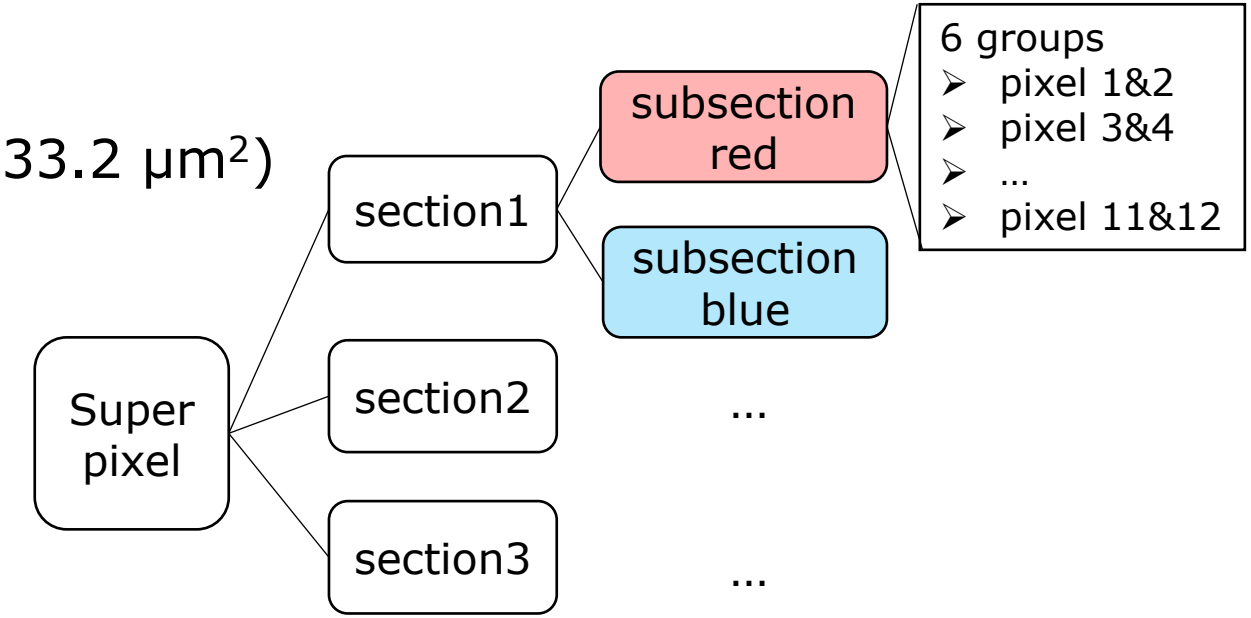
- ✓ Channel combined through OR logic→ low power consumption
- ✓ Common VCO in super pixel → fine timing
- ✓ Small pixel → low sensor capacitance, high spatial resolution



GSMC130-Super Pixel

- Pixel array 576 rows by 144 columns
- Each super pixel with 6×12 pixels (33.2×33.2 μm²)





- Non-adjacent pixels' discriminator output combined through OR gate
- Pixel address info:
  - 10-bit subsection address
  - 3-bit group address
  - 1-bit pixel parity

✓ Simultaneous hits in a 3×4 range can be readout correctly

GSMC130-Super Pixel

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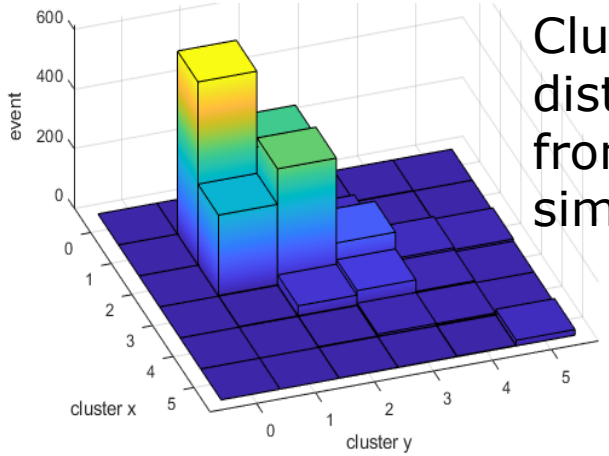
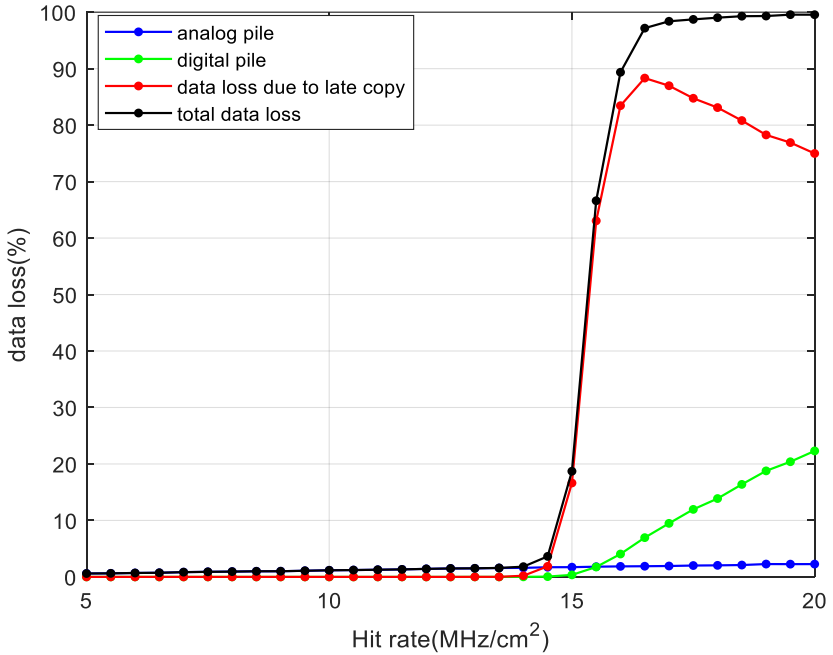
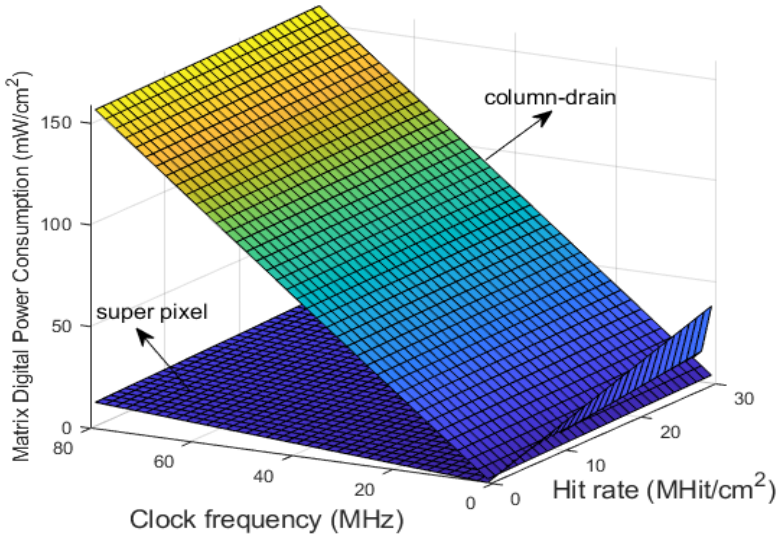
- Expected average cluster size ~2.3 pixels (threshold 150e$^-$)
- Hit loss rate <1% @ 8.5MHz/cm^2 (more than 10 times ITKM count rate)



Cluster size distribution from MC simulation

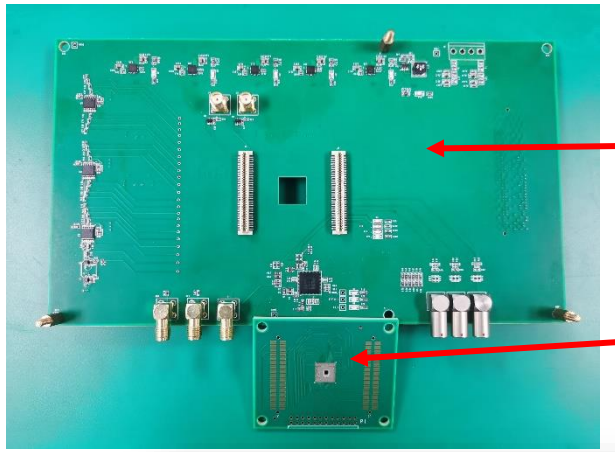


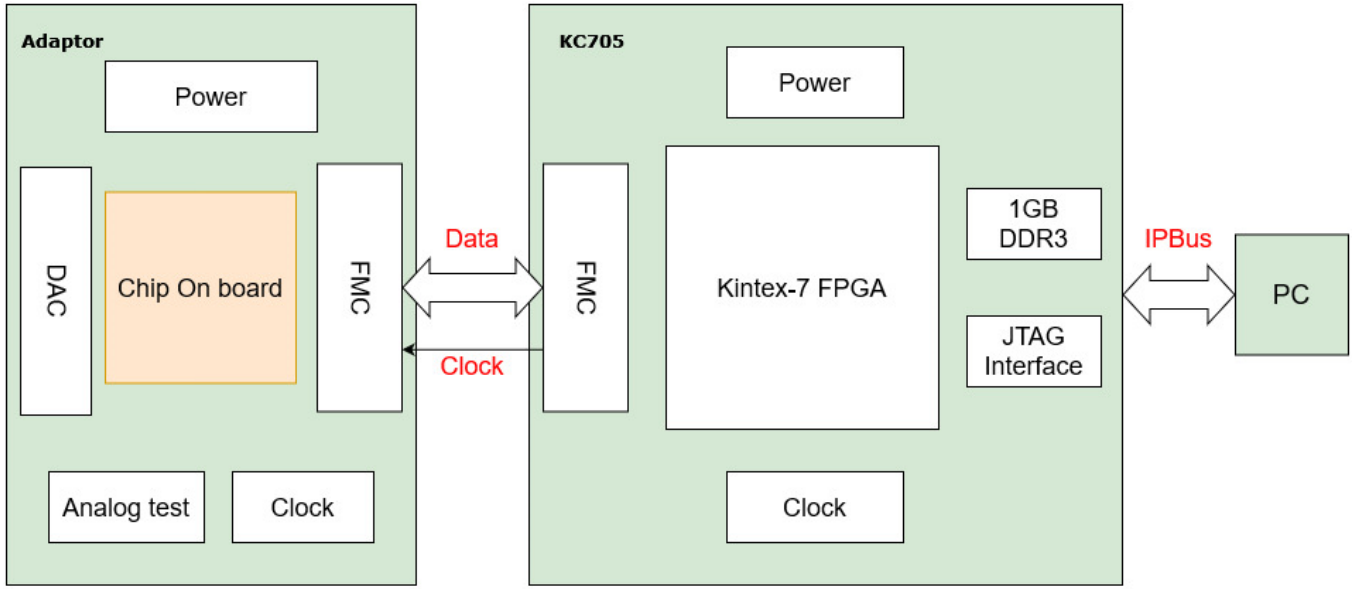


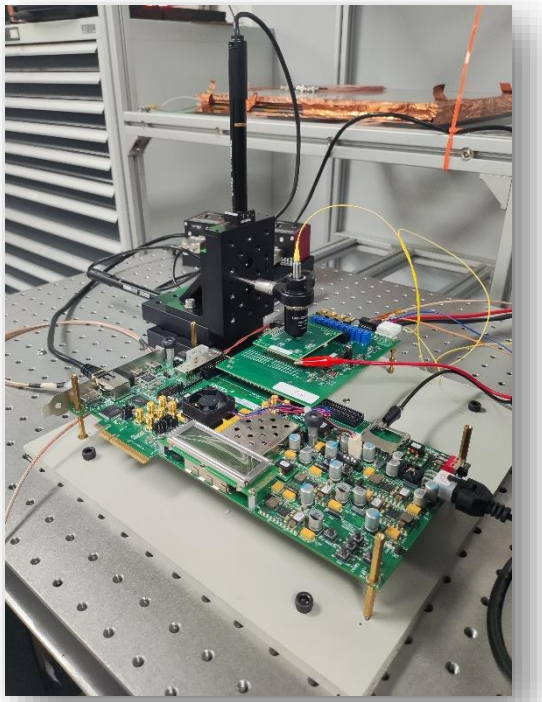
- Considerably reduced power consumption w.r.t column-drain architecture
- Digital power <20mW/cm^2

MAPS test setup

- Adaptor board + chip carrier board
- Common adaptor board design for different chips
  - Clock signal
  - Power supply
  - Test points
- Data acquisition through FPGA development board



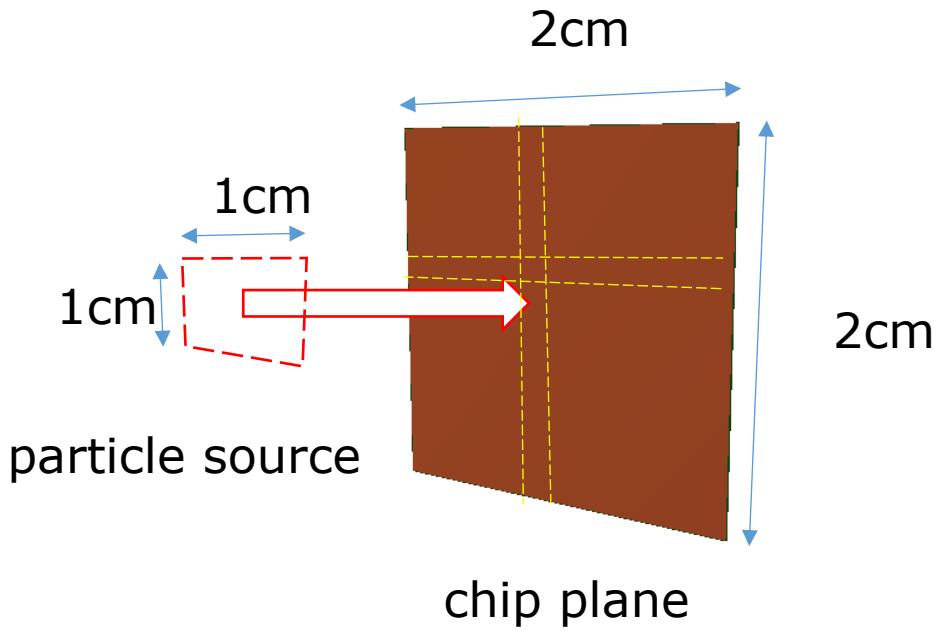


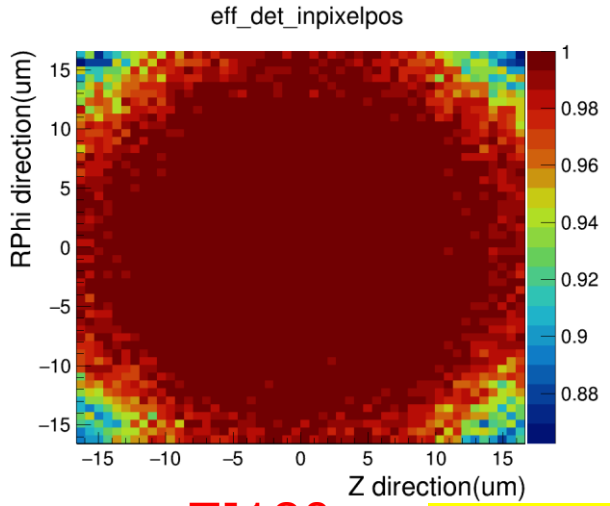


MAPS characterization setup (other chips under test)

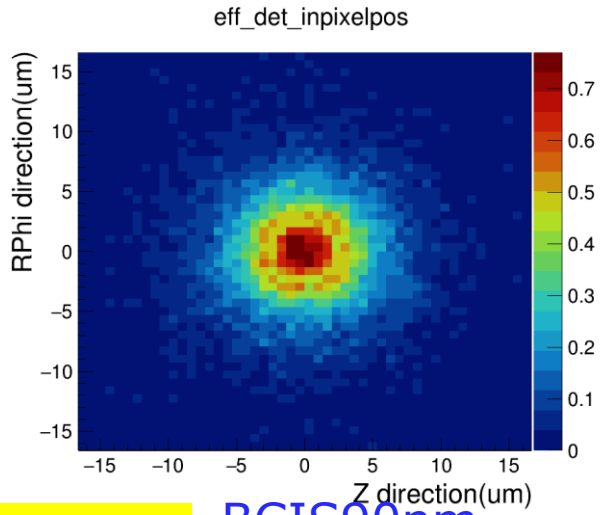
MAPS simulation-MIP response

- 1GeV μ^- perpendicularly, randomly incident
- Ionization & charge collection simulation under STCF-OSCAR framework



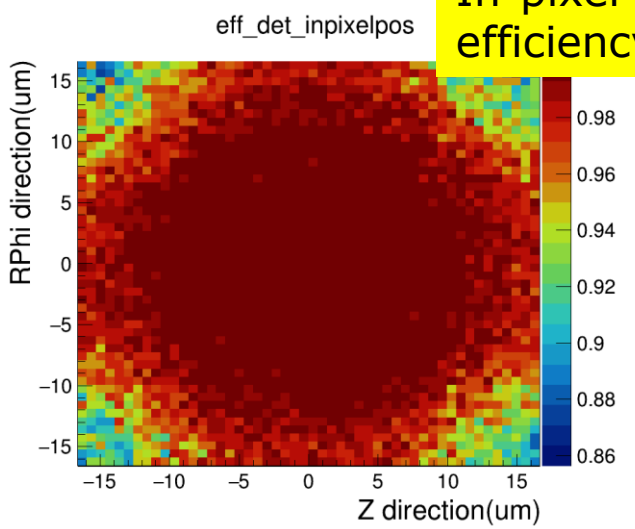


TJ180nm

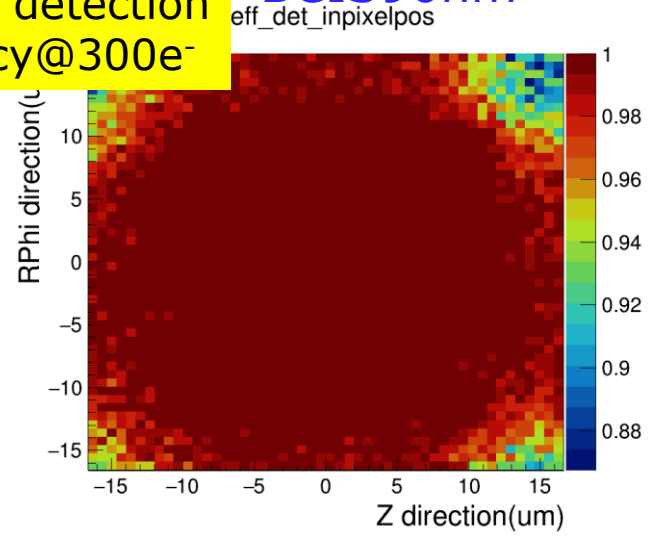


BCIS90nm

In-pixel detection efficiency@300e-



GSMC130nm



Modified-TJ180nm

MAPS simulation-MIP response

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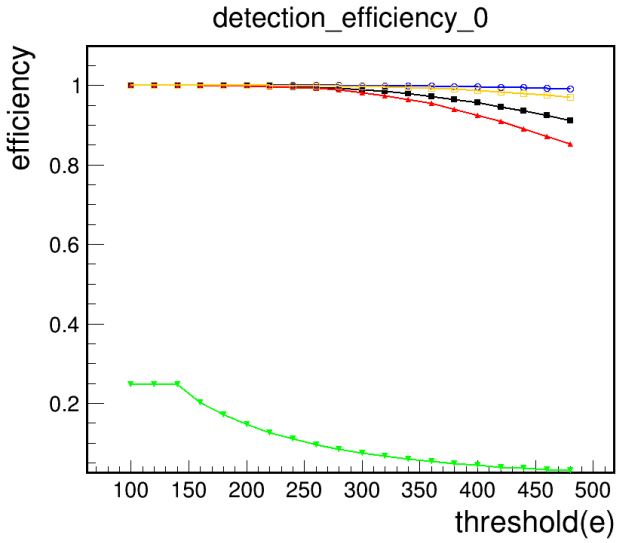
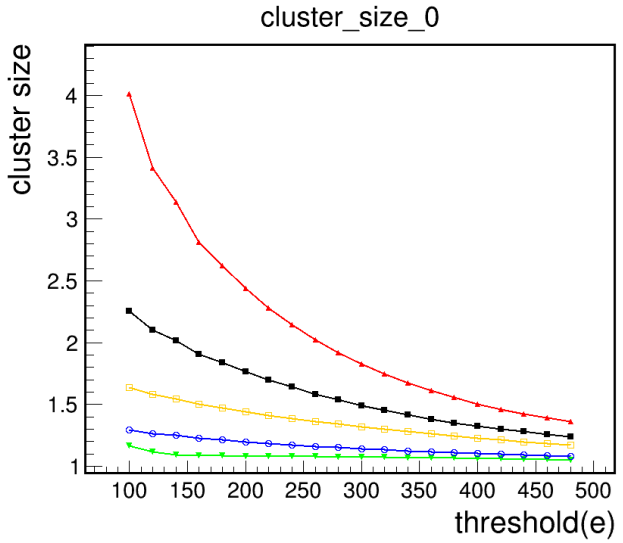
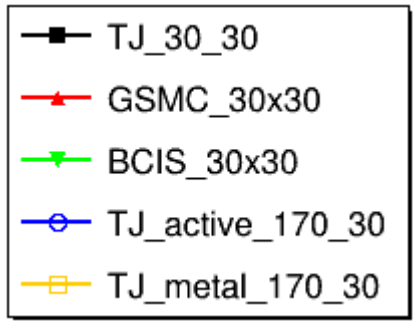
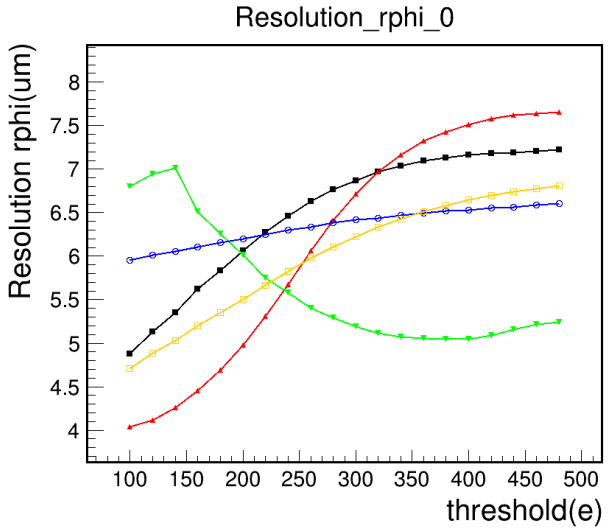
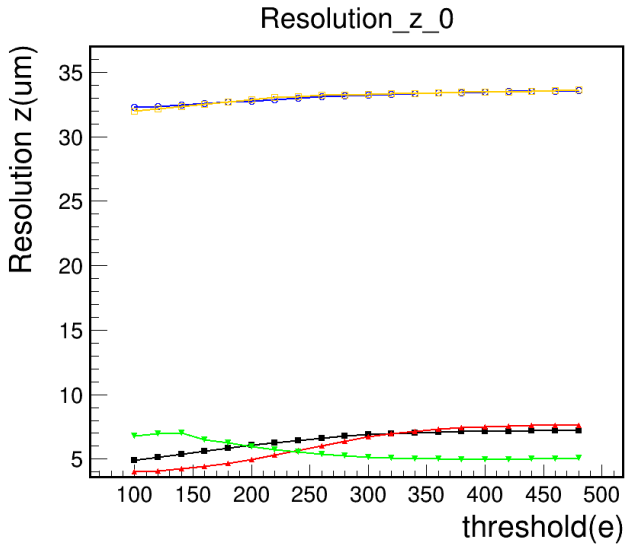










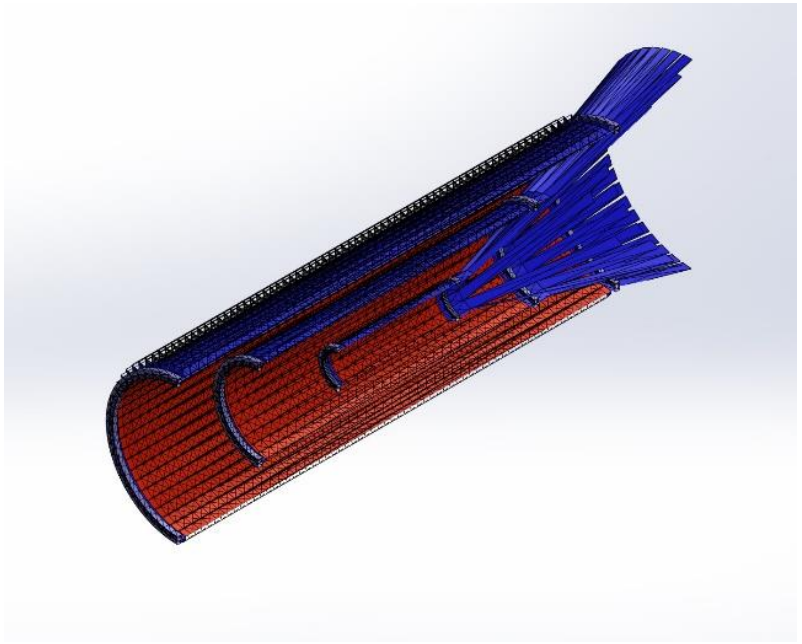
In close contact with foundry for techno improvement

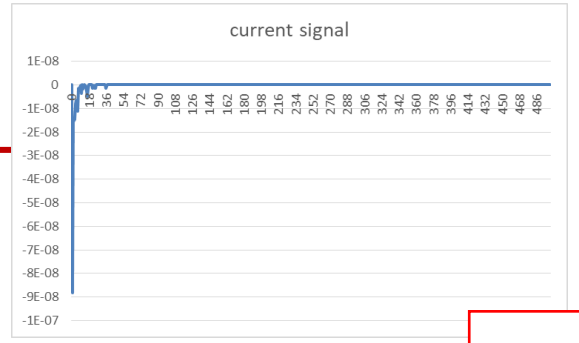
Comparison of different technos & pixel design

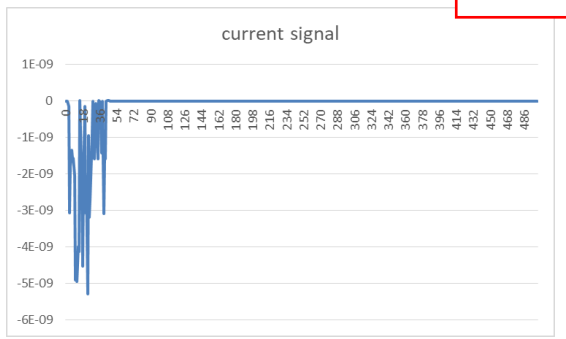
- Good detection efficiency for all technos except for BCIS90, >98% @300e$^-$ threshold
- Spatial resolution varies from 4μm to 8μm in the 30μm pitch direction
- In the 170μm pitch direction, spatial resolution ~30um

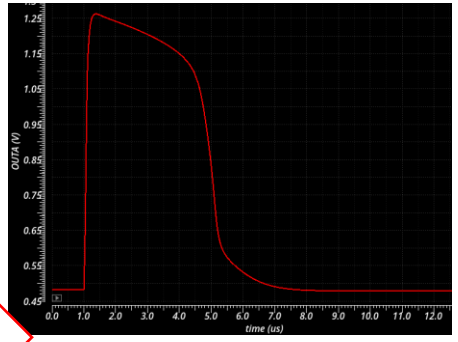
ITKM simulation

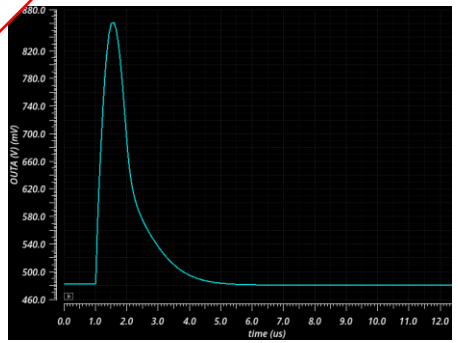
- Preliminary geometry design by DD4hep
- Chip + Flex + Carbon fiber support
  - **~0.27% X_0 for layer 1&2**
  - **~0.29% X_0 for layer 3**
- **Full digitization** process considering pre-amplifier response

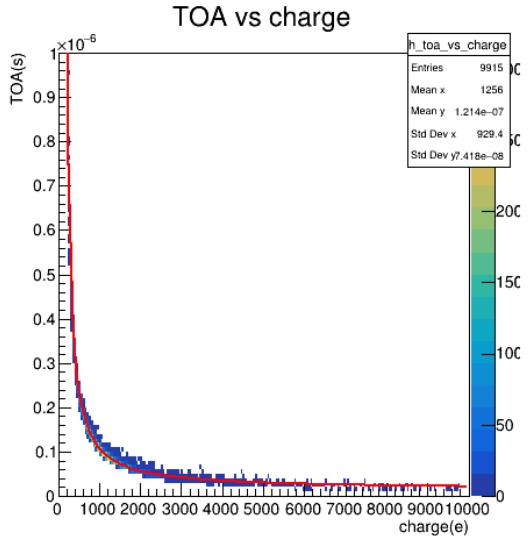


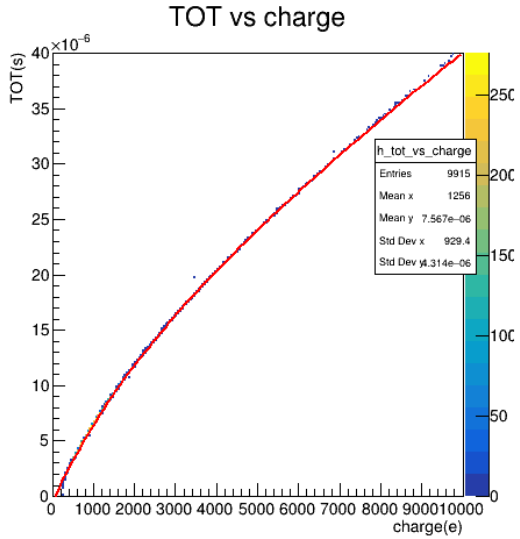






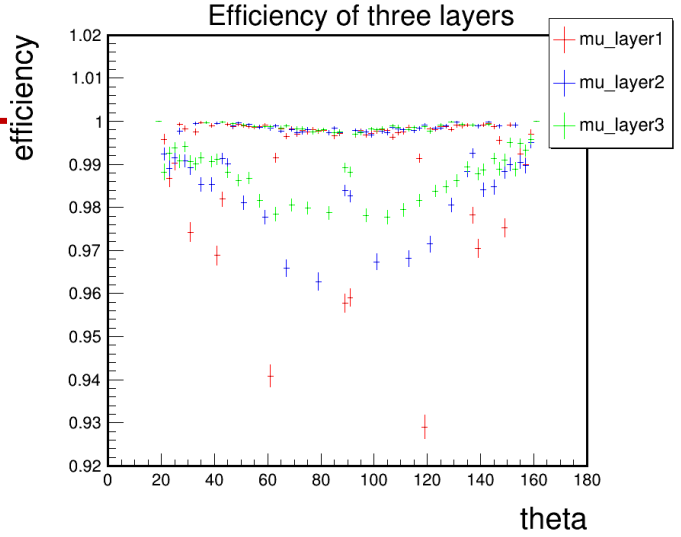


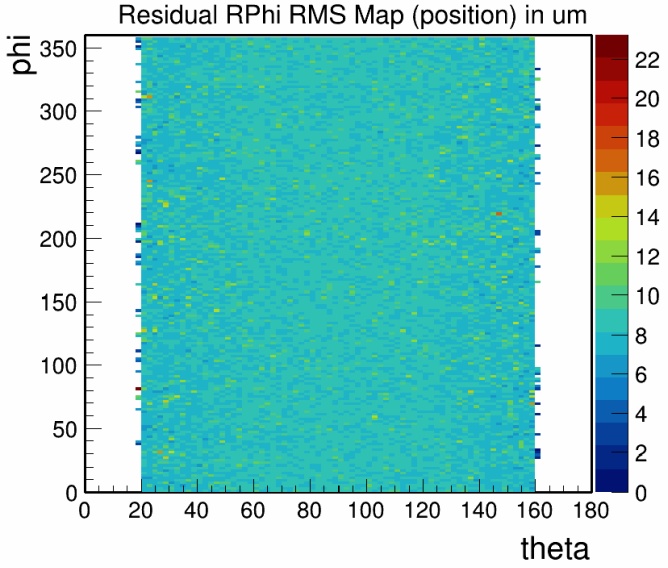


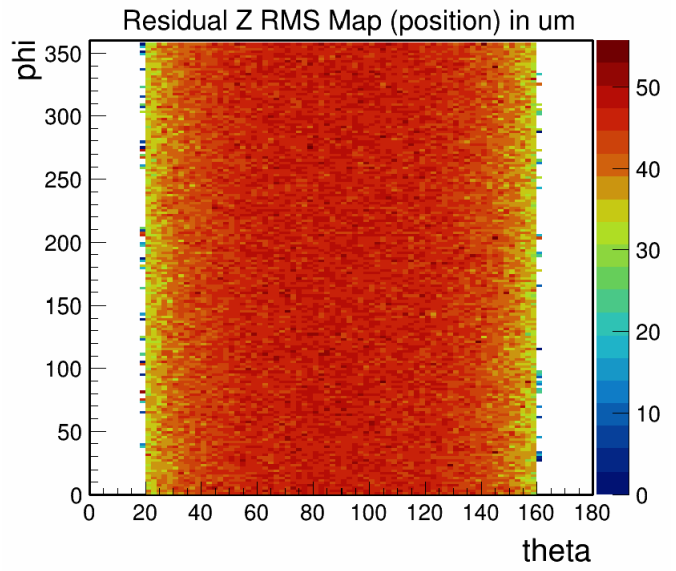


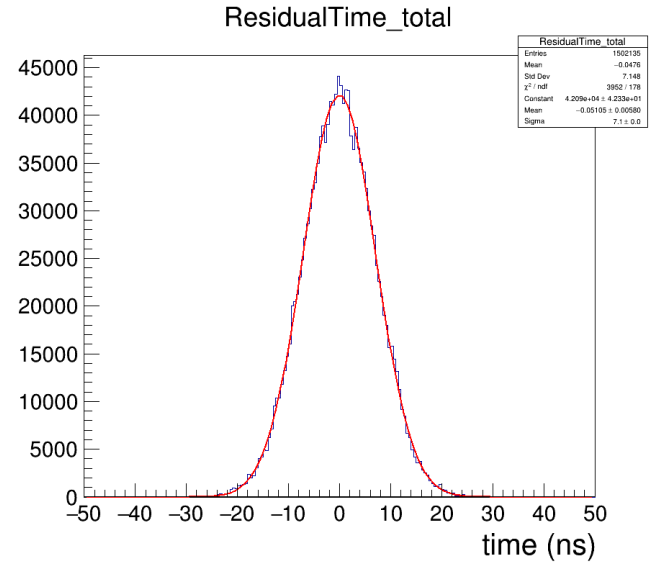
ITKM simulation-Results

- Pixel type:
  - TJ180nm, 170×30 μm², n-well connect
- Simulation settings:
  - 1GeV μ^-, θ range 20° -160°
  - Pixel threshold: 300e⁻









- ✓ Average detection efficiency 99.2%
- ✓ Position resolution: σ_z=33.5μm, $\sigma_{r\varphi}$=6.8μm
- ✓ Time resolution (sensor only) 7.1ns

Module design & simulation

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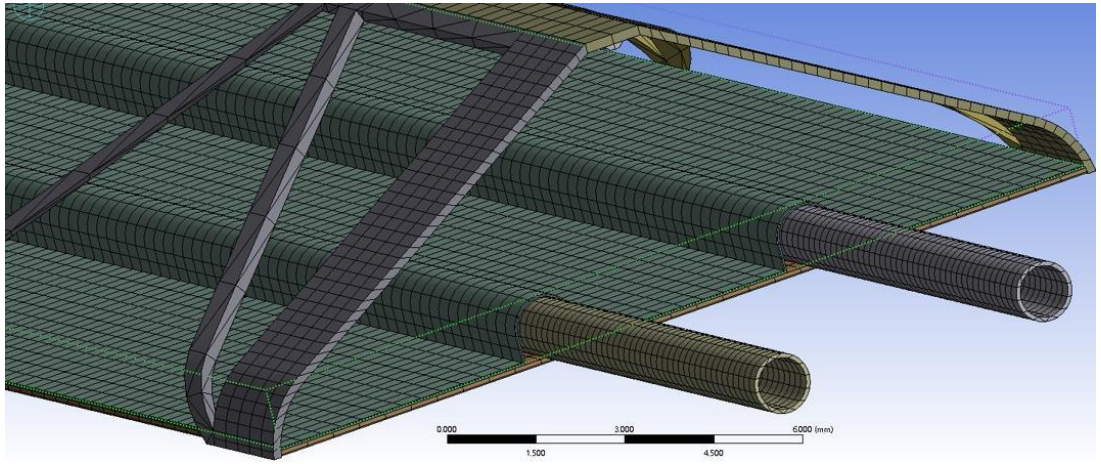
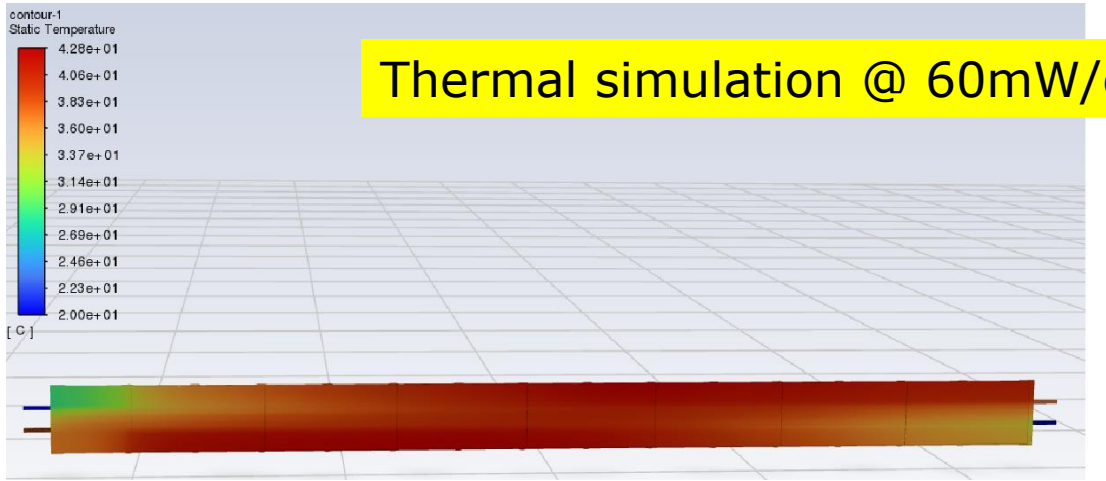
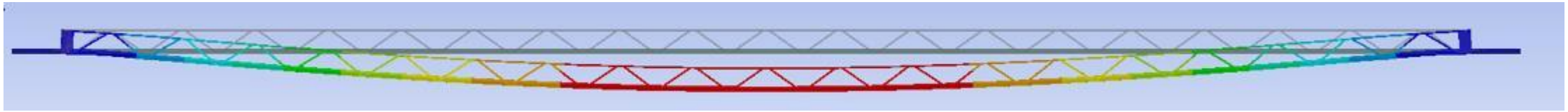
- Stave design based on ALICE ITS2 inner barrel
- FEA with ANSYS





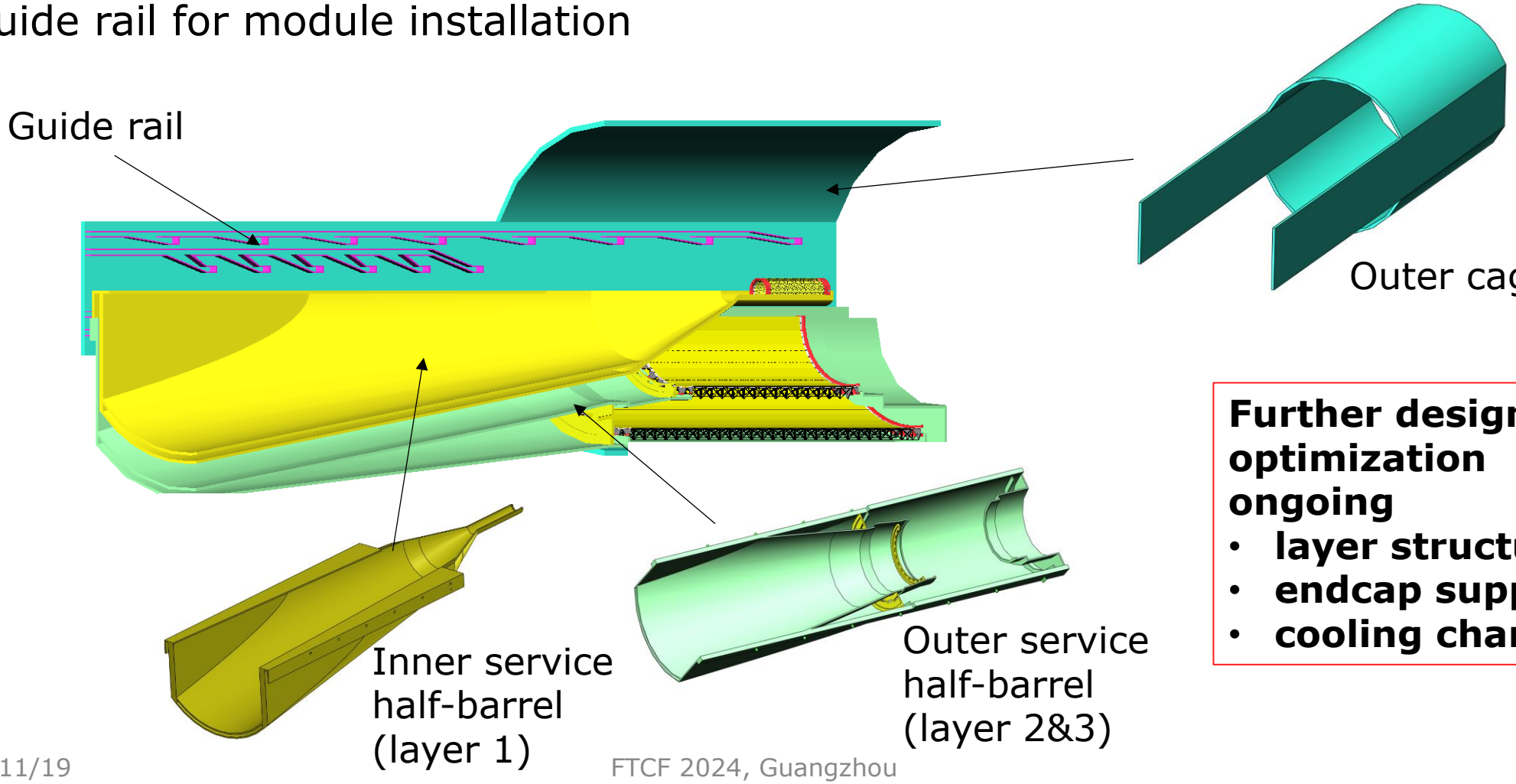
Thermal simulation @ 60mW/cm^2



- Sagitta 167μm @ F=0.2N concentrated load
- Chip temperature < 42.8 (59.5)℃ for flow rate of 2m/s (1m/s)

Mechanical design

- Basic structure: detector barrel + service half-barrel
- Guide rail for module installation



Further design & optimization ongoing
- **layer structure**
- **endcap support**
- **cooling channels**

Conclusions

- MAPS-based inner tracker for STCF is under R&D, aiming at:
  - $\sigma_{r\varphi}$<100μm
  - time resolution ~50ns
  - power consumption <100mW/cm^2
  - material budget ~0.3% X_0 per layer
- Prototype chips design almost finished for 3 technologies. Thorough chip characterization to begin in this year.
- MAPS simulation shows promising results. Further technology optimization ongoing.
- Module design & simulation just beginning. ITKM mechanics also under design.

Conclusions

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Thanks!

Backup

Considerations for STCF MAPS

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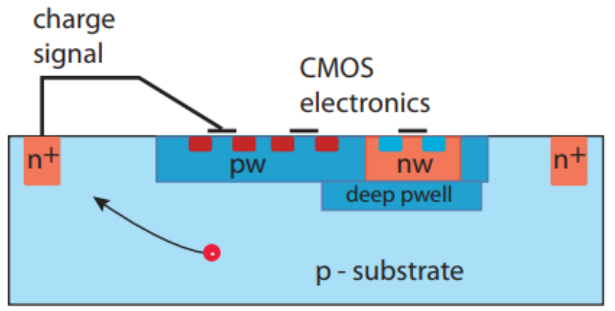
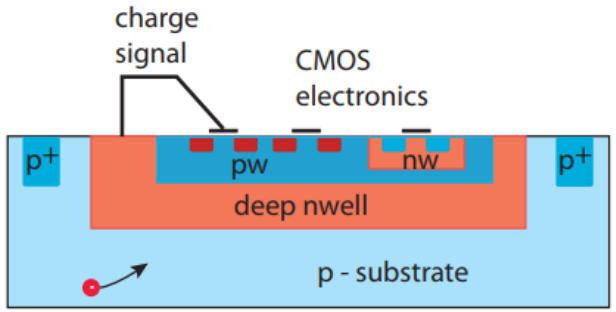
HR-MAPS or **HV-MAPS**?





Low material budget
- Power consumption <100mW/cm^2
- Thin silicon layer ~ 50μm

High hit rate
- Fast readout speed

Pile-up event separation
- Time resolution ~50ns
- Fast charge collection
- Record TOA & TOT information

Moderate position resolution
- Enlarge pixel size if necessary (especially in z direction)

Other considerations
- Technology availability
- Cost-effective

Chip Performance Overview

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Techno	Pixel type	Power Consumption*/ (mW/cm²)	Threshold/e⁻	ENC/e⁻	MISMATCH/e⁻	σ_{t_ele}*/ns
TJ180nm	n-well connect 170×30	55.7	309.0	11.4	5.7	22.0(Q_{inj}=600e⁻)
	metal line connect 170×30	46.2	313.7	11.1	5.7	24.6(Q_{inj}=600e⁻)
BCIS90nm	n-well connect 180×30	~64	198.6	26.6	25	39.1(Q_{inj}=300e⁻)
	metal line connect 180×30	~64	133.2	14.9	13	9.45(Q_{inj}=300e⁻)
GSMC130nm	super pixel 33×33	~40	153.6	5.1	5.8	**1.60**(Q_{inj}=400e⁻)

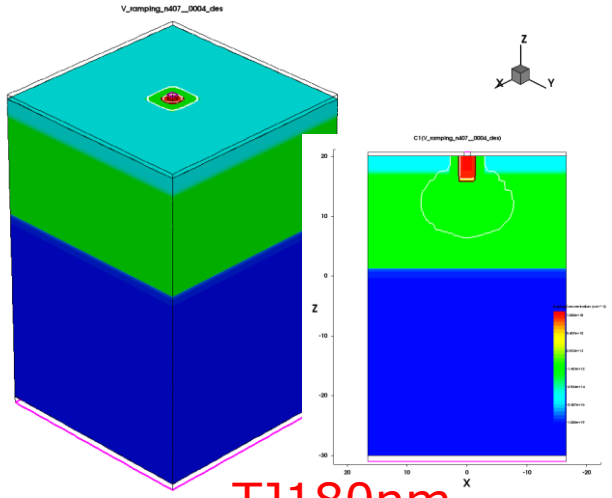
* Power consumption estimated for full-size (2cm×2cm) chip
* Time resolution contributed by electronics: $\sigma_{t\_ele}^2 = \sigma_{Jitter}^2 + \sigma_{TW}^2 + \sigma_{TDC}^2 + \sigma_{CLK}^2$, the value largely depends on the injected charge

Chip design-sensor capacitance

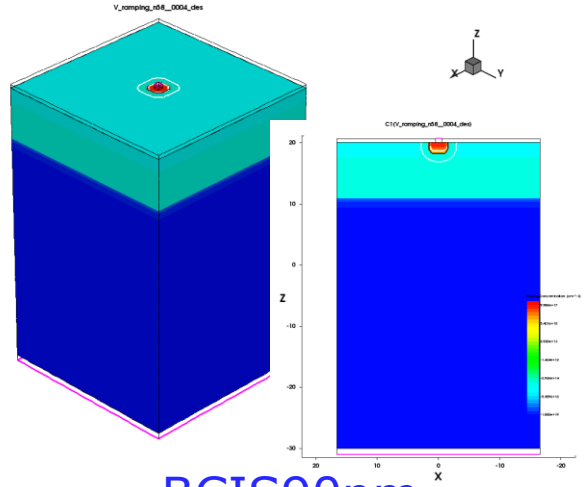
- **TCAD simulation in different technologies**
- Pixel size: 30×30 μm²
- N-well size 2μm
- NW-DPW spacing 2μm

Techno	Sensor capacitance
TJ180nm	2.67fF
BCIS90nm	1.70fF
GSMC130nm	2.68fF
Modified-TJ180nm	1.97fF

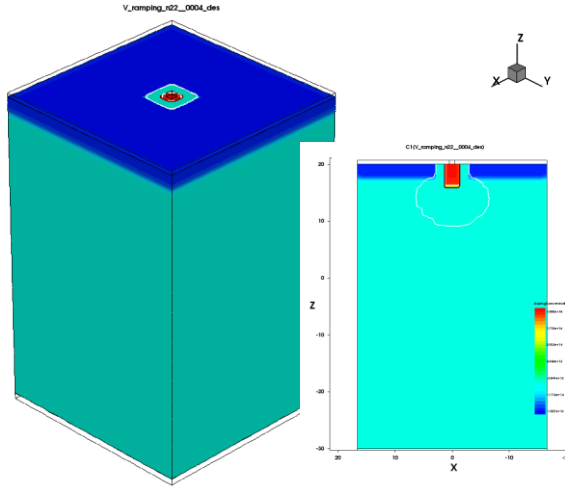
V_{nw}=0.8V V_{sub}=-6V



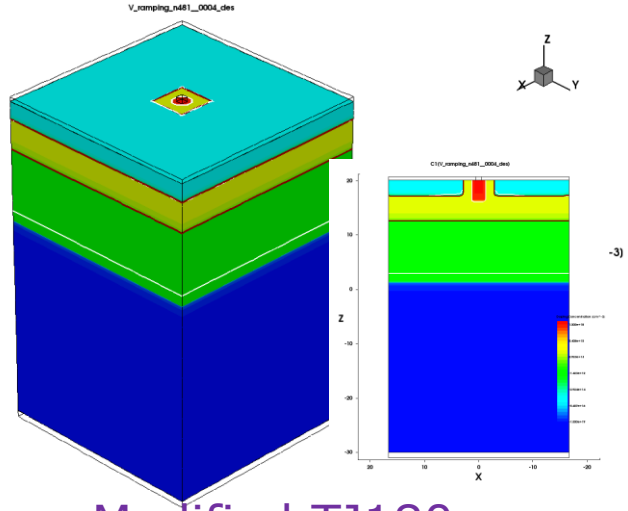
TJ180nm



BCIS90nm



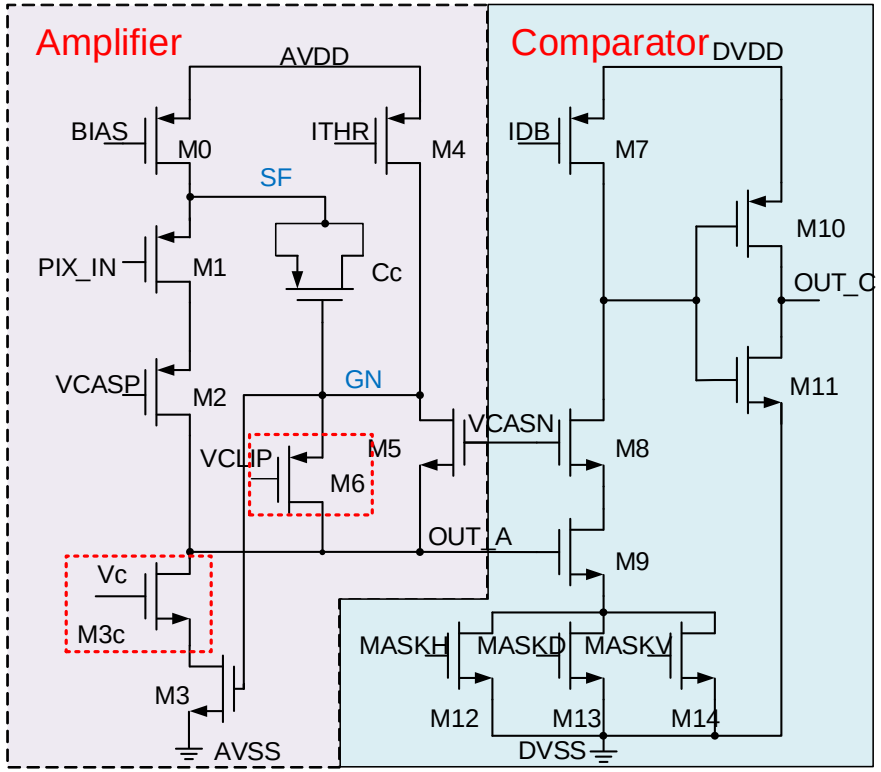
GSMC130nm

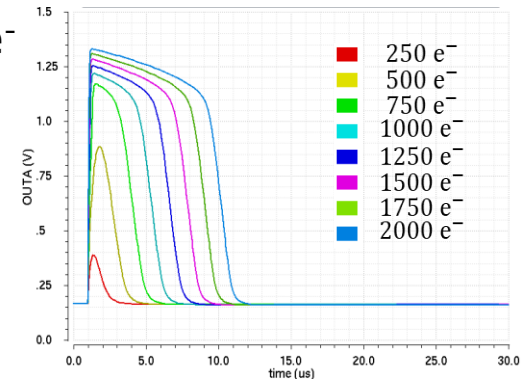


Modified-TJ180nm
(for comparison)

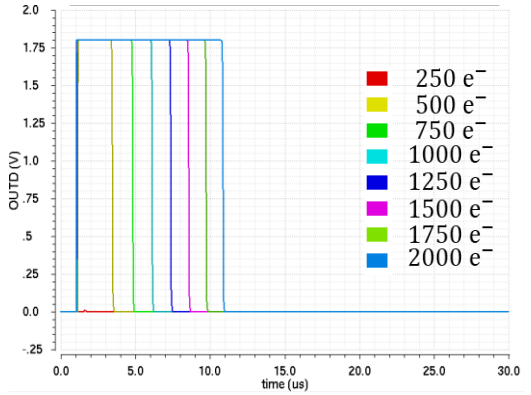
TJ180-Analog Front-end

- Open-loop amplifier + current comparator (referencing ALPIDE and TJ-Monopix)
- For 170×30 n-well connect pixel
  - Threshold=309.0e⁻, ENC=11.4e⁻, MISMATCH=5.7e⁻
  - Analog power consumption ~26 mW/cm²

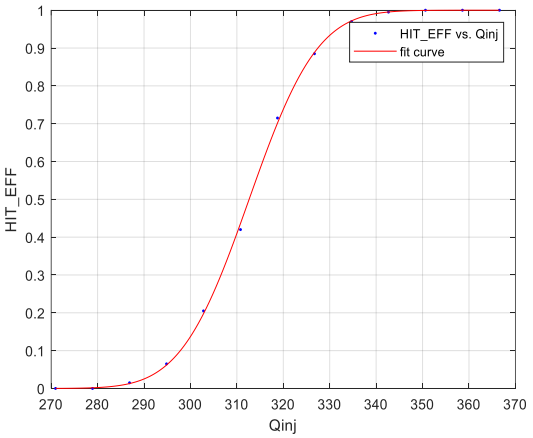


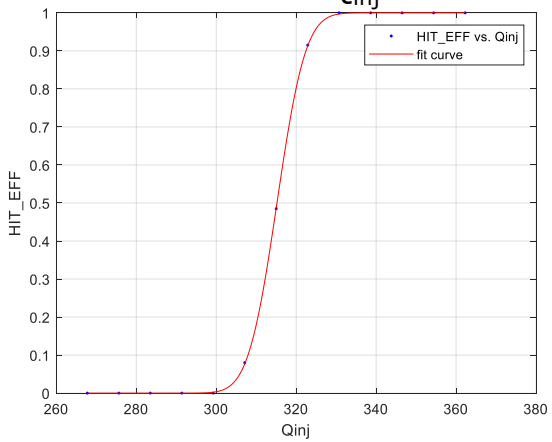


OUTA waveform under different Q_{inj}



OUTC waveform under different Q_{inj}



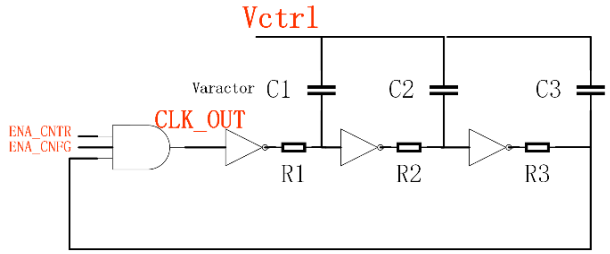


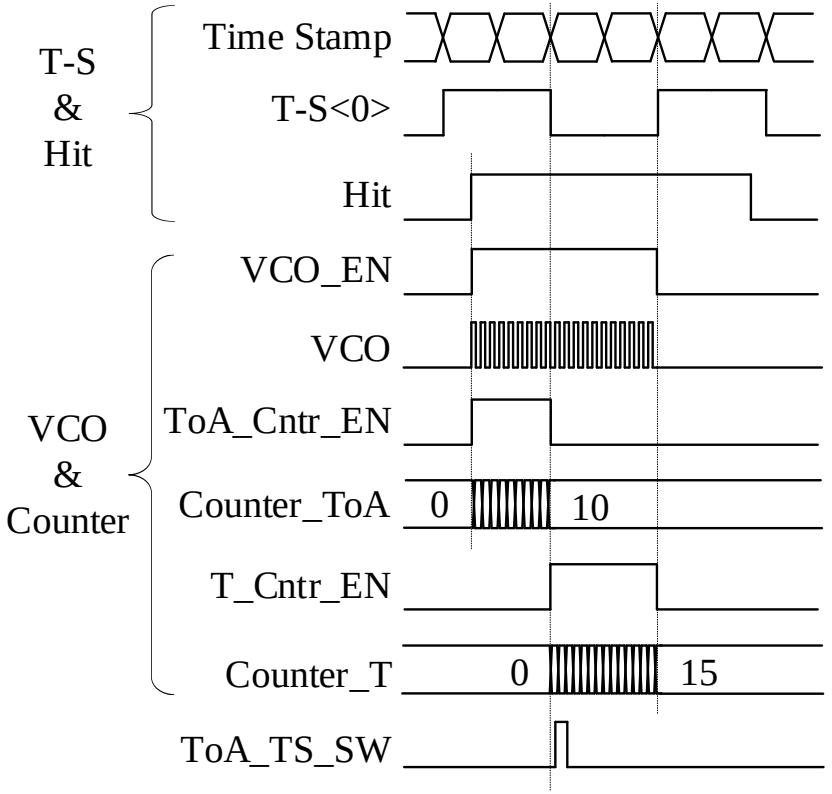
BCIS90-Fine timing with VCO

- Gated VCO in each pixel with 500MHz clock
- VCO counts recorded between
  - Hit LE and system clock rising edge
  - System clock low bit flip
- In pixel time info:
  - 8-bit LE & 8-bit TE coarse timestamp
  - **6-bit TOA VCO count**
  - **6-bit Clock Period VCO count**

VCO frequency calibration

- $ToA = ToA_{TS} - \frac{N_{counter}^{ToA}}{N_{counter}^{T}} \cdot \frac{T_{TS<0>}}{2}$
  - ✓ Accurate TOA timing independent of VCO frequency
- Timing ability σ_{ele}~9.45ns (metal line connect)





MAPS simulation-Charge collection

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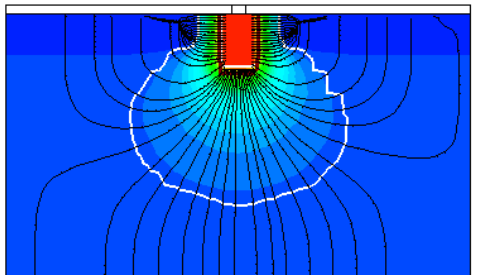
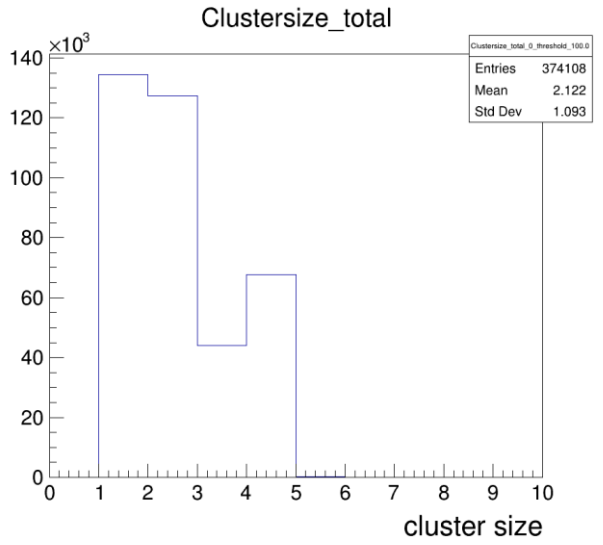
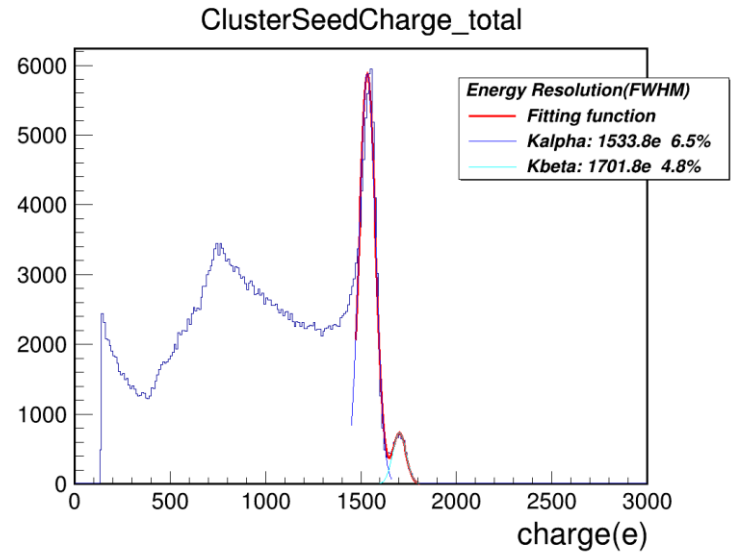
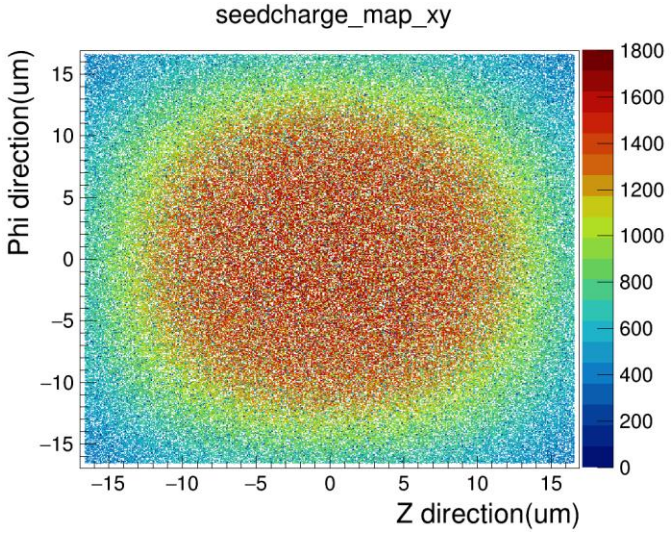
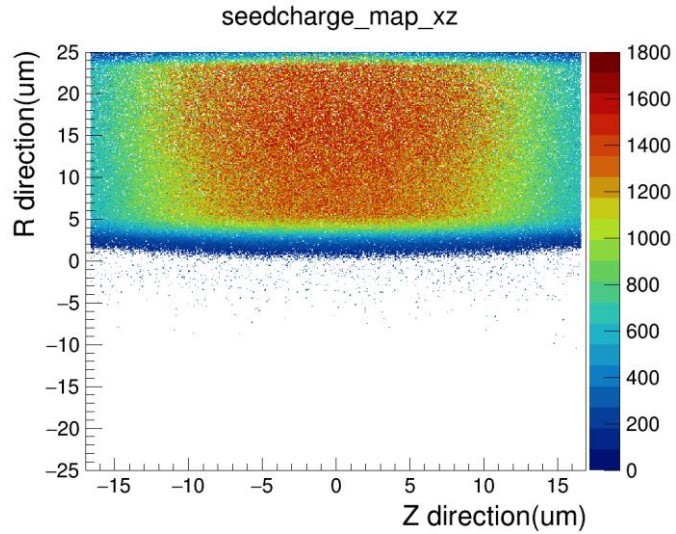
- Fe-55 X-ray incident, result for **TJ180nm small pixel**
- Good energy resolution for 5.9keV X-ray expected
- Charge collection largely depend on depletion volume & in-pixel position
- Insights for MAPS optimization:
  - Larger spacing
  - Individual n-well diode implant
  - Extra n-blanket layer











ITKM geometry

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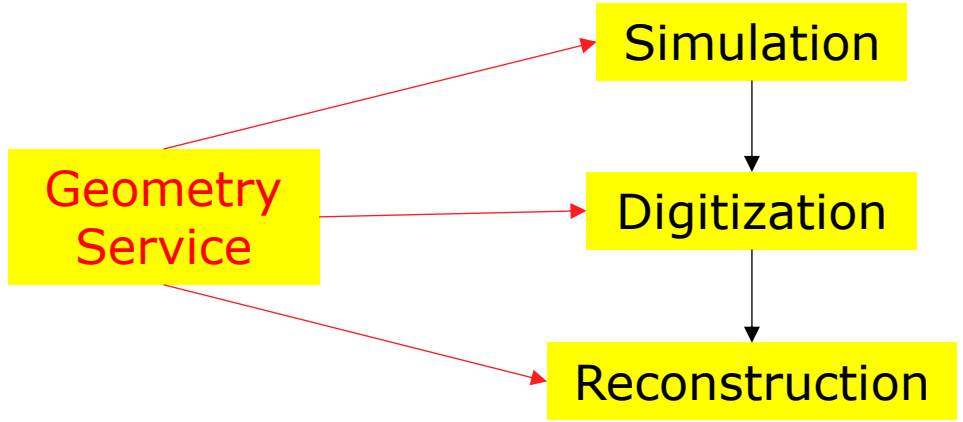
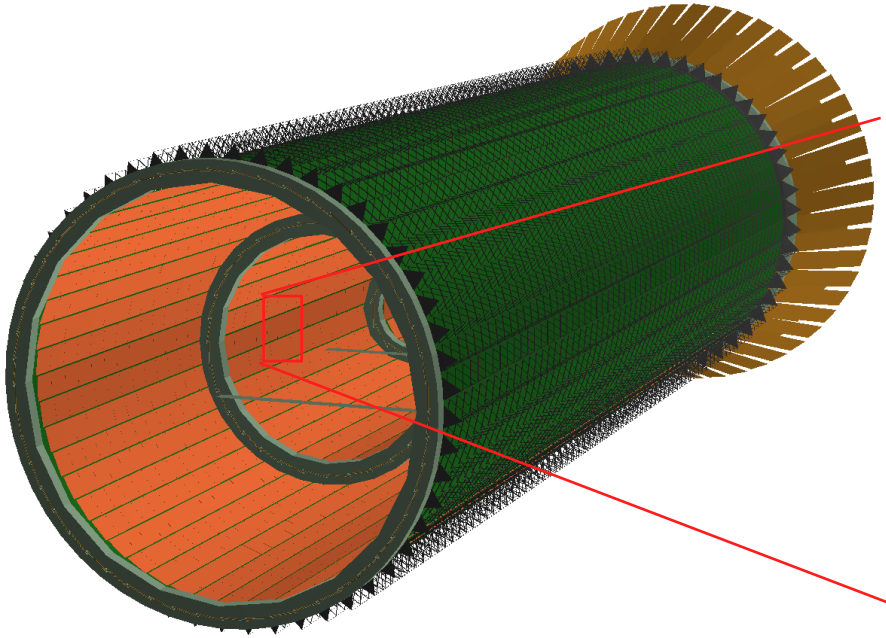
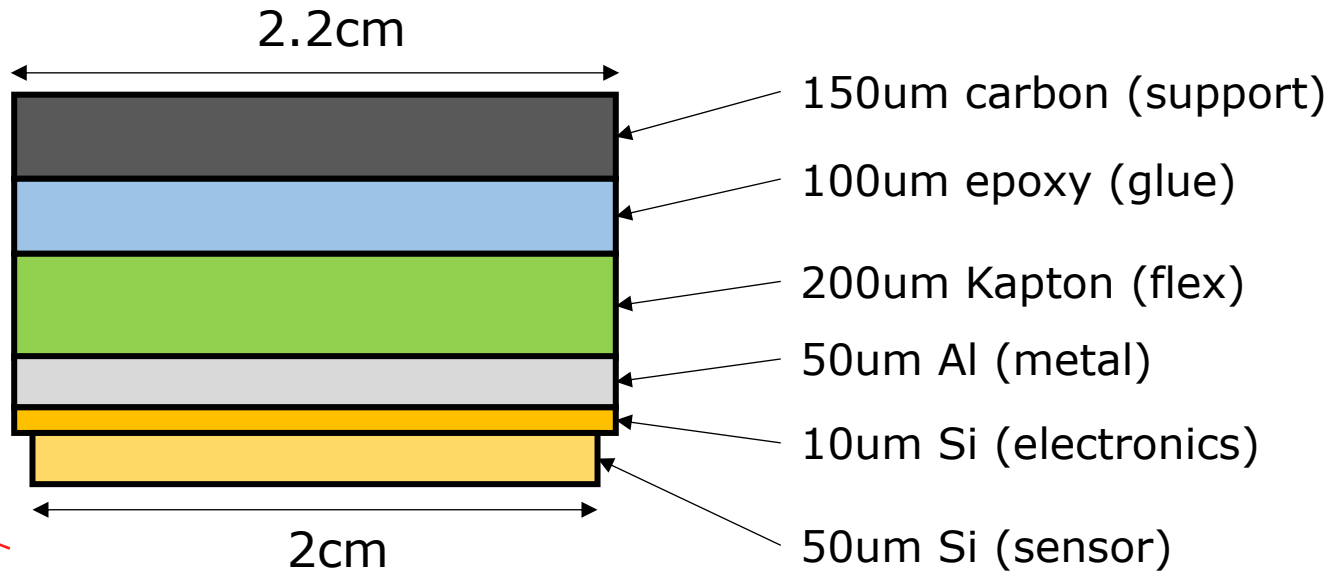
- Geometry constructed by DD4hep
  - Stave width 2.2cm
  - Chip size 2×2 cm^2
  - Pixel geometry: 170×30 μm^2 TJ180nm techno
  - Material budget **0.27% X_0** per layer

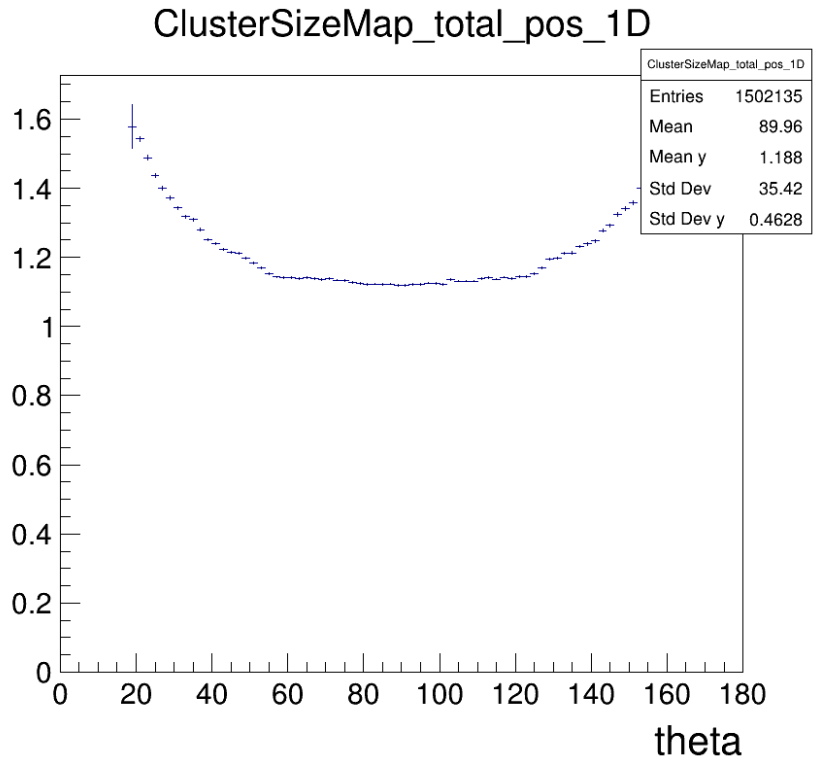




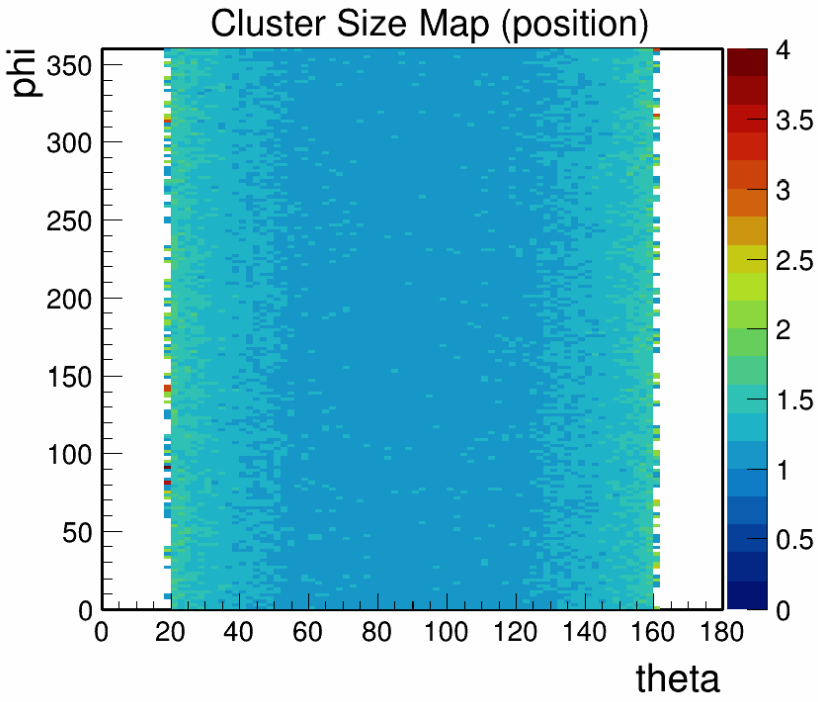


Cluster size

- Simulation settings:
  - 1GeV μ^-, θ range 20° -160°
  - Pixel threshold: 300e$^-$



Cluster size vs. polar angle

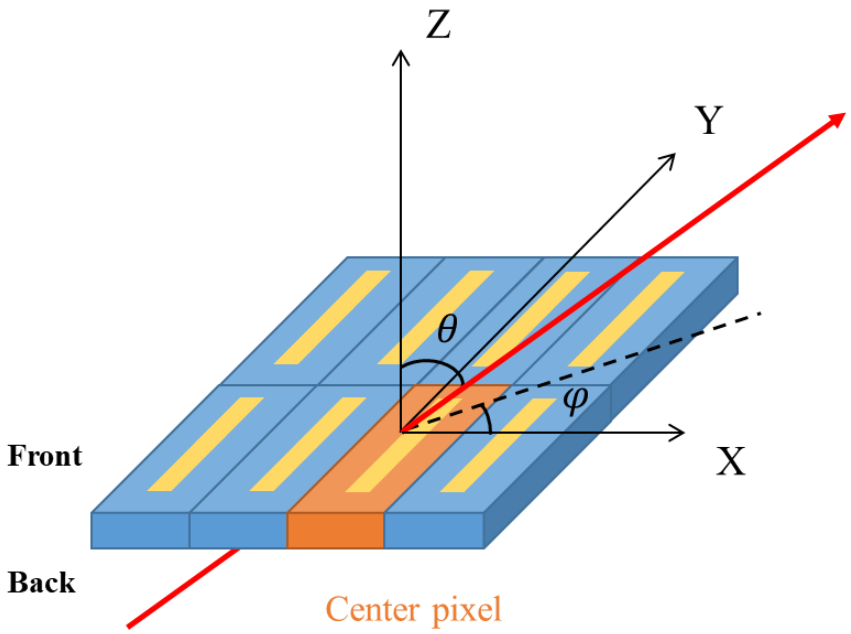


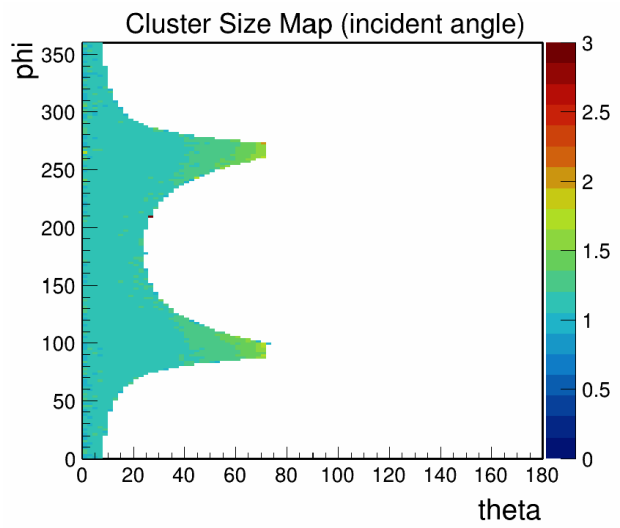
Cluster size vs. polar & azimuthal angle

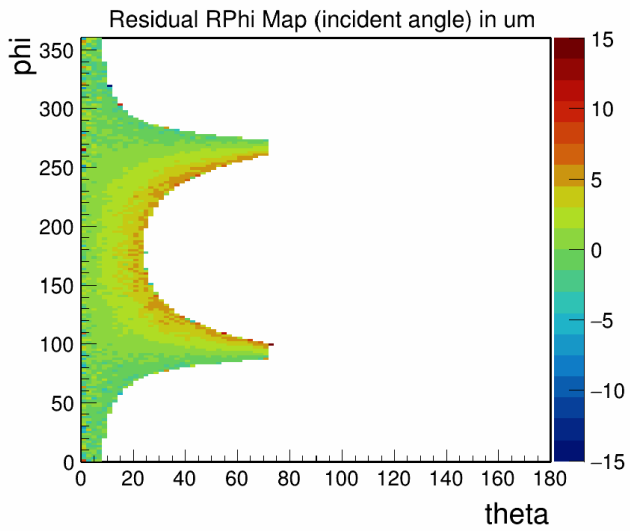
Average cluster size 1.19

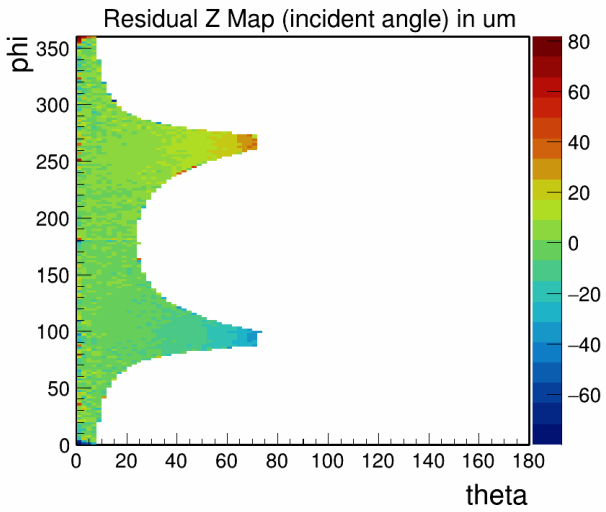
Clustering performance in local coordinate

- Simulation settings:
  - 1GeV μ^-, θ range 20° -160°
  - Pixel threshold: 300e$^-$









ITKM background estimation

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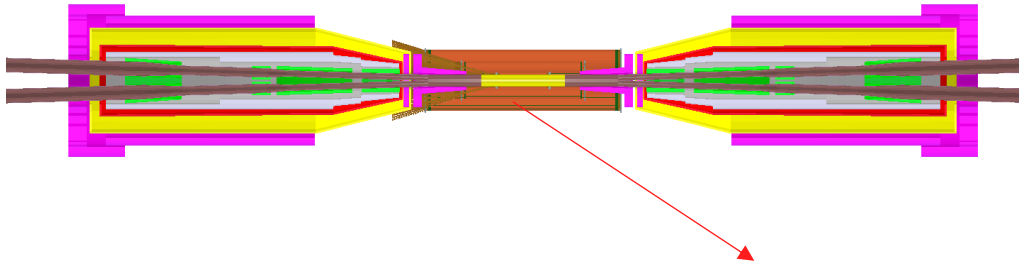
- Background simulation carried out under OSCAR framework
- Three types of backgrounds combined: **Touschek (main background), Luminosity, Beam-gas**
- Background hit rate in terms of fired pixels @ 300e^- threshold



Three layers of ITKM

	Average hit rate per unit area / (kHz/cm^2)	TID/ (Mrad/y)	NIEL/ (n_{eq}/cm^2/y)
ITKM1	671.0	0.585	3.44×10^{10}
ITKM2	20.44	5.54×10^{-3}	7.86×10^{9}
ITKM3	3.35	8.93×10^{-4}	1.05×10^{10}

Values are likely to vary due to interaction region re-design