Karlsruhe Institute of Technology

Electronics and On-Detector Processing

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State-of-the-Art Data Acquisition Systems

Complex system based by custom off-detector readout cards

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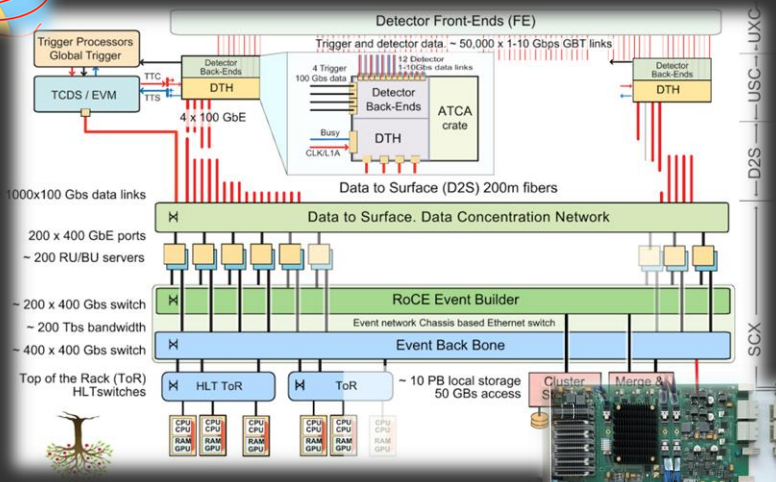
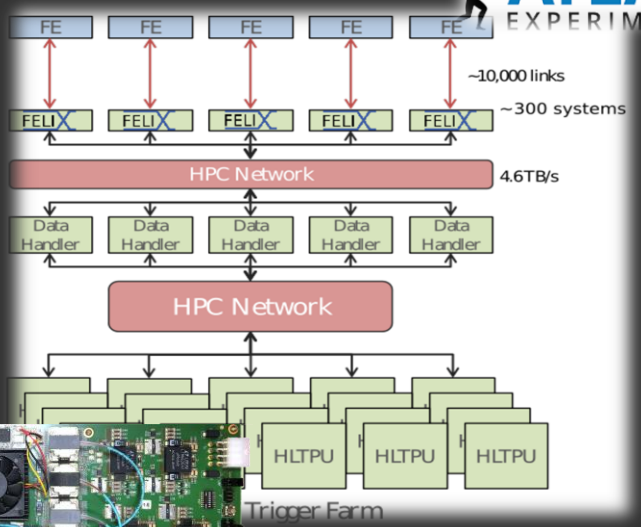
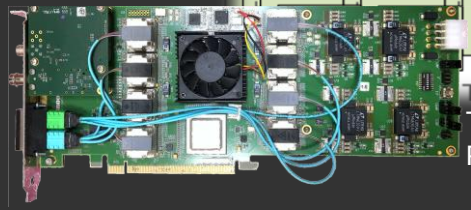
CMS Phase II Upgrade



The DTH400 board prototype-2 together with the companion Rear Transition Module (RTM) housing the embedded controller

Atlas Phase II Upgrade - LHC Run 3 and 4





The Felix PCIe readout card 16-lane PCIe Gen3 interface (120 Gb/s)

- Up to eight complex ATCA readout cards have been developed to manage the full CMS data and trigger systems. In contrast, ATLAS has adopted a more standardized approach, though it significantly differs from the CMS methodology

Outline

Electronics and On-Detector Processing

- **Leveraging COTS Devices for DAQ Systems:**

  How can we effectively utilize Commercial Off-The-Shelf (COTS) components—such as CPUs, GPGPUs, FPGAs, and AI accelerators—to simplify and enhance the efficiency of Data Acquisition (DAQ) systems?

- **Designing a Versatile Off-Detector Readout Card:**

  What design strategies can enable the development of an off-detector readout card that is flexible enough to be deployed across multiple experiments, paving the way for a standardized hardware solution?

- **Future Detector Technologies:**

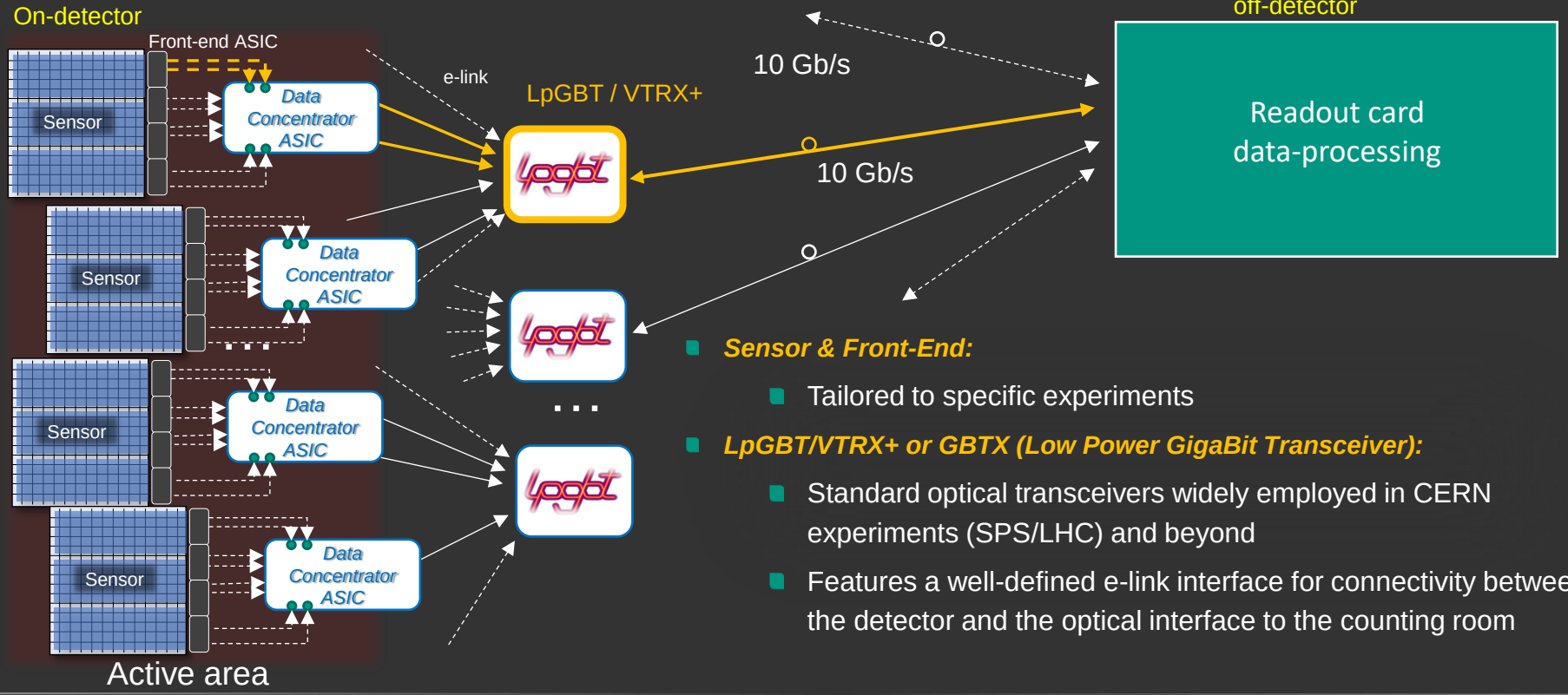
  What are the emerging detector technologies for next-generation experiments, and how can their evolution be anticipated to meet the needs of future research?

- **Impact on DAQ Systems:**

  How will these advancements in detector technologies influence the future of DAQ systems, toward a more **software-defined architecture**? What steps can be taken now to prepare for this transition?

Towards to readout chain simplification

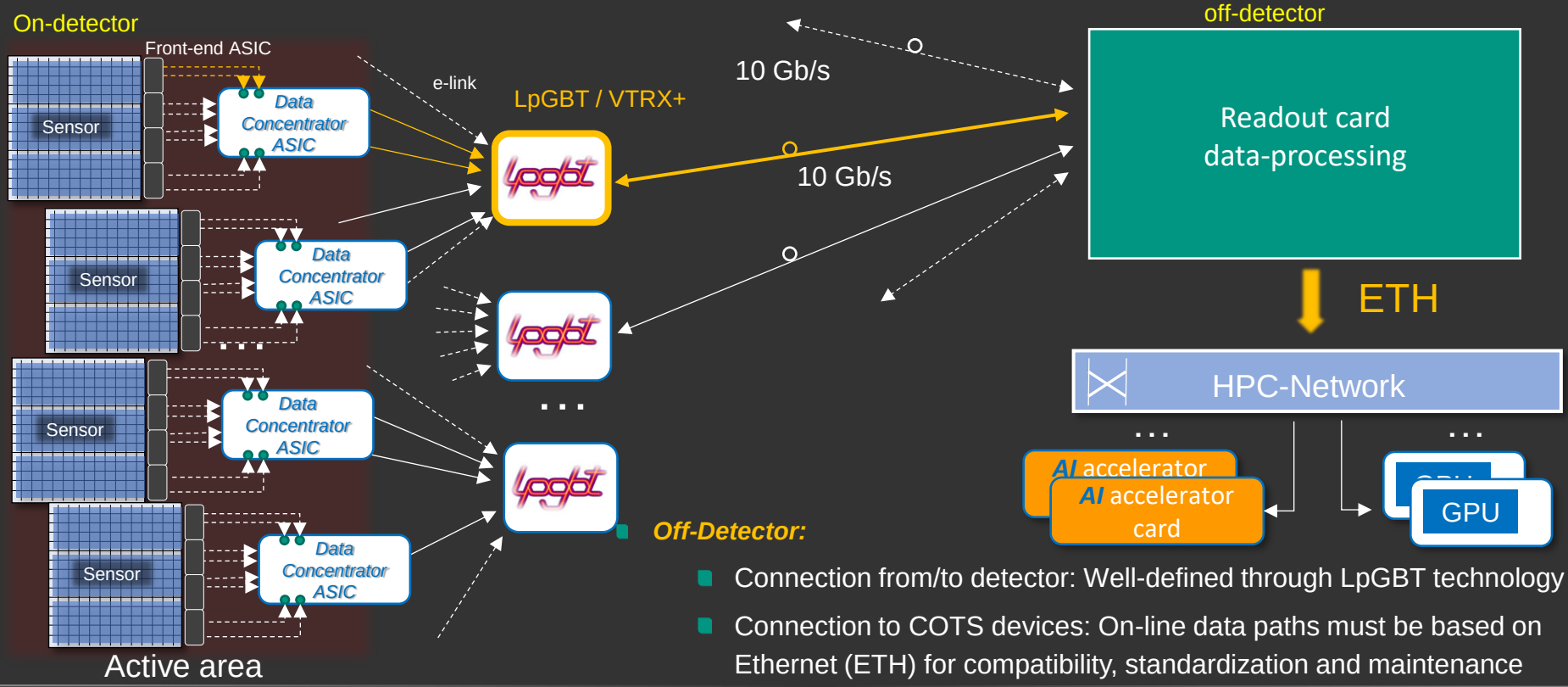
"Common" hardware readout with advanced data processing



- ***Sensor & Front-End:***
  - Tailored to specific experiments
- ***LpGBT/VTRX+ or GBTX (Low Power GigaBit Transceiver):***
  - Standard optical transceivers widely employed in CERN experiments (SPS/LHC) and beyond
  - Features a well-defined e-link interface for connectivity between the detector and the optical interface to the counting room

Towards to detector layout simplification

“Common” hardware readout with advanced data processing

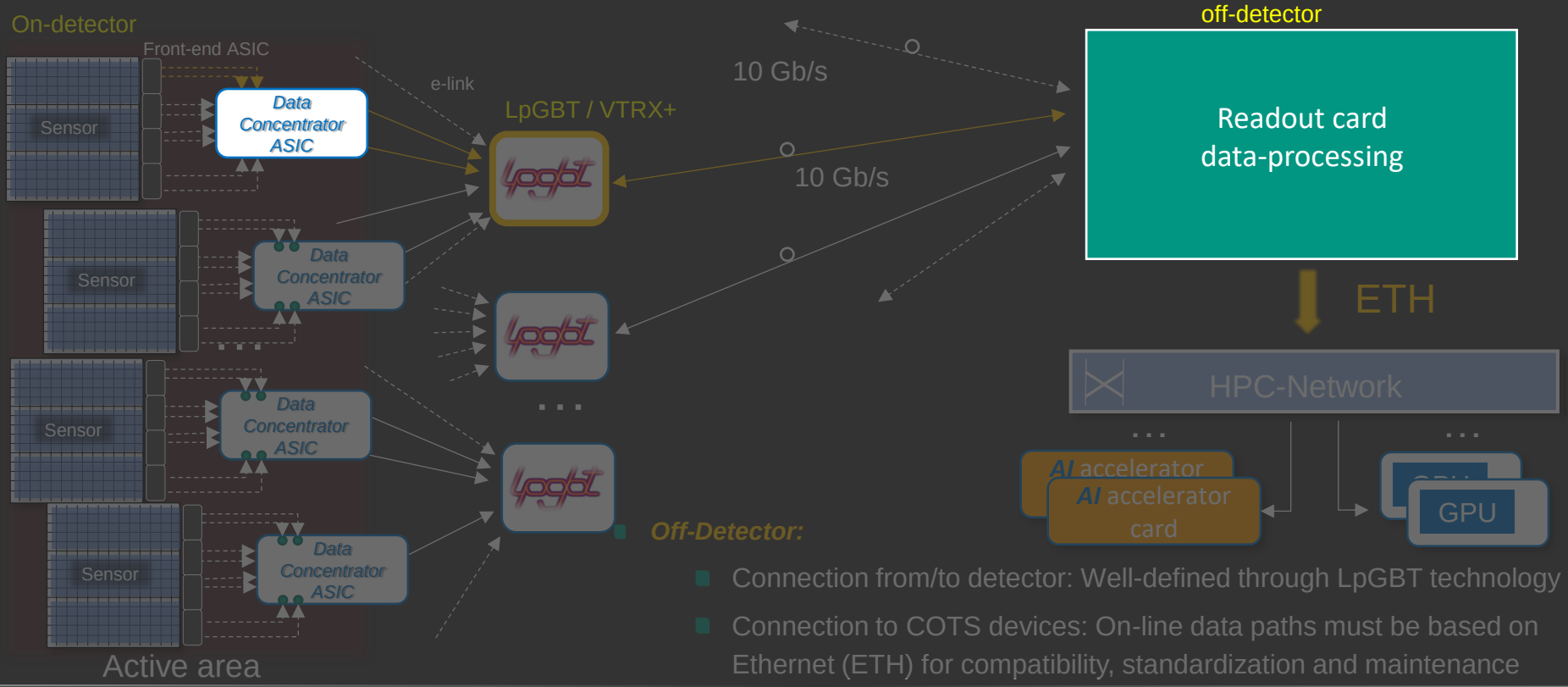


Off-Detector:

- Connection from/to detector: Well-defined through LpGBT technology
- Connection to COTS devices: On-line data paths must be based on Ethernet (ETH) for compatibility, standardization and maintenance

Towards to detector layout simplification

“Common” hardware readout with advanced data processing



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Towards to detector layout simplification

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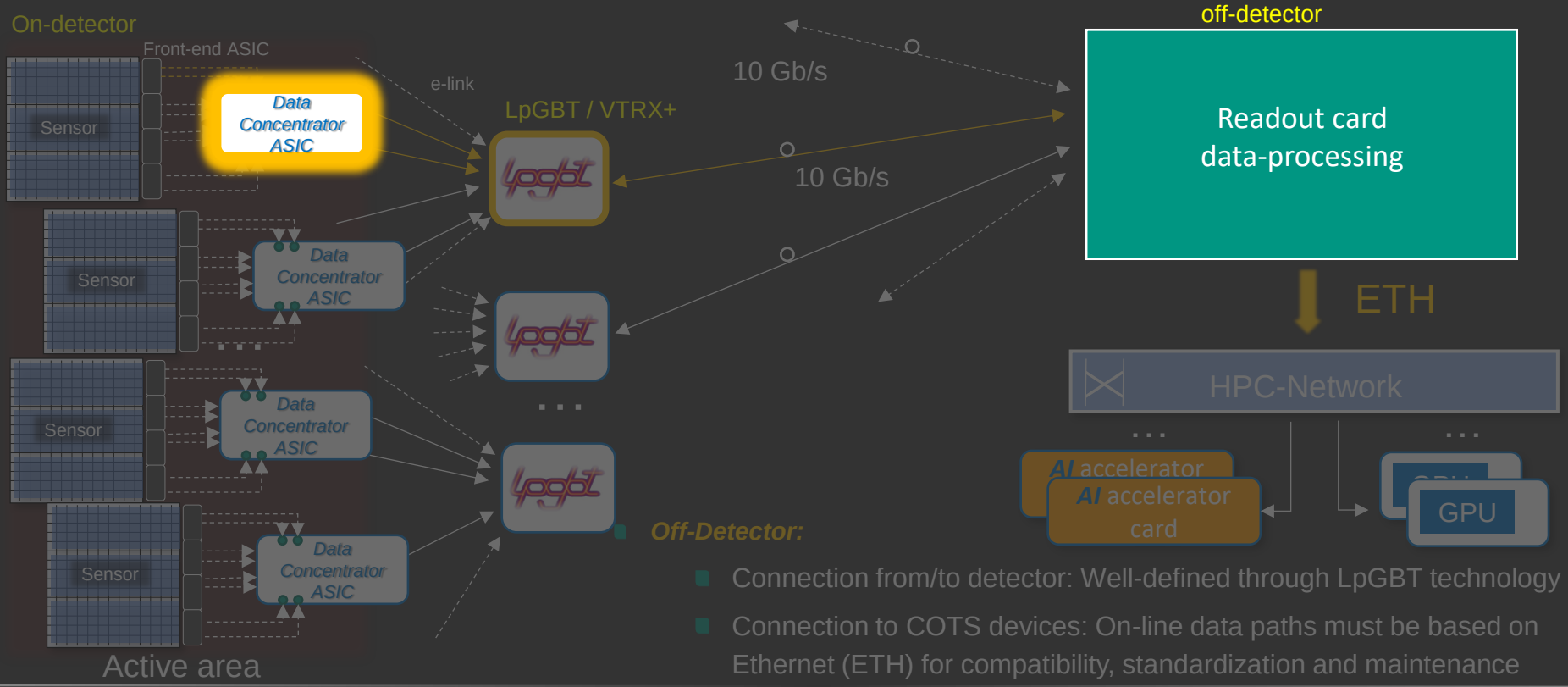

Off-Detector:

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DC (Data Concentrator) - ASIC

Developed for Nuclear and Hadronphysics experiment, like .. PANDA

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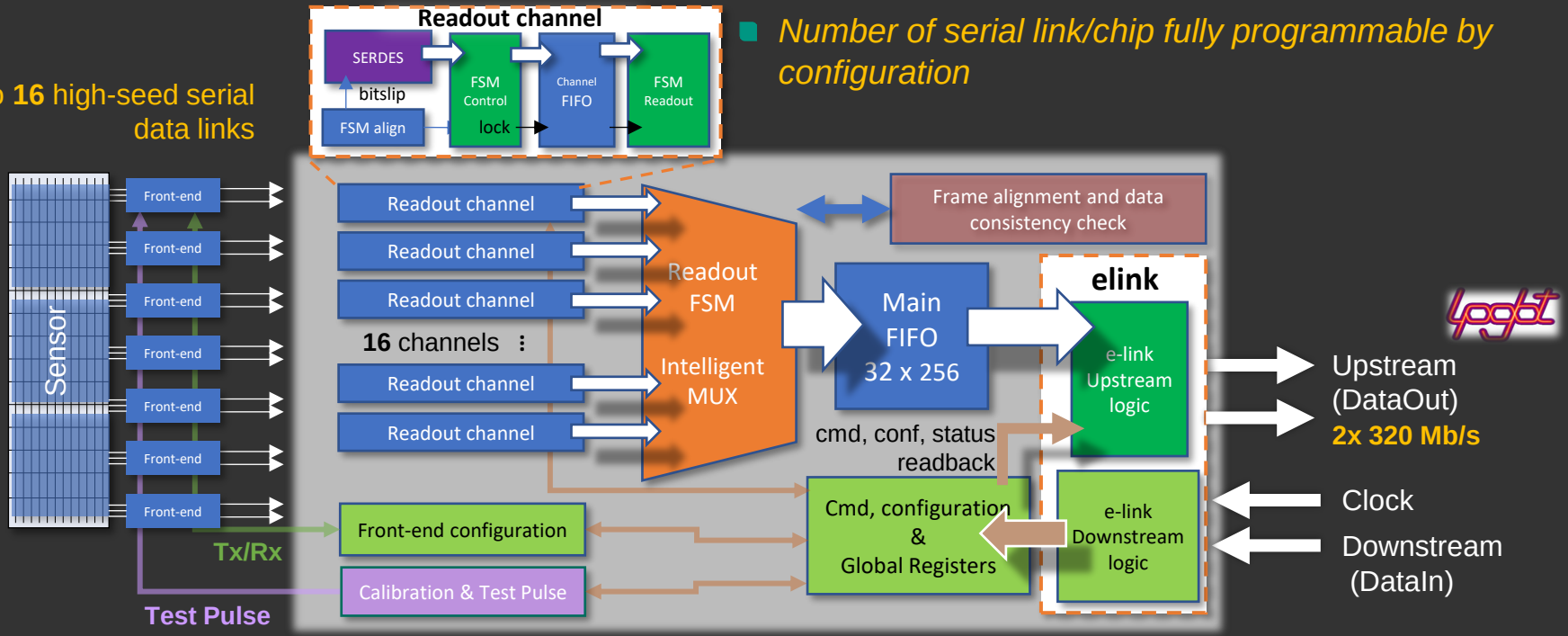
- *Number of serial link/chip fully programmable by configuration*



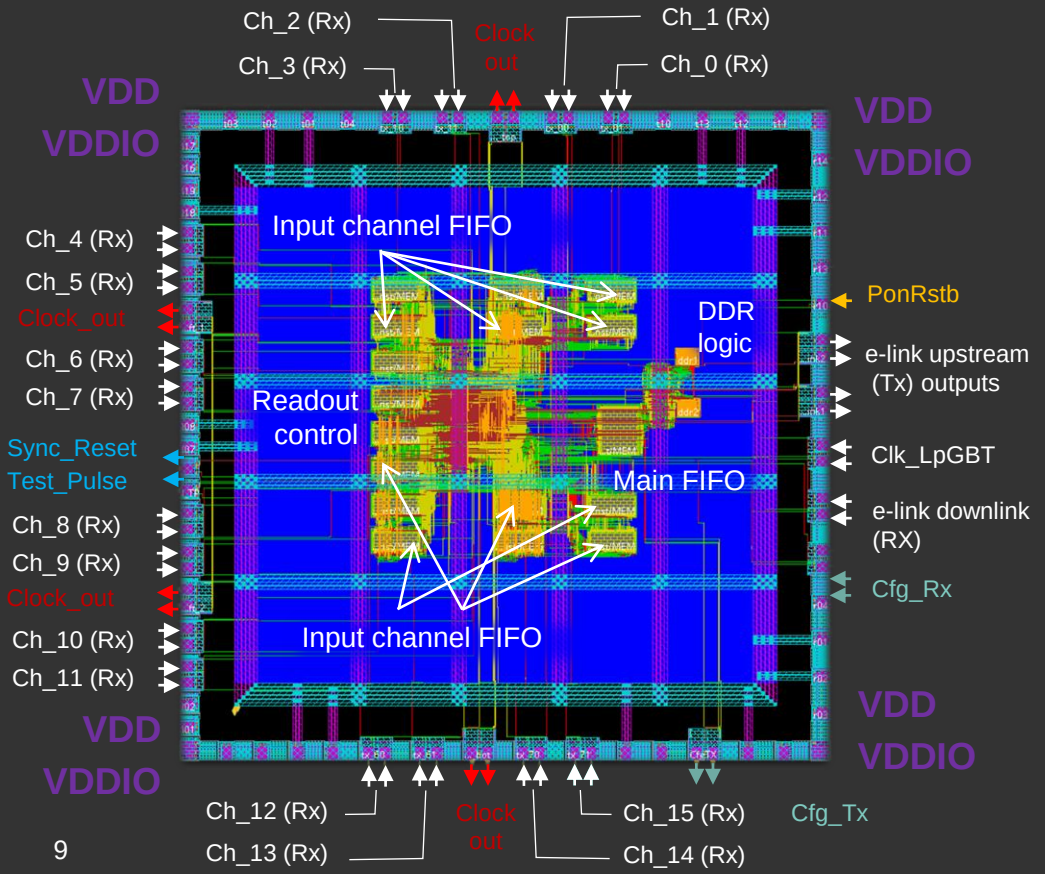
Sensor and front-end

DC ASIC architecture

E/O link interface

MDC current version

Floorplan ASIC and connections

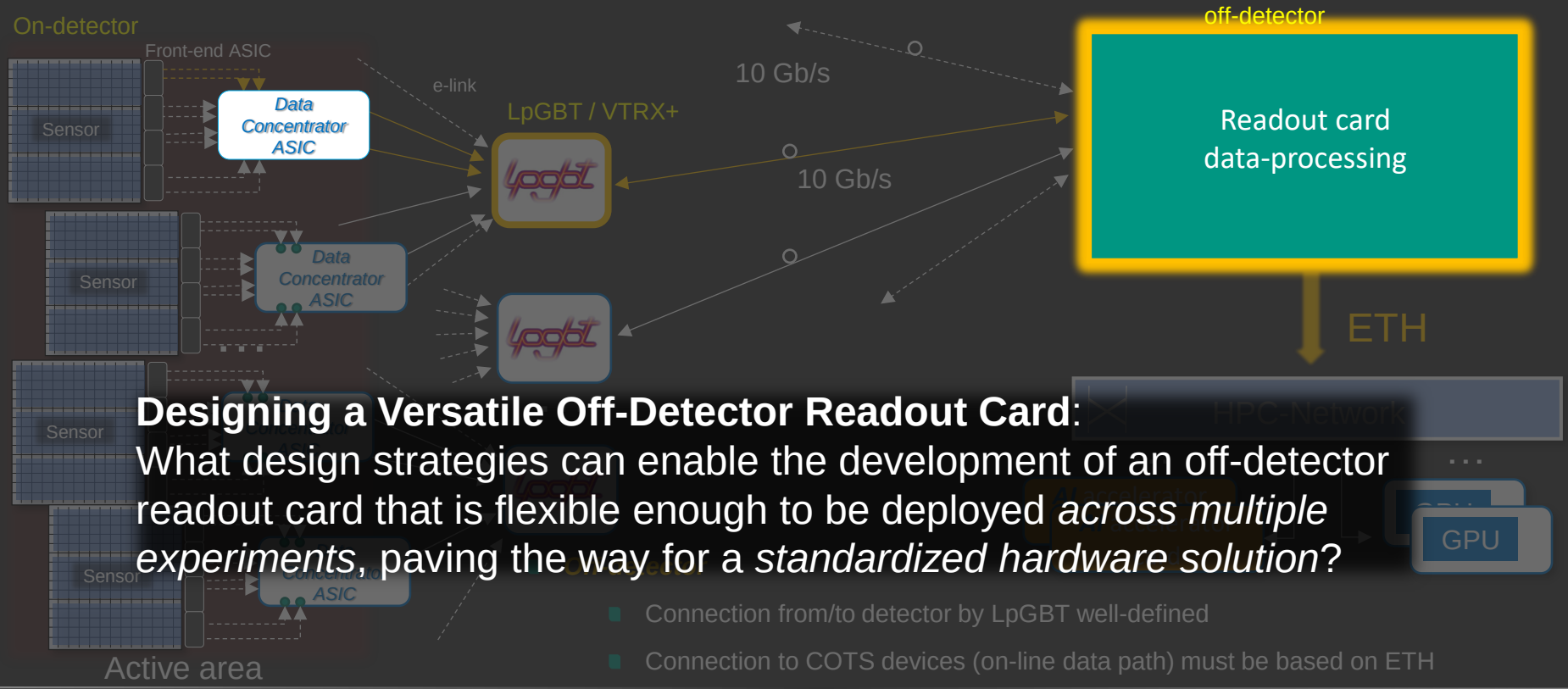


- Die size of 3.38 x 3.38 mm^2
- Low-power CMOS technology
- Double Data rate (block), including the 8b/10b conversion and fast serializer, capable to operate up to 800 Mb/s
- Estimated power (*preliminary*) of 51 mW at a 333 MHz clock toggle rate @ 1.2V
- Area occupancy 3.7% for the logic

The submission of the ASIC is booked for February (2025) in 110 nm CMOS

Towards to detector layout simplification

“Common” hardware readout with advanced data processing



Designing a Versatile Off-Detector Readout Card:
What design strategies can enable the development of an off-detector readout card that is flexible enough to be deployed *across multiple experiments*, paving the way for a *standardized hardware solution*?

- Connection from/to detector by LpGBT well-defined
- Connection to COTS devices (on-line data path) must be based on ETH

How can we *unify all standards ?*

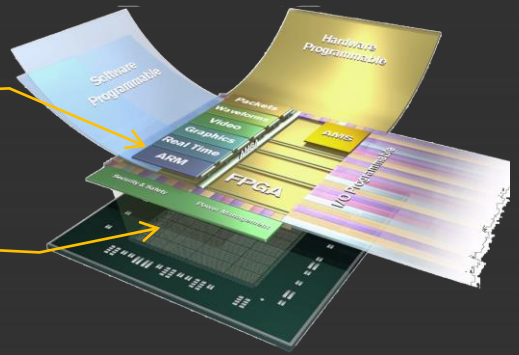
Move towards a common DAQ platform

- Disentangle with multiple standards (ATCA, µTCA, PCIe, ETH and standalone test system) by using of a smart and optimized form factor
- Main processor based on ZYNQ US+
  - Powerful and high-density FPGA programmable layer
  - ARM processors are essential for ***AI***-based training and the intelligent calibration/control of detector

Quad-core ARM 64-bit processor

+

Powerful Field Programmable Gate Arrays (FPGAs)
Developed in 16nm FinFET CMOS technology



AMD-Xilinx Zynq™ UltraScale+™ Multi Processor System-On-Chip devices

- Data upstream to COTS based on standard ETH protocol (100 GbE or more), two possible candidates (UDP/IP and RoCE)

How can we unify all standards ?

Towards a common DAQ platform

Standard-compliant AMC
(Advanced Mezzanine Card) format

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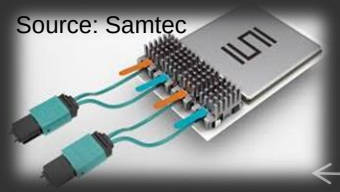
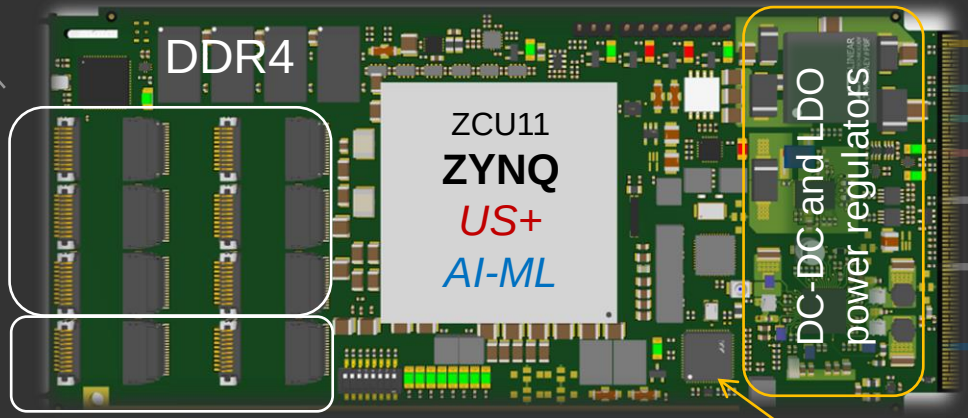
- *Massive optical connection*: from/to detectors fully LpGBT / Aurora compatible
- *Ethernet integration*: 2 x 100 GbE for direct connectivity to COTS devices
- *AI/ML inference capability*: powered by a ZYNQ processor for HW-based AI-ML deployment





36 links
from/to Detetcors
LpGBT @ 10 Gb/s

To COTS
@ 2 x 100 GbE

4 x 25Gb/s

4 x 25Gb/s

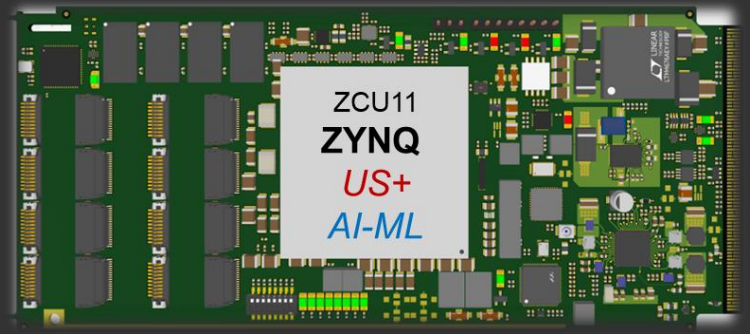
FireFly optical links

Potential to lay the foundation for a standardized off-detector electronics

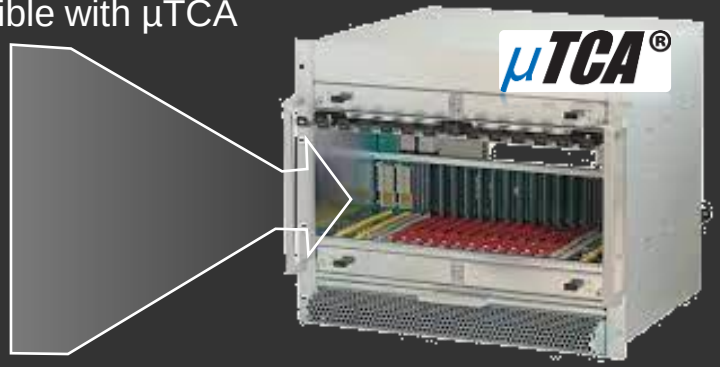
How can we unify all standards ?

Move towards a common DAQ platform

AS-Card (AMC)



Compatible with µTCA



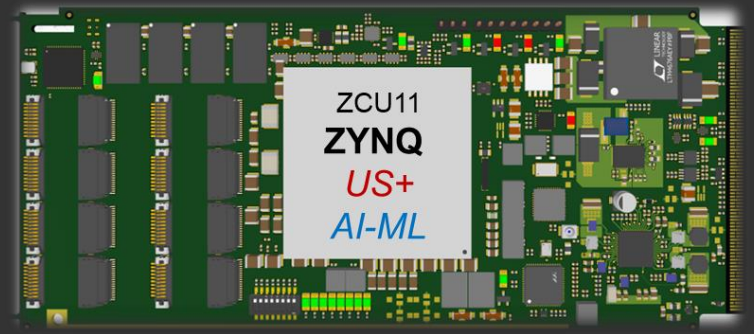
Compatible with many MCH
(MicroTCA Carrier Hub) controllers

- Direct integration of the AMC card in µTCA systems
- Applications:
  - HEP detectors, several sub-detectors at HL-LHC and GSI/FAIR is based on µTCA readout frame
  - Beam diagnostics instrumentations (EuXFEL, FLUTE, FLASH, many others)
  - and … many more …

How can we unify all standards ?

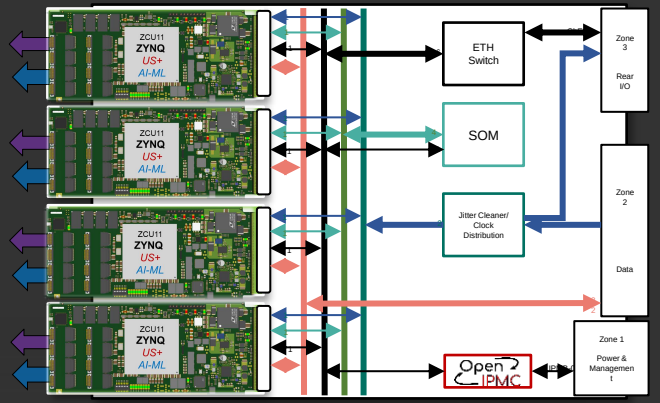
Move towards a common DAQ platform

AS-Card (AMC)



Compatible with ATCA

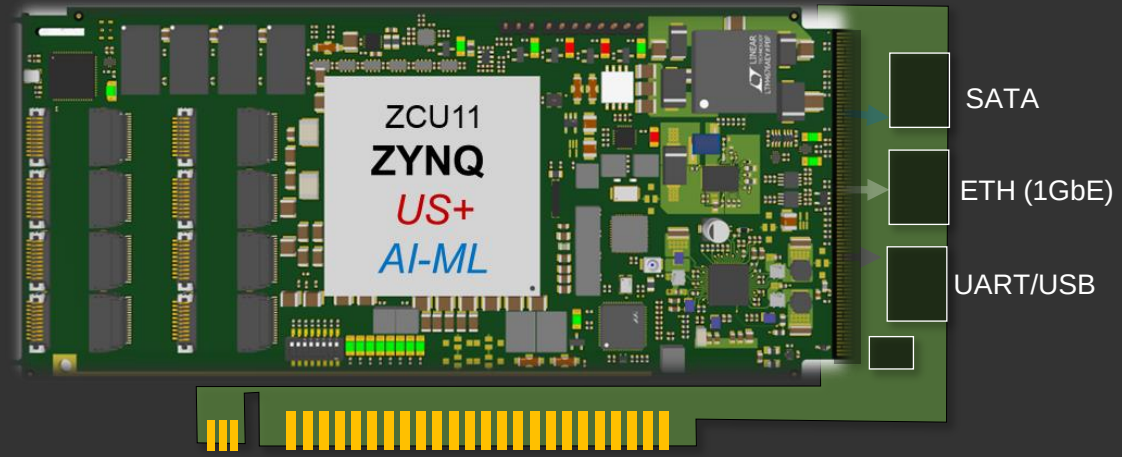
ATCA carrier card (under development at KIT)



- Direct integration on ATCA systems
- Applications:
  - HL-LHC experiments with a higher modularity & scalability
- The system features: # 144 optical links from/to detector + up to 8 data link to DAQ (800 GbE)
  - Which could be extended up to 240 optical links connections

How can we unify all standards ?

Move towards a common DAQ platform



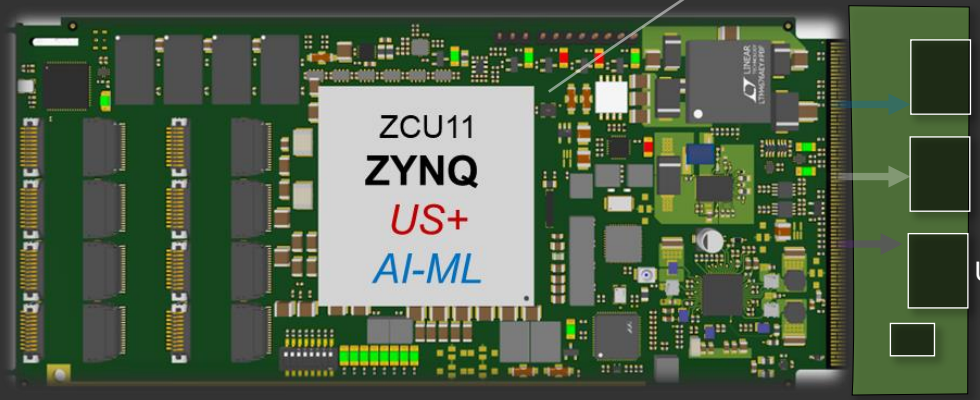
PCIe Gen 4

- Direct integration to PCIe by breakout service card (under design)
- The breakout card includes several useful interfaces, i.e. ETH, SATA and USB

- Applications:
  - Powerful and cost-effective DAQ for compact and smart photon sciences detectors
  - Beam diagnostics instrumentations
- Compute node card for HL-LHC complex detector (i.e. ATLAS, CBM, PANDA, etc.)
- As powerful accelerator card for computer cluster, where *AI-ML algorithms* are deployed

How can we unify all standards ?

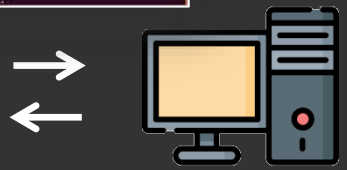
Move towards a common DAQ platform



SATA

ETH (1GbE)

UART/USB



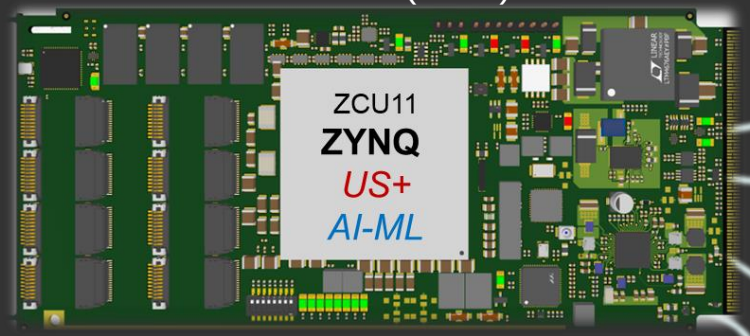
- Simple connection to any PC by ETH (1 GbE) or USB

- Applications:
  - Stand-alone card for lab testing and detector characterization, MPSoC powered by PetaLinux, supporting Python/C++ development deployed on ZYNQ
  - A smart and fast solution designed for beam test setups

How can we unify all standards ?

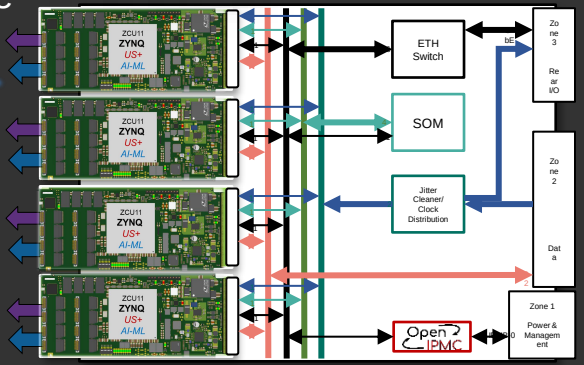
Accelerating Science “common DAQ platform”

AS-Card (AMC)



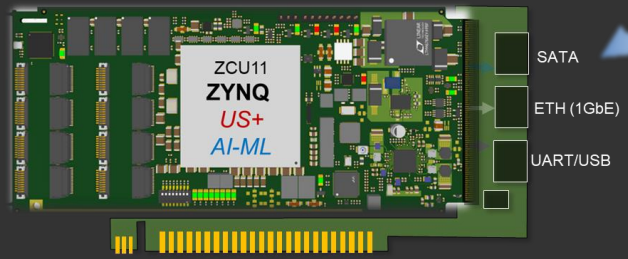
Compatible with µTCA

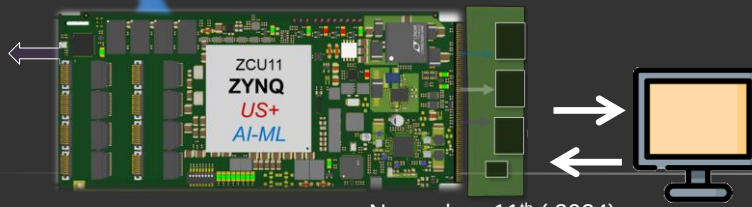
Compatible with ATCA



Standalone DAQ

Compatible with standalone/PCie





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Accelerating Science “common DAQ platform”

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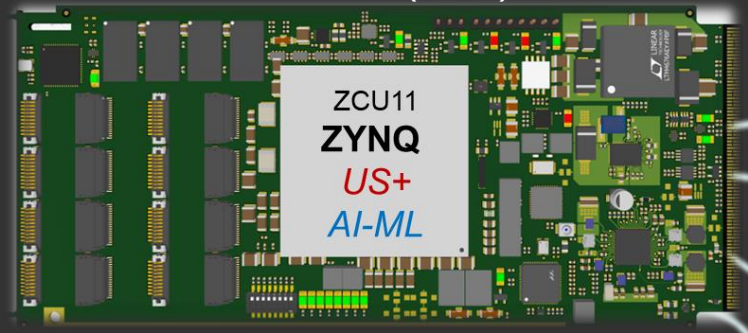
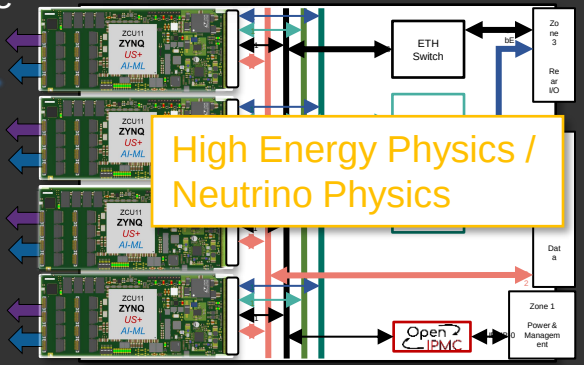


Compatible with µTCA

Accelerator machine (detectors & instrumentations)

Compatible with ATCA

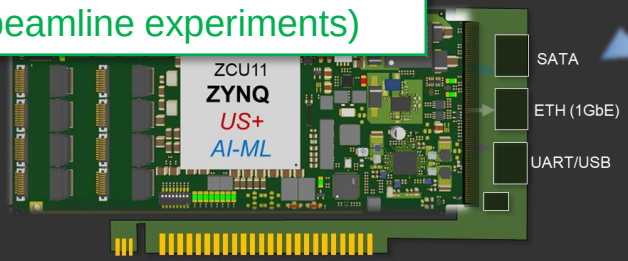


High Energy Physics / Neutrino Physics

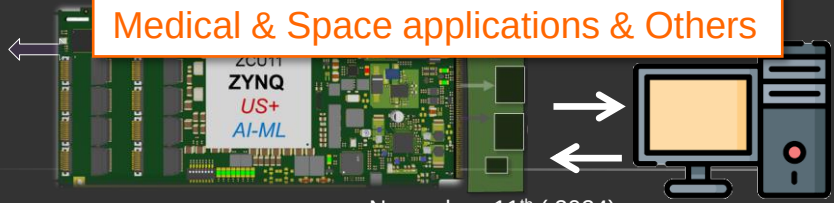
Standalone DAQ

Compatible with tandalone/PCie

Photon Sciences (beamline experiments)



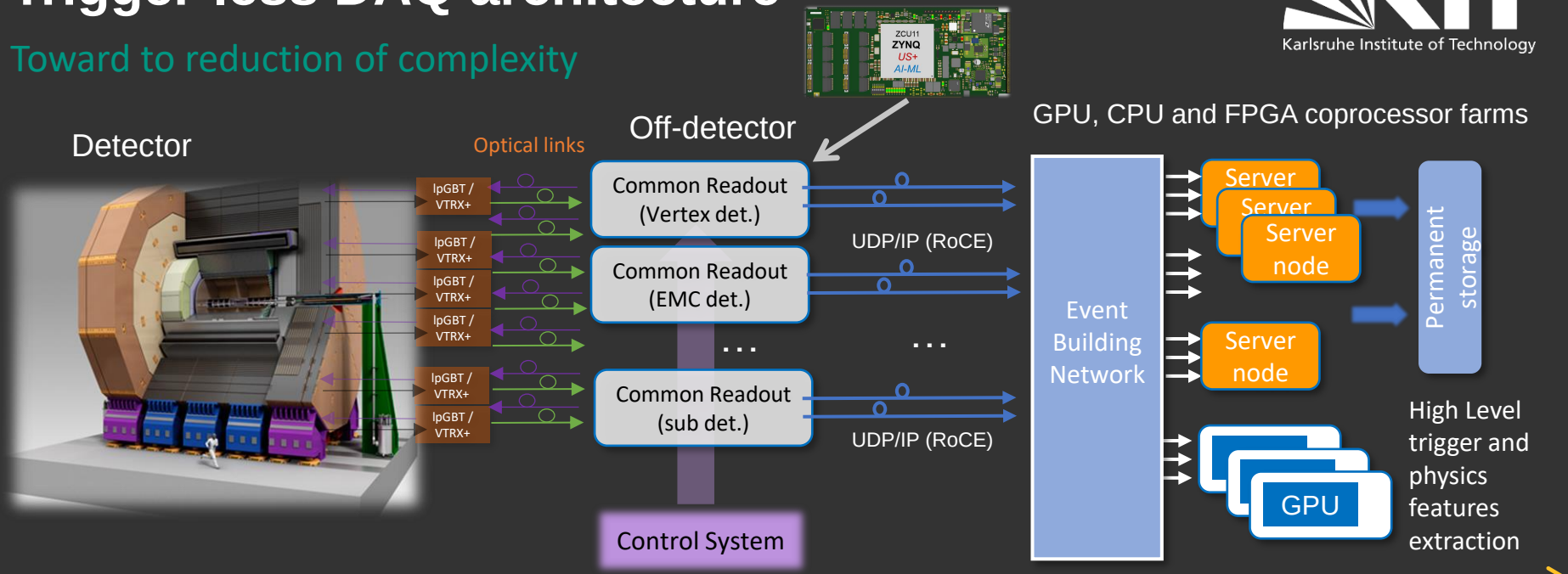
Medical & Space applications & Others



How could the DAQ system potentially be reshaped using this readout card?

Trigger-less DAQ architecture

Toward to reduction of complexity



- Dramatic reduction of custom hardware layers,
  with a single card handling the readout for all detectors and experiments
- Progressing toward a software-defined acquisition architecture, the entire online data path is managed exclusively by COTS (Commercial Off-The-Shelf) devices

FTCF2024-Guangzhou

FUTURE DETECTOR TECHNOLOGIES IN FUTURE TERASCALE EXPERIMENTS

Emerging technologies for future DAQ systems

Driven by the progress of CMOS technologies

Since data acquisition is so close to the hardware, it has to adapt constantly to the dramatic technological evolution which we are witnessing everyday

- Many FPGA and ARM vendors are shifting from producing large to "***TinyFPGA***"
  - Driven by market demand for compact, low-power solutions
- FPGA/RISC-V produced in 7 nm or 16 nm FinFET CMOS technologies
  - Which are intrinsic tolerant (TID)
- With a low material budget (bare-silicon die, available)
  - It could potentially be integrated directly onto the detector module

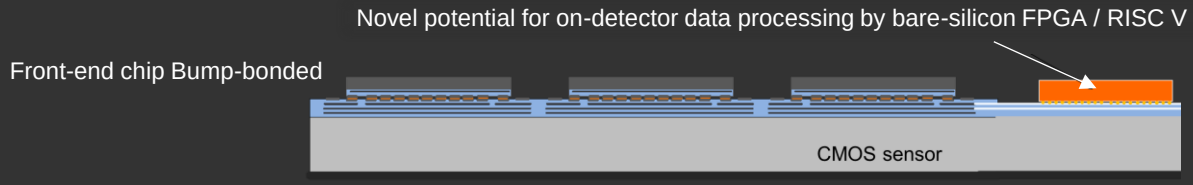
Achronix Speedster7t

- ARM processor for intelligent on-detector electronics, make it very flexible for new application
- i.e. PolarFire (Microchip), Achronix (Speedster7t), many others …

Emerging technologies for future DAQ systems

Driven by the progress of CMOS technologies

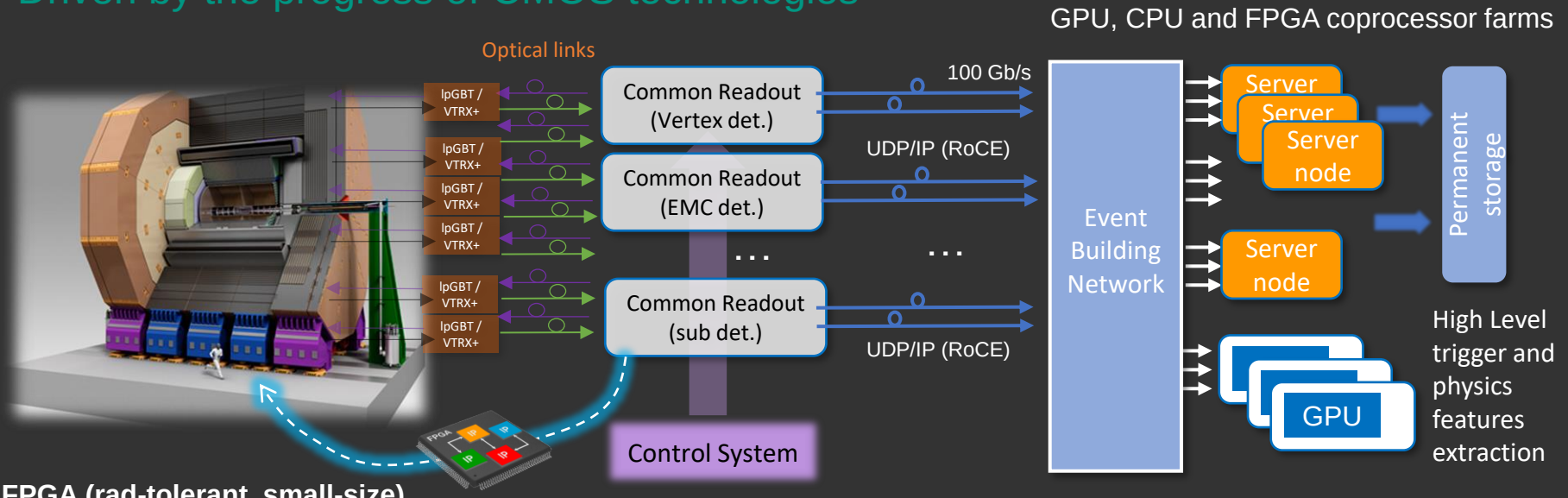
- **Advanced 2.5D/3D/chiplet integration on detector module**
- **Chiplet** is a revolutionary trend in semiconductor devices
- Mature Processes: Technologies like TSV (Through-Silicon Via), RDL (Redistribution Layer), and bump-bonding/hybridization have reached maturity
- Cost Accessibility: These processes are now offered at a reasonable cost, making them more accessible
- Attraction to HEP Community: The affordability and maturity of these technologies are driving increased interest from the High-Energy Physics (HEP) community



SOPHIE project, funded by HELMHOLTZ Innovation pool

Novel DAQ architecture

Driven by the progress of CMOS technologies



FPGA (rad-tolerant, small-size)

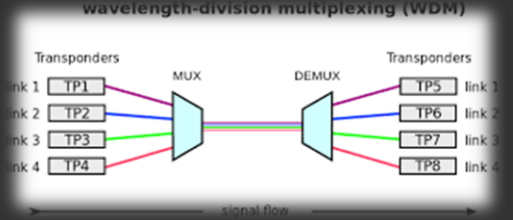
- Move data processing close to data source
- Towards more intelligent front-ends → enhancement of front-end programmability and configurability
- Advanced data processing based on traditional or ***ML*** algorithms (on-detector)
  - On-detector advanced data reduction techniques → reduction of mass and power

Emerging technologies for future DAQ systems

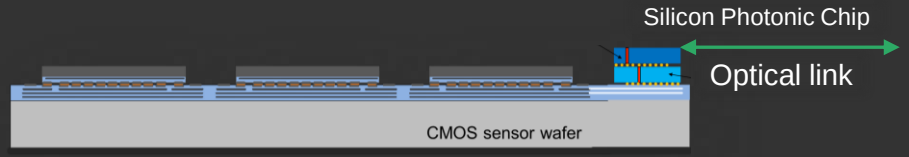
Driven by the progress of CMOS technologies

- **Advanced Silicon Photonics with Wavelength-Division Multiplexing (WDM):**
- Lane speeds of 25 Gbps NRZ or 50 Gbps PAM4, similar to standard commercial Ethernet optical data links
- Fiber capabilities for readout of large-area detectors using only a few fibers (**100** Gbps / **200** Gbps)
- Significant reduction in the number of optical fibers and off-detector cards required
- Enhanced energy efficiency, optimizing data transmission for large-scale systems.

SOPHIE project, funded by HELMHOLTZ Innovation pool

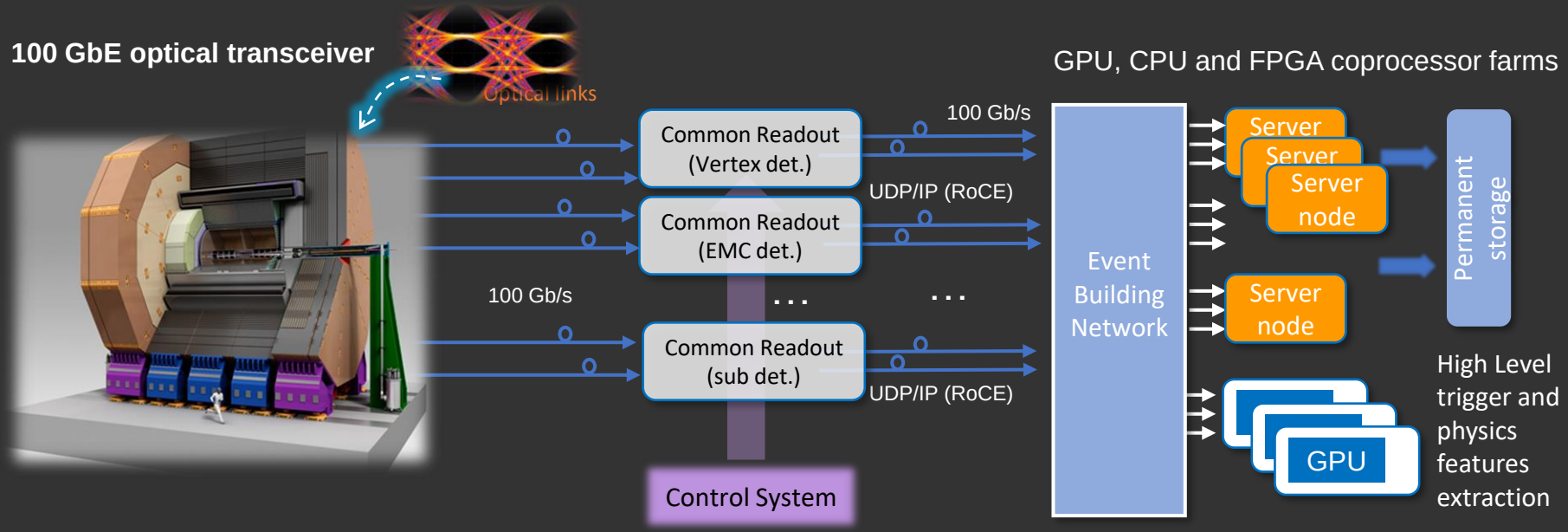


WDM ring resonators with different and tuneable resonator wavelengths



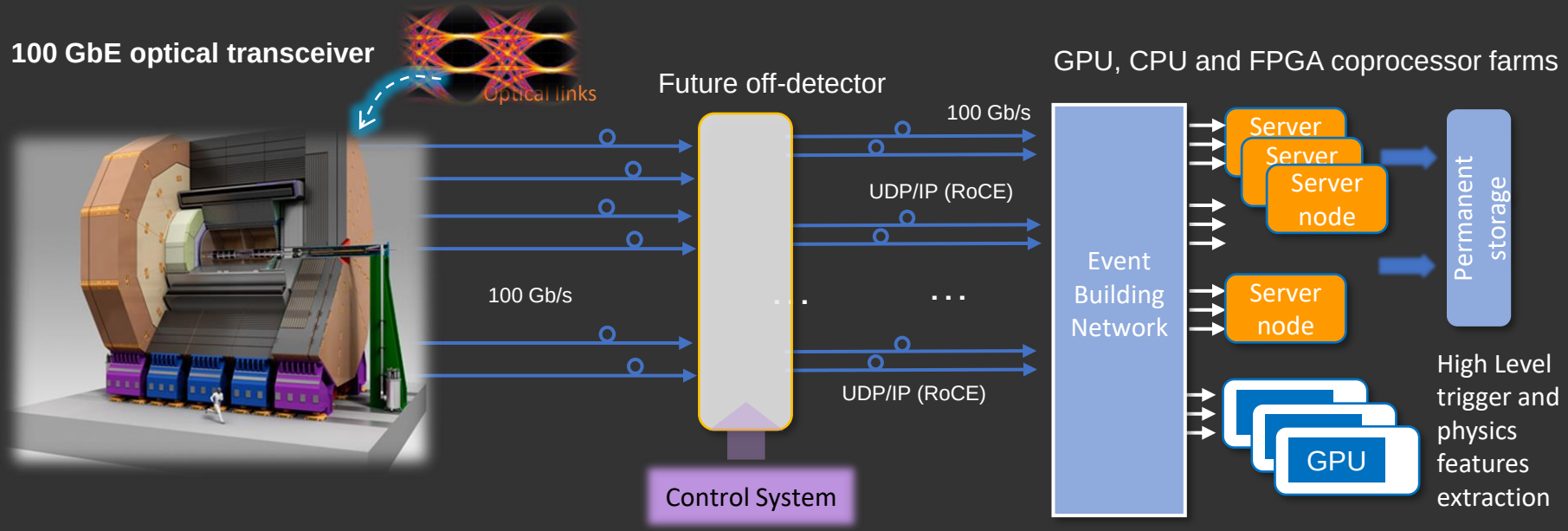
Novel DAQ architecture

Driven by the progress of CMOS technologies



Novel DAQ architecture

Driven by the progress of CMOS technologies

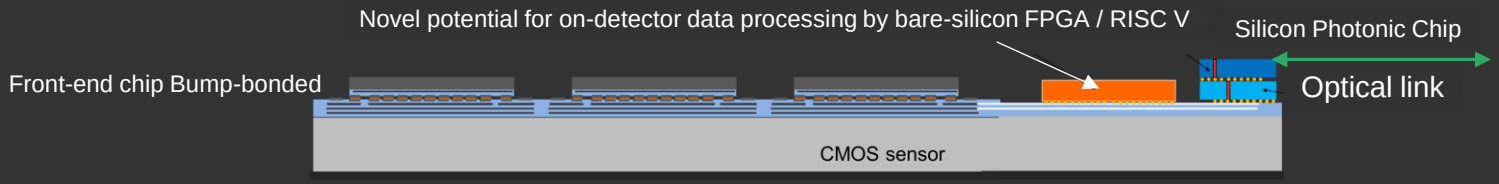


- The new link will drastically ***reshape the design of future***, more efficient, and less experiment-dependent off-detector electronics, paving the way for common DAQ infrastructure
- COTS solutions offer cost-effective, versatile options that can be applied across multiple experiments

Conclusion

Future DAQ systems for in future Terascale experiments

- Current data acquisition systems rely on many standards (ATCA, µTCA, PCIe, ETH, etc.)
- We are developing a versatile common DAQ system capable of supporting a wide range of applications, from large-scale experiments to small standalone systems, with potential use both within and beyond HEP experiments.
- Emerging technologies will play a pivotal role in shaping next generation of DAQ systems
- The direct integration of *Tiny-FPGA* and *Silicon Photonic chips* onto detector modules, using chiplet technology, opens new architectural possibilities for a *fully software-defined DAQ system*



- *Data processing on COTS* devices represents the future of HEP, providing scalable, cost-effective, and versatile solutions to meet the evolving needs of advanced experiments


Thank you for your attention

From custom readout card to COTS

- *Software-defined DAQ* the hardware/infrastructure components are managed by software
- The activities traditionally done by hardware are carried out by software and/or programmable platform (i.e. ARM/FPGA)
  - Enabling the opportunity to reduce the complexity of the HW (readout cards),
  - HW less-dependent on specific experiment / application

- Develop a “common” hardware readout card to streamline system compatibility and integration across experiments
- Minimize development, production, and commissioning efforts and costs within the experimental environment
- Leverage commercial off-the-shelf (COTS) devices to significantly reduce maintenance requirements over the experiment's lifecycle

Future architecture of Data Acquisition Systems for Scientific Applications in the Terascale Era

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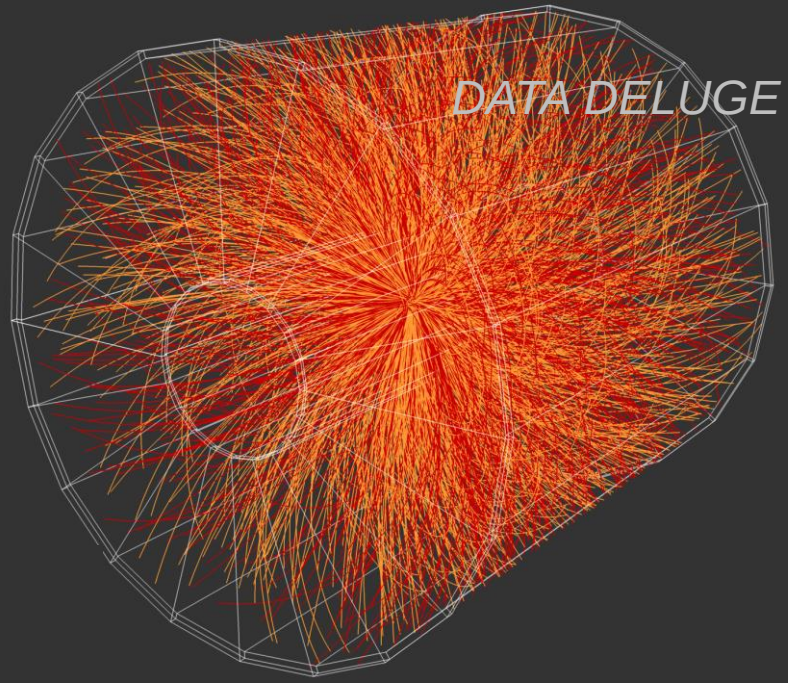
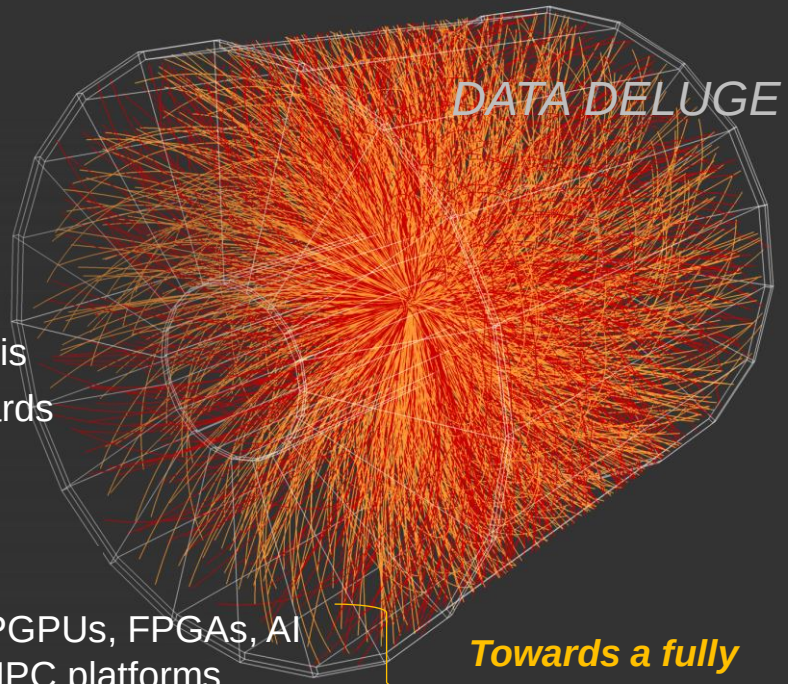
- High-luminosity with collisions close in time and space
  - Fast detector, fast electronics ➡ fast decision
  - Fine granularity ➡ high data volume



Future architecture of Data Acquisition Systems for Scientific Applications in the Terascale Era

Karlsruhe Institute of Technology

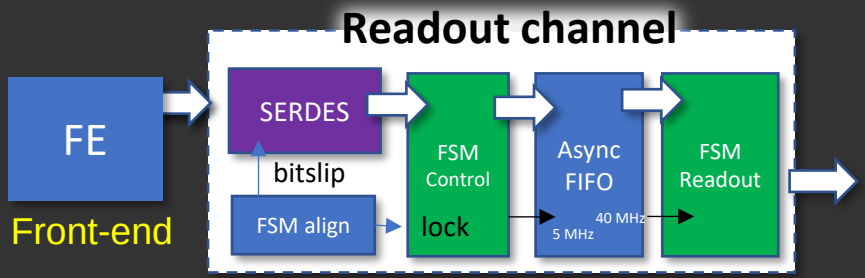
- High-luminosity with collisions close in time and space
  - Fast detector, fast electronics ➡ fast decision
  - Fine granularity ➡ high data volume
- ***New trend***
  - Trigger-less acquisition system with real time analysis
  - Driven by the GPU evolution and HW accelerator cards
- ***Key Highlights:***
  - Fast data transmission
  - COTS (commercial off-the shelf) devices (CPUs, GPGPUs, FPGAs, AI accelerators) to accelerate the data processing on HPC platforms
  - Hardware platform less dependent on specific experiment

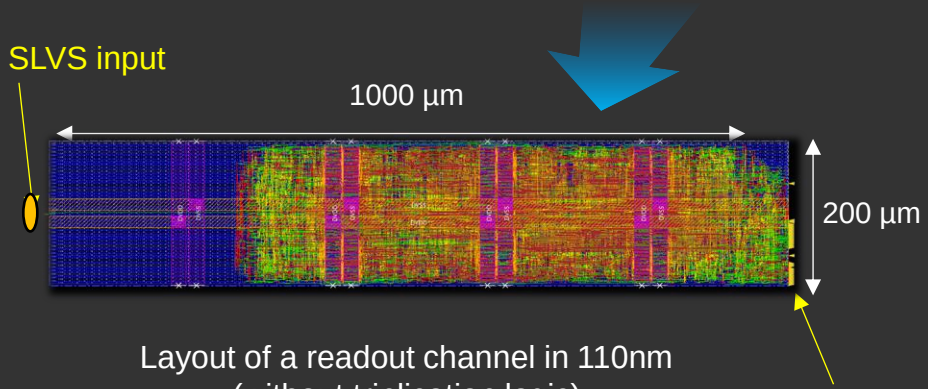


Towards a fully software-defined DAQ system

Readout channel

High efficiency, low-power, small-area logic





Layout of a readout channel in 110nm
(without triplication logic)

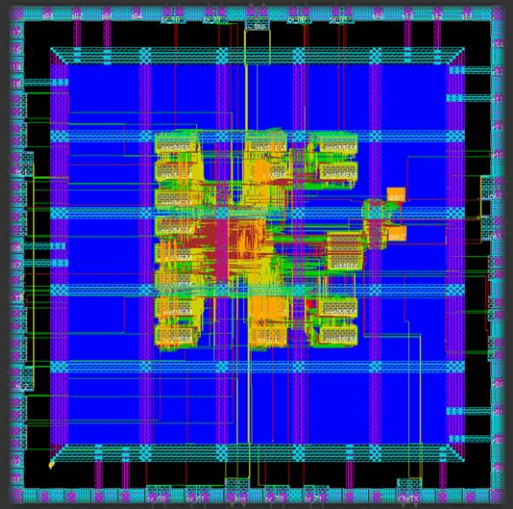
Features:

- Auto-detection/negotiation of active data links, training patter fully programmable
- No-active links are kept in low-power mode
- Data are processed by using of zero-suppression algorithm, empty hits/channels are not transmitted
- Density < 50 %
- Estimated power of 0.8 mW @ 1.2V

Novel DAQ architecture

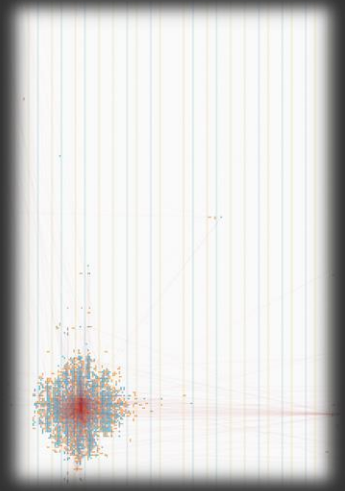
High-performance of Data Concentrator on small-size FPGA

- Comparison between the DC ASIC (110 nm CMOS) and the DC implemented on commercial Efinix Titanium (Ti60) FPGA (bare-silicon size < 5x5 mm^2)

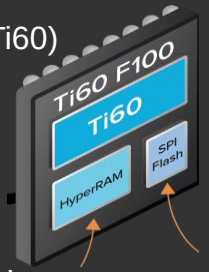


Data Concentrator ASIC

VS



*Data Concentrator FPGA version (**Ti60**)*



- Occupancy < 11 %
- Max clock speed > 500 MHz
- ASiC-like performance
- More flexibility
- More resources (DSP, RAMs ..)
- FinFET 16 nm CMOS ➔ high TID
- Triplication logic possible ➔ high SEU immunity