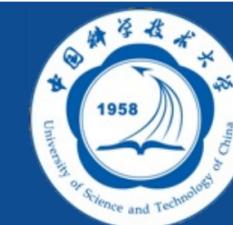




**超级陶粲装置**  
Super Tau-Charm Facility



# STCF Detector Design and R&D

**Jianbei Liu**

**On behalf of the STCF detector group**

**University of Science and Technology of China**

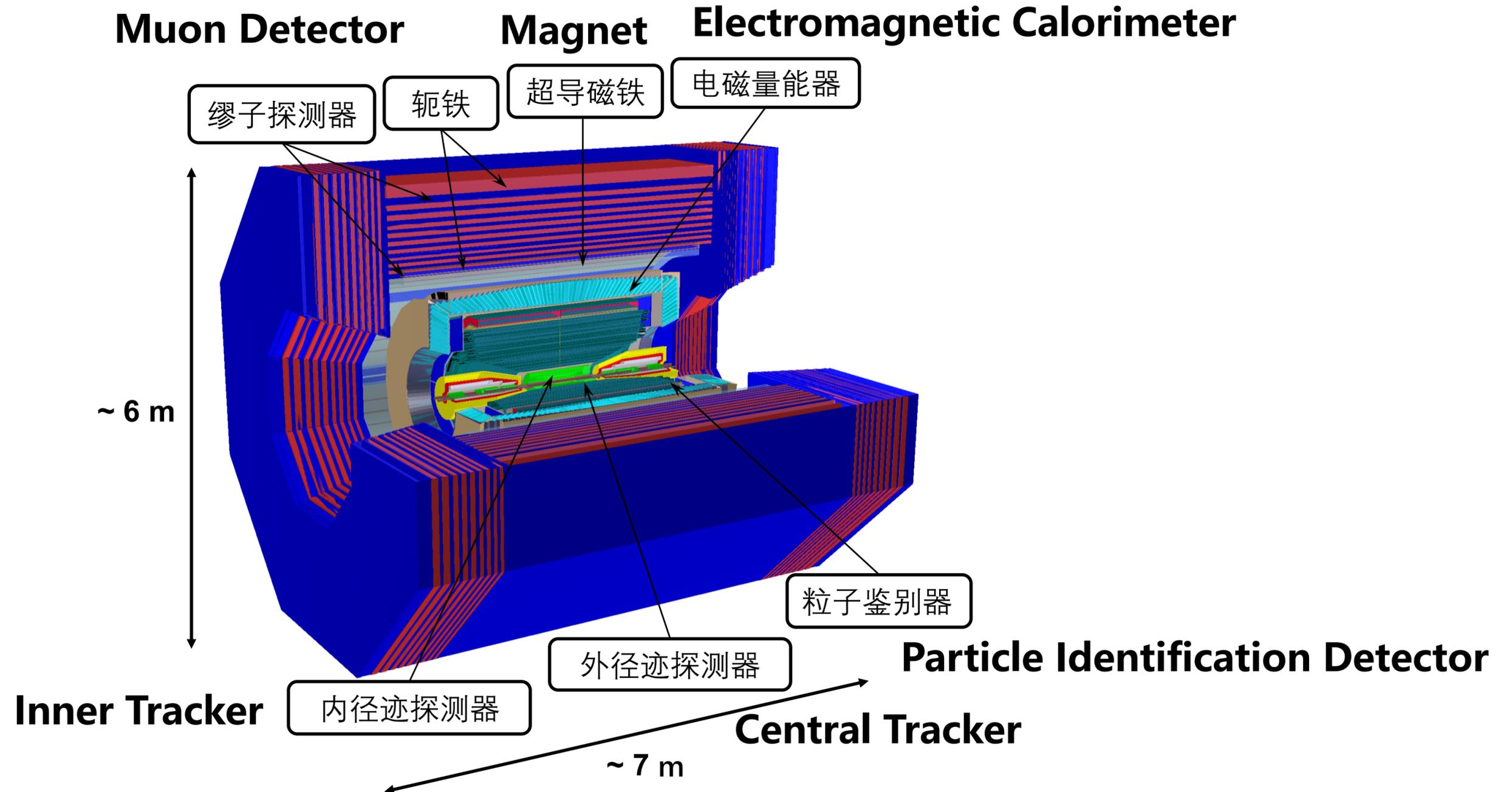
**State Key Laboratory of Particle Detection and Electronics**

**The 6th International Workshop on Future Tau Charm Facilities, 2024**

**SYSU, Guangzhou, China**

**Nov. 18, 2024**

# STCF Detector Layout

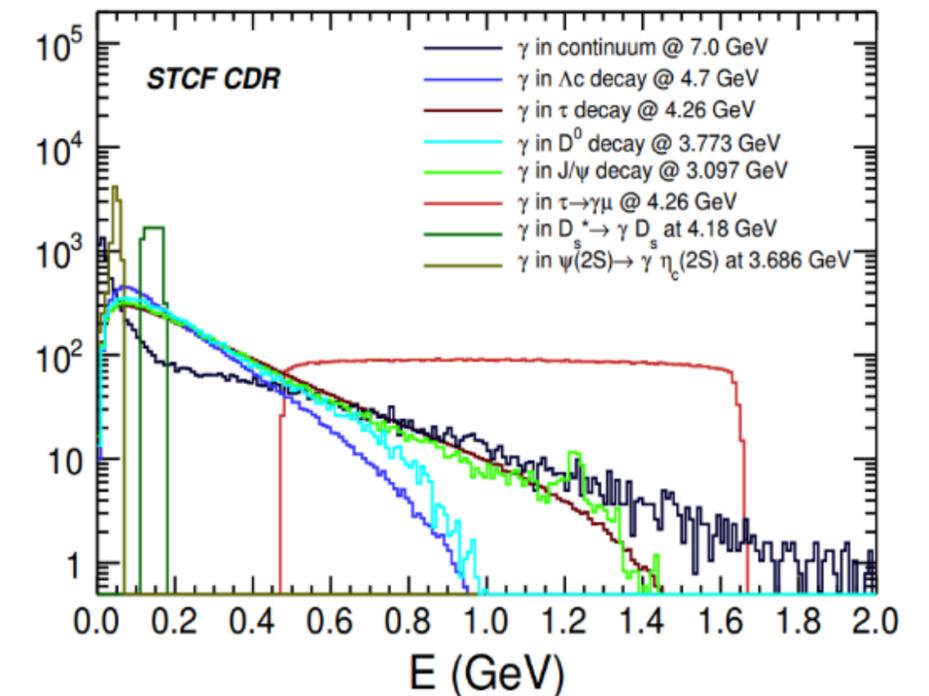
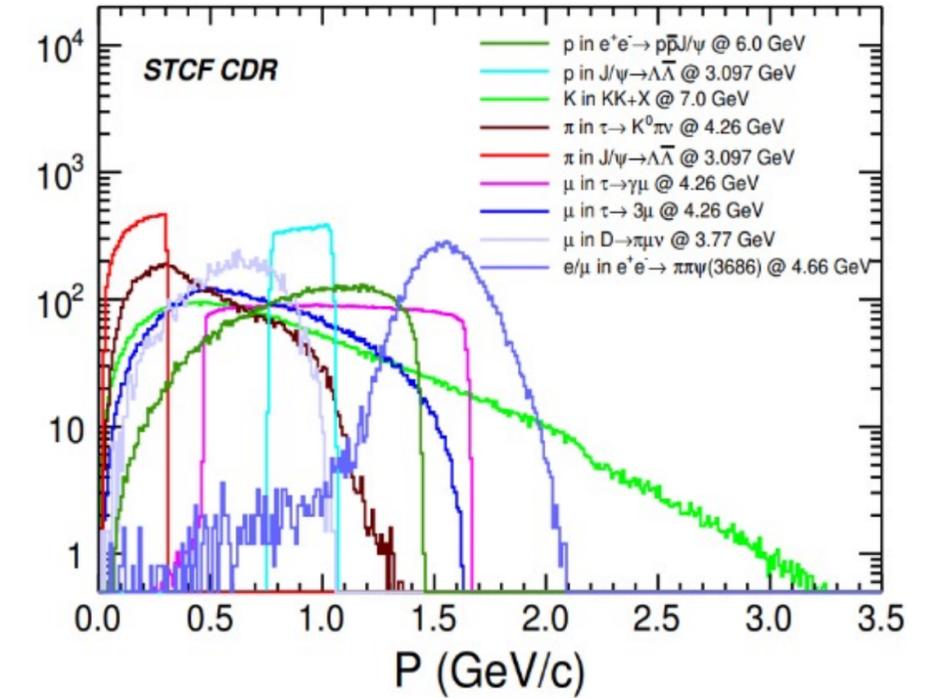


# Physics Requirements

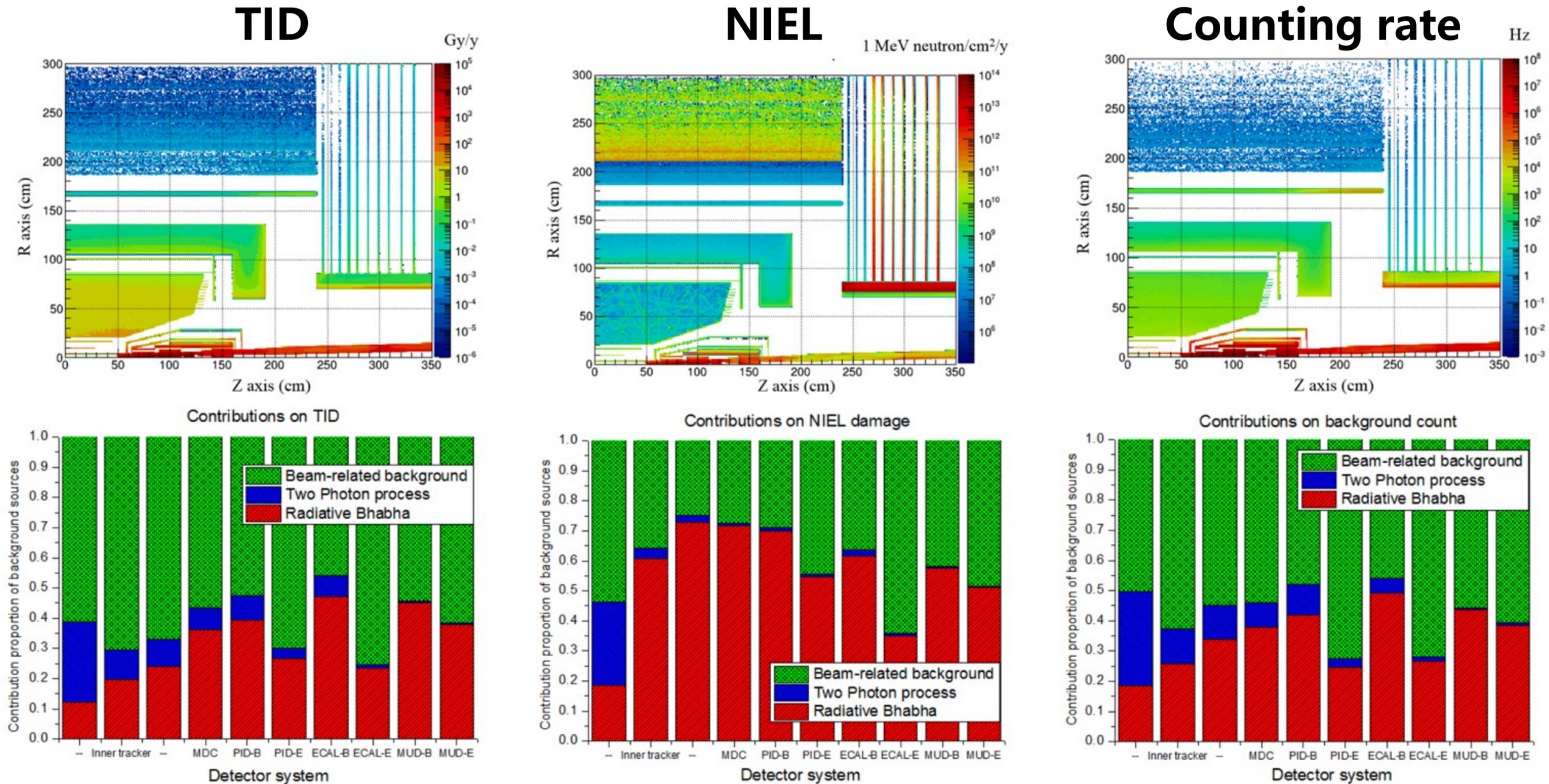
## ❖ Highly efficient and precise reconstruction of exclusive final states produced in 2-7 GeV e+e- collisions

- ▶ Precise measurement of low-p particles (<1 GeV/c) → **low mass**
- ▶ **Excellent PID**:  $\pi/K$  and  $\mu/\pi$  separation up to 2 GeV

Process	Physics Interest	Optimized Subdetector	Requirements
$\tau \rightarrow K_s \pi \nu_\tau$ , $J/\psi \rightarrow \Lambda \bar{\Lambda}$ , $D_{(s)}$ tag	CPV in the $\tau$ sector, CPV in the hyperon sector, Charm physics	ITK+MDC	acceptance: 93% of $4\pi$ ; trk. effi.: > 99% at $p_T > 0.3$ GeV/c; > 90% at $p_T = 0.1$ GeV/c $\sigma_p/p = 0.5\%$ , $\sigma_{\gamma\phi} = 130 \mu\text{m}$ at 1 GeV/c
$e^+e^- \rightarrow KK + X$ , $D_{(s)}$ decays	Fragmentation function, CKM matrix, LQCD etc.	PID	$\pi/K$ and $K/\pi$ misidentification rate < 2% PID efficiency of hadrons > 97% at $p < 2$ GeV/c
$\tau \rightarrow \mu\mu\mu$ , $\tau \rightarrow \gamma\mu$ , $D_s \rightarrow \mu\nu$	cLFV decay of $\tau$ , CKM matrix, LQCD etc.	PID+MUD	$\mu/\pi$ suppression power over 30 at $p < 2$ GeV/c, $\mu$ efficiency over 95% at $p = 1$ GeV/c
$\tau \rightarrow \gamma\mu$ , $\psi(3686) \rightarrow \gamma\eta(2S)$	cLFV decay of $\tau$ , Charmonium transition	EMC	$\sigma_E/E \approx 2.5\%$ at $E = 1$ GeV $\sigma_{\text{pos}} \approx 5$ mm at $E = 1$ GeV
$e^+e^- \rightarrow n\bar{n}$ , $D_0 \rightarrow K_L \pi^+ \pi^-$	Nucleon structure Unity of CKM triangle	EMC+MUD	$\sigma_T = \frac{300}{\sqrt{p^3(\text{GeV}^3)}} \text{ ps}$



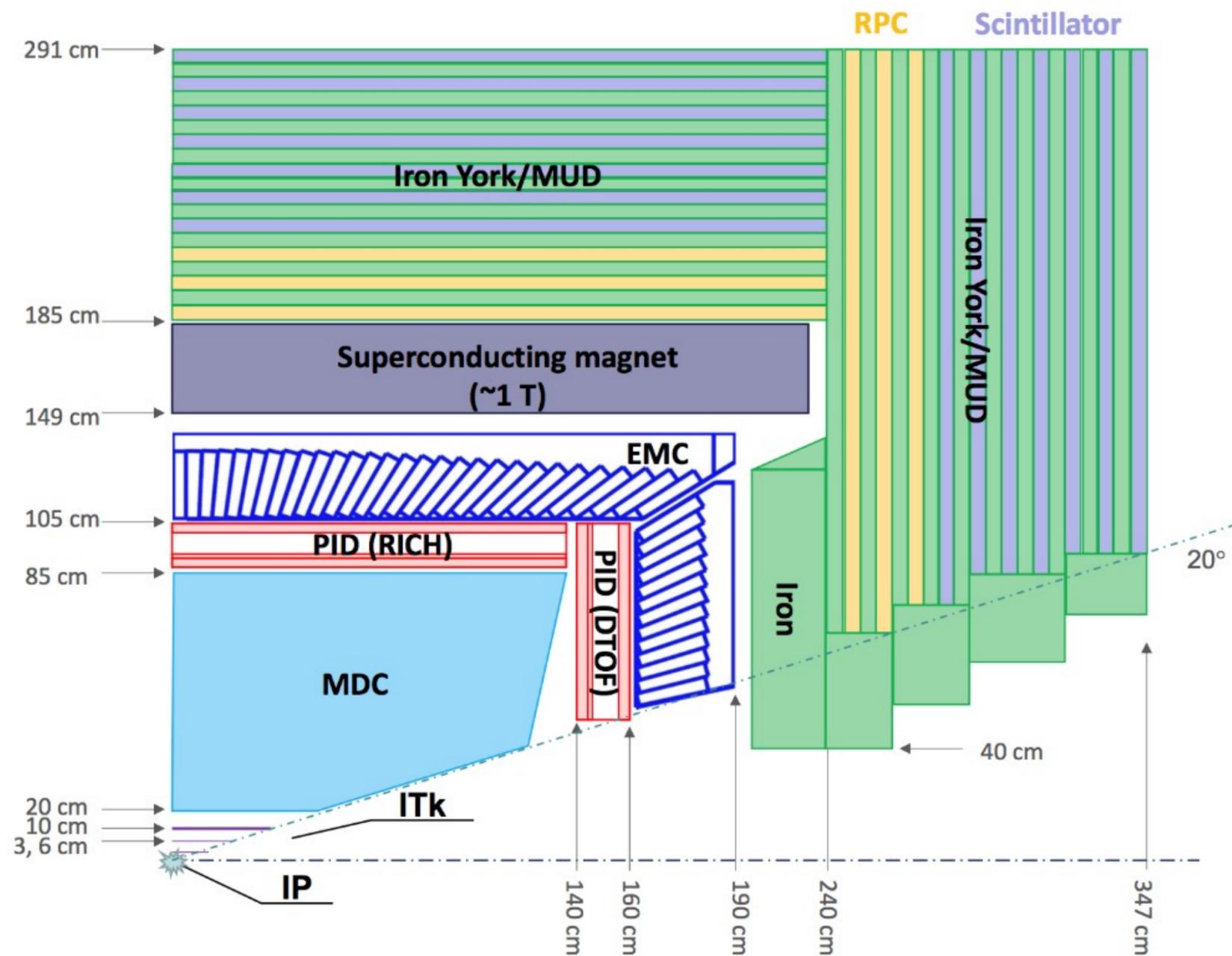
# Beam-induced Backgrounds



**Inner most detector layer:**  $\sim 3.5$  kGy/y,  $\sim 2 \times 10^{11}$  1MeV n-eq/cm<sup>2</sup>/y,  $\sim 1$  MHz/cm<sup>2</sup>

The major challenge is to maintain or even enhance the state of the art performance of  $\tau$ -c detectors in much harsher experimental conditions.

# STCF Detector Conceptual Design



**Solid Angle Coverage :  $94\% \cdot 4\pi$  ( $\theta \sim 20^\circ$ )**

- ❖ **Inner tracker (ITK, two options)**
  - ▶ MPGD: cylindrical MPGD
  - ▶ Silicon: CMOS MAPS
- ❖ **Central tracker (MDC)**
  - ▶ Main drift chamber
- ❖ **PID**
  - ▶ Barrel: **RICH** with CsI-MPGD
  - ▶ Endcaps: DIRC-like TOF (**DTOF**)
- ❖ **EMC**
  - ▶ pure CsI + APD
- ❖ **Muon detector (MUD)**
  - ▶ RPC + scintillator strips
- ❖ **Magnet**
  - ▶ Super-conducting solenoid, 1 T

# STCF Physics & Detector CDR

## Frontiers of Physics

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FRONTIERS OF PHYSICS

REPORT  
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### STCF conceptual design report (Volume 1): Physics & detector

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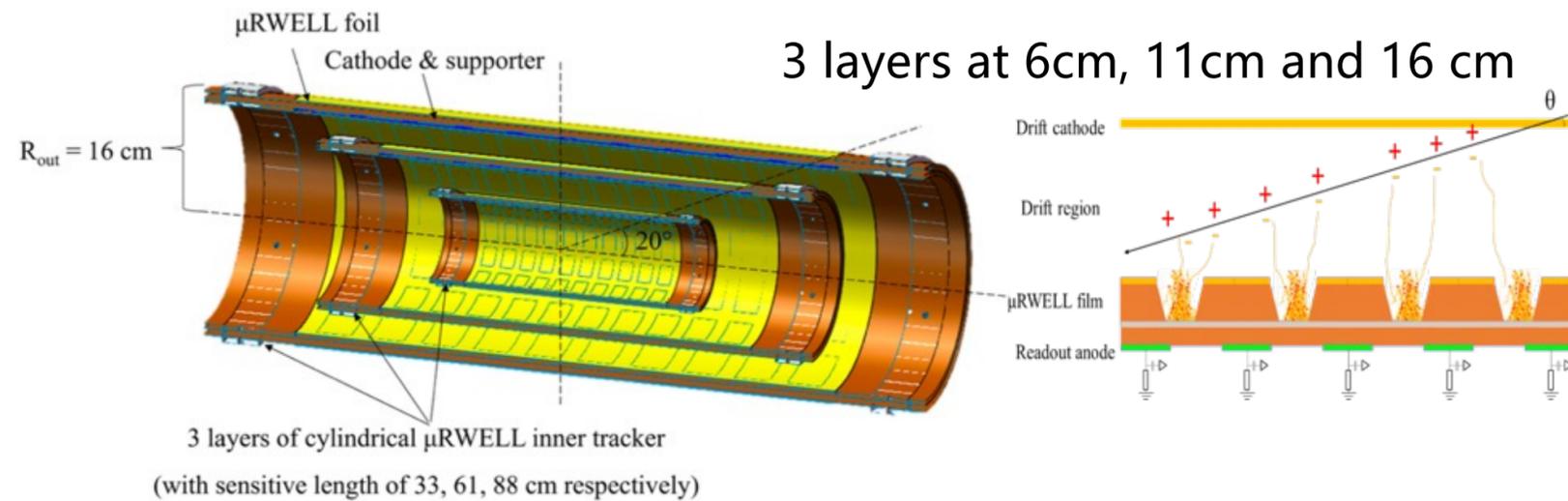
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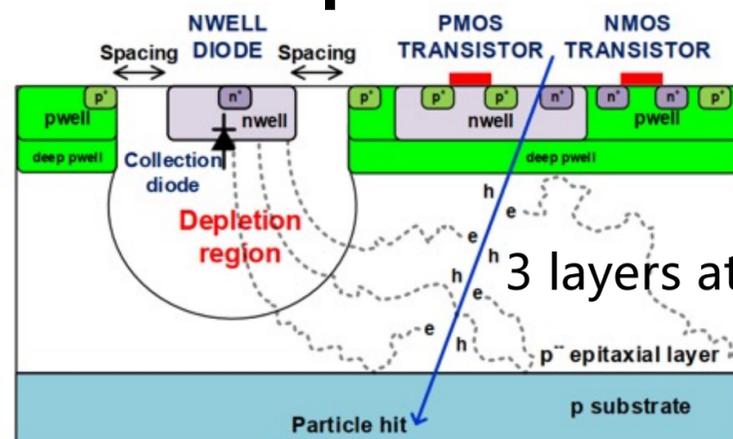
# Tracking System : ITK + MDC

## ITK Gaseous option : MPGD

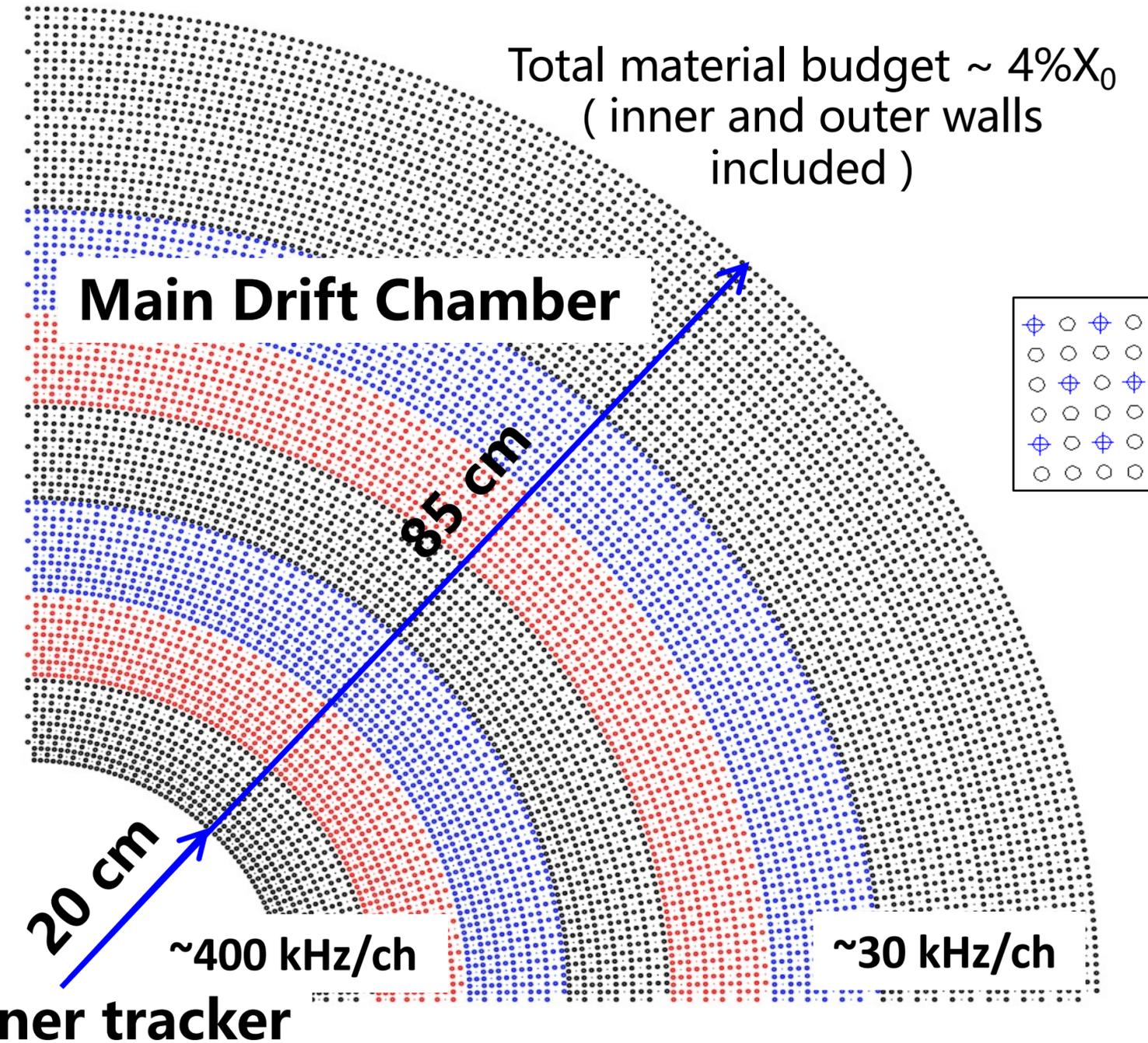


Material budget  $\sim 0.3\%X_0/\text{layer}$

## ITK Silicon option: CMOS MAPS



单片有源像素探测器

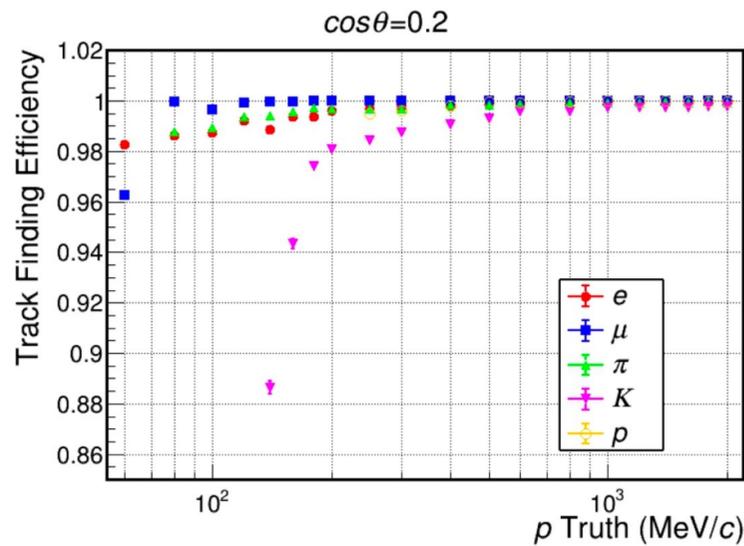


Inner-outer separate designs to accommodate different levels of radiation background

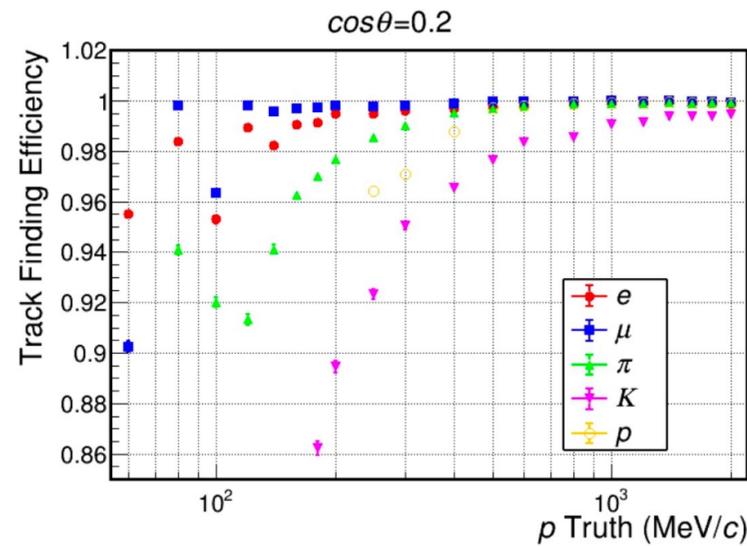
# Tracking Performance with Full Simulation

## Tracking performance for single particles

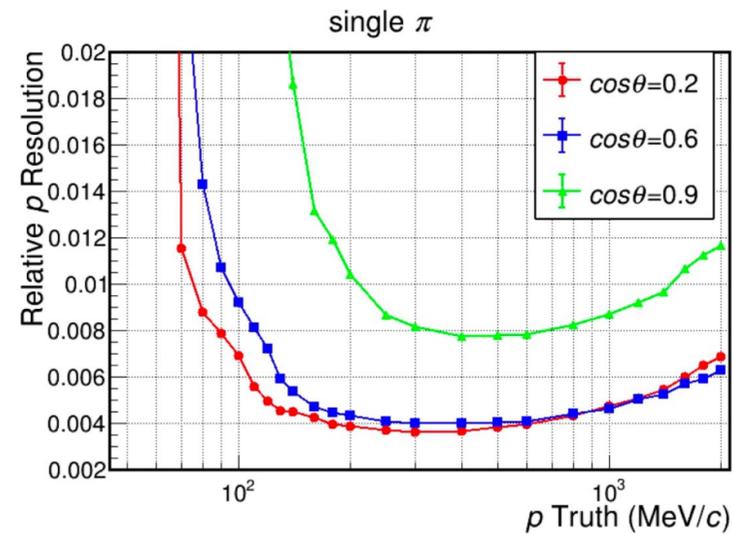
Tracking efficiency without background



Tracking efficiency with background



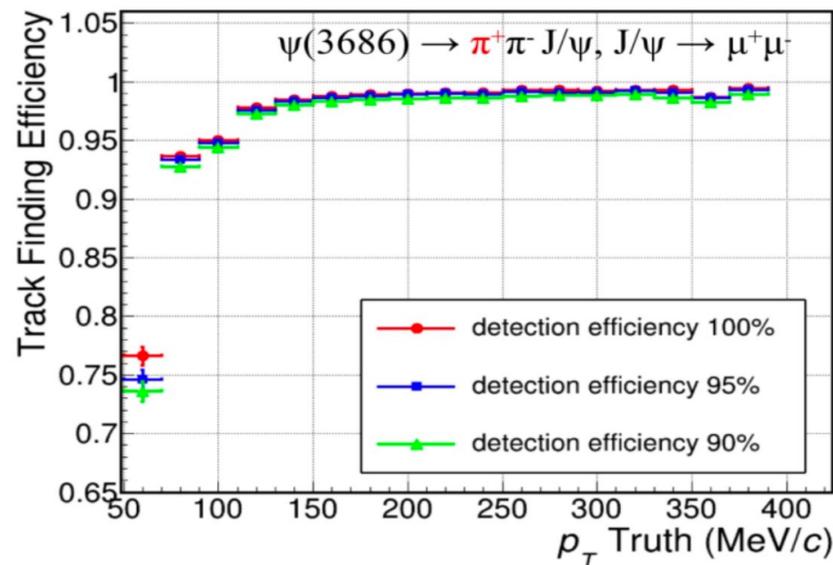
Momentum Resolution



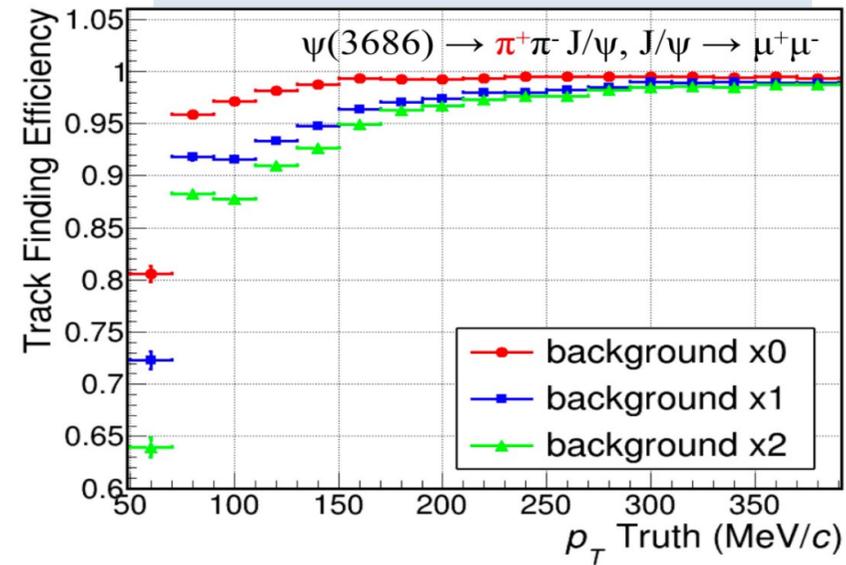
- High tracking efficiency achieved even in presence of beam background
- Momentum resolution meets the physics requirement and is much less impacted by beam background compared to tracking efficiency.

## Tracking performance in physics events

Tracking efficiency with different hit efficiencies



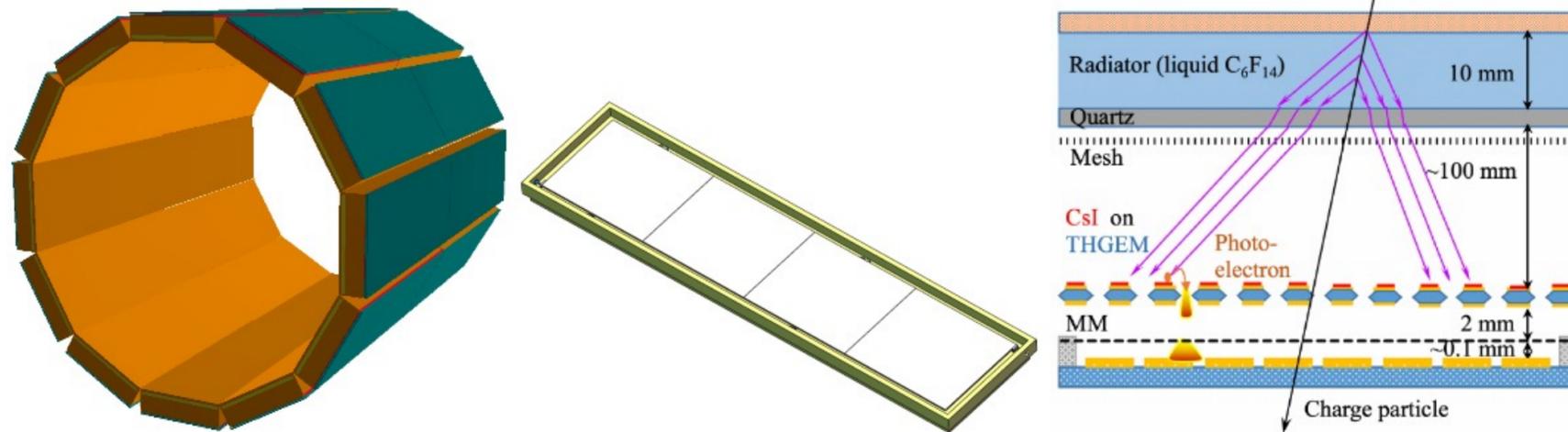
Tracking efficiency with different levels of background



- The lower tracking efficiency in physics events is due to the kinematic distribution of the particle concerned in the events. For example, the pion+ in the events gets much more forward when its momentum goes down.
- The tracking efficiency is robust against beam background and low hit efficiency degradation.

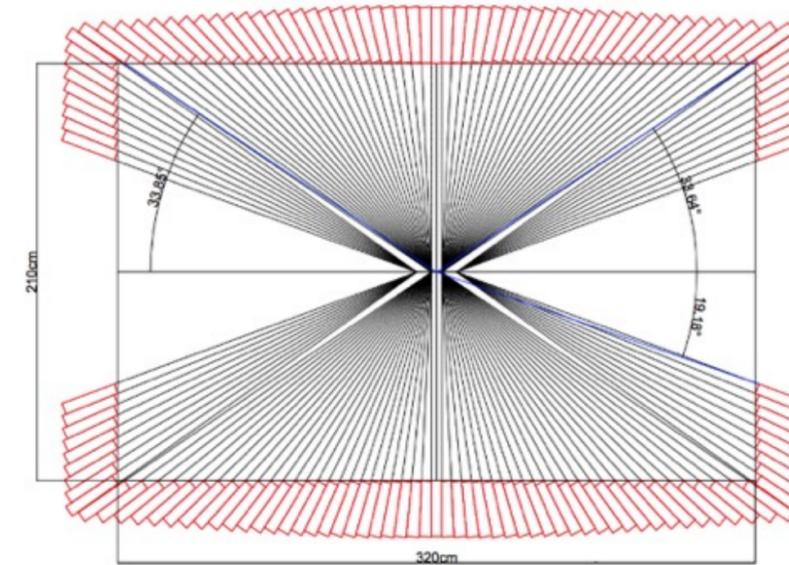
# PID, EMC, MUD

- Barrel PID: A RICH detector using MPGD ( THGEM with CsI + MM ) for photon detection



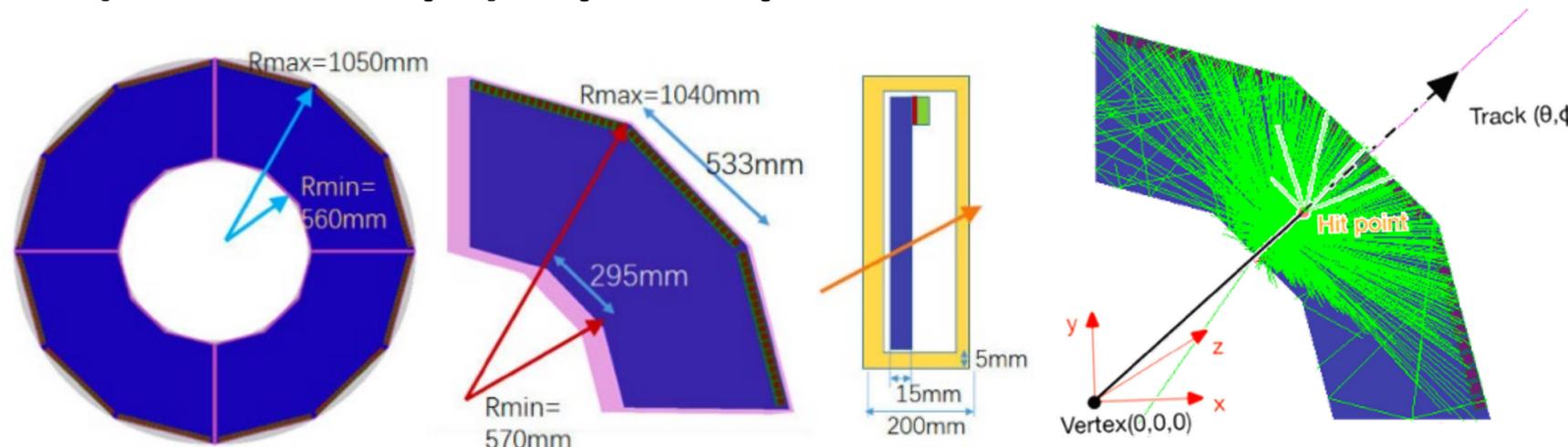
Material budget  $< 0.3X_0$

- EMC: A pure-CsI crystal calorimeter to tackle a high level of background ( $\sim 1\text{MHz}/\text{ch}$ )

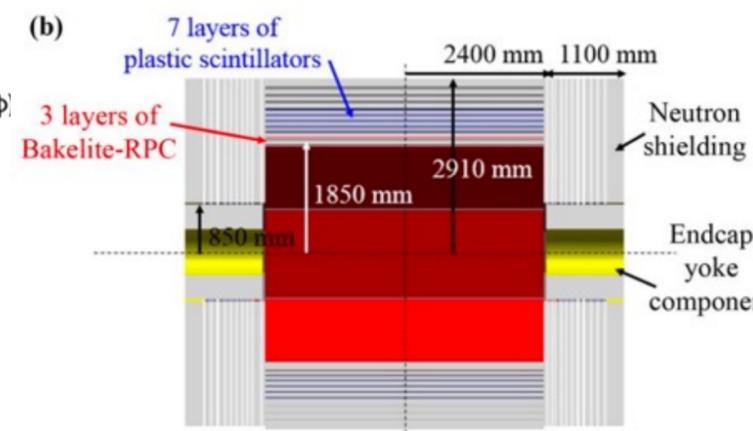


- Crystal size 28cm (15X0)  $5 \times 5\text{cm}^2$
- $\sim 8670$  crystals
- 4 large area APDs ( $1 \times 1\text{cm}^2$ ) to enhance light yield

- Endcap PID: A DIRC-like high-resolution TOF detector ( DTOF  $\sim 30\text{ps}$ ), quartz plate + MCP-maPMT



- MUD: A RPC-scintillator hybrid detector to optimize muon and neutral hadron ID

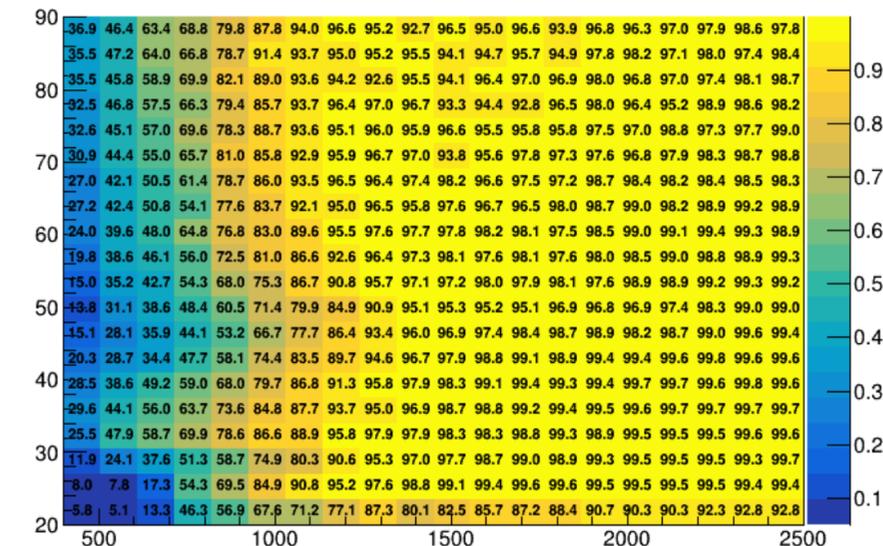
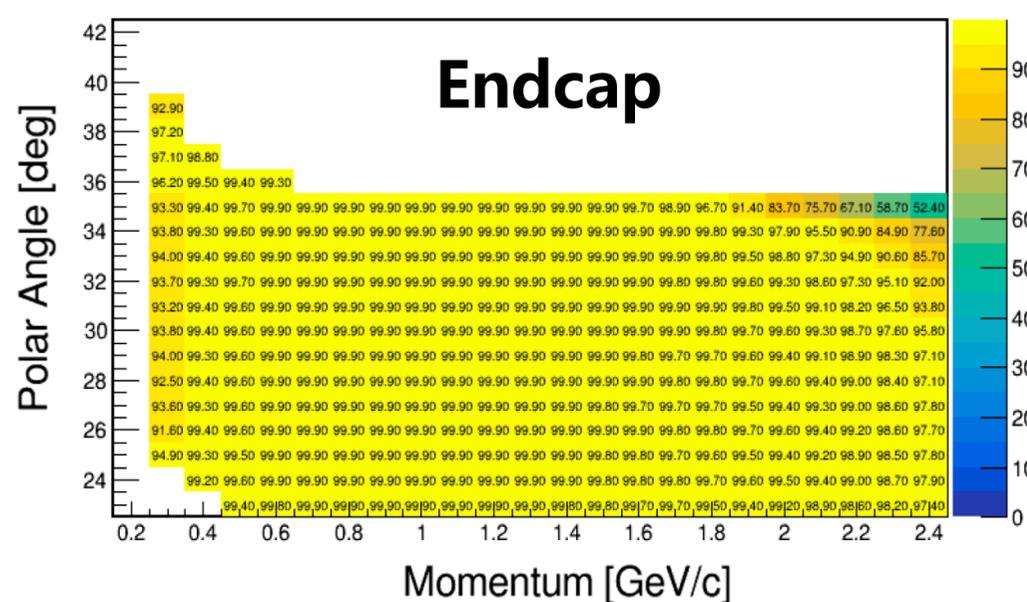
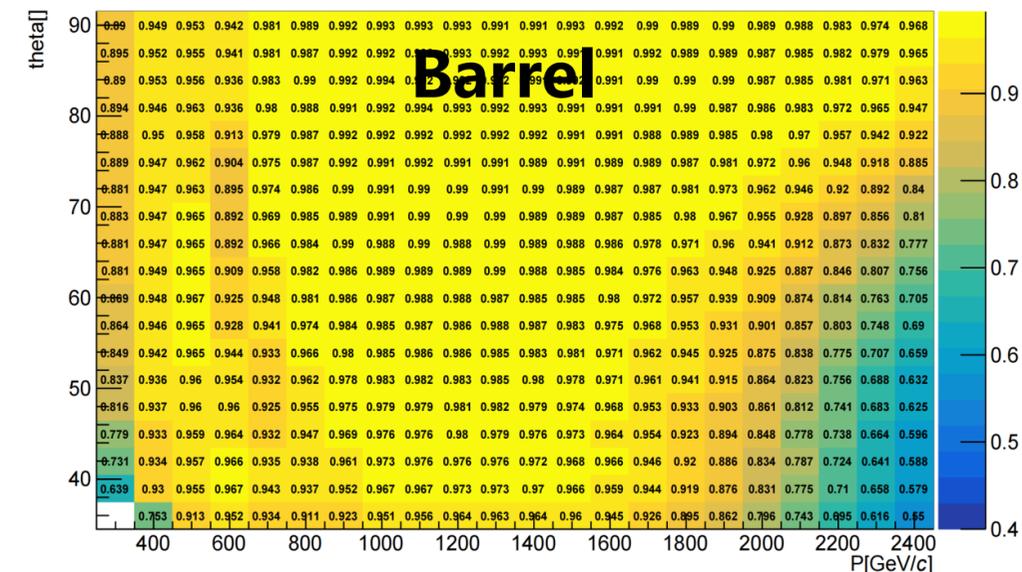


Parameter	Baseline design
$R_{in}$ [cm]	185
$R_{out}$ [cm]	291
$R_e$ [cm]	85
$L_{Barrel}$ [cm]	480
$T_{Endcap}$ [cm]	107
Segmentation in $\phi$	8
Number of detector layers	10
Iron yoke thickness [cm] ( $\lambda=16.77$ )	4/4/4.5/4.5/6/6/6/8/8 cm
Solid angle	Total: $51\text{ cm}, 3.04\lambda$ $79.2\% \times 4\pi$ in barrel $14.8\% \times 4\pi$ in endcap $94\% \times 4\pi$ in total
Total area [ $\text{m}^2$ ]	Barrel $\sim 717$ Endcap $\sim 520$ Total $\sim 1237$

# Performance with Full Simulation (and beam background)

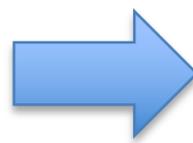
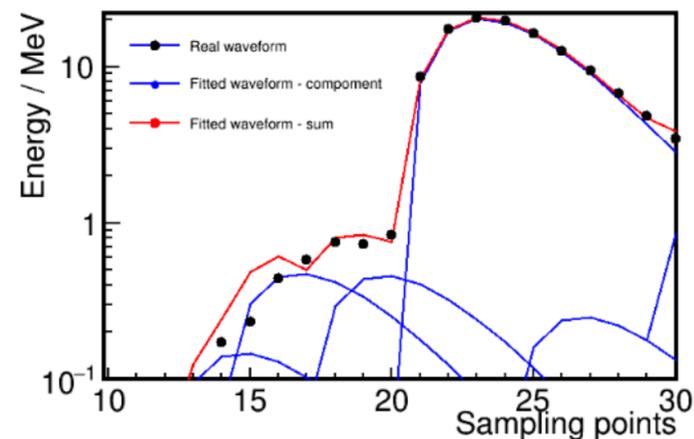
PID: Pion ID eff.  $>97\%$  @ mis-ID ( $K \rightarrow \pi$ ) =  $2\%$

Muon ID eff. @  $\pi$  suppression =  $30$

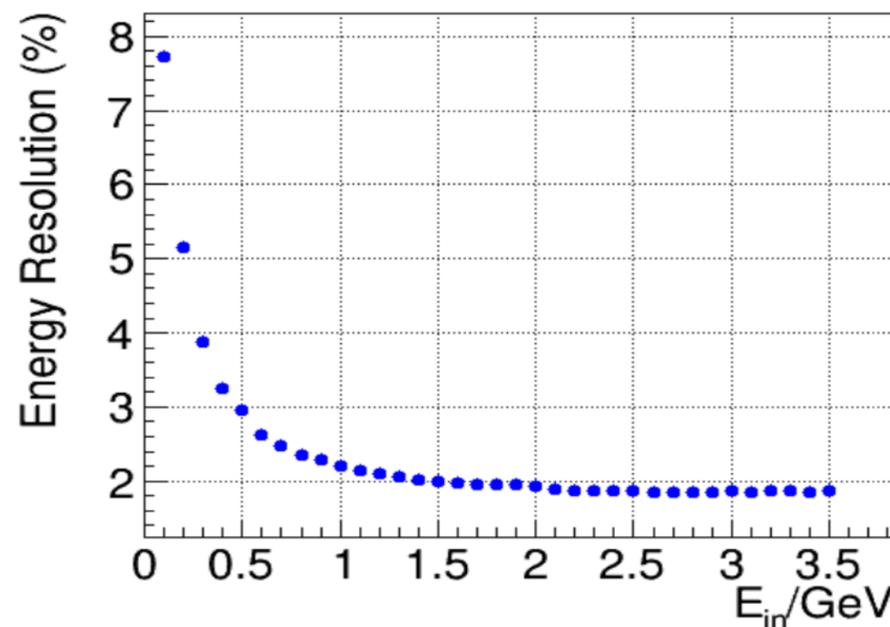


eff.  $\sim > 90\%$  when  $p \sim > 1 \text{ GeV/c}$

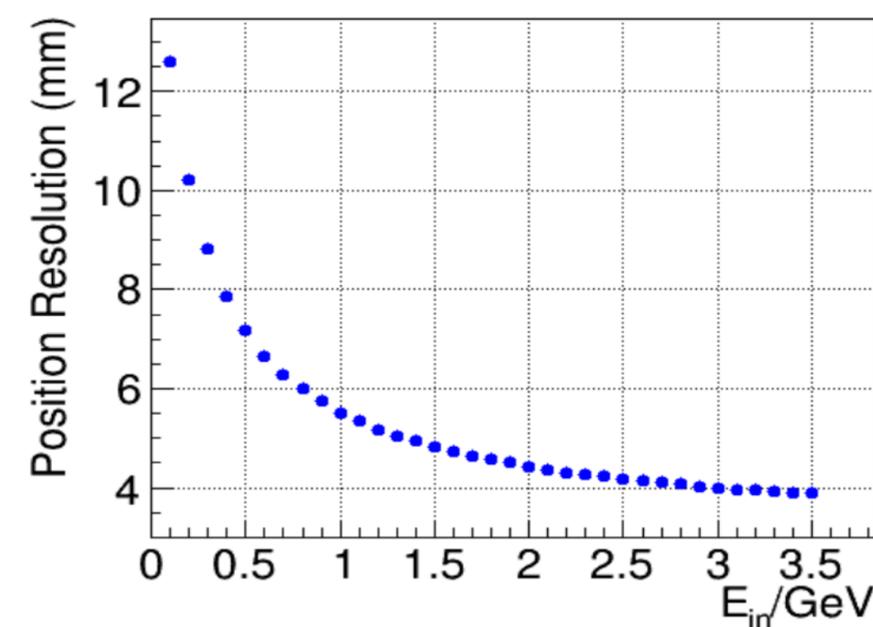
EMC pileup removal with waveform fitting



EMC energy resolution

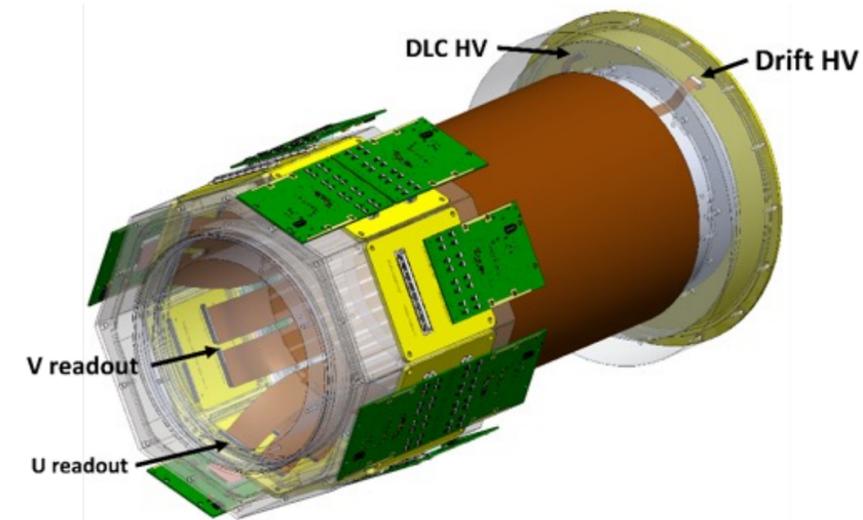
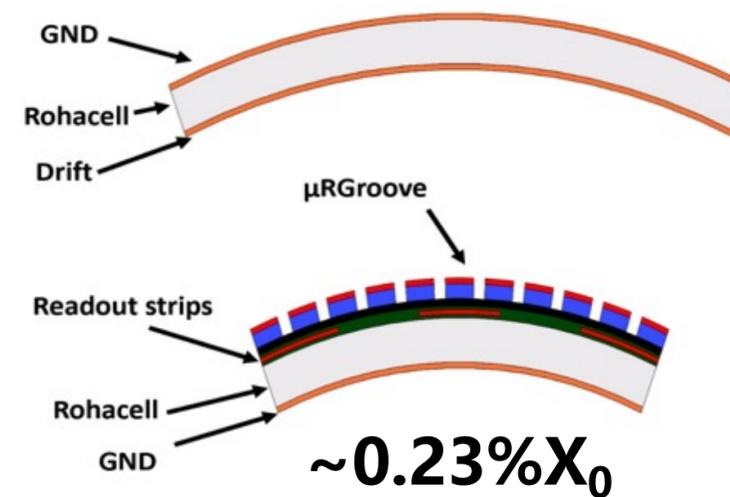
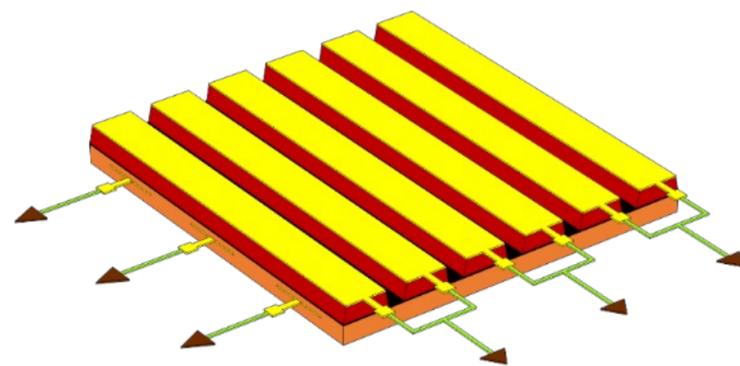
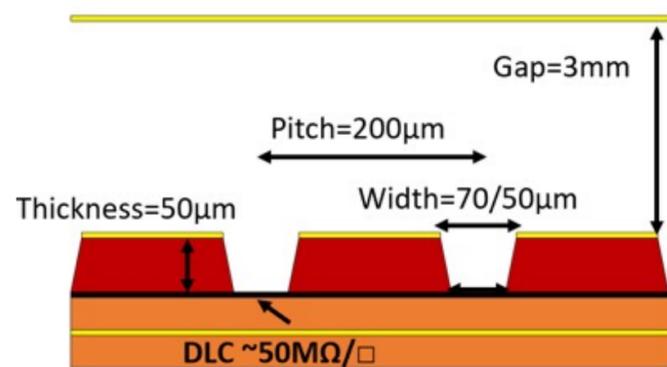


EMC position resolution

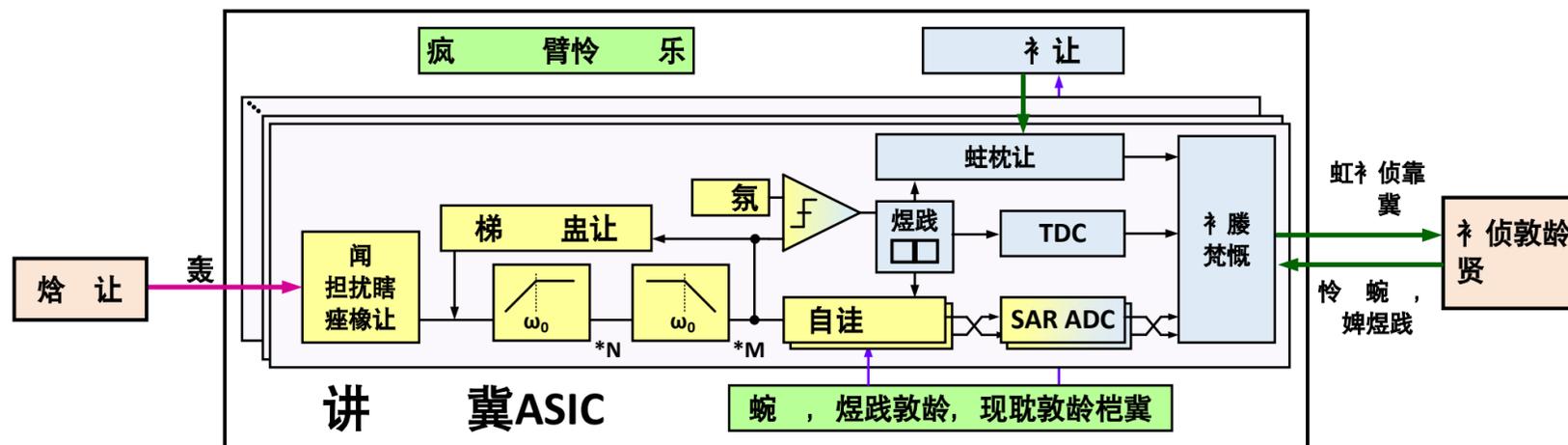


# ITK-MPGD: $\mu$ RGroove

- $\mu$ RGroove : A single-stage MPGD involving no stretching or tensioning, 2D strip readout without charge sharing (large S/N), high rate with fast grounding, easy to make a cylinder, low mass, low production cost



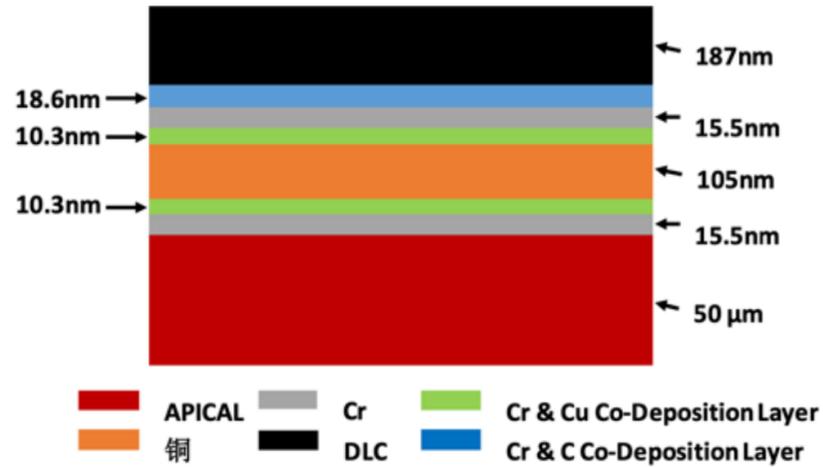
- High-rate readout ASIC for MPGD ( averaged hit rate of 400 kHz/ch)



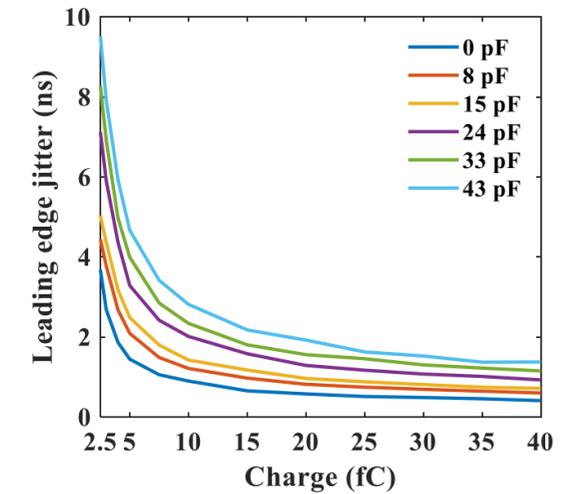
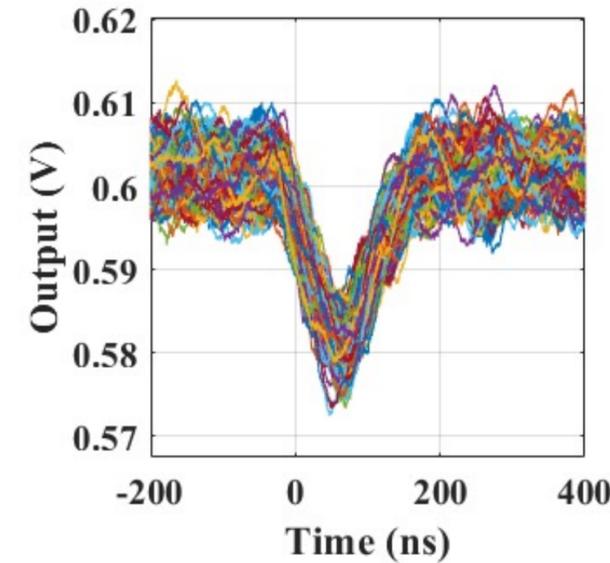
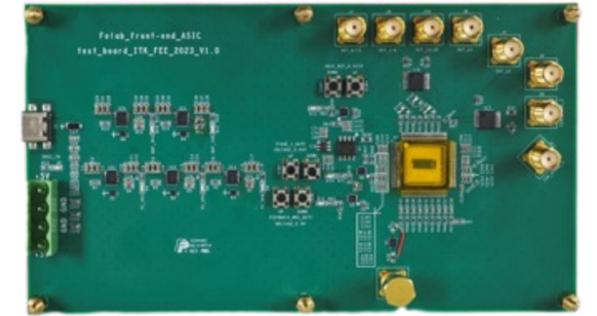
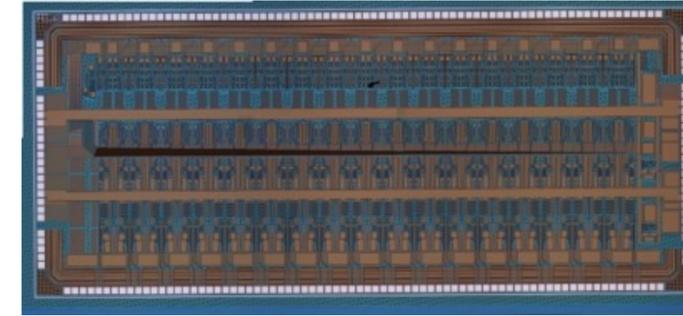
ASIC Specs	Demands
Charge Range	40 fC
Charge precision	$\sim 1$ fC RMS
Time precision	$< 10$ ns RMS
Max. event rate	4 MHz

# ITK-MPGD R&D

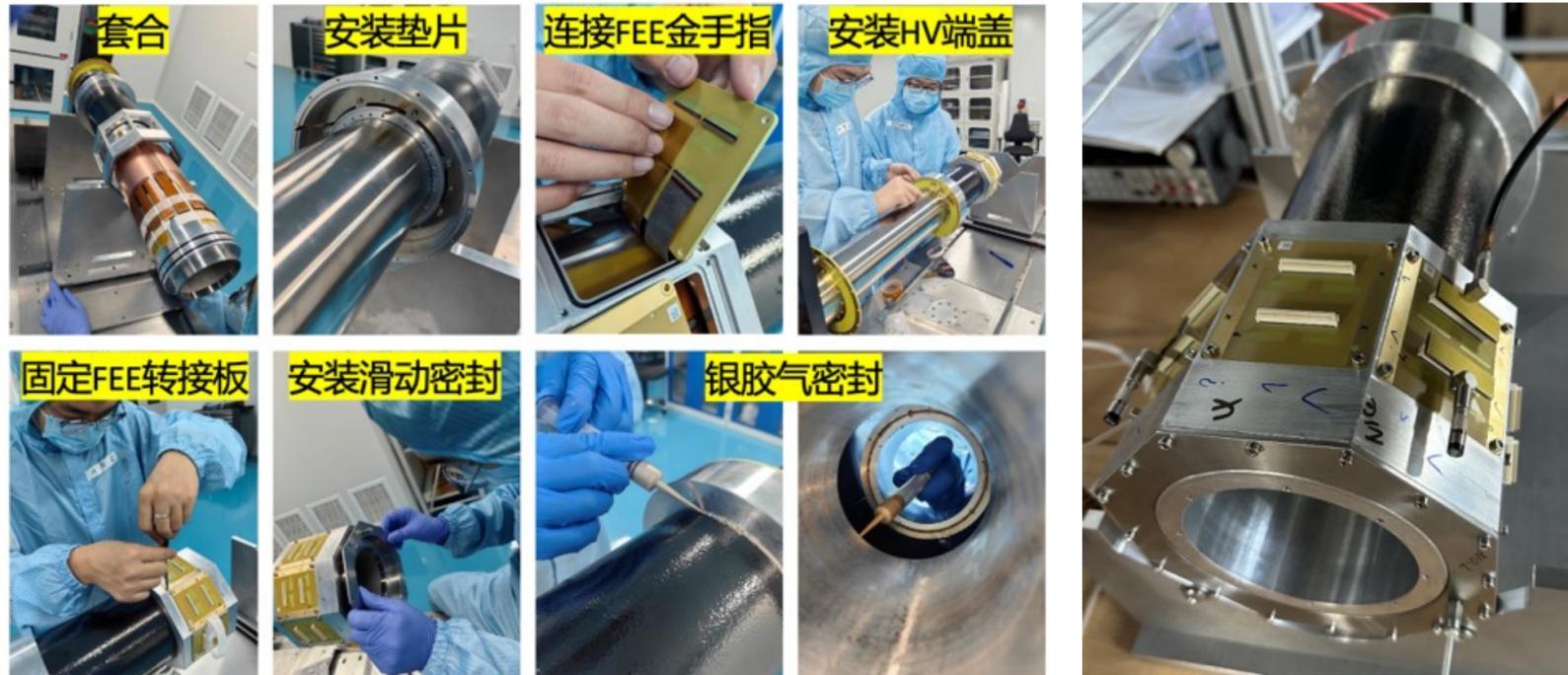
## Development of low mass electrodes



## ASIC design and development



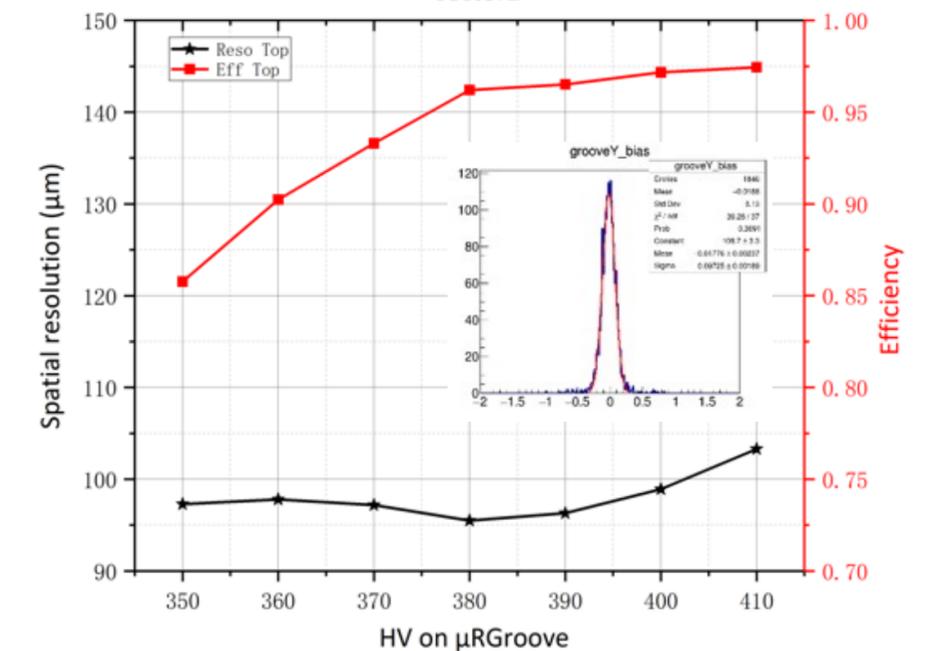
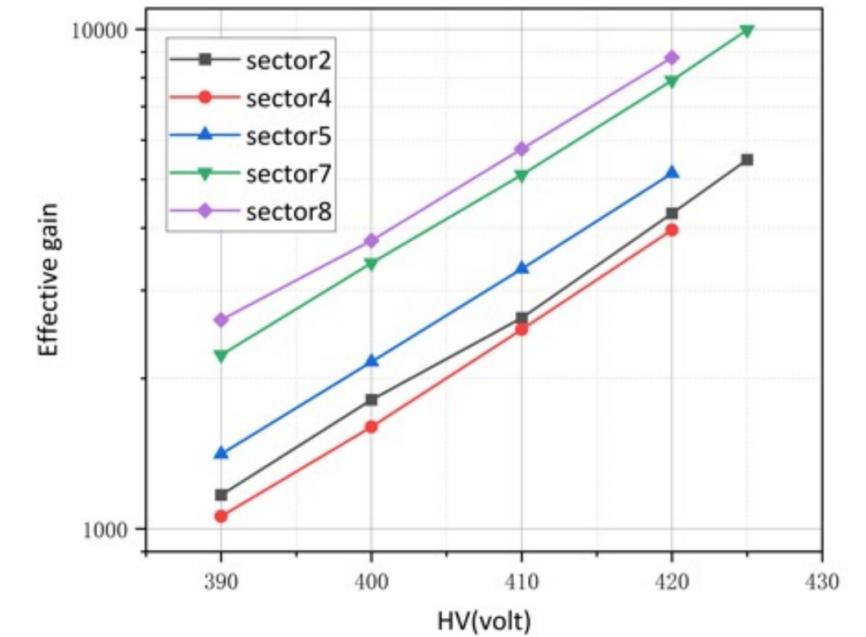
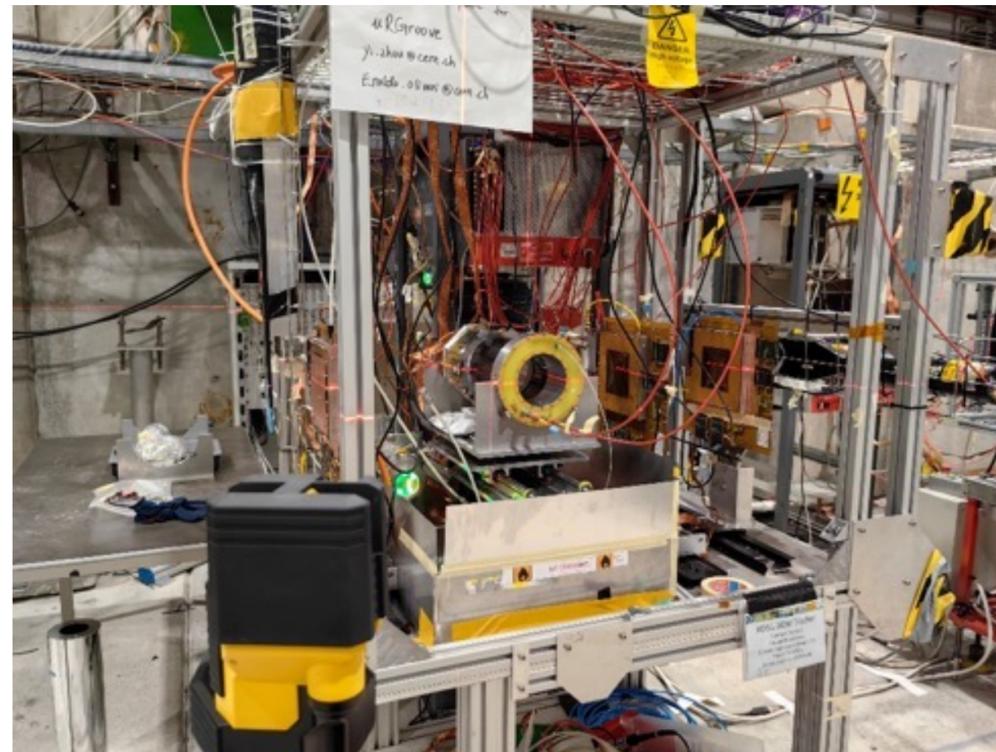
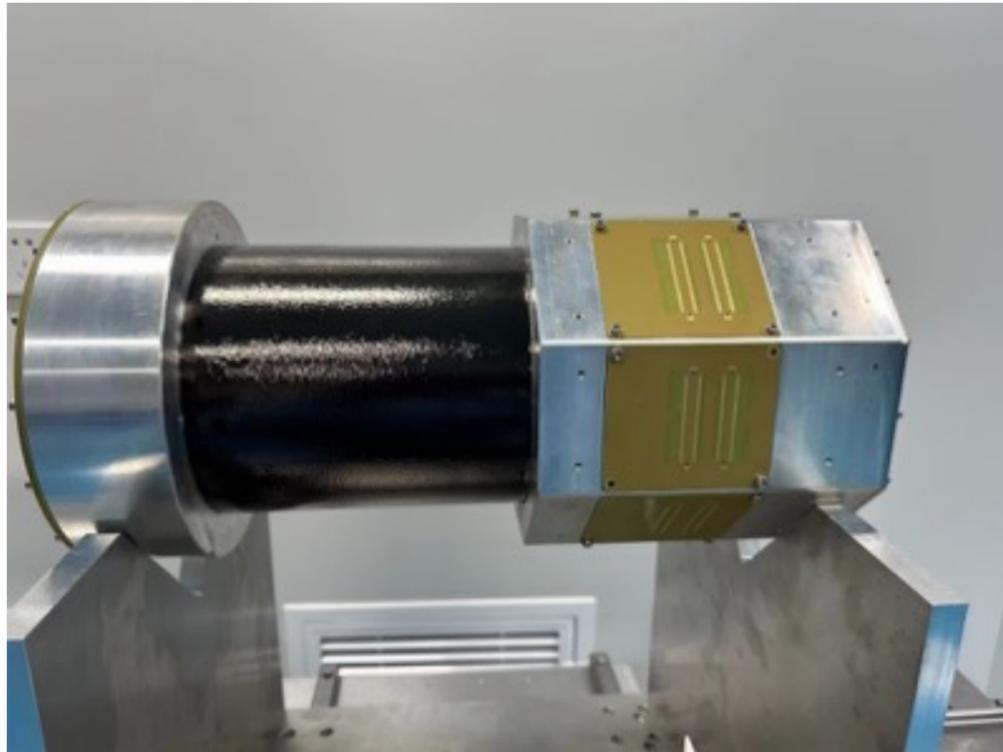
## Fabricating cylindrical structure



Tested the ASIC chip by feeding simulated detector output pulses to the chip at 4MHz with 35pF

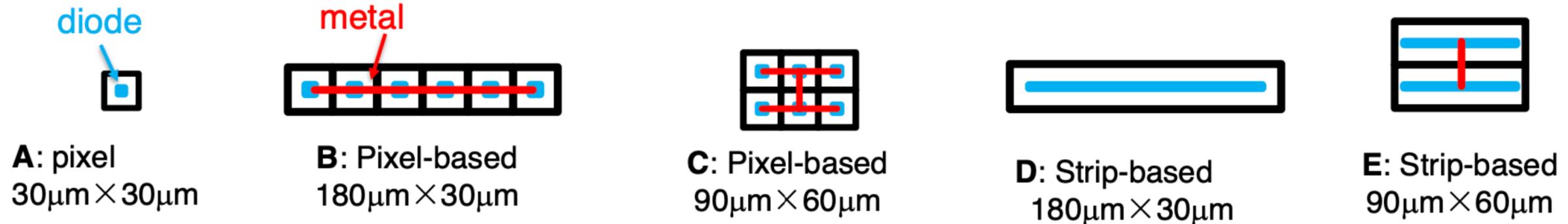
# Inner Layer Prototype

- Built a cylindrical  $\mu$ RGroove prototype for the ITK inner most layer
- Tested the prototype with  $^{55}\text{Fe}$  source in lab and SPS muon beam at CERN
- Effective gain  $\sim 5000$ - $10000$  for most sectors
- Spatial resolution  $< 100$   $\mu\text{m}$  and efficiency  $> 95\%$
- The detector design and fabrication will be optimized in many aspects based on the prototyping experience

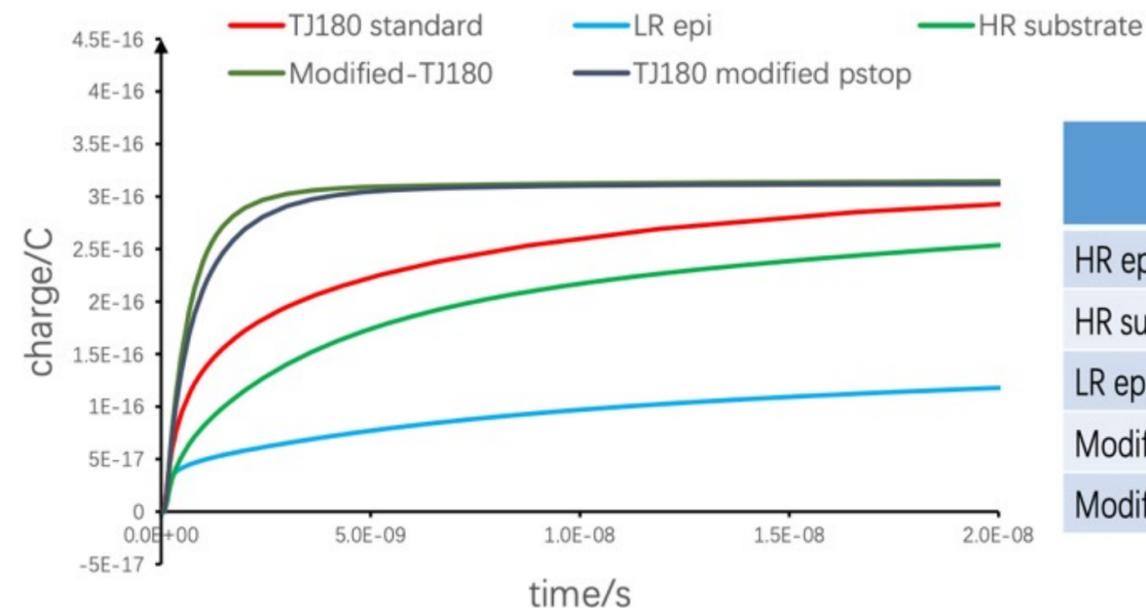


# ITK-MAPS

- Aiming for a low-power MAPS chip design (required for a low-mass system) with timing and charge measurement capability: position, time and charge (TOT)
- Low mass outweighs position resolution: exploring large pixel size to reduce power density



- CMOS techniques being explored:
  - TowerJazz 180nm (HR epi),
  - NexChip FCIS/BCIS 90nm (LR epi )
  - GSMC 130nm (HR substrate)

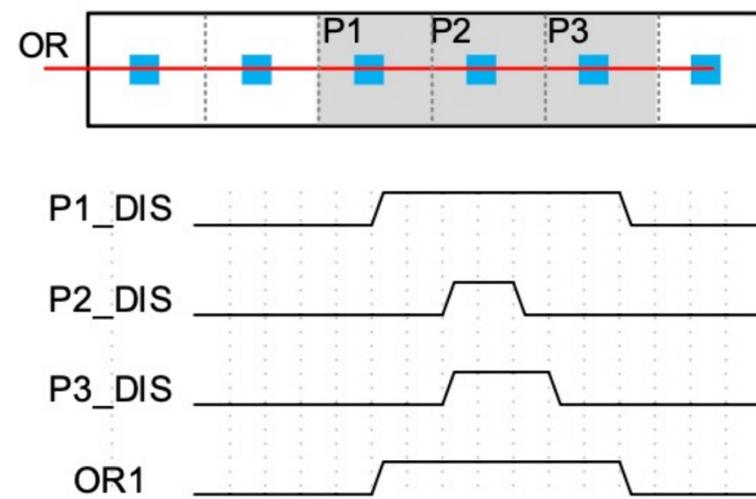


	Collected charge (e)	Collection time(ns)
HR epi (TJ180nm)	2039.81	20.56
HR substrate	2477.65	89.72
LR epi	1089.64	74.57
Modified-TJ180nm	1969.85	1.81
Modified-TJ180nm pstop	1952.04	2.47

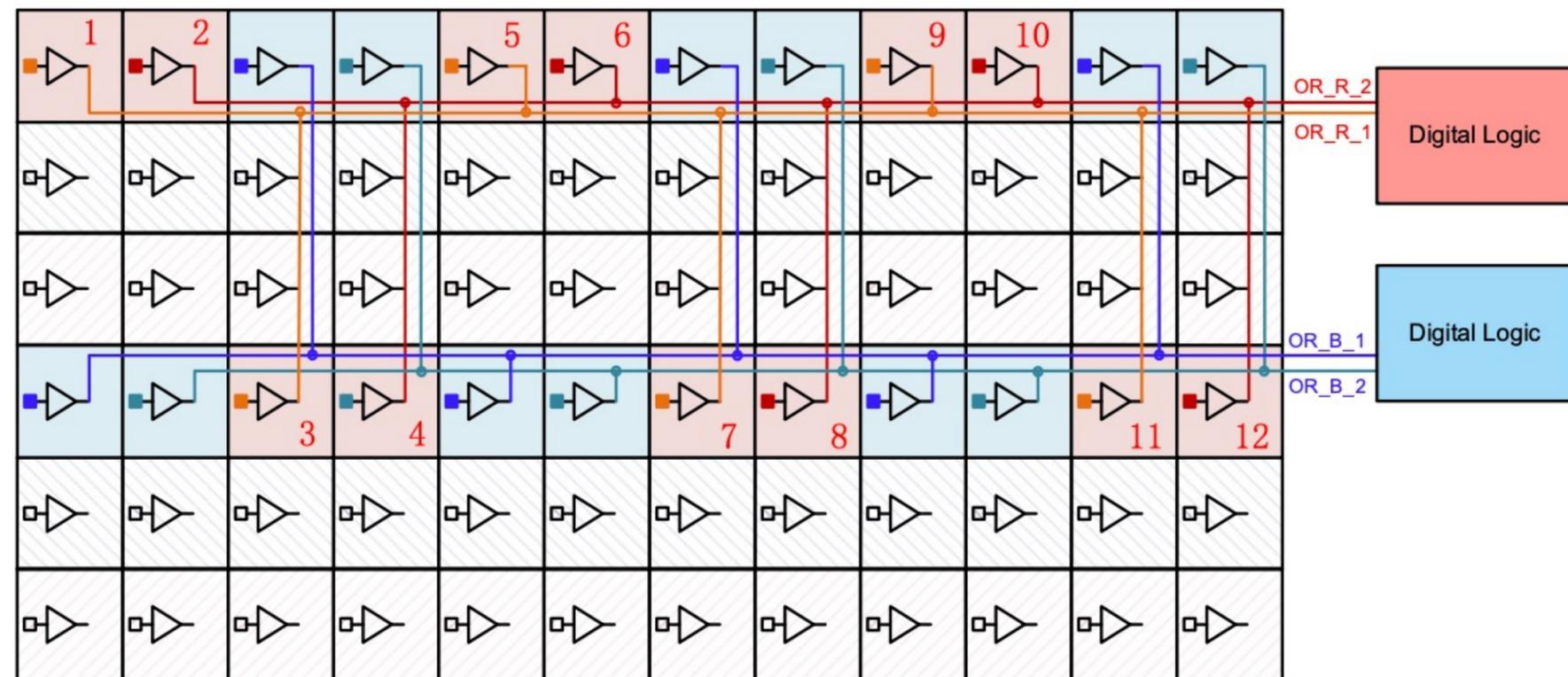
# Super Pixel Design

- ❖ Combining non-adjacent pixels: avoid ToT loss
- ❖ Super pixel with  $6 \times 12$  pixel array
  - 6 sets of digital readout logic
  - When cluster size  $< 3 \times 4$ , no ToT loss occurs

Additional 3-bit for group address



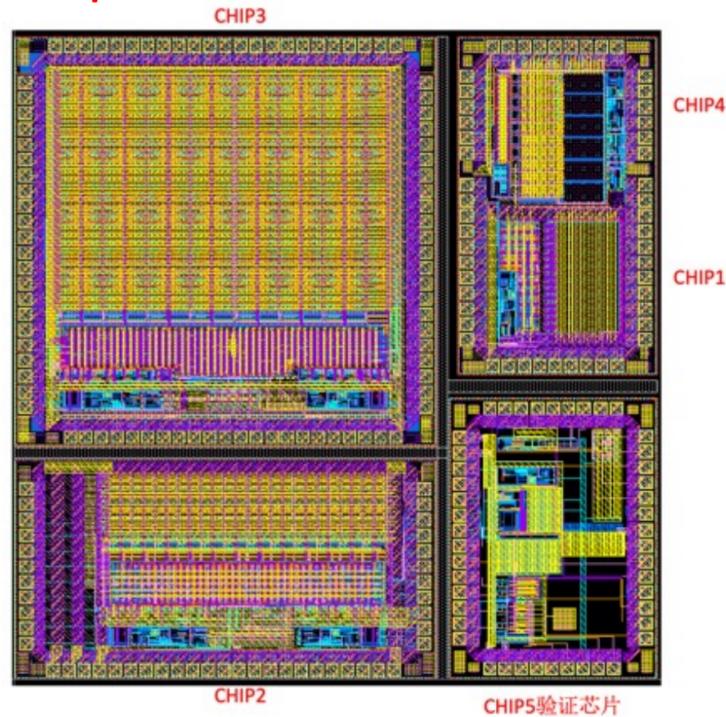
Combining adjacent pixels  
→ ToT loss



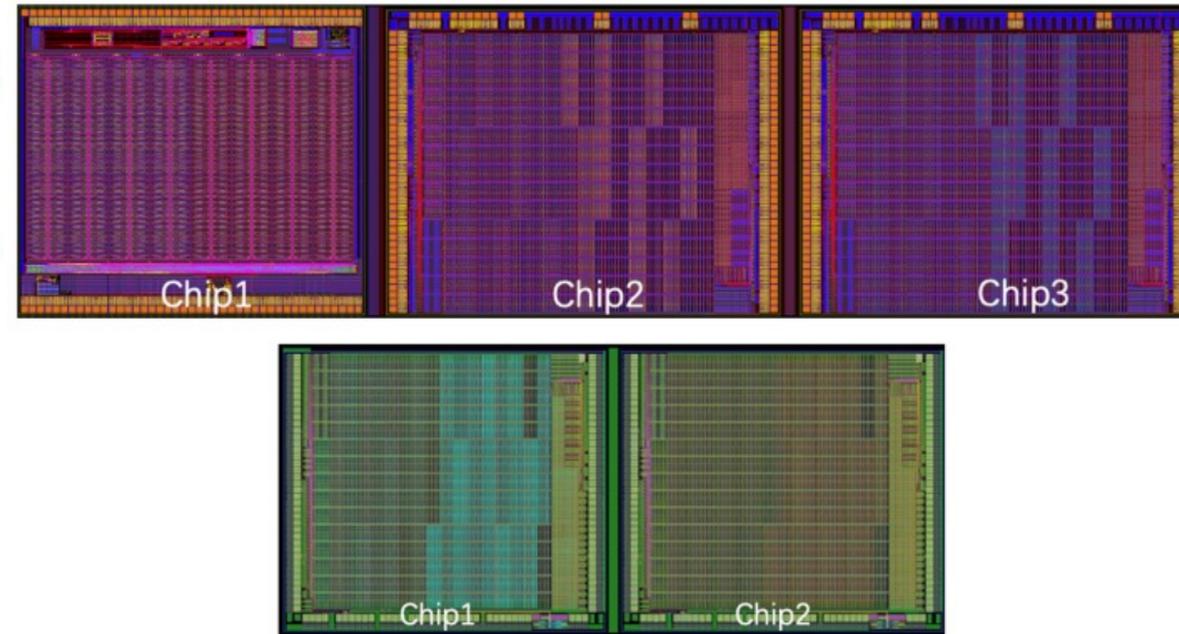
- Providing both high position and high time resolutions for low power consumption

# ITK MAPS Designs

**TowerJazz 180nm**  
Taped out in March 2024



**NexChip BCIS 90nm (Hefei, China)**  
To be taped out in Dec. 2024



**GSMC 130nm (Shanghai, China)** Taped out in Sep. 2024



## Simulated performance

	TJ-MAPS	GSMC-MAPS
<b>Current</b>	<b>800 nA/pix</b>	<b>120*6 nA/pix</b>
Supply Voltage	1.8 V	1.2 V
Threshold	309.0 e <sup>-</sup>	153.8 e <sup>-</sup>
ENC	11.4 e <sup>-</sup>	5.1 e <sup>-</sup>
Mismatch	5.7 e <sup>-</sup>	5.8 e <sup>-</sup>
<b>t<sub>r</sub> @400 e<sup>-</sup></b>	<b>200 ns</b>	<b>81 ns</b>

Items	Power consumption	Notes
Analog in pixel matrix	~26 mW/cm <sup>2</sup>	Strip-based
	~15 mW/cm <sup>2</sup>	Pixel-based
Timestamp clock distribution	12.2 mW/cm <sup>2</sup>	
Dynamic power consumption of the pixel matrix	2.4 mW/cm <sup>2</sup>	with a data rate of 8.7 MHz/cm <sup>2</sup>
Periphery	23.5 mW	32MHz event rate
PLL, serializer, LVDS	39 mW	x 2 data/clock output
Analog configuration	20 mW	
Total	222.6 mW	Strip-based
	184.6 mW	Pixel-based

- Strip-based: 55.7 mW/cm<sup>2</sup>
- Pixel-based: 46.2 mW/cm<sup>2</sup>

# Main Drift Chamber

- Preliminary mechanical design and structural analysis
- Big challenges from super-small cells (5mm\*5mm, distance between wires ~2.5mm )
- Ongoing R&D on feedthroughs, wires and chamber stringing

模型名称: 漂移板15mm  
系列名称: 垂直位移05; 默认1  
图例类型: 静态位移 位移1  
变形比例: 163.317

URES (mm)

1.064e+00  
9.574e-01  
8.510e-01  
7.446e-01  
6.382e-01  
5.319e-01  
4.255e-01  
3.191e-01  
2.127e-01  
1.064e-01  
1.000e-30

BESIII 定位子

BELLEII 定位子

STCF 定位子V1  
铜管, 放电工艺

STCF 定位子V2  
铝管, 拉丝工艺

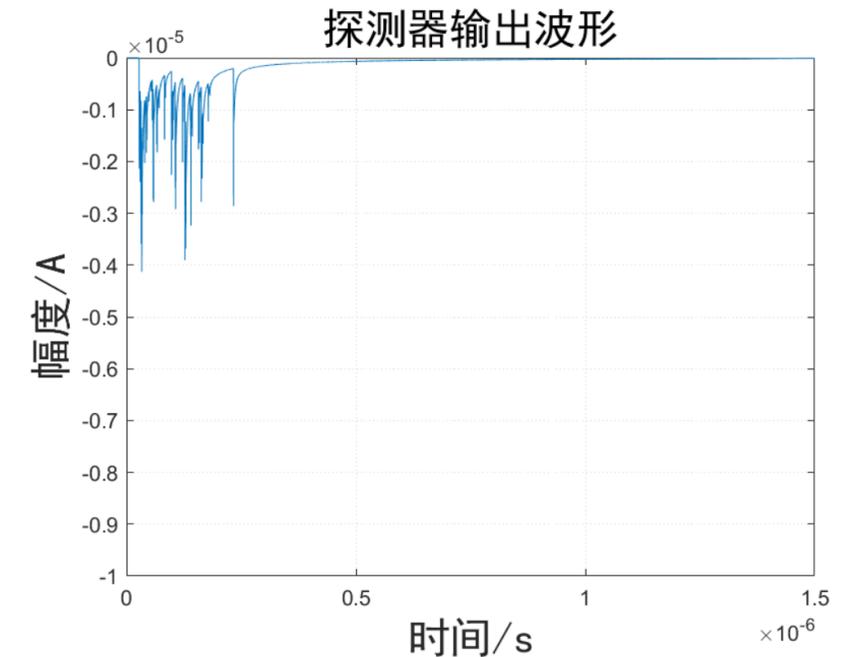
STCF 定位子V3  
减小尺寸, 增加电极连接

图例标题

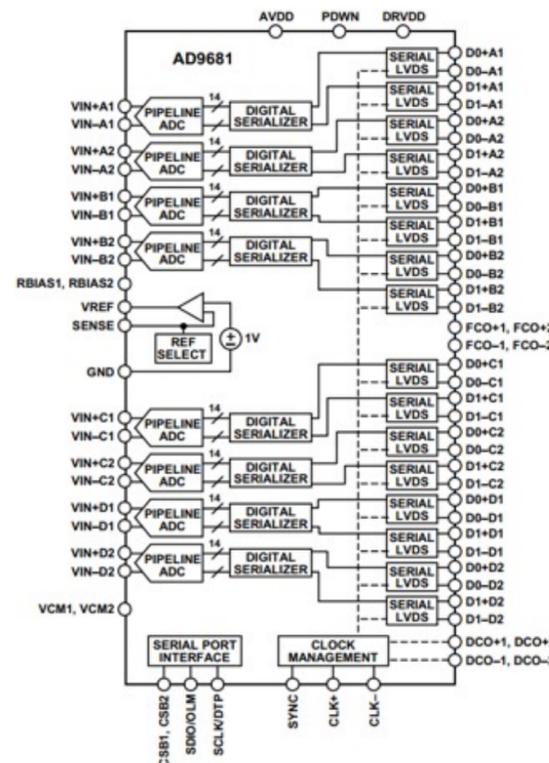
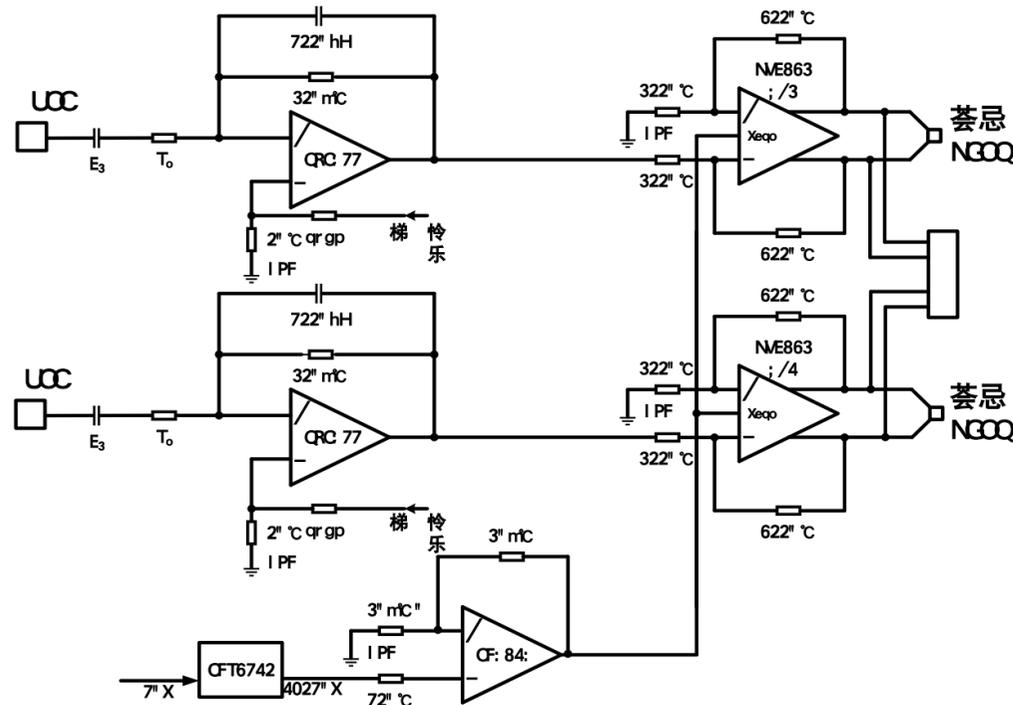
17

# MDC Readout Electronics

- **Challenge: irregular pulse signals overlapping at high rates**
- **Attempt to separate overlapping pulses with waveform digitizing readout. A lot of effort on separation algorithm development and readout optimization.**
- **Developed readout circuit with discrete components (TIA + shaper + ADC). ASIC design also underway.**



Optimized ADC specs: 14 bit, sampling rate 125 MSPS, bandwidth 650 MHz

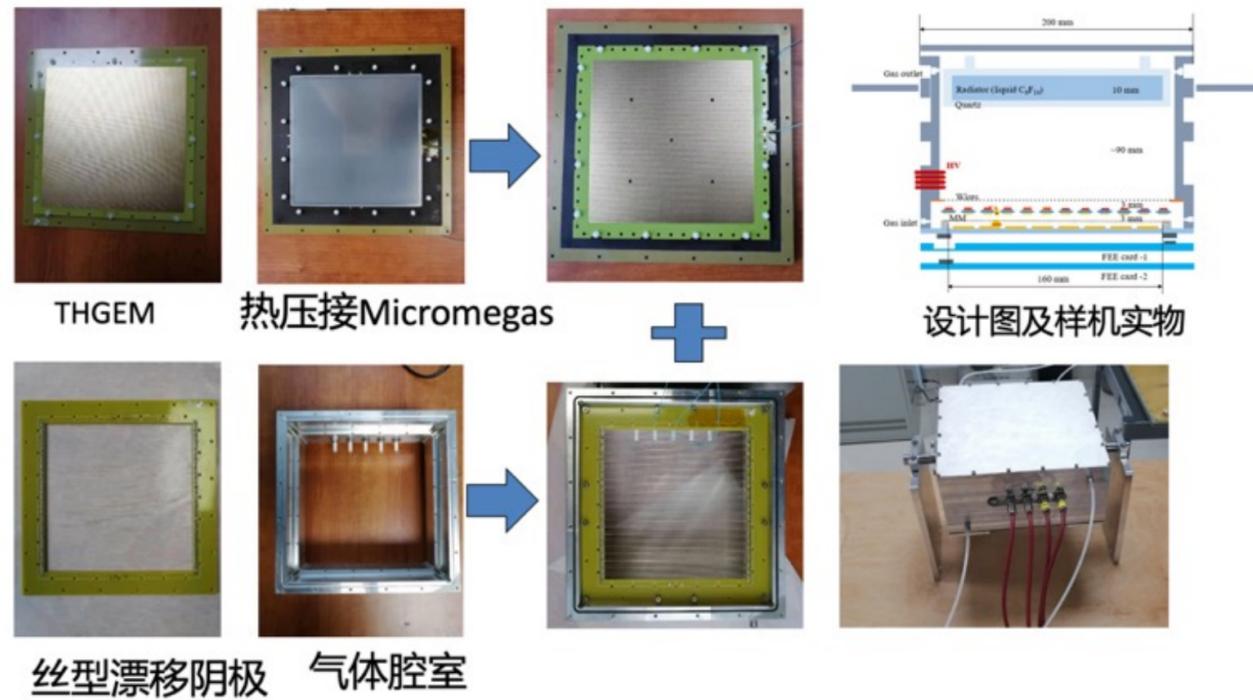


Readout board (16 chs) being tested

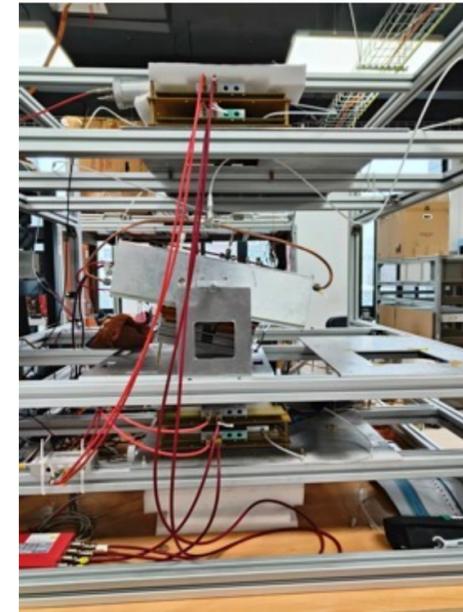


# PID Barrel: RICH Detector R&D

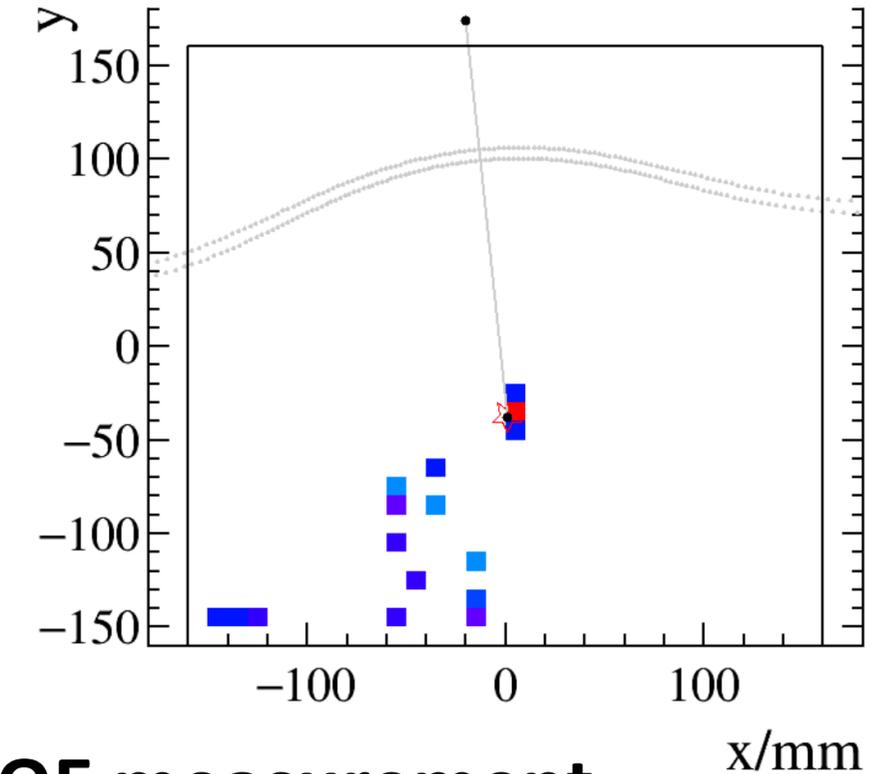
## Fabrication of 30cm\*30cm RICH prototype



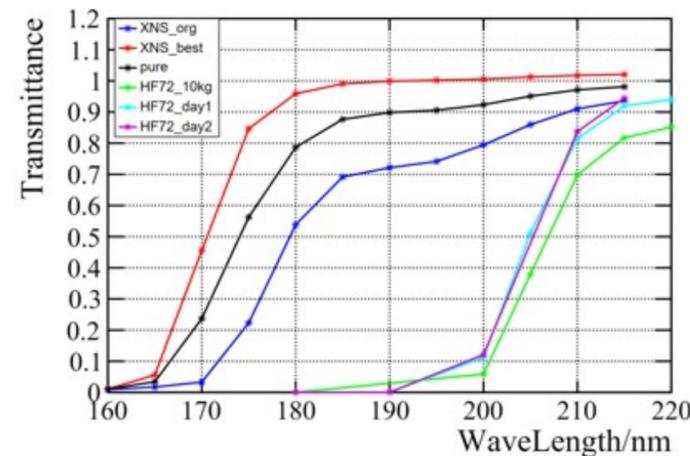
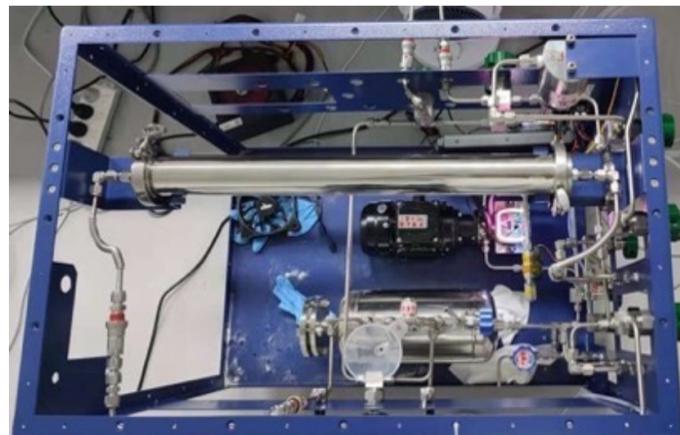
## Cosmic-ray test



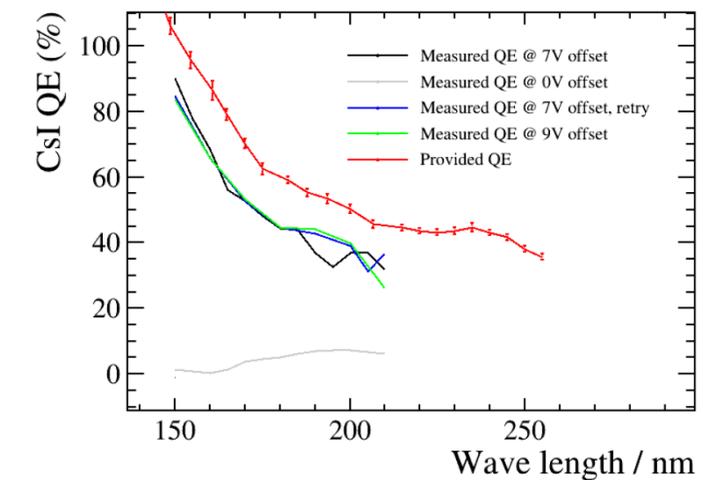
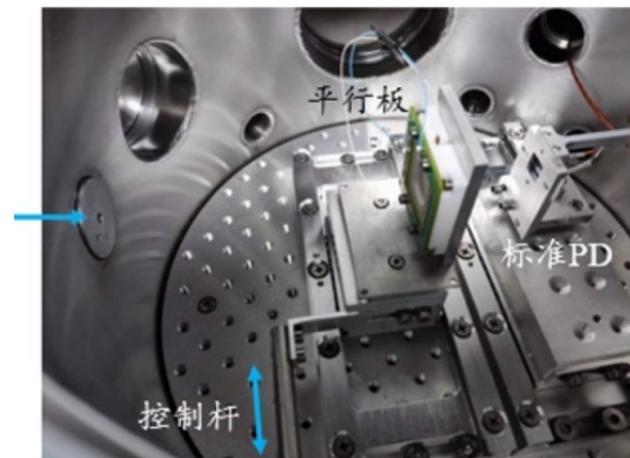
## Very weak light observed Investigation ongoing



## Radiator purifying

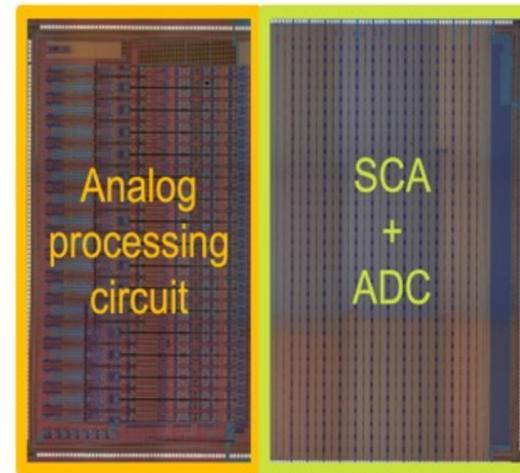
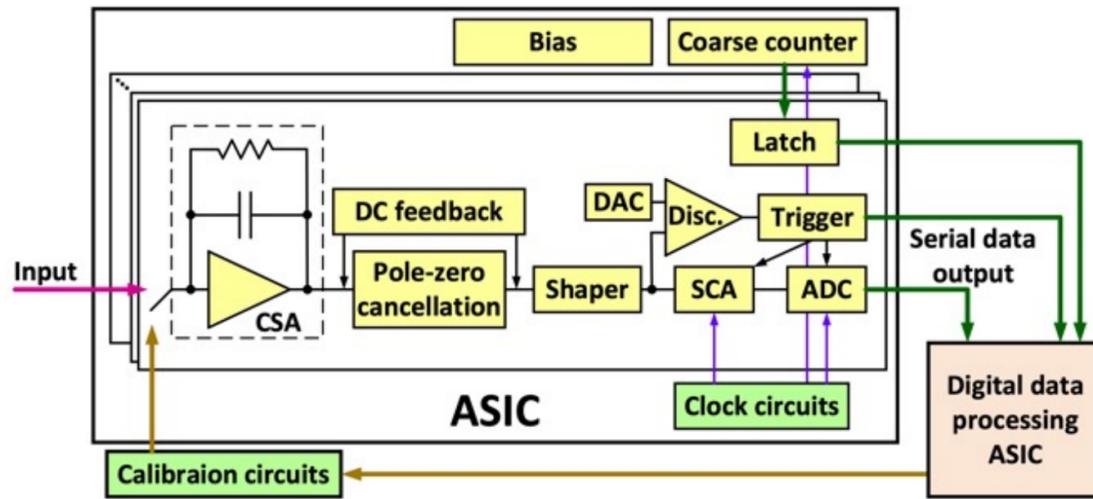


## CsI coating and QE measurement

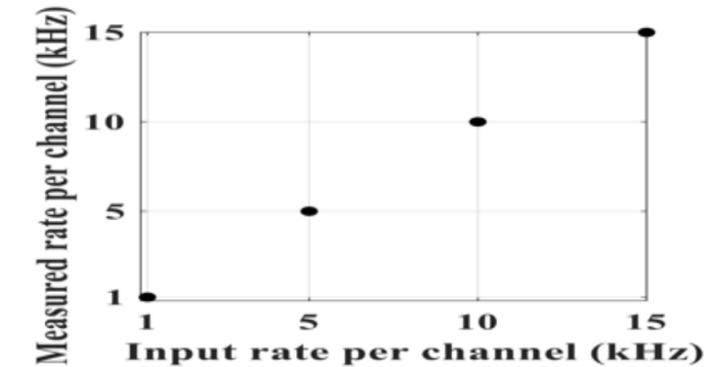
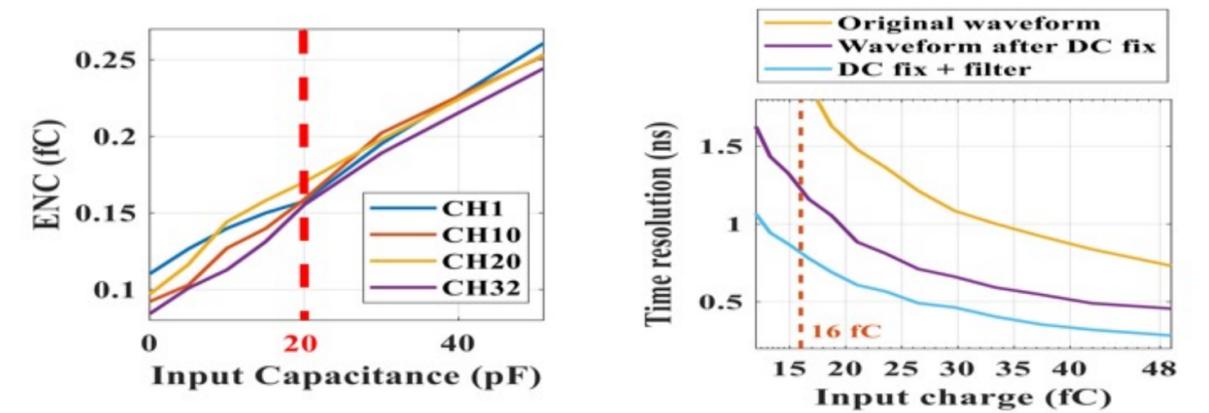


# RICH Readout ASIC

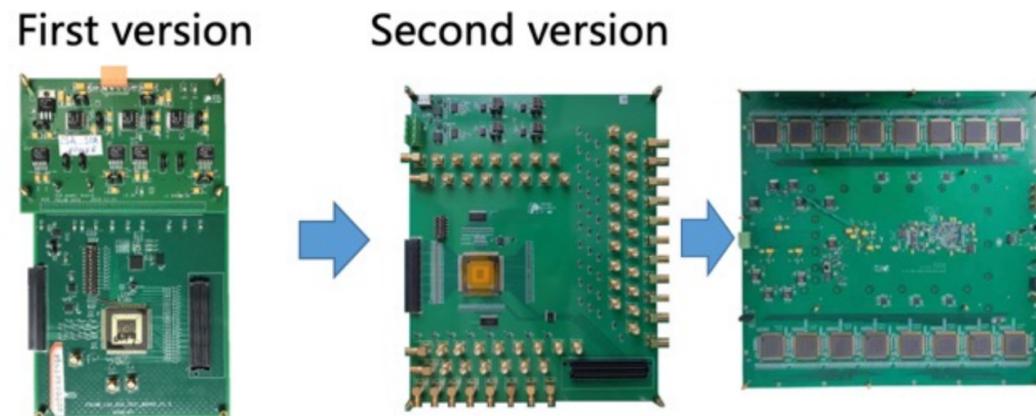
Design specs:  $\sigma_t < 1\text{ns}$  @20fC&20pF,  
event rate  $\sim 100\text{ kHz}$ , 32 channels



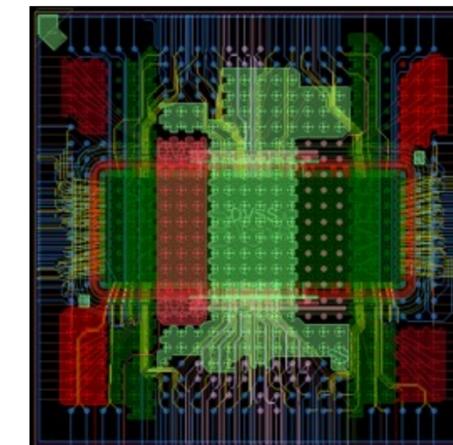
## Test results



## Design iterations

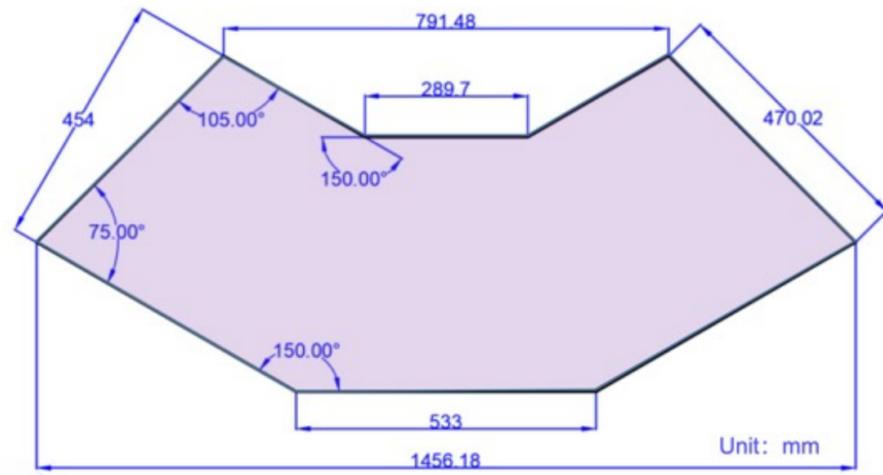


512-channel readout board using the self-developed ASIC

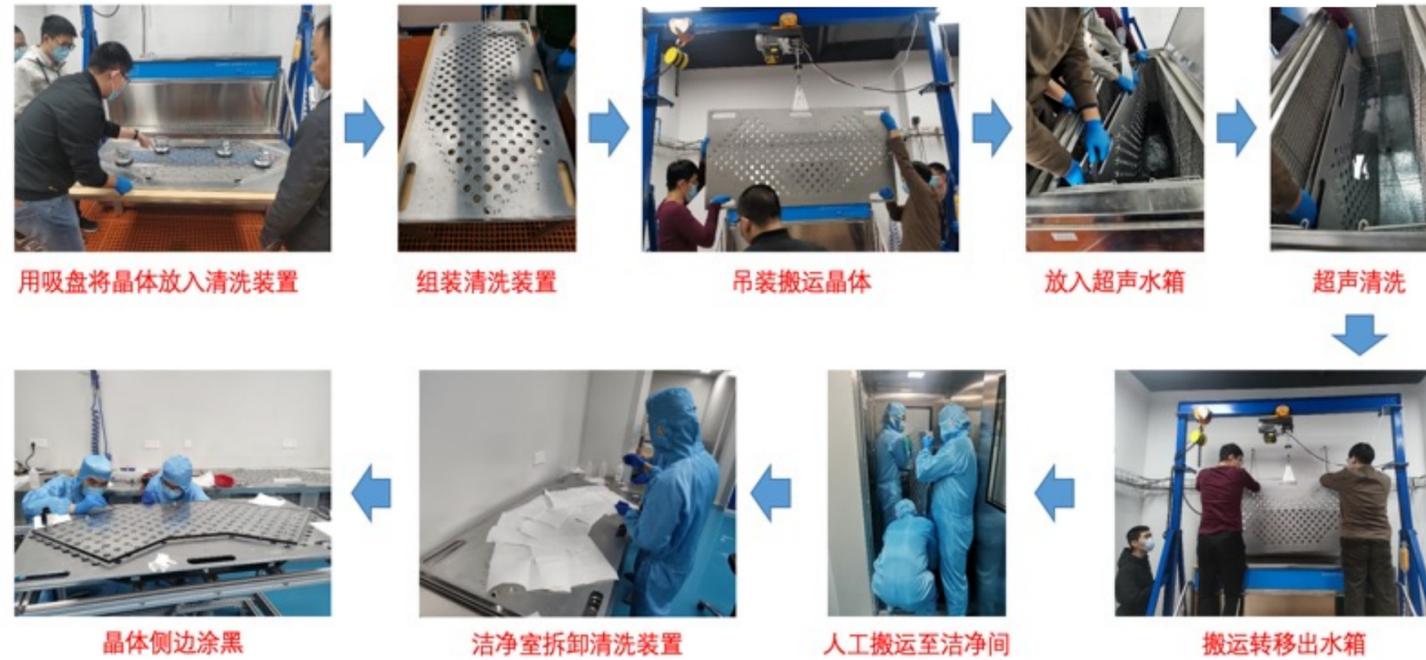


Design with 64 channels is underway

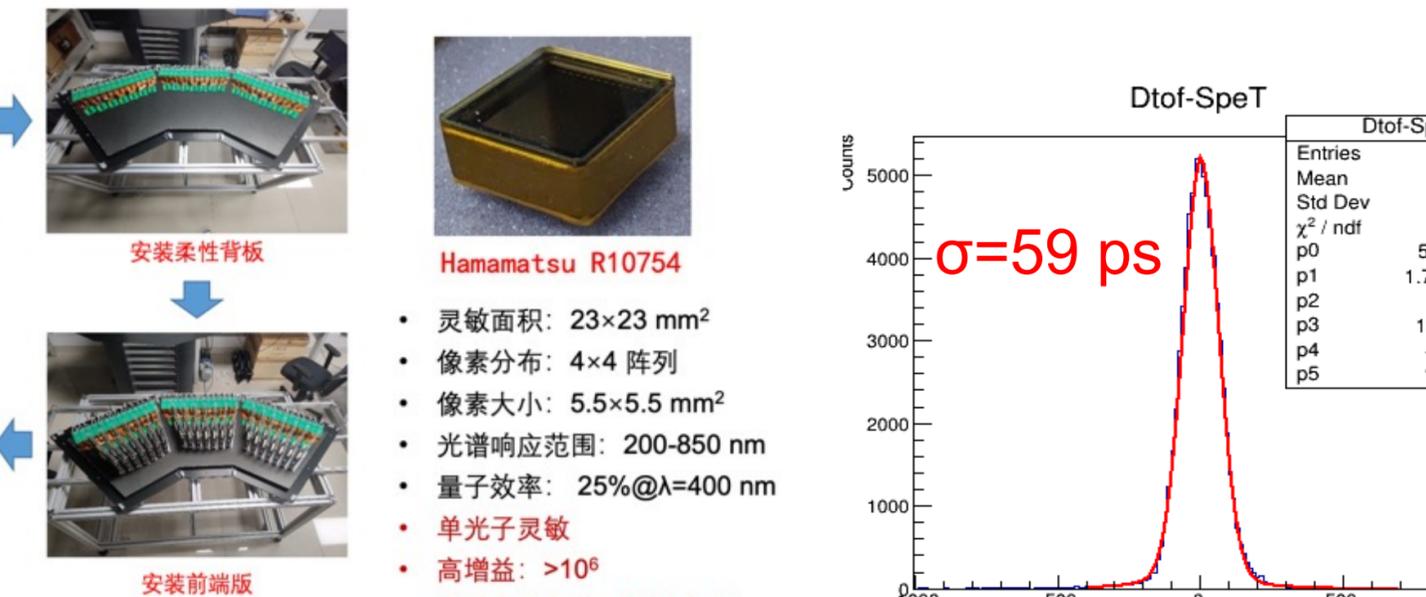
# PID Endcap: A full-sized DTOF prototype



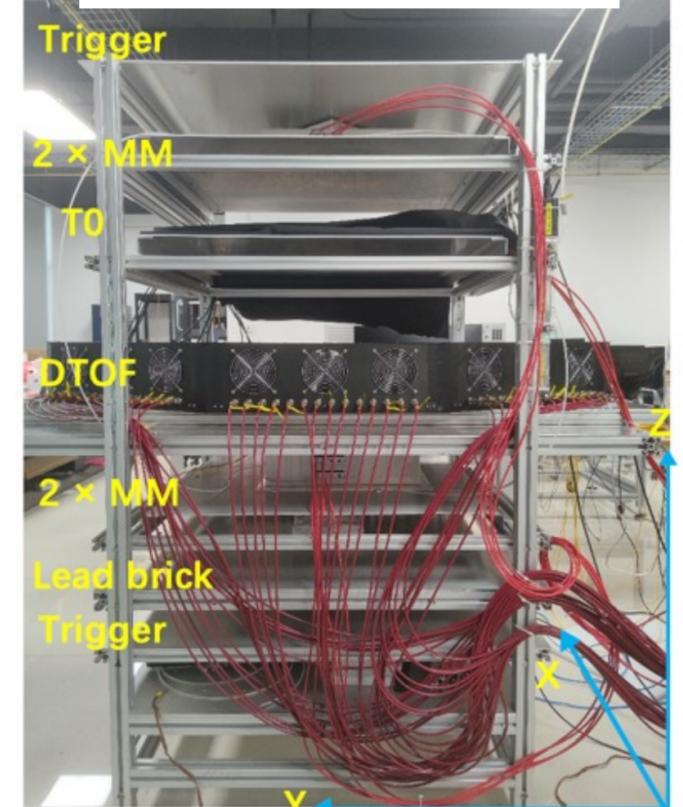
## 石英清洗和安装



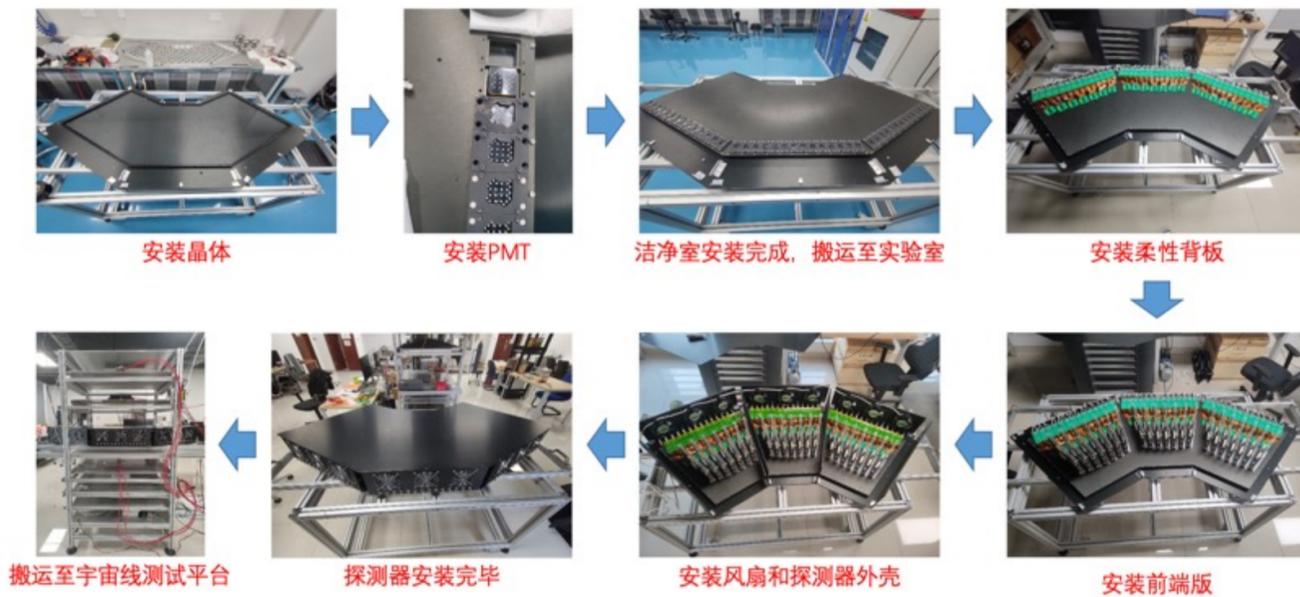
## Quartz radiator cleaning and mounting



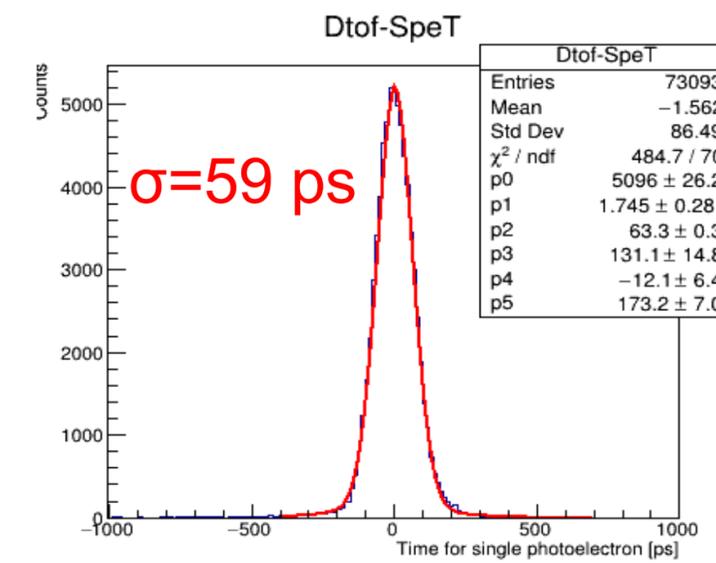
## Cosmic-ray test



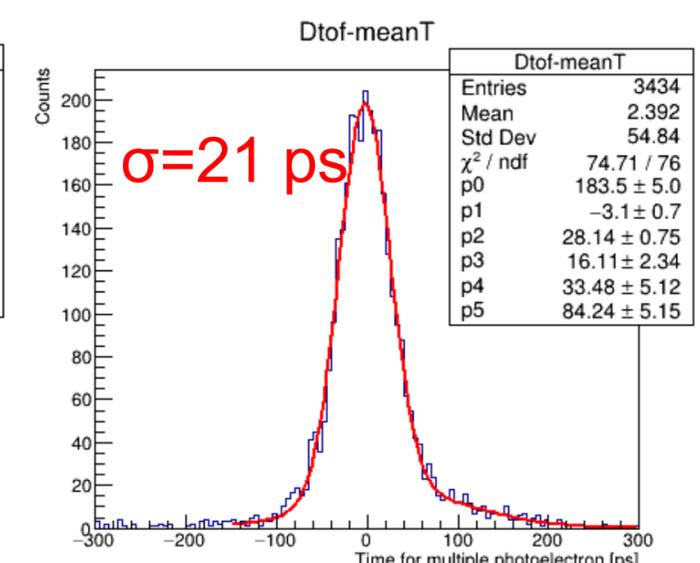
## Detector assembling



- Hamamatsu R10754**
- 灵敏面积:  $23 \times 23 \text{ mm}^2$
  - 像素分布:  $4 \times 4$  阵列
  - 像素大小:  $5.5 \times 5.5 \text{ mm}^2$
  - 光谱响应范围: 200-850 nm
  - 量子效率:  $25\% @ \lambda = 400 \text{ nm}$
  - 单光子灵敏
  - 高增益:  $> 10^6$
  - 增益非均匀性:  $14\% (\sigma/\mu)$
  - 时间性能:  $\sim 27 \text{ ps}$



single photon time resolution

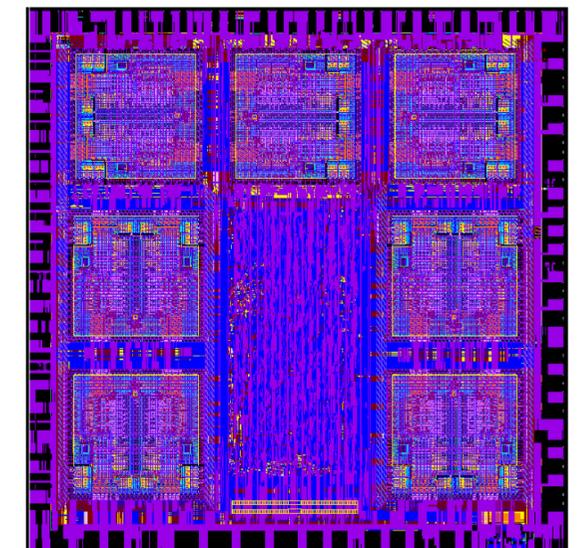
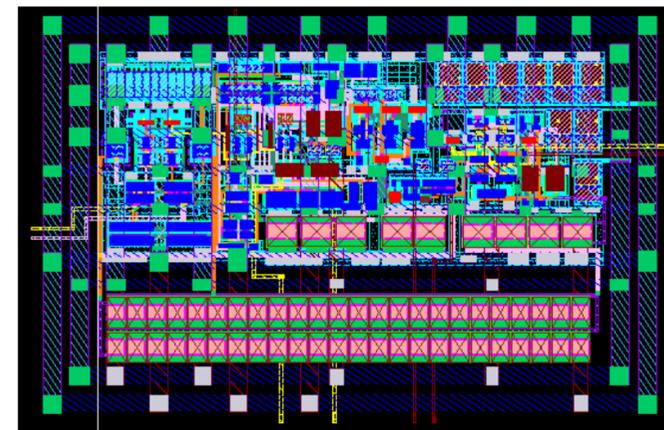
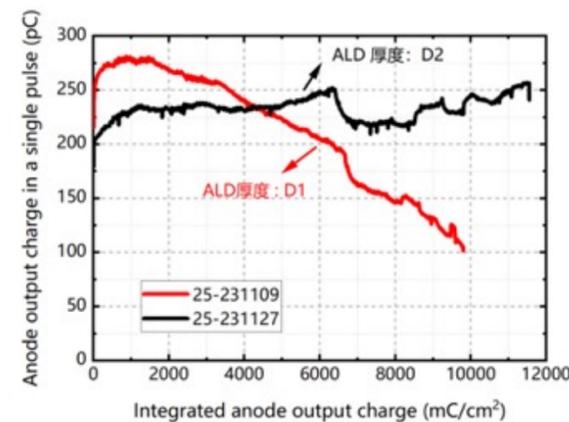
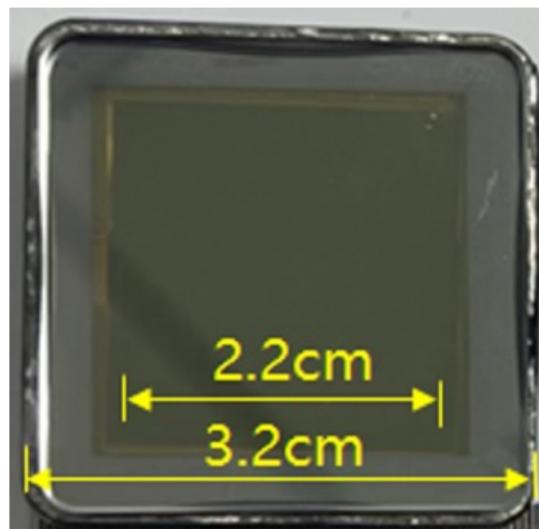
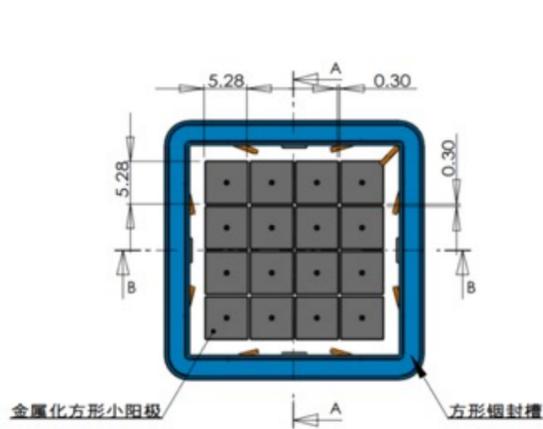
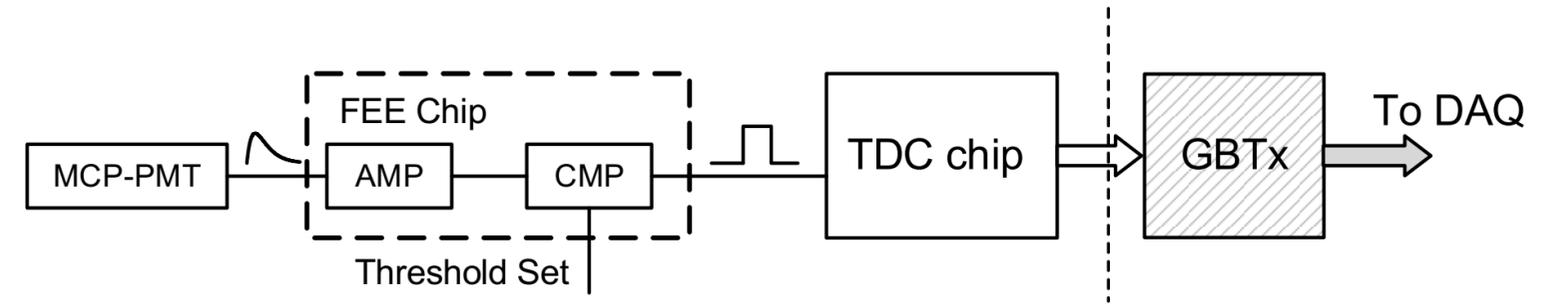


Single track time resolution

# DTOF R&D on MCP-maPMT and Readout ASICs

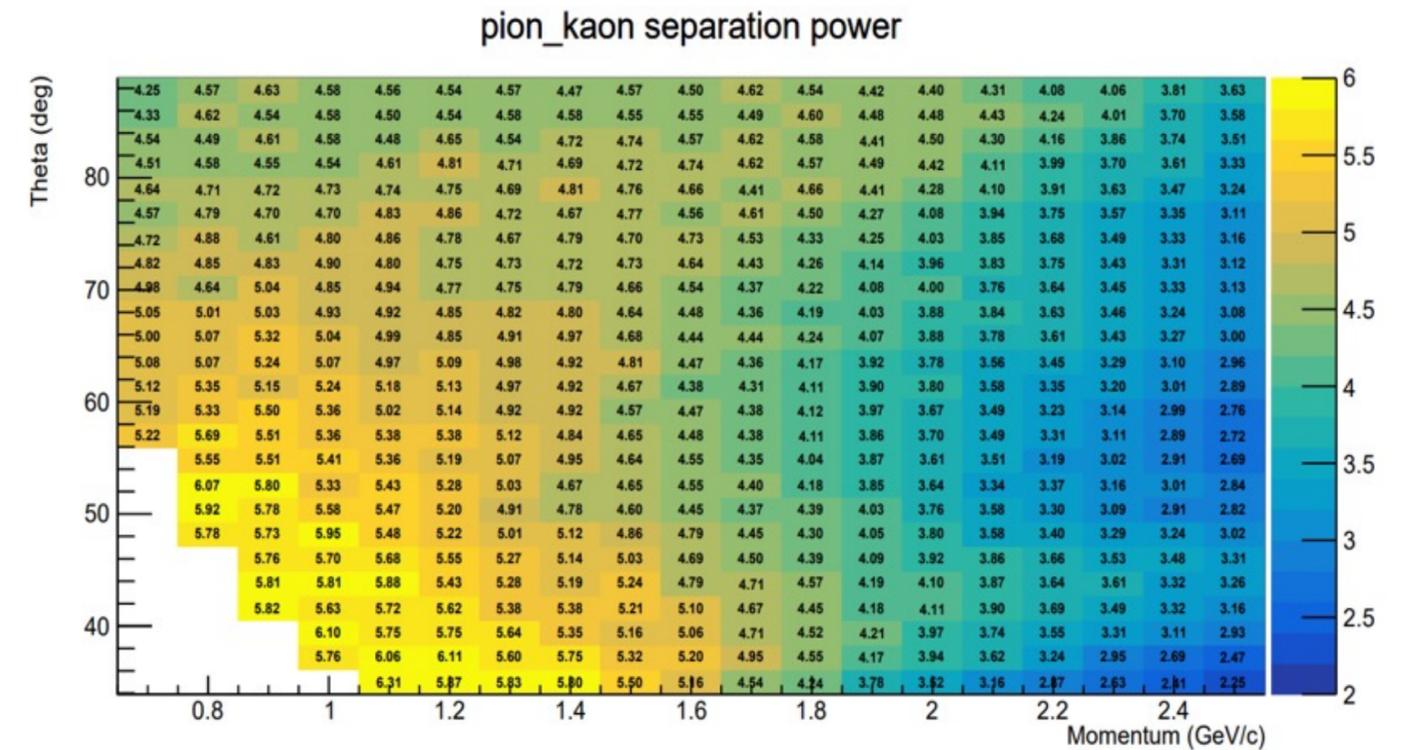
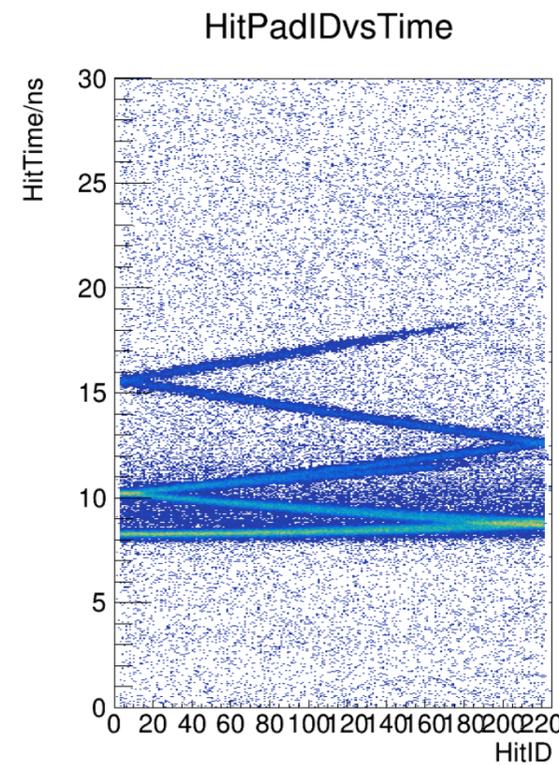
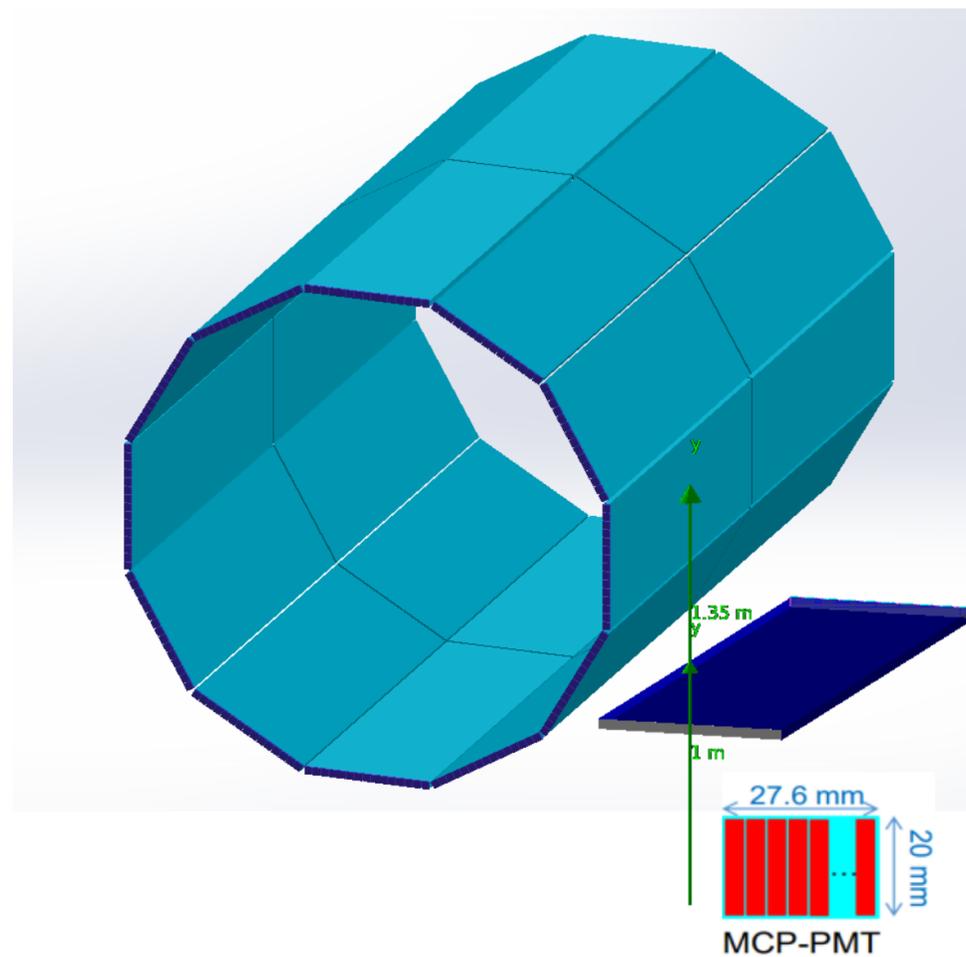
- MCP-maPMT: a critical component of the DTOF technology
- Designed and produced 1-inch MCP-maPMT with 16 anodes, TTS < 40 ps
- Intensive R&D on techniques (ALD and electron scrubbing) to produce long-life MCP-PMT (target > 10 C/cm<sup>2</sup>)

- Two ASICs designed for MCP-maPMT readout.
  - FET (taped out), target ~ 15 ps
  - TDC (taped out), target ~ 15 ps



# Application of DTOF in Barrel

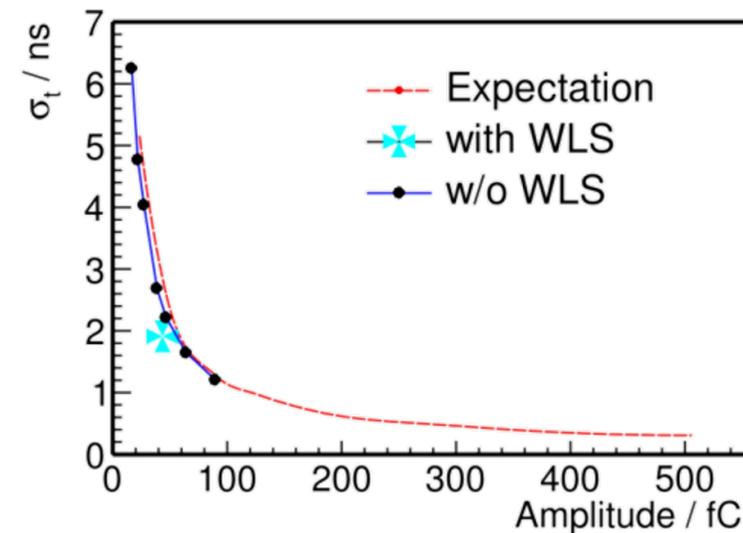
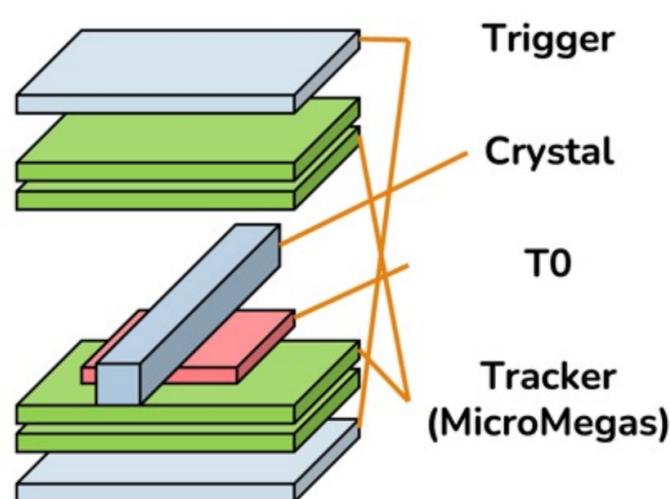
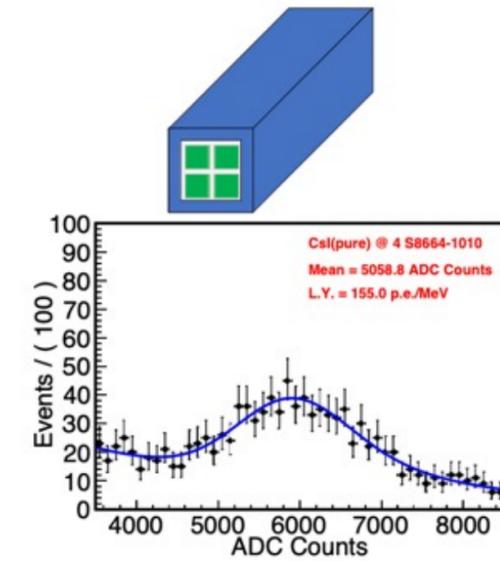
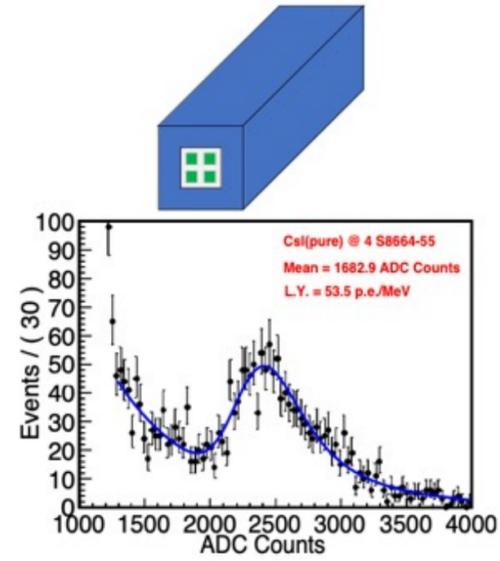
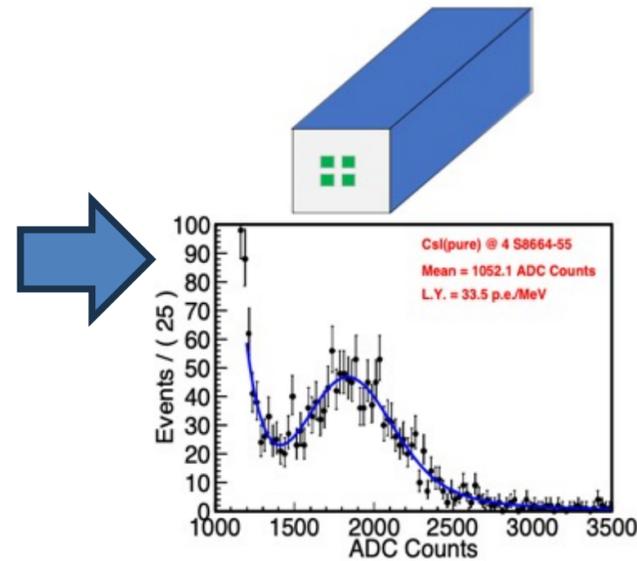
- Conceptual design of barrel PID based on the DTOF technology
- Design optimization by scanning a variety of key design parameters
- Performance with full simulation mostly meet PID requirements
- More studies and work are planned



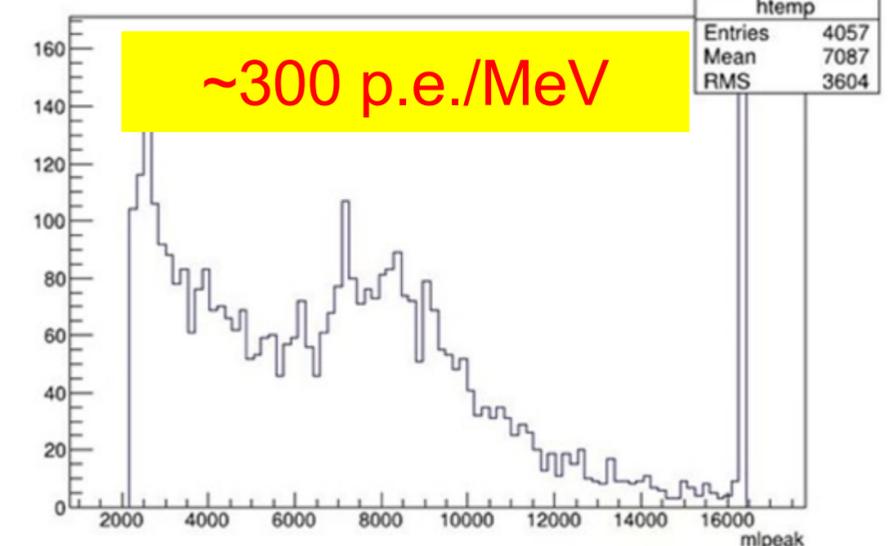
# pCsI EMC : Light yield and timing studies

A major R&D task : enhancing light yield

reflector: 225um thick Teflon



CsI + NOL53 + NOL53 + Teflon

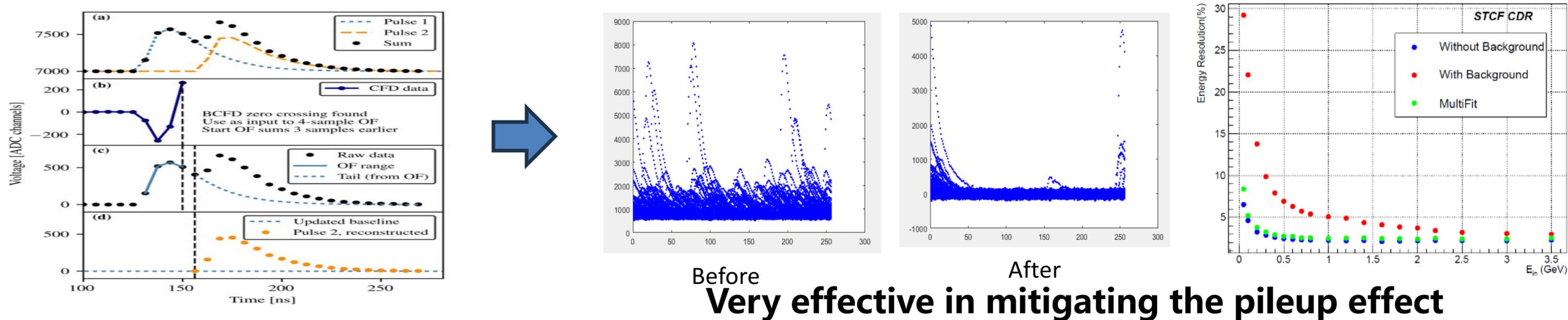


$\sigma_t$  : 2.0 ns @ 0.03 GeV, 0.8 ns @ 0.1 GeV

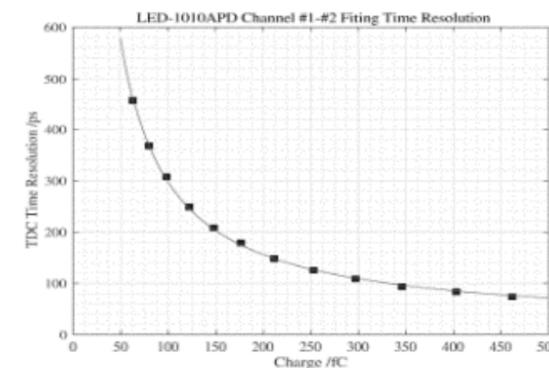
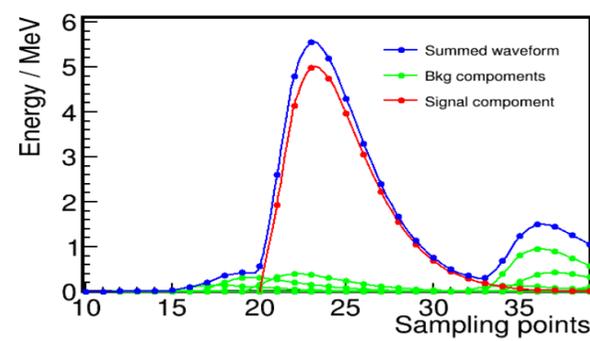
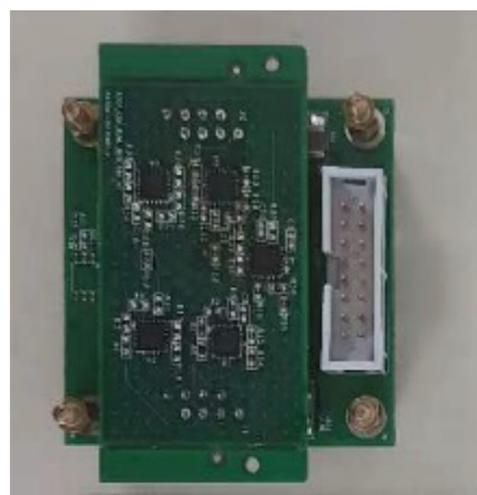
Light yield reached up to 300 p.e./MeV

# pCsl EMC : Pileup mitigation and electronics

## Waveform fitting to remove pileup noise (~1 MHz/ch) and extract signals

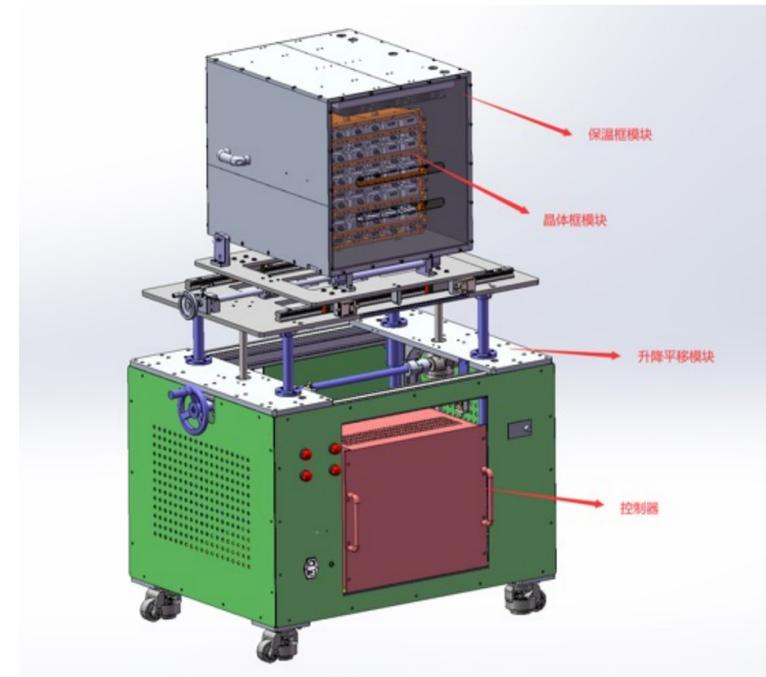
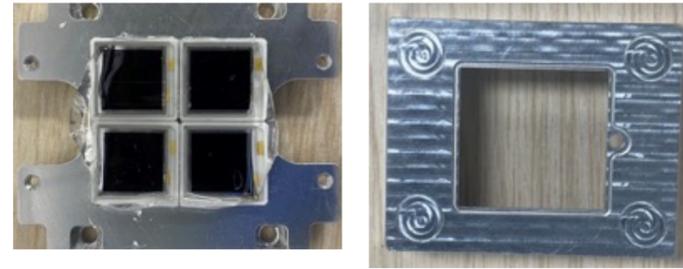
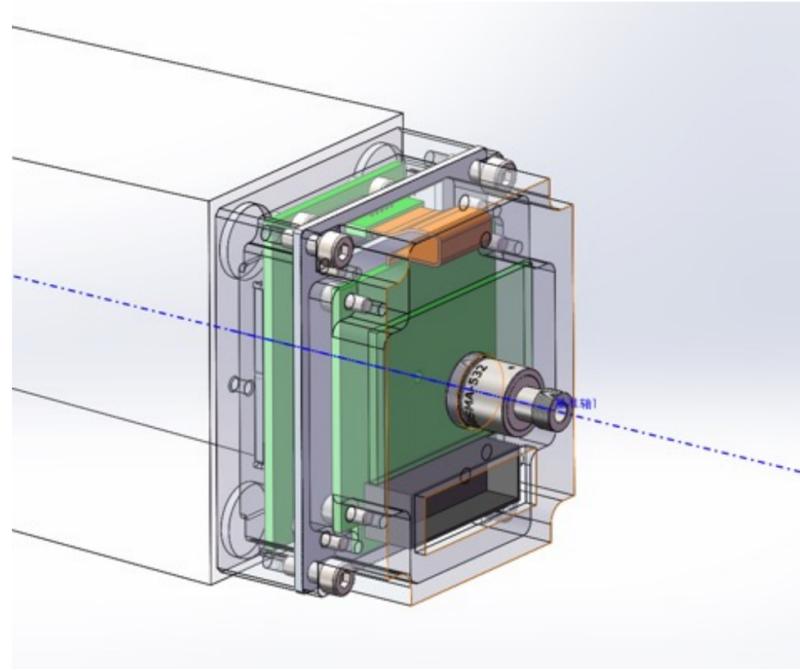
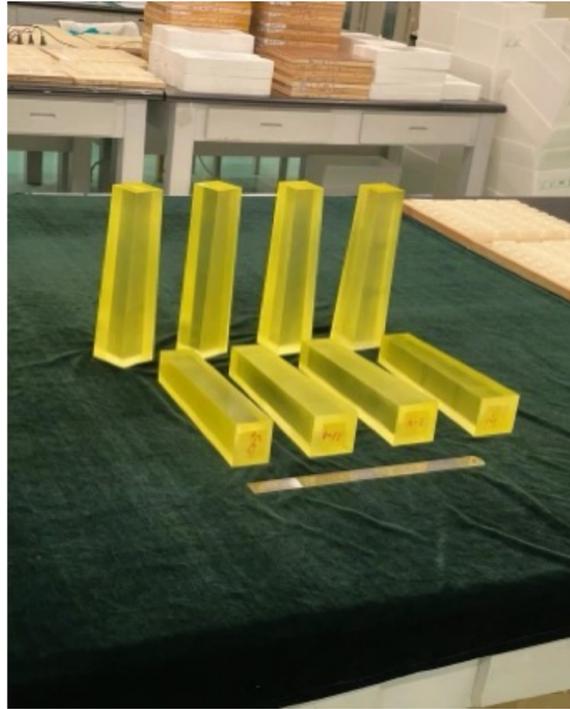


## Development of waveform digitization electronics (CSA + shaper + ADC)



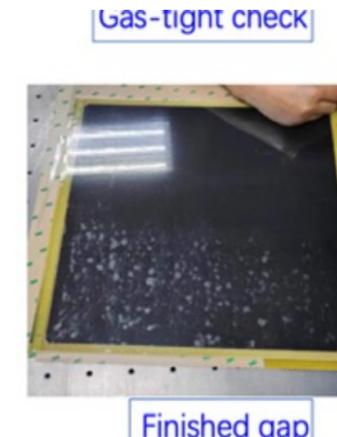
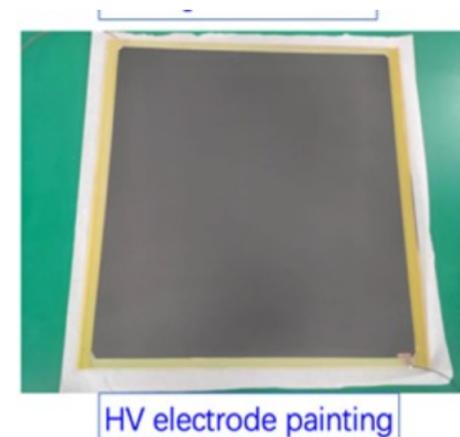
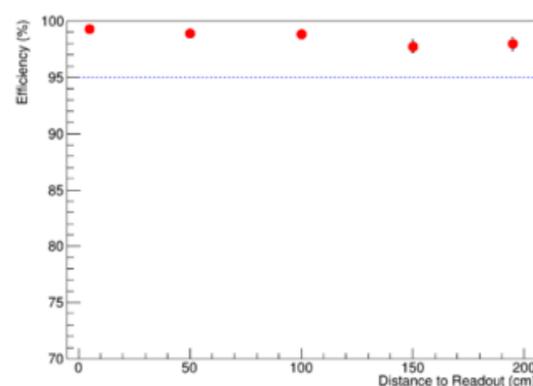
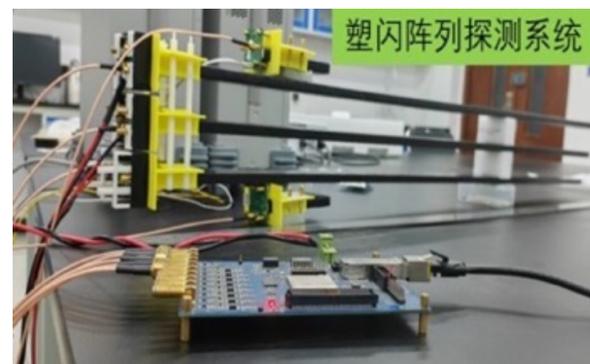
Dynamic range:  
3 MeV ~ 3 GeV  
ENE: ~ 0.4 MeV  
Time resolution :  
< 150 ps@1GeV

# 5 × 5 pCsl EMC Prototype

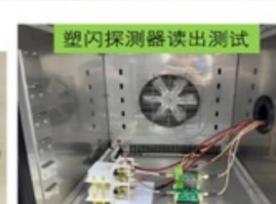
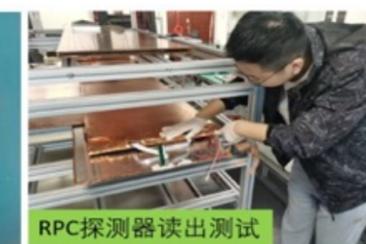
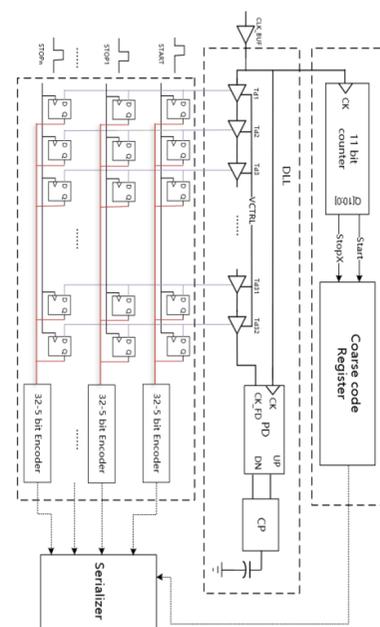
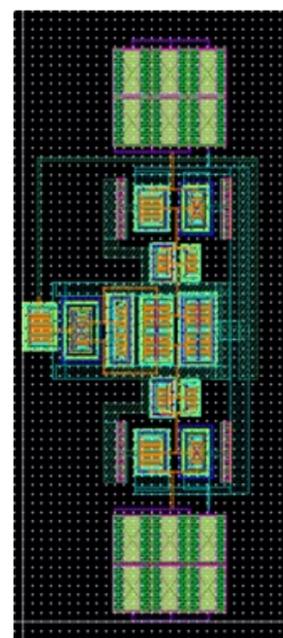
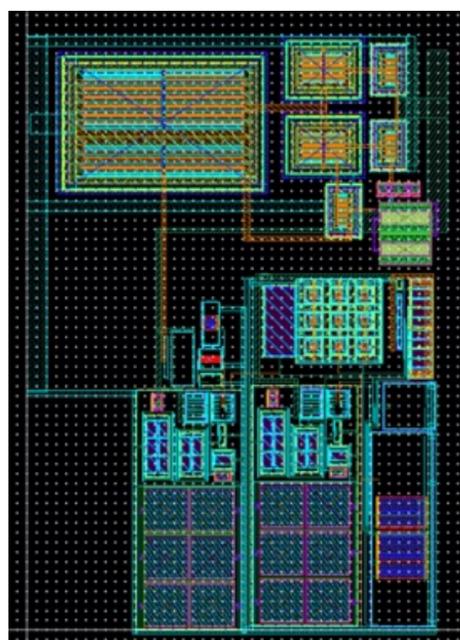


# MUD R&D

- Fabrication and performance studies of large-sized scintillator strips and glass RPC

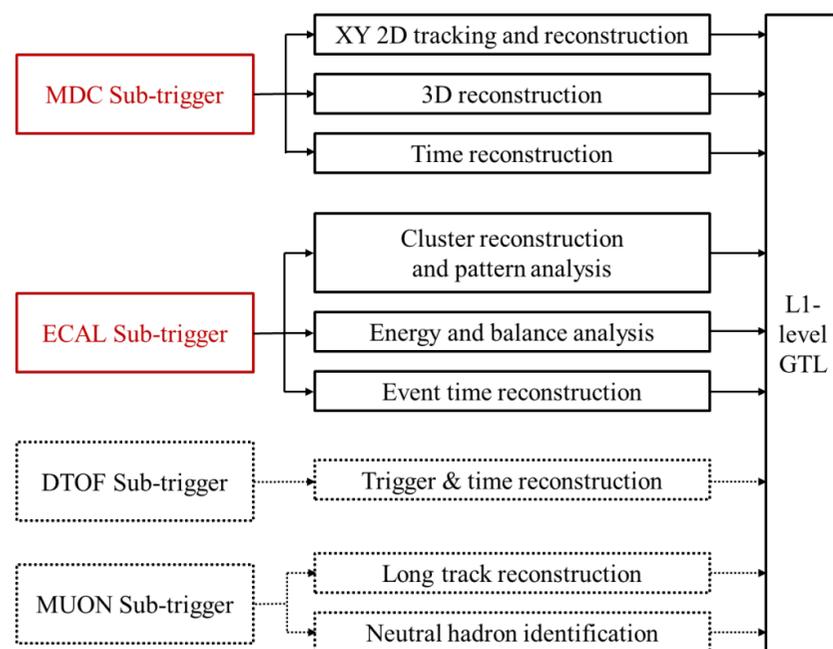
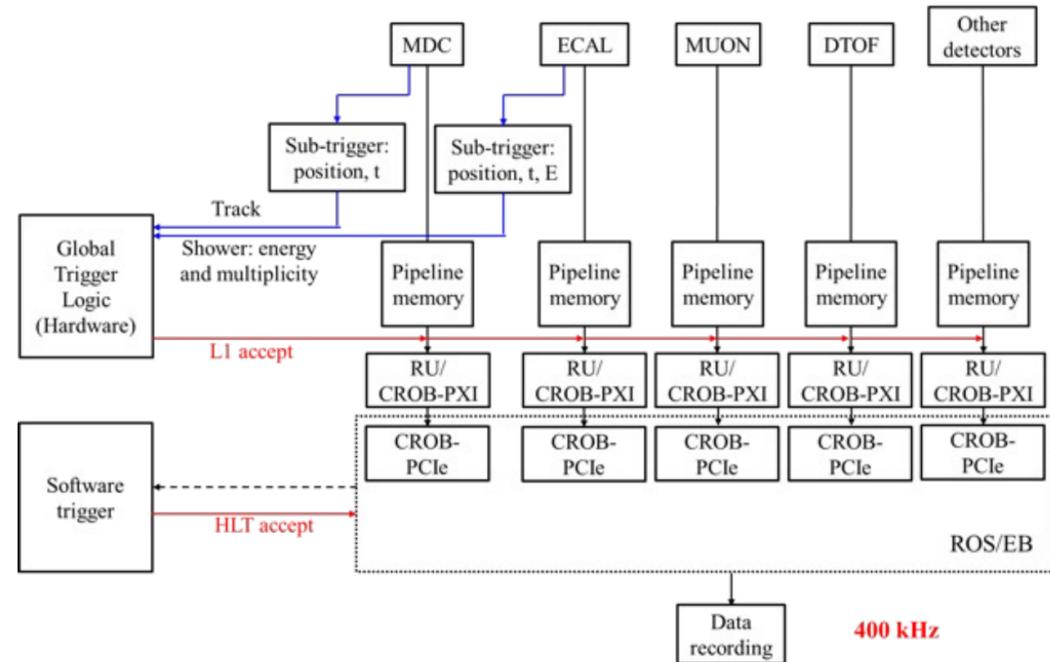


- Design of readout ASICs (FEE + TDC) is underway. First version of the EFF chip already available. Readout electronics with discrete components has been developed for detector testing and characterization



# Trigger and DAQ

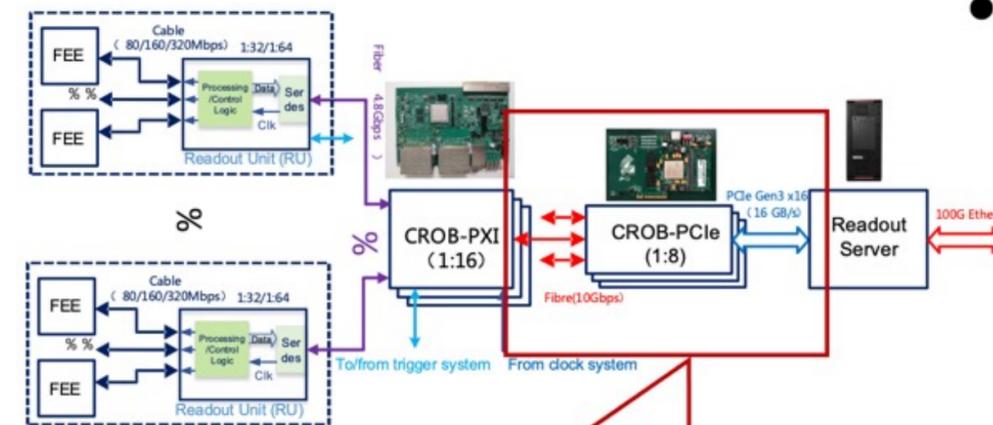
Physics event rate ~ 400 kHz



Component	Num. of channels	Readout time window	Event size (B)	Total (B/s)
ITK (Silicon)	50M	500 ns	14300	5.72G
ITK ( $\mu$ RWELL)	10552	500 ns	17232	6.89G
MDC	11520	1 $\mu$ s	20400	8.16G
PID (RICH)	518400	500 ns	15600	6.24G
PID (DTOF)	6912	500 ns	7380	2.95G
EMC	8670	500 ns	15000	6.00G
MUD	41280	500 ns	262	105M
Total(Silicon)	50.6M	-	72.9k	29.2G
Total( $\mu$ RWELL)	594k	-	75.9k	30.4G

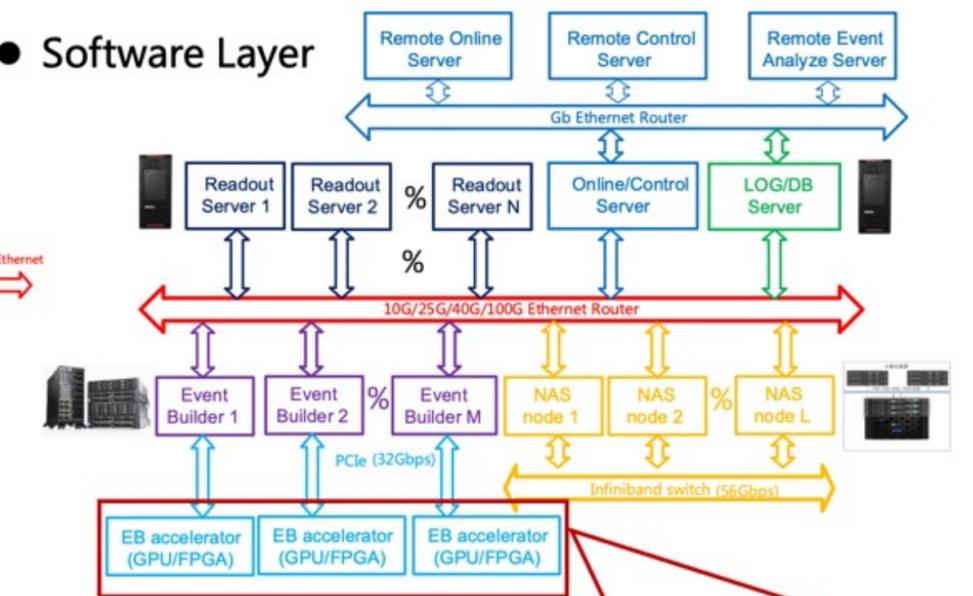
Raw data rate ~ 200 GB/s , after L1 trigger ~ 30 GB/s (latest estimates: ~30 GB/s, ~ 10 GB/s) , HLT is required, anyway.

## ● FPGA Layer



Optional: FPGA 10G Ethernet core: FPGA → Computer Farm

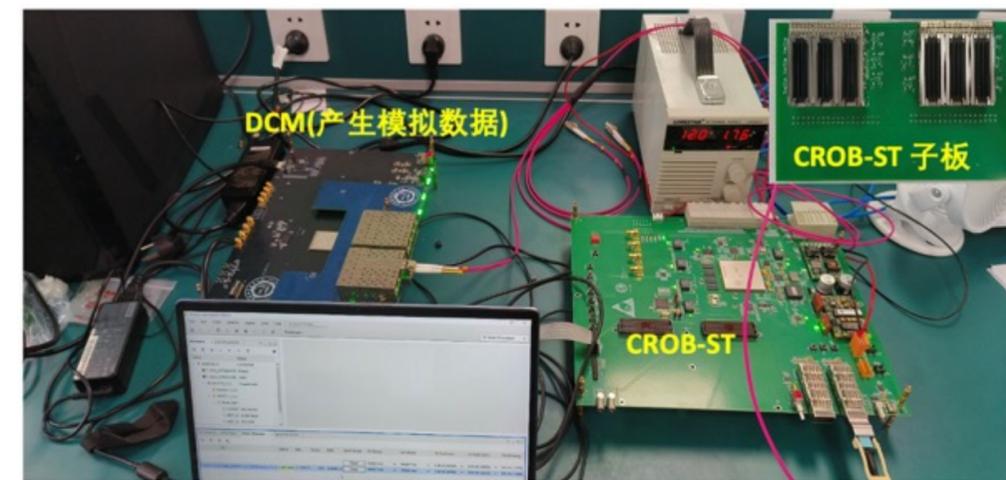
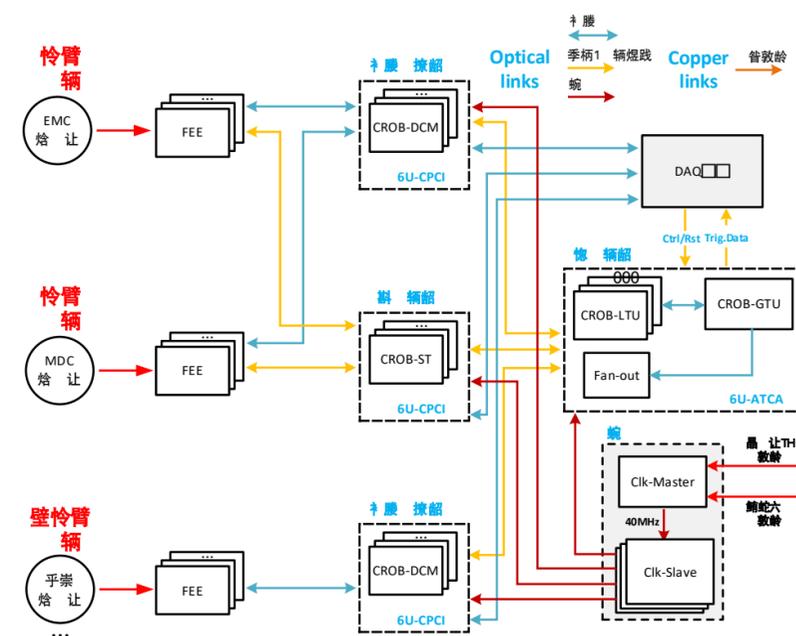
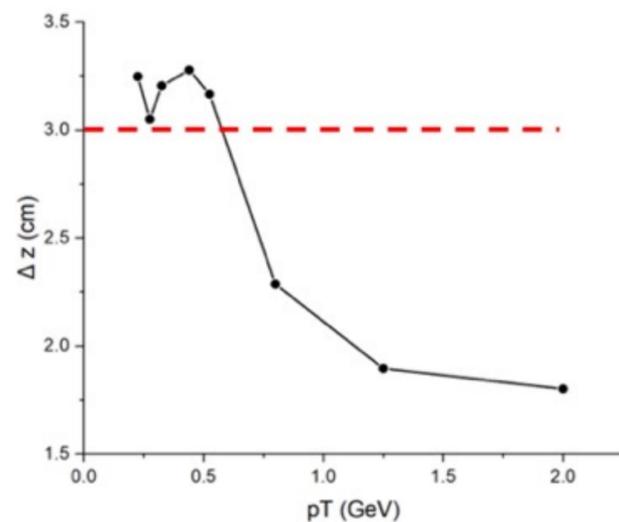
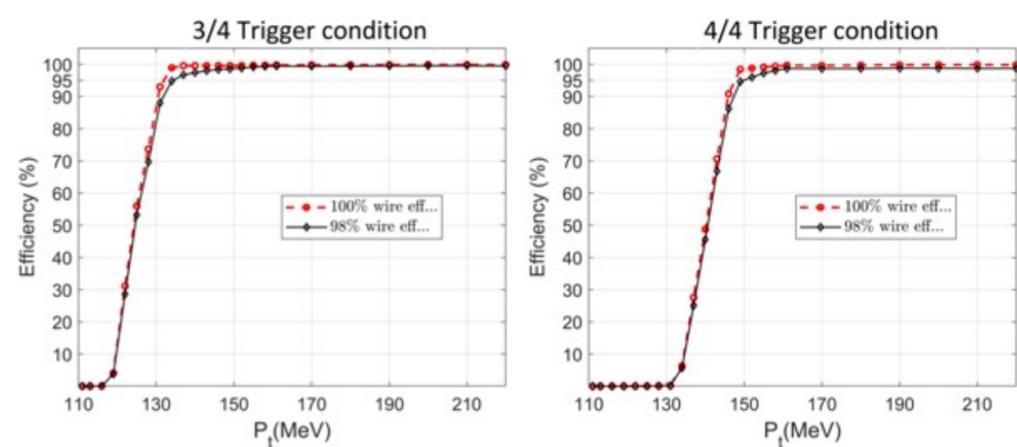
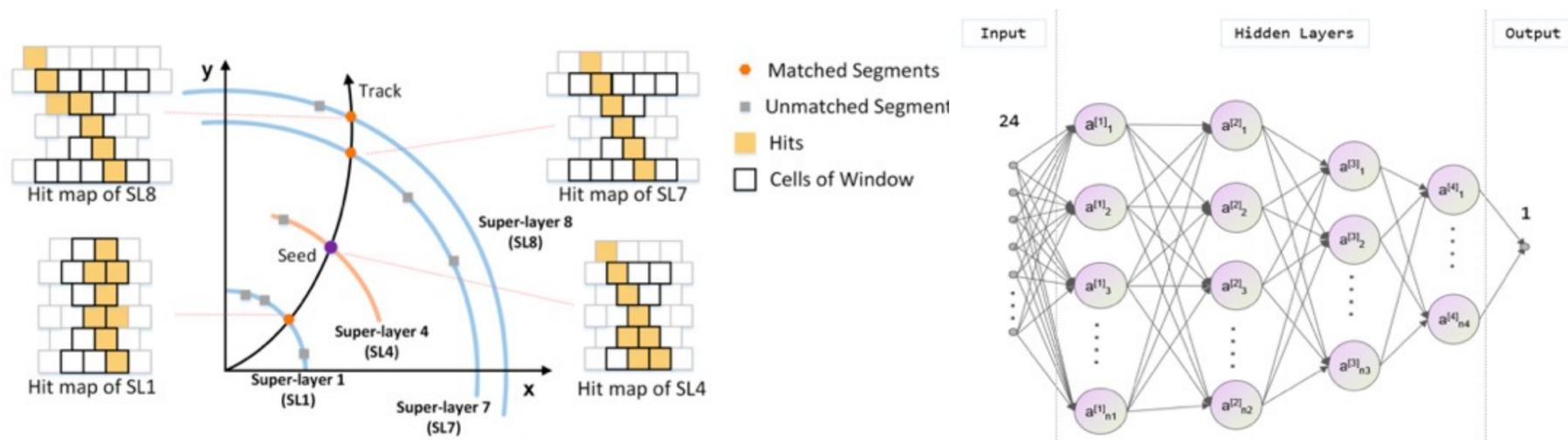
## ● Software Layer



Optional: heterogeneous computing based on FPGA and/or GPU

# Trigger Algorithms and hardware Development

- MDC 2D and 3D tracking algorithms, EMC clustering algorithms, global trigger algorithms.
- PFGE programming to realize the algorithms
- Design of trigger electronics and development of core hardware components

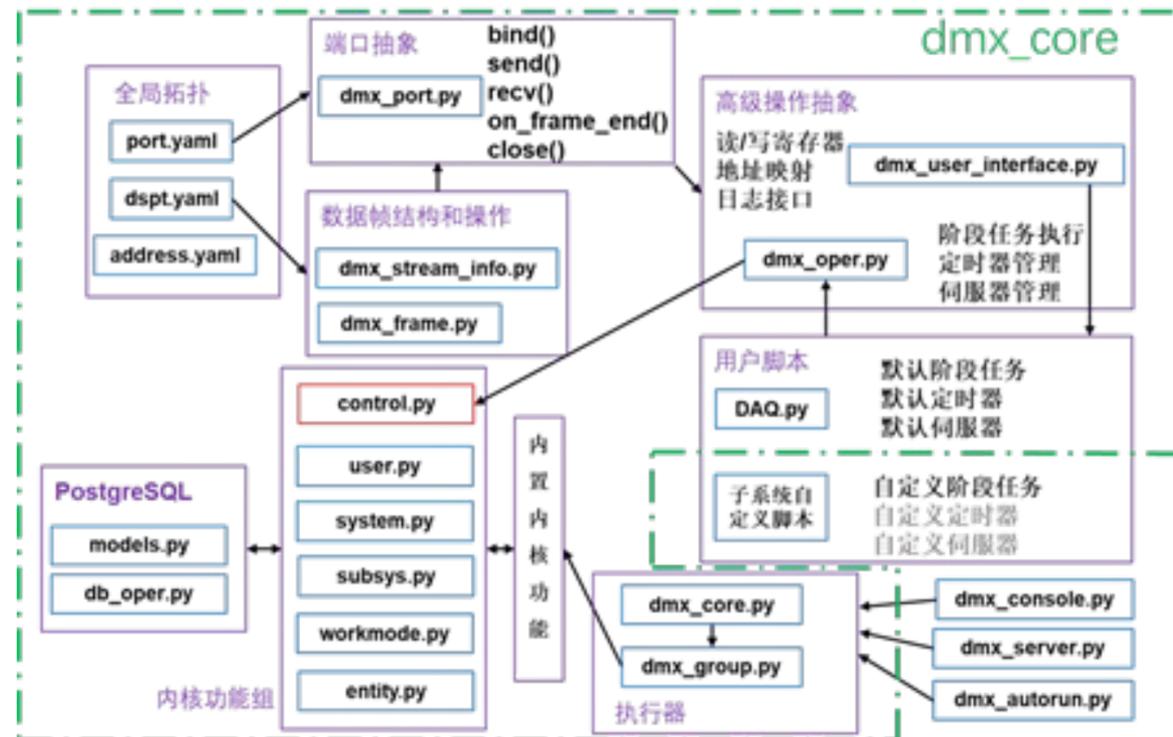


# Global Trigger Study

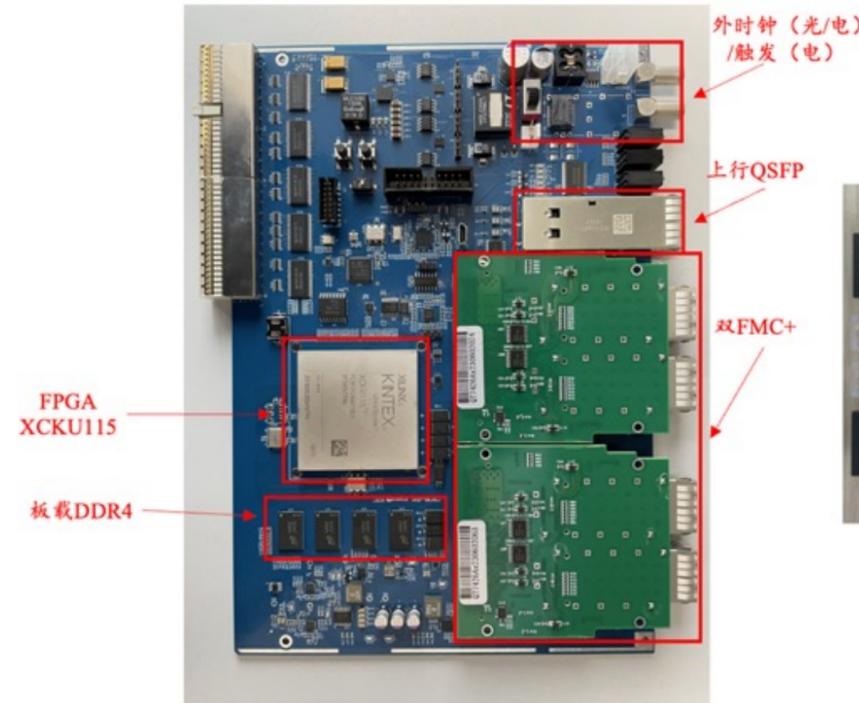
Trigger channel	Physics signal	Energy point	No. of tracks should( is ) matched	No. of matched tracks in Endcap	No. of matched tracks in Barrel	Signal trigger rate	Background trigger rate(kHz)	Signal trigger rate
<b>Charged Channels</b>	$e^+e^- \rightarrow \pi^+\pi^- J\psi; J\psi \rightarrow e^+e^-$	4.26GeV	3550 (2811)	448 (93)	3102 (2718)	949/952 ( $\geq 3$ )		99.7%
	$e^+e^- \rightarrow \pi^+\pi^- J\psi; J\psi \rightarrow \mu^+\mu^-$	4.26GeV	3518 (2765)	452 (122)	3066 (2643)	944/948 ( $\geq 3$ )		99.6%
	$e^+e^- \rightarrow \tau^+ \tau^-$	4.26GeV	1717 (1448)	186 (54)	1531 (1394)	867/879 ( $\geq 2$ )		98.6%
	$e^+e^- \rightarrow \pi^+\pi^- J\psi; J\psi \rightarrow \Lambda \bar{\Lambda}$	3.097GeV	2550 (1917)	220 (67)	2330 (1850)	905/918 ( $\geq 3$ )		98.6%
	$e^+e^- \rightarrow \pi^+\pi^- J\psi; J\psi \rightarrow \Xi^+ \Xi^-$	3.097GeV	2713 (2067)	198 (66)	2515 (2031)	912/922 ( $\geq 5$ )	21.3	98.9%
	$e^+e^- \rightarrow K^+K^- J\psi; J\psi \rightarrow l^+l^-$	4.682GeV	3515 (2641)	365 (90)	3150 (2551)	954/964 ( $\geq 3$ )		99.0%
	$e^+e^- \rightarrow D_0 \bar{D}_0$	3.773GeV	3387 (2644)	312 (73)	3075 (2571)	954/954 ( $\geq 3$ )		100%
	$e^+e^- \rightarrow D^+ D^-$	3.773GeV	4031 (2707)	274 (64)	2640 (2643)	979/983 ( $\geq 3$ )		99.6%
$e^+e^- \rightarrow D_s^+ D_s^-$	4.04GeV	4770 (3312)	462 (98)	4308 (3214)	933/936 ( $\geq 5$ )		99.7%	
<b>Neutral Channels</b>	$J/\psi \rightarrow \text{gam invisible}$	3.097GeV	-	-	-	542/546 ( $\geq 1 \& \& \text{gam\_momentum} \geq 1$ )		99.7%
	$e^+e^- \rightarrow n \bar{n}$	3.097GeV	-	-	-	538/564 ( $\geq 2 \& \& N_{\text{bar}} \geq 1 \& \& E_{\text{Dep}} \geq 0.4$ )	67.0	95.4%
	$e^+e^- \rightarrow \text{gam } n \bar{n}$	3.097GeV	-	-	-	611/613 ( $\geq 2 \& \& N_{\text{bar}} \geq 1 \& \& E_{\text{Dep}} \geq 1$ )		99.7%
	$e^+e^- \rightarrow \text{gam } n \bar{n}(\text{ISR})$	3.713GeV	-	-	-	550/555 ( $\geq 2 \& \& N_{\text{bar}} \geq 1 \& \& E_{\text{Dep}} \geq 0.7$ )		99.1%

# DAQ Software Design and Hardware Development

- Software and firmware architecture based on Data-Matrix: flow processing, hetero-computing, standard interfaces and protocols, global pipeline
- Development of core electronics boards: CROB-PXI, CROB-PCIe, FMCP optical interface board



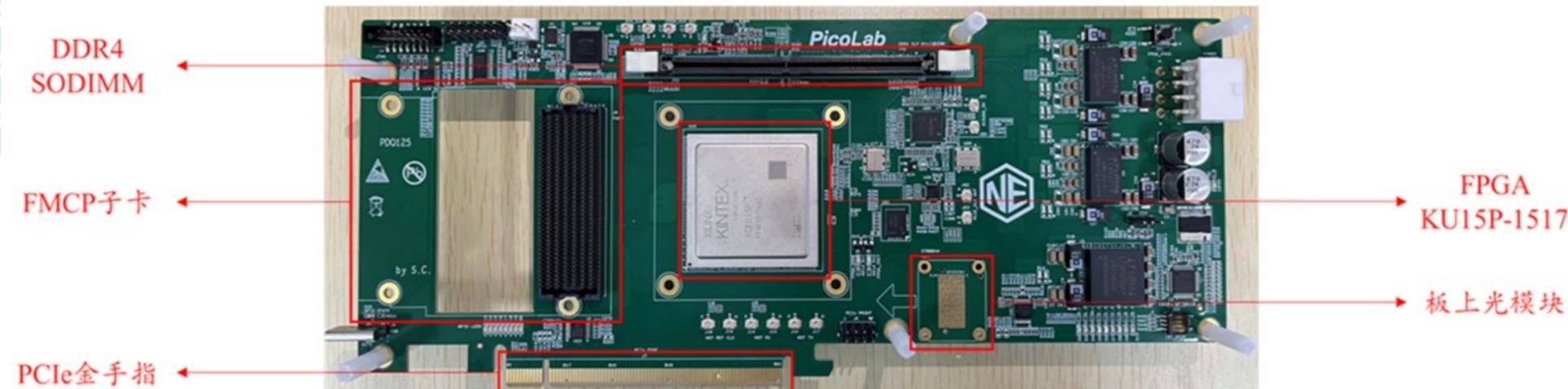
CROB-PXI board



FMCP optical interface board

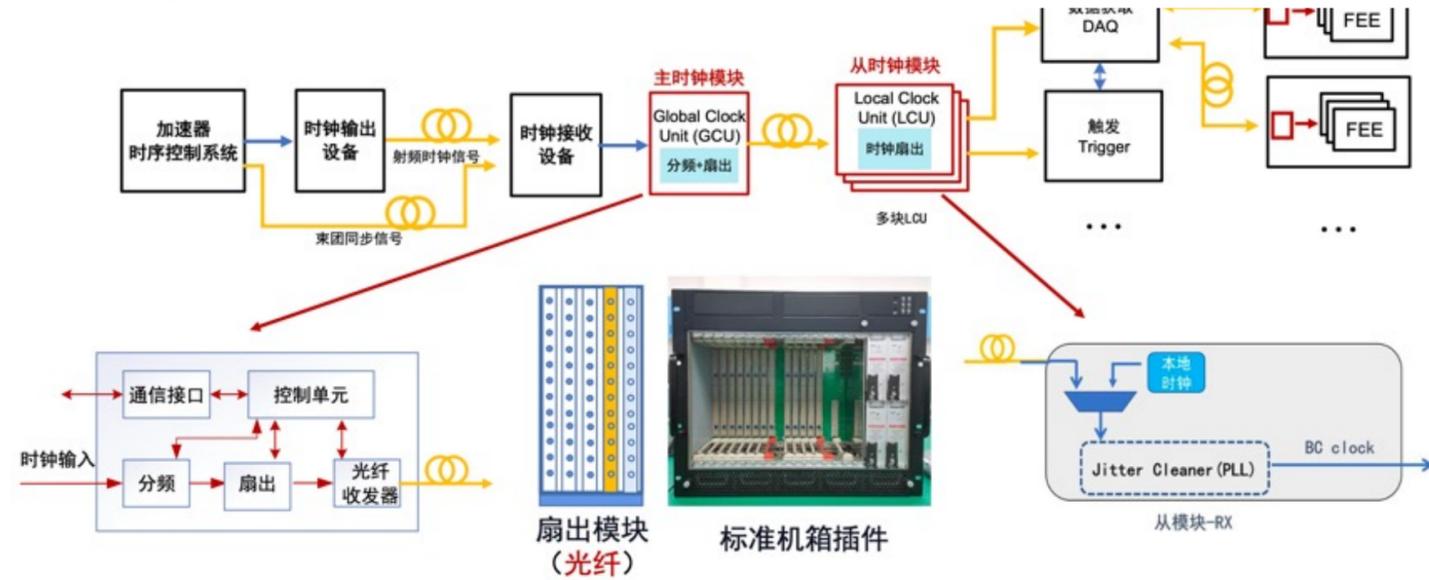


CROB-PCIe board

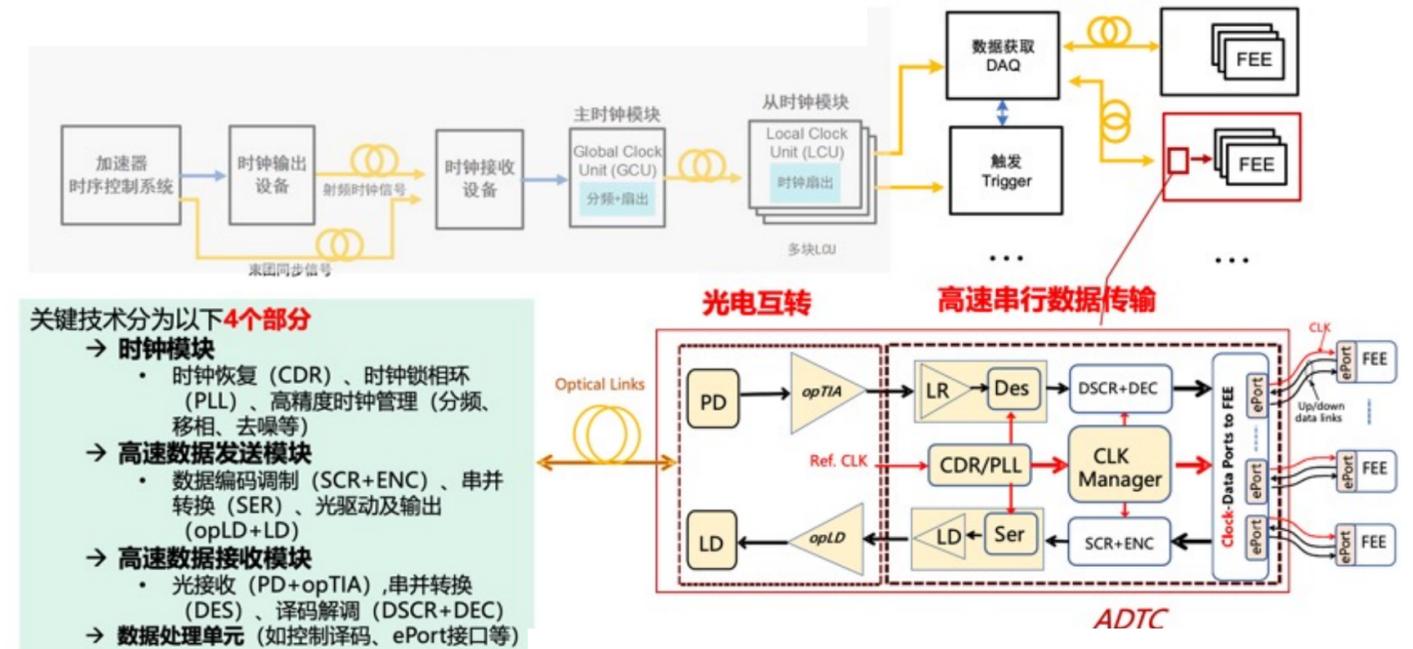


# Clock and Data Transmission

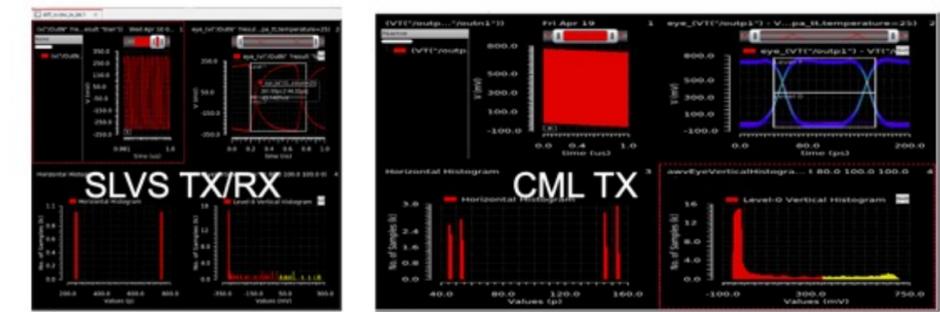
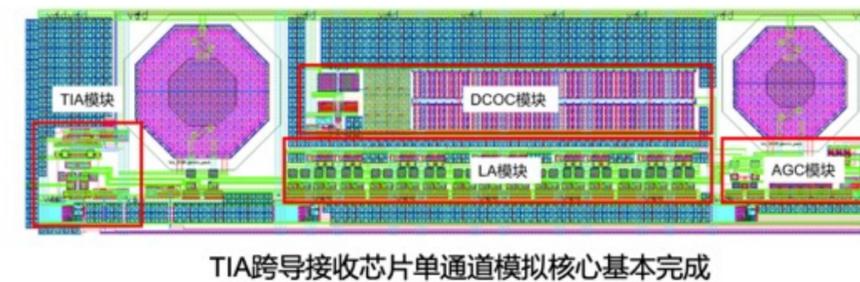
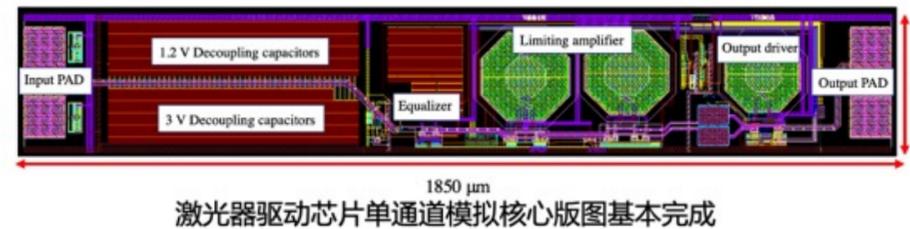
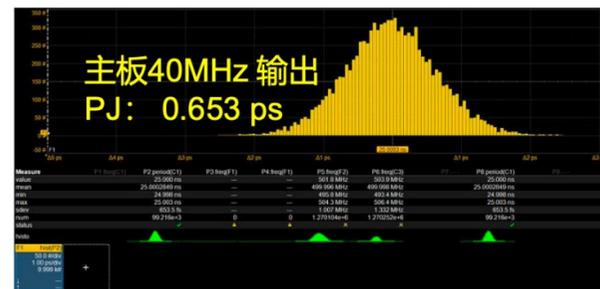
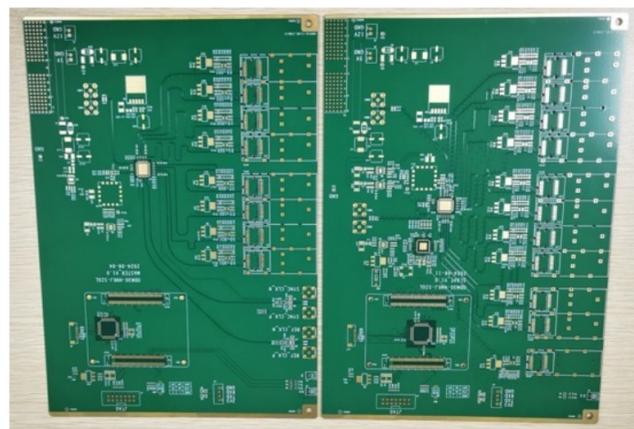
- Master-slave clock distribution scheme : ~ 5ps



- High-speed data transmission : ~ 5Gpbs



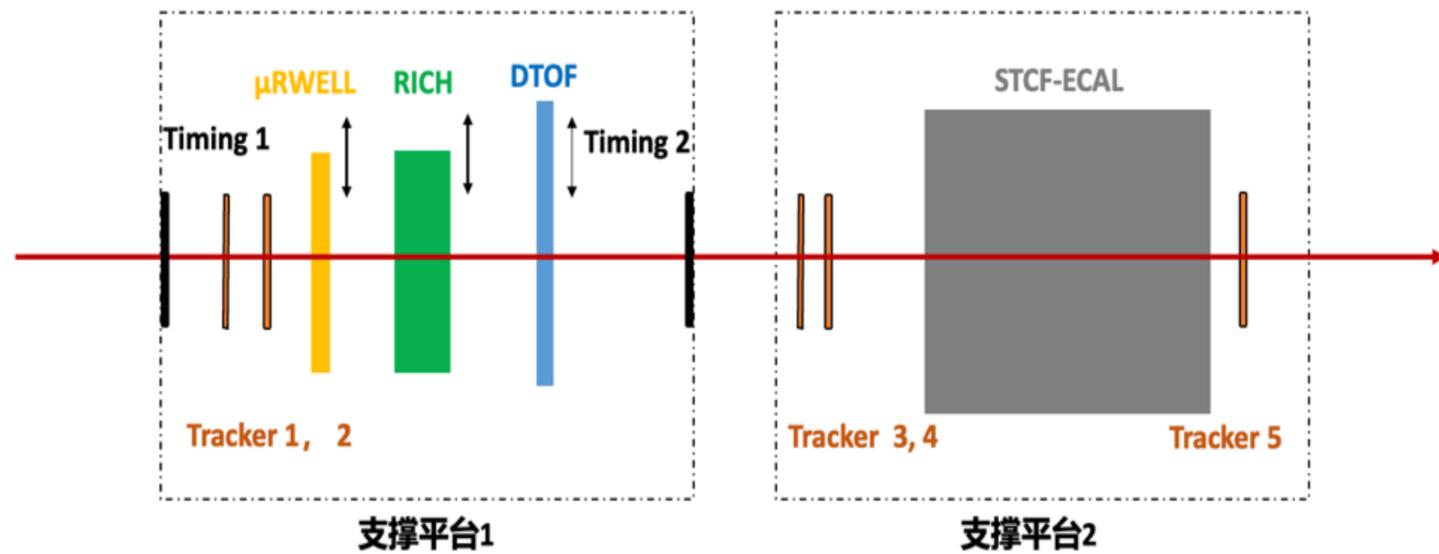
ADTC, an analogue of GBTx



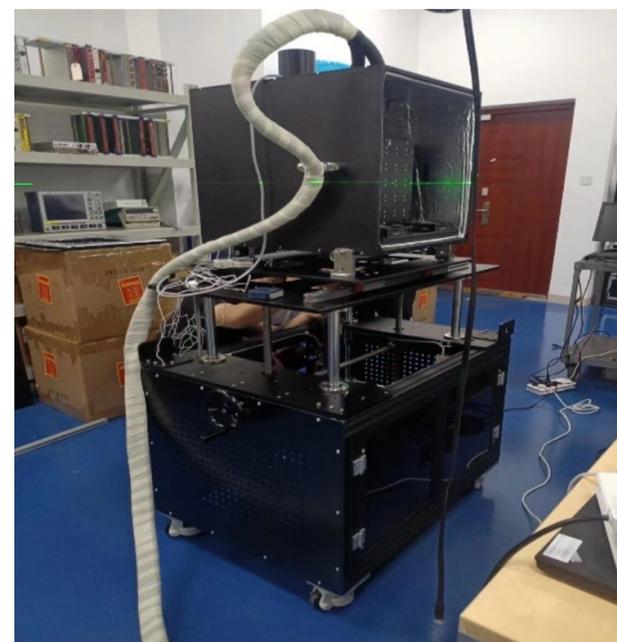
Clock management block and SerDes block taped out

# Combined Beam Test

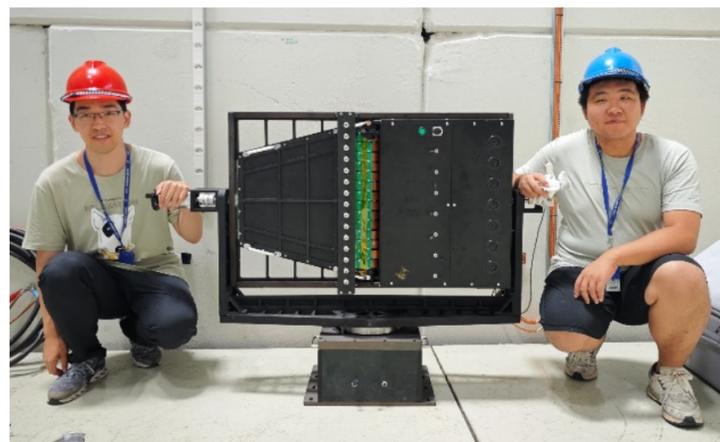
A test beam campaign for a combined system (DTOF, EMC, DAQ)



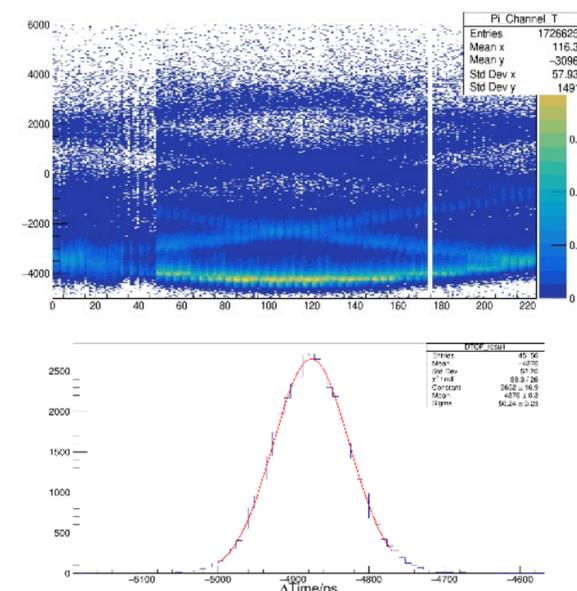
EMC Prototype



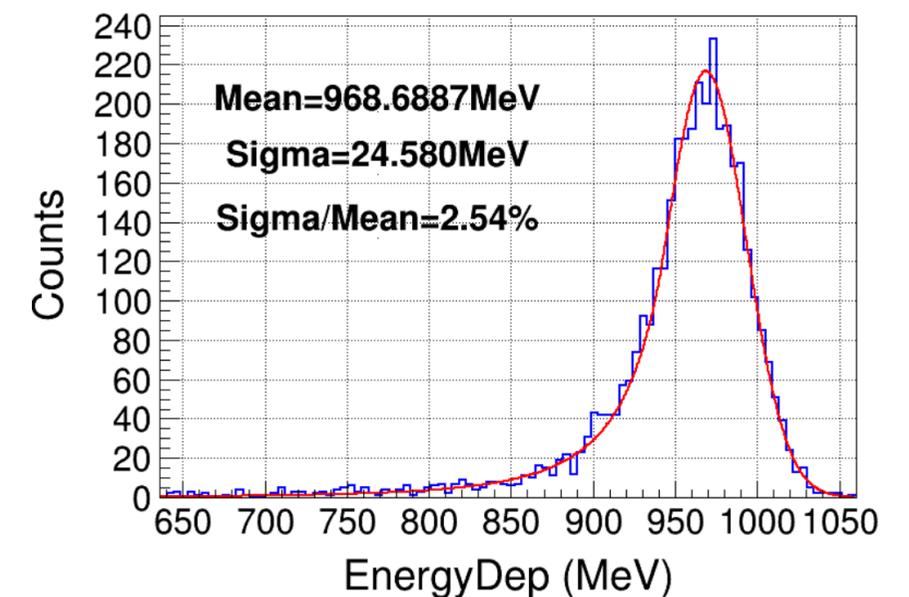
DTOF Prototype



DTOF:  $\sigma_t \sim 25$  ps

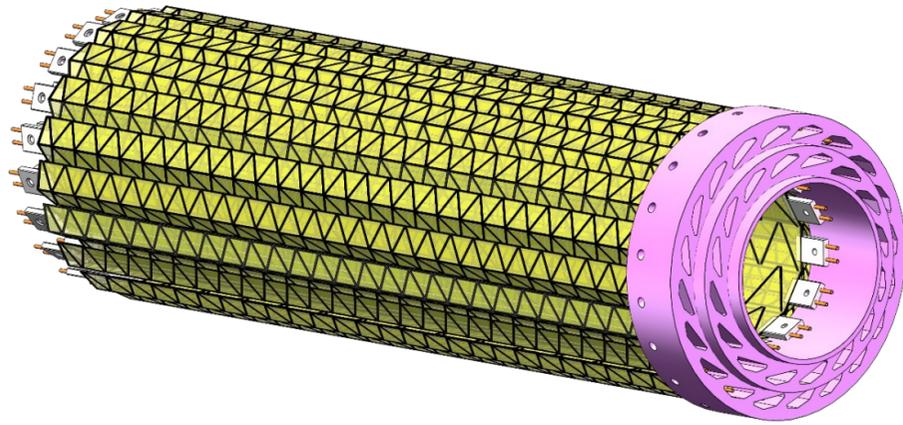


EMC:  $\sigma_E/E \sim 2.5\%$

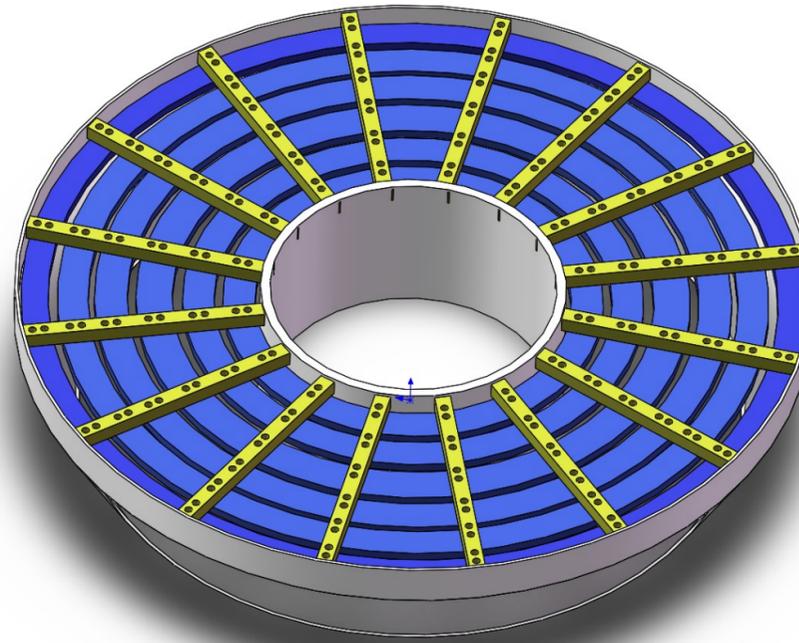


# Detector Mechanical Design

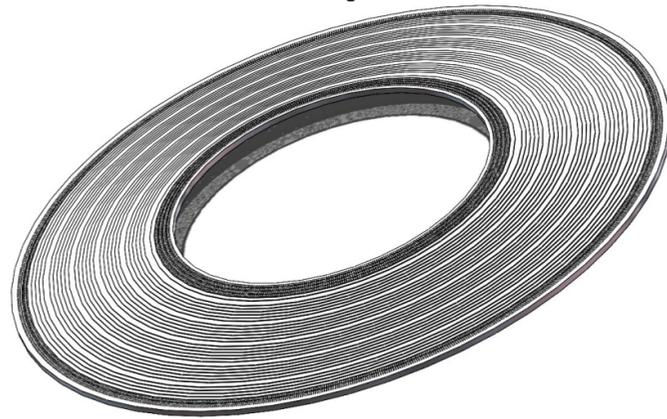
ITK-MAPS



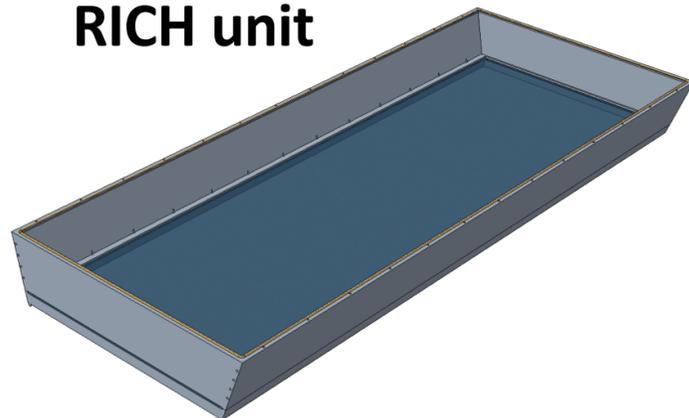
ECAL Endcap



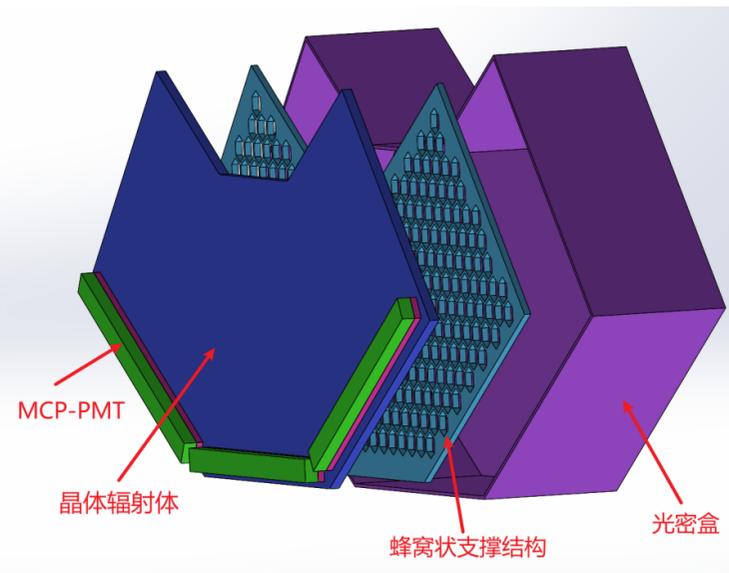
MDC end-plate



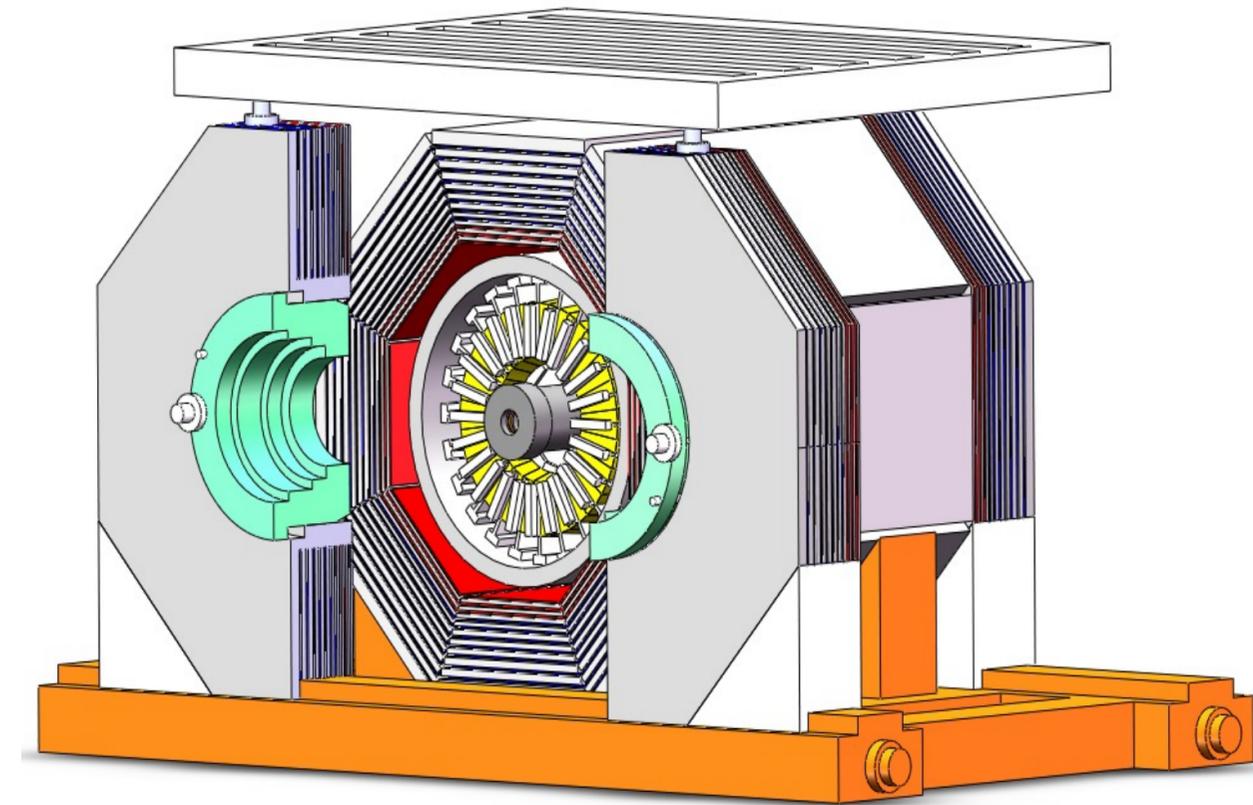
RICH unit



DTOF sector



General structure



# Summary

- **STCF detector conceptual design studies in the past few years have culminated with the publication of the physics and detector CDR.**
- **The STCF project has moved on to the technology R&D stage with strong support from local governments and USTC. A full STCF R&D program has been established and is rapidly moving forward.**
- **Intense R&D activities are underway on the baseline detector concept targeting key technologies of all sub-detectors. Significant progress has been made and some systems have reached milestones.**
- **Some sub-systems not covered in this talk: detector magnet, detector control system, luminosity monitors ...**
- **A lot of synergy with other projects to explore**

**Please join us if you are interested**  
**Still a lot of room to contribute and play an important role**

**Thank you !**