2024年第四届半导体辐射探测器研讨会 @ 青岛

半导体辐射探测器前端读出电子学前沿技术及发展趋势

Frontier Technologies and Trends of Front-end Readout Electronics for Semiconductor Radiation Detectors

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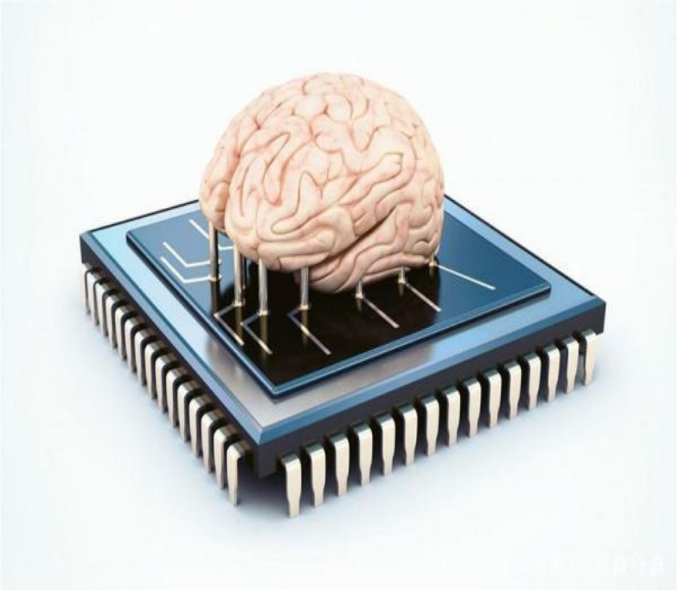
Northwestern Polytechnical University

May 24th, 2024

Outline

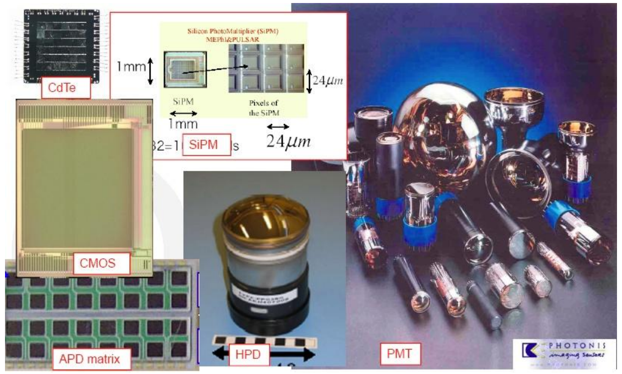


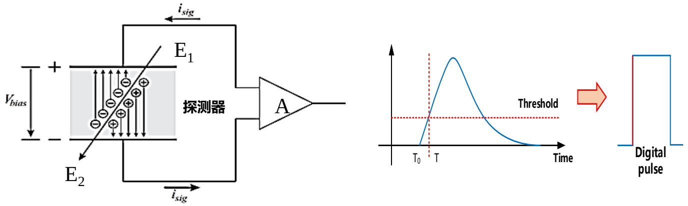
Research Background

1 Semiconductor Radiation Detectors

"Eyes" of Radiation Instrumentation

- Charged particles (h^+, e^-, α, β, Heavy ions), neutrons, photons (X, γ-rays)
- Features → Continuous pulse signals, random in time and amplitude

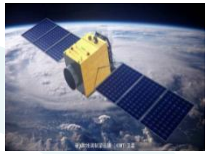




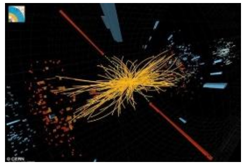
$$Q_E = \frac{E_{dep}}{\varepsilon_x} = \frac{E_1 - E_2}{\varepsilon_x} \propto \Delta V_{step}$$

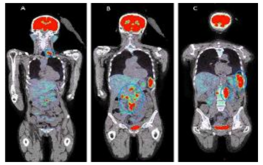
HEP Experiments

Synchrotron radiation



Astronomical telescope





Security Screening

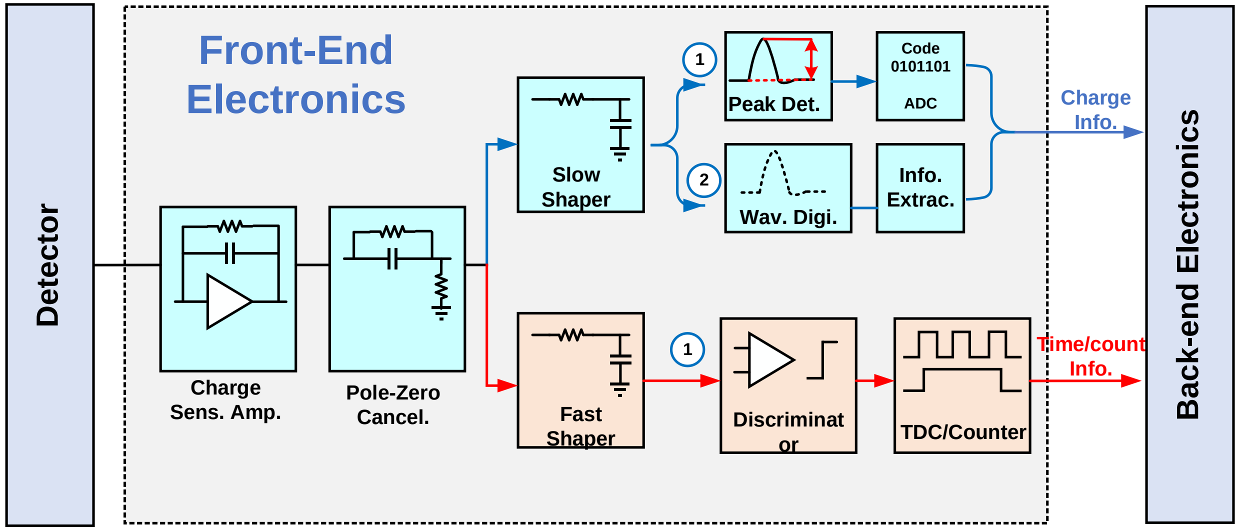
Industrial CT

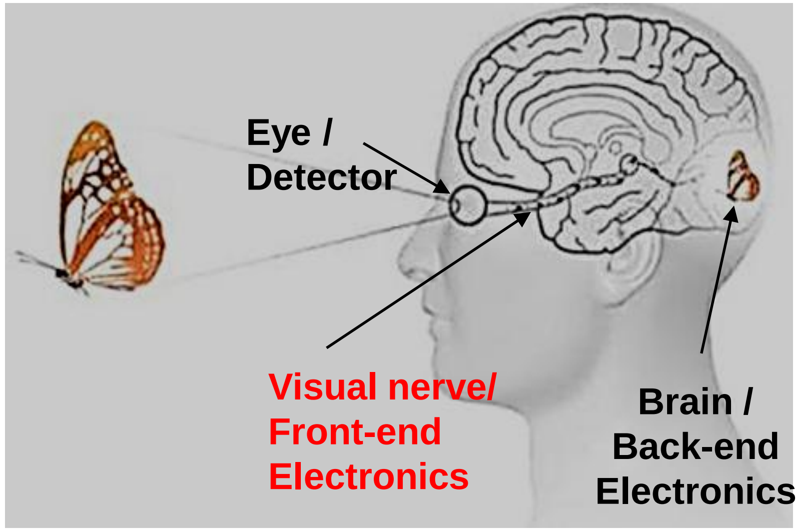
Biomedical Imaging

1 Front-End Electronics

Discrete Circuits & Application-Specific Integrated Circuits (ASICs)

- Signal Modulation: Readout, Charge & Time Measurement, Photon counting
- Digitization: for future processing by computers
- Performance bottle-neck of the detector system





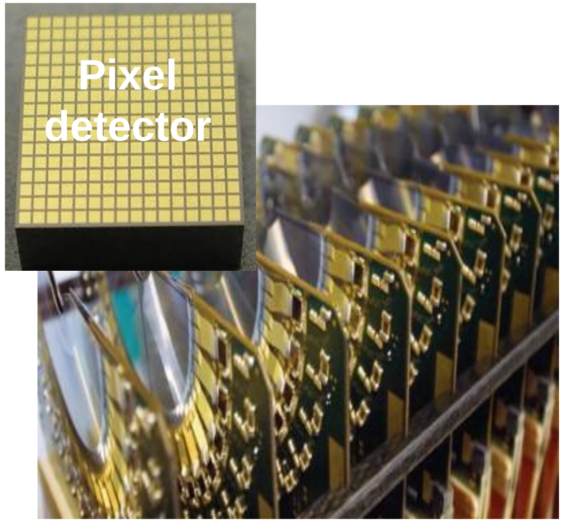
(After L. Zhao, 2023)

Common solution and frontier technologies →
Employing ASICs to construct front-end electronics

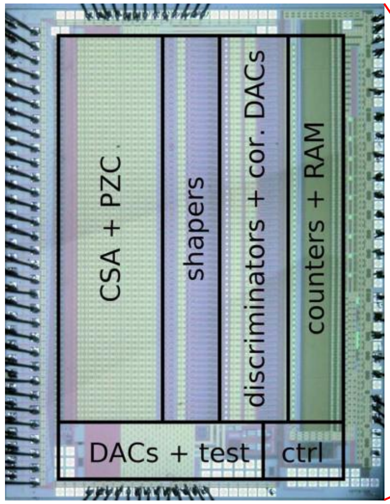
❶ Physical Implementation

☐ Multichannel Readout ASICs

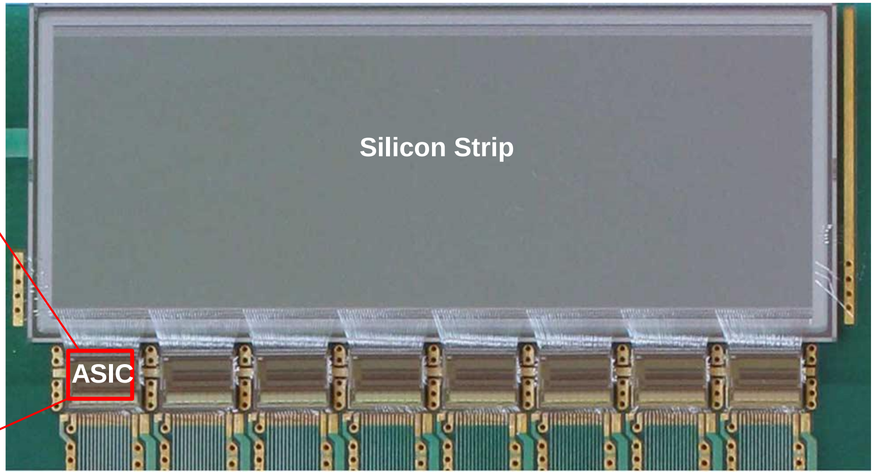
- **Main Blocks**: Charge-Sensitive Amplifier, Pulse Shaper, Discriminator, Peak Detector, ADC/TDC, Counter, Shift Registers
- **Feature**: "Big Analog, Small Digital" (大A小D)



Multichannel electronics



Strip ASIC（64/128/160）



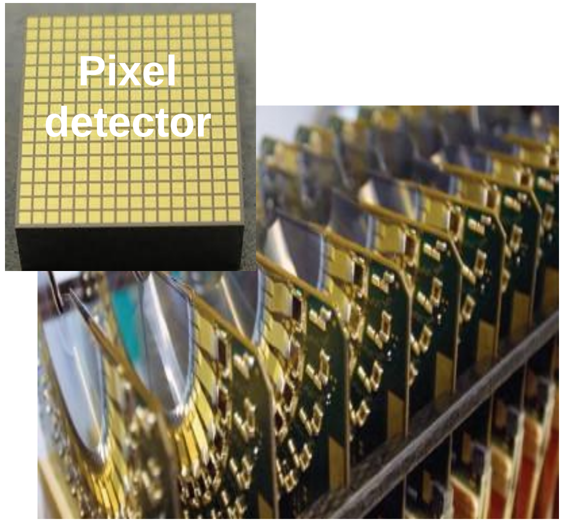
Si Strip Detector module

(R. Szczygiel, AGH Univ. of S&T, Poland, TNS, 2009)

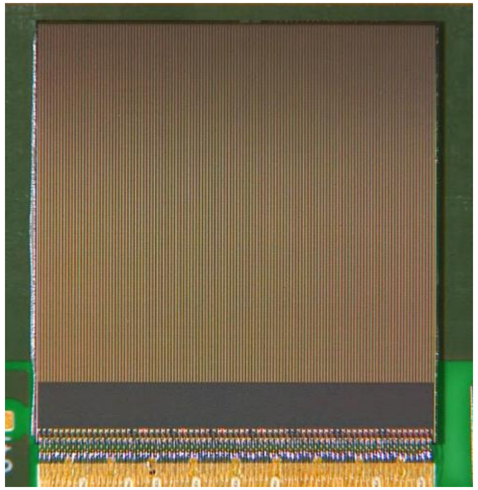
1 Physical Implementation

Pixel Readout ASICs

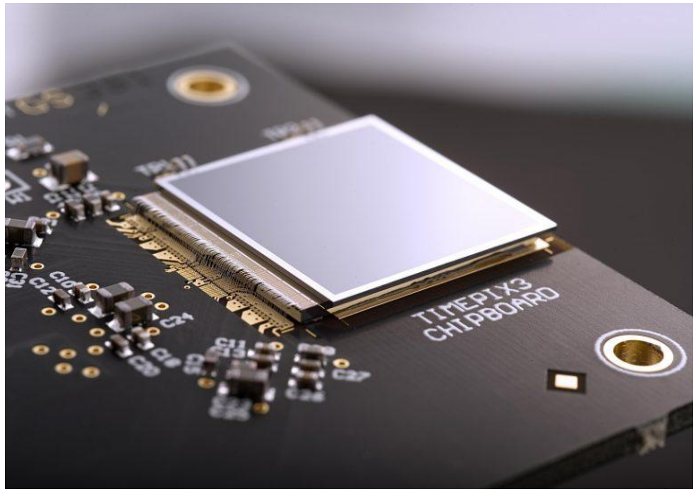
- **Main blocks**: Pixel AFE, Pixel ADC/Counter, Readout Matrix, PISO Registers, Serializer, PLL and Global Controller
- **Feature**: "**A**nalog Islands in **D**igital Sea" （数字海、模拟岛）



Multichannel electronics



Pixel ASIC (50μm pitch，256×256)



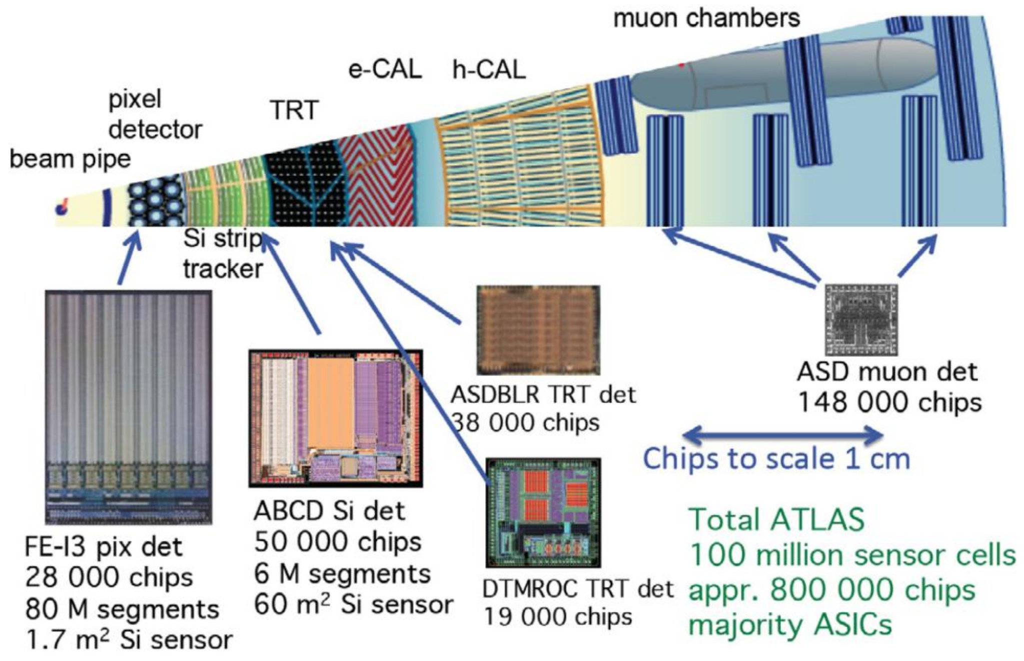
Hybrid Pixel Detector

(https://home.cern/)

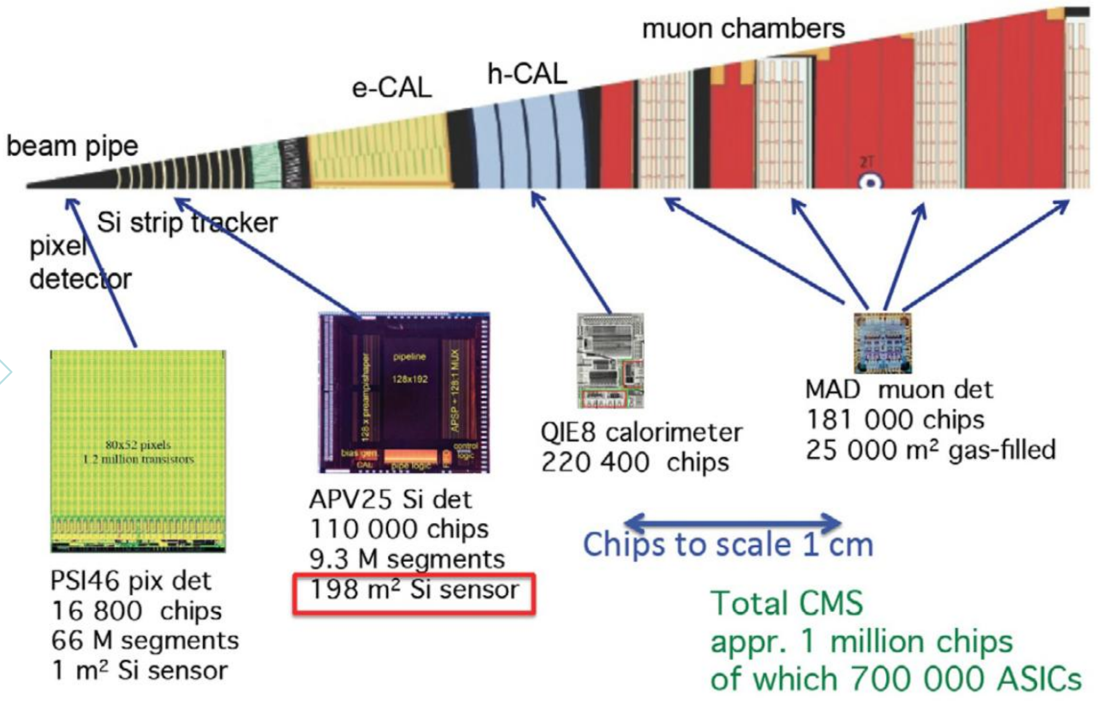
1 Application Example

ASICs for High-Energy Physics Collider

- Illustrate the radial positions of different systems in the LHC ATLAS/CMS
- Different types，Different performance，the amount of chip up to 0.8 million



ATLAS detector

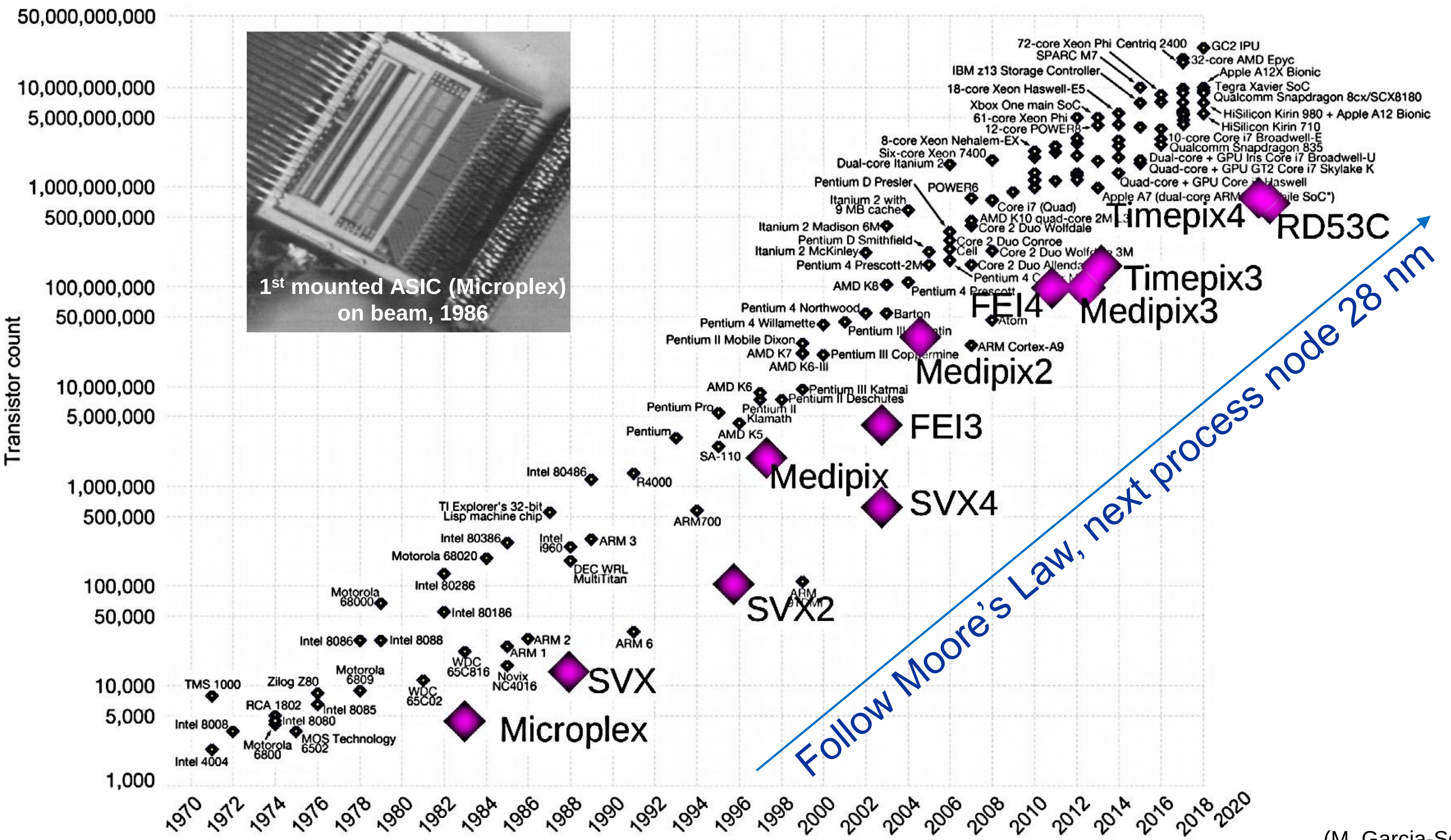


CMS detector

(E. H.M. Heijne, CERN, NIMA, 2023)

❶ Application Example

☐ Tracker ASICs Versus Commercial Electronic Chips

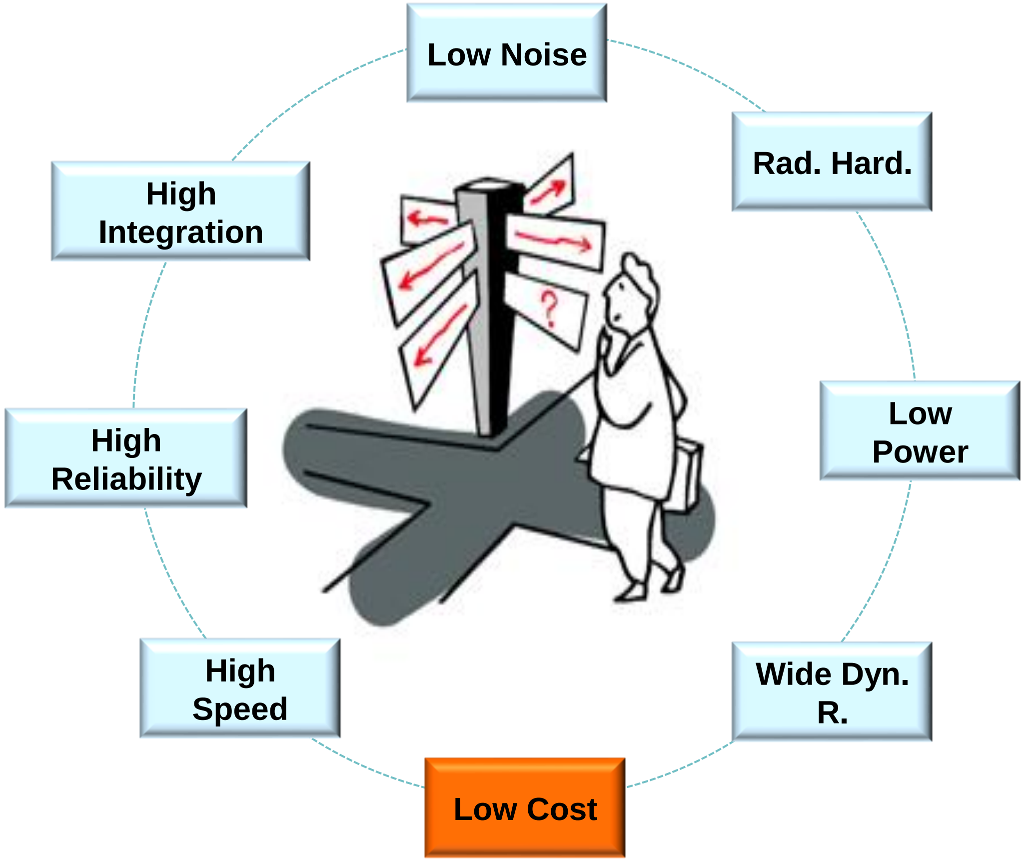


(M. Garcia-Sciveres, NIMA, 2024)

R&D Challenges

Complex Design Considerations

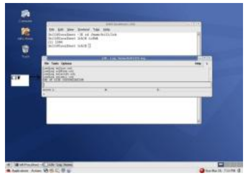
- Performance Matching
  - Dynamic Range
  - Noise Performance
  - Linearity
  - Shaping Time/Count Rate
  - ADC resolution
  - Time precision
  - Consistency
  - Power dissipation
- Physical Connection
  - Package/COB/flip chip/TSV
- Reliability
  - Rad. Hard., Low temp., Life
- Yield & Cost

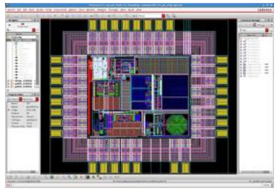


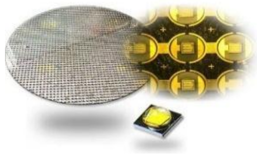
1$/channel?

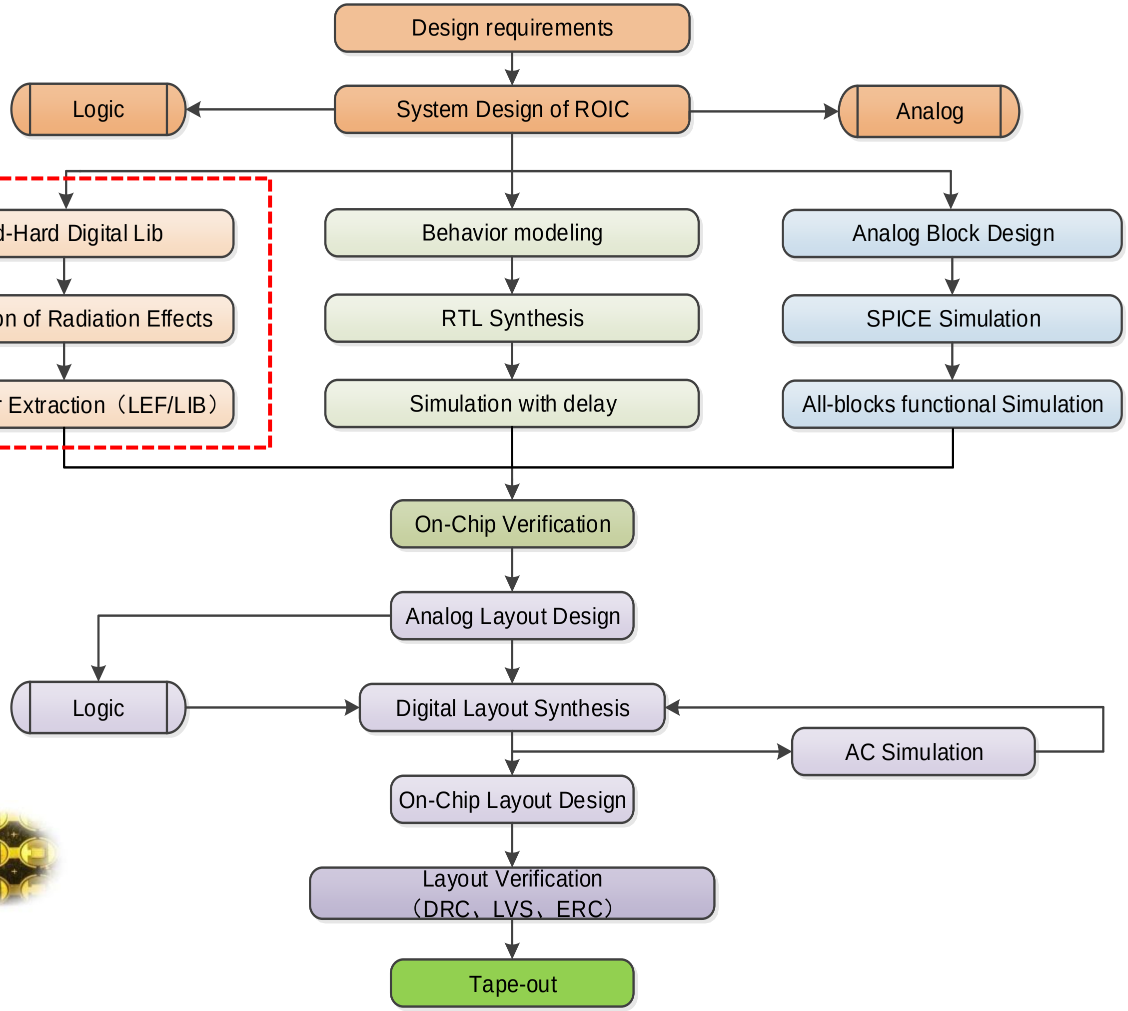
1 R&D Challenges

☐ Multiple iterations → 4~6 years/product









System Design
1~2 months

Circuit Design
3~4 months

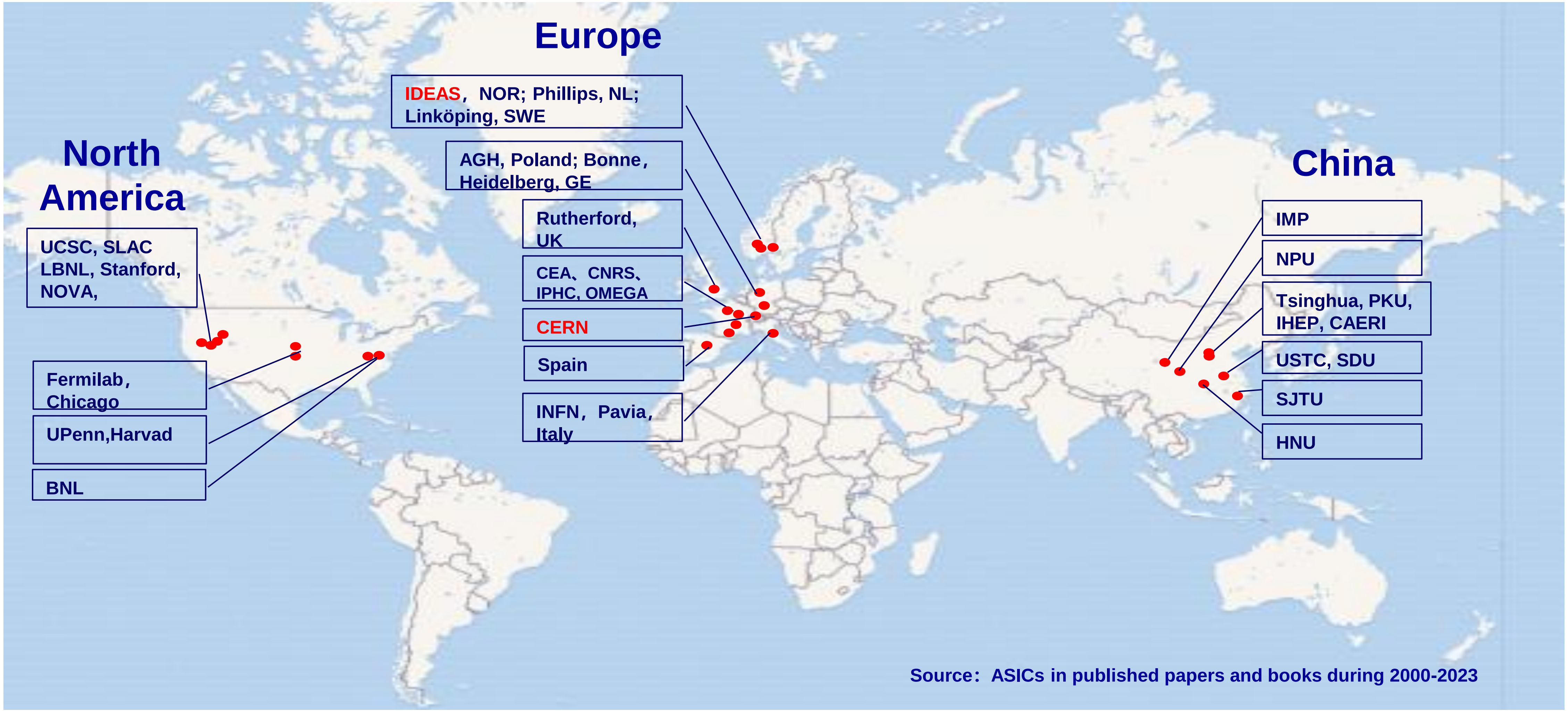
Layout Design
3~4 months

Fabrication & Testing
2~3 months

Front-End Readout ASICs: A Survey

② Research Institutions

☐ Distribution of ASIC Designers



2 Classification

Development of Front-End ASICs in the last 20 years

P-I-N
- Preamp.
- Shaping amp.
- ADC/TDC

Strip
- Multi-ch. ROIC
- Multi-ch. ADC/TDC

Pixel
- Multi-ch. ROIC
- Pixel ROIC

- Monolithic Active Pixel Sensor (MAPS)
- Si Sensor + ROIC, not ASIC

1. Low-Noise Energy-Res. ROICs
2. Large Dyn. Rang. ROICs
3. Low-Noise Phot. Count ROICs
4. Analog Pixel ROICs
5. Digital Pixel ROICs

Charge Measurement

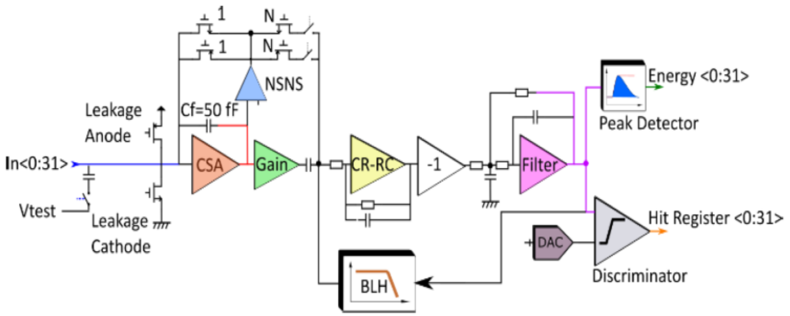
Time Measurement

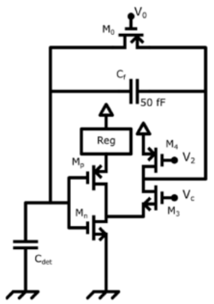
Photon Count Measurement

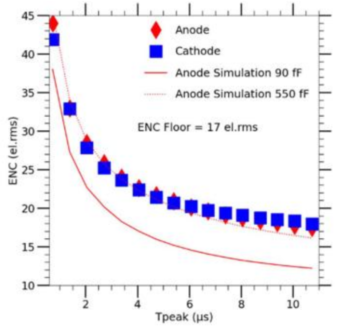
② State-of-the-art Work

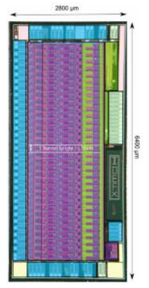
Type I: Low-Noise Energy-Resolving ROICs

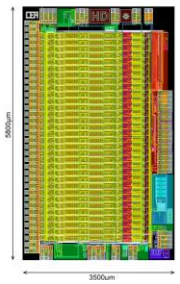
- Topology: CSA, PZC, CR-RC^n, PDH, BLH, DSC, DAC, Mux, TCON
- IDeF-X: 0.35 μm, 32 ch, ±40 fC, 17 e$^-$, 0.73 μs <τ_p< 10 μs, 100 kcps, 0.85 mW/ch
- Low-level threshold is ~ 1.2 keV @ Si Drift Detector, X-ray tube, -10 ℃

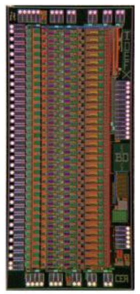




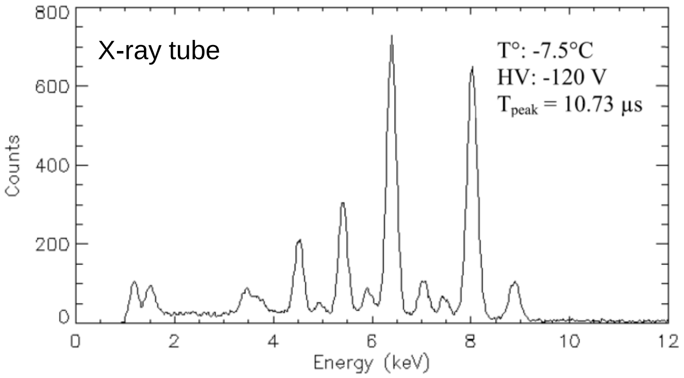


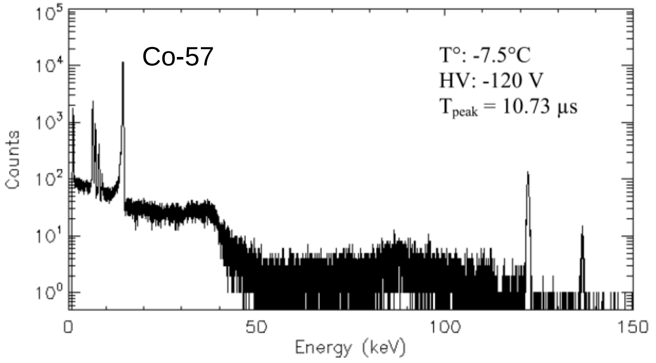

IDeF-X ECLAIRs, 2009


IDeF-X HD, 2010


IDeF-X BD, 2015


IDeF-X HDBD, 2022





(D. Baudin, IRFU/DEDIP, CEA, Université Paris-Saclay, TNS, 2022)

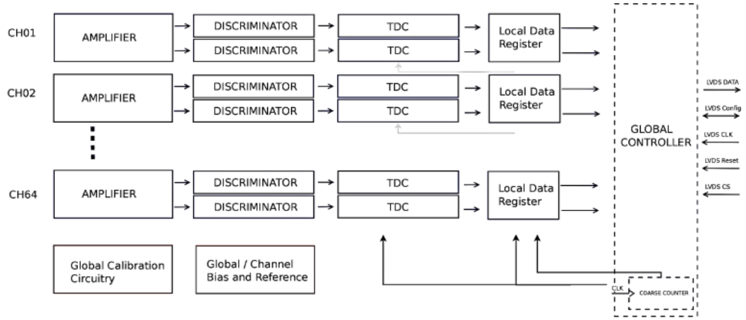
② State-of-the-art Work

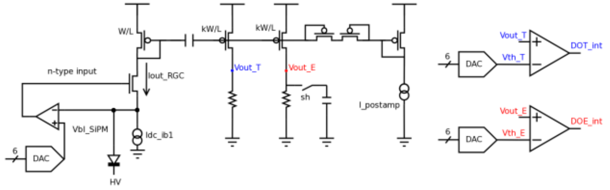
□ Type II: Large-Dynamic Range ROICs

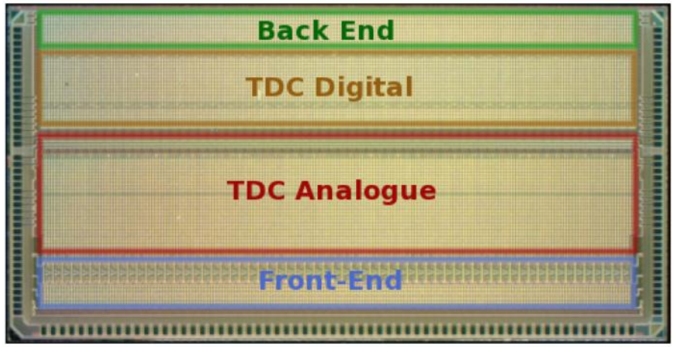
– **Topology: TIA, 2 DSC, TDC/TOT, Loc. Reg., Glb. TCON, LVDS**

– **TOFPET2: 110 nm CMOS, 64 ch, 1500 pC, 500 kcps, 10b ADC, 30-ps TDC, 3.2 Gbps, 8.2 mW/ch**

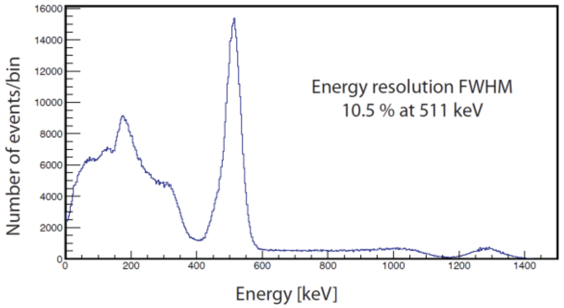
– **LYSO/SiPM → 10.5 % @ 511 keV Na-22, Coin. Time Res. 119 ps**

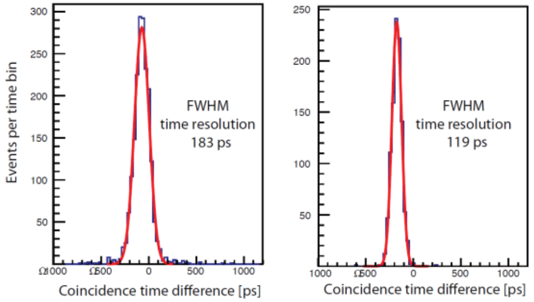






(M. D. Rolo,IFEP, Lispoa, Protigal, Jinst, 2013)

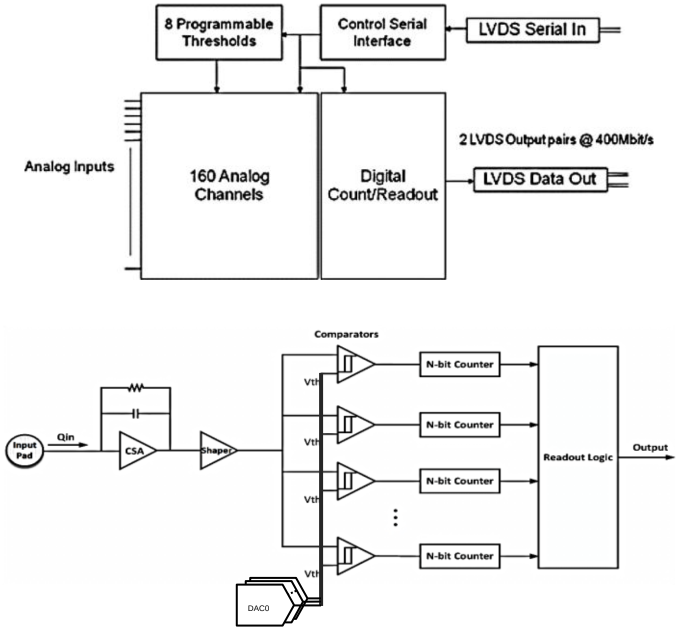




② State-of-the-art Work

☐ Type III: Low-Noise High-Rate Photon-Count ROICs

- Topology: CSA, PZC, CR-RC^n, 8 DSC, 8 Counters, Readout, LVDS
- 180 nm CMOS, 160 ch, 214 e-, 10 ns $<\tau_p<$ 40 ns, 17 Mcps, 4.2 mW/ch → 8 energy bin with 8b counters for strip detector



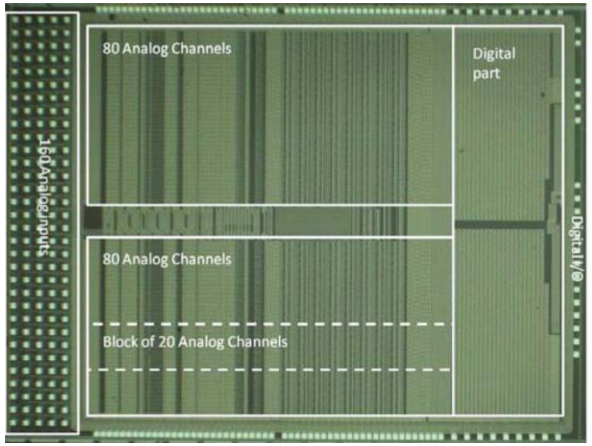


TABLE II
ASIC OVERVIEW

	Target/Simulation	Measured
Number of channels	160	
Gain	2.08mV/keV	2.10mV/keV
Noise level, ENC	300 electrons @5pF	214 electrons @~5pF
Number of energy bins	8	
Counter resolution	8b	
Peak times	10ns, 20ns, 40ns	10ns, 20ns, **40ns**
Maximum count rate	17Mcps @100MHz	17Mcps@100MHz
Maximum frame rate	37kframe/s @100MHz	
Process	180nm CMOS	180nm CMOS
Clock frequency	100MHz, 200MHz	100MHz
Power consumption	800mW @200MHz	670mW @100MHz
Chip area	5mm x 6.6mm	

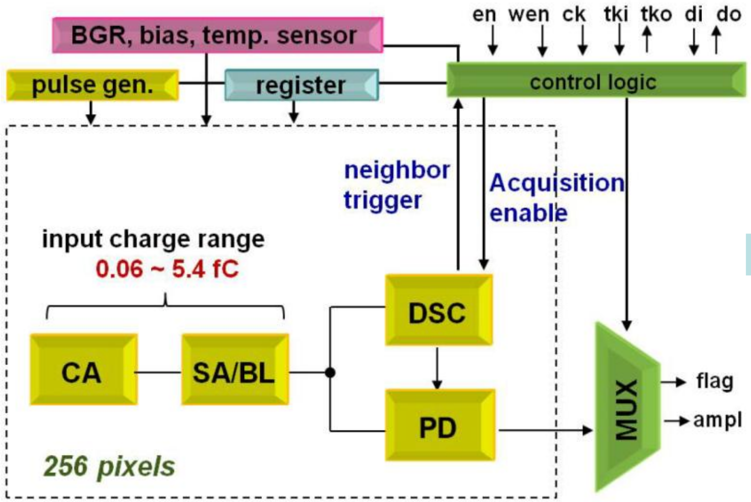
(M. Gustavsson, Linköping University, Sweden, TNS, 2012)

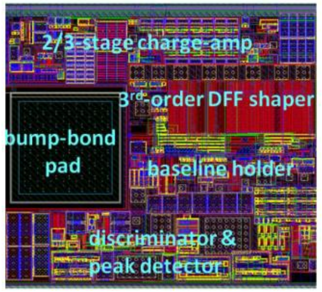
State-of-the-art Work

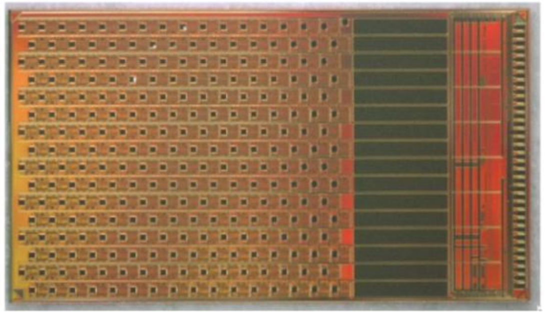
Type IV: Analog Pixel ROICs

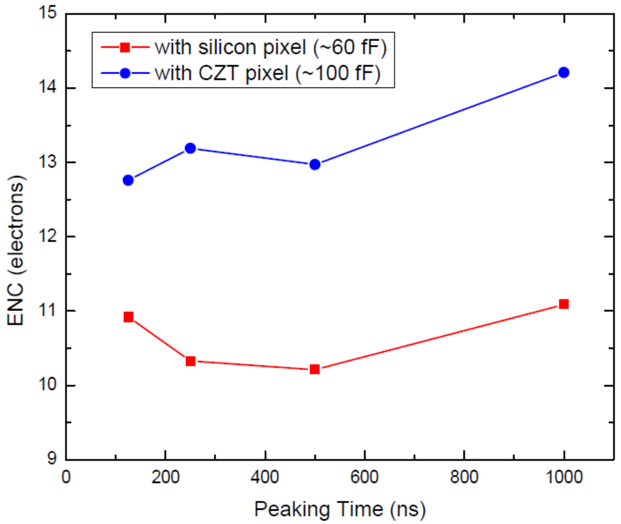
– Topology: Pixel AFE(CSA+SP+BL+DSC+PDH) , Mux, Reg., Global TCON, BGR, Bias, Temp. Sensor

– HEXID2: 130nm CMOS, 250×250 μm^2, 16×16, 0.06 ~ 5.4 fC, 10 ~15 e$^-$, 0.125 μs <τ_p< 1 μs, 0.6 mW/pix → Si/CZT pixel detector for space X-ray imaging







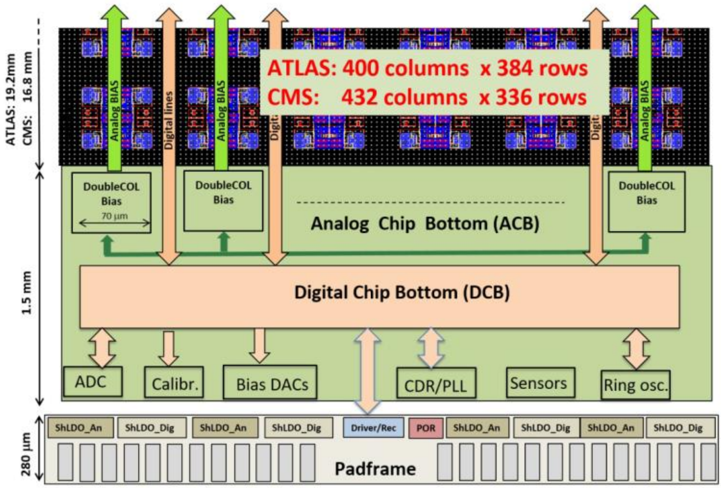


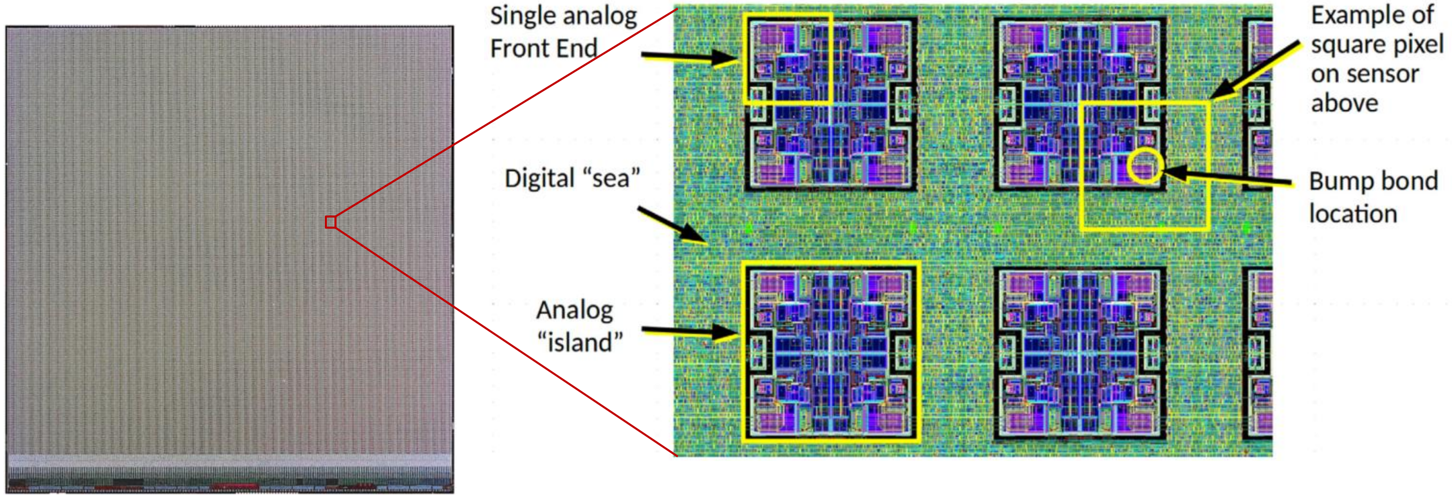
(S. Li, BNL, USA, 2017)

❷ State-of-the-art Work

◻ Type V: Digital Pixel ROICs

- Topology: Pixel AFE(CSA+SP+BL+DSC), Pixel ADC/Counter, Readout Matrix, PISO Registers, Serializer, PLL and Global Controller
- RD53C: 65 nm CMOS, 50 × 50 μm^2, 400×384, ±40 fC, 600 e$^-$, 3 GHz/cm^2, 10 μW/pixel, 500 Mrad
- Others: FE-I4, TDCPix, Velopix, Medipix4, Timepix4, MPA, ClicPix

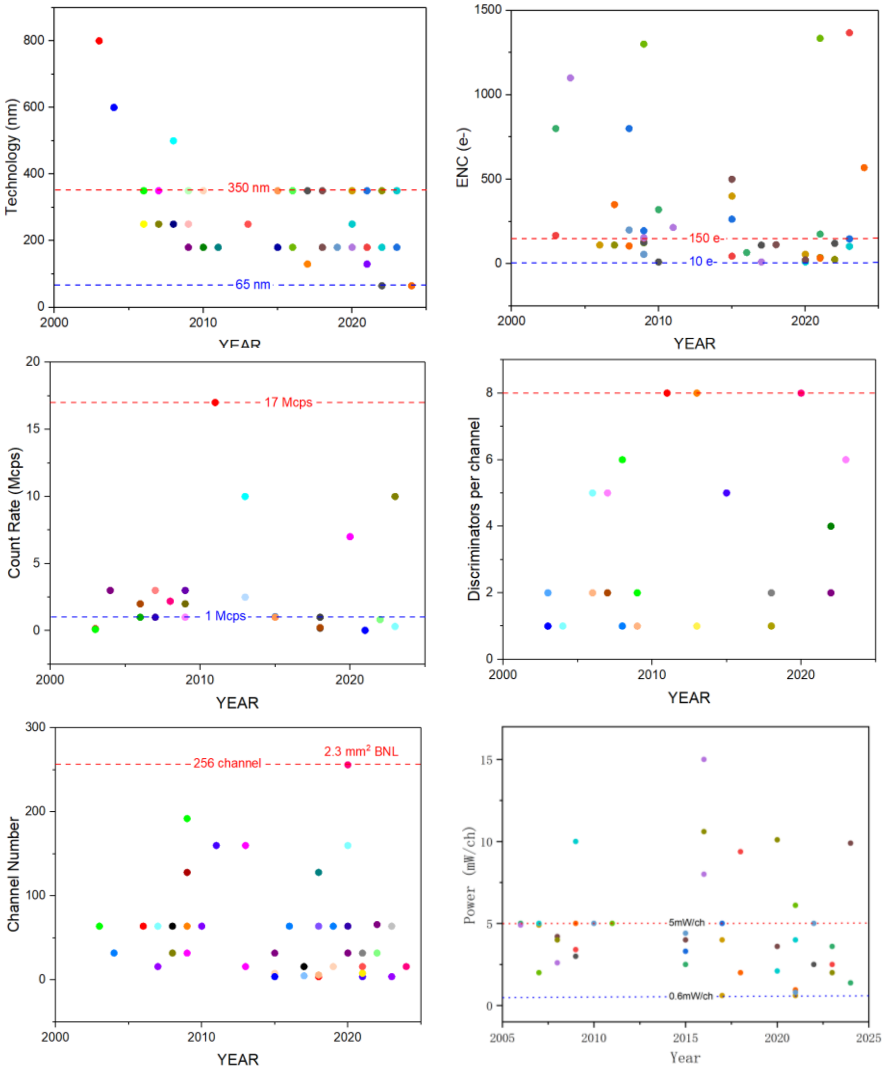




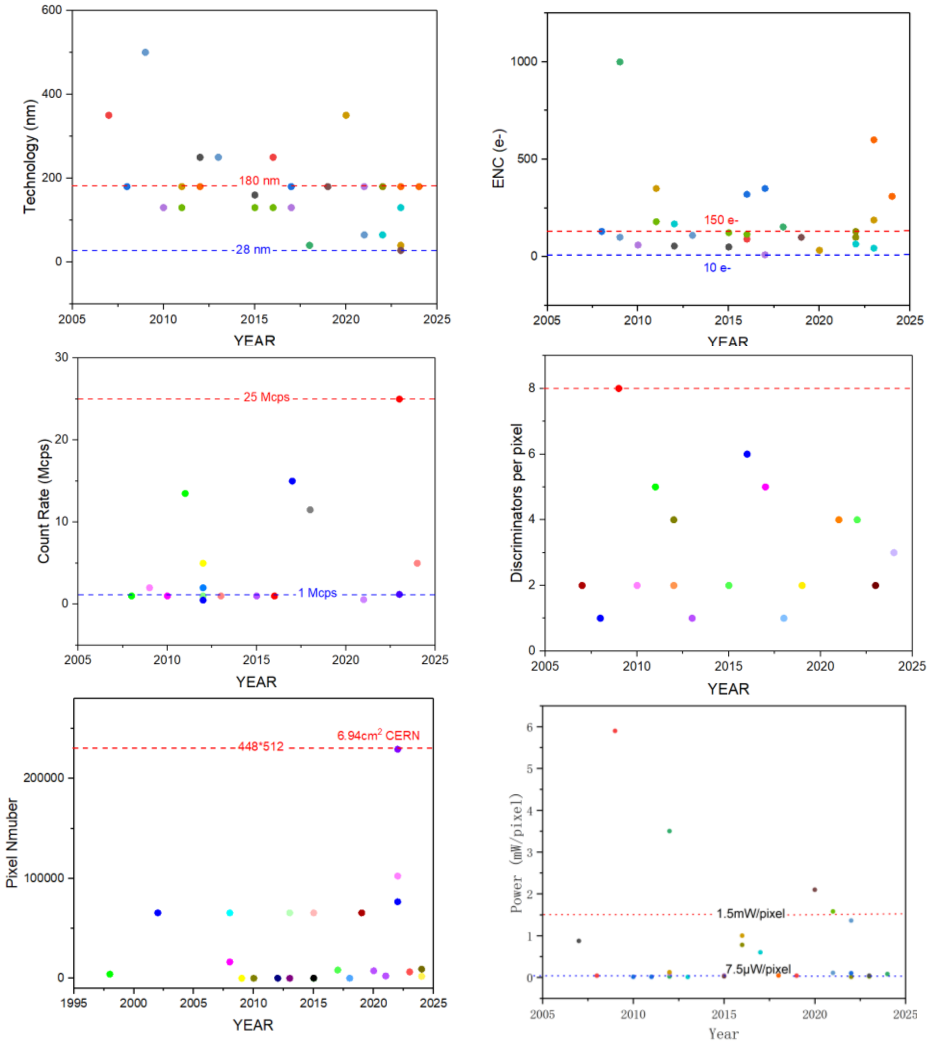
(G.-S., Maurice, LBNL, USA, 2024)

② Performance Overview

Multichannel ROICs



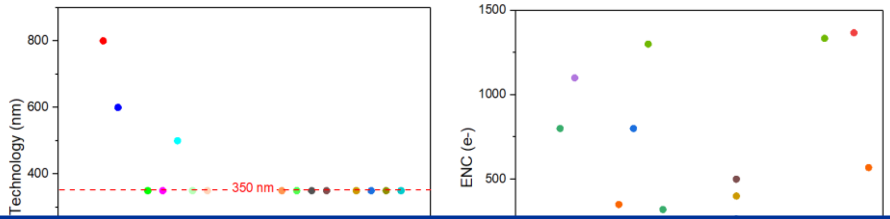
Pixel ROICs



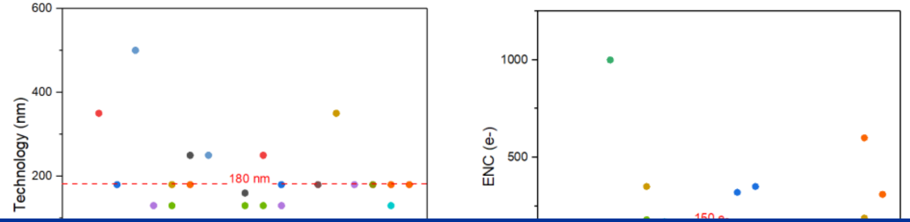
(Source：ASICs in published papers and books during 2000-2023)

2 Performance Overview

Multichannel ROICs

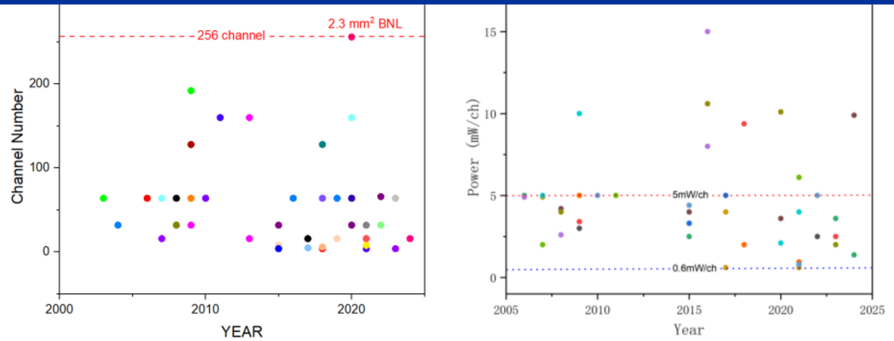


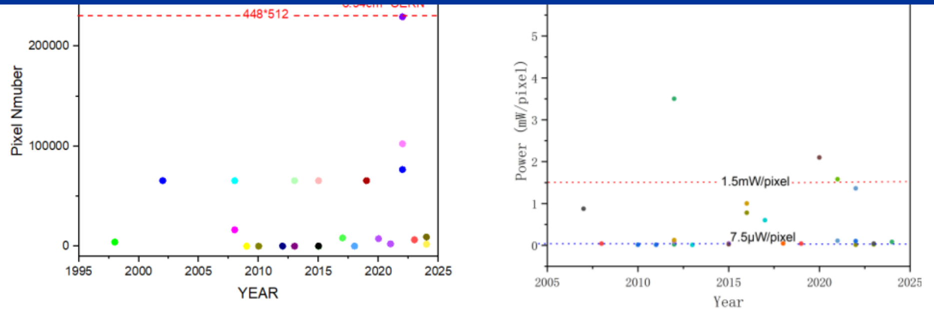
Pixel ROICs



Conclusion

- **Main Electrical Characteristics**
  - **Fabrication Process（nm）: 350 →250 → 180→ 130→ 65 → 40 → 28 (Adv. 65 Vs. 28)**
  - **Equivalent Noise Charge（e-）: < 150 (Mini. ENC 10 Vs. 10)**
  - **Count Rate (Mcps): 0.5→1→2 → 3 → 5 → 10 →17 →25 （Max. 17 Vs. 25)**
  - **Discriminators per channel/pixel: 1→2→4 → 5 → 6 → 8 (Max. 8 Vs. 8)**
  - **Channel/Pixel Number: Continuously increasing (Max. 256 Vs. 448×512)**
  - **Power Dissipation（μW/ch）: 7.5 ~ 5000（Mini. 600 Vs. 7.5)**



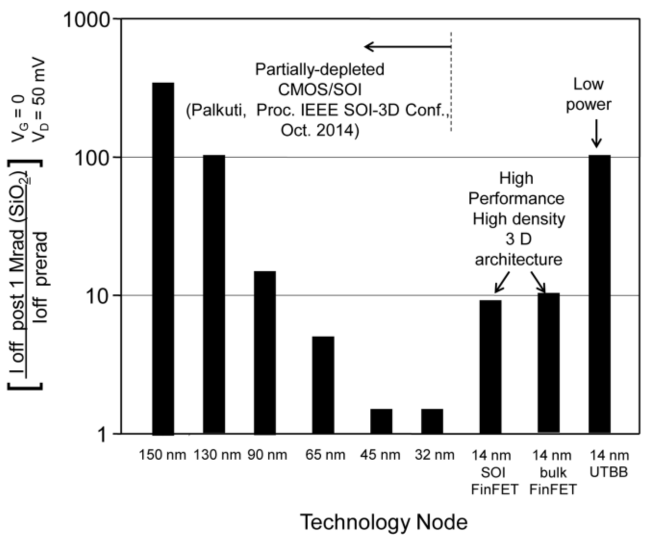


(Source: ASICs in published papers and books during 2000-2023)

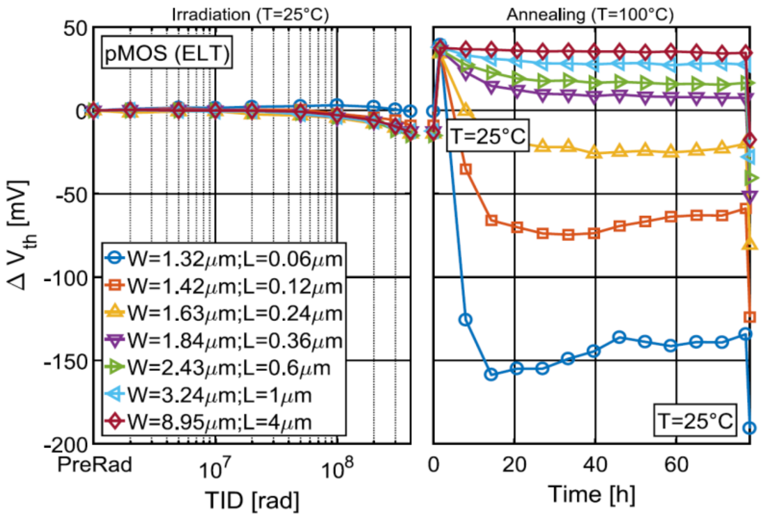
② Performance Overview

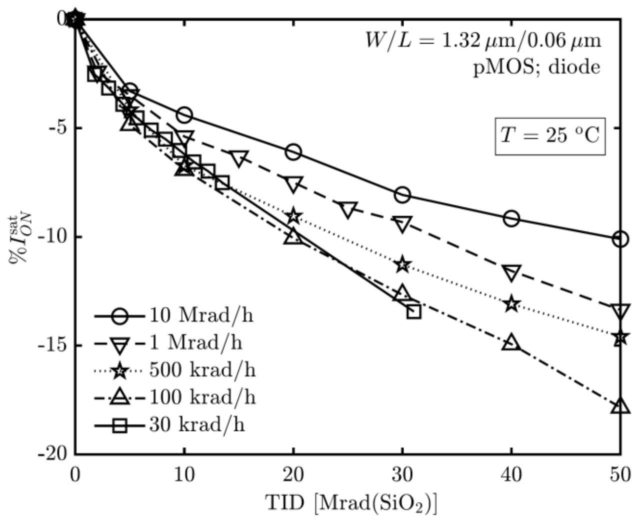
□ Total ionization dose (TID)

- $I_{D,off}$ reduced with the shrink of process nodes, but worse for 14-nm FinFETs
- 65 nm CMOS: ELT shown tiny $I_{D,off}$ and ΔV_{th},@ 100 Mrad but $I_{D,sat,\ on}$ affected by dose rate effects
- Medipix/Timepix Family → 800 Mrad



(Hughes,2015)



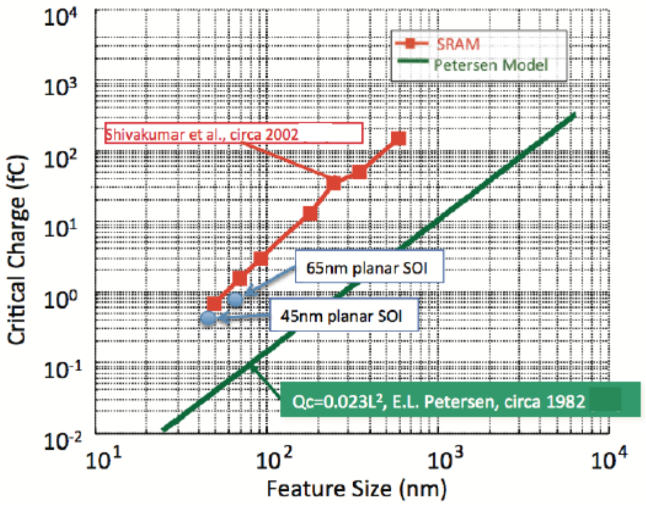


(F. Faccio, CERN, NIM A, 2023)

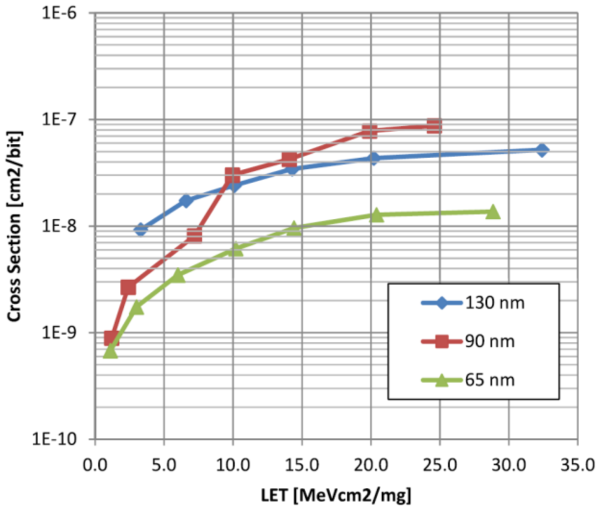
2 Performance Overview

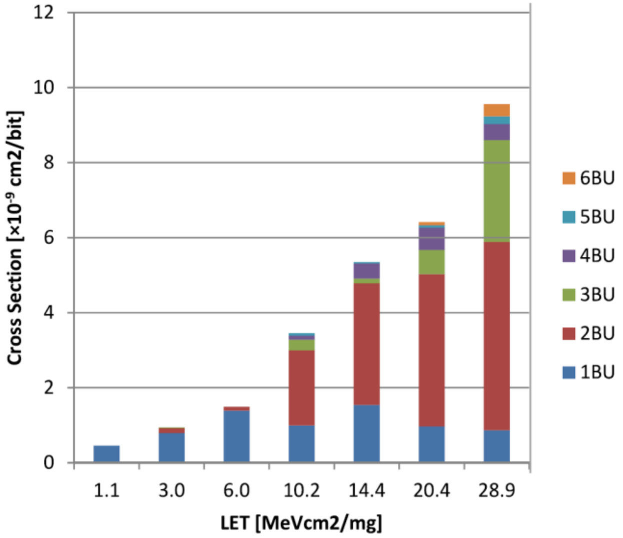
☐ Single Event Effects (SEE)

- Critical charge < **1 fC** @ sub-100 nm nodes → lower LET_{th} → **Multi-bit upset (MBU)**
- Triple-Mode Redundancy, Time Redundancy, EDAC → LET_{th} > **75 MeVcm²/mg**
- SEL immunity → LET_{th} > **100 MeVcm²/mg**



（Massengill，2012）





（F. Faccio, CERN, NIM A, 2023）

② Performance Overview

☐ Technical Trends

– Overseas: 28 nm, larger ch./matrix, 10 e-(rms), 25 Mcps, ~μW/ch, 800 Mrad
– Domestic: all types involving, less applications

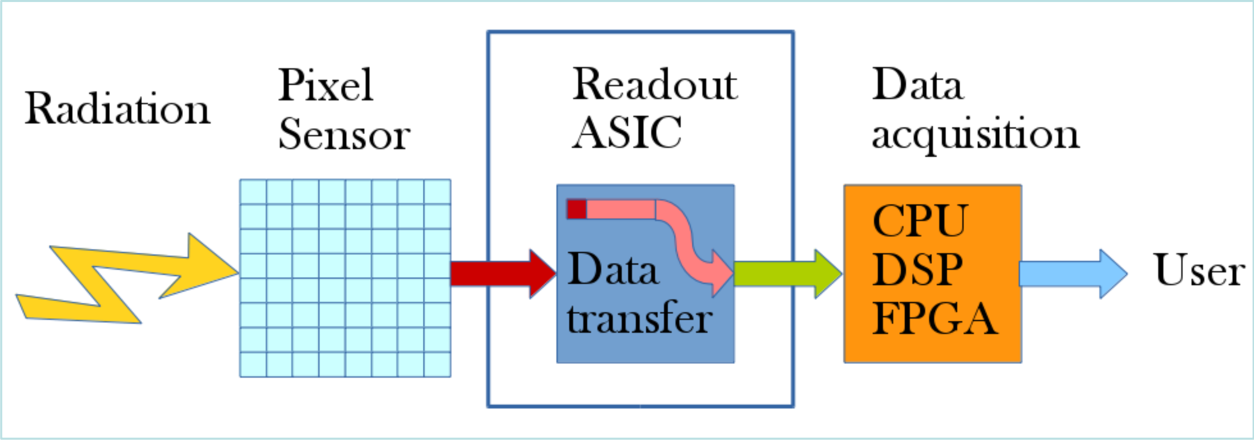
Parameter	Overseas		Domestic	
	Multichannel	Pixel	Multichannel	Pixel
Process (min)	65 nm	28 nm	65 nm	65 nm
Channel No. (max)	256	448×512	64/128	400×512
ENC (min)	10 e^-	10 e^-	25 e^-	100 e^-
Discr. No. (max)	8	8	8	3
Count Depth (max)	24 bits	24 bits	16 bits	24 bits
Count R.（max）	17 Mcps	25 Mcps	10 Mcps	5 Mcps
Power Diss.（min）	600 μW/ch	7.5 μW/pixel	600 μW/ch	38.9 μW/pixel
Radiation hardness	TID > 800 Mrad(Si) SEU LET_{th} > 75 $MeVcm^2/mg$ SEL LET_{th} > 100 $MeVcm^2/mg$		TID > 30 Mrad(Si) SEU LET_{th} > 75 $MeVcm^2/mg$ SEL LET_{th} > 100 $MeVcm^2/mg$	

Intelligent Front-end Processors

3 Requirements

Next-generation Instrumentation

- High-luminosity Collider, Energy-resolving photon-counting CT, X-ray Astronomy
- higher precision detectors（MAPS & HPD)
- ROIC： 50 µm pitch， 448 × 512 (Timepix4, 200 PB, 4.8 Gbps)
- New challenges
  - The rapid increasing amount of data
  - Traditional methods are inefficient

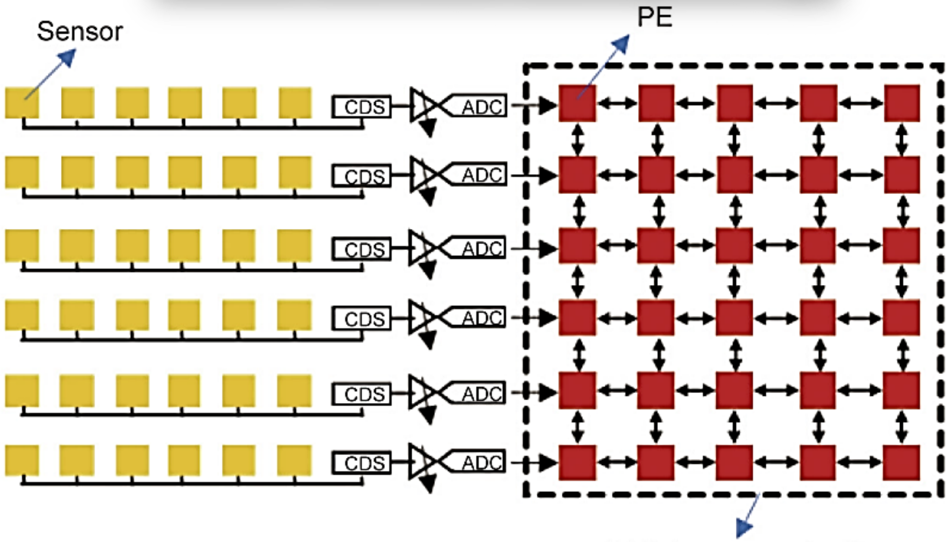


③ Issues and Solution of Current Electronics

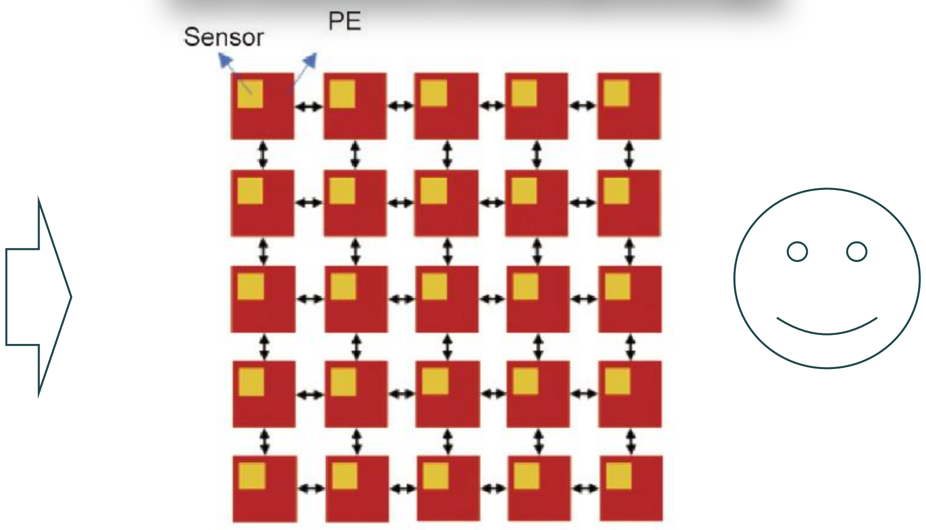
- **Non-idea effects of Sensing**
  - Compton scattering, charge sharing, piles-up, dark/FPN noise etc.
  - Requires feature enhancement
- **Computation Issues**
  - Increased data stream → Accelerator→ Power Wall + Memory Wall
  - Requires data compression, feature extraction & recognition

Fusion of Sensing and computing is a trend

Near-Sensor Computing



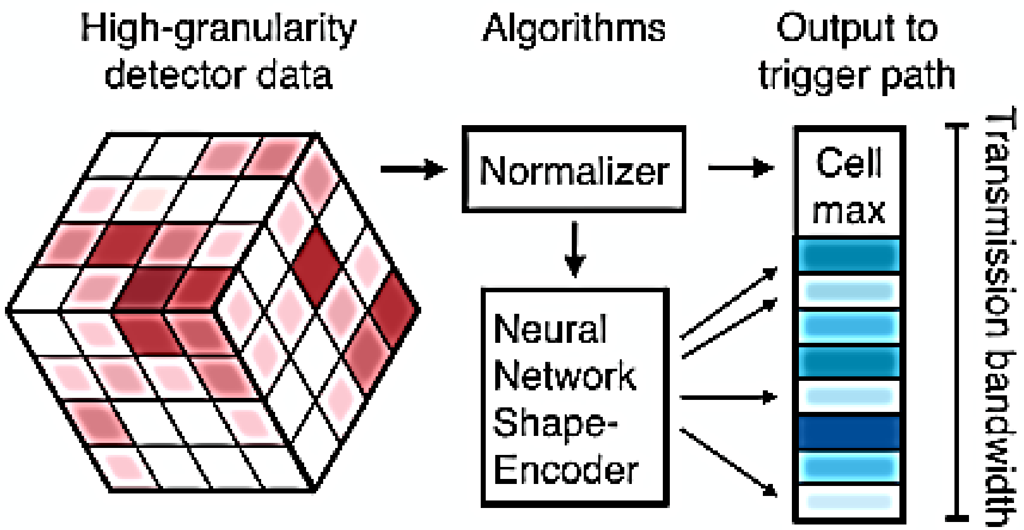
In-Sensor Computing



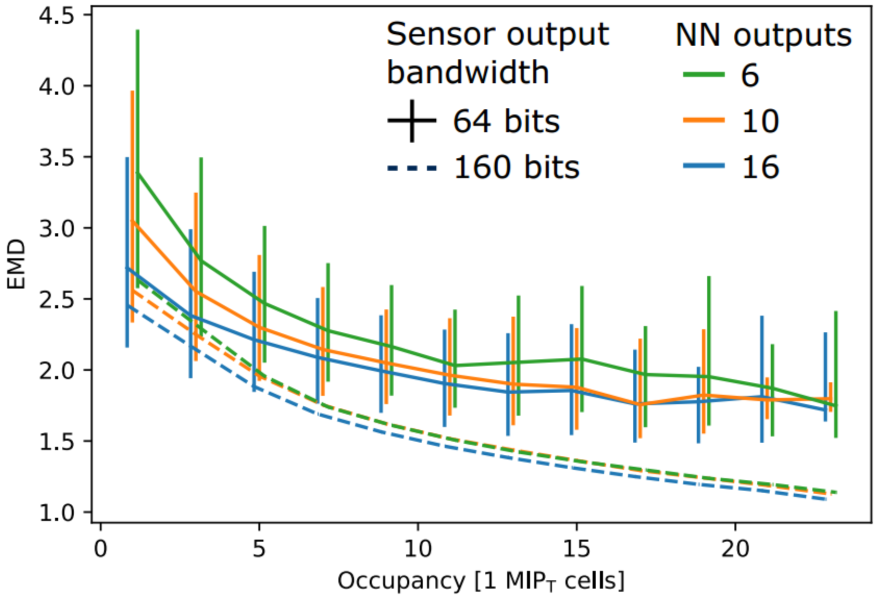
(W. Pan, Engineering, 2022)

③ Relative Work

- **Fermilab(2021): Front-end data compression based on convolutional neural networks for high granularity detectors**
  - **Two neural networks → Encoder and decoder**
  - **Deploying unique compression algorithms for sensors in different detector regions**
  - **Alleviates data transmission issues while retaining key information on detector energy distribution**

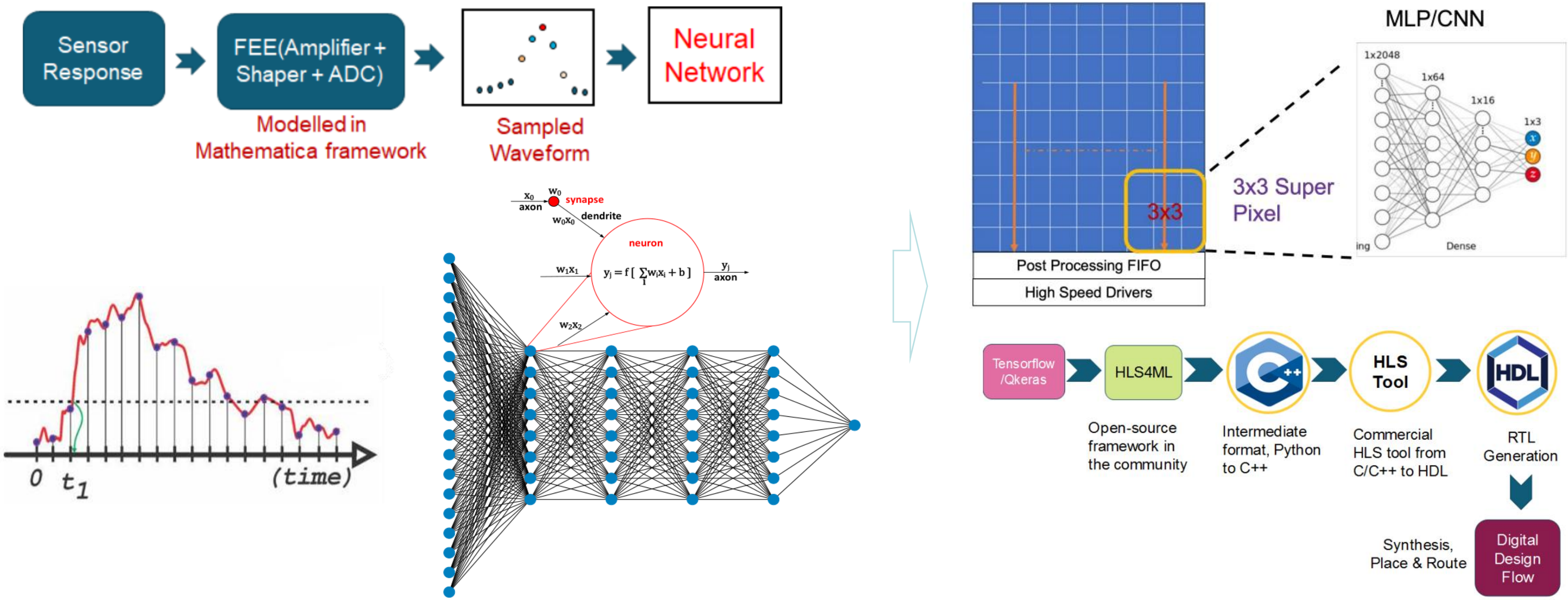


(Giuseppe Di Guglielmo, physics. Ins-det, 2021)



③ Relative Work

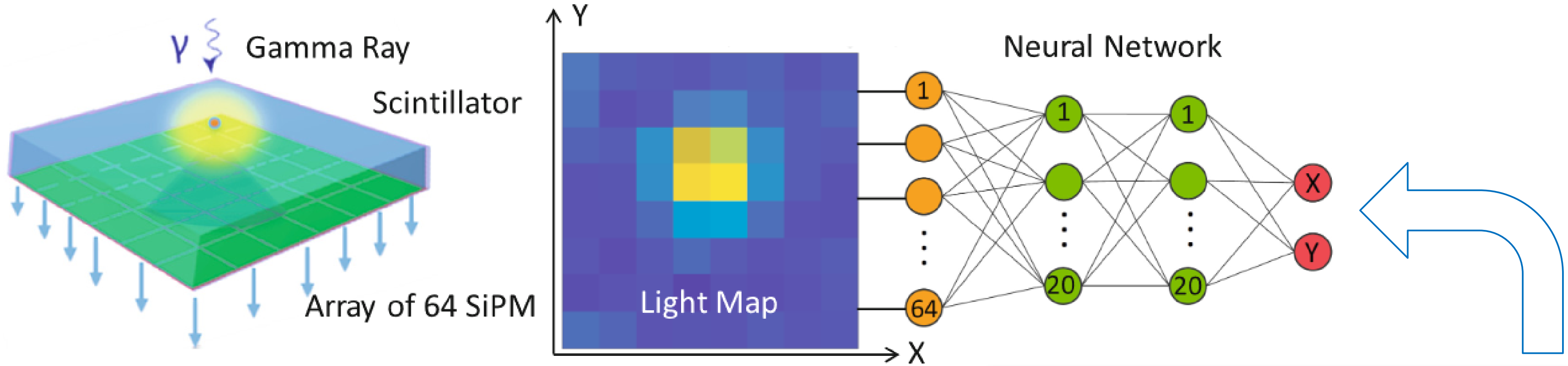
- **BNL(2022): Edge computing architecture for front-end electronics of particle detectors**
  - **Bring AI closer to the original data → Optimize the data processing of the increasing amount of data + Estimating Charge Signals from sampled Waveforms**



(Sandeep Miryala, BNL，ISQED, 2022)

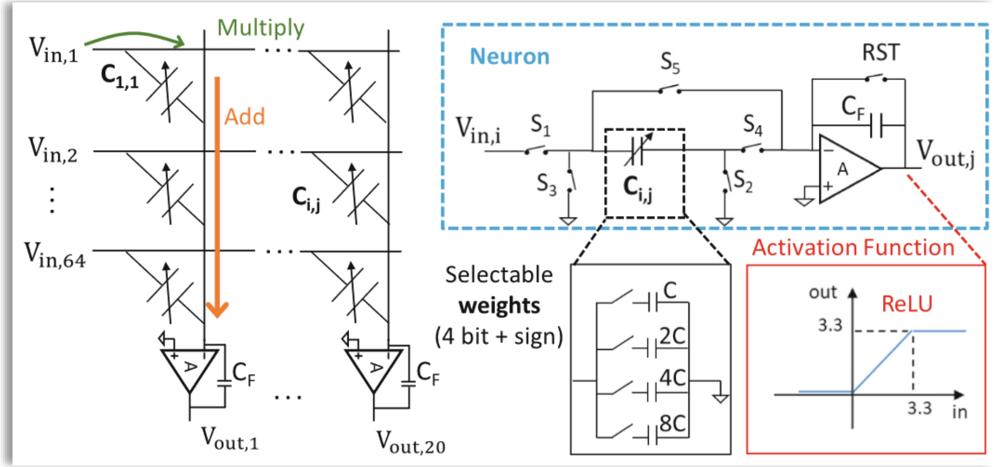
INFN(2024): In-sensor Intelligence in radiation detectors

– 64 inputs, 2 hide layers, and 2 outputs → reduce the data transfer (64→ 2)



- **Locating the scintillation coordinates** of gamma ray photons in scintillators
- **Applied for medical imaging**

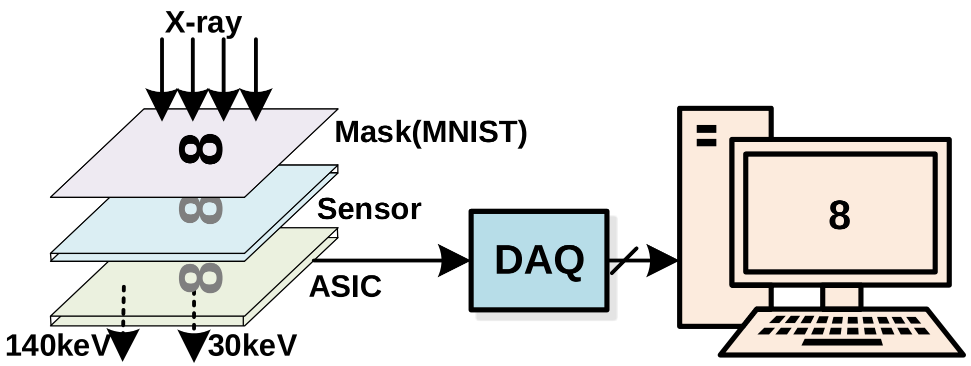
(S. D., Milano, 2024)

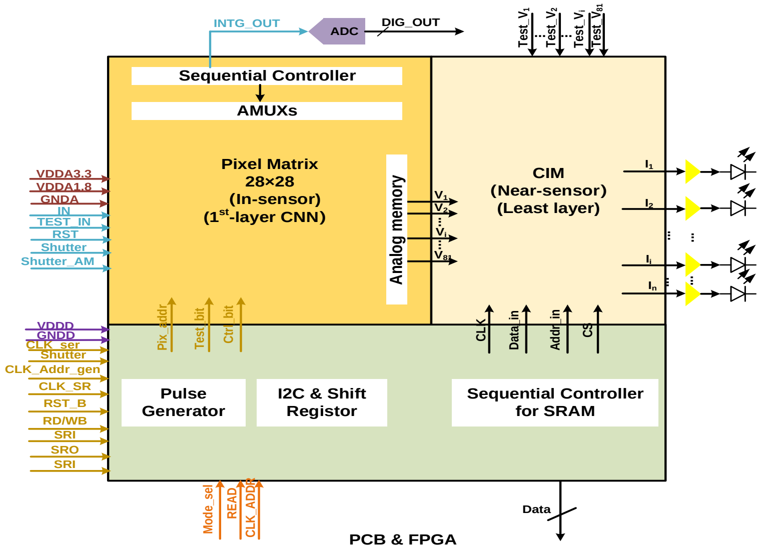


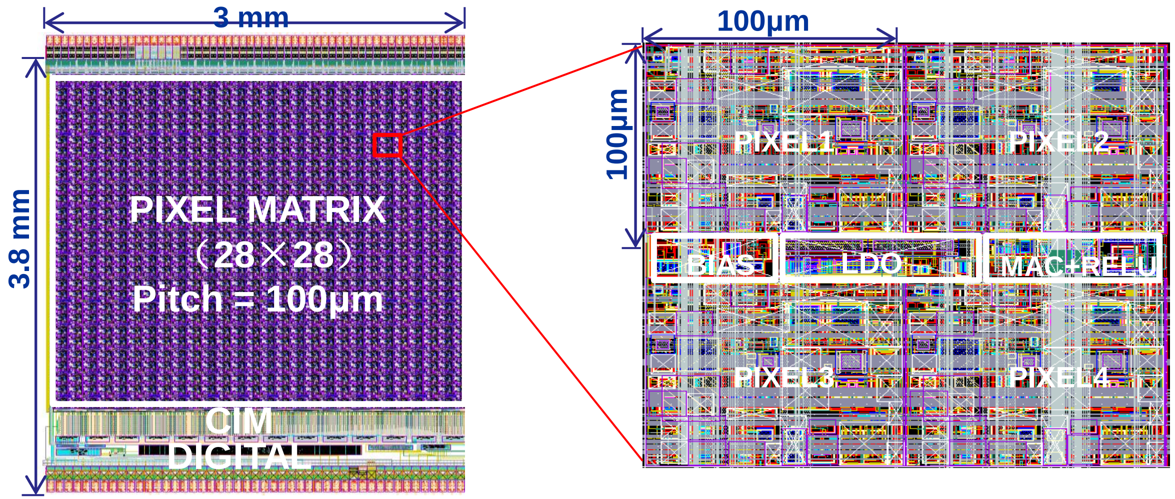
3 Alternative Proposals

NPU (2023): CNN-based Front-end Processor for X-ray imaging

- Pixel Readout + 3 layer Neural network （784 in，2×2 Cov. Layer,10 out)
- Analog computing employed
- Simulated accuracy of 90 %
- Fast X-ray Image Classification





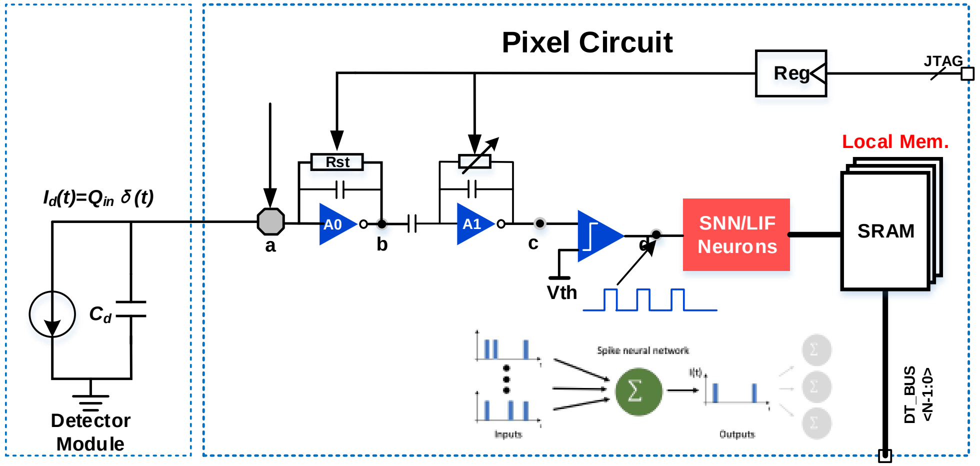


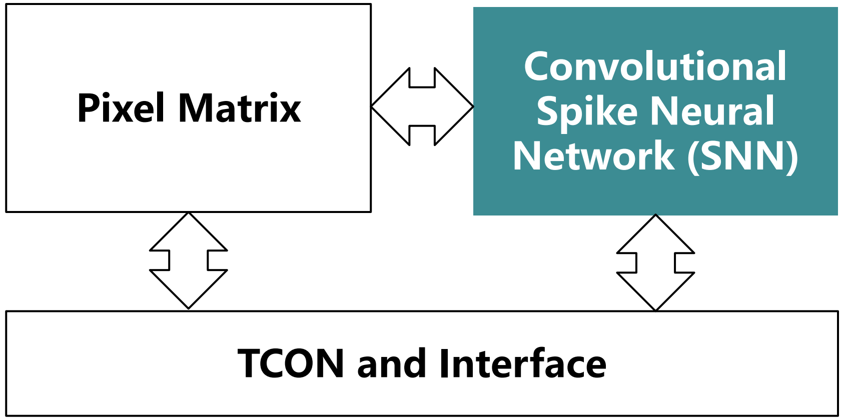
(J. Chen, NPU, 2023)

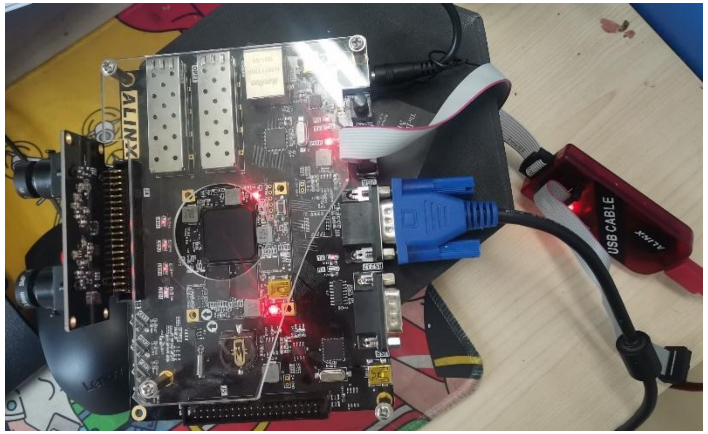
3 Alternative Proposals

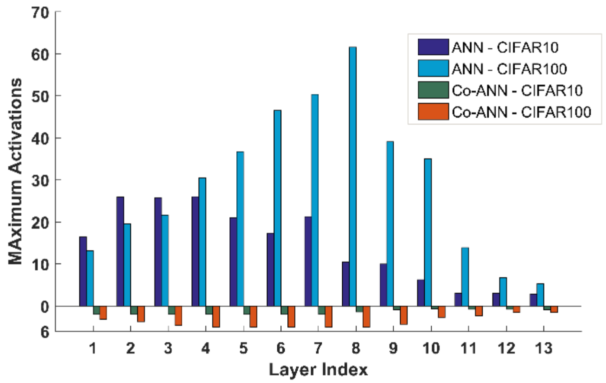
NPU (2024): SNN-based Front-end Processor for X-ray imaging

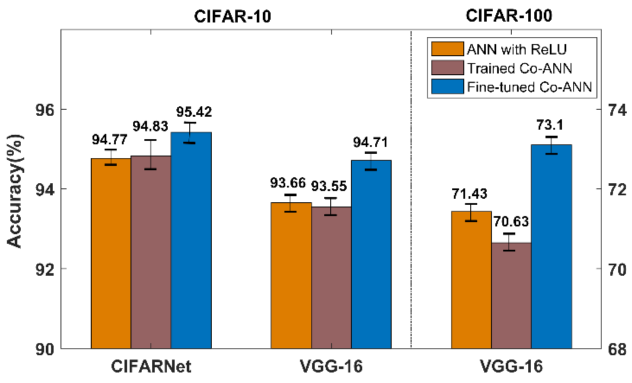
– Using LIF neurons to replace the integrator → improving accuracy to 95.4 %











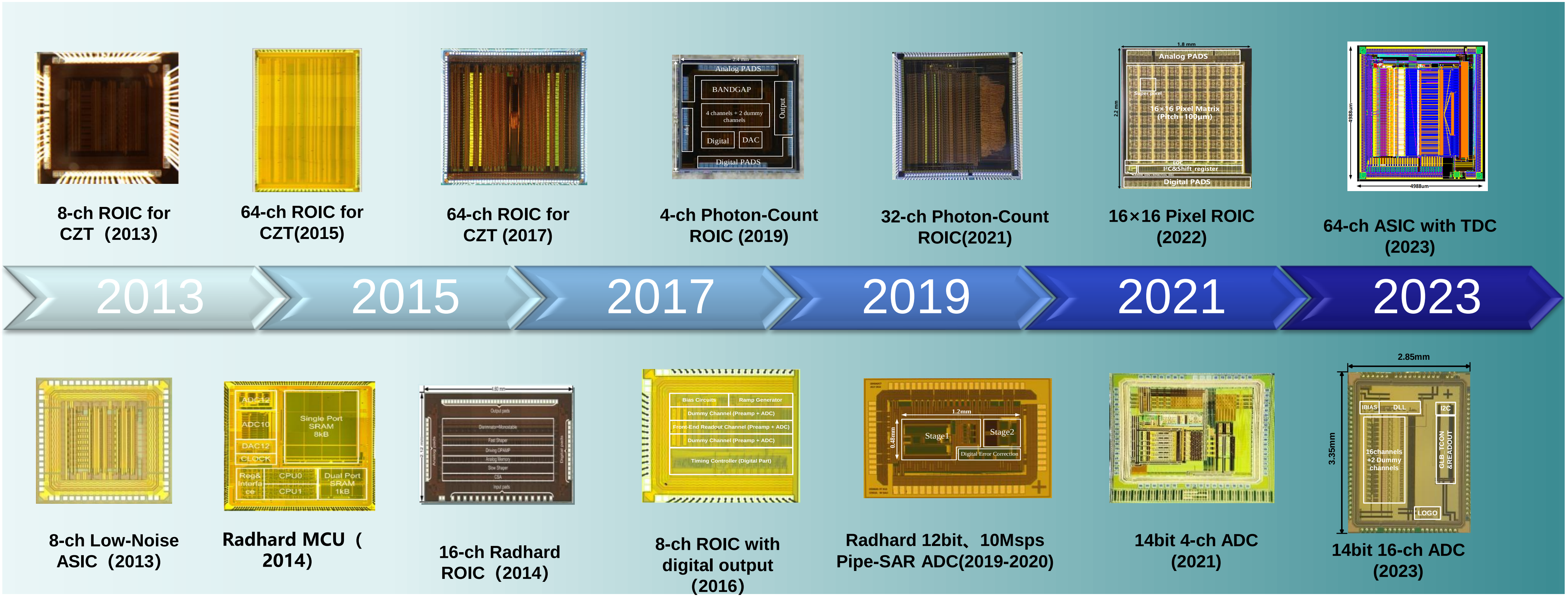
(D. Xu, NPU, 2024)

R&D of ASICs by Our Group

4 ASIC Overview

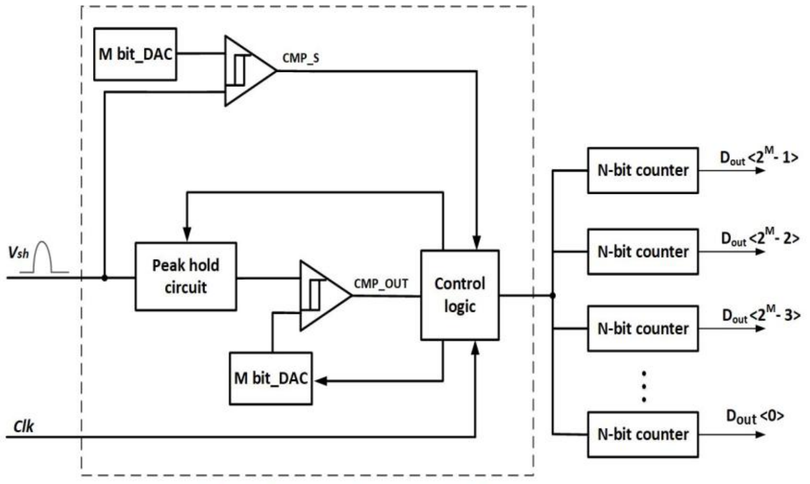
□ Developed Chips in the last 10 years

– 20+ types of ASICs and 50+ types of IP cores **from 0.35 μm → 0.13 μm CMOS**

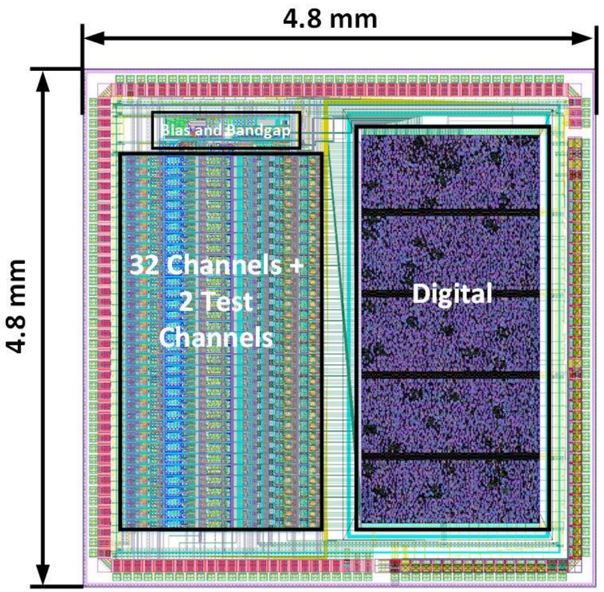


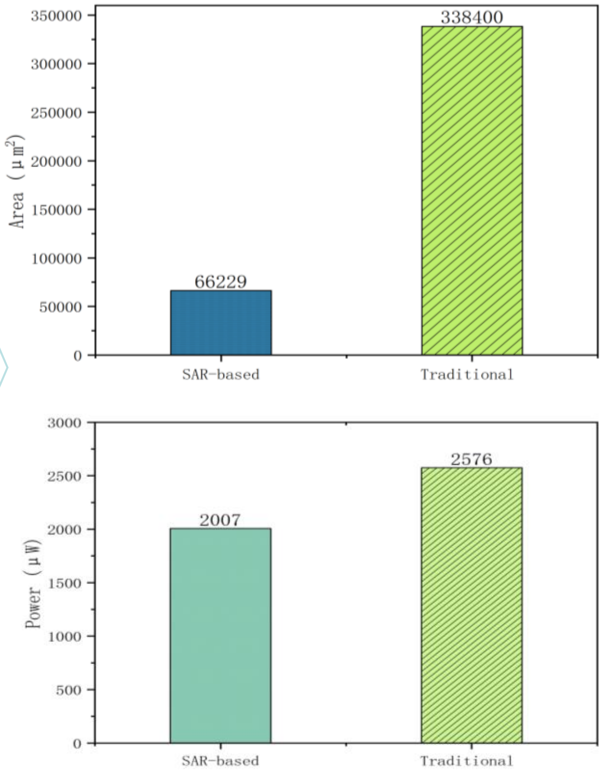
A 32-channel 8-Energy Photon-count ASIC for Si Strip Detectors

- 0.35 μm CMOS 3.3 V, 4.8 mm × 4.8 mm, Taped out：Mar. 2024
- ENC = 53 e- + 4.2 e-/pF, SAR-based photon count → X-ray diffraction imaging



Improved Multi-Energy_Discr_and_Digi

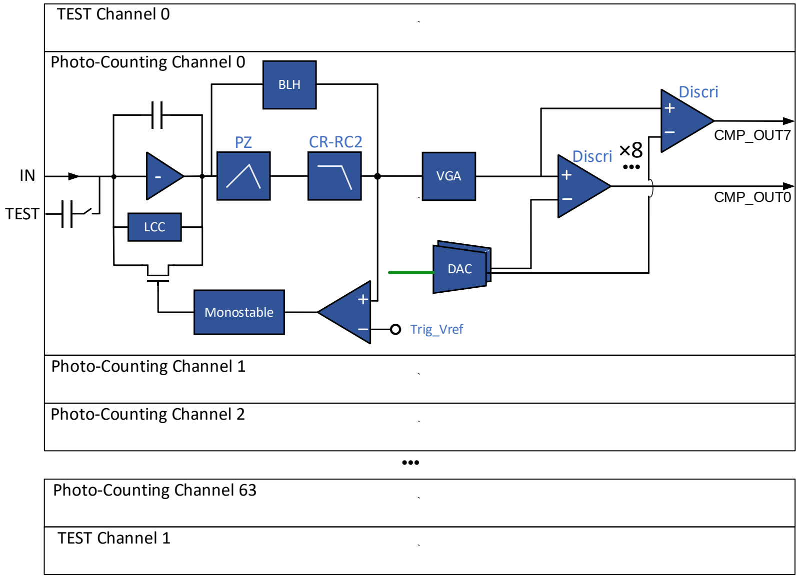


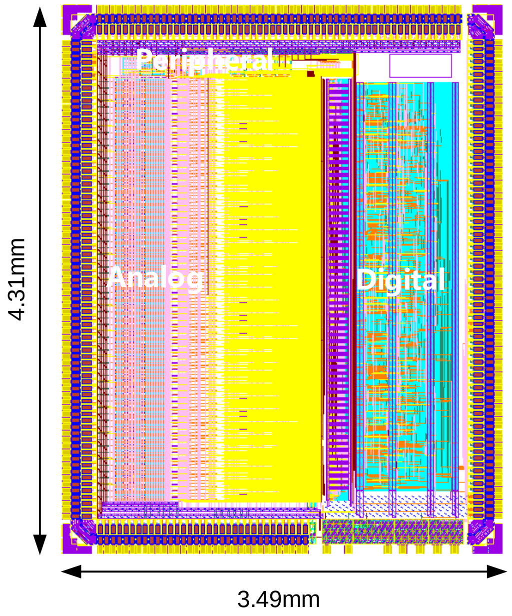


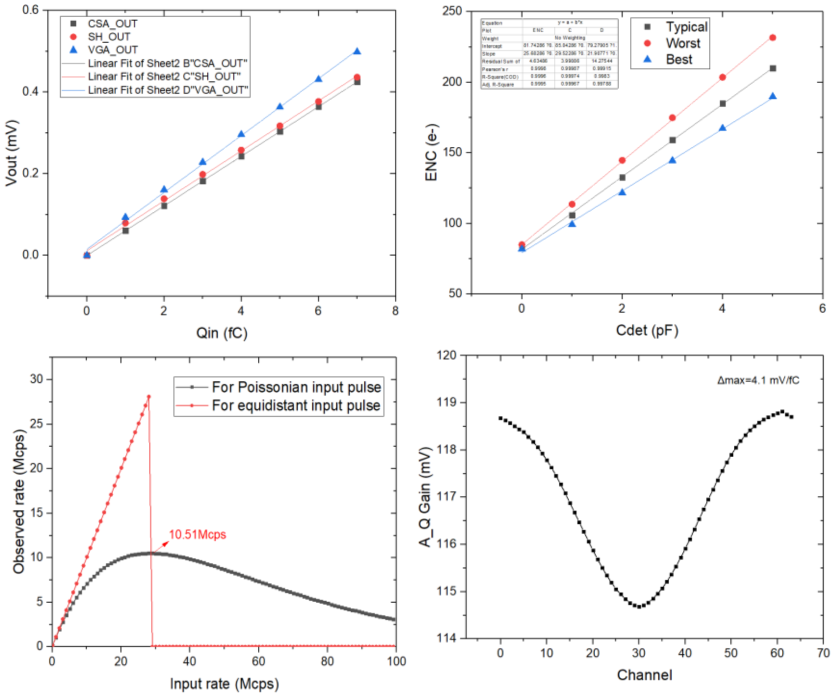
(Submitted to IEEE NSS/MIC 2024)

A 64-ch High-rate Energy-Resolving Photon Count Readout ASIC

- 0.13 μm CMOS 1.2/3.3 V, 4.3 mm × 3.0 mm, Taped out：Mar. 2024
- Eight 5-ns Discriminators/16-bit counters in each channel
- Automatic feedback reset → 10.5 Mcps
- Segmented Si Strip Detectors → CT imaging Scanners







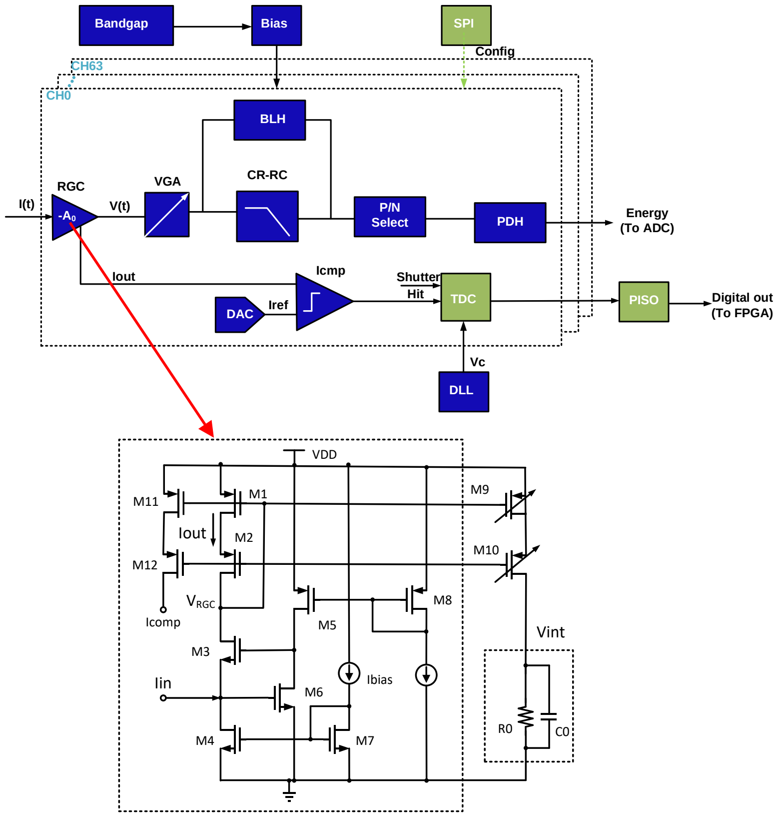
(Submitted to IEEE NSS/MIC 2024)

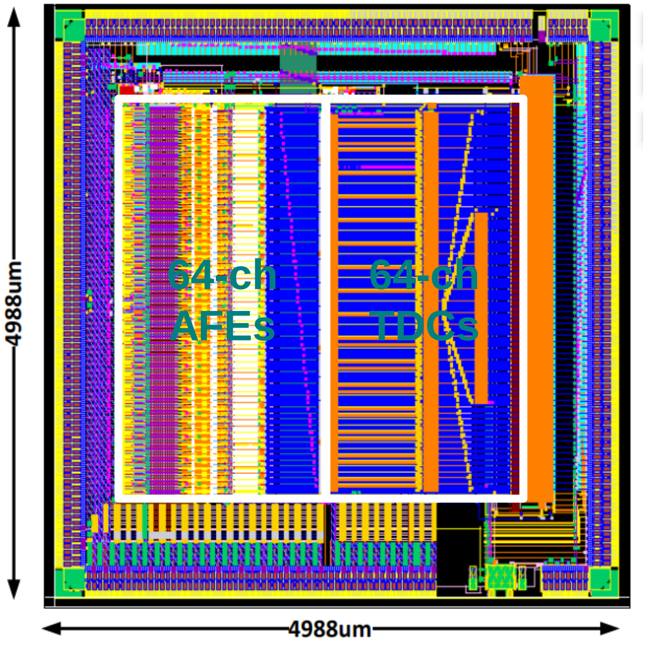
4 Representative work

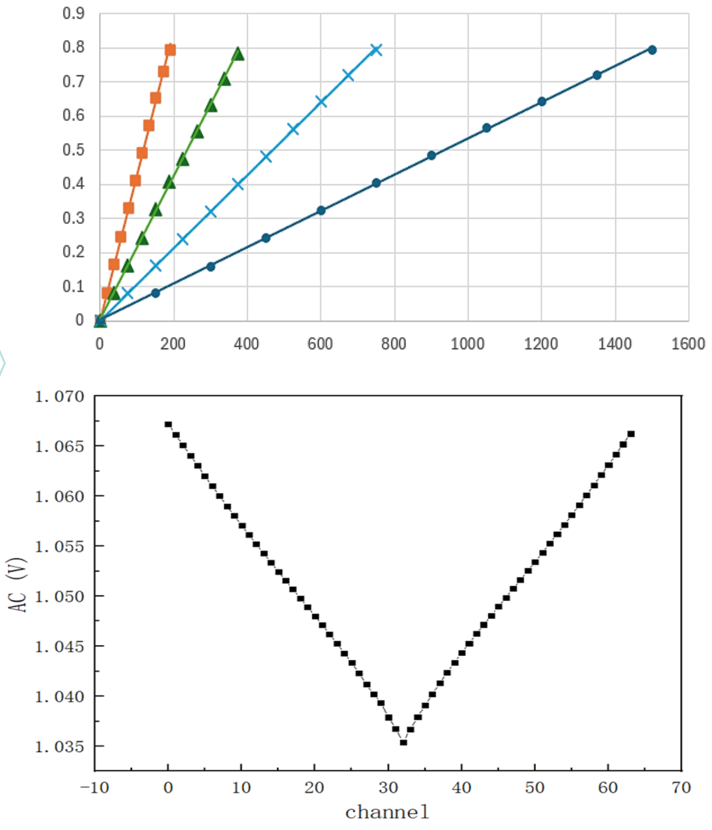
□ A 64-channel Readout ASIC with TDC for SiPM Detectors

– 0.13 μm CMOS 1.2/3.3 V, 4.98 mm × 4.98 mm, Taped out： Mar. 2024

– Q_{in} > 1500 pC, 1 Mcps, T_{bin} = 312.5 ps → SiPM based γ-ray imaging





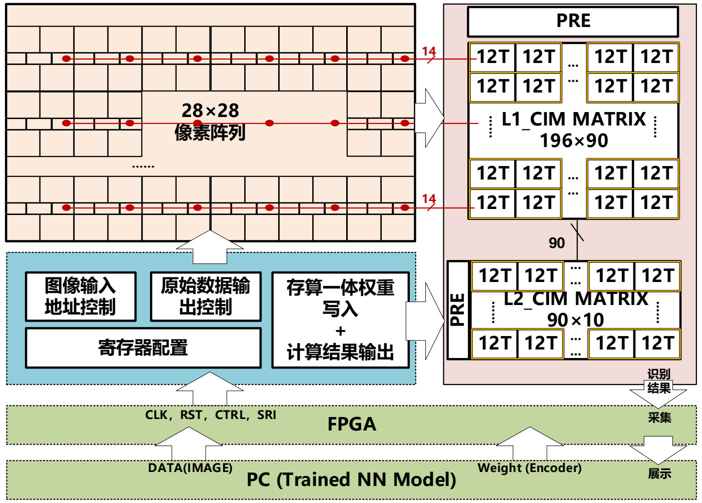


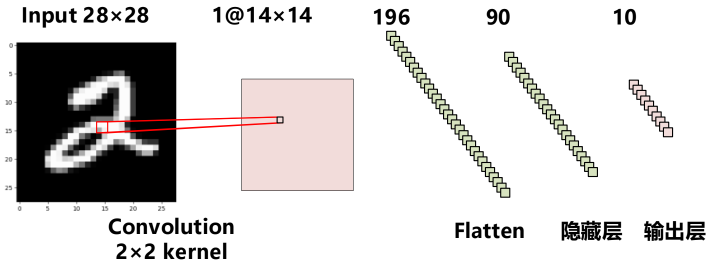
(Submitted to IEEE NSS/MIC 2024)

4 Representative work

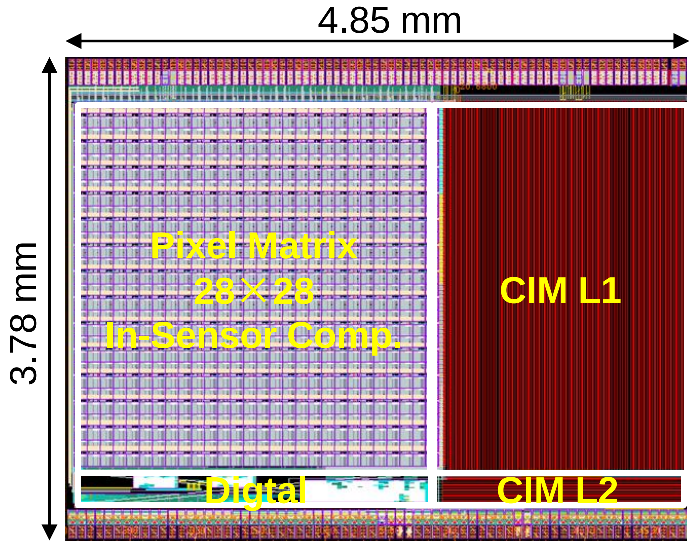
☐ A front-end processor chip based on convolutional neural network

- 0.18 µm CMOS 1.8/3.3 V, 3.78 mm × 4.85 mm, Taped out：Jun. 2024
- 28×28 pixel readout circuits with 2×2 super pixel built-in LDO
- CNN network→ 1st layer (Analog MAC + ReLu) in pixel matrix + 2 layer FC (CIM)
- Precision up to 92 % when hide layer nodes is 90





Conv. Layer	FC Layer	Precision
1 layer（2×2)	Hide（120)	92.0%
1layer（2×2)	Hide（100)	92.5%
1layer（2×2)	Hide（90)	92.2%
1layer（2×2)	Hide（32)	89.6%



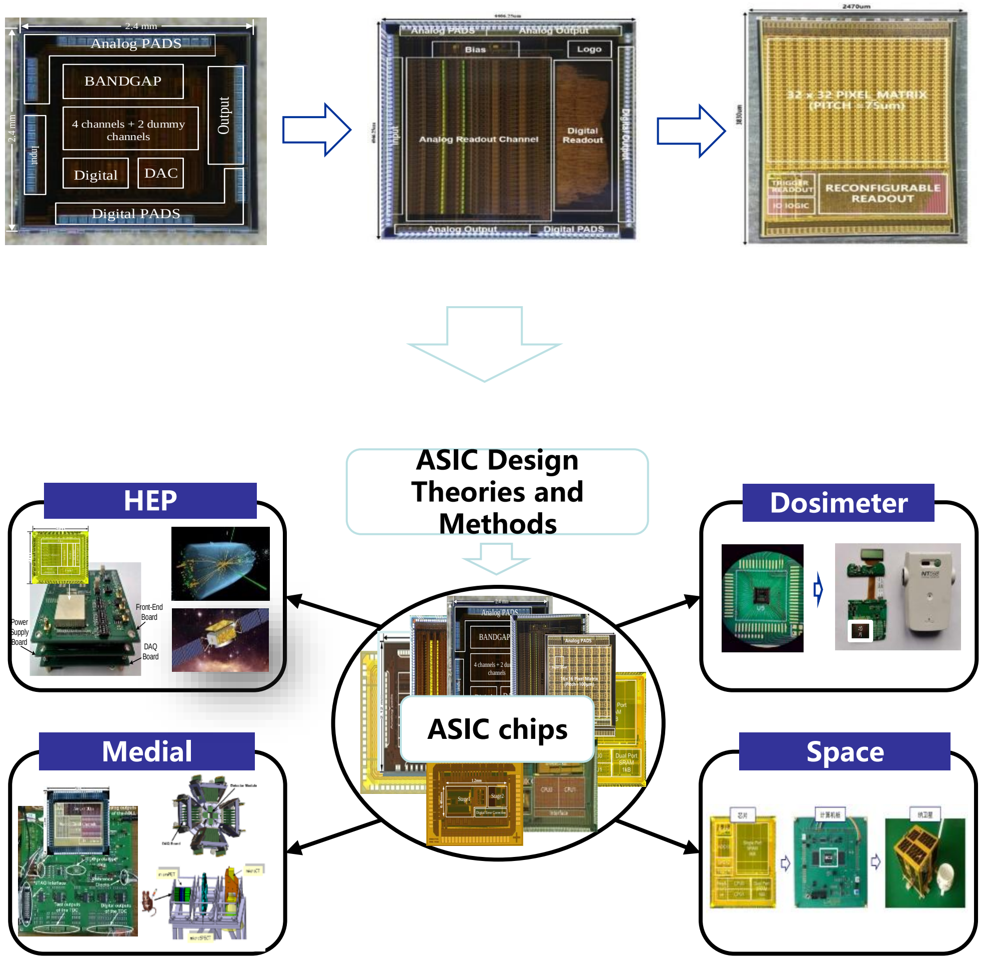
(To be submitted to TCAS-I)

Conclusion and Perspective

5 Conclusion and Perspective

Conclusion

- ✓ Basis of front-end electronics
- ✓ State-of-the-art work and Trends
- ✓ Intelligent front-end Processors
- ✓ R&D of front-end ASICs in NPU



Future Work

- ➢ 192-ch 8-Energy Photon-Count ASIC
- ➢ 256 × 256 pixel readout ASIC
- ➢ CNN/SNN-based front-end Processors

More collaboration !


Thanks for your attention!
Q & A