A CMOS Pixel Sensor for Precise Measurement on Charge and Track of Cosmic Ray

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on behalf of

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Outline

- **Research Motivation**
- **Architecture of Pixel Sensor Chip**
  - Design Goal
  - Process Selection
  - Chip Architecture
- **R&D of Pixel Sensor Chip**
  - Pixel Array and Front-end Circuit
  - Column-end Signal Processing and A/D Conversion
  - Full Function Chip Prototype
  - Chip Readout/Test electronics design
- **Summary & Future Work**

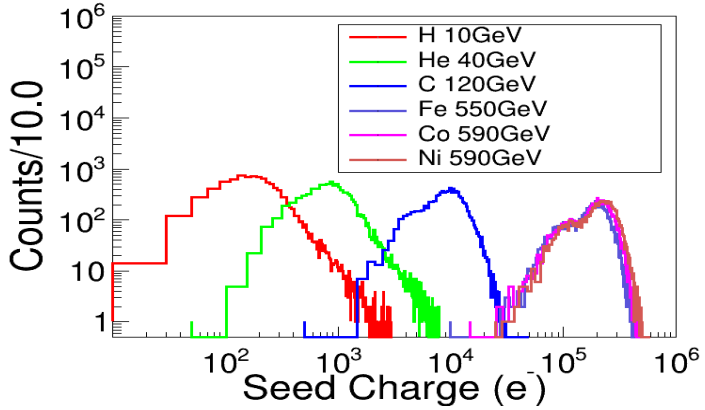
Motivation

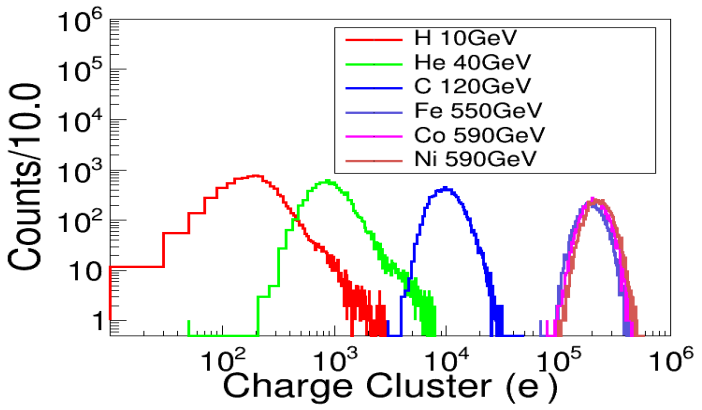
❑ Measurement of particle charge number practical for silicon pixel sensors

- ❖ e^-/h^+ pairs exited proportion to particle ionization energy loss dE/dX
- ❖ ionization energy loss of incident minimum ionization particles proportion to the square of its charge number

$$Bath\ fomula: -\frac{dE}{dx} = Kz^2\frac{Z}{A}\frac{1}{\beta}\left[\ln\frac{2m_e c^2\beta^2\gamma^2 W_{max}}{I^2} - \beta^2 - \frac{\delta(\beta\gamma)}{2}\right]$$

➢ Simulation result: Distribution of charge collected by seed pixel and pixel cluster in X-FAB CIS process for different incident particles



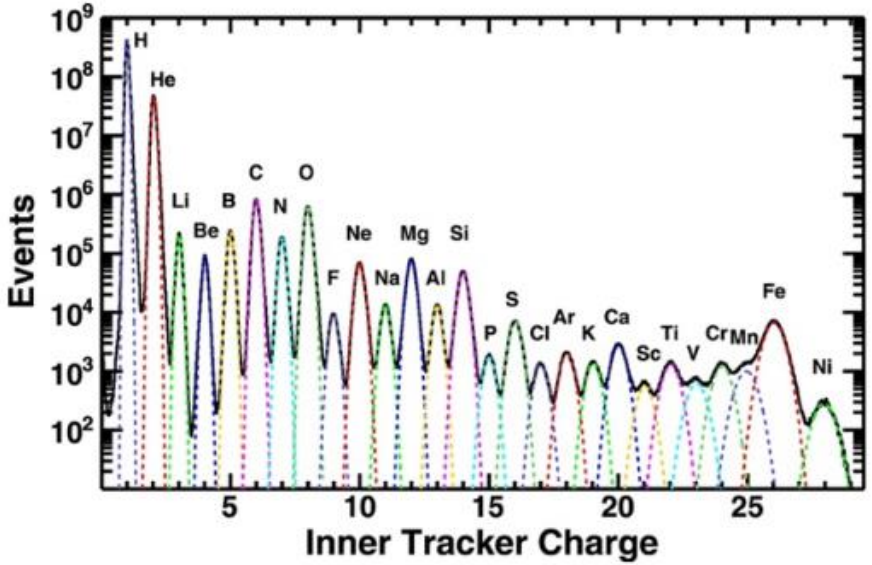


Design Goal

- **Design Goal**
  - distinguish the particle track and nuclear charge number with high precision

- **Physics performance index: same standard with AMS**
  - Target spatial resolusion : ~10um
  - Target charge resolution : 1(H)-28(Ni)

- **Sensor performance index**
  - Pixel pitch: 50um for ~10um resolution
  - AD conversion accuracy: LSB 1mV for noise modeling, 8^{+} bit DR
  - Full scale chip pixel matrix: 256×256



Measurement of nuclei charge distribution by AMS inner tracker

Process selection

❑ **Process investigation**

X-fab

- *180nm CIS*
- *EPI Thickness：5um*
- *EPI resistivity：8 Ω· cm*

TowerJazz

- *180nm CIS*
- *EPI Thickness：18 μm*
- *EPI resistivity：1kΩ·cm*

TSMC

- *180nm CIS*

Lfoundry

- *180nm CIS*
- *EPI resistivity：>2kΩ·cm*

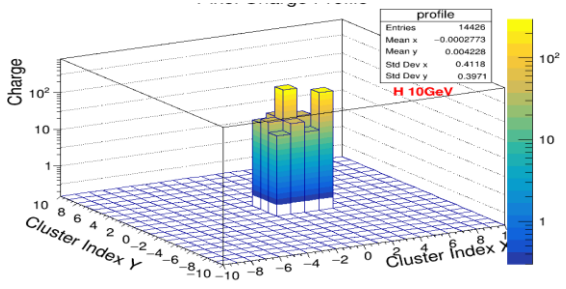
❑ **Only X-fab provides fabrication service for us**

Process Selection

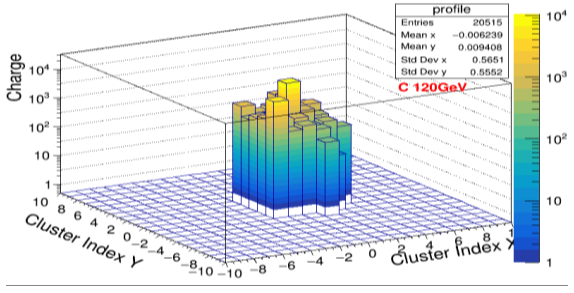
❑ Process Performance Evaluation in AllPix² + TCAD： charge collect ability

- ❖ Charge collection capacity： low Z nuclei distinguishable, saturate for high Z nuclei (Fe/Co/Ni)
- ❖ H^+ excite electron: most in 50+ region
- ❖ Cluster scale: max 7×7 for high Z nuclei， DR for most pixels below 20000e^-

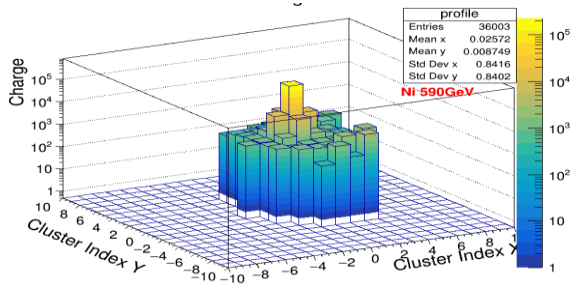
➢ Simulation result: Fire pixel position and charge distribution



❑ Z = 1

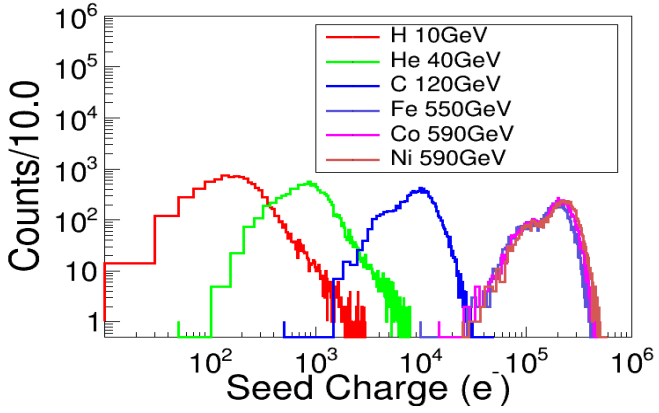


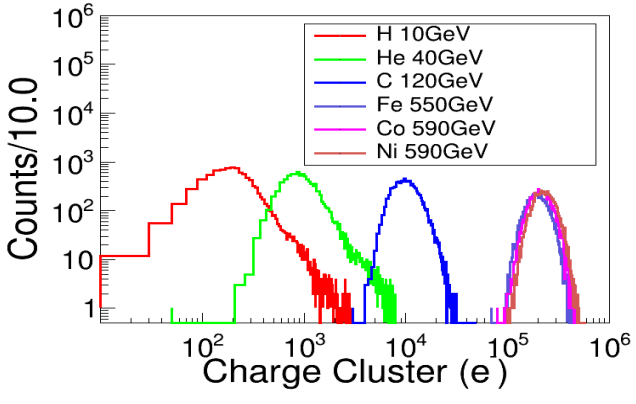
❑ Z = 6



❑ Z = 28

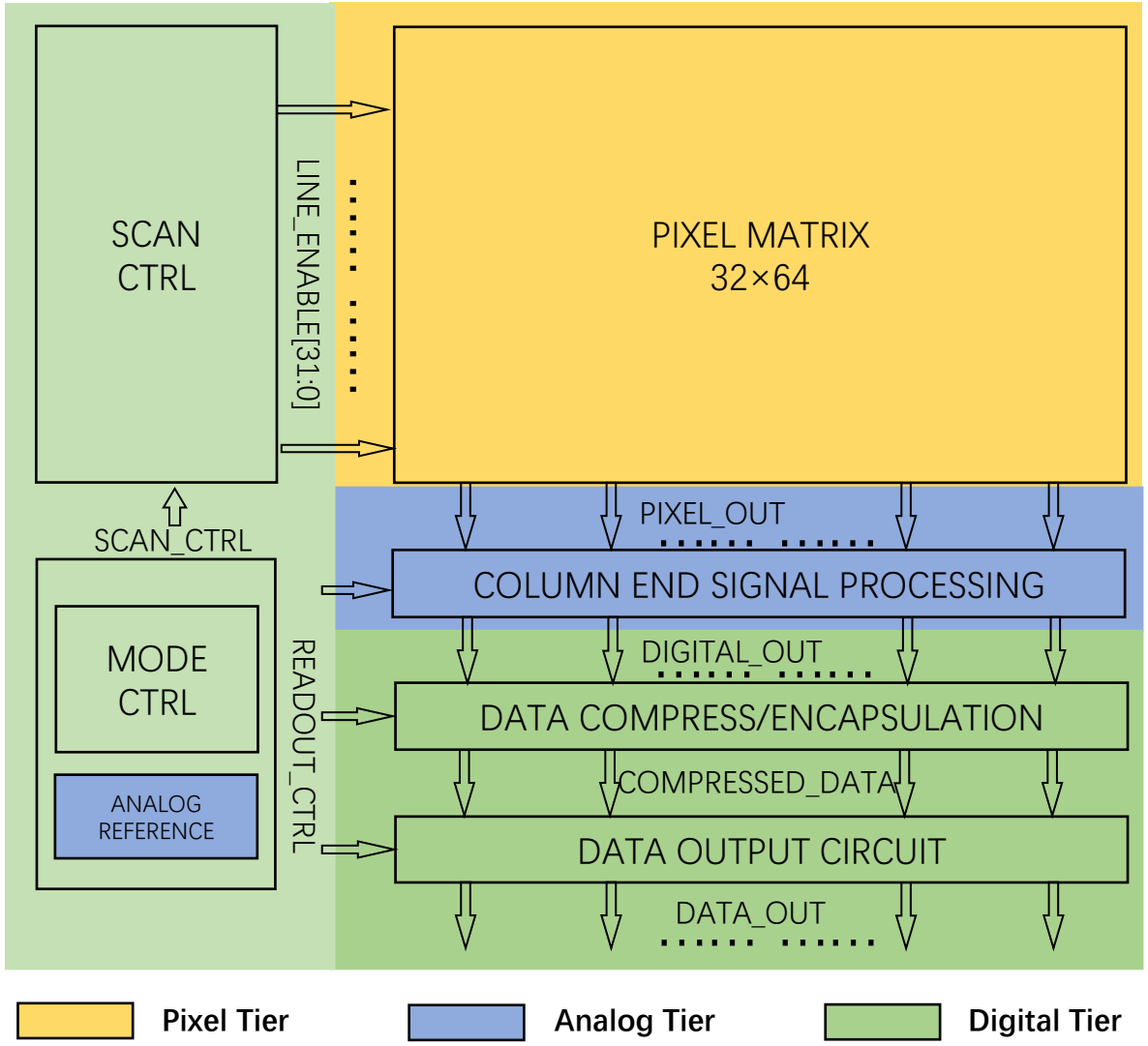
➢ Simulation result: Distribution of charge collected by seed pixel and pixel cluster



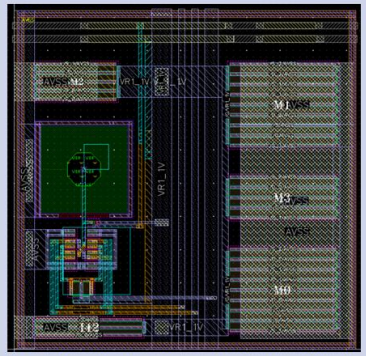
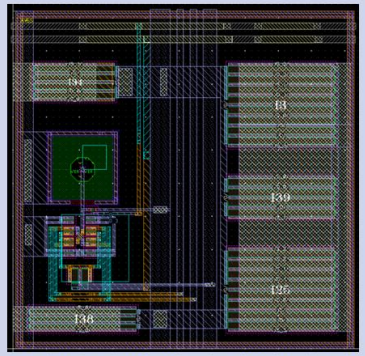
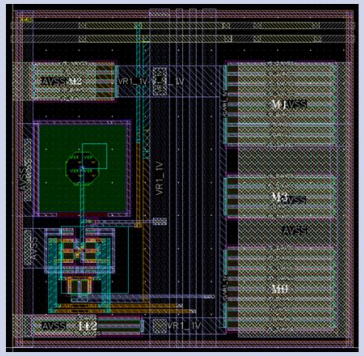


Chip Architecture & Feature—chip overall view

- **X-fab 180nm CIS process**
  - 6 metal layers used
  - No deep P-well: PMOS cannot be used in pixel circuit
- **Pixel array**
  - pixel array: **32 rows × 64 columns**（3 different pixels）
  - Rolling shutter readout mode (600 ns/row)
- **Full functional chip**
  - Frame rate：52kHz（19.2us/frame）
  - DR 23000e-, resolution 25e-
  - Row-end **rolling shutter** pixel driving
  - Column-end signal processing (CDS PGA & ADC)
  - On-chip **data compression & encapsulation**
  - Auxiliary modules: Buffers/I2C/BGR ……
- **Full Function Chip Tape-out in Feb 2024**

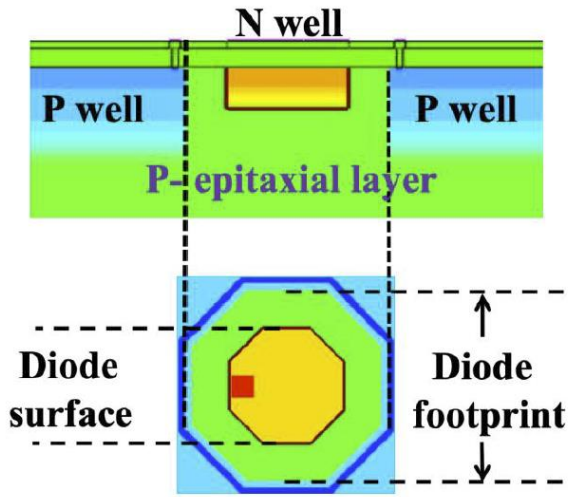


Pixel Array

DIODE S20F200	DIODE S10F100	DIODE S20F200 LONG CHANNEL
		
Column0~15、48-63	Column16~31	Column32~47

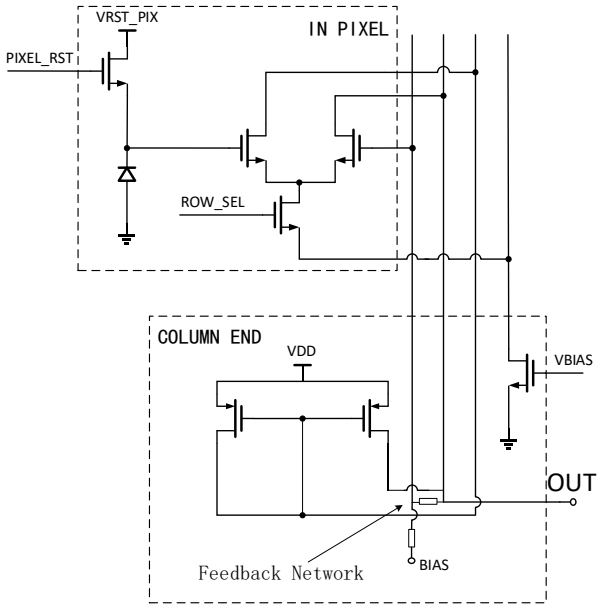
- **Rectangular pixels**
  - Pixel pitch： 50 µm
- **3 different pixels**
  - study charge collection and noise performance
  - Different diode sizes and transistor sizes

- **Octagonal diode:**
  - Diode surface： 10/20 µm²
- **Study RTN (Random Telegraph Noise) performance**
  - Front-end Transistor Size:180nm/500nm × 1.5um × 2
- **Diode surface/footprint:** 0.1

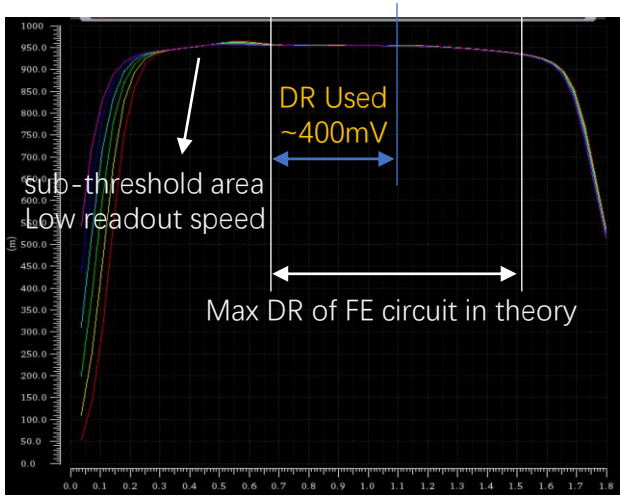


Front-end Readout Circuit

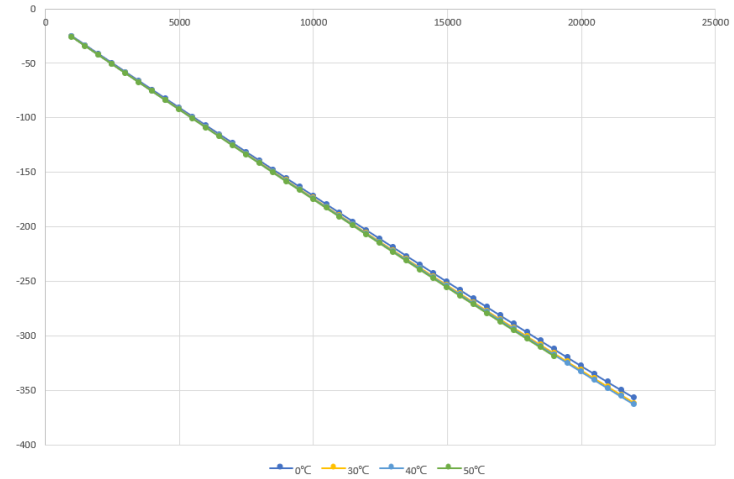
Front-end circuit



Input Voltage - Small Signal Gain@0℃-50℃



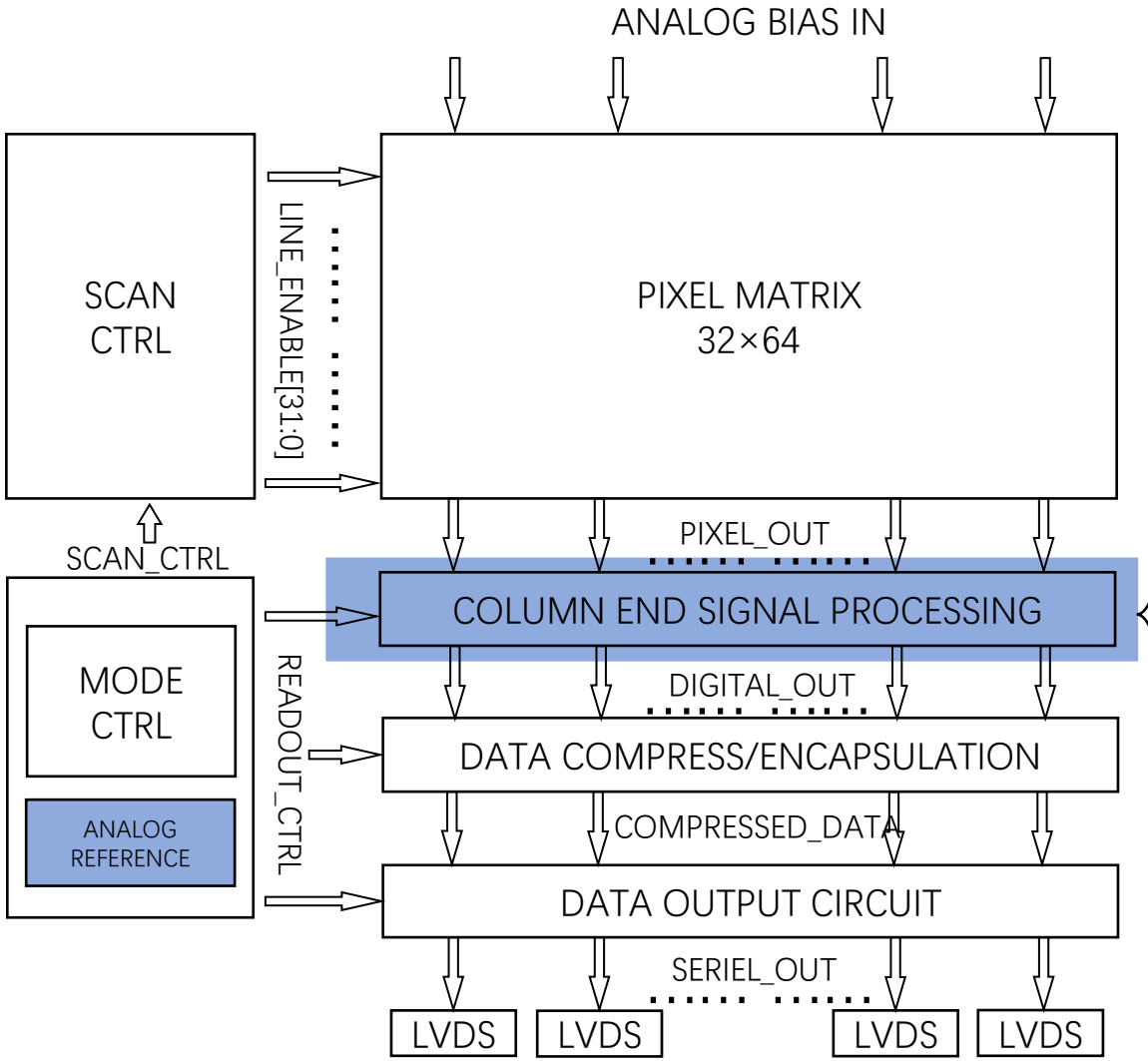
Charge - output voltage@ 0℃-50℃



- ❑ Active reset structure
- ❑ Power supply 1.8V
- ❑ All NMOS in pixel
- ❑ Column-level sharing PMOS-type load
- ❑ CDS compatible

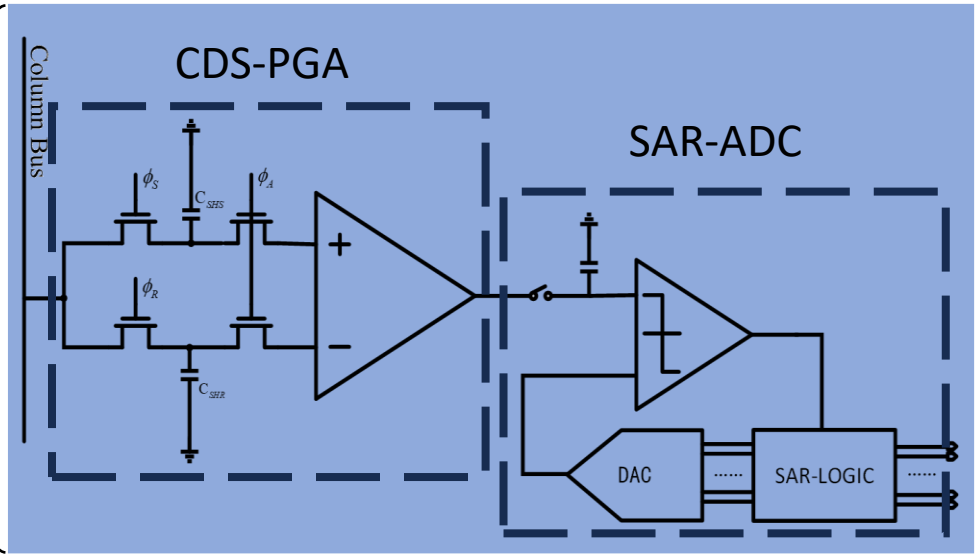
- ❑ Close looped 1×（Higher Precision）
- ❑ Better consistency under Different PVT condition(FPN 10e^-)
- ❑ Relatively larger DR under low supply power(23000 e^-)
- ❑ CVF (Charge-Voltage Factor)： 16uV/ e^-
- ❑ Better linearity throughout DR

Column-level Signal Processing

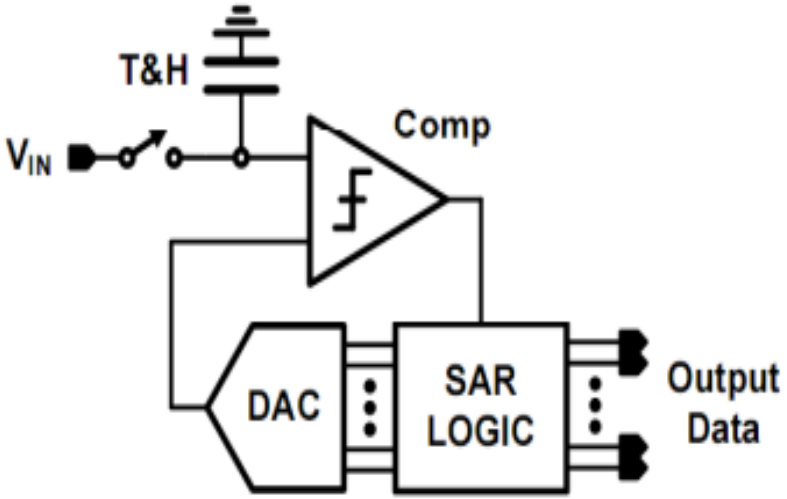


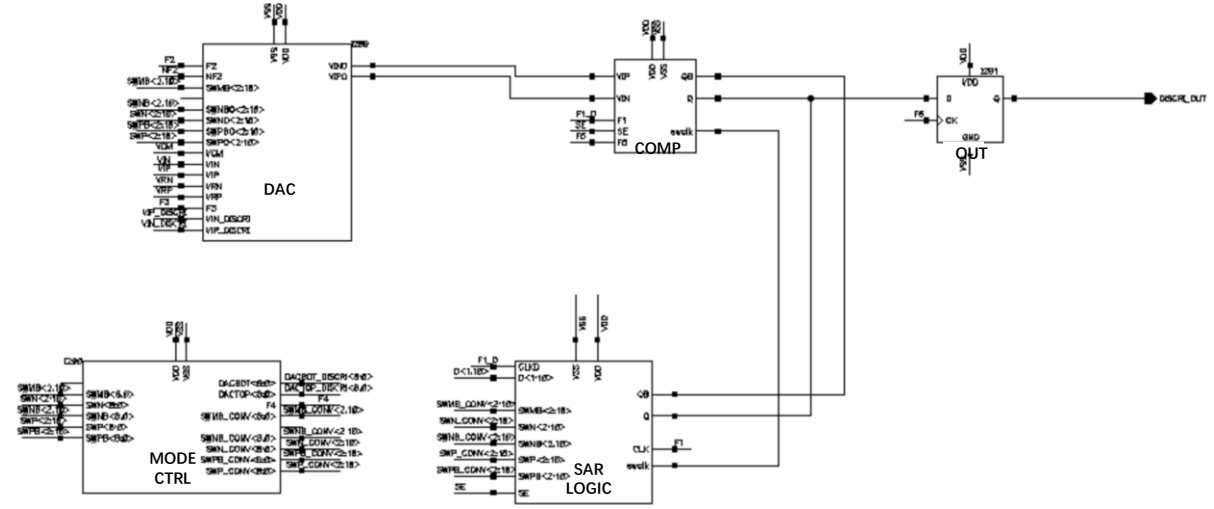
Circuit function

- CDS-PGA: Signal Amplify, Reduce Correlated Noise
- ADC: Convert Analog Signal to Digital region
- Overall performance: DR 23000e^- resolution:25 e^-



Column-level Signal Processing ——SAR-ADC





❑ SAR-ADC Block Diagram

- ❖ N bit digitization in N clock cycles
- ❖ Op. Amp. free, Low power consumption
- ❖ Circuit size practical for column integration

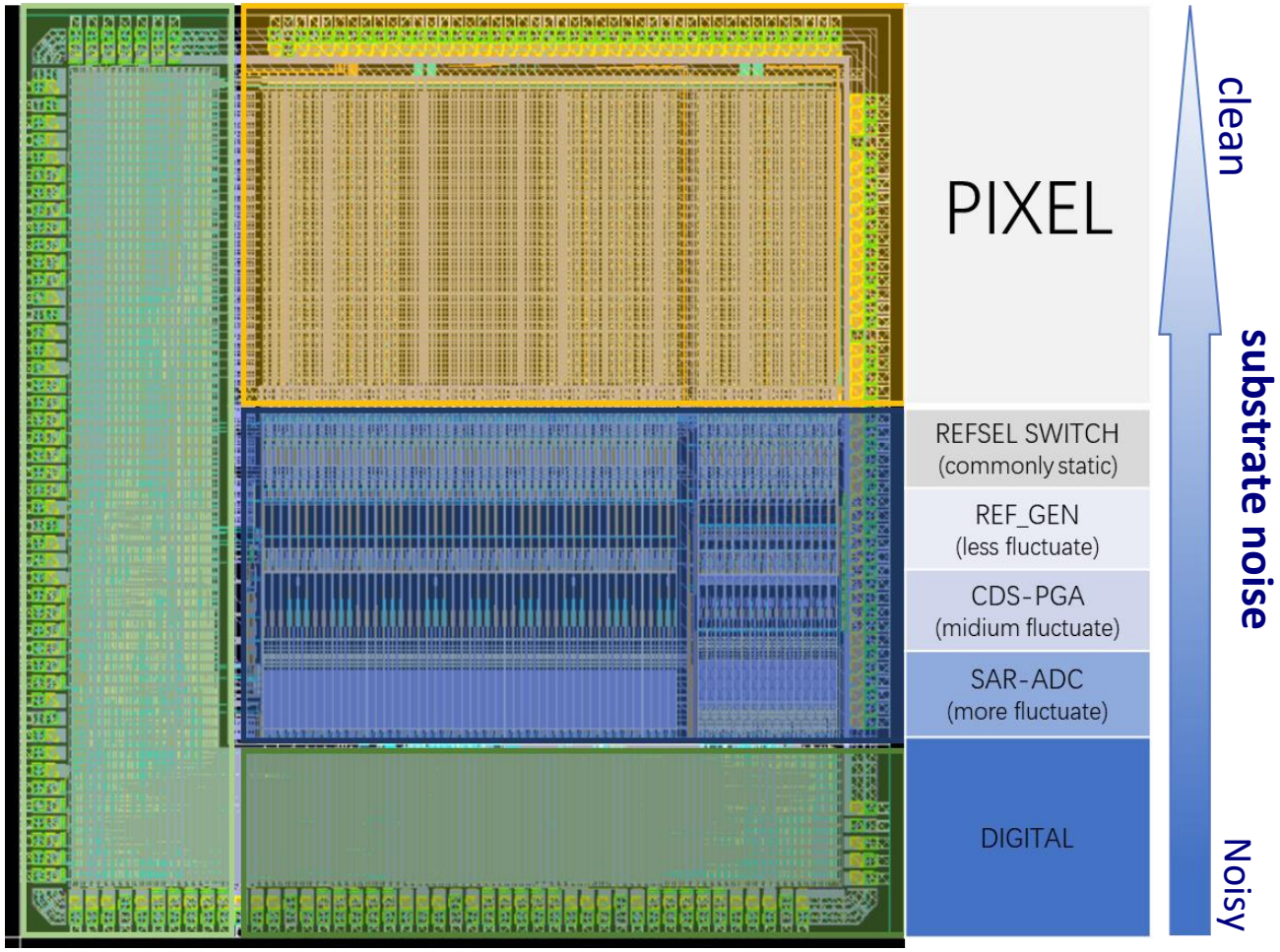
❑ Implemented SAR-ADC

- ❖ S&H integrated with CDAC
- ❖ Capacitor number minimized using monotonous switching timing & bridge capacitor
- ❖ Asynchronous clock generated for high speed conversion

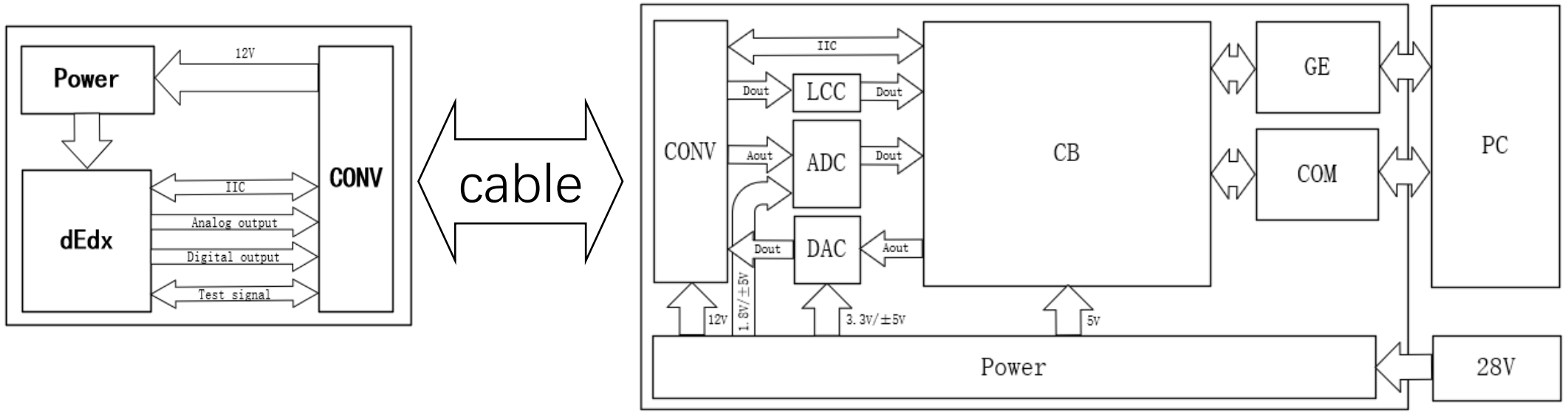
ADC performance index	ENOB	MAX INL	MAX DNL	Samp. Rate	DR	Area
Value (post-layout sim)	8.9 (10) bit	0.9 LSB	0.6 LSB	10MHz	1.2V Vpp	50×920um²

Full Function Chip Prototype

- **Chip floorplan**
  - Core area: 5 × 5 mm^2
  - Pad num. : 193
  - Pixel area: 4 × 2 mm^2
- **Layout arrangement**
  - arranged in order of substrate noise
  - Clean electrical environment for sensing area
- **Submitted in Feb. 2024**
  - Fabrication to be finished in July 2024



Readout/Test Electronics Design



❑ DUT Board

- ❖ Wire bonding
- ❖ Chip power supply, connector

❑ Main Board

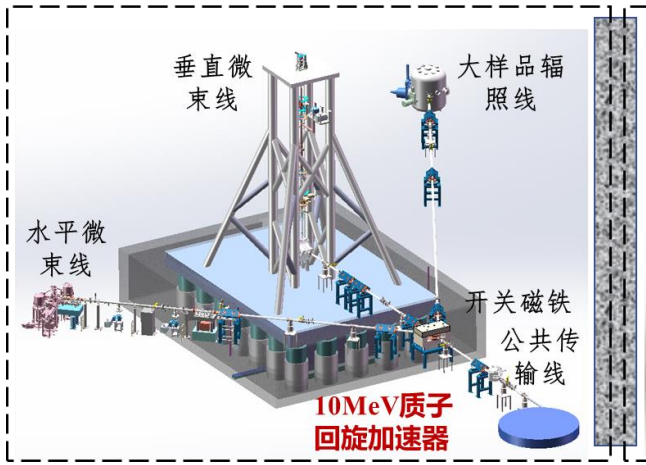
- ❖ Chip configuration, data acquisition, test signal processing
- ❖ Level convertor, ADC, DAC, FPGA Core Board, Gb Ethernet, COM
- ❖ FPGA Core Board: ZYNQ7020

Future Work

- **Basic functional testing of chips**
  - Probe station, chip function, dEdx function
- **Beam experiment**
  - Z=1~26
  - The Heavy Ion Research Facility in Lanzhou(HIRFL):H_2^+~U, 100~1000MeV/u
- **Chip radiation damage test**
  - Space Envirnomrnt Simulation Research Infrastructure(SESRI): 哈工大空间环境地面模拟装置质子辐照损失实验
  - Comparison Fe test results of chips before and after irradiation
- **Next full scale chip to be submitted for fabrication after prototype test**

SESRI: 哈工大十二五国家重大科技基础设施—空间环境地面模拟装置

- **Ion accelerator system**
  - Provide ground simulation radiation sources: P and all heavy ions of He~Bi
  - Low-energy accelerator for 10 MeV protons
  - Medium- and high-energy accelerator for 300 MeV proton/heavy ions
- **Device ion irradiation system**
  - High energy proton irradiation terminal: 单粒子效应(SEE)、位移损伤效应(DDD), 总剂量效应(TID)
  - High energy heavy ion irradiation terminal：重离子辐射效应评测和重离子辐射加固技术验证



低能加速器系统

中高能加速器系统

SESRI: 哈工大十二五国家重大科技基础设施—空间环境地面模拟装置

- Part of the 300MeV proton/heavy ion accelerator can accelerate particles and their parameters:

离子	能量（MeV/u)	LET（MeV·cm²/mg)	射程（μm)
P	100-300	0.0058-0.0029	41.62mm-273.6mm
He	30-80	0.0589-0.0257	4.93mm-28.21mm
C	20-40	0.722-0.4177	813.0-2780
Kr	7-15	35.46-25.64	71.2-167.97
Xe	7-15	64.58-50.36	68.64-148.75
Hf	5-10	85.16-75.78	57.92-106.26
Ta	5-10	86.45-77.2	57.92-105.56
Au	6-8	92.46-89.12	68.48-87.15
Pb	6-7.5	96.44-93.76	68.36-82.46
Bi	6-7.5	97.85-95	68.10-82

Summary

- Proposed Pixel sensor chip can perform particle track and charge distinguish with high precision
- Charge discrimination of the CMOS pixel sensor is based on ionization energy loss measurement of incident particles
- The sensor works in rolling shutter mode and will measure ionization exited elections up to 23000 with ADC in 10-bit accuracy
- The work is conducted in XFAB 0.18um CIS process and has tape-out in Feb. 2024
- The sensor prototype is estimated to perform good distinguish performance upon nuclei from H to C and beyond, high Z nuclei distinguish resolution estimated to be low due to saturation

Thanks

Acknowledgement

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