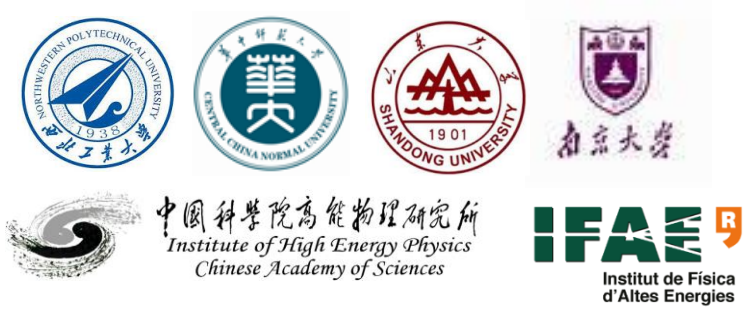

用于CEPC顶点探测器的单片式像素探测器原型样机的研制

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On behalf of the CEPC Vertex detector study team

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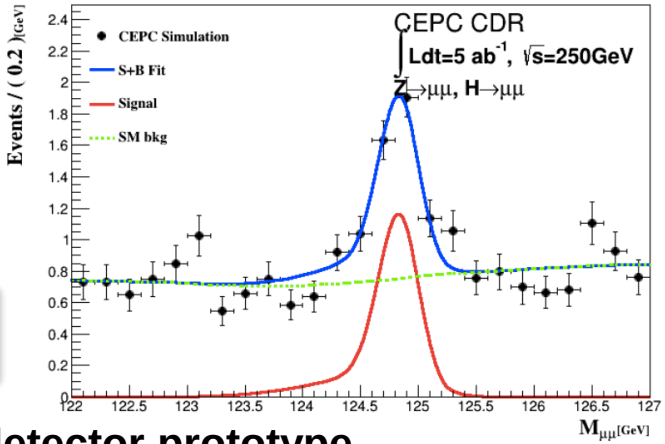
第四届半导体辐射探测器研讨会

2024年5月23-26日

项目背景

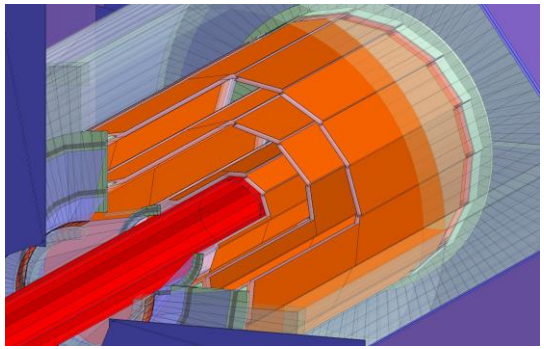
- **Physics motivation**
  - Higgs precision measurement
  - H → bb (precise vertex reconstruction)
  - H → μμ (precise momentum measurement)

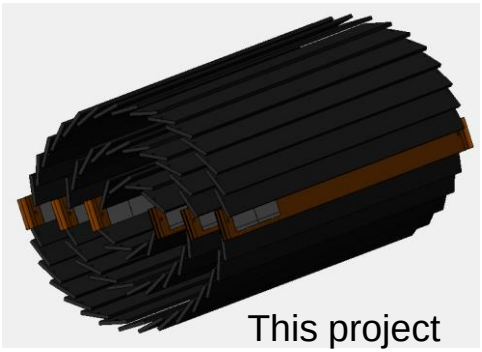


Need tracking detector with high spatial resolution

- **Project MOST2 target: produce the first vertex detector prototype**
  - Spatial resolution 3~5 μm (pixel detector)
  - Radiation hard (> 1 MRad)

CEPC Vertex detector conceptual design (2016)



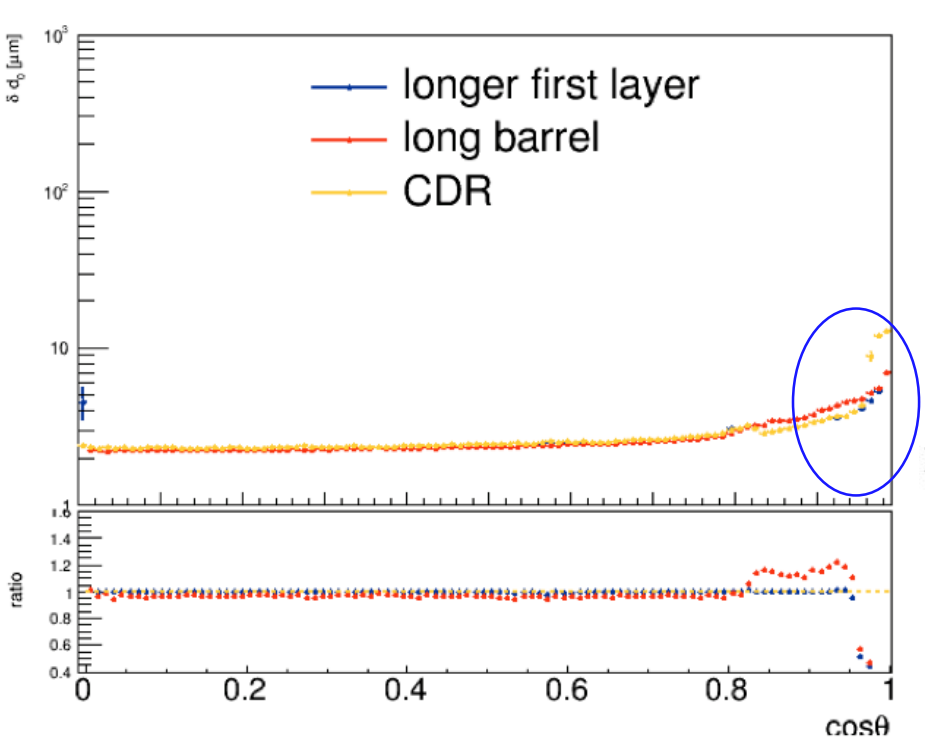


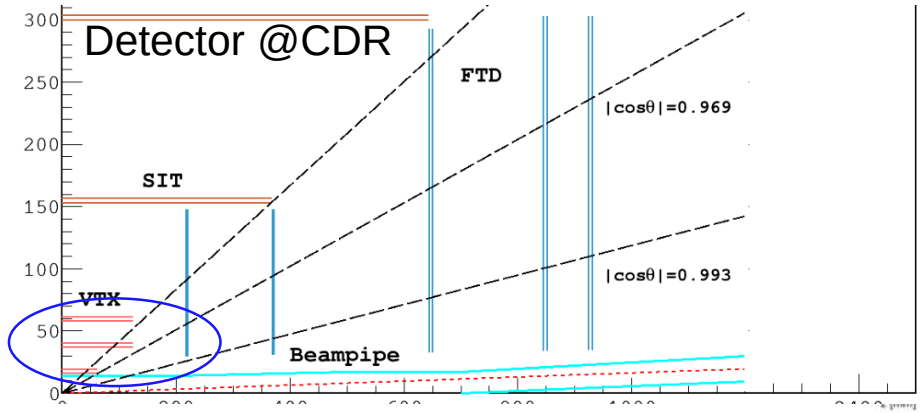
This project
First vertex detector prototype

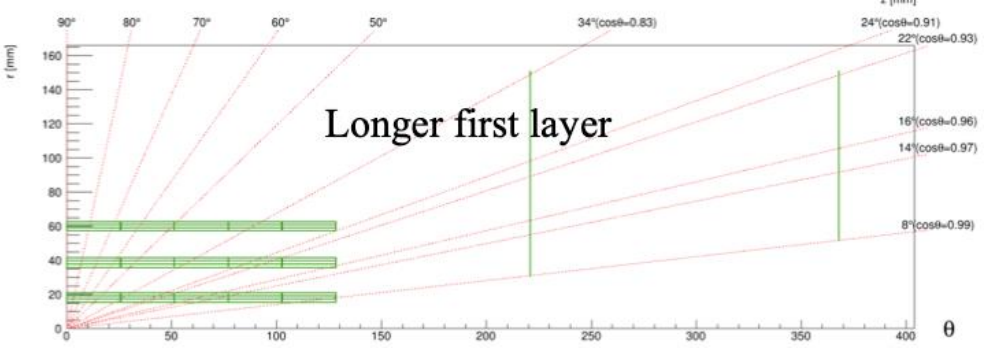
- **Main technology**
  - High spatial resolution technology → design high granularity pixel chip
  - Radiation resistance technology
  - Detector module prototyping and assembly technology

顶点探测器原型样机结构优化

- **Based on CEPC vertex detector conceptual design → Three double-layer barrel detector**
- **One example of detector geometry optimization based on simulation：**
  - Increase the length of the inner layer of the detector
  - To improve the impact parameter resolution for forward tracks

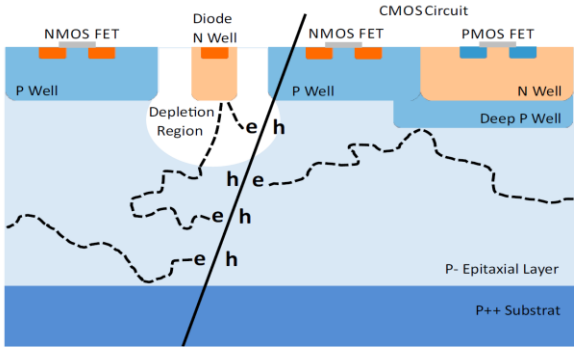




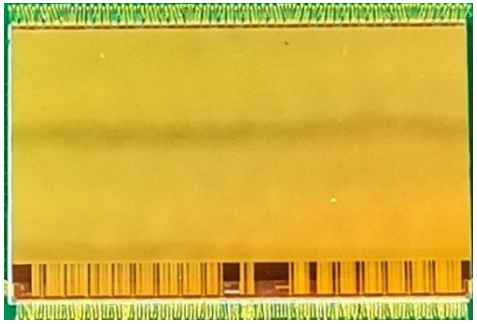


太初芯片概述

- **Motivation: a large-scale & full functionality pixel sensor for the first 6-layer vertex detector prototype**
- **Major challenges for design**
  - Small pixel size → high resolution (3-5 μm)
  - High readout speed (dead time < 500 ns @ 40 MHz) → for CEPC Z pole
  - Radiation tolerance (per year): 1 MRad TID
- **Completed 3 rounds of sensor prototyping in a 180 nm CMOS process**
  - Two MPW chips (5 mm × 5 mm)
    - TaichuPix-1: 2019; TaichuPix-2: 2020 → feasibility and functionality verification
  - 1st engineering run
    - Full-scale chip: TaichuPix-3, received in July 2022 & March 2023

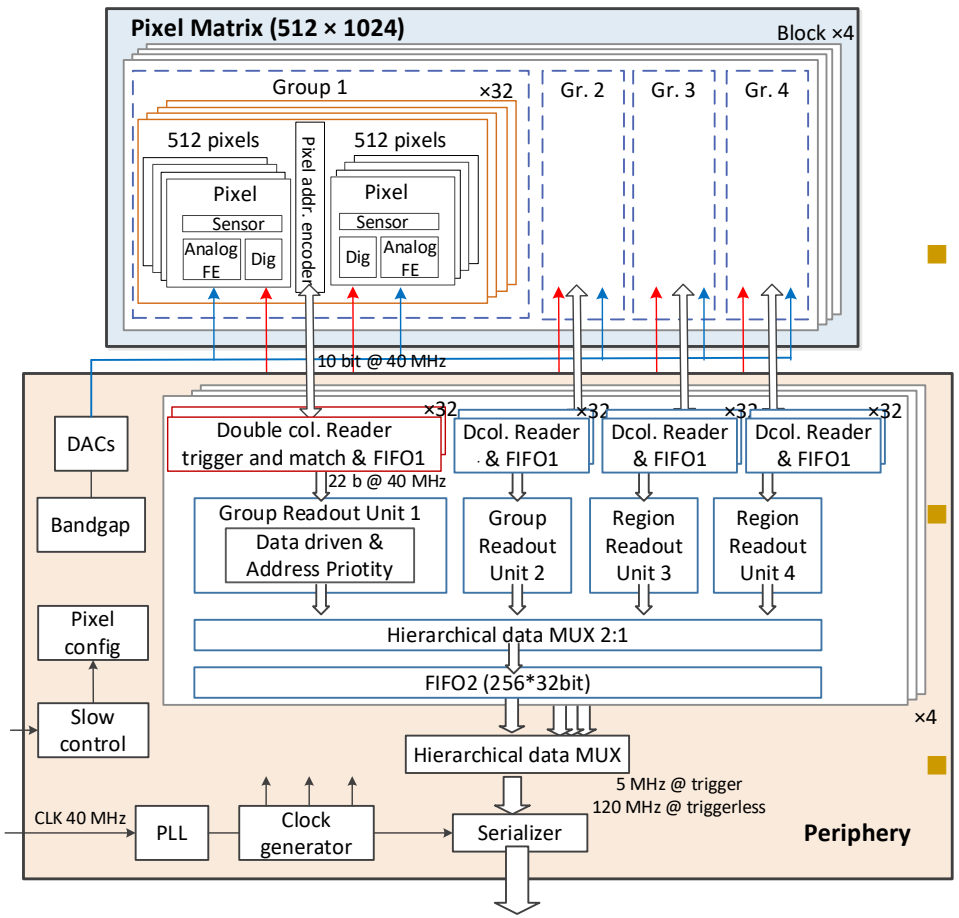


CMOS monolithic pixel sensor



TaichuPix-3
(15.9 × 25.7 mm^2)

芯片结构

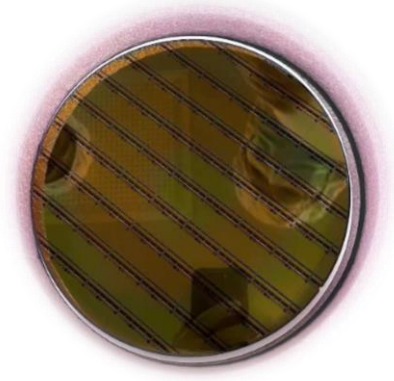


Architecture of the full-scale TaichuPix

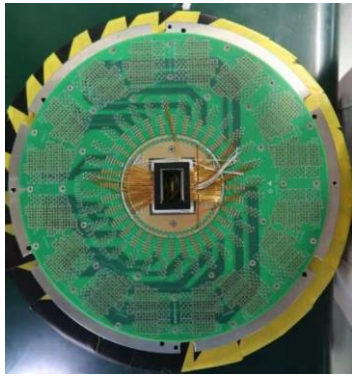
- **Pixel 25 μm × 25 μm**
  - Continuously active front-end, in-pixel discrimination
  - Fast-readout digital, with masking & testing config. logic
- **Column-drain readout for pixel matrix**
  - Priority based data-driven readout
  - Time stamp added at end of column (EOC)
  - Readout time: 50 ns for each pixel
- **2-level FIFO scheme**
  - L1 FIFO: de-randomize the injecting charge
  - L2 FIFO: match the in/out data rate between core and interface
- **Trigger-less & Trigger mode compatible**
  - Trigger-less: 3.84 Gbps data interface
  - Trigger: data coincidence by time stamp, only matched event will be readout
- **Features standalone operation**
  - On-chip bias generation, LDO, slow control, etc.

全尺寸芯片：TaichuPix-3

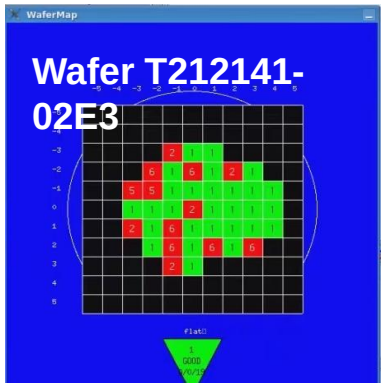
- **12 TaichuPix-3 wafers produced from two rounds**
  - **Wafers tested on probe-station** → chip selecting & yield evaluation



8-inch wafer

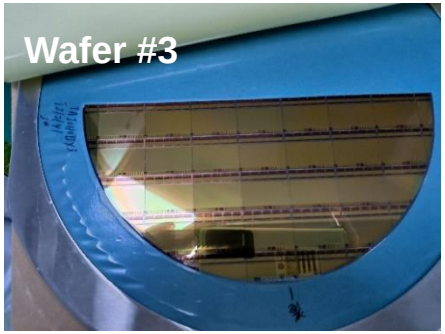


Probe card for wafer test



An example of wafer test result (yield ~67%)

  - **Wafers thinned down to 150 μm and diced**

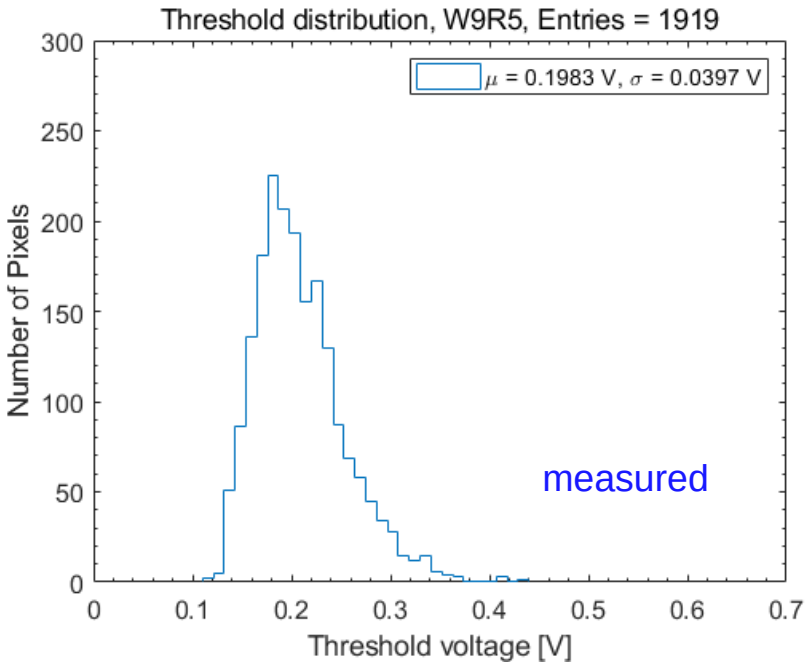


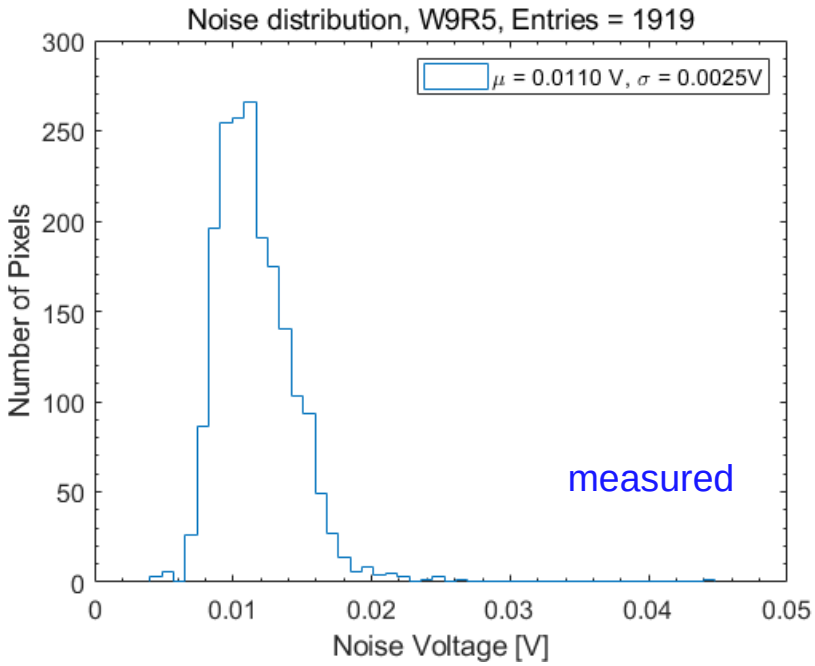
Wafer after thinning and dicing

Thickness after thinning

TaichuPix-3测试结果

- **Pixel threshold and noise were measured with selected pixels**
  - S-curve method was used to test and extract the noise and the threshold
  - Average threshold ~215 e^-, threshold dispersion ~43 e^-, temporal noise ~12 e^- @ nominal bias setting

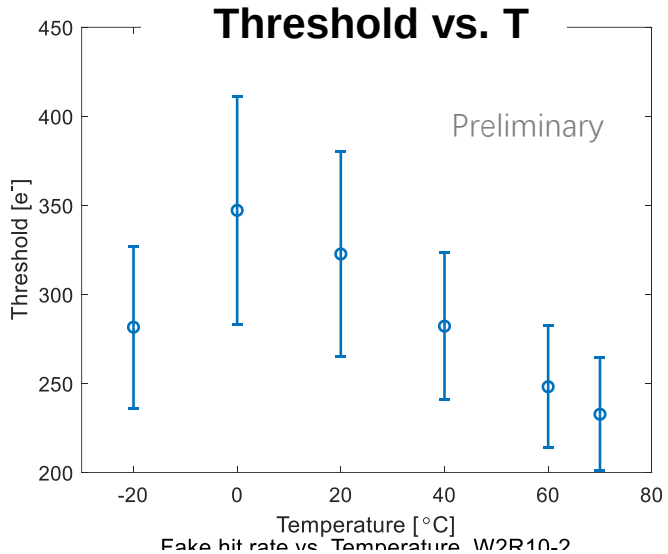


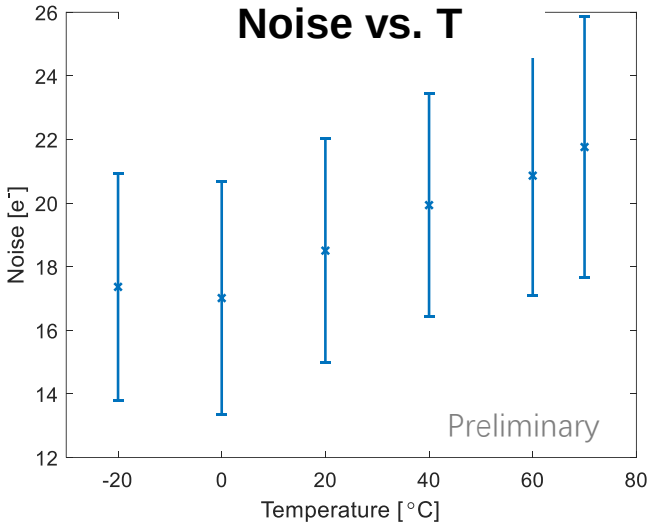


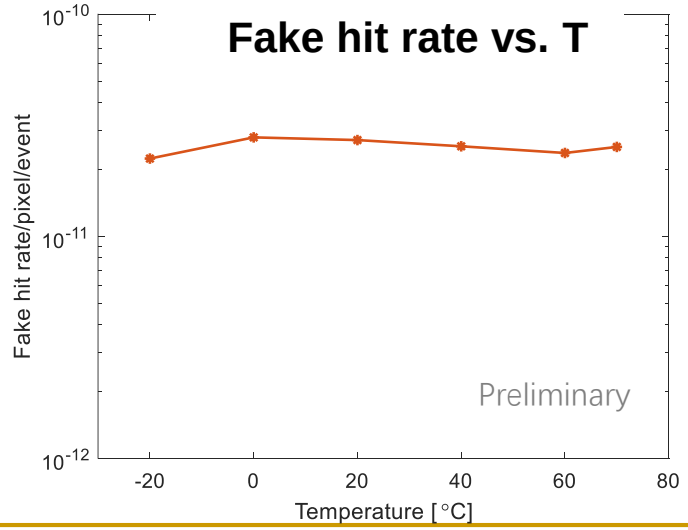
- **Power dissipation of 89 ~ 164 mW/cm^2 tested @ 40MHz clk with different biasing condition**

环境温度对芯片性能的影响

- **Test under a consistent configuration @ different T**



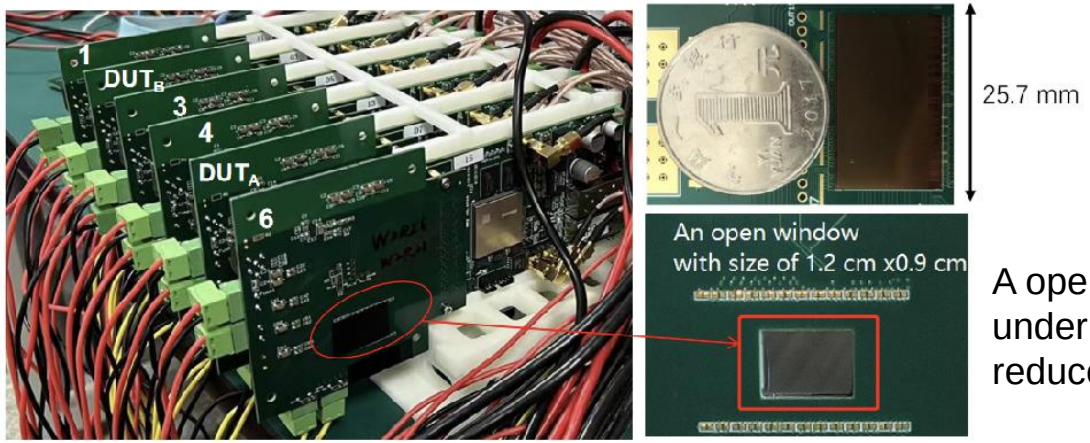




- **TC3 shows a normal functionality @ -20 ~ 70 °C**
- **Main performance (i.e. threshold, noise, fake hit rate) can satisfy the requirements @ -20 ~ 60 °C**
- **Threshold and noise fluctuate with T, probably attribute to the fluctuation of pixel biasing**

TaichuPix-3 望远镜

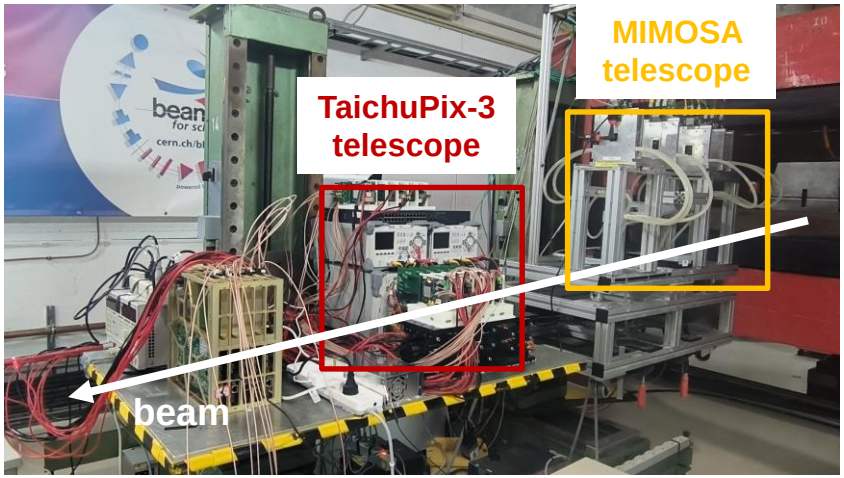
- **The 6-layer of TaichuPix-3 telescope built**
  - Each layer consists of a TaichuPix-3 bonding board and a FPGA readout board



A open window on PCB under TC3 chip to reduce multi-scattering

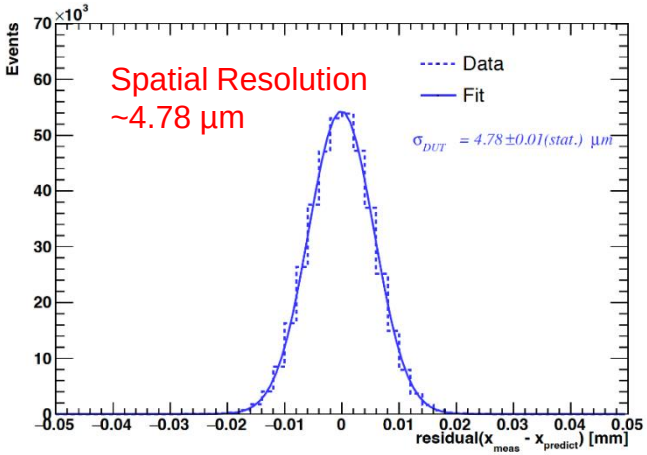
6-layer TaichuPix-3 telescope

- **Setup in the DESY testbeam**
  - TaichuPix-3 telescope in the middle
  - Beam energy: 4 GeV mainly used
  - Tests performed for different DUT (Detector Under Test)

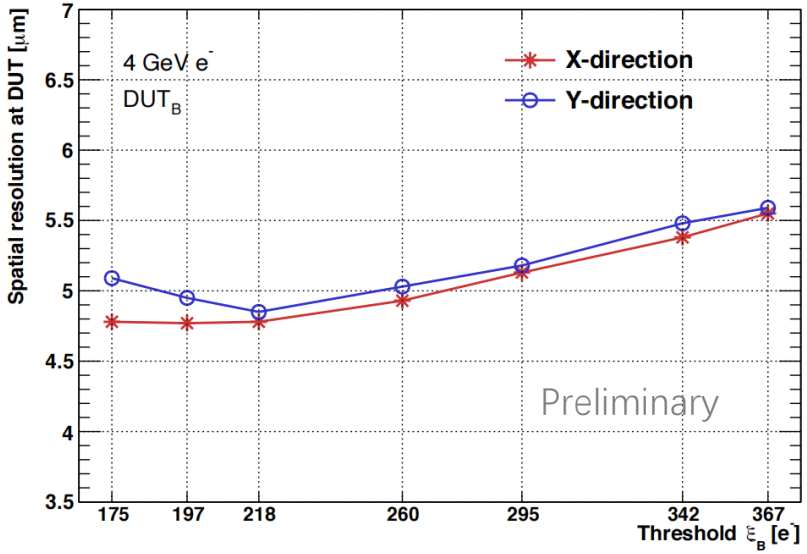


TaichuPix-3 芯片束流测试结果

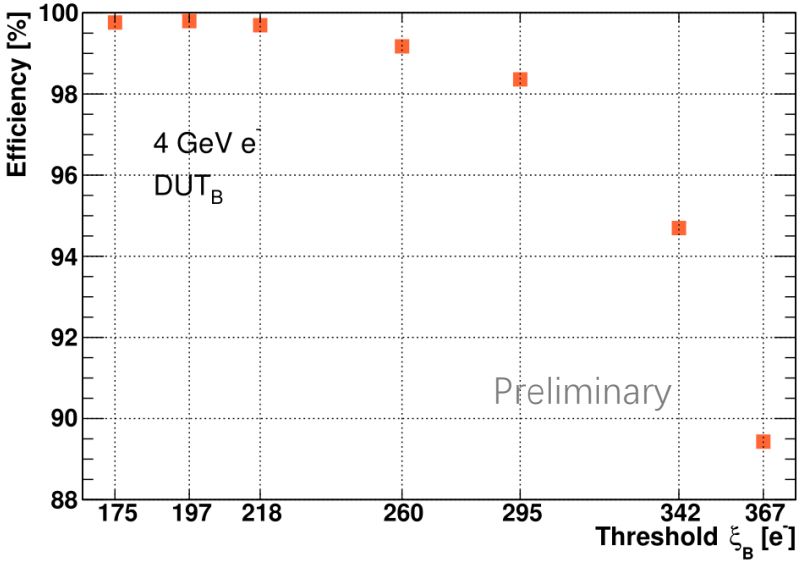
- **Spatial resolution**
  - Gets better when decrease the pixel threshold, due to the increased cluster size
  - A resolution < 5 μm achieved, best resolution is 4.78 μm
- **Detector efficiency**
  - Decreases with increasing the threshold, detection efficiency >99.5% at threshold with best resolution



Distribution of residual X



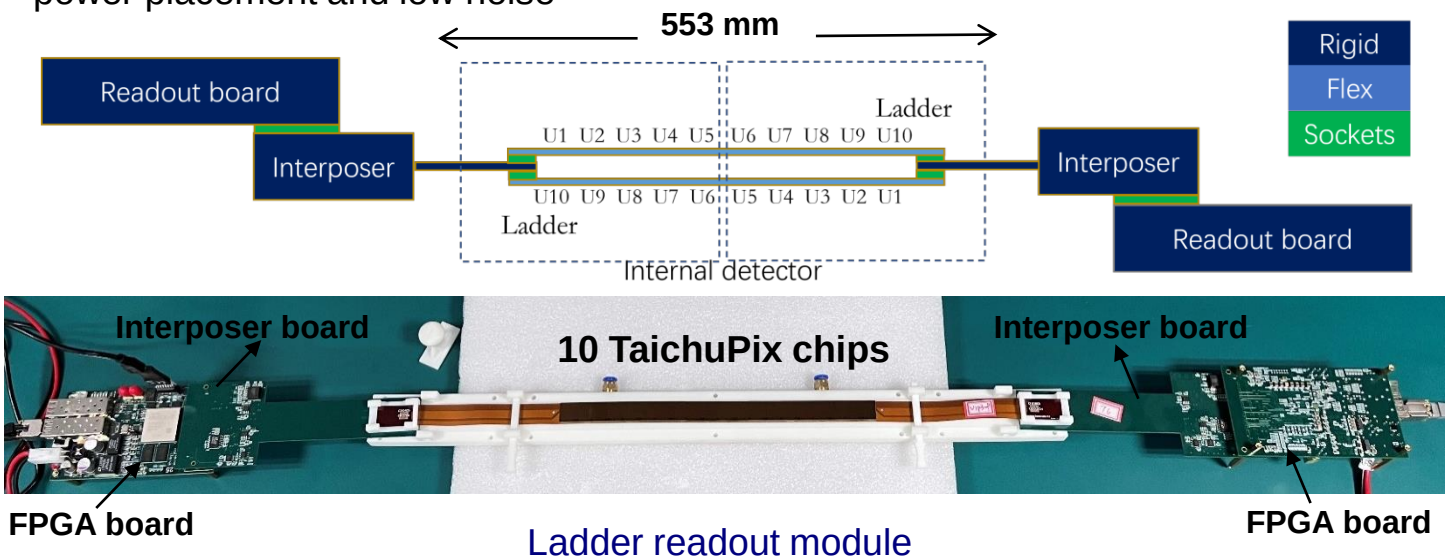
Spatial resolution vs. pixel threshold



Detection efficiency vs. pixel threshold

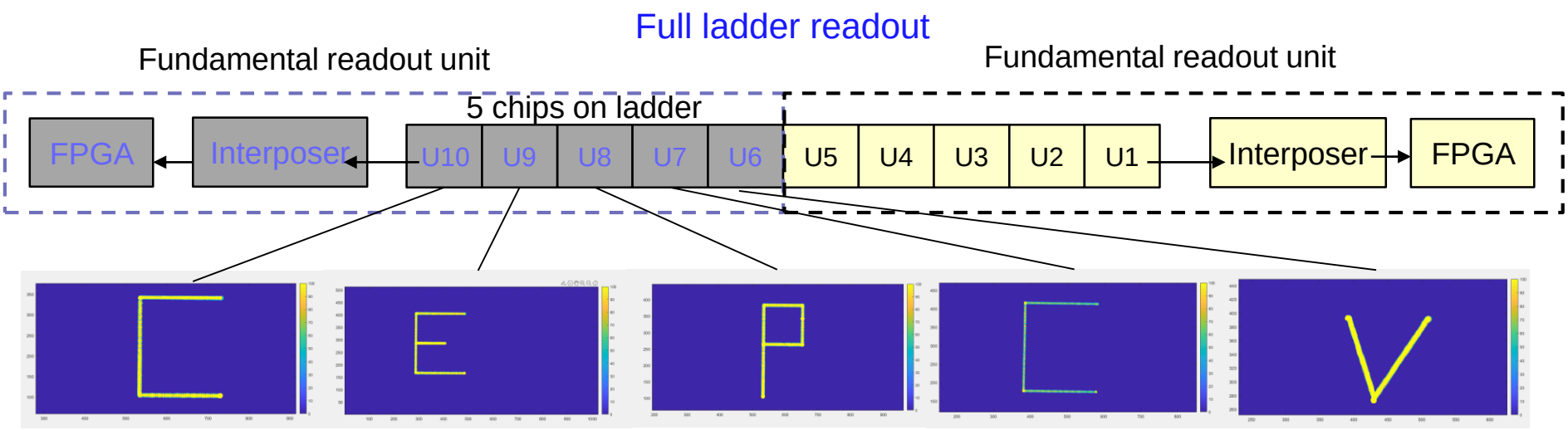
样机模块（Ladder）读出设计

- **Detector module (ladder) = 10 sensors + readout board + support structure + control board**
  - Sensors are glued and wire bonded to the flexible PCB, supported by carbon fiber support
  - Signal, clock, control, power, ground will be handled by control board through flexible PCB
- **Challenges**
  - Long flex cable → hard to assemble & some issue with power distribution and delay
  - Limited space for power and ground placement → bad isolation between signals
- **Solutions**
  - Read out from both ends, readout system composes of three parts, careful design on power placement and low noise



Ladder readout module

Ladder功能测试



Laser tests on 5 Taichupix chip on a full ladder
("CEPCV" pattern by scanning laser on different chips on ladder)

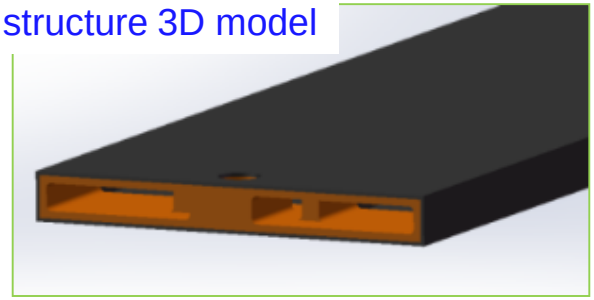
- **A full ladder includes two identical fundamental readout units**
  - Each contains 5 TaichuPix chips, a interposer board, a FPGA readout board

- **Functionality of a full ladder fundamental readout unit was verified**
  - Configuring 5 chips in the same unit
  - Scanning a laser spot on the different chips with a step of 50 μm, clear and correct letter imaging observed
  - **Demonstrating 5 chips working together → one ladder readout unit working**

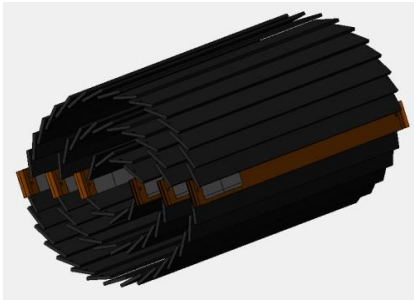
支撑结构及样机装配

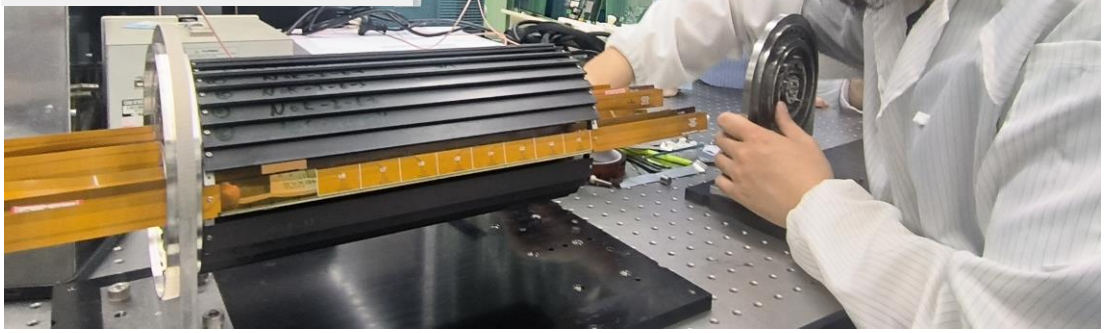
- **Fabricated support structure prototype of the ladder (IHEP designed)**
  - 3 layers of carbon fiber, 0.12 mm thick
- **Both sides of ladder have wire-bonding on chip → Challenging**
- **Six double-side ladders installed on the vertex detector prototype**
  - 12 flex boards , 24 TaichuPix-3 chips installed on detector prototype

Ladder support structure 3D model



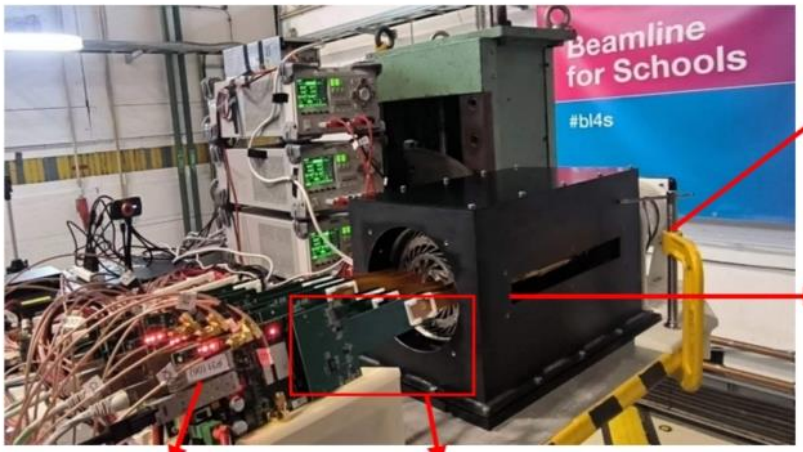
Fabricated ladder support

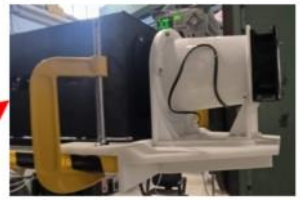


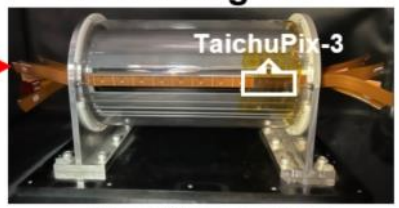


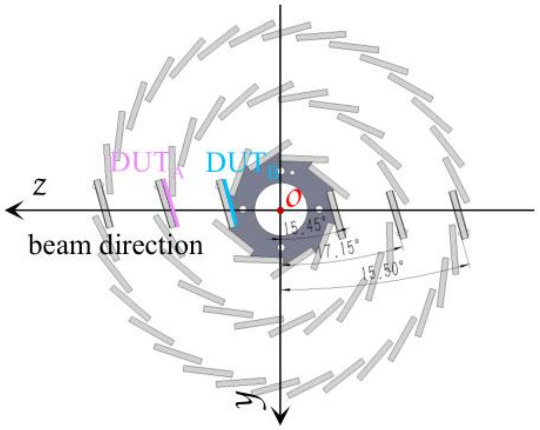
原型样机束流测试

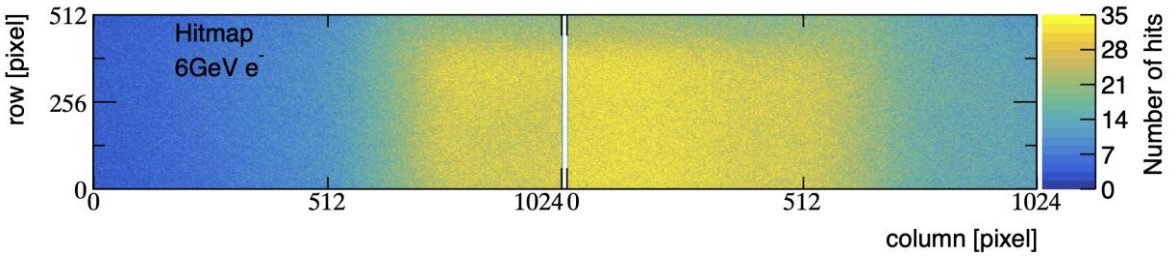
- **Beam test performed at DESY to evaluate the mechanical, electrical and DAQ**
  - The prototype placed within a black box, with an electric fan for cooling

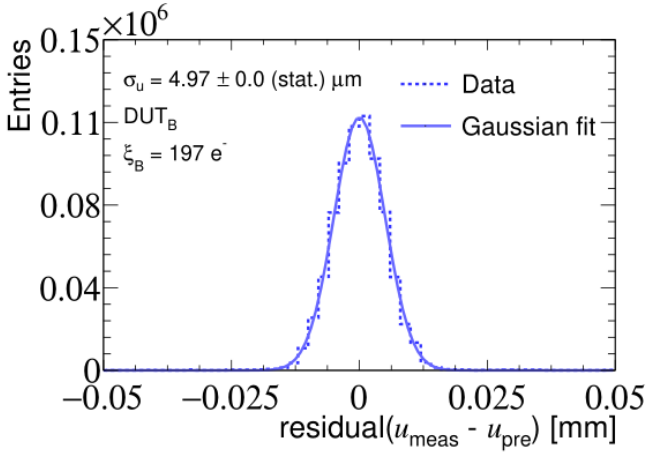



Air cooling fan







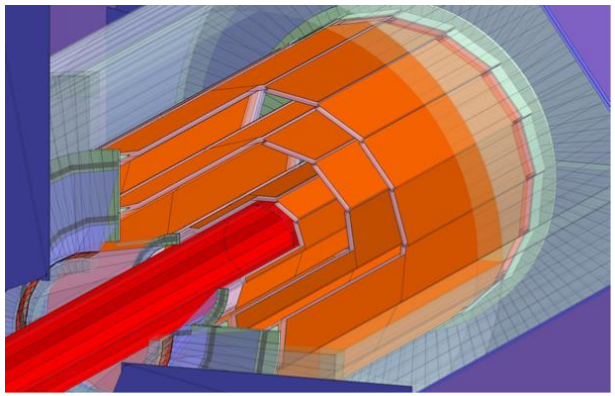


The readout electronics and DAQ system remained stable during the test, the best resolution of 4.97 µm achieved

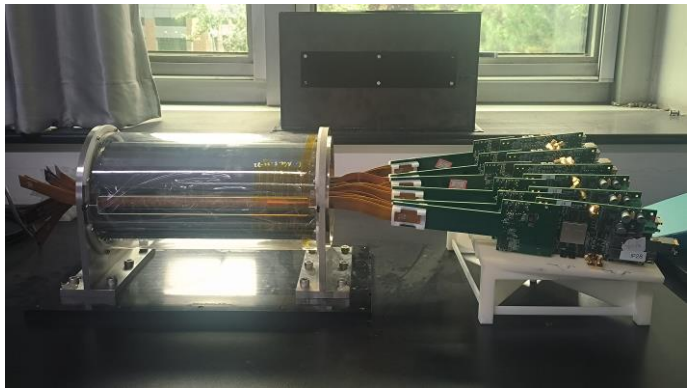
Detailed results in DOI: 10.1109/TNS.2024.3395022

总结与展望

- **First pixel detector prototype developed for CEPC VTX R&D**
  - Monolithic active pixel sensor prototype, TaichuPix chips, developed
  - Detector module prototyping and assembly completed
  - Spatial resolution better than 5 μm achieved for chip-level and detector-level



Concept (2016)



1st Vertex detector prototype (2023)

- **Outlook**
  - Proposed to design new pixel sensor chips in a 65 nm technology
  - Proposed a new ladder design integrated with the optical link

Thank you very much for your attention !