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Test of CMOS chip using 55nm process

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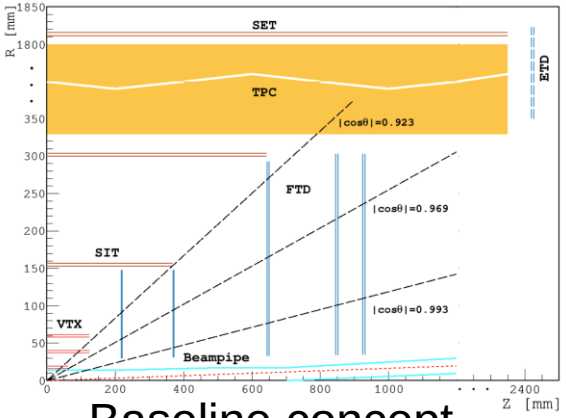
CMOS SENSOR IN FIFTY-FIVE NM PROCESS

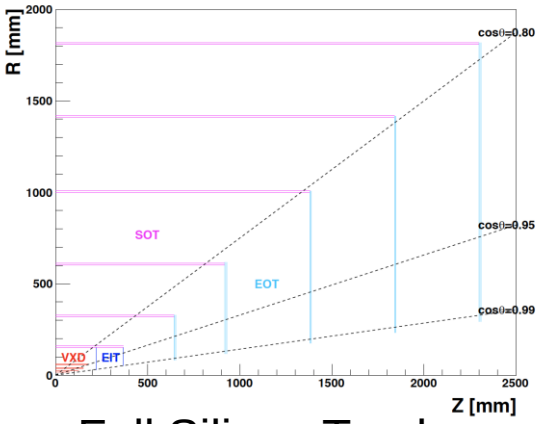
CEPC silicon tracker

- Large area silicon tracker planned
  - ~70 – 140 m^2 depending on detector concept
- Good spatial resolution
- CMOS is a high-performant and cost-effective solution

- Yet more technology options possible compared with vertex detector
  - More tolerant on power consumption
  - ~10um resolution → increased pixel size



Baseline concept



Full Silicon Tracker

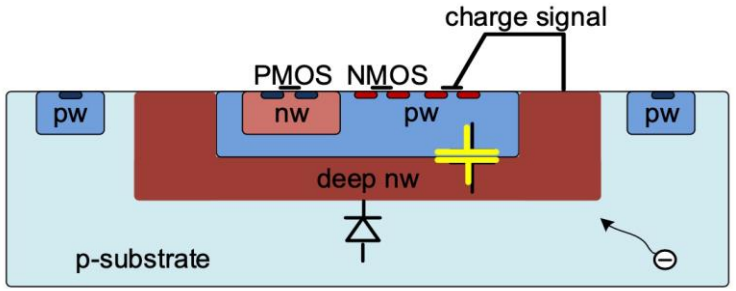
$$\sigma_{1/p_T} = a \oplus \frac{b}{p \sin^{3/2}\theta} \quad [\mathrm{GeV}^{-1}]$$

$a \sim 2 \times 10^{-5}\,\mathrm{GeV}^{-1}$

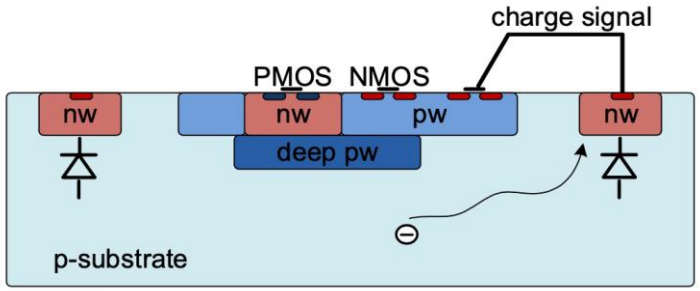
$b \sim 1 \times 10^{-3}$

HVCMOS

- HVCMOS is commercially available process
  - Intrinsically radiation hard
  - Large capacitance → potentially more noise and power
  - Hard for vertex detector but no showstopper for tracker



High Voltage CMOS



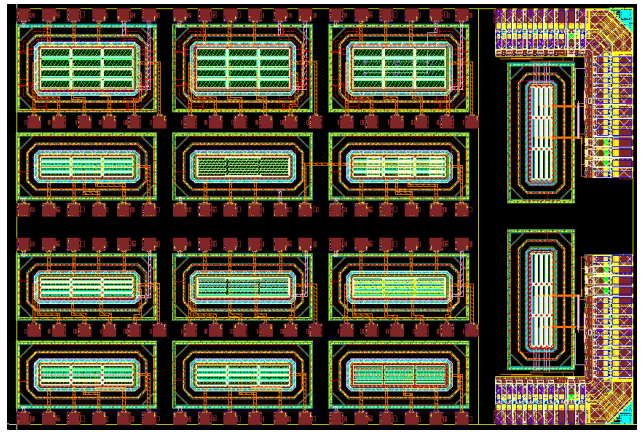
CMOS with small electrode

- Stable supply from the foundry should also be considered
- Efforts formed in search of HVCMOS process with 55/65 nm process provided by a domestic foundry since a couple of years ago
  - SMIC 55nm (non-HV): MPW in Oct 2022 to verify the DNW structure
  - SMIC 55nm HV: MPW in Aug 2023 with high resistivity wafer

MPW (CMOS SENSOR IN FIFTY-FIVE NM PROCESS)

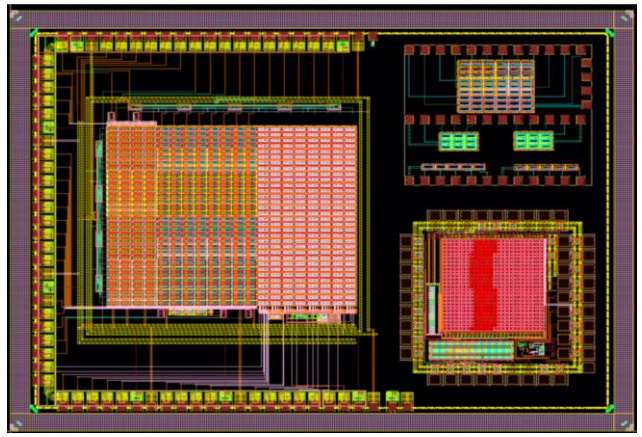
- COFFEE1 in Oct 2022 with SMIC 55nm Low Leakage process
  - No HV application, similar DNW structure
  - Pixel: 25×150 um^2 ~ 50×150 um^2
  - Variation of passive diode arrays
  - Simple amplifier added

$2 \times 3\ \mathrm{mm}^2$



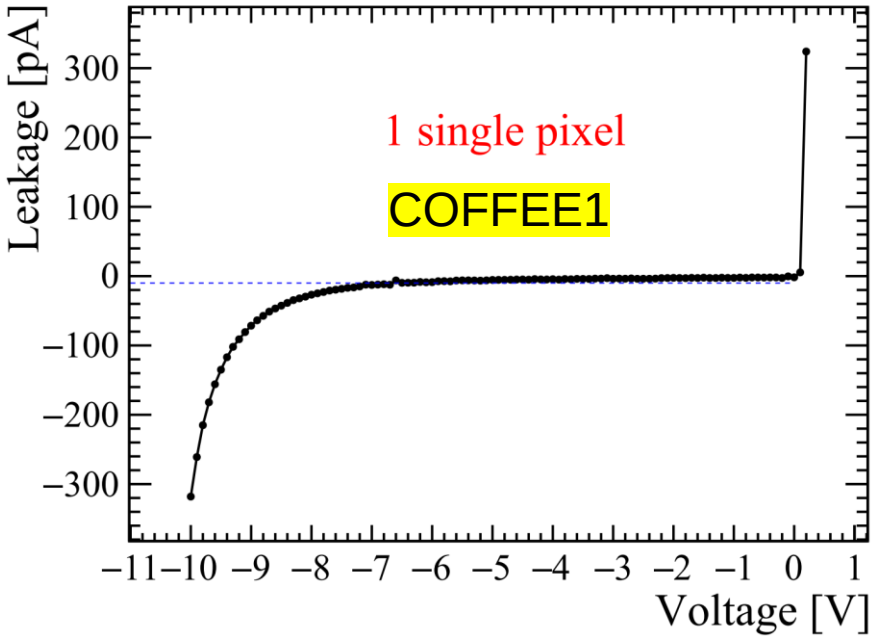
- COFFEE2 in Aug 2023 with SMIC 55nm HV process
  - Validation of the sensor with high resistance wafer of $1\mathrm{k}\Omega \cdot \mathrm{cm}$
  - Variation of diode structures
  - Analog amplifier and switch circuit
  - Test structure for small digital circuit

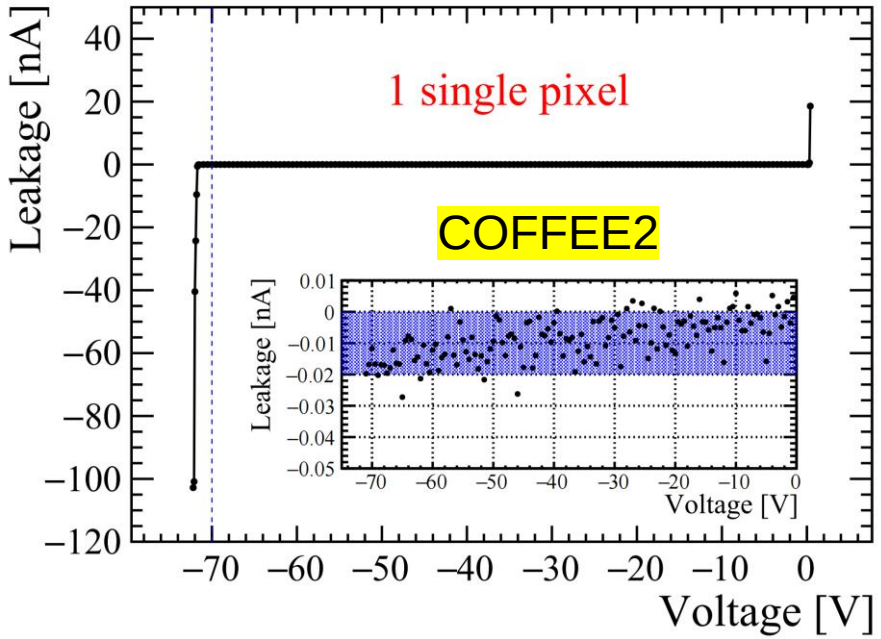
$3 \times 4\ \mathrm{mm}^2$



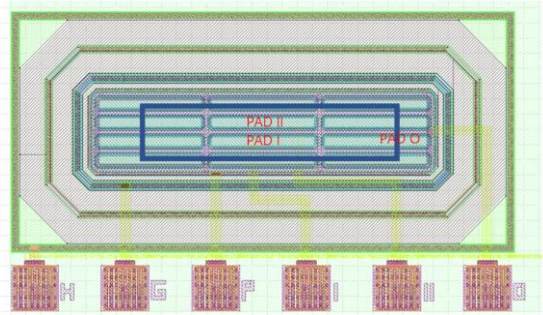
Typical IV

- IV test shows good diode result for all pixel structures
  - Clear positive conduction
  - Leakage is small ~ 10 pA for both COFFEE1 and COFFEE2
  - Reverse breakdown occurs above -70V for COFFEE2



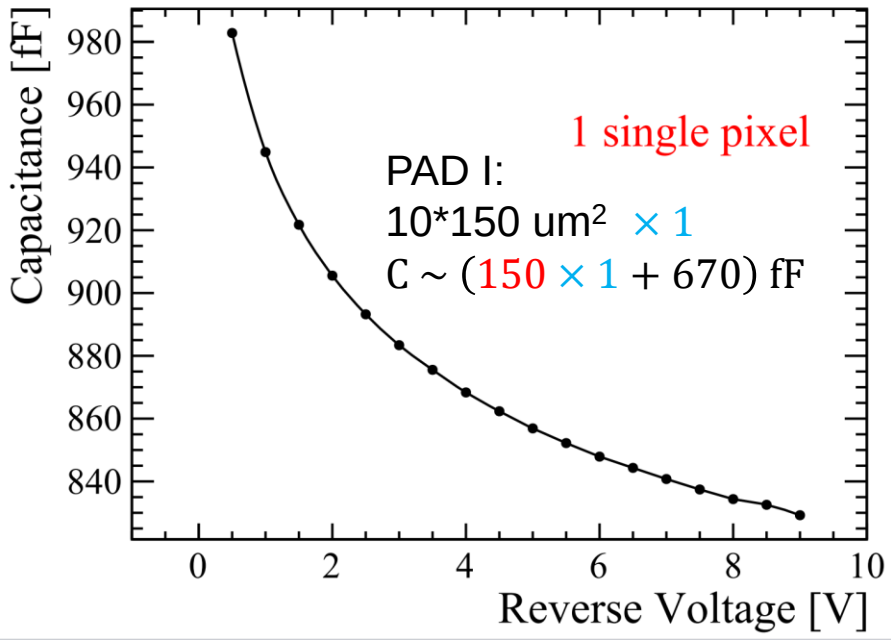


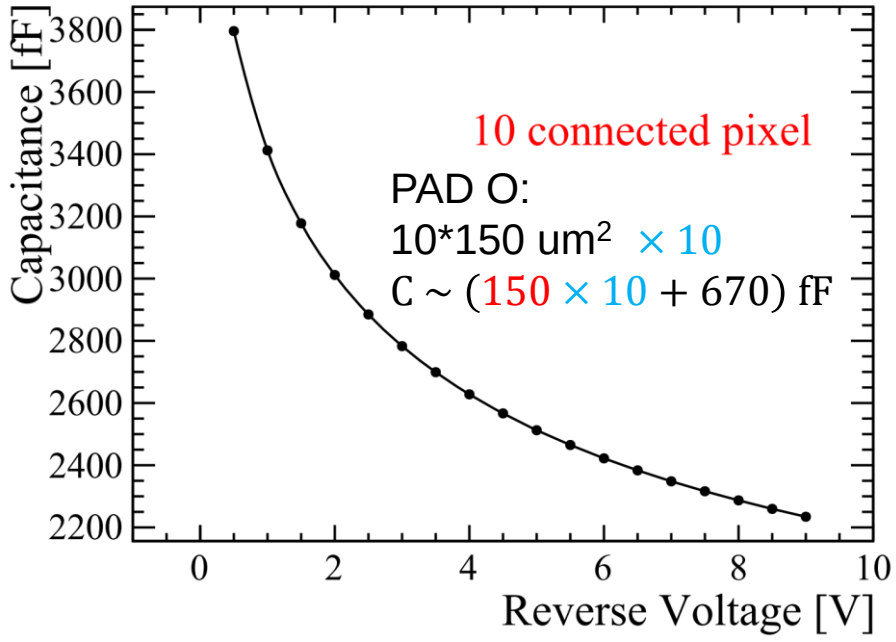
CV results (COFFEE1)



- CV test results are comparable for different diode design:
  - Consider the offset is around 670 fF, C is proportional to parallel number
  - For single small pixel, test are compatible with predictions ~ 150-200 fF

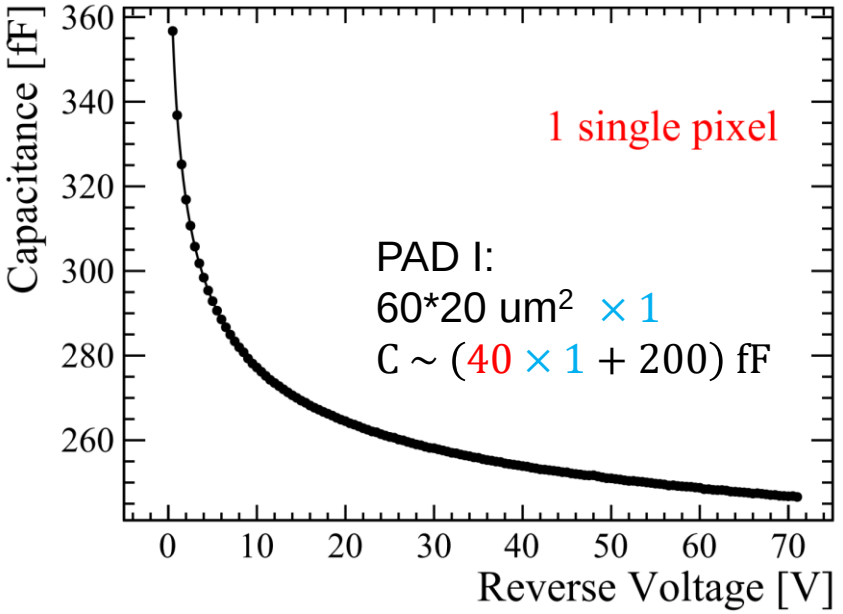
COFFEE1

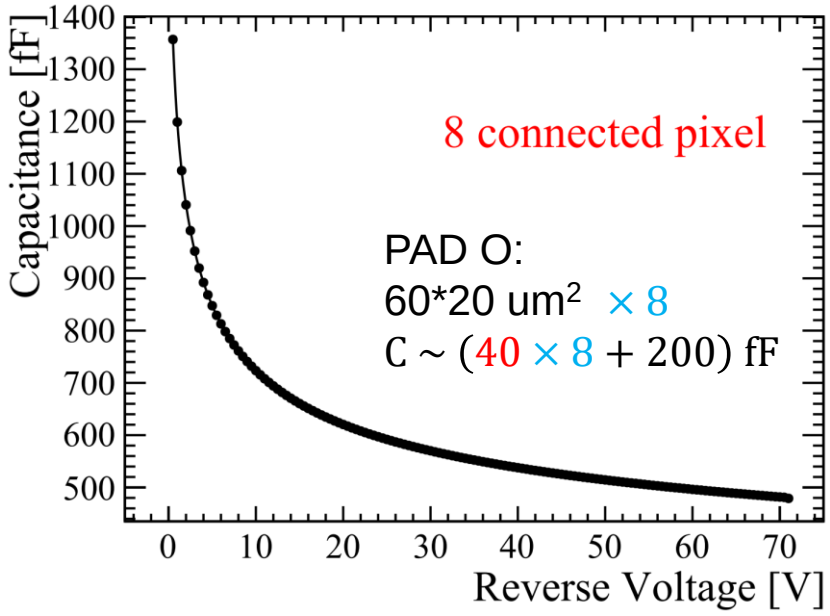


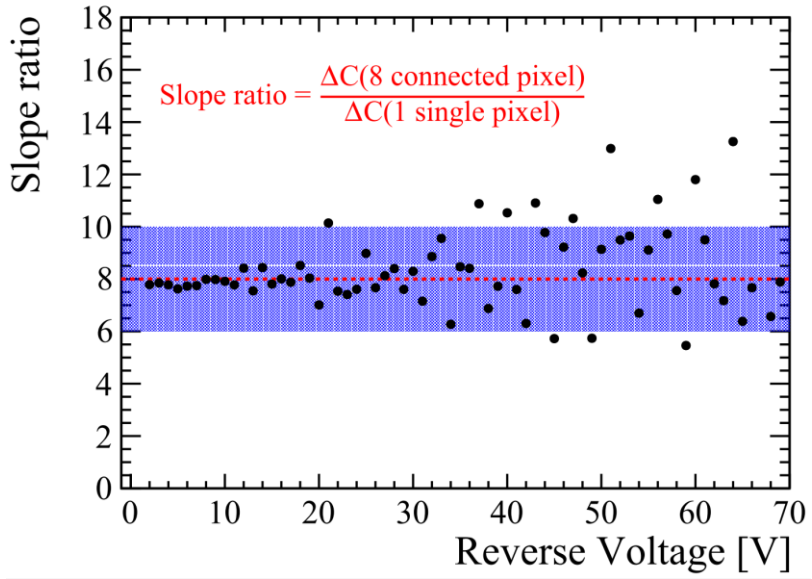


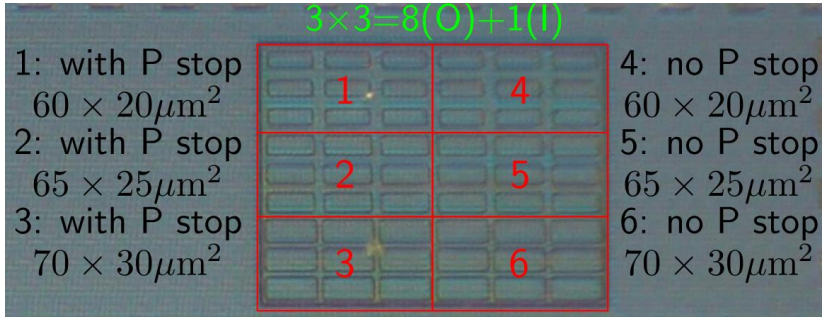
CV results (COFFEE2)

- C variation shows good parallel ratio
- Offset around 200fF, consistent with simulation
- Single pixel ~ 40fF

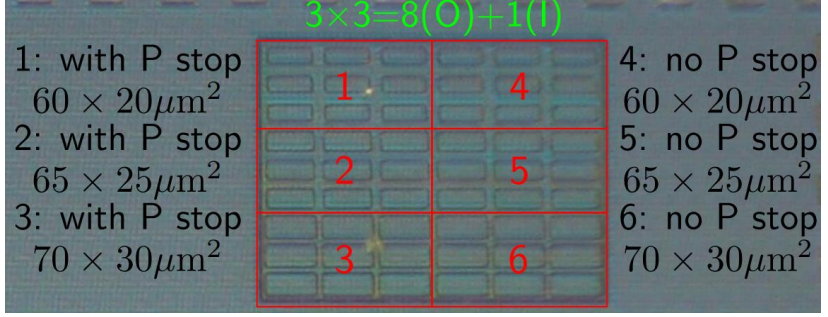




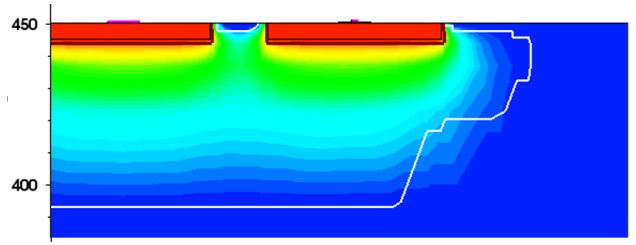


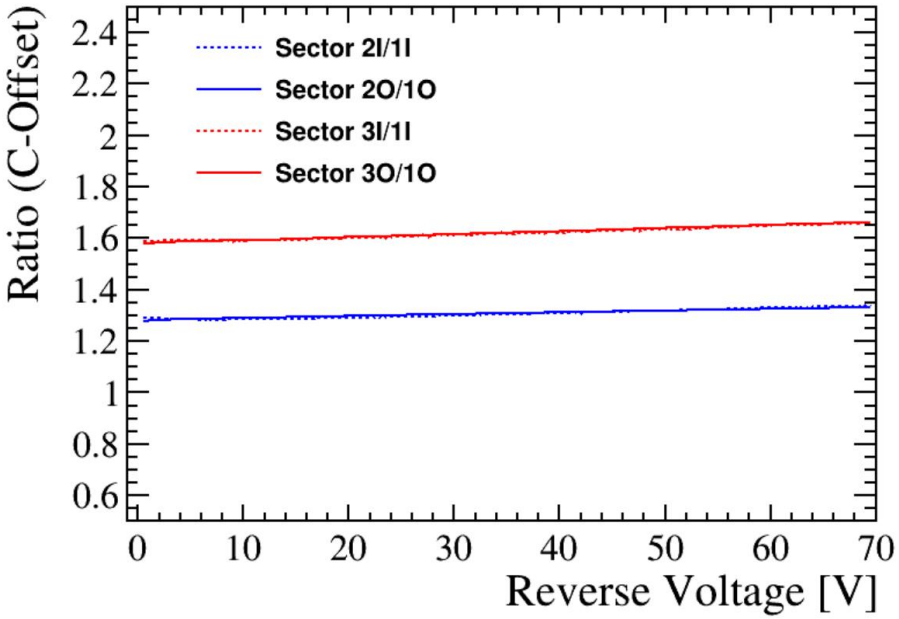


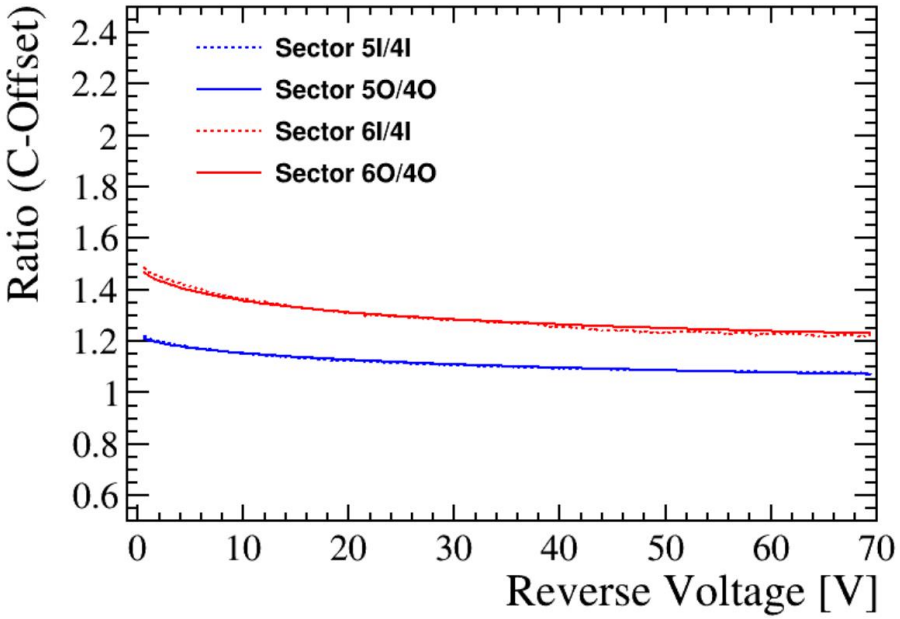
CV results (COFFEE2)



- Pixel area ratio for S2(5)/S1(4)=1.35, S3(6)/S1(4)=1.75
- Subtract offset, C ∝ area for Sector 1/2/3 due to p-stop

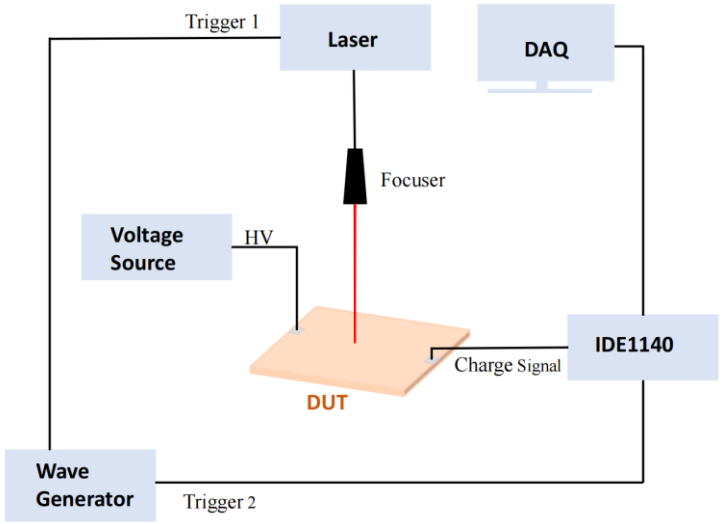


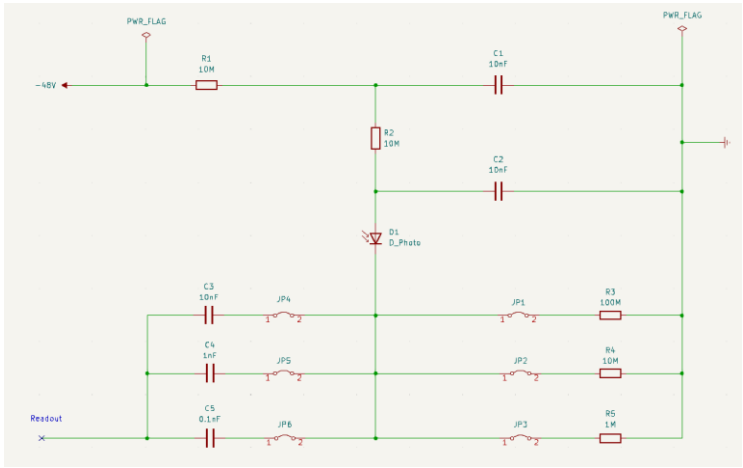


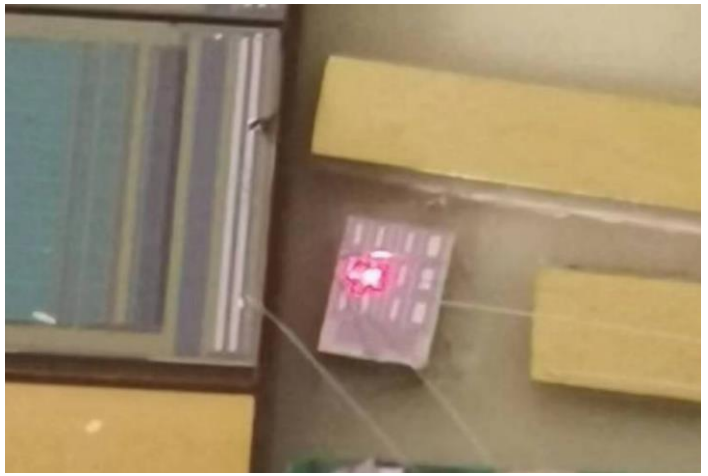


Laser test (COFFEE1)

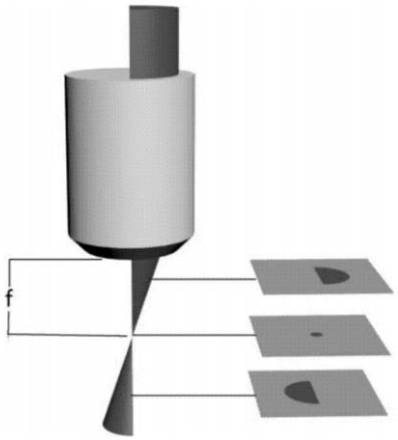
- Signal source: 650nm red laser, penetration depth <10 um
- Low pass filter connected to source meter, large ground resistor to sample signal charge, AC readout
- Frame rate capability >10 kHz, test under 500Hz



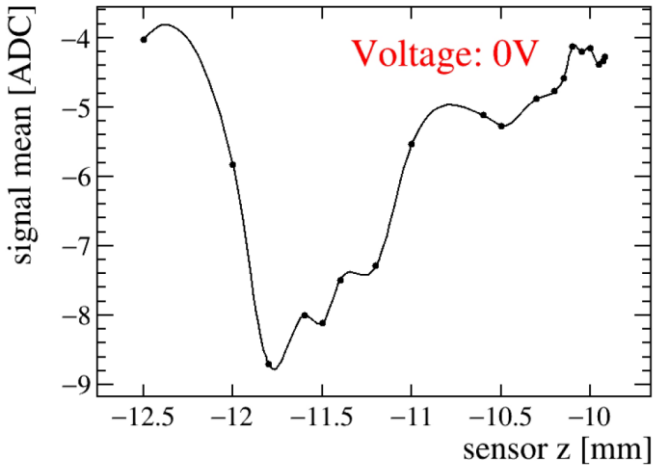


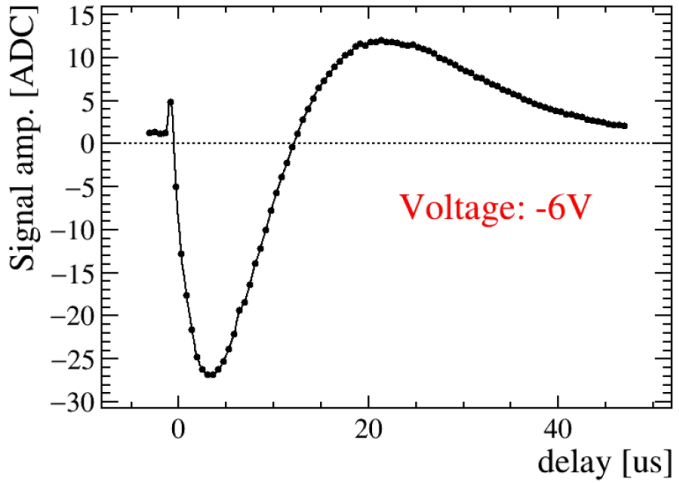


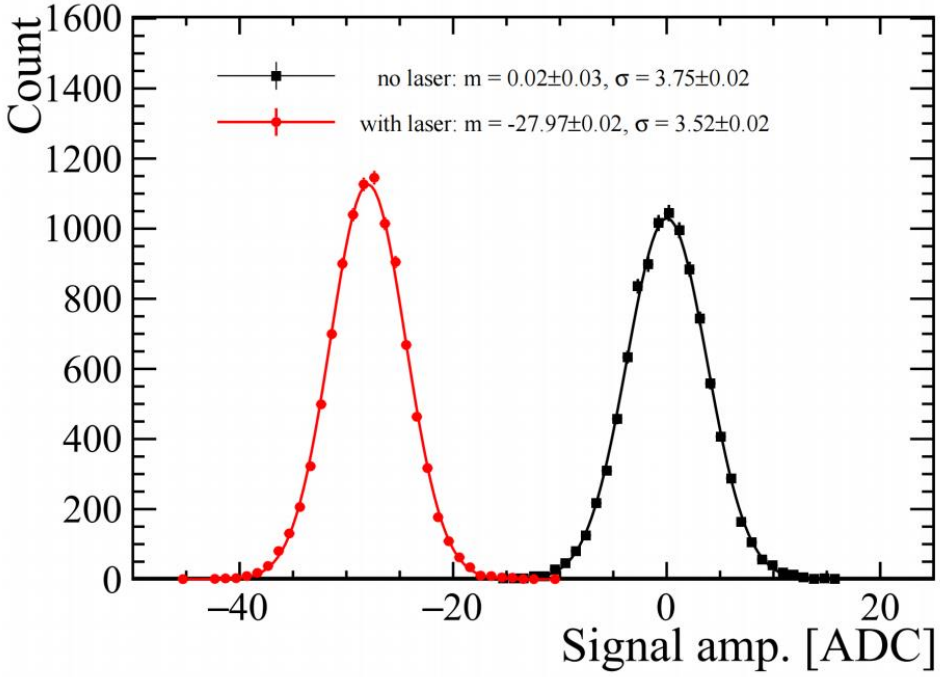
Laser test (COFFEE1)



- Clear signal with laser emitting
- After spatial and time-delay scans, max signal in -28 ADC
  - Corresponding to 0.38 fC (2400 e) have collected from pixels







Conclusion

- HVCMOS is a promising technology for silicon tracker
  - Tested 2 MPW for different design
- Test results verified the rationality of the diode design
  - Low leakage ~ 10 pA
  - Reverse breakdown at 8V for COFFEE1 and > 70V for COFFEE2
  - CV results consistent with TCAD simulation
  - For COFFEE1 found signal with laser test
- More test ongoing
  - COFFEE2 test with radiation source, irradiation test, circuit testing